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Review

A Survey of Ultra-Low-Power Amplifiers for Internet of Things Nodes

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Abstract: This paper investigates CMOS operational transconductance amplifier (OTA) design methodologies suitable for Internet of Things nodes. The use of MOS transistors in the subthreshold of the body terminal for signal input or bias, as well as newer inverter- and digital-based techniques, is considered. Solutions from the authors' work are utilized as main case examples. State-of-the-art ultra-low-power OTAs are then thoroughly compared using a data-driven approach. According to the findings, digital- and inverter-based solutions have the lowest area occupation and superior small-signal performance but are inherently susceptible to process, supply, and temperature (PVT) variations. The only "analog" approach suitable for a sub-0.6 V supply is body driving in conjunction with subthreshold bias. It offers competitive large-signal performance and, more importantly, is less sensitive to PVT variations at the expense of silicon area.

Keywords: bulk-driven; low-voltage; operational transconductance amplifiers; subthreshold; ultra-low-power design

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1. Introduction

The Internet of Things (IoT) has wide-ranging potential applications with expected significant impacts across various industries, including agriculture, healthcare, automotive, and industrial manufacturing. A conservative projection estimates that the number of interconnected IoT devices will reach approximately 29 billion by 2030 from 9.7 billion in 2020, indicating a substantial growth in the use of this technology in the coming years [1].

Among the most important characteristics of IoT nodes are computing, wireless communication, and sensor capabilities [2]. Indeed, IoT node implementation requires circuits that connect the digital processing domain with physical signals received from the analog world via sensors such as temperature, CO_2, light, humidity, displacement, pressure, and acceleration. As a result, analog interfaces are critical elements in the IoT paradigm [3] because IoT nodes are commonly wireless and energy-autonomous and hence have a very limited power budget that often relies on small primary batteries or area-constrained energy harvesters, with the optional support of secondary batteries. As a result, there is an urgent need to heavily reduce the power consumption of digital cores and analog frontends, and, for this purpose, efficient IoT nodes must exploit ultra-low-voltage design techniques with an operating voltage of 1 V or less. Furthermore, the utilization of sub-100 nm CMOS technologies is required to improve the power-delay product of digital circuits, which constitute the bulk of an IoT device [2]. However, the scaling of CMOS technology, the low supply voltage available, and the limited allowed power consumption lead to deleterious effects in the analog domain, such as a drop in output resistance, dynamic range, and signal-to-noise ratio. Consequently, designing the analog front end becomes a challenging task that can seriously impact the overall IoT node performance [4].

In this framework, the operational transconductance amplifier (OTA) is one of the fundamental building blocks of the analog front end. Various design techniques are today avail-

able to enable efficient OTA performance at low power, including weak inversion (or subthreshold) operation [5–11], bulk-driving (or body-driving) [12–30], body-biasing [31–33], inverter-based [34–43], and fully digital approaches [44–51]. Floating-gate and quasi-floating-gate techniques can also be mentioned [52,53]. However, the latter ones employ custom transistors that are not included in commercial design kits. In addition, the temperature dependence of the pseudo-resistor adopted (not adequately modeled in CAD tools) limits the use of this approach. Furthermore, a relevant limitation is leakage currents, which can make this technique unfeasible in sub-100 nm CMOS processes. As a result, we will not investigate floating-gate and quasi-floating-gate transistor solutions by limiting our analysis to techniques appropriate for conventional CMOS technologies and acceptable by the industry standards.

The aim of this paper is hence to review the main design techniques suitable for ultra-low-power, ultra-low-voltage OTAs, highlighting their advantages and trade-offs. In this field, the authors have decades of expertise and have devised several solutions, some of which will be discussed in the next sections and will be chosen as design examples. A data-driven analysis of the state of the art is also performed to offer the designer some guidance for selecting the best OTA solution based on the specified design parameters and system needs.

The paper is organized as follows. Sections 2–6 provide a succinct examination of the working principles of the CMOS subthreshold, body-driving, body-biasing, inverter-based, and digital techniques, as well as selected example designs. Section 7 compares the key solutions acquired from the state of the art and that exploit the preceding methodologies. A quantitative, data-driven comparison is performed by considering the primary performance parameters and evaluating specific figures of merit often used in the literature. Section 8 summarizes the authors' conclusions.

2. Subthreshold Approach

Operating transistors in the weak inversion (or subthreshold, SUB) region has been the primary technique for low-voltage and low-power analog design in MOS technology since the 1970s [5].

It is worth noting that in the subthreshold, the saturation condition is reached when $V_{DS} \cong 4\ V_T$, where V_T is the thermal voltage. In this region, an exponential behavior between the drain current and the gate-source voltage is found. The second column of Table 1 shows the small-signal parameters of a gate-driven n-MOS transistor operating in the subthreshold region and in saturation. A bipolar-like behavior is apparent from the linear dependence of the transconductance g_m on the drain current I_D (1a). Subthreshold devices also show the highest transconductance efficiency (g_m/I_D) [4], while the intrinsic voltage gain, A_v, = g_m/g_{ds}, is equal to the reciprocal of $n\lambda V_T$ (which is strictly related to the channel length), resulting in a minimization of distortion [6].

Table 1. Small-signal parameters of an N-channel MOS transistor (saturation region).

	Subthreshold		**Above Threshold Bulk-Driven**	
$g_m = \frac{\partial I_D}{\partial V_{GS}}$	$\frac{I_D}{nV_T}$	(1a)	$\sqrt{\frac{2KWI_D}{L}}$	(1b)
$g_{mb} = \frac{\partial I_D}{\partial V_{BS}}$	$\lambda_B g_m$	(2a)	$\frac{C_{BC}}{C_{GC}} g_m$	(2b)
$g_{ds} = \frac{\partial I_D}{\partial V_{DS}}$	λI_D	(3a)	λI_D	(3b)
f_T	$\frac{g_m}{2\pi(C_{GS}+C_{GD}+C_{GB})}$	(4a)	$\frac{g_{mb}}{2\pi(C_{SB}+C_{DB}+C_{b-sub})}$	(4b)

g_m: gate-source transconductance, g_{mb}: body-source transconductance, g_{ds}: drain-source conductance, f_T: transition frequency, I_D: drain current; W: transistor channel width, L: transistor channel length, V_T: thermal voltage, n: subthreshold slope, μ_n: electron mobility, C_{OX} specific gate capacitance, $K = \mu_n C_{OX}$: transconductance factor, λ_B: body effect coefficient, λ: channel-length modulation coefficient, C_{GS}: gate-to-source capacitance; C_{GD}: gate-to-drain capacitance; C_{GB}: gate-to-bulk capacitance; C_{SB}: source-to-bulk capacitance; C_{DB}: drain-to-bulk capacitance; $C_{B\text{-}sub}$: bulk-to-substrate capacitance, C_{BC}: bulk-to-channel capacitance; C_{GC}: gate-to-channel capacitance.

The main drawback of the approach is a larger drain current error between two otherwise ideally matched transistors, which, in the implementation of an OTA, tends to increase the offset and noise and to reduce the common-mode rejection ratio, CMRR.

Overcoming this issue may result in a complex design [54]. Moreover, since subthreshold operation implies very low standby currents, the reduced transconductance leads to limited bandwidth (4a), which is only partially compensated by the lower MOS parasitic capacitances provided by the scaled technologies. However, this is not a main issue because most of the sensor node applications, such as monitoring pressure, temperature, humidity, acceleration, or bio-signals, usually involve frequencies around the kilohertz [3]. For these reasons, the subthreshold region is popular in the implementation of analog building blocks, including OTAs supplied from 1 V under very limited current budgets [7–11,15].

As an example, a solution operating at 1 V and proposed in [11] is shown in Figure 1. The OTA clearly illustrates that conventional circuit configurations are employed. In this case, we have a folded-cascode differential stage M_1–M_8, followed by a common-source stage M_9–M_{10}, and as a final non-inverting stage, a common-source M_{11} transistor with a current mirror-load M_{12}–M_{13}. The subthreshold biasing point of the transistors here is the key aspect, and, in addition, the use of three gain stages is to compensate for the diminished intrinsic stage gain. Nested Miller frequency compensation capacitors C_1 and C_2 provide closed-loop stability.

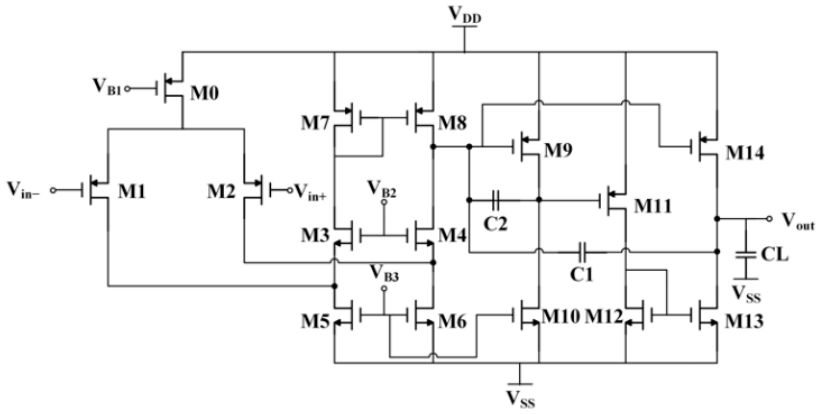

Figure 1. Schematic of the three-stage CMOS OTA operating in the subthreshold region proposed in [11].

The DC gain and the gain–bandwidth product (*GBW*) are

$$A = g_{m1,2} g_{m9} g_{m11} r_{o1} r_{o2} r_{o3} \tag{5}$$

$$GBW = \frac{g_{m1,2}}{C_1} \tag{6}$$

where r_{oi} is the equivalent small-signal resistance at the output of the i-th stage ($r_{o1} \approx r_{d8}$, $r_{o2} = r_{d9} // r_{d10}$, and $r_{o3} = r_{d13} // r_{d14}$). The DC gain is found to be greater than 120 dB, and the GBW is 20 kHz. The solution allows the driving of high capacitive loads up to 200 pF, with only 170 nA of standby current.

3. Body-Driven Approach

Traditional gate-driven approaches, either above or below the threshold, control the conductivity of the channel and, consequently, the drain current, I_D, via the gate-source voltage. In contrast, in the bulk- or body-driven (BD) approach, I_D is controlled by the bulk-source voltage, V_{BS}. Figure 2a,b shows two different ways to implement a p-channel differential pair, one through the usual gate-driven approach and the other through the alternative bulk-driven approach. In the latter case, the differential input signal is applied

to the bulk terminals of the transistors couple M_{2B}–M_{3B}, while the gate terminals are kept to a reference voltage (V_{SS} in this case) [17].

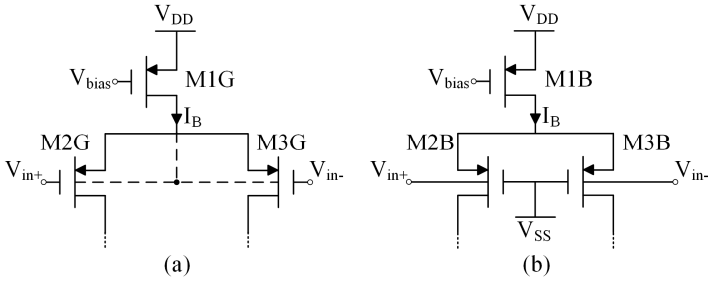

Figure 2. (**a**) Gate-driven and (**b**) bulk-driven p-channel differential pairs.

Removing the limitation given by the threshold voltage associated with the gate terminal, the input common-mode range of the BD pair is maximized, since the input voltages can span from V_{SS} to V_{DD}. The main advantage of this approach is, indeed, the ability to achieve rail-to-rail input operation under supply voltages comparable to or even less than the threshold voltage. It is, of course, mandatory that the bulk-source junction is not turned on. Otherwise, the bulk source junction starts to draw a non-negligible current. For rail-to-rail operation, the approach is hence particularly profitable for supplies (V_{DD}–V_{SS}) below 0.5 V, just below the junction threshold.

Returning to Figure 2b, we observe that the gates of M_{2B}–M_{3B}, connected to V_{SS}, can be instead used to set the standby current of M_{2B}–M_{3B} through a conventional current mirror and by eliminating the tail current generator M_{1B}. In this manner supply demand is further reduced at the cost of a lower power supply rejection ratio, *PSRR* [55]. It is also noteworthy that the BD approach requires the use of a triple-well technology if the body terminal of both *p*- and *n*-channel MOS devices must be exploited. As a drawback, this results in greater area occupation.

The third column of Table 1 shows the small-signal parameters of a body-driven transistor operating in saturation above the threshold region. Since the bulk transconductance g_{mb} is only about 10% to 20% of g_m, as highlighted by (2b), bulk-driven configurations are characterized by reduced values of the intrinsic gain A_v and transition frequency f_T.

Several bulk-driven OTAs have been proposed in literature [12,14–30]. Most of these solutions also operate transistors in the subthreshold to minimize the supply voltage requirements. Moreover, multistage architectures are often utilized to overcome the lower value of the DC gain. Positive feedback is also exploited to increase both the input transconductance and the gain–bandwidth product. To give an example, the schematic of the OTA proposed in [29] is shown in Figure 3. The resulting differential gain and gain–bandwidth product can be expressed as follows:

$$A = \frac{\beta}{1-\alpha} g_{mb1,2} r_o \tag{7}$$

$$GBW = \frac{\beta}{1-\alpha} \frac{g_{mb1,2}}{C_L} \tag{8}$$

where the effect of the positive feedback is displayed by factor $(1 - a)$ at the denominator. Of course, parameter a must be close but lower than 1 to preserve stability. With a = 0.83, and b= 15, we obtain a DC gain slightly lower than 40 dB and a *GBW* equal to 5 kHz, with a power consumption of around 32 nW. It is noteworthy that because of the absence of the tail current generator, M1–M2 is a pseudo-differential pair, but thanks to the action of M7 and M8, the whole OTA provides a quasi-differential behavior, as shown in [29].

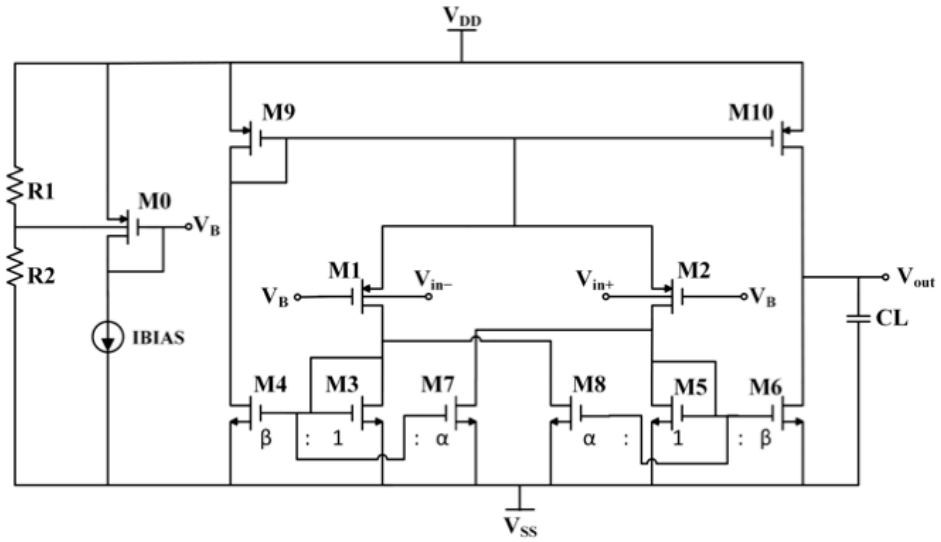

Figure 3. Schematic of the OTA with positive feedback proposed in [29].

For the same purpose of increasing input transconductance, the combination of the body-driven and AC-coupled gate-driven approaches has also been proposed in [56]. As it was already stated, this solution is not considered in this discussion due to the QFG technique limitation in the CMOS process.

4. Body-Biased Approach

The body-biased (BB) approach is aimed at overcoming the limitations of the CMOS technology and/or of the conventional OTA topologies through threshold lowering [8,14], level shifting [16], body-driven gain boosting [19], and non-tailed differential pairs [33,55]. These techniques can also be combined together.

The body-biased approach followed in [31] exploits a gate-driven differential pair, thus providing a high gate transconductance, but (1) the tail current source is eliminated, leaving extra room for the input swing; additionally, (2) the body terminals of the pair are used both to control the common-mode (and hence also the DC) current and to reduce the threshold voltage through the body effect. Figure 4a,b, shows, respectively, the minimum-supply gate-driven differential pair and the simplified schematic of the common-mode control circuit. The common-mode control voltage V_b is generated in the circuit of Figure 4b, forcing $I_B/2$ to flow in M_{1R} (M_{2R}) when $V_{in+} = V_{in-} = V_{icm}$. Then, V_b is applied to the main circuit of Figure 4a. It is apparent that the quiescent (and common-mode) current in M_1–M_2 is mirrored from that of M_{1R}–M_{2R}, and hence, M_1–M_2 acts as a differential pair but without the tail current source. Moreover, under suitable values of $W/L)_{1R-2R}$ and I_B, the voltage V_b is less than V_{DD}, and the threshold voltage of M_{1R}–M_{2R} is diminished.

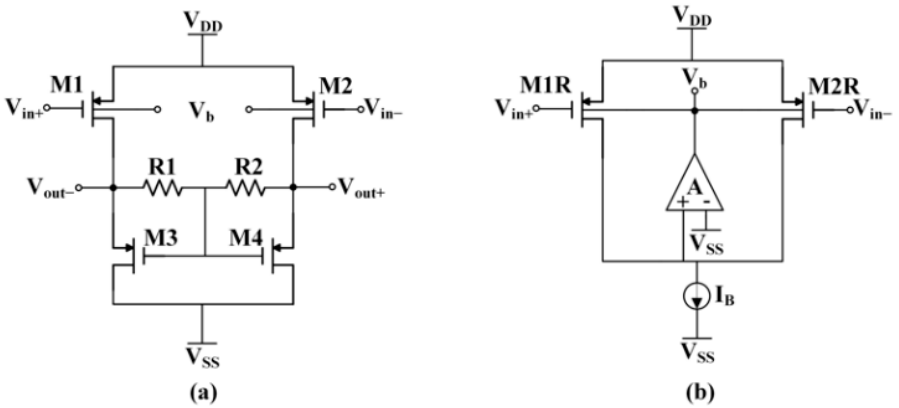

Figure 4. (**a**) Minimum-supply differential pair (**b**) common-mode control circuit proposed in [31].

The gain of the circuit in Figure 4a can be expressed as

$$A \approx \frac{g_{m1,2}}{2} R_{1,2} \tag{9}$$

where the output resistance of transistors is neglected.

Based on this approach, an optimized solution that provides relatively low noise around 65 nV/$\sqrt{Hz}$ and a total current consumption of 27 µA with a good trade-off between DC gain (65 dB) and gain–bandwidth product (1 MHz) has been experimentally validated in [33].

5. Inverter-Based Approach

All the previous OTAs require manual design flow from the schematic level to the layout and routing. Moreover, the BD and BB approaches especially result in considerable area occupation because separate wells must be used. In other words, unlike digital designs, the previous OTAs do not take advantage of design automation and technology scaling.

The inverter-based (INV) approach exploits CMOS inverters as transconductance stage elements, as said, in an attempt to extend the digital design flow to the analog domain, keep low the design effort, and provide portability across technologies. An early implementation of this approach is the so-called Nauta transconductor and further derivations [34–42].

As an introduction, consider the inverter M1–M2 in Figure 5 and neglect, for the moment, resistor RF. It can be seen that the inverter works as an amplifier, provided that it is biased in its switching threshold so that both transistors are in saturation. Under this biasing condition, the small-signal transconductance of the inverter is equal to the sum of the transconductances of both the nMOS and pMOS transistors, i.e., $g_m = g_{m1} + g_{m2}$.

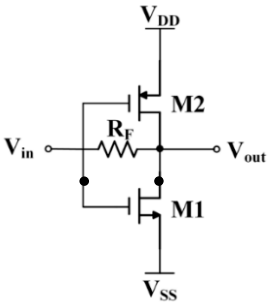

Figure 5. The CMOS inverter uses an analog amplifier that is self-biased at the switching threshold.

The bias point can be obtained through self-biasing using the resistive feedback provided by R_F, as shown in Figure 5, or with more complex, higher-efficiency topologies [40], even exploiting the body terminal [37]. In conclusion, the circuit in Figure 5 can be used as a transimpedance amplifier because it has a relatively low input resistance.

To obtain a transconductance amplifier, we can return to a conventional single-stage OTA, as exemplified in Figure 6a. The key concept here is to replace each transistor in the signal path (M_1–M_4) with an inverter. The gate and the drain of the original transistors correspond to the input and output of the associated inverter, respectively. The source terminal is not important, as it is kept at a fixed potential. This is true for active load transistors M_3 and M_4 but also for the pair M_1 and M_2, since, as is well known, the common source is at the virtual ground, provided that the input signal is purely differential. As a result, the circuit in Figure 6b is derived, which represents the basic inverter-based single-stage OTA. Indicating with G_{mi} and R_{oi} the transconductance and output resistance of the i-th inverter, the output voltage is given by $V_{out} = (G_{m1}G_{m4}/G_{m3}\, V_{in+} - G_{m2}\, V_{in-})R_{o4}$. If $G_{m1} = G_{m2} = G_{m1,2}$, and $G_{m3} = G_{m4}$, then the gain can be expressed as

$$A = G_{m1,2} R_{o4} \tag{10}$$

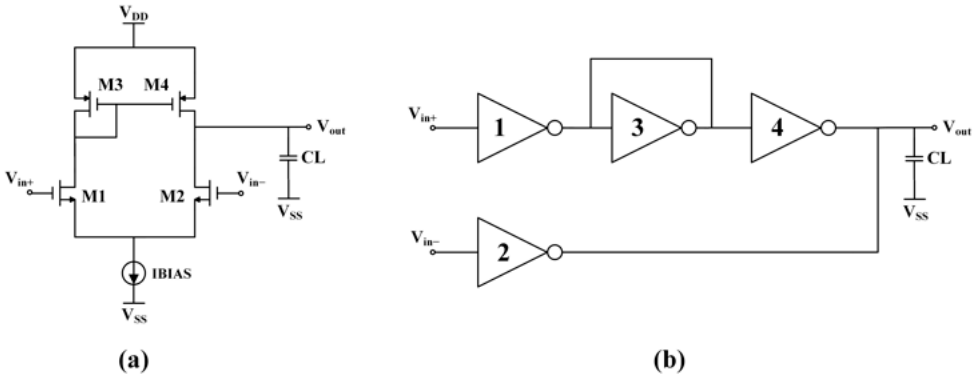

Figure 6. Conventional (**a**) and inverter-based (**b**) single-stage OTA.

The expression of GBW is as in (6) by replacing $g_{m1,2}$ with $G_{m1,2}$ and C_1 with $C_{L.}$ (In this case, dominant pole compensation is adopted.)

While this circuit can be designed using standard cells and automated place and route, it has several drawbacks, such as low DC gain and *CMRR* (due to the unavoidable mismatches between G_{m1} and G_{m2} and between G_{m3} and G_{m4}), it implements only a *pseudo-differential* OTA, and it does not offer DC current control [42]. The latter limitation is fundamental for applications with a limited power budget. Moreover, it makes the solution very sensitive to process, supply, and temperature (PVT) variations.

A four-stage inverter-based OTA that uses the bulk terminals of both the p-channel and n-channel MOS transistors of the standard-cell inverter as current and voltage control inputs was proposed in [43]. The body-control approach is similar to that used in digital applications to handle process variations. All the standard-cell inverters used for analog functions are connected to an analog building block generator, which provides the bulk voltages and which, in turn, enables each cell's static output voltage to be adjusted to half the supply voltage and the quiescent current to be set to a multiple of a reference current. The simplified schematic of the OTA proposed in [43] is shown in Figure 7, where inverters 1–5 are simple inverters (×1), inverter 6 is made up of two parallel inverters (×2), and inverter 7 is made up of four parallel inverters (×4). The body-control section is not shown for simplicity, but the interested reader can refer to [43] for further details.

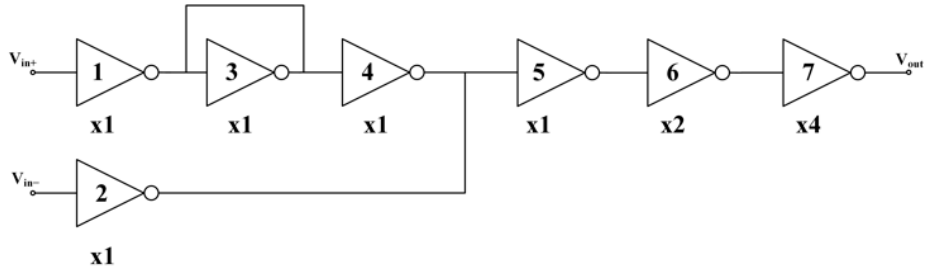

Figure 7. Schematic of the inverter-based OTA in [43].

In summary, this solution operates at a 0.5 V supply and provides a DC gain of around 70 dB, a gain–bandwidth product around of 7 MHz, and a slew rate of 1.51 V/µs, with a power consumption of only 0.88 µW.

6. Digital Approach

Analog processing requires a well-defined biasing point for the active devices, which, in turn, require a well-defined quiescent current, setting the lower limit for the DC power consumption. With the digital-based approach, it is possible to eliminate any quiescent bias current and to ensure low power consumption, low area occupation, and low complexity at the cost of weak control over current consumption and hence performance across PVT variations.

Several fully digital OTAs (DIGOTA) with a sub-1 V supply and nanowatt power consumption have been presented in literature [43–51]. These solutions do not require a DC current, as they are essentially digital standard cell-based OTAs and share with the inverter-based approach the advantages of both simple design and portability over technologies.

In this context, a passive-less fully-digital operational transconductance amplifier (DIGOTA) that employs time-domain processing, zero bias current, and passive-less self-oscillation common-mode compensation was proposed in [45,46] and finally improved in [51].

The principle of operation of the DIGOTA is the same as the NOT approach and relies on the observation that a simple pair of digital inverters, as shown in Figure 8a, under an input differential signal $(V_{IN+} - V_{IN-}) > 0$ ($(V_{IN+} - V_{IN-}) < 0$) generates a high (low) output differential voltage, provided that the input common-mode voltage, V_{CM}, is close to the inverter trip point, V_{trip}. If V_{CM} is away from V_{trip}, the digital outputs of the inverters are equal and cannot discriminate whether $(V_{IN+} - V_{IN-}) > 0$, or $(V_{IN+} - V_{IN-}) < 0$. However, the information related to the signal $V_{CM} < V_{trip}$ or $V_{CM} > V_{trip}$ still provides useful information that can be exploited to correct the common-mode input signal and enforce the desired condition, $V_{CM} = V_{trip}$, through a negative feedback loop.

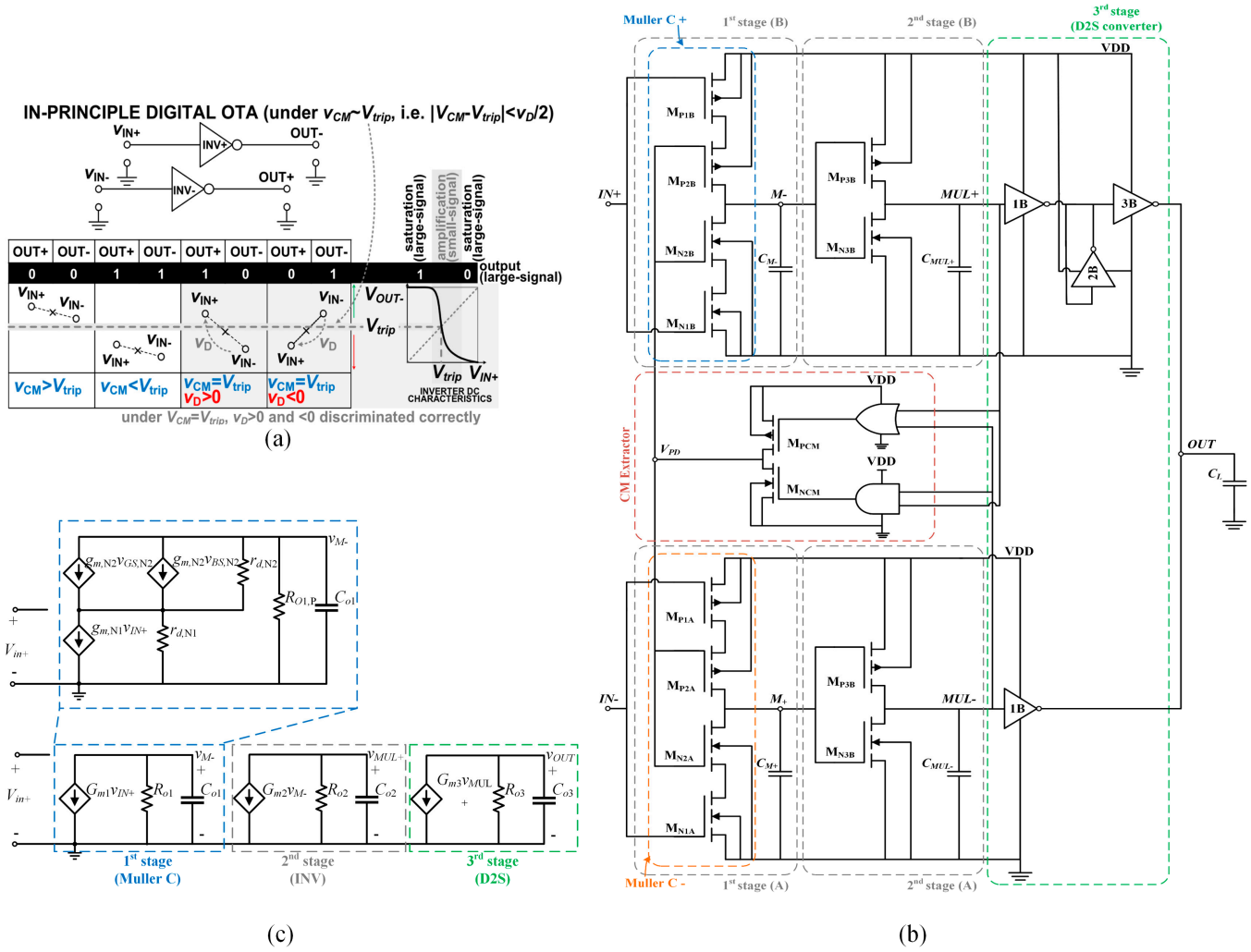

Figure 8. (**a**) Principle of operation of the DIGOTA introduced in [46]; (**b**) schematic and (**c**) small-signal model of the DIGOTA proposed in [51].

The schematic of the DIGOTA recently introduced in [51] is shown in Figure 8b. The compensation of the common-mode voltage is implemented by adopting an input stage

based on the Muller C-element driven by the two input voltages, V_{IN+} and V_{IN-}, and by the signal V_{PD}. The differential-to-single-ended (D2S) output stage is implemented in this work by inverters 1B and 2B (constituting an inverting voltage buffer), with inverters 1A and 3B acting as transconductance amplifiers. As a result, the DIGOTA is made up of three gain stages, namely the Muller C-element, the inverter, and the output stage. Remarkably, it has been demonstrated in [51] that the equivalent small-signal model can be reduced to that of a conventional three-stage OTA, as shown in Figure 8c. Assuming that V_{PD} is almost constant, the small-signal parameters in Figure 8c can be expressed as (Note that a more accurate evaluation of $g_{m,\mathrm{N1}}$ and $g_{m,\mathrm{P1}}$ includes the body transconductance of the transistors $\mathrm{M_{N2}}$ and $\mathrm{M_{P2}}$, as detailed in [51]):

$$G_{m1} = g_{m,N1} + g_{m,P1} \tag{11}$$

$$G_{m2} = g_{m,N3} + g_{m,P3} \tag{12}$$

$$G_{m3} = 2(g_{mN,1A} + g_{mP,3B}) \tag{13}$$

$$C_{O1} = C_{par1} + C_M \tag{14}$$

$$C_{O2} = C_{par2} + C_{MUL} \tag{15}$$

$$C_{O3} = C_{par3} + C_L \tag{16}$$

$$R_{O1} = R_{O1,N} \| R_{O1,P} \tag{17}$$

$$R_{O2} = r_{d,N3} \| r_{d,P3} \tag{18}$$

$$R_{O3} = r_{d,N3} \| r_{d,P3} \tag{19}$$

with C_{par_i} being the parasitic capacitance at the output of the i-th stage. $R_{O1,N}$ and $R_{O1,P}$ are the resistances of the cascode gain stage. The voltage gain and the GBW are, therefore, equal to

$$A = G_{m1} G_{m2} G_{m3} R_{O1} R_{O2} R_{O3} \tag{20}$$

$$GBW = \frac{G_{m1} G_{m2} G_{m3} R_{O1} R_{O2}}{C_L} \tag{21}$$

Under a 0.3 V supply and a load of 250 pF (and at 27 °C), the power consumption of the OTA is 44.2 nW, while the occupied area is 625 μm^2. DC gain is 66 dB, and GBW is 12.3 kHz. Power dissipation ad GBW increases to 198.6nW and 59 kHz at 70 °C, just to give and idea of the sensitivity of temperature.

7. Comparison and Discussion

With a view of making a more detailed comparison among the examined approaches, we will consider only the ultra-low power OTAs with a supply equal to or less than 0.7 V, which are summarized in Table 2. Note that simulated INV solutions have also been considered, due to the lack of fabricated examples. The main OTA parameters such as DC gain, gain–bandwidth product (GBW), phase margin (PM), slew rate (SR), noise, common-mode rejection ratio (CMRR), and power supply rejection ratio (PSRR), together with the well-known figures of merit, FOM_S, FOM_L, $IFOM_S$, and $IFOM_L$ [10,11,21–23,26,27,51], defined in (18) and (19), are evaluated.

$$FOM_S = \frac{GBW}{Power} C_L \tag{22}$$

$$FOM_L = \frac{SR}{Power} C_L \tag{23}$$

$$IFOM_S = \frac{GBW}{I_T} C_L \tag{24}$$

$$IFOM_L = \frac{SR}{I_T} C_L \tag{25}$$

where I_T is the total bias current.

For a specified capacitance load, (22)–(25) show a trade-off between small-signal and large-signal parameters and total power/bias current consumption.

If we also consider the area occupation, we can define the following two additional figures of merit ($IFOM_{AS}$ and $IFOM_{AL}$) in (24) and (25) [30,46,51]

$$IFOM_{AS} = \frac{GBW}{Area \cdot I_T} C_L \tag{26}$$

$$IFOM_{AL} = \frac{SR}{Area \cdot I_T} C_L \tag{27}$$

From the inspection of Table 2, the lowest value of power consumption, which was around 1 nW, was achieved by [39,47], which used a DIG and an INV approach, respectively. The highest value of the DC gain was 98 dB and was achieved by [28], which combined the BD and the SUB approach, while the highest *GBW* was achieved by [23] (with minimum C_L of 3pF), which exploited an INV approach.

The highest $IFOM_S$ was achieved by the INV OTA proposed in [47], while the highest $IFOM_L$ was achieved by the BD + SUB OTA proposed in [29]. It is also apparent that the DIG and INV approach resulted in the lowest area occupation.

Figures 9 and 10 show the plots of $IFOM_S$ and $IFOM_L$ (on a semilogarithmic scale) for the different OTAs as functions of the technology node. Additionally, $IFOM_S$ and $IFOM_L$ reached the maximum in the 0.18 mm technology node, and the best small-signal performance was achieved by the DIG approach, whereas DIG and SUB + BD shared the best large-signal performance. Interestingly, SUB + BD was still the best in the minimum technology node implementations (i.e., 65-nm), though no DIG implementations here are available for comparison.

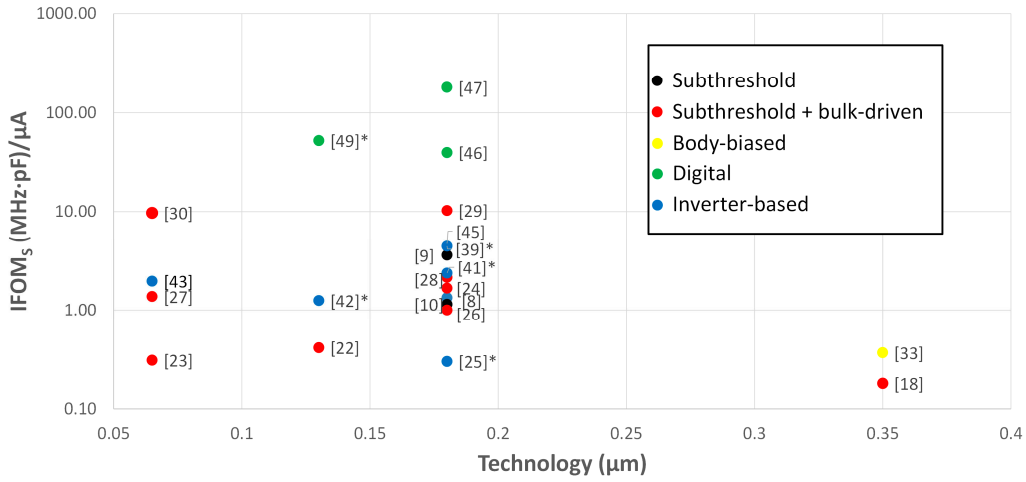

Figure 9. $IFOM_S$ vs. technology (* simulated).

Table 2. Comparison of ultra-low-power OTAs (* simulated).

	[8]	[9]	[10]	[18]	[22]	[23]	[24]	[26]	[28]	[27]	[29]	[30]	[33]	[25] *	[41] *	[39] *	[43]	[42] *	[45]	[47]	[46]	[49]
Year	2005	2014	2016	2007	2014	2015	2016	2018	2020	2020	2022	2023	2017	2017	2020	2020	2022	2022	2020	2021	2021	2021
Tech. [µm]	0.18	0.18	0.18	0.35	0.13	0.065	0.18	0.18	0.18	0.065	0.18	0.065	0.35	0.18	0.18	0.18	0.065	0.13	0.18	0.18	0.18	0.13
Op. mode[b]	SUB	SUB	SUB	SUB, BD	SUB, BD	SUB, BD	BD	SUB, BD	SUB, BD	SUB, BD	SUB, BD	BD	BB	INV	INV	INV	INV	INV	DIG	DIG	DIG	DIG
Area [mm^2] × 10^{-2}	1.7	5.7	3.6	6	8.3	0.5	2	0.8	1	0.2	0.9	0.11	1.4	-	0.08	0.07	0.02	0.02	0.1	0.1	0.1	0.01
Supply [V]	0.5	0.5	0.5	0.6	0.25	0.5	0.7	0.3	0.3	0.25	0.4	0.3	0.7	0.5	0.5	0.3	0.5	0.3	0.3	0.3	0.5	0.55
CL [pF]	20	30	40	15	15	3	20	20	30	15	150	50	10	20	10	10	0.5	2	150	80	150	250
DC gain [dB]	62	70	77	69	60	46	57	63	98.1	70	37	38	65	91	25.2	51	64	34.97	30	30	73	87
I_T [µA]	150	0.15	0.14	0.9	0.072	366	36	0.056	0.043	0.104	0.081	8.5	27	26	0.558	0.002	1.75	20.3	0.008	0.002	0.215	14.9
Power [µW]	75	0.075	0.07	0.54	0.018	183	25.2	0.017	0.013	0.026	0.033	2.55	18.9	13	0.279	0.001	0.875	6.1	0.002	0.001	0.108	8.2
GBW [kHz]	0.01	18	4	11	2	38,000	3000	3	3	10	6	1650	1000	394	132	0.74	6850	12,700	0.2	4	60	3150
PM [°]	60	55	56	65	53	57	60	61	54	88	79	70.3	60	59	87	90	62	62	-	54	-	65
SR [V/ms]	2000	3	2	15	0.7	43,000	2800	7	9	2	7.9	180	250	-	-	-	1510	5680	0.1	0.2	19	2.7
Noise [nV/sqrt(Hz)]	280	310	-	290	3300	926	100	1850 *	1800 *	-	-	250	65	31.8	-	809	-	-	21,000	-	-	175
CMRR (dB)	65	-	55	74.5	-	35	19	72	60	62.5	36	39.8	45	-	-	37	-	27	41	-	65	46
PSRR [dB]	43	-	52	-	-	37	52	62	61	38	30	44.7	50	122.3	76.8	41	-	-	30	-	50	39
# stages	2	2	2	2	2	3	3	2	3	3	1	3	2	-	-	-	4	-	-	-	-	-
FOM_S [MHz·pF/µW]	2.67	7.20	2.29	0.31	1.67	0.62	2.38	3.33	7.15	5.48	25.6	32.35	0.53	0.61	4.73	14.8	3.91	4.16	15.6	598	80.2	96.0
FOM_L [(V/µs)·pF/µW]	0.53	1.20	1.14	0.42	0.58	0.7	2.22	8.45	21	1.15	34.1	3.53	0.13	-	-	-	0.86	1.86	5.31	28.96	26.5	0.08
$IFOM_S$ [MHz·pF/µA]	1.33	3.60	1.14	0.18	0.42	0.31	1.67	1	2.15	1.37	10.3	9.71	0.37	0.30	2.37	4.44	1.96	1.25	4.69	179	40.1	52.8
$IFOM_L$ [(V/µs)·pF/µA]	0.27	0.60	0.57	0.25	0.15	0.35	1.56	2.54	6.3	0.29	13.64	1.06	0.09	-	-	-	0.43	0.56	1.59	8.69	13.3	0.05
$IFOM_{AS}$ [MHz·pF/µA·mm^2]	78.43	63.16	31.75	3	5	63	84	122	219	685	11,838	9156	26.5	-	2957	6107	9786	5730	4773	122,62	40,852	598,189
$IFOM_{AL}$ [[(V/µs)·pF/µA·mm^2]	15.69	10.53	15.87	4.2	1.8	71.2	78.6	309.2	642.9	144.2	15,745	999	6.6	-	-	-	2150	2565	1623	5943	13,499	513

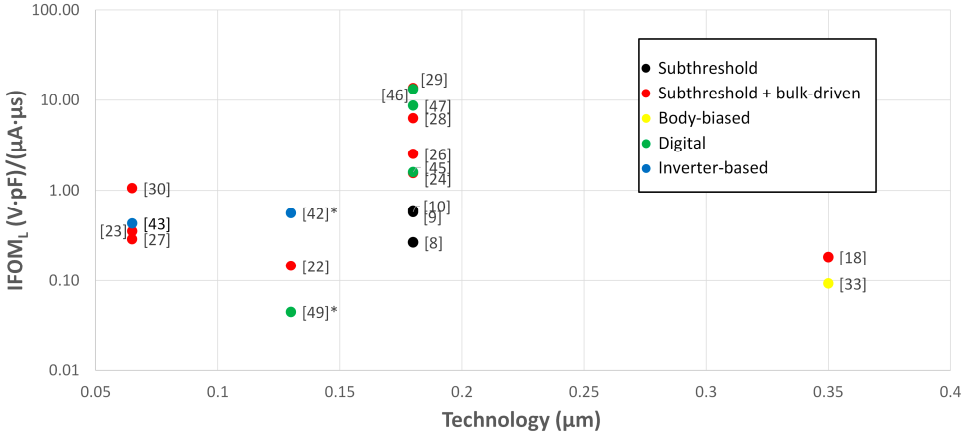

Figure 10. *IFOM*$_L$ vs. technology (* simulated).

Figures 11 and 12 also show *IFOM*$_{AS}$ and *IFOM*$_{AL}$ as functions of the technology node. In general, the highest values of *IFOM*$_{AS}$ were achieved by the DIG and INV approaches, thanks to their inherent reduced area occupation. SUB + BD was competitive for the large-signal performance.

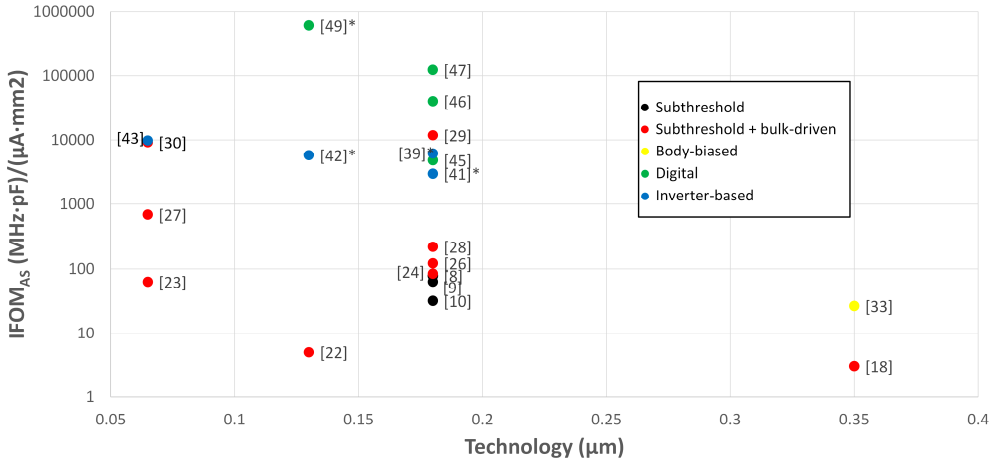

Figure 11. *IFOM*$_{AS}$ vs. technology (* simulated).

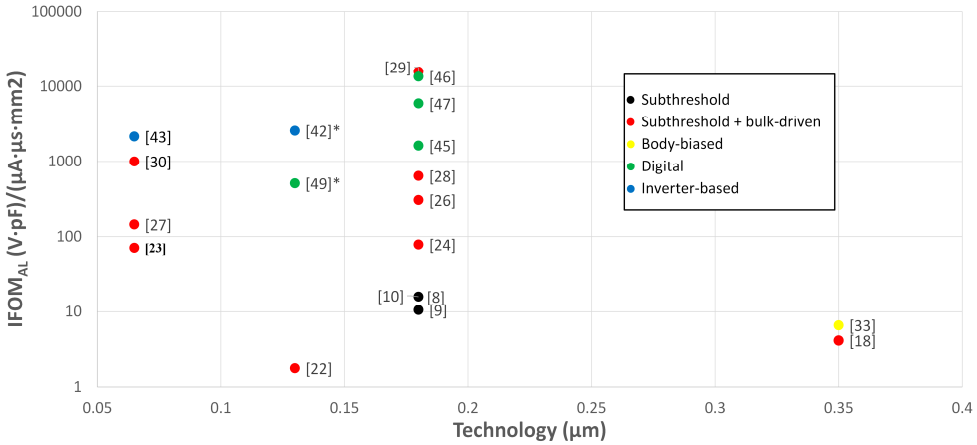

Figure 12. *IFOM*$_{AL}$ vs. technology (* simulated).

Another comparison was carried out considering the effect of the supply voltage reduction, as illustrated in Figures 13 and 14, showing the *IFOM*$_S$ and *IFOM*$_L$ as functions

of V_{DD}, respectively. Below 0.6 V, DIG approaches provided the best $IFOM_S$, which were greater up to one order of magnitude with respect to INV and SUB-BD counterparts. $IFOM_L$ were dominated by SUB-BD and DIG approaches, which provided similar values.

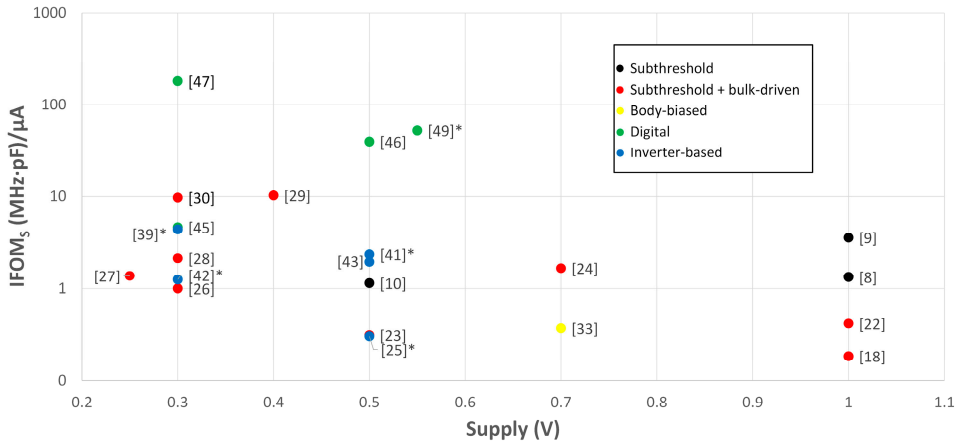

Figure 13. $IFOM_S$ vs. supply voltage (* simulated).

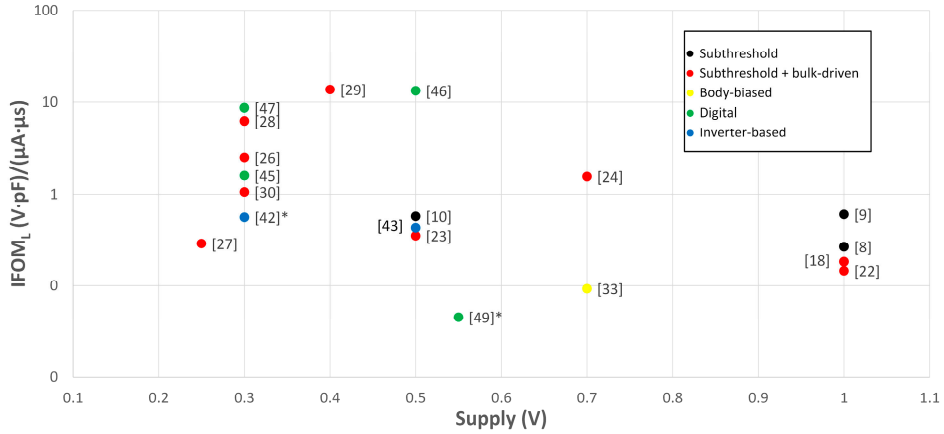

Figure 14. $IFOM_L$ vs. supply voltage (* simulated).

Considering also the area occupation, Figures 15 and 16 show the $IFOM_{AS}$ and $IFOM_{AL}$ achieved by the OTAs as functions of the supply voltage. Similar considerations for Figures 13 and 14 can be derived.

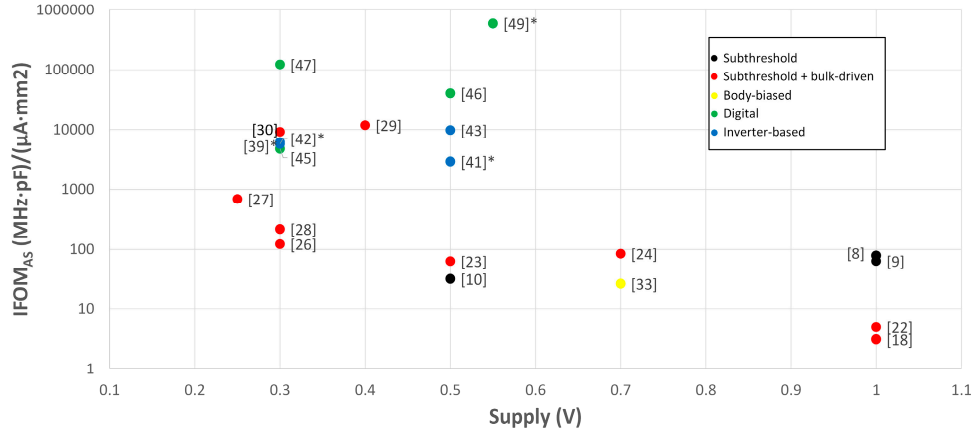

Figure 15. $IFOM_{AS}$ vs. supply voltage (* simulated).

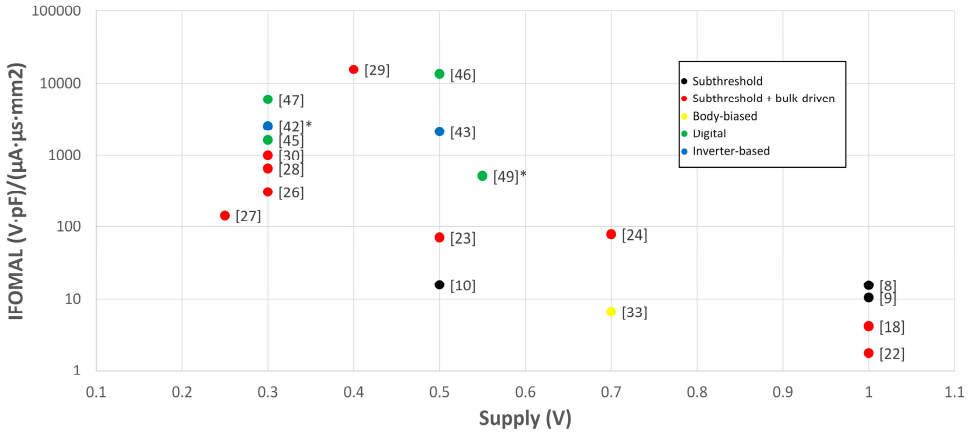

Figure 16. $IFOM_{AL}$ vs. supply voltage (* simulated).

8. Conclusions

This paper describes OTA solutions amenable for IoT applications that require low-voltage and low-current capabilities together with reduced area occupation. After providing a succinct examination of the working principles of the CMOS subthreshold, body-driving, body-biasing, inverter-based, and digital techniques by the utilization of exemplifying solutions proposed by the authors, a comparison of cutting-edge CMOS OTA designs suitable for IoT applications was performed. The comparison was carried out by taking into account small-signal and large-signal performances, as well as area occupation and robustness against PVT variations. According to the findings, only the SUB + BD, DIG, and INV approaches are suitable for supply voltages less than 0.6 V. Furthermore, DIG and INV require the least amount of silicon area, provide design portability across multiple technologies, and support automated design. SUB + BD, on the other hand, which is an 'analog' approach, necessitates a custom design and a larger area but maintains performance across technology scaling, providing competitive large-signal performance. It was noted that the SUB + BD approach continues to provide the best results in the smallest technology node implementations available, namely 65 nm (although this may be due to a lack of DIG implementations in this technology). More importantly, with a well-defined bias point, it allows for better control over power dissipation (and thus small- and large-signal performances) in the face of PVT variations.

In summary, applications requiring reliable current control must prefer SUB + BD or at the very least, INV, with current control solutions if silicon area is a major concern. DIG solutions, while promising, will require further study and development.

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Abbreviations

BB	Bulk-Biased
BD	Bulk-Driven
CAD	Computer-Aided Design
CMOS	Complementary Metal–Oxide–Semiconductor
CMRR	Common-Mode Rejection Ratio
DIGOTA	Digital OTA
GBW	Gain–Bandwidth product

IoT	Internet of Things
MOS	Metal–Oxide–Semiconductor
OTA	Operational Transconductance Amplifier
PM	Phase Margin
PSRR	Power Supply Rejection Ratio
PVT	Process, Supply, and Temperature
SR	Slew Rate

References

1. Number of Internet of Things (IoT) Connected Devices Worldwide from 2019 to 2021, with Forecasts from 2022 to 2030. Available online: https://www.statista.com/statistics/1183457/iot-connected-devices-worldwide/ (accessed on 6 September 2023).
2. Alioto, M. (Ed.) *Enabling the Internet of Things: From Integrated Circuits to Integrated Systems*; Springer International Publishing: Berlin/Heidelberg, Germany, 2017; ISBN 978-3-319-51480-2.
3. Jang, T.; Kim, G.; Kempke, B.; Henry, M.B.; Chiotellis, N.; Pfeiffer, C.; Kim, D.; Kim, Y.; Foo, Z.; Kim, H.; et al. Circuit and System Designs of Ultra-Low Power Sensor Nodes with Illustration in a Miniaturized GNSS Logger for Position Tracking: Part I—Analog Circuit Techniques. *IEEE Trans. Circuits Syst. Regul. Pap.* **2017**, *64*, 2237–2249. [CrossRef]
4. Sansen, W. 1.3 Analog CMOS from 5 Micrometer to 5 Nanometer. In Proceedings of the 2015 IEEE International Solid-State Circuits Conference—(ISSCC) Digest of Technical Papers, San Francisco, CA, USA, 22–26 February 2015; pp. 1–6.
5. Vittoz, E.; Fellrath, J. CMOS Analog Integrated Circuits Based on Weak Inversion Operations. *IEEE J. Solid-State Circuits* **1977**, *12*, 224–231. [CrossRef]
6. Hollis, T.M.; Comer, D.J.; Comer, D.T. Optimization of MOS Amplifier Performance through Channel Length and Inversion Level Selection. *IEEE Trans. Circuits Syst. II Express Briefs* **2005**, *52*, 545–549. [CrossRef]
7. Valero Bernal, M.R.; Celma, S.; Medrano, N.; Calvo, B. An Ultralow-Power Low-Voltage Class-AB Fully Differential OpAmp for Long-Life Autonomous Portable Equipment. *IEEE Trans. Circuits Syst. II Express Briefs* **2012**, *59*, 643–647. [CrossRef]
8. Chatterjee, S.; Tsividis, Y.; Kinget, P. 0.5-V Analog Circuit Techniques and Their Application in OTA and Filter Design. *IEEE J. Solid-State Circuits* **2005**, *40*, 2373–2387. [CrossRef]
9. Magnelli, L.; Amoroso, F.A.; Crupi, F.; Cappuccino, G.; Iannaccone, G. Design of a 75-nW, 0.5-V Subthreshold Complementary Metal–Oxide–Semiconductor Operational Amplifier. *Int. J. Circuit Theory Appl.* **2014**, *42*, 967–977. [CrossRef]
10. Qin, Z.; Tanaka, A.; Takaya, N.; Yoshizawa, H. 0.5-V 70-nW Rail-to-Rail Operational Amplifier Using a Cross-Coupled Output Stage. *IEEE Trans. Circuits Syst. II Express Briefs* **2016**, *63*, 1009–1013. [CrossRef]
11. Grasso, A.D.; Marano, D.; Palumbo, G.; Pennisi, S. Design Methodology of Subthreshold Three-Stage CMOS OTAs Suitable for Ultra-Low-Power Low-Area and High Driving Capability. *IEEE Trans. Circuits Syst. Regul. Pap.* **2015**, *62*, 1453–1462. [CrossRef]
12. Blalock, B.J.; Allen, P.E.; Rincon-Mora, G. Designing 1-V Op Amps Using Standard Digital CMOS Technology. *IEEE Trans. Circuits Syst. II Analog Digit. Signal Process.* **1998**, *45*, 769–780. [CrossRef]
13. Bialko, M.; Guzinski, A.; Allen, P.E.; Blalock, B.J.; Rincon-Mora, G. Comments on "Designing 1-V Op-Amps Using Standard Digital CMOS Technology" [and Reply]. *IEEE Trans. Circuits Syst. II Analog Digit. Signal Process.* **1999**, *46*, 1448. [CrossRef]
14. Lehmann, T.; Cassia, M. 1-V Power Supply CMOS Cascode Amplifier. *IEEE J. Solid-State Circuits* **2001**, *36*, 1082–1086. [CrossRef]
15. Stockstad, T.; Yoshizawa, H. A 0.9-V 0.5-Um Rail-to-Rail CMOS Operational Amplifier. *IEEE J. Solid-State Circuits* **2002**, *37*, 286–292. [CrossRef]
16. Carrillo, J.M.; Duque-Carrillo, J.F.; Torelli, G.; Ausin, J.L. Constant-g/Sub m/Constant-Slew-Rate High-Bandwidth Low-Voltage Rail-to-Rail CMOS Input Stage for VLSI Cell Libraries. *IEEE J. Solid-State Circuits* **2003**, *38*, 1364–1372. [CrossRef]
17. Carrillo, J.M.; Torelli, G.; Perez-Aloe Valverde, R.; Duque-Carrillo, J.F. 1-V Rail-to-Rail CMOS OpAmp With Improved Bulk-Driven Input Stage. *IEEE J. Solid-State Circuits* **2007**, *42*, 508–517. [CrossRef]
18. Ferreira, L.H.C.; Pimenta, T.C.; Moreno, R.L. An Ultra-Low-Voltage Ultra-Low-Power CMOS Miller OTA with Rail-to-Rail Input/Output Swing. *IEEE Trans. Circuits Syst. II Express Briefs* **2007**, *54*, 843–847. [CrossRef]
19. Monsurrò, P.; Pennisi, S.; Scotti, G.; Trifiletti, A. 0.9-V CMOS Cascode Amplifier with Body-Driven Gain Boosting. *Int. J. Circuit Theory Appl.* **2009**, *37*, 193–202. [CrossRef]
20. Raikos, G.; Vlassis, S. Low-Voltage Bulk-Driven Input Stage with Improved Transconductance. *Int. J. Circuit Theory Appl.* **2011**, *39*, 327–339. [CrossRef]
21. Zuo, L.; Islam, S.K. Low-Voltage Bulk-Driven Operational Amplifier with Improved Transconductance. *IEEE Trans. Circuits Syst. Regul. Pap.* **2013**, *60*, 2084–2091. [CrossRef]
22. Ferreira, L.H.C.; Sonkusale, S.R. A 60-dB Gain OTA Operating at 0.25-V Power Supply in 130-Nm Digital CMOS Process. *IEEE Trans. Circuits Syst. Regul. Pap.* **2014**, *61*, 1609–1617. [CrossRef]
23. Abdelfattah, O.; Roberts, G.W.; Shih, I.; Shih, Y.C. An Ultra-Low-Voltage CMOS Process-Insensitive Self-Biased OTA With Rail-to-Rail Input Range. *IEEE Trans. Circuits Syst. Regul. Pap.* **2015**, *62*, 2380–2390. [CrossRef]
24. Cabrera-Bernal, E.; Pennisi, S.; Grasso, A.D.; Torralba, A.; Carvajal, R.G. 0.7-V Three-Stage Class-AB CMOS Operational Transconductance Amplifier. *IEEE Trans. Circuits Syst. Regul. Pap.* **2016**, *63*, 1807–1815. [CrossRef]
25. Vlassis, S.; Kulej, T.; Khateb, F.; Souliotis, G. 0.5 V Bulk-Driven Ring Amplifier Based on Master–Slave Technique. *Analog Integr. Circuits Signal Process.* **2017**, *90*, 189–197. [CrossRef]

26. Kulej, T.; Khateb, F. Design and Implementation of Sub 0.5-V OTAs in 0.18-Mm CMOS. *Int. J. Circuit Theory Appl.* **2018**, *46*, 1129–1143. [CrossRef]
27. Woo, K.-C.; Yang, B.-D. A 0.25-V Rail-to-Rail Three-Stage OTA With an Enhanced DC Gain. *IEEE Trans. Circuits Syst. II Express Briefs* **2020**, *67*, 1179–1183. [CrossRef]
28. Kulej, T.; Khateb, F. A 0.3-V 98-dB Rail-to-Rail OTA in 0.18 µm CMOS. *IEEE Access* **2020**, *8*, 27459–27467. [CrossRef]
29. Ballo, A.; Grasso, A.D.; Pennisi, S. 0.4-V, 81.3-nA Bulk-Driven Single-Stage CMOS OTA with Enhanced Transconductance. *Electronics* **2022**, *11*, 2704. [CrossRef]
30. Ballo, A.; Grasso, A.D.; Pennisi, S.; Susinni, G. A 0.3-V 8.5-µ A Bulk-Driven OTA. *IEEE Trans. Very Large Scale Integr. VLSI Syst.* **2023**, *31*, 1444–1448. [CrossRef]
31. Grasso, A.D.; Monsurrò, P.; Pennisi, S.; Scotti, G.; Trifiletti, A. Analysis and Implementation of a Minimum-Supply Body-Biased CMOS Differential Amplifier Cell. *IEEE Trans. Very Large Scale Integr. VLSI Syst.* **2009**, *17*, 172–180. [CrossRef]
32. Centurelli, F.; Monsurro, P.; Pennisi, S.; Scotti, G.; Trifiletti, A. Design Solutions for Sample-and-Hold Circuits in CMOS Nanometer Technologies. *IEEE Trans. Circuits Syst. II Express Briefs* **2009**, *56*, 459–463. [CrossRef]
33. Grasso, A.D.; Pennisi, S.; Scotti, G.; Trifiletti, A. 0.9-V Class-AB Miller OTA in 0.35-µm CMOS With Threshold-Lowered Non-Tailed Differential Pair. *IEEE Trans. Circuits Syst. Regul. Pap.* **2017**, *64*, 1740–1747. [CrossRef]
34. Nauta, B. A CMOS Transconductance-C Filter Technique for Very High Frequencies. *IEEE J. Solid-State Circuits* **1992**, *27*, 142–153. [CrossRef]
35. Andreani, P.; Mattisson, S. On the Use of Nauta's Transconductor in Low-Frequency CMOS g/Sub m/-C Bandpass Filters. *IEEE J. Solid-State Circuits* **2002**, *37*, 114–124. [CrossRef]
36. Figueiredo, M.; Santos-Tavares, R.; Santin, E.; Ferreira, J.; Evans, G.; Goes, J. A Two-Stage Fully Differential Inverter-Based Self-Biased CMOS Amplifier with High Efficiency. *IEEE Trans. Circuits Syst. Regul. Pap.* **2011**, *58*, 1591–1603. [CrossRef]
37. Shrimali, H.; Chatterjee, S. 11 GHz UGBW Op-Amp with Feed-Forward Compensation Technique. In Proceedings of the 2011 IEEE International Symposium of Circuits and Systems (ISCAS), Rio de Janeiro, Brazil, 15–18 May 2011; pp. 17–20.
38. Kaliyath, Y.; Laxminidhi, T. A 1.8 V 11.02 µW Single-Ended Inverter-Based OTA with 113.62 dB Gain. In Proceedings of the 2016 IEEE Distributed Computing, VLSI, Electrical Circuits and Robotics (DISCOVER), Mangalore, India, 13–14 August 2016; pp. 237–241.
39. Rodovalho, L.H.; Aiello, O.; Rodrigues, C.R. Ultra-Low-Voltage Inverter-Based Operational Transconductance Amplifiers with Voltage Gain Enhancement by Improved Composite Transistors. *Electronics* **2020**, *9*, 1410. [CrossRef]
40. Bae, W. CMOS Inverter as Analog Circuit: An Overview. *J. Low Power Electron. Appl.* **2019**, *9*, 26. [CrossRef]
41. Manfredini, G.; Catania, A.; Benvenuti, L.; Cicalini, M.; Piotto, M.; Bruschi, P. Ultra-Low-Voltage Inverter-Based Amplifier with Novel Common-Mode Stabilization Loop. *Electronics* **2020**, *9*, 1019. [CrossRef]
42. Sala, R.D.; Centurelli, F.; Scotti, G. A Novel Differential to Single-Ended Converter for Ultra-Low-Voltage Inverter-Based OTAs. *IEEE Access* **2022**, *10*, 98179–98190. [CrossRef]
43. Centurelli, F.; Giustolisi, G.; Pennisi, S.; Scotti, G. A Biasing Approach to Design Ultra-Low-Power Standard-Cell-Based Analog Building Blocks for Nanometer SoCs. *IEEE Access* **2022**, *10*, 25892–25900. [CrossRef]
44. Crovetti, P.S. A Digital-Based Analog Differential Circuit. *IEEE Trans. Circuits Syst. Regul. Pap.* **2013**, *60*, 3107–3116. [CrossRef]
45. Toledo, P.; Crovetti, P.; Aiello, O.; Alioto, M. Fully Digital Rail-to-Rail OTA With Sub-1000-Mm^2 Area, 250-mV Minimum Supply, and nW Power at 150-pF Load in 180 Nm. *IEEE Solid-State Circuits Lett.* **2020**, *3*, 474–477. [CrossRef]
46. Toledo, P.; Crovetti, P.; Aiello, O.; Alioto, M. Design of Digital OTAs With Operation Down to 0.3 V and nW Power for Direct Harvesting. *IEEE Trans. Circuits Syst. Regul. Pap.* **2021**, *68*, 3693–3706. [CrossRef]
47. Toledo, P.; Crovetti, P.; Klimach, H.; Bampi, S.; Aiello, O.; Alioto, M. A 300mV-Supply, Sub-nW-Power Digital-Based Operational Transconductance Amplifier. *IEEE Trans. Circuits Syst. II Express Briefs* **2021**, *68*, 3073–3077. [CrossRef]
48. Toledo, P.; Rubino, R.; Musolino, F.; Crovetti, P. Re-Thinking Analog Integrated Circuits in Digital Terms: A New Design Concept for the IoT Era. *IEEE Trans. Circuits Syst. II Express Briefs* **2021**, *68*, 816–822. [CrossRef]
49. Palumbo, G.; Scotti, G. A Novel Standard-Cell-Based Implementation of the Digital OTA Suitable for Automatic Place and Route. *J. Low Power Electron. Appl.* **2021**, *11*, 42. [CrossRef]
50. Toledo, P.; Crovetti, P.S.; Klimach, H.D.; Musolino, F.; Bampi, S. Low-Voltage, Low-Area, nW-Power CMOS Digital-Based Biosignal Amplifier. *IEEE Access* **2022**, *10*, 44106–44115. [CrossRef]
51. Privitera, M.; Crovetti, P.S.; Grasso, A.D. A Novel Digital OTA Topology with 66-dB DC Gain and 12.3-kHz Bandwidth. *IEEE Trans. Circuits Syst. II Express Briefs* **2023**, *early access*. [CrossRef]
52. Ramirez-Angulo, J.; Carvajal, R.G.; Tombs, J.; Torralba, A. Low-Voltage CMOS Op-Amp with Rail-to-Rail Input and Output Signal Swing for Continuous-Time Signal Processing Using Multiple-Input Floating-Gate Transistors. *IEEE Trans. Circuits Syst. II Analog Digit. Signal Process.* **2001**, *48*, 111–116. [CrossRef]
53. Ramirez-Angulo, J.; Lopez-Martin, A.J.; Carvajal, R.G.; Chavero, F.M. Very Low-Voltage Analog Signal Processing Based on Quasi-Floating Gate Transistors. *IEEE J. Solid-State Circuits* **2004**, *39*, 434–442. [CrossRef]
54. Rajput, K.K.; Saini, A.K.; Bose, S.C. DC Offset Modeling and Noise Minimization for Differential Amplifier in Subthreshold Operation. In Proceedings of the 2010 IEEE Computer Society Annual Symposium on VLSI, Lixouri, Greece, 5–7 July 2010; pp. 247–252.

55. Di Cataldo, G.; Grasso, A.D.; Pennisi, S.; Scotti, G.; Trifiletti, A. CMOS Non-Tailed Differential Pair: CMOS Non-Tailed Differential Pair. *Int. J. Circuit Theory Appl.* **2015**, *44*, 1468–1477. [CrossRef]
56. Khateb, F. Bulk-Driven Floating-Gate and Bulk-Driven Quasi-Floating-Gate Techniques for Low-Voltage Low-Power Analog Circuits Design. *AEU-Int. J. Electron. Commun.* **2014**, *68*, 64–72. [CrossRef]