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0.4-V, 81.3-nA Bulk-Driven Single-Stage CMOS OTA with Enhanced Transconductance

Andrea Ballo, Alfio Dario Grasso and Salvatore Pennisi *

DIEEI (Dipartimento di Ingegneria Elettrica Elettronica e Informatica), University of Catania, 95125 Catania, Italy
* Correspondence: salvatore.pennisi@unict.it

Abstract: The paper describes a single-stage operational transconductance amplifier suitable for very-low-voltage operation in power-constrained applications. The proposed circuit avoids the tail current generator in the differential pair while preventing pseudo-differential operation. Moreover, the adoption of positive feedback allows increasing the stage transconductance while minimizing the current consumption. Experimental measurements on prototypes implemented in a standard CMOS 180-nm technology, show superior performance as compared to the state of the art.

Keywords: bulk-driven transistors; low power; low voltage; OTA; positive feedback

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1. Introduction

The operational transconductance amplifier (OTA) is a key element for analog CMOS integrated circuit (IC) design as it is virtually present in any monolithic electronic system that bases its performance on accurate high-gain closed-loop configurations. However, designing OTAs with acceptable performance is becoming increasingly difficult in modern CMOS technologies. In fact, nanoscale nodes require supply voltages of less than 1 V [1–6]. Furthermore, extending the autonomy of battery-powered or even harvested-powered devices places severe constraints on the current consumption, and this is particularly detrimental to analog and mixed-signal implementations.

The design approaches that are usually exploited to implement an OTA with stringent low-power and low-voltage constraints are based on the adoption of bulk-driven (body-driven) transistors [7–14], on weak inversion operation [15–22], or a combination of both of them [23–33].

The body-driven approach is especially suited in applications where the supply voltage is comparable or even lower than the transistor threshold voltage and a wide input common-mode range (ideally rail-to-rail) is required at the same time [2,9]. However, the main drawback of the bulk-driven approach is that the bulk transconductance is about 60 to 90% lower than the gate transconductance for equal bias current and transistor dimensions, leading to both poor DC gain and gain-bandwidth performance. At the cost of increased area occupation, the adoption of multistage OTAs can overcome the former issue of DC gain [11,29,31] but the gain-bandwidth penalty can be overcome only by increasing the input stage transconductance and, in turn, the quiescent current of the input stage. As an interesting alternative, the input equivalent transconductance of a bulk-driven differential pair can be increased by exploiting partial positive feedback techniques [10,12,34,35].

Following the latter approach, we describe in this paper a bulk-driven single-stage OTA whose topology is a modified version of the one developed in [4]. The solution boosts the bulk transconductance of the differential pair to a level similar to or even higher than that of a conventional gate-driven stage [36]. Compared to the solution in [12], the proposed one is characterized by some distinctive features. Namely, subthreshold-biased MOS transistors are exploited to meet ultra-low-voltage supply requirements, which are further reduced by eliminating the tail current generator in the differential pair. Moreover, the pseudo-differential behavior caused by the elimination of the tail generator is

avoided, approaching a truly differential OTA performance. These strategies, together with an optimized design, have resulted in a single-stage OTA with excellent performance, validated through experimental measurements on prototypes designed in standard 180-nm CMOS technology.

The paper is organized as follows. Section 2 describes the principle of operation of the circuit and related derivation of main design equations. Section 3 reports the validation of the OTA through experimental measurements and the comparison with other solutions in the literature, showing a significant advance of the state of the art. Finally, some concluding remarks are offered in Section 4.

2. The Proposed Amplifier

The schematic diagram of the proposed single-stage OTA is shown in Figure 1. Where not explicitly drawn, the bulk terminal of each transistor is assumed to be connected to its source. The circuit is made up of the bulk-driven non-tailed differential pair M_1–M_2 loaded by current mirror M_3–M_4 and M_5–M_6. The additional current mirror M_9–M_{10} implements differential to single-ended conversion. The bias current in M_1 and M_2 is set through the diode-connected transistor M_0, which generates voltage V_B to be applied to the gates of M_1–M_2. The bulk terminal of M_0 is biased by the voltage divider R_1–R_2, which is basically the analog ground i.e., the quiescent input voltage of the pair. More specifically, M_0 and M_1 (M_2) act as a current mirror provided that $V_{in-} = V_{in+} = (R_1 V_{SS} + R_2 V_{DD})/(R_1 + R_2)$, and in this case we get $I_{D1,2} = I_{Bias}(W/L)_{1,2}/(W/L)_0$.

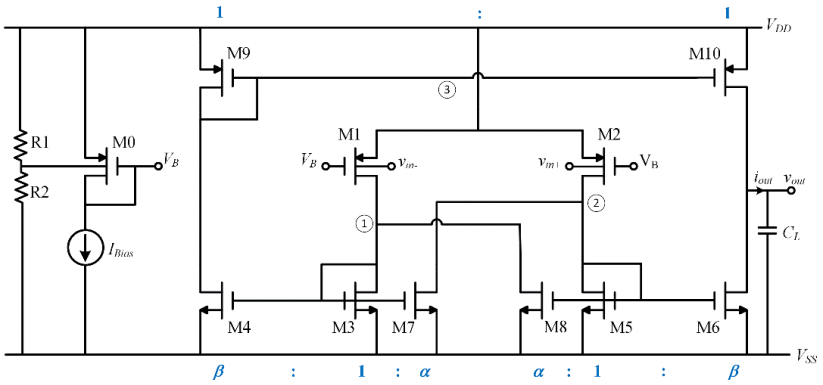


Figure 1. Proposed single-stage OTA.

Like the solution proposed in [12,36], an additional cross-coupled load made up of transistors M_7 and M_8 is exploited to produce a local positive feedback that boosts the equivalent differential transconductance, G_m. Indeed, assuming $(W/L)_9 = (W/L)_{10}$, i.e., unitary current mirror M_9–M_{10}, and defining parameters α and β as

$$\alpha = \frac{(W/L)_7}{(W/L)_3} = \frac{(W/L)_8}{(W/L)_5} \tag{1}$$

and

$$\beta = \frac{(W/L)_4}{(W/L)_3} = \frac{(W/L)_6}{(W/L)_5}, \tag{2}$$

straightforward small-signal analysis gives

$$i_{d3} = \frac{g_{mb1,2}}{(1+\alpha)(1-\alpha)}(\alpha v_{in+} - v_{in-}), \tag{3a}$$

$$i_{d5} = \frac{g_{mb1,2}}{(1+\alpha)(1-\alpha)}(-v_{in+} + \alpha v_{in-}) \tag{3b}$$

where $g_{mb1,2}$ is the bulk transconductance of M_1 and M_2.

It can be noted that, because of the absence of the tail current generator, M_1–M_2 is a pseudo-differential pair. However, thanks to the action of M_7 and M_8, the whole OTA provides a quasi-differential behavior. Indeed, Equation (3a,b) show that i_{d3} and i_{d5} depend on a α-weighted difference between v_{in+} and v_{in-}, with ideal truly differential behavior achieved for α approaching 1.

Assuming a balanced differential input, i.e., $v_{in+} = v_d/2$ and $v_{in-} = -v_d/2$, and no mismatches in the OTA current mirrors, the differential-mode transconductance, G_m, is found to be

$$G_m = \frac{i_{out}}{v_{in+} - v_{in-}} = \beta \frac{i_{d5} - i_{d3}}{v_d} = \frac{\beta}{1-\alpha} g_{mb1,2} \tag{4}$$

where i_{out} is the OTA short-circuit output current.

It is apparent that the differential-mode transconductance can be significantly increased by choosing suitable values of the transistor aspect ratios in (1) and (2). Of course, parameter α must be lower than 1 to ensure that the magnitude of the local positive feedback is kept below unity, to prevent the amplifier from becoming a latch. Although values very close to 1 can, in principle, generate a very large G_m increase, it is advisable to set α less than 0.9 to have a sufficient safety margin against process mismatches [34,35], while achieving a quite good differential behavior.

The complete OTA open loop transfer function, taking into account the parasitic capacitances and capacitive load, is expressed by

$$A_{OL}(s) = G_m r_o \frac{1 - s\frac{C_{db1,2}}{g_{mb1,2}}}{1 + sr_o C_L^*} \cdot \frac{1 + s\frac{C_1}{2(1-\alpha)g_{m3,4}}}{1 + s\frac{C_1}{(1-\alpha)g_{m3,4}}} \cdot \frac{1 + s\frac{C_2}{2(1-\alpha)g_{m5,6}}}{1 + s\frac{C_2}{(1-\alpha)g_{m5,6}}} \cdot \frac{1 + s\frac{C_3}{2g_{m9,10}}}{1 + s\frac{C_3}{g_{m9,10}}} \approx \frac{G_m r_o}{1 + sr_o C_L^*}, \tag{5}$$

where r_o is the OTA output resistance equal to $r_{d10}//r_{d6}$, C_L^* is the sum of the load capacitance and the parasitic capacitances and C_i, I = 1, 2, 3, represents the total parasitic capacitance at nodes 1, 2 and 3. Assuming C_L is much higher than the parasitic capacitances, the high-frequency poles and zeros can be neglected and the rightmost approximation in (5) holds. As usual, the gain-bandwidth product is therefore given by

$$GBW \approx \frac{G_m}{C_L} = \frac{\beta}{1-\alpha} \frac{g_{mb1,2}}{C_L} \tag{6}$$

From Equation (3a,b) we can also evaluate the OTA transconductance under common-mode input signal (i.e., $v_{in+} = v_{in-} = v_{cm}$). Ideally, in this case, the symmetry of the topology would nullify the common-mode transconductance, $G_{m,cm}$, as can be easily seen if we take the difference of i_{d3} and i_{d5}. To have a more realistic result, we should consider the mismatches between the bulk transconductances of M_1 and M_2 and parameter α, by defining

$$i_{d1} = \left(g_{mb1,2} - \frac{\Delta g_{mb}}{2}\right) v_{cm} \tag{7}$$

$$i_{d2} = \left(g_{mb1,2} + \frac{\Delta g_{mb}}{2}\right) v_{cm} \tag{8}$$

$$i_{d8} = \left(\alpha + \frac{\Delta\alpha}{2}\right) i_{d5} \tag{9}$$

$$i_{d7} = \left(\alpha - \frac{\Delta\alpha}{2}\right) i_{d3} \tag{10}$$

After some algebraic manipulations we get

$$G_{m,cm} = \beta \frac{i_{d5} - i_{d3}}{v_{cm}} = \frac{2\beta g_{mb1,2}}{1 - \alpha^2 + \left(\frac{\Delta\alpha}{2}\right)^2} \left(\alpha \frac{\Delta g_{mb}}{2g_{mb1,2}} + \frac{\Delta\alpha}{2} + \frac{\Delta g_{mb}}{2g_{mb1,2}}\right) \approx \frac{\beta}{1-\alpha} g_{mb1,2} \left(\frac{\Delta g_{mb}}{g_{mb1,2}} + \frac{\Delta\alpha}{1+\alpha}\right) \tag{11}$$

where in the approximation we neglected the term $\left(\frac{\Delta\alpha}{2}\right)^2$ in the denominator because it is much lower than 1.

It is seen that the common-mode transconductance is proportional to the sum of the relative tolerances of $g_{mb1,2}$ and parameter α. Additional degradation is also caused by mismatches in the β parameter and in the current mirror gain M_9–M_{10}, here neglected for simplicity. All these errors can be relevant due to the simple current mirror topologies adopted and can be counteracted by choosing large MOSFET channel lengths and careful layout.

By taking the ratio of (4) and (8) one can evaluate the common-mode rejection ratio (*CMRR*) which, as a result, is exclusively dependent on the last factor between brackets in (8).

3. Results and Comparison

The circuit in Figure 1 was designed and fabricated using a standard 180-nm CMOS process supplied by STMicroelectronics. Note that like all the recent sub-350-nm processes, the adopted technology allows the use of triple-well NMOS transistors, thus allowing independent control of the bulk terminals. The circuit layout and the chip microphotograph are shown in Figure 2. The occupied area is 866.25 μm^2.

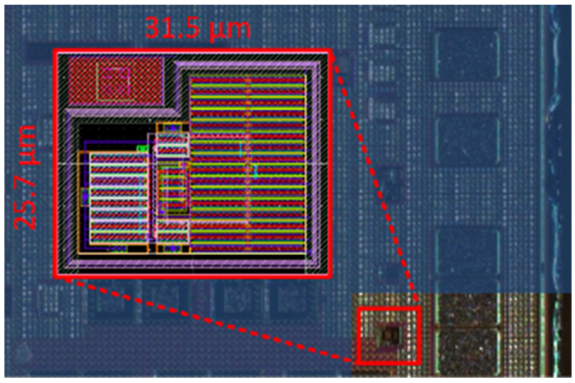


Figure 2. Layout and chip microphotograph of the proposed OTA.

The nominal supply voltage and bias current is set equal to 400 mV and 5 nA, respectively, forcing all the transistors to work in the subthreshold region. The total nominal DC current consumption is equal to 81.35 nA. Note that with such value of V_{DD} the potential forward biasing of the bulk-source pn junction is inherently avoided.

According to the adopted transistor dimensions summarized in Table 1, parameters α and β are nominally equal to 0.83 and 15, respectively. Consequently, the bulk transconductance of M_1 and M_2, equal to 4.71 µA/V, is boosted by about 88 times, yielding from (6) a theoretical *GBW* equal to about 5 kHz for a nominal load capacitance of 150 pF.

Table 1. Transistor dimensions.

Device	Value (µm/µm)
M_0, M_1, M_2	3/0.26 (×2)
M_3, M_5	6/0.26
M_4, M_6	6/0.26 (×15)
M_7, M_8	5/0.26
M_9, M_{10}	6/0.26 (×4)

The measured open-loop Bode plots (magnitude and phase) of a representative OTA sample is depicted in Figure 3 while Figure 4 shows the measured gain for all the samples superimposed to the simulated one. Table 2 summarizes the measured main performance

metrics averaged over the ten samples. The variability of the parameters is evaluated through the relative standard deviation which is lower than about 30% in all cases.

Figure 3. Measured open-loop AC response for C_L = 150 pF.

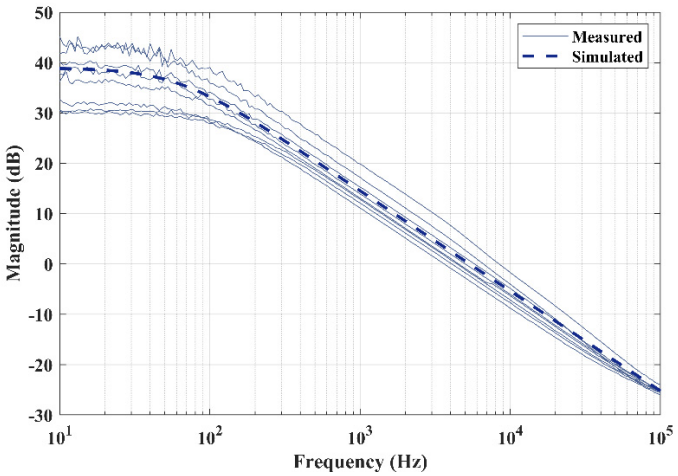


Figure 4. Measured open-loop gain for all the samples superimposed to simulations for C_L = 150 pF.

Table 2. Average main performance parameters over 10 samples for C_L = 150 pF.

Parameter	Average	Min	Max
DC Gain (dB)	37.7	30.1	45.2
GBW (kHz)	5.56	3.64	8.84
Phase Margin (deg)	79.3	66.9	87.5
Positive Slew Rate (V/ms)	7.43	6.34	8.52
Negative Slew Rate (V/ms)	7.36	6.28	8.74

Figure 5 shows the transient response of the same sample in unity-gain feedback configuration for C_L equal to 30 pF (loading capacitance equal to 30 pF represents the total

load due to the package, the oscilloscope probe, and the PCB), 150 pF and 1 nF, confirming that the approximated single-pole transfer function in (5) well describes the OTA behavior.

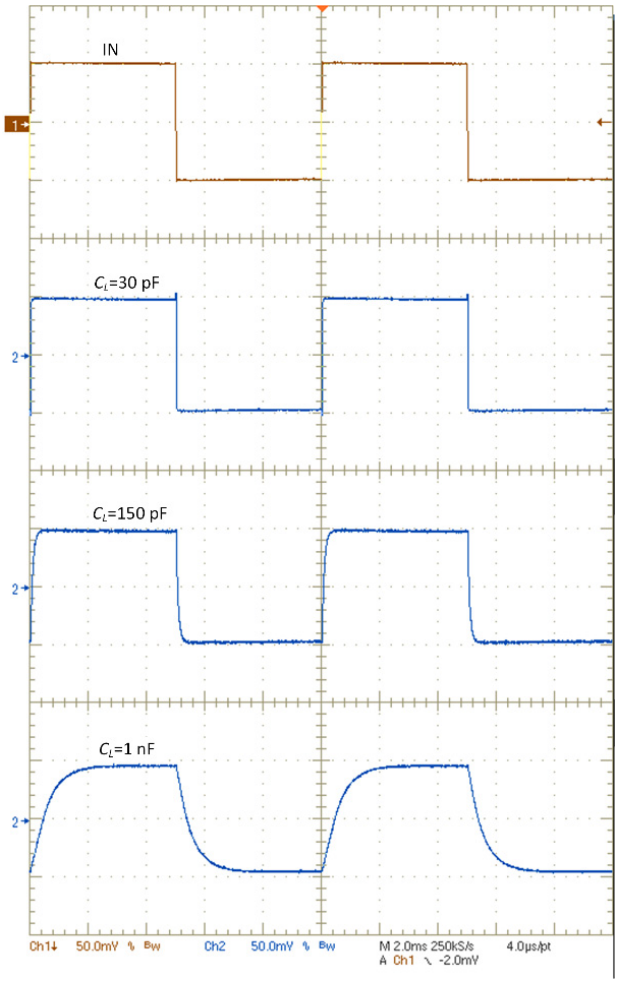


Figure 5. Measured step response in unity gain configuration for different capacitive loads.

The robustness of the OTA over process, temperature and mismatch variations is assessed through corner simulations and Monte Carlo analysis. Results are summarized in Tables 3–6 where the main amplifier specifications are simulated over three different temperatures (namely −10 °C, 27 °C and 85 °C) in all transistor corners, showing that the amplifier is stable in all conditions. Moreover, Monte Carlo simulation results over 100 runs confirm the robustness of the OTA, the relative standard deviation being lower than 25% in all cases.

Table 3. Corner and Monte Carlo analysis results for $T = -10$ °C.

Parameter	TT	SS	SF	FS	FF	Monte Carlo	
						μ	σ
Power (nW)	26.1	19	18.3	20.5	29.8	24	4.6
DC Gain (dB)	34.1	23.6	20.4	43.6	41.7	33	9.7
GBW (kHz)	1.51	0.39	0.25	3.56	4.13	1.94	0.48
Phase Margin (deg)	88.9	93.2	94.7	77.6	77.8	86.1	14.3
Positive Slew Rate (V/ms)	7.37	8.07	7.85	6.8	6.6	7.33	0.47
Negative Slew Rate (V/ms)	7.32	8.04	7.82	6.78	6.6	7.29	0.46

Table 4. Corner and Monte Carlo analysis results for T = 27 °C.

Parameter	TT	SS	SF	FS	FF	Monte Carlo	
						μ	σ
Power (nW)	32.5	30.9	31.6	32.1	33.6	32.4	2.6
DC Gain (dB)	44.6	42.3	40	45.7	45.2	44.4	5.7
GBW (kHz)	5.66	4.06	3.3	6.32	6.42	5.75	1.12
Phase Margin (deg)	66.2	75.5	80	62.9	62.7	67.9	15.1
Positive Slew Rate (V/ms)	7.45	8.23	8.01	6.89	6.65	7.43	0.48
Negative Slew Rate (V/ms)	7.37	8.14	7.92	6.85	6.6	7.36	0.47

Table 5. Corner and Monte Carlo analysis results for T = 85 °C.

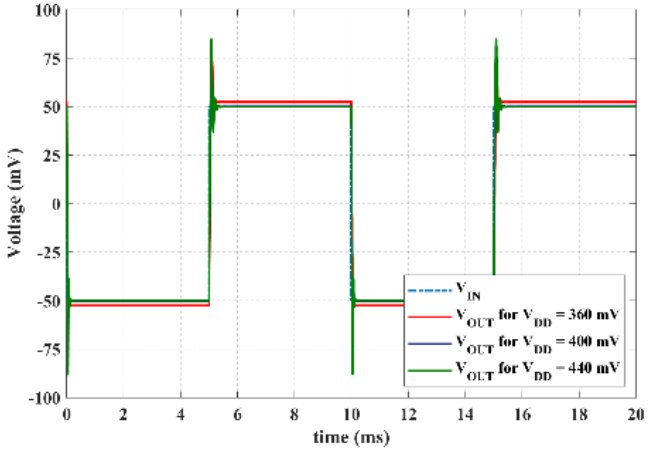
Parameter	TT	SS	SF	FS	FF	Monte Carlo	
						μ	σ
Power (nW)	36.6	35.6	37	36.5	37.8	36.8	2.4
DC Gain (dB)	44.7	45.1	44.2	44.8	44.2	45	4.9
GBW (kHz)	5.94	5.87	5.71	6.02	5.94	6.28	1.48
Phase Margin (deg)	61.4	60.8	62.1	62.1	62.7	64.2	17.6
Positive Slew Rate (V/ms)	7.53	8.33	8.15	6.96	6.74	7.51	0.49
Negative Slew Rate (V/ms)	7.44	8.23	8.01	6.91	6.66	7.43	0.47

Table 6. Comparison With Other Sub-1-V OTAs.

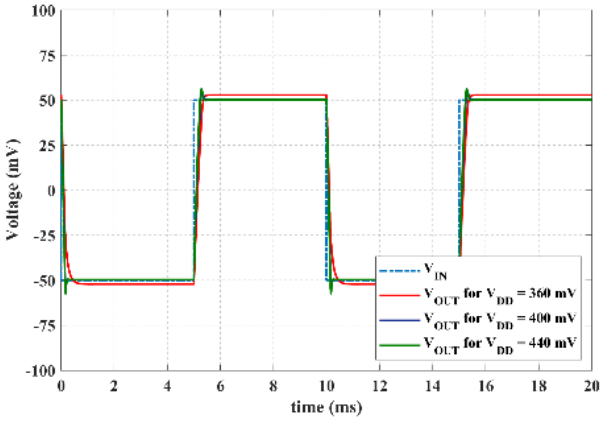
Ref. #	[7]	[18]	[24]	[12]	[10]	[19]	[13]	[25]	[20]	[27]	[22]	[11]	[28]	[30]	[29]	[31]	This Work
Year	1998	2005	2007	2007	2011	2012	2013	2014	2014	2015	2016	2016	2018	2020	2020	2020	2022
Technology [µm]	2	0.18	0.35	0.35	0.18	0.18	0.35	0.13	0.18	0.065	0.18	0.18	0.18	0.18	0.18	0.065	0.18
Area [mm^2]	1.515	17	0.06	0.0532	0.063	0.057	0.1575	0.083	0.057	0.00495	0.036	0.0198	0.0082	0.0085	0.0098	0.002	8.66×10^{-4}
Supply [V]	1	0.5	0.6	1	1	0.8	1	0.25	0.5	0.5	0.5	0.7	0.3	0.3	0.3	0.25	0.4
C_L [pF]	22	20	15	17	1	8	15	15	30	3	40	20	20	30	30	15	150
DC gain [dB]	49	62	69	76.2	64	51	88	60	70	46	77	57	63	65	98.1	70	38
I_{bias} [µA]	300	150	0.9	358	130	1.5	197	0.072	0.15	366	0.14	36	0.056	0.042	0.04333	0.10400	0.08135
Power [µW]	300	75	0.54	358	130	1.2	197	0.018	0.075	183	0.07	25.2	0.0168	0.0126	0.013	0.026	0.03254
GBW [MHz]	1.3	10	0.011	8.1	2	0.057	11.67	0.002	0.018	38	0.004	3	0.0028	0.00296	0.0031	0.0095	0.00556
PM [°]	57	60	65		45	60	66	53	55	57	56	60	61	52	54	88	79
SR [V/µs] [a]	1.6	2	0.015	3.88	0.7	0.14	1.95	0.0007	0.003	43	0.002	2.8	0.0071	0.00415	0.0091	0.002	0.0074
CMRR [dB]	56.2	65	74.5	70.5	88	65	40	-	-	35	55	19	72	110	60	62.5	36
PSRR [dB]	60.8	43	-	45	70	-	40	-	-	37	52	52	62	56	61	38	30
Operation mode	BD	GD	BD	BD	BD	GD	BD	BD	GD	BD	GD	BD	BD	BD	BD	BD	BD
Stage #	2	2	2	1	2	1	2	2	2	3	2	3	2	2	3	3	1
$IFOM_S$ [MHz·pF/µA]	0.10	1.33	0.18	0.38	0.02	0.30	0.89	0.42	3.60	0.31	1.14	1.67	1.00	2.11	2.15	1.37	10.25
$IFOM_L$ [(V/µs)·pF/µA]	0.12	0.27	0.25	0.18	0.01	0.75	0.15	0.15	0.60	0.35	0.57	1.56	2.54	2.96	6.30	0.29	13.64
$IFOM_{AS}$ [MHz·pF/µA·mm^2]	0.06	78.43	3.06	7.23	0.24	5.33	5.64	5.02	63.16	62.92	31.75	84.18	121.95	248.74	219.00	685.10	11,838.33
$IFOM_{AL}$ [(V/µs)·pF/µA·mm^2]	0.08	15.69	4.17	3.46	0.09	13.10	0.94	1.76	10.53	71.20	15.87	78.56	309.23	348.74	642.86	144.23	15,745.41

[a] average value.

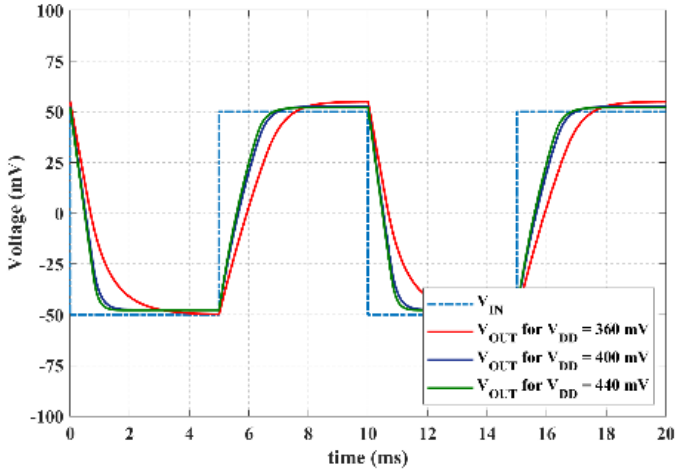
Finally, the robustness over supply voltage variations is assessed in Figure 6 where the simulated step response in unity-gain configuration is reported for different capacitive load conditions and ±10% voltage variations.



(**a**)



(**b**)



(**c**)

Figure 6. Simulated transient response for supply voltage variations of ±10% for: (**a**) C_L = 30 pF, (**b**) C_L = 150 pF and (**c**) C_L = 1 nF.

Table 6 compares the proposed OTA with other experimentally tested solutions in the literature working with a supply voltage lower than 1 V. In order to assess the trade-off between speed performance and total bias current, I_T, (and, indirectly, power consumption) for a given load, we adopt in Table 3 the traditional figures of merit.

$$IFOM_S = \frac{GBW}{I_T} C_L \tag{12}$$

$$IFOM_L = \frac{SR}{I_T} C_L \tag{13}$$

where SR is the average slew rate. To take into account also the area occupation, two additional figures of merit are adopted:

$$IFOM_{AS} = \frac{\omega_{GBW}}{Area \cdot I_T} C_L \tag{14}$$

$$IFOM_{AL} = \frac{SR}{Area \cdot I_T} C_L \tag{15}$$

It is apparent that the proposed solution exhibits the best small-signal performance with a 4.77 X and 17.28 X improvement of $IFOM_S$ and $IFOM_{AS}$ over the best solutions in Table 3. Similar conclusions apply to the large-signal performance, where the improvement of $IFOM_L$ and $IFOM_{AL}$ is equal to 2.16 X and 24.49 X. Note, however, that the gain of the proposed solution is the lowest one, being a single-stage OTA.

4. Conclusions

In this paper a power efficient single-stage, fully-differential bulk-driven OTA is introduced. The circuit is particularly suited for ultra-low-voltage applications since a novel circuit technique allows eliminating the tail current generator. Nano-power and very-low-voltage features enable operation of battery-less sensor nodes directly powered by single solar cells or operating with scaled voltage to reduce the power consumption of the digital subsection. The proposed single-stage can be profitably exploited also for the implementation of multi-stage OTAs using simple additional common-source stages to increase the total gain.

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Conflicts of Interest: The authors declare no conflict of interest.

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