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Single-Branch Wide-Swing-Cascode Subthreshold GaN Monolithic Voltage Reference

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Abstract: A voltage reference generator in GaN IC technology for smart power applications is described, analyzed, and simulated. A straightforward design procedure is also highlighted. Compared to previous low-power monolithic solutions, the proposed one is based on a single branch and on transistors operating in a subthreshold. The circuit provides a nearly 2.7 V reference voltage under 4 V to 24 V supply at room temperature and with typical transistor models. The circuit exhibits a good robustness against large process variations and improves line regulation (0.105 %V) together with a reduction in area occupation (0.05 mm^2), with a reduced current consumption of 2.7 µA (5 µA) in the typical (worst) case, independent of supply. The untrimmed temperature coefficient is 200 ppm/°C.

Keywords: AlGaN/GaN HEMT; smart power; wide bandgap; voltage reference; planar integration

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1. Introduction

Voltage reference generators are fundamental building blocks used in the power management section of virtually any integrated circuit (IC) system. They provide a stable and accurate reference output voltage, V_{REF}, that is used by other blocks to work correctly. Examples of systems that exploit voltage references for proper function include switching power converters, linear regulators, oscillators, PLLs, A/D and D/A converters, operational amplifiers, etc. The characteristics of V_{REF} are usually measured in terms of insensitivity to supply voltage variations (either as line regulation, $\Delta V_{REF}/\Delta V_{DD}$, or power supply rejection, *PSR*, as a function of frequency) and to temperature (voltage drift or temperature coefficient, $TC = \Delta V_{REF}/\Delta T$). Insensitivity to load variations (load regulation, $\Delta V_{REF}/\Delta I_{LOAD}$) is another important feature that is often achieved by a following voltage regulator circuit. Other sources of inaccuracy in IC implementations are caused by process variations and mismatches.

After the seminal work carried out by Widlar in bipolar technologies [1] and the related following developments, CMOS voltage references have been devised, which were based at first on the Widlar bandgap technique [2–4] and, later, on alternative approaches more suitable under low supply voltages [5–8] and low currents [9–14], specifically aimed at satisfying requirements of modern battery-operated, energy-harvested, and wearable/implantable electronics.

In these last years, the emergence of GaN (gallium nitride) HEMT (high electron mobility transistor) technologies have attracted considerable interest by the power IC design community. Indeed, GaN HEMT processes are ultimately being developed in an attempt to allow for the realization of next-generation, fully integrated GaN power converters integrating both high-voltage power devices and low-voltage peripheral driving devices with mixed-signal functional blocks into the same substrate (smart power). A monolithic solution is in fact preferable as, in addition to minimizing the area, the cost, and the packaging effort and to improving the reliability, this solution also reduces the

interconnection parasites between the driver and the power switch. This allows for all the potential advantages of the wide bandgap GaN devices, which can be summarized into higher power density, breakdown voltage, operating temperature, and frequency and lower on-resistance when compared to traditional power MOS devices [15–18].

In the field of smart power electronics, the implementation of a monolithic GaN gate driver for a GaN power switch is one of the major emerging research targets [19–26], as it is one of the main building blocks of power converters. Of course, a GaN gate driver needs auxiliary sub circuits to operate correctly, including a voltage reference generator. Unfortunately, the available GaN technologies for smart power ICs are far from mature and suffer from a large spread in process parameters, especially in terms of device threshold voltages. This is a severe limitation when implementing a voltage reference that must provide a reliable, maximally constant voltage under the extreme technology corners other than in a wide temperature range. In this context, previous GaN solutions are basically focused on minimizing the temperature coefficient of the reference voltage, but disregard the problem that different samples from different lots may provide very different reference voltage values owing to the very large parameter spread.

In this paper, the topology of a voltage reference generator designed in a commercial AlGaN/GaN technology for smart power applications [27,28] is presented. The design is not trivial and takes into consideration the limitations of the technology that provide only n-channel enhancement (E) and depletion (D) devices but lack a complementary p-channel transistor and p-n junctions. In particular, since p-n junctions are essential for bandgap references, new methods that allow for the design of a low-TC reference generator operating in the wide temperature range offered by the GaN technology and in a wide supply range from around 4 V to 24 V, as required by consumer and automotive applications, must be devised. In addition, low area occupation and low current consumption are key features that are more and more in demand also from the automotive sector. Indeed, the number of electronic devices to be embedded in the vehicle is constantly increasing and this should not significantly impact the battery autonomy.

The paper is organized as follows. Section 2 illustrates the solutions found in the literature. The proposed architecture as well as an accurate design methodology are then presented in Section 3. The main simulation results are summarized in Section 4. The authors' conclusions are drawn in Section 5.

2. Previous Art

The simplest and most widely used method for implementing a voltage reference in a GaN IC exploits an external zener diode. However, this causes non-negligible drawbacks such as the increase in inductive parasitic effects due to the bonding wires and, above all, large temperature drift in V_{REF}. It is therefore essential to avoid the zener diode and to realize the voltage reference in a monolithic form to counteract these drawbacks.

2.1. Schottky-Diode-Based GaN Voltage Reference

The first monolithic voltage reference in AlGaN/GaN HEMT and Schottky diodes technology [28] is depicted in Figure 1 [29]. The depletion transistor, Q_{D1}, implements a current source and is operated in the subthreshold regime to obtain relatively low power consumption (0.8 mA at room temperature). It should be noted that Q_{D1} must also provide enough current driving capability to the external load to prevent V_{REF} from being affected by the load because no additional voltage regulator was used in this application. Diodes D_3 and D_4 implement a source degeneration of Q_{D1} that stabilizes the current magnitude against process tolerances (for instance, variations of threshold voltage of Q_{D1}). Moreover, D_3 and D_4 also allow for compensation of the effects that temperature changes have onto D_1 and D_2.

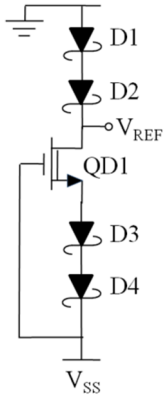

Figure 1. Schottky-diode-based GaN voltage reference [29].

The output reference voltage is expressed by

$$V_{REF} = -V_{D1} - V_{D2}. \quad (1)$$

A *TC* of less than 0.5 mV/°C was reported in [29].

It should be noted that the voltage drop across D_3 and D_4 must be smaller than the magnitude of the threshold voltage of Q_{D1} to ensure the transistor turn-on.

This early solution suffers from several drawbacks. A negative supply voltage (−9 V) is indeed required; otherwise, V_{REF} would depend linearly on V_{DD}, which means unitary line regulation. A relatively high temperature coefficient is also observed and Schottky diodes are not always offered by commercial GaN platforms. Finally, a high current consumption is found.

To solve these drawbacks, two reference voltage generators based on two different current mirrors were proposed in [30].

2.2. Reference Voltage Generators Based on Current Mirrors

The first solution discussed in [30] is shown in Figure 2 and is based on the Wilson current mirror (Q_{E1}–Q_{E3}), in which the reference current $I_{REF} = I_{Q,D1}$ is realized through Q_{D1} and the current limiting resistor R_1. As shown in [30], the circuit's loop gain ensures that approximately the same current I_{REF} flows in the two branches.

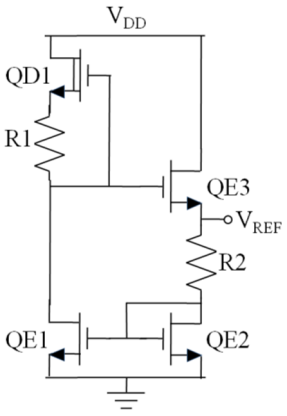

Figure 2. GaN voltage reference based on Wilson current mirror [30].

By setting R_1 suitably large, we obtain a very small I_{REF} value, so that Q_{D1} is biased in the near threshold, i.e., $V_{GS,D1}$ is approaching the (negative) threshold voltage $V_{TH,D}$, whereas $V_{GS,E1}$ and $V_{GS,E2}$ are approaching the threshold voltage $V_{TH,E}$:

$$I_{REF} = \frac{V_{SG,D1}}{R_1} \approx -\frac{V_{TH,D}}{R_1} \quad (2)$$

It is shown in [30] that the threshold voltages of the D-type transistor and of the E-type transistor were both proportional to the absolute temperature (PTAT), with the TC of the D-GaN smaller than that of the E-GaN. For the specific adopted technology, setting V_{DS} = 1 V, it is seen that $V_{TH,D}$ increases with temperature by 1.1 mV/°C, whereas $V_{TH,E}$ increases with temperature by 4.1 mV/°C. As a result, I_{REF} will exhibit a complementary to absolute temperature (CTAT) behavior.

Equally sized transistors Q_{E1}–Q_{E2} of the Wilson current mirror ensure, at a first approximation, the same drain current I_{DE1} and I_{DE2}; hence, we have $I_{DE2} \approx I_{DE1} = I_{REF}$. As a consequence, V_{REF} is given by

$$V_{REF} = V_{GS,E2} + I_{D,E2}R_2 \approx V_{TH,E1-E2} - \frac{R_2}{R_1}V_{TH,D1}. \quad (3)$$

From the above considerations, it is seen that an ideally zero *TC* can be achieved by suitably setting the ratio R_2/R_1 to 4.1/1.1 = 3.72.

The main drawbacks of this solution are listed below. V_{REF} is still dependent on V_{DD} because the drain-to-source voltage seriously affects the threshold voltage of the E-GaN (with a slope of −36.3 mV/V [30]). A large area occupation is caused by the required large values of R_1 and R_2. Unavoidable mismatch affects I_{DE1} and I_{DE2} because Q_{E1} and Q_{E2} work at substantially different V_{DS} values.

A second improved solution was then presented in the same paper [30], as described below. A wide-swing-cascode structure Q_{E1}–Q_{E4} is used to suppress the V_{DS} variations of Q_{E1}–Q_{E2} and to accurately set $I_{DE1} = I_{DE2}$. Moreover, Q_{E3} in Figure 2 is changed into a depletion device, Q_{D2}, in Figure 3. This choice allows us to decrease the minimum required V_{DD} that can be now from 3.9 V to 24 V, thanks to the negative threshold of Q_{D2}.

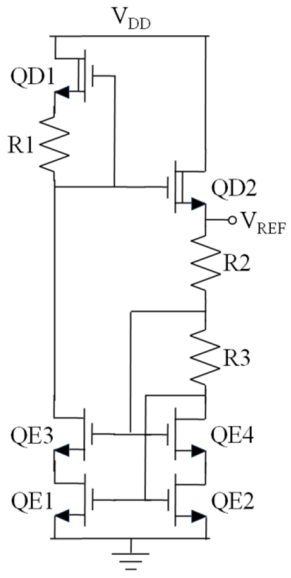

Figure 3. GaN voltage reference based on wide-swing-cascode current mirror [30].

With a similar analysis performed before for the circuit in Figure 2, we obtain the expression of V_{REF} for the circuit in Figure 3:

$$V_{REF} \approx V_{TH,E} - \frac{R_2 + R_3}{R_1}V_{TH,D}. \quad (4)$$

Again, as in (3), by suitably selecting the ratio $(R_2 + R_3)/R_1$, the *TC* of V_{REF} can be ideally nullified.

This solution is still affected by some drawbacks. V_{REF} is residually dependent on V_{DD} because current I_{D1} in saturation linearly depends on V_{DS} through the Early effect,

and V_{DS} is in turn the result of the V_{DD} voltage divider between the output impedance of Q_{D1} and that of the current mirror (drain of Q_{E3}), which are both high impedances. A large area occupation is still caused by the required large values of the resistors. Two branches are used.

2.3. 2-T Voltage Reference

The 2-T voltage reference was recently proposed in [31] and its schematic diagram is shown in Figure 4. It is constituted by only one branch made up of two transistors, a depletion device, Q_{D1} (acting as current source and a diode-connected enhancement device) and Q_{E1} (acting as a diode-connected load). From inspection, we see that $V_{GS,E2} = -V_{GS,D1} = V_{REF}$ with both transistors currents equal. Assuming Q_{E1} and Q_{D1} in saturation with the expression of the currents in the form $I_D = k_n(V_{GS} - V_T)^2$, where k_n is the transconductance factor, we have

$$V_{REF} \approx \frac{\sqrt{\frac{k_{n,E}}{k_{n,D}}}V_{TH,E} - V_{TH,D}}{1 + \sqrt{\frac{k_{n,E}}{k_{n,D}}}}. \tag{5}$$

By suitably selecting the transconductance factor ratio, $k_{n,E}/k_{n,D}$, the TC of the reference voltage can be minimized.

From (5), we can also evaluate the reference current:

$$I_{REF} = k_{n,E}(V_{REF} - V_{TH,E})^2 \approx k_{n,E}\left(\frac{-V_{TH,D} - V_{TH,E}}{1 + \sqrt{\frac{k_{n,E}}{k_{n,D}}}}\right)^2 \tag{6}$$

The main drawbacks of this solution are listed below. V_{REF} is dependent on V_{DD} because current I_{D1} of Q_{D1} in saturation linearly depends on V_{DS} through the Early effect, and V_{DS} is in turn equal to $V_{DD} - V_{REF}$. Though the minimum number of transistors is used and no resistors are exploited, a large area occupation is still necessary because large channel lengths are required to reduce the current consumption and to improve line regulation. It should also be noted that current I_{REF} cannot be freely chosen, once the transconductance ratio is set for TC minimization.

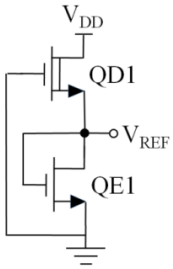

Figure 4. 2-T GaN voltage reference [31].

3. Proposed Voltage Reference Generator

The proposed solution aims at four main targets, namely low area and low current consumption independent from supply; robustness against process corners; and of course, a reasonably low temperature coefficient. These features must be obtained under an additional constraint derived from the adopted technology that is characterized by D-type transistors with very stable threshold voltage, $V_{TH,D}$, in which TC is about 250 μV/°C, much lower than the TC of $V_{TH,E}$ (that is 4.2 mV/°C). This technological behavior then makes approaches such as that in [30] almost useless because, using (3) or (4), the TC minimization of V_{REF} would require an extremely large and unpractical resistor ratio (as high as 17).

To achieve the aforementioned goals, the proposed voltage reference generator shares the best properties of previous topologies [30,31] but with a further reduction in current consumption by operating all the transistors in their subthreshold region. Furthermore, insensitivity to supply voltage variations and parameter spread is improved through suitable circuit solutions and design strategy.

3.1. Circuit Description

The schematic diagram of the proposed GaN voltage reference circuit is illustrated in Figure 5. As in [31], a single branch is exploited to halve current consumption with respect to the two-branch topologies and, as in [30], the reference current can be arbitrarily set by means of resistors.

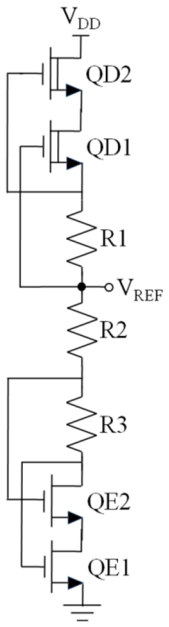

Figure 5. Proposed single-branch, double wide-swing-cascode, voltage reference.

The topology is made up of an upper-side section (Q_{D1}, Q_{D2}, and R_1) that generates the reference current and a lower side section (Q_{E1}, Q_{E2}, R_2, and R_3) which acts as an active load.

From inspection of the reference current generator formed by the wide-swing structure Q_{D1}-Q_{D2} and current-limiting resistor R_1, current I_{REF} (flowing from V_{DD} to ground) is equal to $V_{SG,D1}/R_1$. Unlike in (2), $V_{SG,D1}$ cannot be approximated by $-V_{TH,D}$ because the transistors will be all operated in subthreshold. Therefore, previous analyses such as those carried out in [30] and [31] cannot be adapted to this case and new design equations must be developed, as described in Section 3.2.

It is seen that the additional cascode device Q_{D2} in the current generator does not vary the value of I_{REF}, but it allows for decreasing the second-order dependence of I_{REF} (and hence of V_{REF}) on the supply voltage. Indeed, Q_{D2} shields the drain-source voltage of Q_{D1} from V_{DD} variations by setting $V_{DS,D1}$ constant and equal to $V_{SG,D2}$, hence independent of V_{DD}.

Hence, assuming that Q_{D1} and Q_{D2} have the same aspect ratio and the same drain current, we have that

$$-V_{GS,D1} = -V_{GS,D2} = V_{DS,D1} \tag{7}$$

As a drawback, the minimum supply voltage is slightly increased by $V_{DS,D1}$.

The reference current is then injected into the low-impedance load made up of transistors Q_{E1}–Q_{E2} and resistors R_2-R_3, which act similarly to the previous circuit of Figure 3.

It should be noted that the function of cascode transistor Q_{E2} is to make $V_{DS,E1}$ independent of the threshold voltage variations caused by the large process spreads. Indeed, a simple evaluation shows that

$$V_{DS,E1} = V_{GS,E1} - V_{GS,E2} + R_3 I_{REF}, \tag{8}$$

indicating that a global variation affecting both thresholds of Q_{E1} and Q_{E2} does not vary $V_{DS,E1}$. On the contrary, $V_{DS,E2}$ depends on $V_{GS,E2}$

$$V_{DS,E2} = V_{GS,E2} - V_{DS,E1}. \tag{9}$$

3.2. Analysis and Design Strategy

The analysis of the proposed topology begins by evaluating the reference current. Equation (2) is rearranged here as in (10) to take into account that Q_{D1} operates in the subthreshold. In particular, ΔV_{SUB} is the amount of subthreshold voltage:

$$I_{REF} = \frac{V_{SG,D1}}{R_1} \approx -\frac{V_{TH,D} + \Delta V_{SUB}}{R_1}. \tag{10}$$

Assuming as a design specification I_{REF} = 2.5 µA, using minimum size depletion transistors, and considering that in the adopted technology $V_{TH,D} = -691$ mV, by setting $\Delta V_{SUB} = -150$ mV, we have from (10) that the required value of R_1 is about 340 kΩ.

Once I_{REF} is set, assuming that $V_{GS,E1}$ and $V_{GS,E2}$ are almost equal, we can set $V_{DS,E1}$ from (7) through R_3. For $V_{DS,E1}$ around 300 mV, R_3 = 300 mV/2.5 µA = 120 kΩ is required.

Let us now consider the lower part of the circuit. The reference voltage is expressed by

$$V_{REF} \approx V_{GS,E1} + (R_2 + R_3) I_{REF}. \tag{11}$$

As stated before, the very small *TC* of $V_{TH,D}$ is reflected into I_{REF} that is almost constant with temperature. The last term of (11) is hence roughly constant with *T*, and consequently, the *TC* of V_{REF} is dominated by the *TC* of $V_{GS,E1}$. Note that following an approach such as that in (3) or (4) would lead to an impractically large R_2+R_3 value that is 17 times R_1, i.e., around 5.8 MΩ. We instead utilize (11) to compensate for the variations in V_{REF} due to process corners. Specifically, SS, or slow-slow models, are characterized by the highest threshold magnitudes for both E- and D-type transistors, and FF, or fast-fast models, are characterized by the lowest threshold magnitudes. The large thresholds spread of the adopted technology is summarized in Table 1, which shows 42% and 28% variations in $V_{TH,E}$ and $V_{TH,D}$, respectively, at room temperature. Considering the SS corner and (10) and (11), it is seen that $V_{TH,E}$ ($V_{TH,D}$) tends to increase (decrease) V_{REF}. The FF corner works in the opposite manner. As a result, there is an optimal value of R_2+R_3 that minimizes the effect of the process spread at a specified temperature. By considering SS and TT corners and taking the absolute value of the threshold differences, from (10) and (11), we have

$$R_2 + R_3 \approx \frac{\Delta V_{TH,E}}{|\Delta V_{TH,D}|} R_1, \tag{12}$$

which gives R_2 + R_3 around 555 kΩ and, consequently, R_2 = 435 kΩ since R_3 is already known.

Table 1. Threshold spread in SS and FF corners (room temperature).

Thresholds	Typ	SS	FF
$V_{TH,E}$ (V)	1.62	2.28	0.918
$V_{TH,D}$ (V)	−0.691	−0.287	−1.10

Consider now the enhancement devices. The following simplified equation holds for the drain current of the generic transistor Q_E operating in the subthreshold.

$$I_{REF} \approx I_{0,E} e^{\frac{V_{GS,E}-V_{TH,E}+\eta_E V_{DS,E}}{n_E V_T}} \left(1 - e^{-\frac{V_{DS,E1}}{V_T}}\right), \tag{13}$$

where V_T is the thermal voltage, n_E is the subthreshold slope coefficient, η_E is the drain induced barrier lowering (DIBL) coefficient, and $I_{0,E}$ is proportional to (W/L) and V_T^2. We neglected body effect for simplicity. In the following, $V_{DS} >> V_T$ is always met, and therefore, the factor in round brackets in (13) can be also neglected. Evaluating $V_{GS,E1}$ from (13) yields

$$V_{GS,E1} \approx V_{TH0,E} + n_E V_T \ln \frac{I_{REF}}{I_{0,E1}} - \eta_E V_{DS,E1}. \tag{14}$$

A similar equation holds also for $V_{GS,E2}$. Now, substituting (8) in (14) and expressing $V_{GS,E1} - V_{GS,E2}$ as $\ln[(W/L)_{E2}/(W/L)_{E1}]$, we have

$$V_{GS,E1} \approx V_{TH0,E} + n_E V_T \ln \frac{I_{REF}}{I_{0,E1}} - \eta_E n_E V_T \ln \frac{(W/L)_{E2}}{(W/L)_{E1}} - \eta_E R_3 I_{REF}. \tag{15}$$

Equation (15) shows that the temperature coefficient can be minimized through a suitable selection of the ratio $(W/L)_{E2}/(W/L)_{E1}$ that is found through computer simulation, as the temperature coefficient of $V_{GS,E1}$ cannot be easily evaluated analytically.

4. Validation Results

The proposed solution in Figure 5 was simulated using Spectre and the design kit of a commercial GaN smart power technology supplied by TSMC with L_{min} equal to 1 µm and 0.55 µm for enhancement and depletion transistors, respectively. The transistor thresholds have been already given in Table 1. The aspect ratio and multiplicity of the transistors together with the resistor dimensions and their nominal values are summarized in Table 2.

Table 2. Transistor dimensions and resistor values of the proposed voltage reference circuit.

Device	W (µm)	L (µm)	Multiplicity	Value
Q_{D1}–Q_{D2}	5	0.5	1	
Q_{E1}	250	1	8	
Q_{E2}	200	1	3	
R_1	2	1000	1	320.22 kΩ
R_2	2	1400	1	448.42 kΩ
R_3	2	400	1	128.20 kΩ

Note that resistor values are those obtained in the previous section with only marginal fine-tuning optimizations, while optimal $(W/L)_{E2}/(W/L)_{E1}$ was found to be 3/10 through computer simulations.

Figure 6 shows the reference voltage versus supply voltage at room temperature and when using typical model parameters for both enhanced and depletion devices (TT case). An average reference voltage approximately equal to 2.685 V is found starting from the minimum supply of 3.9 V. Below 3.9 V, the circuit does not work properly because the reference voltage is not kept constant. From the inset in Figure 6, we compute the line regulation that is found to be $\Delta V_{REF}/\Delta V_{DD}$ = (2.706 − 2.685)/(24 − 3.9) = 1.05 mV/V, or equivalently, 0.105%V.

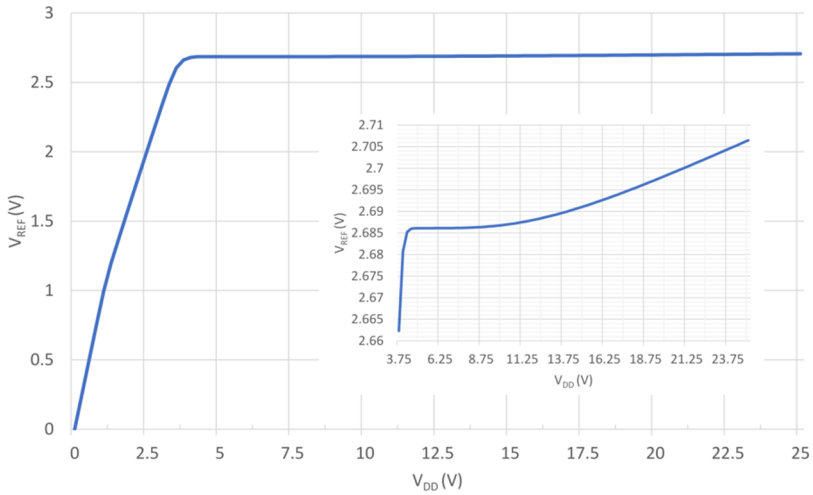

Figure 6. Reference voltage versus supply voltage (TT corner, room temperature).

Current I_{REF} versus supply voltage is shown in Figure 7, under the same room temperature and typical process conditions. I_{REF} is roughly equal to 2.7 µA for V_{DD} greater than 3.9 V. A current consumption independent of supply voltage is achieved.

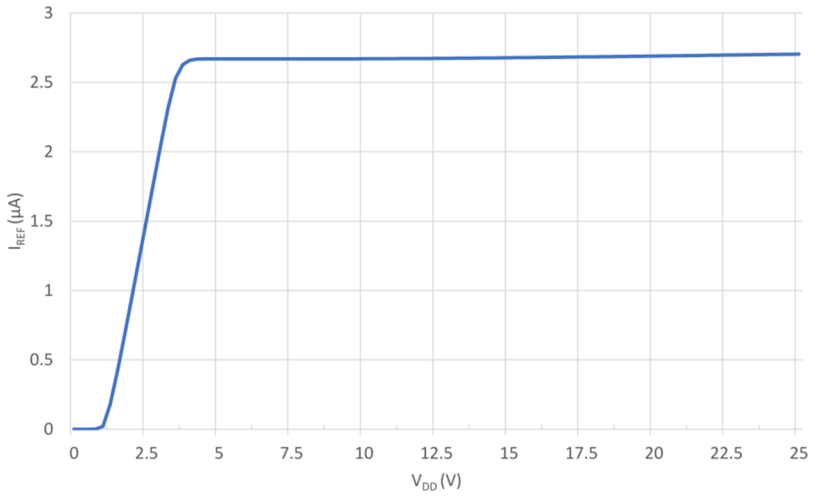

Figure 7. Reference current versus supply voltage (TT corner, room temperature).

Knowing the resistor values and from the values of V_{REF} and I_{REF}, we can infer from (10) that the value of $V_{GS,E1}$ is 1.14 V, confirming the subthreshold operation.

As already stated, GaN IC technologies suffer from large process spreads. It is therefore essential to simulate the effects of process variations together with temperature. Figure 8 illustrates the corner analysis (SS, TT, and FF cases) of the reference voltage versus temperature (from −40 °C to 190 °C) under the two extreme supply voltages: 3.9 V and 24 V. A sharp decrease in V_{REF} is found for temperatures below 23 °C and is due to the fitting point of the device models at ambient temperature. Nevertheless, the reference voltage ranges from 2.47 V to 2.71 V, with less than ±4.5% variability in the whole temperature range and within the 3.9–24 V supply. The robustness of the solution and the viability of the design approach is hence confirmed to counteract process, temperature, and supply variations. Considering the worst-case curve (SS at 3.9 V), the *TC* is evaluated to be around 200 ppm/°C.

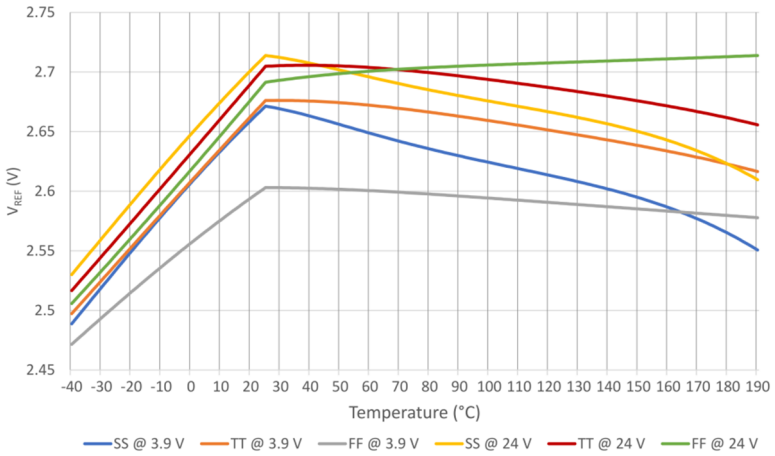

Figure 8. Corner analysis of reference voltage in the temperature range from −40 °C to 190 °C for two supply values (3.9 V and 24 V).

It was also confirmed (not shown) that the maximum current consumption is as low as 5 µA, under corner FF.

Figure 9 shows the magnitude of the power supply rejection, or *PSR*, of the voltage reference, under different corners and temperatures. DC supply voltage is set to 24 V. It is seen that the worst case is given by the SS corner at low temperature, while the best case is given by FF corner at high temperature. *PSR* is better than −45 dB in the 10 MHz frequency range, indicating that a disturbance in the supply is attenuated by more than 170 times.

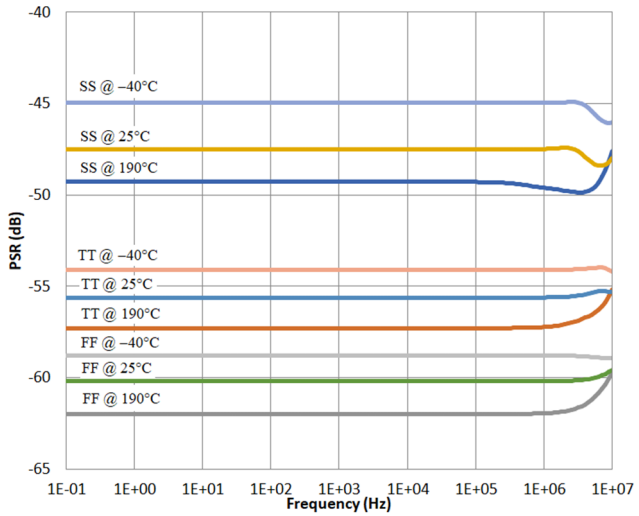

Figure 9. Corner analysis of power supply rejection, or *PSR*, at three temperatures and maximum supply of 24 V.

Figure 10 depicts the layout of the proposed voltage reference generator. Occupied area is 176.6 µm × 261.8 µm.

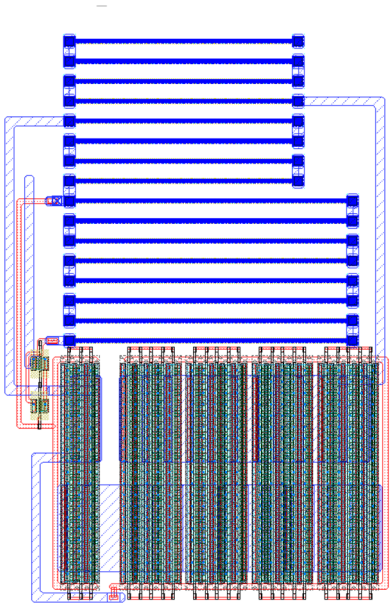

Figure 10. Layout of the voltage reference generator (width is 176.6 µm, and length is 261.8 µm).

Table 3 summarizes the main performance of the proposed voltage reference together with a comparison to the previously published solutions. Another reference, [21], that was not discussed before as it is not suitable for automotive applications, is added here for the sake of completeness. It is seen that the proposed solution, together with [30] and [31], are the only solutions able to work under a 24 V supply. However, the typical current consumption of the proposed solution is the lowest, even considering the worst-case scenario (5 µA). Limited area occupation is also a key feature of the proposed solution, and line sensitivity is also good in comparison to the state of the art. The *TC* achieved is similar to the values reported by the other untrimmed solutions.

Table 3. Performance comparison of GaN voltage references.

Ref. Year	This Work * 2022	[21] 2022	[31] 2022	[30] 2020	[29] 2010
Supply (V)	3.9~24	4~16	4.8~50	3.9~24	−4.3~−10
V_{REF} (V)	2.7	2.3	2.53	3.19	−2.1
Tot. current (µA)	2.7 (5, worst case)	43	60	6.2	800
Line Regul. (%V)	0.105	NA	0.063	0.32	N/A
PSR @100Hz (dB)	−45 (worst case)	NA	−42.8	−45	−35
Temp. Range (°C)	−40~190	25~550	−25~250	−50~200	25~250
TC (ppm/°C)	200 $^{+}$ (worst case)	242 $^{+}$	26.2	23.6	238 $^{+}$
Area (mm^2)	0.05	0.03	0.104	0.52 (0.31 w/o PADs)	0.164

* Simulations; $^{+}$ Untrimmed.

5. Conclusions

The aim of this paper was to present a novel topology for a reference voltage generator amenable for GaN IC processes, together with its optimal design methodology. The solution is made up of a single branch that allows for setting the standby reference current in the microampere range through practical resistor values. The solution is also designed to operate in a wide supply voltage range, from around 4 V to 24 V, in order to meet the requirements of consumer and automotive applications.

In addition, the circuit allowed for low area occupation (0.05 mm^2) and low current consumption (2.7 µA). Both features are becoming more and more important targets also in the automotive sector to save space inside the vehicle and to preserve the battery autonomy.

A unique characteristic of the solution related to the low current consumption was the operation of the transistors in the subthreshold regime. For this purpose, a straightforward, accurate design strategy was also developed. Indeed, after describing the topology, equations based on a subthreshold operation were formulated and component values

were derived from these equations. Taking these results as the initial point, fine-tuning dimensioning was performed through computer simulations.

Unlike prior art, the proposed solution was also targeted at counteracting the large parameter spreads of commercial GaN IC technologies. Indeed, it provided an average reference voltage of around 2.685 V at room temperature with ±120 mV variation (<±4.5%), against a ±42% and 28% variability of the threshold voltages of enhancement and depletion devices, respectively.

The temperature coefficient of the reference voltage achieved is around 200 ppm/°C and is similar to the values reported by the other untrimmed GaN solutions.

Presently, the circuit does not cope with SF and FS corners; in this case, external trimming is mandatory. To avoid trimming, future research will focus on threshold voltage on-chip sensing and on the definition of calibration strategies to inherently reduce the temperature coefficient. Work is also ongoing to improve current drive capabilities by designing a low-dropout regulator in the same IC GaN technology. To this purpose, an operational transconductance amplifier has already been presented in [32].

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