Design of Three-Stage OTA Based on Settling-Time Requirements Including Large and Small Signal Behavior

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***Abstract*— In this paper we are going to analyze the settling-time in single-, two- and three-stage amplifiers with the intent of deriving approximate but useful design equations that include the effects of the zeros and of the slew-rate limitations. The analysis is mainly devoted to the definition of an approach for the design of three-stage CMOS operational transconductance amplifiers from settling-time specifications. A design example is carried out to validate the proposed approach.**

***Index Terms*— Settling-time, operational transconductance amplifiers, multi-stage amplifiers, feedback amplifiers, CMOS, low-voltage.**

I. Introduction

OPERATIONAL transconductance amplifiers (OTAs) are the main building blocks in many analog and mixed-signal electronic circuits. Across the last decades, the design of OTAs has evolved with the fabrication process of integrated circuits (ICs) since it had to follow the technology scaling mainly imposed by the digital trend predicted by the Moore's law. As a consequence, the lowering of the supply voltage ($V_{DD} < 1\,V$) and the reduction of the transistor intrinsic gain ($g_m r_d \sim 10$) made the realization of cascoded structures unfeasible and pushed the interest of the research towards the design of multistage amplifiers [1]–[8]. In this scenario, the main performance metric used to evaluate (and compare) the 'speed' of OTAs remained the gain-bandwidth product (GBW).

In the last fifteen years, the design of low-voltage and multi-stage CMOS OTAs from settling-time specifications has raised the attention of the scientific community because of the growing demand for high-performance discrete-time circuits (i.e., advanced switched-capacitor circuits or data converters) and for circuits that require fast reactions to step inputs (i.e., voltage regulators) [9]–[18]. Despite the significant number of proposed design procedures, many of them do not provide simple relationships between the amplifier parameters and the settling-time, which cut their utility in a real design. Further, most of them assume that the amplifier behaves in a linear fashion and do not analyze the large-signal effects caused by slew-rate (SR) limitations which can severely affect the time response.

In the past, the SR was analyzed in monolithic operational amplifiers since the '70s [19], [20]. In [21], [22] the authors analyze in great detail the SR of a two-pole amplifier. However, the analysis does not include zeros or higher order amplifiers and manipulating the final results to obtain a design equation is not so straightforward. In [23], [24] the authors introduce some improved slew rate models which are not exploited to predict the settling-time. In [25], [26] the authors propose very accurate models for the settling-time but they are limited to particular topologies.

In recent years an efficient technique for the analysis and the design of the settling-time in amplifiers was developed by the authors. In particular, the approach allows to design and optimize the amplifier in the time domain [27], [28]. However, the methodology previously presented does not allow to include the SR effect, since it is focused only on the small signal settling-time. In this paper, we extend the previous methodology to model and evaluate the whole settling-time taking into account the SR effect, also. In particular, we are going to analyze the settling-time in single-, two- and three-stage amplifiers with the intent of deriving approximate but useful design equations that include the effects of the zeros and of the SR limitations.

In the discussion we shall focus our analysis to those amplifiers in which the slew-rate limitation resides in the first stage and is associated with the capacitor responsible for the dominant pole.[1] This class of amplifiers includes many topologies based on Miller or reversed-Miller compensations. The analysis also concentrates on those amplifiers where the zeros of the transfer function are placed above the GBW. This is a minor limitation since, as shown in sections III-B and IV-B, one or more zeros placed below the GBW slow down the transient response and, if not used to cancel one or more corresponding poles, lead to bad designs. In addition, the compensation cases that rely on the cancellation of a pole using a low-frequency zero, such as those in [29]–[38], can

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[1] If the slew-rate limitation does not reside in the first stage, as shown in section III-D, the circuit can experience a positive feedback connection during its slewing period, thus revealing large overshoots and loosing settling-time performance [24]. In a well-designed amplifier, this situation must be avoided and is not included in our analysis.

be managed as detailed in [39] where an extensive model of the pole-zero compensation and some useful design criteria are provided in terms of transient response.

The paper is structured as follows. In section II we analyze in detail the step response in single-pole amplifiers with slew-rate limitations. In sections III and IV the analysis is extended to the two- and three-pole amplifiers. In section V we propose our design procedure and in section VI we design a three-stage CMOS OTA to validate the proposed approach.

II. The Step Response in Single-Pole Amplifiers

A. Small-Signal Analysis

The generic loop gain of a single pole amplifier is

$$T(s) = \beta a(s) = \frac{\beta a_0}{1 + \frac{s}{\omega_d}} \tag{1}$$

where $a(s)$ is the open-loop transfer function, β is the loop feedback factor, a_0 is the open-loop dc gain and ω_d is the frequency of the pole. As long as $\beta a_0 \gg 1$, the frequencies of interest reside for $\omega \gg \omega_d$ and we can always simplify this single-pole transfer function into

$$T(s) = \frac{1}{s/\text{GBW}} \tag{2}$$

where $\text{GBW} = \beta a_0 \times \omega_d$ defines the gain-bandwidth product of the amplifier.

As known, if we close the amplifier (2) in feedback, we obtain the closed-loop transfer function

$$A(s) = A_0 \frac{T(s)}{1 + T(s)} = \frac{A_0}{1 + \frac{s}{\text{GBW}}} \tag{3}$$

where $A_0 = 1/\beta$ is the closed-loop dc gain[2] and the GBW becomes the pole of the closed-loop amplifier.

A convenient way to analyze the amplifier's time response is to use a dimensionless transfer function normalized to the GBW. Hence, defining $\bar{s} = s/\text{GBW}$ as the dimensionless frequency and $\bar{t} = \text{GBW} \cdot t$ as the corresponding dimensionless time, the closed-loop transfer function becomes

$$A(\bar{s}) = \frac{A_0}{1 + \bar{s}} \tag{4}$$

If $y(\bar{t})$ is the output response to a step input, the dimensionless settling-time within a certain percentage error, ϵ, is defined as

$$\bar{t}_s = \min \left\{ \bar{t}^\star : \left| \frac{y(\infty) - y(\bar{t})}{y(\infty)} \right| \leq \epsilon \ \forall \, \bar{t} \geq \bar{t}^\star \right\} \tag{5}$$

and the resulting dimensionless settling-time for the single-pole amplifier is

$$\bar{t}_{s(\text{sp})} = |\ln \epsilon| \tag{6}$$

Clearly, dividing $\bar{t}_{s(\text{sp})}$ by the GBW, returns the dimensional settling-time (expressed in seconds) for the single-pole amplifier, that is

$$t_{s(\text{sp})} = \frac{|\ln \epsilon|}{\text{GBW}} \tag{7}$$

[2]Actually A_0 can differ from $1/\beta$ since it depends on the terminal where the input signal is applied.

A useful parameter that we shall use extensively in the following is the *normalized settling-time* (NST), defined as the settling-time of the amplifier under test, t_s, normalized to the settling-time of a linear single-pole amplifier with the same GBW, that is

$$\text{NST} = \frac{t_s}{t_{s(\text{sp})}} = \frac{\text{GBW}}{|\ln \epsilon|} t_s \tag{8}$$

The normalized settling-time can be evaluated also noting that $\bar{t}_s = \text{GBW} \cdot t_s$ represents the dimensionless settling-time of the amplifier under test, and so

$$\text{NST} = \frac{\bar{t}_s}{\bar{t}_{s(\text{sp})}} = \frac{\bar{t}_s}{|\ln \epsilon|} \tag{9}$$

Obviously, when the amplifier under test is the single-pole amplifier in (1), the normalized settling-time, by definition, equals 1.

B. Large-Signal Analysis and Slew-Rate Modeling

The simple model derived so far assumes that the amplifier behaves in a linear fashion, however, especially for large input signals, slew-rate (SR) limitations can seriously affect the time response.

Current limitations in transconductors give rise to slew-rate, therefore a single-pole amplifier with this non-linearity can be represented by the block schematic in Fig. 1a, where $Q(s) = 1$. In the figure, the output current of the transconductor is set by

$$i_t(v_d) = \begin{cases} G_m v_d & \text{for } |v_d| \leq \dfrac{I_o}{G_m} \\ I_o \operatorname{sgn}(v_d) & \text{for } |v_d| > \dfrac{I_o}{G_m} \end{cases} \tag{10}$$

The output impedance of the first stage of the amplifier is also responsible for the dominant pole and is simplified with its reactive element as $Z_o = R_o/(1 + sC_oR_o) \approx 1/(sC_o)$. The gain-bandwidth product results $\text{GBW} = \beta G_m/C_o$. Capacitor C_o and the saturation current, I_o, set also the slew-rate as $\text{SR} = I_o/C_o$.

Normalizing the complex variable, s, to the gain-bandwidth product of the amplifier (i.e., $\bar{s} = s/\text{GBW}$), we can reduce the block schematic in Fig. 1a into the equivalent block schematic of Fig. 1b, where the parameter

$$\nu = \frac{I_o}{\beta G_m} = \frac{\text{SR}}{\text{GBW}} \tag{11}$$

is the *equivalent saturation limit* of the saturation block.

As demonstrated in the Appendix A, for a single-pole amplifier, the NST has the closed-form solution

$$\text{NST}_{\text{sp}} = \begin{cases} 1 & \text{for } \left| \dfrac{\Delta Y}{\nu} \right| < 1 \\ 1 + \dfrac{\frac{\Delta Y}{\nu} - \left(1 + \ln \frac{\Delta Y}{\nu}\right)}{|\ln \epsilon|} & \text{for } \left| \dfrac{\Delta Y}{\nu} \right| \geq 1 \end{cases} \tag{12}$$

where ΔY is the output step. The plot of (12) is depicted in Fig. 2 versus the normalized output, $\Delta Y/\nu$, and for different values of the response accuracy level, ϵ.

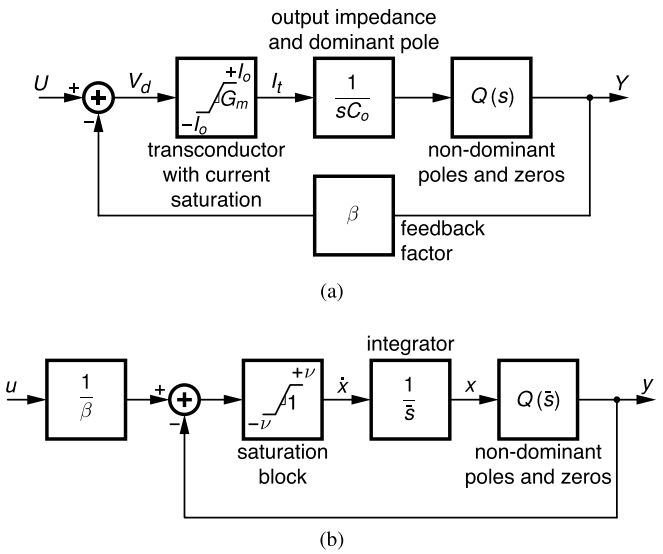

Fig. 1. Block schematic representation of a generic amplifier with a Slew-Rate modeling. a) Actual schematic. b) Equivalent version (lower-case variables represent time-domain signals with respect to the dimensionless time, $\bar{t} = \mathrm{GBW} \cdot t$).

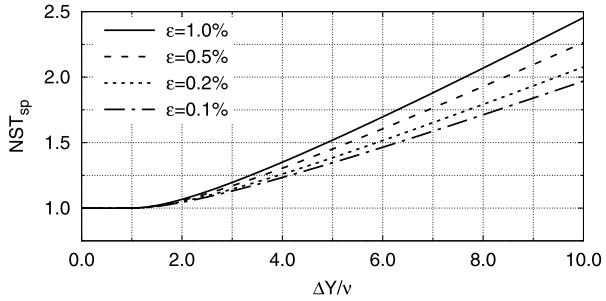

Fig. 2. Plot of the NST versus $\Delta Y/\nu$ for the single-pole amplifier.

III. The Step Response in Two-Pole Amplifiers

A. Small-Signal Analysis of a Pure Two-Pole Amplifier

A pure two-pole amplifier contains a dominant pole, a second high-frequency pole and no zeros. Using the approximation in (2) for modeling the high dc gain and the dominant pole, the loop gain is

$$T(s) = \frac{1}{\frac{s}{\mathrm{GBW}}(1 + a_1 s)} = \frac{1}{\frac{s}{\mathrm{GBW}}\left(1 + \frac{s}{\omega_s}\right)} \tag{13}$$

where $\omega_s = 1/a_1$ is the second (non-dominant) pole.

Closing the system (13) in a loop leads to the closed-loop transfer function

$$A(s) = \frac{A_0}{1 + \frac{s}{\mathrm{GBW}} + \frac{s^2}{\mathrm{GBW}\omega_s}} = \frac{A_0}{1 + \frac{s}{\mathrm{GBW}} + \frac{s^2}{\mathrm{GBW}^2 K}} \tag{14}$$

where $K = \omega_s/\mathrm{GBW}$ is the *separation factor*, that is, the ratio between the second pole and the gain-bandwidth product of the amplifier. The separation factor was established in [40] and, in a stable feedback amplifier, it is related to the phase margin through the relationship $K \approx \tan(\mathrm{PM})$. Hence it is responsible for the amplifier stability and for its transient response [41]–[43].

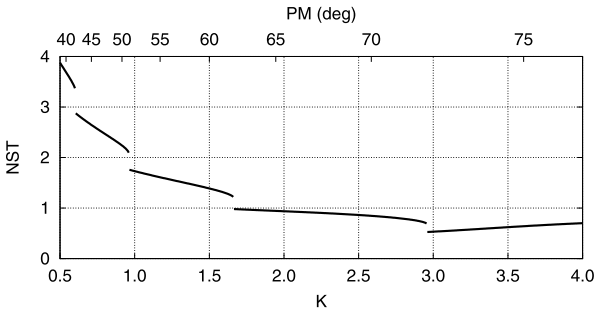

Fig. 3. Plot of the normalized settling-time, NST, versus the separation factor, K, for the pure two-pole amplifier. The response accuracy level is $\epsilon = 0.5\%$. The PM is also shown.

TABLE I
Minimum NST and Corresponding K for Different Accuracy Levels

	$\epsilon = 1.0\%$	$\epsilon = 0.5\%$	$\epsilon = 0.2\%$	$\epsilon = 0.1\%$
$\mathrm{NST}_{\min}$	0.55	0.53	0.51	0.50
K	2.73	2.96	3.19	3.32

To understand how the separation factor affects the response to a step input, we used MATLAB to compute the NST defined in (8). To do so, first we normalize (14) with respect to GBW (i.e., $\bar{s} = s/\mathrm{GBW}$), thus leading to

$$A(\bar{s}) = \frac{A_0}{1 + \bar{s} + \frac{\bar{s}^2}{K}} \tag{15}$$

Second, we numerically evaluate the corresponding time response to a unity-step input, $y(\bar{t})$, and find the dimensionless settling-time as in (5). Finally, we evaluate the NST from (9).

The plot of the NST versus the separation factor, K, is reported in Fig. 3 for the accuracy level of $\epsilon = 0.5\,\%$. As explained in the Appendix B, this plot is a discontinuous function and, as long as the amplifier operates in the linear region, it is independent of the signal amplitude. Different plots but with similar behaviors are observed for different accuracy levels. The plot shows how the separation factor affects the settling-time of the amplifier. A small separation factor ($K < 1$) can lead to a prohibitively large settling-time. Conversely, a higher separation factor, can lead to a fast amplifier [18], [28]. However, in this latter case, for the same GBW and load capacitor, the increased speed is paid in terms of power consumption.

Tab. I reports the minimum NST and the corresponding value of separation factor, K, for different accuracy levels under the assumption that the amplifier operates in the linear region. It is worth noting that these minimum values are placed in points of discontinuities for which any small deviation (due to approximate modeling, process tolerances, etc.) will move the NST away from these ideal points. For this reason, as better discussed in [28], the minimum NST in Tab. I is realistically unreachable while the specification NST $\lesssim 1$ becomes a reasonable target for almost any practical design.

As a final key point, if the closed-loop transfer function is available in the form

$$A(s) = \frac{A_0}{1 + \alpha_1 s + \alpha_2 s^2} \tag{16}$$

a comparison with (14) allows us to evaluate the open-loop parameters from

$$\text{GBW} = \frac{1}{\alpha_1} \tag{17a}$$

$$K = \frac{\alpha_1^2}{\alpha_2} \tag{17b}$$

B. Small-Signal Analysis of a Generic Two-Pole Amplifier

The generic two-pole amplifier includes a zero in the loop gain, so that

$$T(s) = \frac{1 + b_1 s}{\frac{s}{\text{GBW}}(1 + a_1 s)} = \frac{1 + \frac{s}{\omega_z}}{\frac{s}{\text{GBW}}\left(1 + \frac{s}{\omega_s}\right)} \tag{18}$$

where $\omega_z = 1/b_1$. The corresponding closed-loop transfer function takes the form

$$A(s) = A_0 \frac{1 + b_1 s}{1 + \alpha_1 s + \alpha_2 s^2} \tag{19}$$

where

$$\alpha_1 = \frac{1}{\text{GBW}} + b_1 \tag{20a}$$

$$\alpha_2 = \frac{a_1}{\text{GBW}} \tag{20b}$$

As long as the GBW remains below the zero of the transfer function (i.e., $|b_1| < 1/\text{GBW}$), under the assumption that the time response of the closed-loop amplifier is mainly determined by the denominator of $A(s)$, we can define an equivalent or *global separation factor* for the generic two-pole amplifier using the coefficients of its closed-loop gain, as we did in (17b), so that

$$\hat{K} = \frac{\alpha_1^2}{\alpha_2} = \frac{(1 + b_1 \text{GBW})^2}{a_1 \text{GBW}} \tag{21}$$

This ensures that the generic two-pole amplifier has almost the same NST of the pure two-pole one.

Therefore we can satisfy the NST specification of the generic two-pole amplifier by applying to $\hat{K}$ the same value that we would choose for the pure two-pole amplifier. In particular, minimizing the NST in a generic two-pole amplifier means setting $\hat{K} = K$ using the numerical values in Tab. I.

The case with the zero placed below the GBW is not considered in the paper since this situation represents a bad example of design and must be avoided. In this case, the time response is slowed down by the factor $(1 + b_1 \text{GBW})$ that heavily affects the main time constant of the amplifier. Occasionally, a zero can be intentionally placed below the GBW for compensating a low-frequency pole as, for example, in [44]. This case is not covered here as it was exhaustively discussed in [39] where the pole-zero compensation is examined in terms of time response.

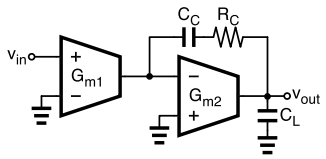

Fig. 4. Block schematic of a two-stage amplifier. The compensation is performed through a Miller network composed by the series of C_C and R_C.

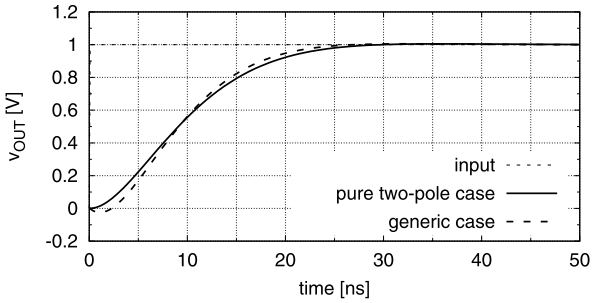

Fig. 5. Time response to a step input for two different design cases. Maintaining the same GBW and the same global separation factor, the two responses are equivalent.

C. The Design Using the Global Separation Factor

To prove the validity of our assumption, we simulated the ideal two-stage amplifier in Fig. 4 for two different compensation cases: the *pure two-pole case* and the *generic case*. The two cases are compared through the 0.5-% settling-time.

In both the designs we maintained $G_{\text{m1}} = 100\,\mu\text{A/V}$, $C_\text{C} = 1\,\text{pF}$ and $C_\text{L} = 2\,\text{pF}$, so that the GBW is kept constant, also. In the pure two-pole case, we set $K = 2.96$, $G_{\text{m2}} = K G_{\text{m1}}(C_\text{L}/C_\text{C}) = 592\,\mu\text{A/V}$ and $R_\text{C} = 1/G_{\text{m2}} = 1.69\,\text{k}\Omega$, so to remove the right-half plane zero and obtain a pure two-pole amplifier. In the generic case, we imposed the global separation factor to $\hat{K} = 2.96$ but we set to zero the value of R_C, so that $b_1 = -C_\text{C}/G_{\text{m2}}$. From (21) we got $G_{\text{m2}} = 781\,\mu\text{A/V}$.

In both cases the simulated GBW is 100 Mrad/s (about 15.5 MHz). In the pure two-pole case, with a phase margin of 72.2°, the simulated settling-time is 28.0 ns (NST = 0.53). In the generic case, the phase margin reduces by 3.4° and the settling-time becomes 25.5 ns (NST = 0.48). The plot of the output response for the two cases is shown in Fig. 5 where a good matching between the two curves is apparent.[3]

D. Large-Signal Analysis and Slew-Rate Modeling

The slew-rate analysis of two-pole amplifiers is carried out for those amplifiers where the slew-rate limitation resides in the first stage and is associated with the capacitor responsible for the dominant pole. If this is not the case, the circuit can experience a positive feedback connection during its slewing

[3] Although the generic case would lead to a slightly superior performance in terms of settling-time, this design is more power consuming since, for the same capacitive load and GBW, it requires a higher G_{m2}. As a consequence, this strategy has no practical application in the Miller compensation of two-pole amplifiers and was just presented to prove the assumption that two amplifiers with the same global separation factor have similar NST.

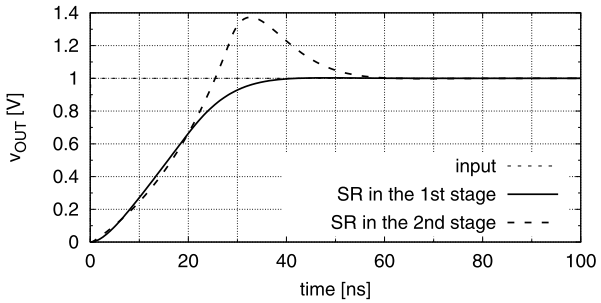

Fig. 6. Transient response of a two-stage amplifier with SR limitations. In the solid-line case the maximum current of the first stage is limited to 40 μA. In the dashed-line case the maximum current of the second stage is limited to 140 μA. Other small-signal parameters are the same of the first circuit designed in section III-C and plotted in Fig. 5.

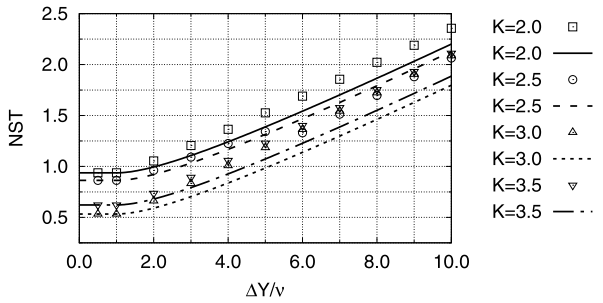

Fig. 7. Plot of the NST versus $\Delta Y/\nu$ for the pure two-pole amplifier. The accuracy level is $\epsilon = 0.5\%$. Points represent simulations of the amplifier in Fig. 1b with $Q(\bar{s}) = 1/(1+\bar{s}/K)$. Lines plot the NST forecasted by (23). The plot shows simulations for different values of the separation factor, K. Including also the simulations for $K = 1.0$, $K = 1.5$ and $K = 4.0$, the maximum error is maintained below 23%.

period, thus revealing large overshoots and loosing speed performance [24].

This is what happens, for example, in two-stage Miller-compensated amplifiers such as that in Fig. 4. Specifically, connecting the circuit in unity-gain configuration and assuming that the SR limitation is in the second stage, when a large input step is applied, the second transconductor provides a current independent of the voltage at its input node. This means that the second stage is no more controlled by the loop and that the output of the first stage is directly connected to the overall output, v_{out}, through the path provided by the compensation network, C_C–R_C. It is apparent that, as long as the second stage operates in slew-rate condition, the overall feedback of the network remains positive. The consequence is clearly reported in Fig. 6 where the case with slew-rate limitation in the first stage is compared to the case with slew-rate limitation in the second stage. As depicted in the figure, even if the circuit is perfectly compensated from a small-signal point of view, a large overshoot arise if the SR limitation does not reside in the first stage.

To ensure that the slew-rate of the first stage is the limiting factor, the designer can adopt slew-rate enhancers [45]–[48] or class-ab topologies [27], [49], [50] to overcome the current limitation of the subsequent stage.

As far as the slew-rate modeling is concerned let us focus our attention to relationship (12) which was derived for the single-pole case. It says that, with respect to the situation without SR limitations, the small-signal NST increases by

$$\Delta\text{NST} = \frac{\frac{\Delta Y}{\nu} - \left(1 + \ln\frac{\Delta Y}{\nu}\right)}{|\ln\epsilon|} \tag{22}$$

This statement can be supposed as true for the two-pole case, too. Therefore, we assume that, if SR limitations occur, the small-signal normalized settling-time, NST_0, increases by (22) also in the case of two-pole amplifiers. In other words, for two-pole amplifiers, we assume that

$$\text{NST} = \begin{cases} \text{NST}_0 & \text{for } \left|\dfrac{\Delta Y}{\nu}\right| < 1 \\ \text{NST}_0 + \dfrac{\frac{\Delta Y}{\nu} - \left(1 + \ln\frac{\Delta Y}{\nu}\right)}{|\ln\epsilon|} & \text{for } \left|\dfrac{\Delta Y}{\nu}\right| \geq 1 \end{cases} \tag{23}$$

We checked the validity of our assumption through the simulation of an ideal case. In Fig. 7 we plotted the NST obtained from the direct simulation of a two-pole amplifier realized with the schematic in Fig. 1b where $\nu = 0.1$ V and

$$Q(\bar{s}) = \frac{1}{1 + \frac{\bar{s}}{K}} \tag{24}$$

The figure reports the simulation points of the NST versus the normalized output step, $\Delta Y/\nu$. In the same plot, lines report the values predicted using (23). The separation factor was varied from $K = 1.0$ to $K = 4.0$ with a 0.5-step but only the most commonly used interval ($K \in [2.0, 3.5]$) was reported in the figure. For this interval of values of K, the maximum error between the points and the values predicted by (23) maintains below 17%. If we include also the cases not reported in the figure (i.e., $K = 1.0$, $K = 1.5$ and $K = 4.0$), the maximum percentage error is 23%.

IV. The Step Response in Three-Pole Amplifiers

A. Small-Signal Analysis of a Pure Three-Pole Amplifier

A pure three-pole amplifier does not contain zeros and, as we did for the pure two-pole case, is modeled by

$$T(s) = \frac{1}{\frac{s}{\text{GBW}}\left(1 + a_1 s + a_2 s^2\right)} \tag{25}$$

where coefficients a_1 and a_2 account for the non-dominant poles (complex-conjugate, in many cases) and where, once again, we used the approximation in (2) for modeling the high dc gain and the dominant pole.

The amplifier in (25) can be represented as in Fig. 8a, where the non-dominant poles arise because of an inner loop or stage in a nested-loop structure [28]. This inner stage is characterized by its own internal gain-bandwidth product, GBW_i, and by its own second pole, ω_s, so that we can define an *internal separation factor*, $K_i = \omega_s/\text{GBW}_i$, which is responsible for the stability of the inner loop. Hence, describing the inner stage as in (14), we can express the non-dominant poles of the whole amplifier as a function of GBW_i and K_i, as in Fig. 8b.

If the inner stage is stable, we can assume that the bandwidth of the "non-dominant poles" block in Fig. 8b is mainly set by GBW_i which, in turn, becomes the equivalent second pole of the overall amplifier. This means that we can define

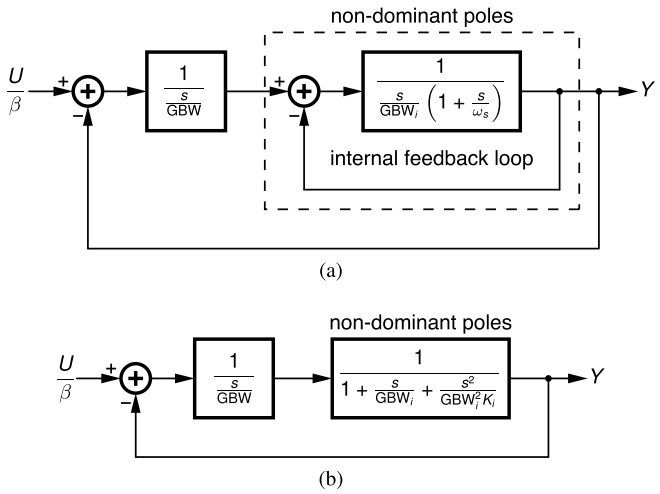

Fig. 8. Block schematic representation of a pure three-pole amplifier. a) The poles of the amplifier arise from two nested feedback loops. b) The non-dominant poles arise from the internal feedback loop.

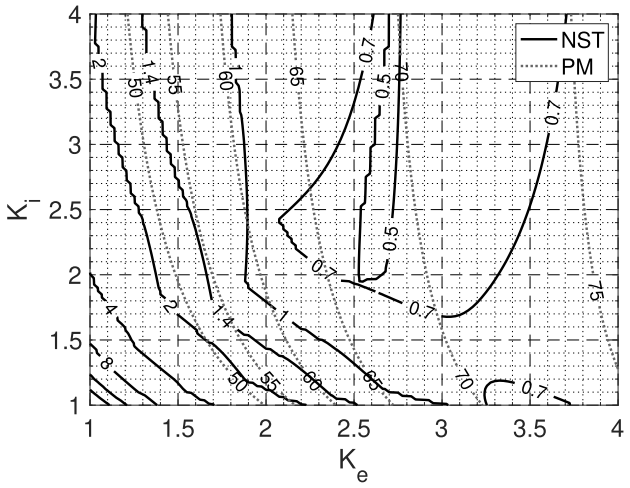

Fig. 9. Contour plot of the normalized settling-time, NST, for the pure three-pole amplifier. The response accuracy level is $\epsilon = 0.5\%$. The settling-time is normalized to that of a single-pole system having the same GBW. The PM is also plotted.

the *external separation factor*, $K_e = \mathrm{GBW}_i/\mathrm{GBW}$, which is responsible for the stability of the outer loop. When the loop gain is known in the form expressed by (25), we can evaluate

$$K_e = \frac{1}{a_1 \mathrm{GBW}} \tag{26a}$$

$$K_i = \frac{a_1^2}{a_2} \tag{26b}$$

so that

$$T(s) = \frac{1}{\frac{s}{\mathrm{GBW}}\left(1 + \frac{s}{K_e \mathrm{GBW}} + \frac{s^2}{K_e^2 K_i \mathrm{GBW}^2}\right)} \tag{27}$$

Closing the system (25) in feedback, the closed-loop transfer function takes the form

$$A(s) = \frac{A_0}{1 + \alpha_1 s + \alpha_2 s^2 + \alpha_3 s^3} \tag{28}$$

where

$$\alpha_1 = \frac{1}{\mathrm{GBW}} \tag{29a}$$

$$\alpha_2 = \frac{a_1}{\mathrm{GBW}} = \frac{1}{K_e\,\mathrm{GBW}^2} \tag{29b}$$

$$\alpha_3 = \frac{a_2}{\mathrm{GBW}} = \frac{1}{K_e^2 K_i\,\mathrm{GBW}^3} \tag{29c}$$

To evaluate the NST of the amplifier in (25), we normalize (28) by the GBW (i.e., $\bar{s} = s/\mathrm{GBW}$) and, by applying a step input, we use MATLAB to compute the settling-time, $\bar{t}_s$, for a given accuracy level, ϵ. Then, from (9), we obtain the NST as a function of the separation factors, K_e and K_i, for the accuracy level, ϵ.

Fig. 9 reports the contour plot of the NST as a function of the two separation factors and for the accuracy level of $\epsilon = 0.5\%$. This plot, carried out for the pure three-pole amplifier, is equivalent to the plot in Fig. 3, which was obtained for the two-pole case. It allows to determine the minimum normalized settling-time, $\mathrm{NST}_{\min}$, and the corresponding values of the separation factors, K_e and K_i. Also in this case, the NST is a discontinuous function and different contour plots, but with similar behaviors, are observed for different accuracy levels. Tab. II reports a summary of the results for different accuracy levels. As for the two-pole case, these minimum values are placed in points of discontinuities for which any small deviation (due to approximate modeling, process tolerances, etc.) would move the NST away from these ideal points. This makes the minimum NST in Tab. II realistically unreachable while the specification NST $\lesssim 1$ is still a reasonable target for almost any practical design. Fig. 9 shows that this target can be obtained from a wide area in the right side of the plot. However, in general, the higher are the separation factors (K_e or K_i) the higher results the power dissipation of the amplifier. As a rule-of-thumb, a good trade-off seems to be setting K_e and K_i 10–20% higher than the optimum value of Tab. II.

TABLE II
MINIMUM NST AND CORRESPONDING K_e AND K_i FOR DIFFERENT ACCURACY LEVELS

	$\epsilon = 1.0\%$	$\epsilon = 0.5\%$	$\epsilon = 0.2\%$	$\epsilon = 0.1\%$
$\mathrm{NST}_{\min}$	0.43	0.40	0.39	0.38
K_e	2.55	2.55	2.60	2.63
K_i	1.78	2.00	2.18	2.40

Finally, if the closed-loop transfer function is available in the form described by (28), we can evaluate the open-loop parameters from (29), that is

$$\mathrm{GBW} = \frac{1}{\alpha_1} \tag{30a}$$

$$K_e = \frac{\alpha_1^2}{\alpha_2} \tag{30b}$$

$$K_i = \frac{\alpha_2^2}{\alpha_1 \alpha_3} \tag{30c}$$

B. Small-Signal Analysis of a Generic Three-Pole Amplifier

The generic three-pole amplifier includes two zeros in the loop gain, so that

$$T(s) = \frac{1 + b_1 s + b_2 s^2}{\frac{s}{\mathrm{GBW}}\left(1 + a_1 s + a_2 s^2\right)} \tag{31}$$

The resulting closed-loop transfer function takes the form

$$A(s) = A_0 \frac{1 + b_1 s + b_2 s^2}{1 + \alpha_1 s + \alpha_2 s^2 + \alpha_3 s^3} \tag{32}$$

where

$$\alpha_1 = \frac{1}{\mathrm{GBW}} + b_1 \tag{33a}$$

$$\alpha_2 = \frac{a_1}{\mathrm{GBW}} + b_2 \tag{33b}$$

$$\alpha_3 = \frac{a_2}{\mathrm{GBW}} \tag{33c}$$

As long as the GBW remains below the zero of the transfer function (i.e., $|b_1| < 1/\mathrm{GBW}$), under the assumption that the time response of the closed-loop amplifier is mainly determined by the denominator of $A(s)$, we can define the equivalent or *global separation factors* for the generic three-pole amplifier using the coefficients of its closed-loop gain, as we did in (30), so that

$$\hat{K}_e = \frac{\alpha_1^2}{\alpha_2} = \frac{1}{a_1 \mathrm{GBW}} \frac{(1 + b_1 \mathrm{GBW})^2}{1 + \frac{b_2 \mathrm{GBW}}{a_1}} \tag{34a}$$

$$\hat{K}_i = \frac{\alpha_2^2}{\alpha_1 \alpha_3} = \frac{a_1^2}{a_2} \frac{\left(1 + \frac{b_2 \mathrm{GBW}}{a_1}\right)^2}{1 + b_1 \mathrm{GBW}} \tag{34b}$$

This ensures that the generic three-pole amplifier has almost the same NST of the pure three-pole one.

Therefore we can satisfy the NST specification of the generic three-pole amplifier by applying to $\hat{K}_e$ and $\hat{K}_i$ the same values that we would choose for the pure three-pole amplifier. In particular, minimizing the NST in a generic three-pole amplifier means setting $\hat{K}_e = K_e$ and $\hat{K}_i = K_i$ using the numerical values in Tab. II.

Like for the two-pole case, we do not consider the situation of zeros placed below the GBW since they heavily degrade the time response of the amplifier and lead to an unacceptable design that must be avoided. Furthermore, the case of zeros intentionally placed below the GBW for compensating low-frequency poles, as in [29]–[38], is discussed in [39] in terms of transient response.

C. The Design Using the Global Separation Factors

To prove the validity of our assumption, we simulated the step response of a pure three-pole amplifier with the generic amplifier in Fig. 10, compensated using the well-known Reversed Nested Miller Compensation (RNMC). The two responses are compared in terms of 0.5-% settling-time.

The pure-three pole amplifier was modeled and simulated through the transfer function in (28) for which we set a GBW of 100 Mrad/s (about 15.5 MHz), $K_e = 2.55$ and $K_i = 2.00$. According to Tab. II, this minimizes the settling-time.

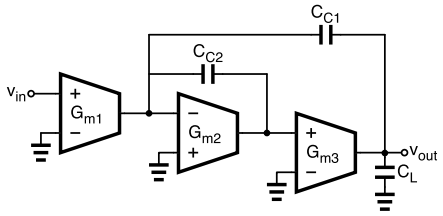

Fig. 10. Block schematic of a three-stage amplifier. The compensation is performed through a Reversed Nested Miller network composed by capacitors C_{C1} and C_{C2}.

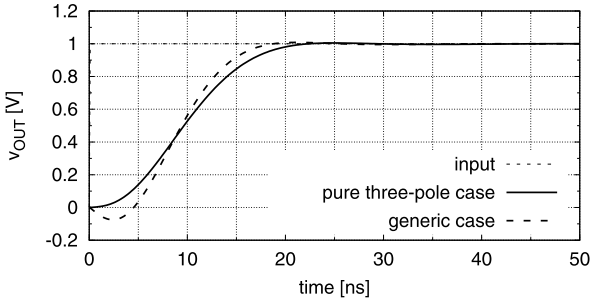

Fig. 11. Three-pole amplifiers. Time response to a step input for two different design cases. Maintaining the same GBW and the same global separation factor, the two responses are equivalent.

For the generic amplifier we simulated the topology in Fig. 10, for which we assumed that $G_{m1} = 100\,\mu\mathrm{A/V}$, $C_{C1} = 1\,\mathrm{pF}$ and $C_L = 2\,\mathrm{pF}$ were known[4] and used (34) to finalize our design with the constraints $\hat{K}_e = 2.55$ and $\hat{K}_i = 2.00$.

The coefficients of the transfer function in (31) are

$$\mathrm{GBW} = \frac{G_{m1}}{C_{C1}} \tag{35a}$$

$$a_1 = \frac{C_L C_{C2}}{C_{C1} G_{m3}} + \frac{C_{C2}}{G_{m3}} - \frac{C_{C2}}{G_{m2}} \tag{35b}$$

$$a_2 = \frac{C_{C2} C_L}{G_{m2} G_{m3}} \tag{35c}$$

$$b_1 = -\frac{C_{C2}}{G_{m2}} \tag{35d}$$

$$b_2 = -\frac{C_{C1} C_{C2}}{G_{m2} G_{m3}} \tag{35e}$$

Hence, we set C_{C2} to the reasonable value of 1 pF and used (34) to obtain $G_{m2} = 653\,\mu\mathrm{A/V}$ and $G_{m3} = 655\,\mu\mathrm{A/V}$.

In both cases the simulated GBW is 100 Mrad/s (about 15.5 MHz). In the pure three-pole case, the simulated settling-time is 21.5 ns (NST = 0.41). In the generic case, the settling-time results 23.5 ns (NST = 0.44). The plots of the two output responses are shown in Fig. 11 where a good matching between the two curves is apparent.

D. Large-Signal Analysis and Slew-Rate Modeling

Similarly to the two-pole case, even the slew-rate analysis of three-pole amplifiers deals with amplifiers with the slew-rate limitation in the first stage. If this condition is not guaranteed, the circuit can experience large overshoots and

[4]Usually, G_{m1} is known because set by noise specifications. Then, C_{C1} was set accordingly so maintain the same GBW for an effective comparison.

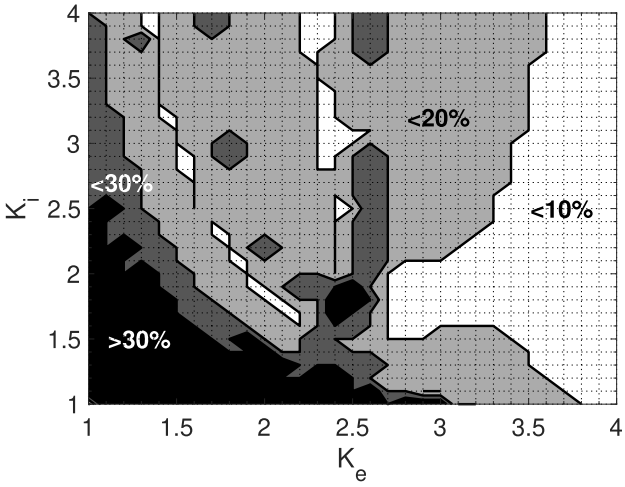

Fig. 12. Maximum percentage error between the NST of a simulated three-pole amplifier and the values predicted by (23). The accuracy level is $\epsilon = 0.5\%$. White: the error is below 10%. Light gray: the error is between 10% and 20%. Dark gray: the error is between 20% and 30%. Black: the error is above 30%.

increase the settling-time due to positive feedback connections during the slewing period [24]. Slew-rate enhancers [48] or class-ab topologies [27], [49] can be used to guarantee that the limitation is in the first stage.

As we assumed in section III-D, referring to the slew-rate of two-pole amplifiers, also in this case we take for granted that, with respect to the situation without SR limitations, the NST increases with (22). Therefore, we assume that the NST behaves as in (23).

We checked the validity of this statement by computing the maximum percentage error between the NST of a simulated three-pole amplifier and the values predicted by (23). The amplifier was realized with the block schematic in Fig. 1b where $\nu = 0.1$ V and

$$Q(\bar{s}) = \frac{1}{1 + \frac{\bar{s}}{K_e} + \frac{\bar{s}^2}{K_e^2 K_i}} \tag{36}$$

The separation factors, K_e and K_i, were swept in the range $[1.0, 4.0]$ and for each pair of points, we simulated the maximum error between the settling-time and (23) while sweeping the output signal, $\Delta Y/\nu$, from 0.5 to 10.0. The plot in Fig. 12 shows the region where the error remains below 10% (white), the region where the error is between 10% and 20% (light gray), the region where the error is between 20% and 30% (dark gray), and the region where the error is above 30% (black).

The sets of simulations discussed above, confirmed that (23) is a fairly good approximation of the behavior of the NST also in three-pole amplifiers.

V. The Settling-Time Based Design Procedure

In this section we propose a procedure for the design of a three-stage OTA[5] on the basis of settling-time requirements.

[5]The procedure can be used also for the design of a two-stage OTA whose open-loop gain can be modeled with a third-order transfer function, such as a two-stage amplifier that exploits the Ahuja compensation [51].

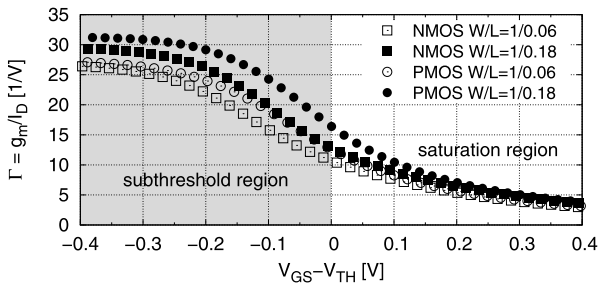

Fig. 13. Plot of the g_m-over-I_D ratio versus $V_{GS} - V_{TH}$ for a 65-nm process. Two different channel lengths for NMOS and PMOS type transistors are reported.

In the general context described so far, the OTA is modeled by the block schematic in Fig. 1. In sections III and IV we found that, with a proper choice of the separation factors, the small-signal normalized settling-time, NST_0, can be set less than 1 and that, under the presence of slew-rate limitations, the overall normalized settling-time behaves as in (23). Unfortunately, we cannot use (23) as a design equation because we cannot guarantee a precise value of NST_0. However, we can use (12), instead, provided that we ensure $\mathrm{NST}_0 \lesssim 1$.

Let us focus our attention on the argument of (12), $\Delta Y/\nu$. Replacing the value of ν in (11), we obtain

$$\frac{\Delta Y}{\nu} = \beta \frac{G_m}{I_o} \Delta Y \tag{37}$$

It is clear that the higher is the value of (37) the higher is the NST and, consequently, the settling-time. In general, β is a fixed quantity that depends on the application. In those applications where β can be programmed from $\beta_{\min}$ to $\beta_{\max}$ (i.e., in programmable A/D or D/A converters, β can be selected by changing the connections of a suitable array of capacitors), the amplifier must be designed in the worst-case scenario, that is, for $\beta = \beta_{\max}$. Regarding ΔY, the worst case depends on the power supply, V_{DD}. However, in some cases the maximum output can be lower than V_{DD}, and the design is more relaxed (i.e., in SC amplifier where the output returns to zero during the sampling phase, the maximum output step is limited to $\pm V_{\mathrm{DD}}/2$ during the evaluation phase). Finally, as far as the ratio G_m/I_o is concerned, it is strictly related to the bias point of the first stage. More specifically, referring to the typical case of a CMOS source coupled differential pair, G_m and $I_o/2$ are the small-signal transconductance and the bias current of each input transistors, respectively. Therefore

$$\frac{G_m}{I_o} = \frac{\Gamma}{2} \tag{38}$$

being Γ the transistor g_m-over-I_D ratio, a parameter that defines the bias condition of the device [52]. Fig. 13 reports the simulated plot of Γ versus the gate-source overdrive, $V_{GS} - V_{\mathrm{TH}}$, for the standard-threshold and complementary devices of a 65-nm process.[6] In the lighter area ($V_{GS} > V_{\mathrm{TH}}$)

[6]Although the plot is obtained for a particular CMOS process, similar plots are common to many technologies and do not differ very much from each other [53].

the transistors operate in the saturation region. In the darker area the transistors operate in the subthreshold region. In the analog design scenario, all transistors are biased so that $V_{GS} \sim V_{\rm TH}$. This makes the stage more efficient since, for a given drain current, the transistors exhibits a higher transconductance. Furthermore, this reduces also the drain-source saturation voltage ($V_{DS}^{\rm sat}$) thus providing more room for voltage swing, a critical requirement in low-voltage applications. However, from (38), a higher Γ means a slower amplifier, so that a trade-off between speed and power dissipation must be considered while setting the bias currents of the devices of the first stage. Due to all these considerations, the choice of the g_m-over-I_D ratio has a limited range (typically, $8\,{\rm V}^{-1} \leq \Gamma \leq 16\,{\rm V}^{-1}$).

From the above discussion, we can finally obtain our fundamental design equations that relates the GBW to the settling-time specification. Solving (8) for the GBW, using (12) for the NST, and considering (38) with $\Delta Y = V_{\rm DD}$, we have

$$\mathrm{GBW} = \frac{|\ln\epsilon| + \beta\frac{\Gamma}{2}\,V_{\rm DD} - \left[1 + \ln\left(\beta\frac{\Gamma}{2}\,V_{\rm DD}\right)\right]}{t_s} \tag{39}$$

that allows the designer to set the GBW on the basis of the required settling-time, and other amplifier parameters.

The value of the transconductance of the first stage, $G_{\rm m1}$, is imposed on the basis of noise considerations. Assuming for the first stage the CMOS source coupled differential pair and neglecting the flicker noise to simplify the discussion, the input voltage spectral density of the OTA is approximated by

$$S_n = 2 \cdot 4kT \cdot \frac{2}{3}\frac{1}{G_{\rm m1}}\,(1+c) \tag{40}$$

being k the Boltzmann's constant, T the absolute temperature and $c \sim 1$ a coefficient that depends on the transconductor topology. Therefore the value of $G_{\rm m1}$ results

$$G_{\rm m1} \approx \frac{16}{3}\frac{kT}{S_n}\,(1+c) \tag{41}$$

In Miller-compensated amplifiers the main capacitor connected between the output of the first stage and the output of the overall amplifier, $C_{\rm C1}$, is responsible for the gain-bandwidth product as $\mathrm{GBW} = \beta G_{\rm m1}/C_{\rm C1}$. Therefore, we obtain for $C_{\rm C1}$

$$C_{\rm C1} = \frac{\beta G_{\rm m1}}{\mathrm{GBW}} \tag{42}$$

The remaining design equations come from (34) where $\hat{K}_e$ and $\hat{K}_i$ must be set as in Tab. II or at a slightly higher value to mitigate the effects of the discontinuities at the absolute minimum points of the NST function.

The steps of the proposed design procedure are summarized in Fig. 14.

Start Known parameters are $V_{\rm DD}$, $C_{\rm L}$, β, S_n, t_s and ϵ
1) Choose the g_m-over-I_D (Γ) of the first stage on the basis of a speed/dissipation trade-off
2) Evaluate the GBW from (39)
3) Evaluate $G_{\rm m1}$ from (41)
4) Evaluate the main compensation capacitor, $C_{\rm C1}$, from (42)
5) Assuming the open-loop transfer function as in (31), determine coefficients a_1, a_2, b_1 and b_2 in terms of the amplifier parameters (i.e., transconductances, capacitors, etc.)
6) Choose $\hat{K}_e$ and $\hat{K}_i$ from Tab. II
7) Use the two equations in (34) for dimensioning two proper unknown parameters of the amplifier

Fig. 14. Steps of the proposed design procedure.

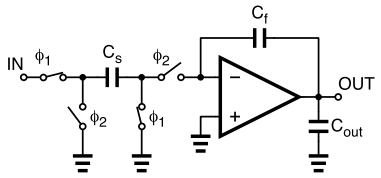

Fig. 15. Forward-Euler SC integrator.

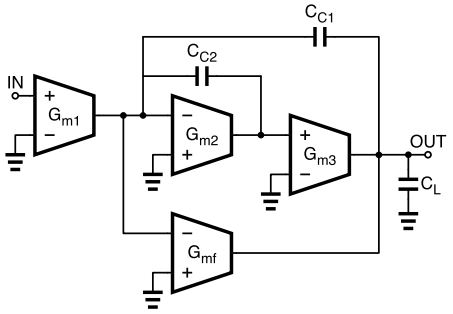

Fig. 16. Block schematic of a RNMC-FF three-stage amplifier. The compensation is performed through a Reversed Nested Miller network, composed by capacitors $C_{\rm C1}$ and $C_{\rm C2}$, and a feed-forward transconductor, $G_{\rm mf}$.

VI. Design Example and Validation

In this section, to demonstrate and confirm the advantages of the design procedure presented, we are going to describe the design of a three-stage operational transconductance amplifier (OTA) suitable for the switched-capacitor application shown in Fig. 15 where $C_s = C_f = C_{\rm out} = 0.4\,{\rm pF}$. During the evaluation phase, ϕ_2, the OTA drives the load capacitance $C_{\rm L} = C_{\rm out} + C_s C_f/(C_s + C_f) = 0.6\,{\rm pF}$ with the feedback factor $\beta = C_f/(C_s + C_f) = 0.5$. The sampling frequency of the SC integrator is assumed $f_s = 1/T_s = 25\,{\rm MHz}$ so that the output signal is required to settle within the interval of time $T_s/2 = 20\,{\rm ns}$, with a maximum error $\epsilon = 0.5\%$. The power supply is $V_{\rm DD} = 1\,{\rm V}$.

Among the various three-stage OTA topologies, we chose a Reversed Nested Miller Compensated amplifier which is intrinsically advantageous with respect to a Nested Miller one [54]. In particular, for its simplicity, we considered the topology with two capacitors only (i.e., with no elements to eliminate the RHP zero) and a Feed-Forward stage that slightly improves the large signal behavior. The amplifier block schematic, named RNMC-FF, is shown in Fig. 16.

The transistor-level implementation is shown in Fig. 17 and exploits a 65-nm CMOS process provided by STMicroelectronics. Standard threshold devices ($t_{\rm ox} = 1.8\,{\rm nm}$, $V_{\rm THn} \sim 470\,{\rm mV}$ and $|V_{\rm THp}| \sim 440\,{\rm mV}$) were used for all the transistors with the exceptions of the source coupled pair, M1–M2

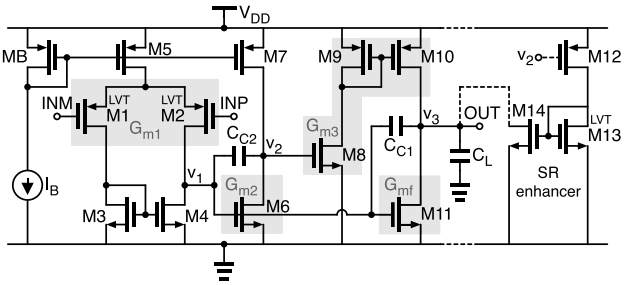

Fig. 17. Transistor-level schematic of the RNMC-FF three-stage amplifier.

($t_{ox} = 1.3\,\text{nm}$ and $|V_{THp}| \sim 243\,\text{mV}$) and of the slew-rate enhancer device, M13 ($t_{ox} = 1.8\,\text{nm}$, $V_{THn} \sim 317\,\text{mV}$).

The first stage of the OTA is made up of a PMOS source coupled differential pair with current mirror load (M1–M5). The common source M6, biased by M7, is the second stage. The common source M8 and the current mirror M9–M10, used to obtain a further signal inversion, realize the third stage. Transistor M11 acts as the feed-forward stage, G_{mf}, and provides the bias current to the third stage.

To overcome the slew-rate (SR) limitations that occur during negative steps at the output node, the SR enhancer M12–M14 was added in parallel to M11 to help the discharge of the load capacitor. The SR enhancer works as follows. In bias condition, M12 reads the voltage v_2 and provides a small (and negligible) current to the low-threshold transistor, M13. Since the threshold voltage of M14 is higher than that of M13, the SR enhancer is designed so that, in bias condition, the regular-threshold device, M14, remains disconnected from the output node. This is accomplished by setting

$$[V_{GS13}]_{\text{bias}} < V_{TH14} \tag{43}$$

When node v_2 goes low and transistor M8 switches off (i.e., $v_2 = V_{TH8}$), the increment of current in M12 must be able to increase the gate-source voltage of M13 above the threshold voltage of M14, thus connecting this latter device to the output node to sink the extra current. To do so, the SR enhancer must satisfy the condition

$$[V_{GS13}]_{v_2=V_{TH8}} > V_{TH14} \tag{44}$$

In our design, we assumed that the specifications on the input noise spectral density, S_n, imposed $G_{m1} = 320\,\mu\text{A/V}$. Therefore, we chose $\Gamma = 16\,\text{V}^{-1}$ for the g_m-over-I_D ratio of M1–M2 and, using (39), we obtained the minimum required GBW of 55 MHz.

At this point, we should evaluate capacitor C_{C1} from (42). However, due to the low transistor intrinsic gain ($g_m r_d \sim 10$), (42) overestimates the value of the compensation capacitor which would lead to a lower GBW. The actual expression of the GBW takes the form [18]

$$\text{GBW} = \frac{\beta G_{m1}}{C_{C1}} \cdot \frac{1}{1+\eta} \tag{45}$$

where, for the RNMC-FF OTA, the error is

$$\eta = \frac{1}{G_{m2} R_{o2}} + \frac{C_{C2}/C_{C1}}{G_{m2} R_{o1}} \tag{46}$$

TABLE III
RESULTS OF THE DIMENSIONING PROCEDURE

Parameter	Value
G_{m1}	$320\,\mu\text{A/V}$
G_{m2}	$664\,\mu\text{A/V}$
G_{m3}	$664\,\mu\text{A/V}$
G_{mf}	$664\,\mu\text{A/V}$
C_{C1}	385 fF
C_{C2}	247 fF

being R_{oi} the output resistance of the i-th stage. Assuming $G_{m2} R_{o1,2} \sim 10$ and $C_{C1} \sim C_{C2}$, we can estimate the error as $\eta \sim 0.2$. This means that we can use all the expressions that we derived so far, provided that we dimension our circuit for an equivalent GBW which is 20% higher than that obtained from (39). Therefore we set GBW = 66 MHz and evaluate $C_{C1} = 385\,\text{fF}$ from (42).

The open-loop transfer function takes the expression in (31) where

$$b_1 = \left(\frac{G_{mf}}{G_{m3}} - 1\right) \frac{C_{C2}}{G_{m2}} \tag{47a}$$

$$b_2 = -\frac{C_{C1} C_{C2}}{G_{m2} G_{m3}} \tag{47b}$$

$$a_1 = \left(1 + \frac{C_L}{C_{C1}}\right) \frac{C_{C2}}{G_{m3}} + \left(\frac{G_{mf}}{G_{m3}} - 1\right) \frac{C_{C2}}{G_{m2}} \tag{47c}$$

$$a_2 = \frac{C_L C_{C2}}{G_{m2} G_{m3}} \tag{47d}$$

Setting $G_{mf} = G_{m3}$, coefficient b_1 becomes zero and a_1 turns into

$$a_1 = \left(1 + \frac{C_L}{C_{C1}}\right) \frac{C_{C2}}{G_{m3}} \tag{48}$$

Substituting these coefficients in (34) and using the values[7] in Tab. II for $\hat{K}_e$ and $\hat{K}_i$, we obtain two equations that can be solved for the two unknown time constants, $\tau_1 = C_{C2}/G_{m3}$ and $\tau_2 = C_L/G_{m2}$. Since C_L is known, G_{m2} is easily evaluated. Setting $G_{m3} = G_{m2}$ allows us to determine C_{C2}, also. The values obtained from the dimensioning procedure are reported in Tab. III. The corresponding transistors' aspect ratios are reported in Tab. IV.

All the simulations were conducted using the Spectre simulator in the Cadence environment. The open-loop gain of the SC integrator in Fig. 15 was carried out through an ac-sweep simulation. The resulting Bode plot is shown in Fig. 18. The circuit exhibits a GBW of 57.5 MHz, which is the value required by (39), with a phase margin of 65 deg. The simulated GBW is in agreement with the discussion that led to relationships (45) and (46).

All the remaining transient simulations concern the step responses of the SC integrator during the evaluation phase, ϕ_2. Hence, the circuit was simulated using the simplified schematic in Fig. 19. In this case, the input step was set equal to the voltage stored in C_s during the sampling phase, ϕ_1, but

[7] To mitigate the effects of the discontinuities at the absolute minimum points of the NST function, we increased $\hat{K}_e$ and $\hat{K}_i$ by 10% with respect to the values reported in Tab. II.

TABLE IV
TRANSISTORS' ASPECT RATIOS FOR THE RNMC-FF OTA

Transistor	Aspect ratio
M1*, M2*	5.5/0.12
M3, M4	2/0.25
M5	16/0.25
M6, M8, M11	6/0.25
M7	20/0.25
M9, M10	18/0.25
M12	0.5/0.12
M13*	0.5/0.25
M14	5/0.12
MB	8/0.25

* Low-voltage transistors

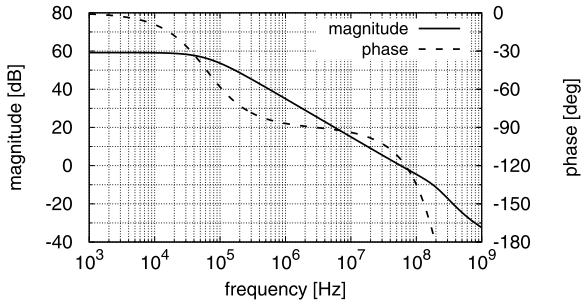

Fig. 18. OTA loop gain Bode plots: magnitude (solid line) and phase (dashed line).

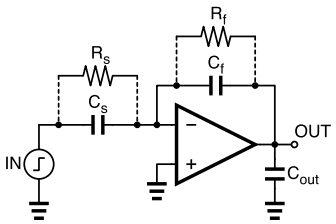

Fig. 19. Equivalent schematic of the Forward-Euler SC integrator.

changed in sign. Two big resistors, R_f and R_s (in the order of tenths of megaohms), were used to create a dc path across the integrator thus setting its bias point.[8]

The transient responses of the closed-loop amplifier to different input steps are shown in Fig. 20. Subfigures 20a and 20b report the response to a ±100-mV step for the rising edge at the output and the falling one, respectively. The simulated 0.5-% settling-times are 7.8 ns (NST = 0.52) and 9.8 ns (NST = 0.66), respectively. With respect to the minimum theoretical NST reported in Tab. II, this is a good result if we consider the approximate nature of the transfer function in (31) (the amplifier has other poles that were not considered because placed at higher frequencies) and of coefficients in (47) (where we neglected the contributions of the output resistances and capacitors of the transconductors). Subfigures 20c and 20d report the response to a ±800-mV step. This signal excursion is close to the rail-to-rail situation but still guarantees that all

[8]To not alter the overall transfer function of the integrator the two resistors must satisfy the constraint $R_s C_s = R_f C_f$.

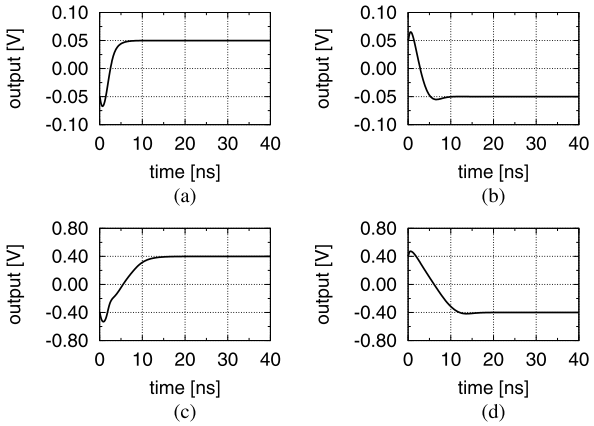

Fig. 20. Transient simulation of the closed-loop amplifier compensated with the RNMC-FF. (a) +100-mV output step. (b) −100-mV output step. (c) +800-mV output step. (d) −800-mV output step.

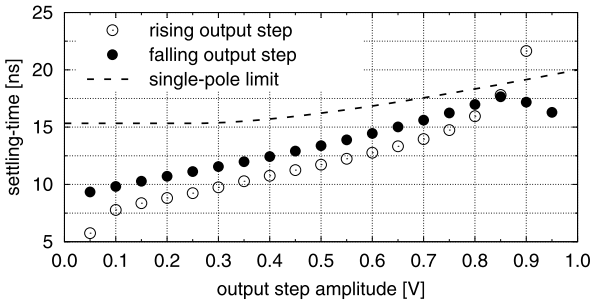

Fig. 21. Settling-time versus output step amplitude for the closed-loop amplifier compensated with the RNMC-FF. The plot shows also the single-pole limit evaluated using (12).

the transistors work in the saturation region. Due to slew-rate limitations, the 0.5-% settling-times increase up to 16.0 ns (NST = 1.07) and 17.0 ns (NST = 1.14), for the rising output step and the falling one, respectively.

The plot of the 0.5-% settling-time versus the output step amplitude is shown in Fig. 21. The curve of the single-pole limit, that was used to obtain the GBW specification from (39), is also reported. The settling-times, for both the rising and the falling edges, remain below the single-pole limit except when the output step approaches the supply voltage, V_{DD}, because some transistors exit from the saturation region. Despite this, the settling-time specifications are guaranteed up to an output step of 850 mV. The small differences in the rising settling-time with respect to the falling one are justified by the asymmetrical structures of the two final stages of the amplifier. The figure validates the proposed SR modeling and the design procedure advanced in section V. In particular it confirms the goodness of (39) in determining the GBW specification from the settling-time requirements.

A final Monte-Carlo simulation (400 run) was carried out to check the behavior of the circuit under both global and local process variations. The results are summarized in the histograms in Fig. 22. Subfigures 22a and 22b refer to the rising and the falling cases of a ±100-mV output step. Subfigures 22c and 22d refer to the rising and the falling cases of a ±800-mV output step. As revealed from Fig. 22d, a very small

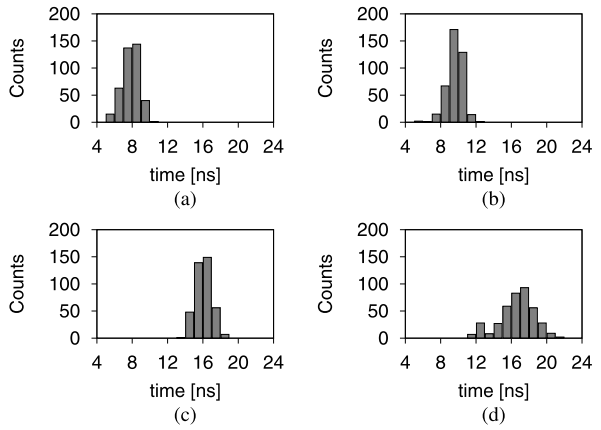

Fig. 22. Monte-Carlo simulation of the settling-time of the closed-loop amplifier compensated with the RNMC-FF. (a) +100-mV output step. (b) −100-mV output step. (c) +800-mV output step. (d) −800-mV output step.

number of samples fall outside the settling-time specifications of 20 ns, a good result considering that the circuit was not designed to be robust against process variations. However, our design procedure can be easily extended in the worst case corner of a PVT scenario or integrated with the approach proposed in [28].

VII. Conclusion

In this paper we analyzed the settling-time in single-, two- and three-stage amplifiers including the effects of the zeros and of the slew-rate limitations. The analysis led to useful design equations and to an approach for the design of three-stage CMOS operational transconductance amplifiers from settling-time specifications. A design example was carried out on to validate the theoretical analysis and the proposed design procedure.

Appendix A
Normalized Settling-Time for the Single-Pole Amplifier With Slew-Rate Limitation

A single-pole amplifier with slew-rate limitation can be modeled with the equivalent block schematic in Fig. 1b with $Q(\bar{s}) = 1$.

The differential equation related to the state variable x is[9]

$$\dot{x}(\bar{t}) = \begin{cases} -x(\bar{t}) + \dfrac{u(\bar{t})}{\beta} & \text{for } \left|\dfrac{u(\bar{t})}{\beta} - x(\bar{t})\right| < \nu \\ \nu & \text{for } \left|\dfrac{u(\bar{t})}{\beta} - x(\bar{t})\right| \geq \nu \end{cases} \tag{49}$$

with $y(\bar{t}) = x(\bar{t})$.

Assuming that we apply a positive input step[10] of amplitude $\Delta U/\beta \geq \nu$, the amplifier enters the slewing period. Relationship (49) reduces to

$$\dot{x}(\bar{t}) = \nu \tag{50}$$

[9]Remember that, since the amplifier in Fig. 1b is normalized with respect to the GBW, the time is the dimensionless variable $\bar{t} = \text{GBW} \cdot t$.

[10]A similar discussion can be made for a negative input step, $\Delta U/\beta \leq -\nu$.

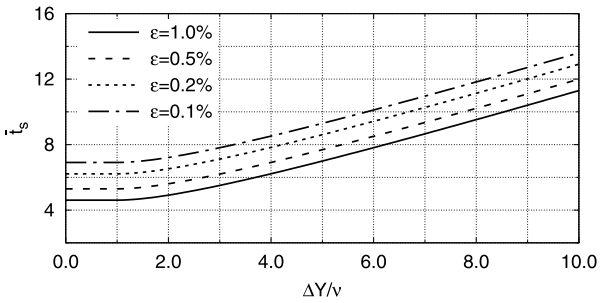

Fig. 23. Plot of the dimensionless settling-time, $\bar{t}_s$, versus $\Delta Y/\nu$ for the single-pole amplifier.

whose solution is

$$x(\bar{t}) = \nu \cdot \bar{t} \quad \text{for } \bar{t} < \bar{t}_{\text{SR}} \tag{51}$$

being $\bar{t}_{\text{SR}}$ is the time at which $\Delta U/\beta - \nu \cdot \bar{t}_{\text{SR}} = \nu$ or

$$\bar{t}_{\text{SR}} = \frac{\Delta U/\beta}{\nu} - 1 \tag{52}$$

For $\bar{t} \geq \bar{t}_{\text{SR}}$, the saturation block is linear and (49) becomes

$$\dot{x}(\bar{t}) = -x(\bar{t}) + \frac{\Delta U}{\beta} \tag{53}$$

whose solution is of the type $x(\bar{t}) = A\mathrm{e}^{-(\bar{t}-\bar{t}_{\text{SR}})} + B$. Constants A and B can be determined considering that

$$x(\bar{t}_{\text{SR}}) = \frac{\Delta U}{\beta} - \nu \tag{54a}$$

$$x(+\infty) = \frac{\Delta U}{\beta} \tag{54b}$$

and

$$x(\bar{t}) = -\nu \cdot \mathrm{e}^{-(\bar{t}-\bar{t}_{\text{SR}})} + \frac{\Delta U}{\beta} \quad \text{for } \bar{t} \geq \bar{t}_{\text{SR}} \tag{55}$$

Bearing in mind that $y(\bar{t}) = x(\bar{t})$ and applying the definition of the settling-time in (5), we obtain

$$\bar{t}_s = \bar{t}_{\text{SR}} + \ln\left(\frac{1}{\epsilon}\frac{\nu}{\Delta U/\beta}\right) \tag{56}$$

Taking into account (52) and defining the output step as

$$\Delta Y = \frac{\Delta U}{\beta} \tag{57}$$

the dimensionless settling-time results

$$\bar{t}_s = |\ln \epsilon| + \frac{\Delta Y}{\nu} - \left(1 + \ln\frac{\Delta Y}{\nu}\right) \tag{58}$$

which is valid under the initial assumption of large-signal, $\Delta Y/\nu \geq 1$. The plot of (58) versus $\Delta Y/\nu$ is shown in Fig. 23 where $\bar{t}_s = |\ln \epsilon|$ was considered for $\Delta Y/\nu < 1$.

Evaluating the NST means dividing the dimensionless settling-time, $\bar{t}_s$, by its small-signal value, $|\ln \epsilon|$. Therefore, we can write our final relationship in (12).

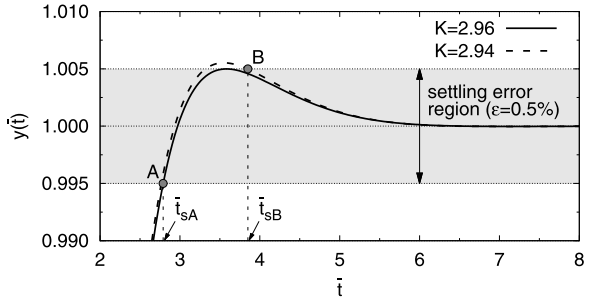

Fig. 24. Plots of the output, $y(\bar{t})$, for two different values of K. The response for $K = 2.96$ (solid line) leads to the minimum NST. The response for $K = 2.94$ (dashed line) explains the jump discontinuity in the settling-time.

APPENDIX B
JUMP DISCONTINUITIES IN THE NST

The plot of the NST in Fig. 3 presents several jump discontinuities, a consequence of the oscillating nature of the output response and of the settling-time definition in (5). In this appendix we are going to explain where they come from.

As known, the settling-time is defined as the time required to the output to reach its final value within an assigned settling error, ϵ. The plot in Fig. 3 was obtained with MATLAB by applying a unity step to the closed-loop system in (15) and evaluating the corresponding time response, $y(\bar{t})$. For each value of K, we computed the dimensionless 0.5-% settling-time, $\bar{t}_s(K)$, and, finally, we divided the result by $|\ln \epsilon|$, thus obtaining the NST versus K. Since the NST and $\bar{t}_s$ differ by the product of a constant term, we are going to inspect how the dimensionless settling-time behaves as we move K.

Fig. 24 shows the time response of the output, $y(\bar{t})$, for two different values of K. In the figure, the solid curve is the output response obtained for $K = 2.96$. From Tab. I, this is the value that results in the minimum NST for $\epsilon = 0.5\%$. In this case, indeed, the first peak of $y(\bar{t})$ just touches the upper settling error limit and the output enters the settling error region in the point 'A', thus reaching the absolute minimum settling time identified by $\bar{t}_{sA}$ in the figure [55].

For a slightly lower value of K, the output becomes as that in the dashed line in Fig. 24, where the specific case of $K = 2.94$ is depicted. In this case, the output enters the settling error region in the point 'B' and the settling-time jumps from $\bar{t}_{sA}$ to $\bar{t}_{sB}$, thus causing the discontinuity observed in the proximity of $K = 2.96$ in Fig. 3. In a similar manner, the other jump discontinuities observed in Fig. 3 arise when the oscillations cause the subsequent peaks of $y(\bar{t})$ to touch the settling error limits of the settling error region.

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