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PH.D. DISSERTATION

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DESIGN OF CMOS ANALOG BUILDING BLOCKS FOR ULTRA-LOW CURRENT AND ULTRA-LOW VOLTAGE APPLICATIONS

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To mom, dad and my sister who are everything to me.

To grandmother Pina, to whom all my childhood and life memories are linked. I treasure the memory of our favorite game: going out and watching the trains from the street near her house. I still remember the way she held my hand which was strong and loving at the same time. She taught me to look at the world with sensitive and courageous eyes. This small milestone and also those that will arrive in the future are dedicated to her.

Abstract

Modern systems on a chip (SoC) contain more and more features that need to be smarter than ever, leading to the rapid growth of low-power systems such as portable and wearable medical electronic devices, smartphones, wireless intelligent systems, wireless sensor networks, wearable health-care monitoring devices and so on. Of course, due to the limited energy storage of primary or secondary batteries, low-power design techniques are mandatory to significantly reduce energy consumption. However, designing ultra-low voltage and ultra-low current analog and mixed-signal integrated circuits, especially in nanoscale technology, represents a major challenge.

In this PhD thesis, the limitations of low-power operation in analog design were analyzed along with the most widely used low-voltage, low-current analog design techniques that overcome these restrictions.

After this preliminary description, two fundamental CMOS analog building blocks were designed under ultra-low voltage and low power conditions: (1) Voltage references and (2) Operational transconductance amplifiers (OTAs). An accurate analysis of these circuit topologies was carried out, also validated by exhaustive schematic and post-layout simulations and by experimental results. Comparison with the state of the art was also performed to assess the objectives achieved by this research in comparison with the literature.

Specifically, the proposed solutions are briefly described below.

A first solution of 160-nm CMOS resistor-less nano-power voltage reference with trimming strategy was proposed, designed, and measured. The solution is the only one in the literature able to cover both the widest range of supply voltage and temperature which are 1.2 to 5 V and –40 to 125 °C, respectively. A measured reference voltage of 348 mV was found with only 25-nA of current consumption. The solution is also characterized by a reduced value of Line Sensitivity (LS) which is 0.14 %/V with a reference voltage variation of 1.81 mV.

The above 160-nm CMOS resistor-less nano-power voltage reference with trimming strategy was also cascaded by an analog output voltage buffer with ultra-low current consumption. The proposed buffer was expressly designed to complement the ultra-low-current reference voltage reference with the main goal to preserve the key performance. Experimental results provide validation that the reference voltage and the LS are preserved and maintained equal to 348 mV and 0.14 %/V, respectively, even with the use of the buffer. The total supply current is 45 nA while the supply voltage range is from 1.2 to 5 V.

A second solution, a 28-nm CMOS resistor-less voltage reference with process corner compensation for biomedical application was proposed, designed, and measured. The main novelty of the proposed topology relies in the trimming strategy of the active load which allows to reduce by a factor of 10 the reference voltage variation across corners with respect to the same reference topology without trimming.

A 50pF-400pF 0.4-V subthreshold bulk-driven rail-to-rail CMOS Operational Transconductance Amplifier (OTA) was also proposed and designed by using a 65-nm CMOS bulk technology. The adoption of the low supply of 0.4-V together with current consumption of 1.58-µA gives rise to a limited power consumption which is one of the advantages of the proposed OTA. The combination of low power consumption and overall good small-signal performances give rise to the best FoM_S (Figure of Merit) in the state of the art. Besides, the large signal performance has been compared through the FoM_L, providing one of the best results.

To conclude the research work, a 65-nm four-stage bulk-driven super class AB OTA was proposed. The solution is based on a modular topology in which additional gain stages based on the same structure can be cascaded to boost the DC gain and without requiring an explicit frequency

compensation (it is stable through the load capacitor). The proposed architecture allows to boost the DC gain from 58 dB to 88 dB by exploiting a 2-stage and a 4-stage configuration. This last DC gain value together with 0.4-V supply and 3.75-nA current consumption represents one of the best results achieved. Indeed, the small-signal performances (in terms of FoM_S) is the best one in the state of the art.

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C_{ox}: Oxide capacitance per area
f_T: Transition frequency
g_{ds}: Drain-source transconductance
g_m: Transistor transconductance
g_{mb}: Body transconductance
i_c: Inversion coefficient
I_D: Drain-current
k: Boltzmann's constant
k_t: temperature coefficient
L: Channel length
n: Slope factor
OTA: Operational Transconductance Amplifier
T_0: absolute temperature
V_A: Early voltage
V_{BS}: Bulk-source voltage
V_{DD}: Supply voltage
V_{DS}: Drain-source voltage
V_{DSsat}: Drain-source saturation voltage
V_{GS}: Gate-source voltage
V_{REF}: Reference voltage
V_T: Thermal voltage
V_{TH}: Threshold voltage
V_{TH0}: Threshold voltage when $V_{BS} = 0$
W: Channel width
γ: Technology-specific body factor
λ: Channel-length modulation coefficient
λ_D: drain-induced-barrier-lowering factor
μ: Mobility current carriers
Φ_F: Technology-specific Fermi's potential

List of Abbreviations

A/D: Analog-to-Digital
BD: Bulk driven
CMOS: Complementary Metal Oxide Semiconductor
CMRR: Common-Mode Rejection Ratio
CTAT: Complementary to absolute Temperature
D/A: Digital-to-Analog
DT: Dynamic threshold
FG: Floating gate
GBW: Gain-bandwidth
GD: Gate driven
IC: Integrated Circuit
IoT: Internet of Things
LS: Line Sensitivity
MOS: Metal Oxide Semiconductor
PSRR: Power-Supply Rejection Ratio
PTAT: Proportional to Absolute Temperature
PVT: Process, Voltage and Temperature
RMS: Root Mean Square
SiP: System-in-Package
SNR: Signal-to-Noise Ratio
SR: Slew Rate
SVR: Supply Voltage Rejection
TC: Temperature Coefficient

Chapter 1

Low-Power Analog Circuit Design

1.1 Introduction to Low-Power Analog Circuit Design

The foundation of the unprecedent success of the electronics industry is given by the invention of the integrated circuits (IC) in 1958 which replaced discrete-devices electronics. According to the well-known prediction of Gordon Moore who claimed that circuit complexity would double over two years, the number of devices inside a chip has increased exponentially leading to the development of multi-function circuits integrated into a single chip [1]. Technology scaling with the minimization of transistors sizing has made possible the reduction of both the occupied silicon area and cost per function. Over the years, research and development have been focused on raising operation speed and design complexity by focusing on the area occupation, cost and speed, the power consumption has been considered as a side issue.

A radical change towards ultra-low power electronics [2] was given by the development of two main types of systems: (1) portable and wearable battery-based systems that required little weight together with long battery operation time; (2) battery-less systems where energy is harvested from environment. Modern systems on chip (SoC) contain more and more functionalities which have to be smarter than ever before, leading to the rapid growth of low-power systems like portable and wearable medical electronic devices, smartphones, wireless smart systems, wireless sensor networks, wearable health care monitoring devices and so on. Of course, due to the limited energy storage of primary or secondary batteries, low-power design techniques are mandatory to significantly reduce power consumption [2]. However, ultra-low voltage and ultra-low current analog and mixed-signal IC design, especially in nanometer technology, represents a great challenge. Indeed, since the average power consumption of a CMOS digital circuit is proportional to the square of the supply voltage, the most efficient way to reduce power consumption in digital design is to reduce the supply voltage. However, the same approach is not effective for analog circuit design where the power consumption only marginally decreases by reducing the supply voltage. In fact, in this case the power consumption is mainly set by the required signal-to-noise ratio (SNR) and the frequency of the operation (or the required bandwidth). This leads to consider the power consumption required to process an analog signal almost independent of the supply voltage. In addition, low supply voltage may have a significant negative impact on the main parameters of an analog IC such as dynamic range, power supply rejection and noise immunity, among others. Comprehensive knowledge of the MOS transistor operating at very-low current and very-low voltage became also necessary leading to a more accurate low-power MOS transistor model development.

The aforementioned considerations are elaborated in the following sections.

1.2 Low-Voltage Analog Circuit Design Limitations

From the IC design point of view, the main drawback of decreasing the supply voltage is the reduction of the operational voltage range achieved by standard circuit topologies. Analog circuits are strongly affected from this limitation more than digital counterparts and this is exacerbated under the adoption of advanced nanoscale technologies. CMOS nanotechnologies through a thinner

layer of the gate oxide in the MOS transistor cause a great increase of the subthreshold leakage current, thus limiting the threshold voltage reduction. The dependence of the supply voltage V_{DD} and the threshold voltage V_{TH} on the technology node over years predicted by IRDS (International Roadmap for Devices and Systems) is shown in Fig. 1.

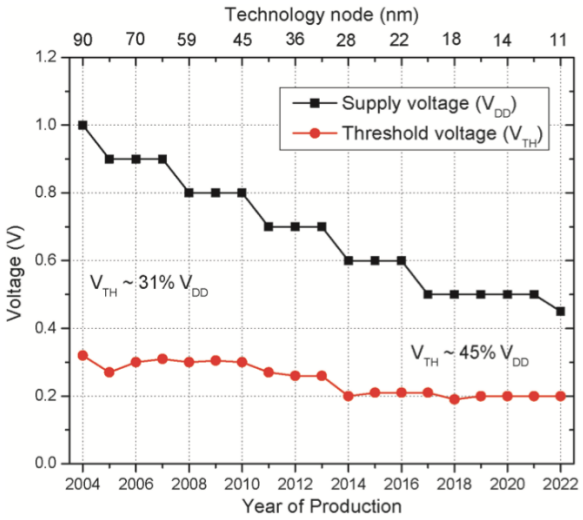


Fig. 1. Supply voltage and threshold voltage dependence on the technology node over years [10].

At a first glance, it can be observed that threshold voltage does not follow the supply voltage reduction trend over technology node as a result of the presence of the leakage current. The minimum supply voltage in a CMOS analog design is related both to the sum of the gate-source voltages V_{GS} of the MOS transistors and to the required voltage swing.

1.2.1 Analog signal processing limit

In analog signal processing circuits, the amount of the consumed power allows to maintain the signal energy above the fundamental limit of the thermal noise in order to achieve the required signal-to-noise ratio (SNR). For a given temperature T, the minimum power consumption of an analog circuit is set by the required SNR and the operating frequency f (or the required bandwidth). It can be also optimized by considering the voltage swing which is proportional to the ratio between the supply voltage and the peak-to-peak signal amplitude. Assuming k as the Boltzmann's constant, the minimum power consumption for a single pole circuit with rail-to-rail operation can be written as follows [3]:

$$P_{min} = 8kTfSNR \tag{1}$$

For every increase of 10 dB of SNR it's required a factor 10 of power increase thus making the strong limitation apparent.

On the other hand, the minimum power of a digital system in which each elementary operation requires a certain number m of binary gate transition cycles that dissipate an amount of energy E_{tr} can be expressed as follows:

$$P_{mindig} = mfE_{tr} \tag{2}$$

where f is the signal frequency.

Being the number of transition m weakly dependent on SNR in a logarithmic proportionality, this leads the minimum power dissipation of a digital system to follow this trend.

The immunity to the thermal noise imposes a minimum energy per transition E_{trmin} around $8kT$ by limiting also the absolute minimum power. These fundamental limits are shown in Fig. 2 where a comparison between power consumption of an analog and digital system as a function of SNR is

plotted. It is seen that analog systems may consume less power than a digital circuits when a small SNR is required. Otherwise, when a higher value of SNR is required, analog systems become inefficient [3].

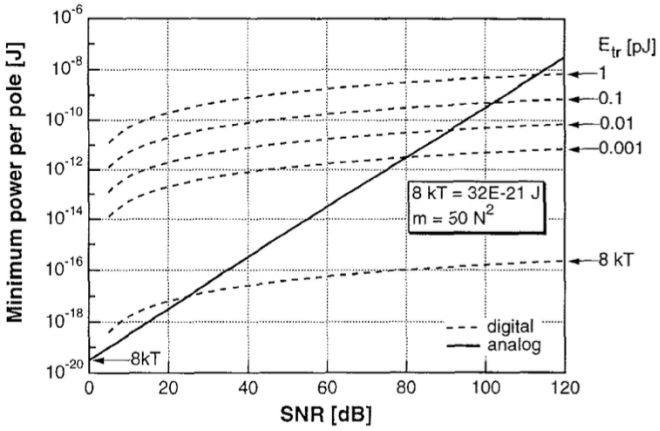


Fig. 2. Minimum power of analog and digital systems as a function of SNR.

1.2.2 MOS device operating in weak inversion

The threshold voltage V_{TH} does not decrease proportionally to the supply voltage V_{DD} as has already been stated. This leads to the reduction of the voltage headroom thereby limiting the available overdrive voltage. Limitations like this are exacerbated in circuits which contain stacked transistors such as cascode structure, often used in analog building blocks. The required minimum supply voltage is increased in stacked structures and this value should be sensibly higher than V_{TH} to ensure the conventional strong inversion region. For this reason, especially in nanoscale technology, the operating point of the transistors has been moved to moderate or weak inversion.

These different operating regions of the MOS transistor can be described by using the inversion coefficient i_c given by the ratio between the transistor drain current I_D and the specific current I_{spec}, expressed as follows:

$$i_c = \frac{I_D}{I_{spec}} = \frac{I_D}{2n\mu C_{ox}\frac{W}{L}V_T^2} \tag{3}$$

where n is the slope factor, μ is the mobility current carriers, C_{ox} is the oxide capacitance per area, W is the channel width, L is the channel length and V_T is the thermal voltage.

The different regions can be distinguished by using this parameter as follows: transistor operating in strong inversion for $i_c > 10$, in weak inversion for $i_c < 0.1$ and in moderate inversion for $i_c \cong 1$.

Weak inversion is used when the input voltage is lower than the threshold voltage. In this region a weak inversion layer beneath the gate is created and a very small number of the carriers create a diffusion current. It consists of the dominant current floating through the MOS transistor showing an exponentially dependence on the gate-source voltage V_{GS} (as a bipolar transistor). The main advantage of the use of the MOS transistors operating in weak inversion is the reduced power consumption in comparison to those operating in strong inversion.

1.2.3 MOS device models and g_m/I_D parameter

New simulation models of the MOS devices in advanced nanoscale technology have been developed with the aim to become more accurate in all the inversion regions. To give an example, the charge-based EKV model of the MOS transistor operating in all inversion region has been accurately discussed in [4]-[6] . This model uses one equation to describe all the inversion regions and thanks to its high accuracy can be successfully applied to low-voltage and low-power IC designs. The EKV model is based on g_m/I_D parameter which represents the transconductance

efficiency of a MOS transistor. Thanks to the adoption of this parameter, it is possible to effectively describe how much current (or power) has been transformed into device transconductance. Moreover, the g_m/I_D approach allows to reach the minimum power consumption at low operating current at the cost of lower speed and higher silicon area occupation. The widely used expression of g_m/I_D is related to i_c that defines the specific inversion region and is given by (4):

$$\frac{g_m}{I_D} = \frac{1}{nV_T} \frac{1}{0{,}5+\sqrt{0.25+i_C}} \quad (4)$$

This parameter is not-technology related, and so it can be used over different CMOS technologies.

1.2.4 Voltage headroom

The reduced transistor sizes and gate-oxide thickness to the order of nanometer have resulted in a lower breakdown voltage. Consequently, the supply voltage must be reduced to ensure the correct circuit operation and reliability. The voltage swing in a CMOS circuit determines the minimum value of the supply voltage V_{DD} under which it is able to operate. To give a quantitative example, a standard NMOS device in a 130 nm technology has a threshold voltage around 300 mV that is required to achieve saturation in the strong inversion region. In addition, the use of different NMOS devices in a stacked structure severely limits the minimum supply voltage which consequently shall be forced to be higher than 1 V. Better performances can be achieved by using multi-threshold process or BiCMOS technology with the disadvantages of a higher costs. Advanced techniques for IC design have been developed in a standard CMOS process to allow low-voltage and low-power operation. Nevertheless, ultra-low voltage design has an additional limitation related to the degradation of the DR which is the ratio between the maximum voltage swing (or supply voltage) and noise. Being the noise relatively constant, the lower value of the supply voltage leads to the DR degradation.

1.2.5 Process and temperature variations

It is very difficult to precisely ensure the design geometric dimensions, the doping profile, or the dielectric layer thickness in a fabricated chip, especially when the technology is deeply scaled. These physical variations have a negative impact to the electrical parameters of a circuit. In addition, electrical parameters can be also affected by the chip interconnections which generate several parasitics. Moreover, the semiconductor structure is subject to ageing, thus leading electrical parameters to change over time. These changes add other type of variations known as systematic errors.

A commercial IC has to be robust against temperature variations in a wide range of temperature (from – 40 °C to 85 °C at least) to ensure the industrial requirement. Temperature variations lead to a change in the behavior of some electrical parameters, thus adding several deviations and systematic errors in IC design parameters. The voltage headroom, for example, is strictly dependent on temperature. Therefore, making the circuit robust against process and temperature variations is an important restriction in a circuit design.

1.2.6 Mismatching

The IC performances are strictly related to the mismatch of the parameters. Systematic and random deviations already discussed, give rise to devices mismatch and consequently to a degradation of circuit parameters (such as the offset voltage in an operational amplifier). This situation is exacerbated in low-power operation where it is necessary a tradeoff between mismatch and low-power operation requirements. For example, amplifier's main parameters like common-mode-rejection ratio (CMRR) and power-supply-rejection ratio (PSRR) are deteriorated

both from mismatches and low-power limitations. Therefore, accurate layout techniques are convenient to reduce mismatches when the supply voltage becomes very low [7].

1.3 Low-Voltage Analog Circuit Design Techniques

Several techniques and approaches are suitable for low-voltage analog circuit design. The most used ones are: (1) MOS transistors operating in subthreshold region, (2) self-cascode structures, (3) level shifter techniques, (4) bulk-driven MOS transistors, (5) floating-gate MOS transistors and (6) dynamic-threshold MOS transistors. Generally, from the industry acceptance point of view, low-voltage approaches can be also divided into two groups: conventional methods and unconventional methods. The first group includes MOS transistors operating in subthreshold region, self cascode structures and level shifter techniques which represent the most common approaches to implement low-voltage analog design. On the other hand, unconventional methods include the remaining low-voltage techniques that are still gaining acceptance by the industry design standards.

1.3.1 MOS transistors operating in subthreshold region

Low supply voltage introduces several problems which have a negative impact on the circuit design. Among all, the limited inversion level the MOS transistors operate in has become a crucial issue. This turns out in higher mismatch between transistor parameters, higher temperature sensitivity and lower operational frequency. Moreover, the increased silicon area occupation due to large transistors dimensions must be required to compensate the low transconductance value. Consequently, this causes an increased noise and adds several secondary effects in transistor modeling. Another critical issue lies in the limited number of stacked transistors to ensure their operation in saturation region. MOS transistors operating in deep-subthreshold region have a theoretical limit for the saturation voltage defined as $V_{DS} \approx 4V_T \approx 4\frac{kT}{q}$, that is around 100 mV at room temperature (25 °C). The increased inversion level consequently rises this value.

As already discussed before, the MOS inversion region can be defined by the inversion coefficient i_c already defined in (3). MOS transistors operate in weak inversion for $i_c < 0.1$ and in strong inversion for $i_c > 10$. Moderate inversion region occurs when transistors operate exactly in the middle of these two regions. The relationship between the normalized power consumption, speed (in terms of cut-off frequency) and silicon area occupation as a function of the inversion coefficient is shown in Fig. 3 [8]. As can be seen by inspection of this figure, moderate inversion region represents a good trade-off between the considered performances for the most of analog circuits.

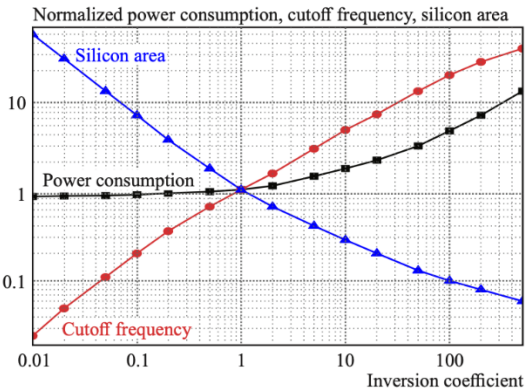


Fig. 3. Normalized power consumption, cut-off frequency and silicon area occupation as a function of the inversion coefficient.

When the input voltage V_{GS} is greater than the threshold voltage V_{TH}, the MOS transistor is working in strong inversion region. It means that inversion region creates a depletion region beneath the gate electrode and the drift current constitutes the overall current. The drain current depends quadratically on V_{GS} as follows:

$$I_D = \frac{1}{2}\mu C_{OX}\frac{W}{L}(V_{GS} - V_{TH})^2(1 + \lambda V_{DS}) \quad (5)$$

On the other hand, when the input voltage is lower than the threshold voltage the MOS transistor is working in weak inversion region. A small number of carriers create a diffusion current through a weak inversion layer beneath the gate electrode. This current constitutes the overall current and it depends exponentially on V_{GS} as follows:

$$I_D = 2\mu C_{OX}\frac{W}{L}V_T^2 e^{\left(\frac{V_{GS}-V_{TH0}}{V_T}\right)} \quad (6)$$

However, when the input voltage is comparable with the threshold voltage, the MOS transistor is working in the middle region known as moderate inversion. The current is given by a sum of (5) and (6) but in this case the drain current dependence on the input voltage (equation 7) is not exponential or quadratic and it is difficult to be described analytically.

$$I_D = \mu C_{OX}\frac{W}{L}V_T^2\left[\ln\left(1 + e^{\left(\frac{V_{GS}-V_{TH}}{2V_T}\right)}\right)\right]^2 \quad (7)$$

Although some complex equations are used to describe the behavior in the moderate inversion region, large errors or discontinuities in the small signal transistor parameters are inevitable. In addition, it is impossible to precisely predict the circuit performances of a circuit working in weak inversion with a hand calculation. Therefore, most of the designers assume MOS transistors work in strong inversion assuming power consumption and speed higher than needed [9].

Edge cases such as strong inversion and weak inversion do not provide a good trade-off between power consumption, area occupation and speed. Therefore, some attempts have been made over years to define a one-equation model suitable for all the operating regions. At this purpose, the g_m/I_D methodology represents a good compromise between transconductance g_m and drain-source saturation voltage V_{DSsat}. This methodology accurately describes moderate inversion region, that from the analog IC design point of view is the best way to achieve the minimum power consumption with a low current consumption at the cost of a lower speed and larger area occupation. An accurate transistor model does not take into account only the correct I-V characteristic but must include also the current derivatives such as, in this case, the transconductance. This method also simplifies the calculations of the transistor dimensions thus making easy a crucial design phase. The simplified expression of g_m/I_D was shown in equation (3), and it has become a fundamental equation for analog IC design thanks to its portability across different technologies. Fig. 4 shows the g_m/I_D dependence on the inversion coefficient i_c. Transistors operate in subthreshold region or weak inversion when $i_c \leq 0.1$. Under this condition, MOS transistors exhibit high voltage gain, low drain current and low saturation voltage at the cost of larger dimensions. Instead, transistors operate in above-threshold or in strong inversion region when $i_c \geq 10$. Although they show a lower gain and a larger drain current, MOS transistors working in this region are able to process high frequency signals and do not require large area occupation. Finally, the intermediate region or moderate inversion region ($0.1 \leq i_c \geq 10$) represents a good trade-off on the already mentioned performances.

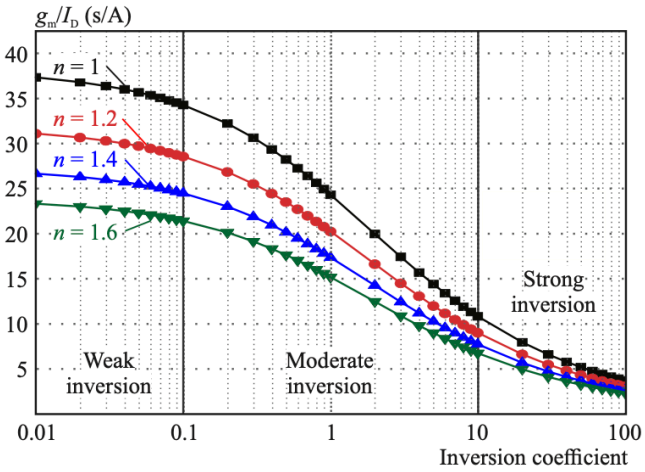


Fig. 4. Dependence of g_m/I_D parameter on the inversion coefficient i_c.

1.3.2 Self-cascode structures

The self-cascode structure with MOS transistors (shown in Fig. 5) offers a higher output impedance together with an increased input voltage swing compared to standard cascode ones [9]. The self-cascode is a two-transistor structure which can be treated as a single transistor where both transistor's gates are driven by a common input signal. The lower transistor M_1 works out of saturation while the upper transistor M_2 works in saturation. Under the following condition $(W/L)_2 \gg (W/L)_1$, the circuit acts as a single MOS transistor operating in saturation region with a significant reduction of the channel modulation effect λ. The output resistance r_{out} is approximately proportional to $(W/L)_2/(W/L)_1$ ratio and the saturation voltage is $V_{DSsat} = V_{GS} - V_{TH}$, comparable to a single transistor structure. The working principle of this structure lies in the use of different threshold voltages of the transistor ($V_{TH1} \neq V_{TH2}$), a not feasible requirement in standard low-cost CMOS technology.

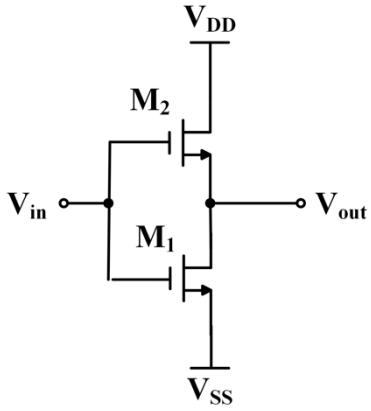


Fig. 5. The self-cascode structure.

1.3.3 Level shifter techniques

Dynamic voltage level shifter techniques represent a viable solution for low-voltage input signal circuits [7]. These techniques use resistors for shifting the input common-mode voltage to the operation region of the input differential pair of the MOS transistors. In this way, a sufficient transconductance g_m can be obtained in comparison with other low-voltage design techniques.

1.3.4 Bulk-driven MOS transistors

The MOS transistor is controlled by the potential applied at the gate terminal in a conventional approach. However, in a bulk-driven approach, the bulk terminal of the MOS transistor is used as an input terminal to control the drain current. The bulk-source voltage V_{BS} is used to modulate the current that flows through the device and it consequently introduces a body transconductance g_{mb}. Although the input signal is applied to the bulk terminal, the bias voltage is connected to the gate terminal in order to create a channel between source and drain terminals. If the voltage V_{GS} is kept constant, it's possible to modulate the inversion channel using the voltage applied to the bulk terminal. The bulk terminal used as an input terminal significantly reduces the input signal required to overcome the threshold voltage of the MOS transistor. The effect of the V_{BS} on the threshold voltage can be expressed as follows:

$$V_{TH} = V_{TH0} \pm \gamma\left(\sqrt{2|\Phi_F| - V_{BS}} - \sqrt{2|\Phi_F|}\right) \tag{8}$$

where γ is the technology-specific body factor and Φ_F is the technology-specific Fermi's potential.

By inspection of (8), it is apparent that any changes on V_{BS} result in a variation on V_{TH} which can be used to modify the inversion coefficient and finally, to control the MOS transistor drain current.

The properties of a bulk-driven MOS transistor can be analyzed by making a comparison between the conventional gate-driven (GD) and bulk-driven (BD) approaches on single stage common-source amplifiers (Fig. 6 and Fig. 7 respectively).

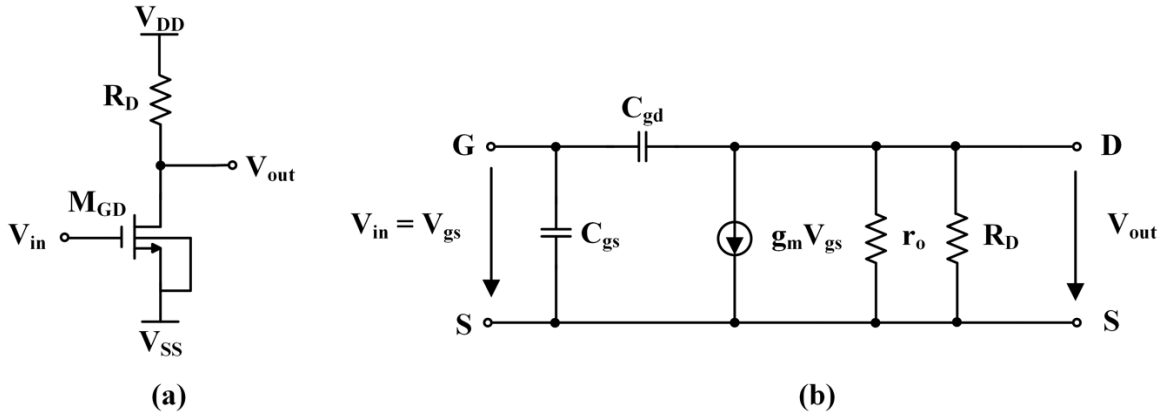


Fig. 6. Gate-driven single stage common-source amplifier. (a) Schematic diagram and (b) Small-signal model.

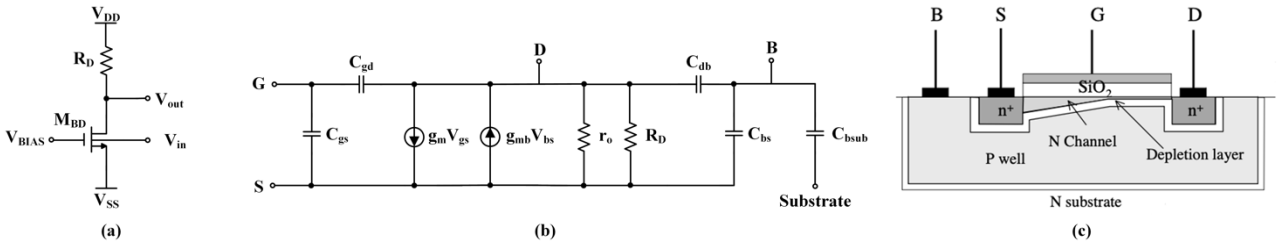


Fig. 7. Bulk-driven single stage common-source amplifier. (a) Schematic diagram and (b) Small-signal model (c) Cross-section.

It can be noted that the input capacitance in a BD single-stage amplifier is higher than in the GD approach as a result of the introduction of the parasitic capacitance C_{bsub} between bulk and substrate terminals. The input capacitance in GD amplifier depends on gate-source capacitance C_{gs} and gate-drain capacitance C_{gd} while in BD amplifier it depends on the combination between the bulk-source capacitance C_{bs}, bulk-drain capacitance C_{bd} and bulk-substrate capacitance C_{bsub}.

The transconductance of a conventional GD transistor operating in strong inversion region and in weak inversion region can be expressed by the following equation (9) and (10), respectively:

$$g_m = \beta \frac{W}{L} \cdot (V_{GS} - V_{TH}) \tag{9}$$

$$g_m = \frac{I_D}{nV_T} \tag{10}$$

The relationship between the transconductance of a GD transistor g_m and the transconductance of a BD transistor g_{mb} is given by (11) and (12):

$$g_{mb} = \frac{\gamma}{2\sqrt{2|\Phi_F| - V_{BS}}} \cdot g_m \tag{11}$$

$$g_{mb} = \frac{C_{btot}}{C_{gtot}} \cdot g_m \tag{12}$$

where C_{btot} and C_{gtot} are the total parasitic capacitance between bulk channel and gate channel, respectively. Finally, equation (13) allows to compare the transconductance achieved through GD and BD approaches. It can be noted that BD MOS transconductance is only 20 – 30 % of the GD MOS transconductance.

$$g_{mb} = (0.2 \div 0.3) \cdot g_m \tag{13}$$

To move forward the frequency analysis, firstly it is important to define the transition frequency of a GD transistor $f_{T,GD}$ as follows:

$$f_{T,GD} = \frac{g_m}{2\pi C_{gs}} \tag{14}$$

Fig. 8 shows the schematic diagram and the small signal model employed to investigate on the frequency performance of a BD transistor.

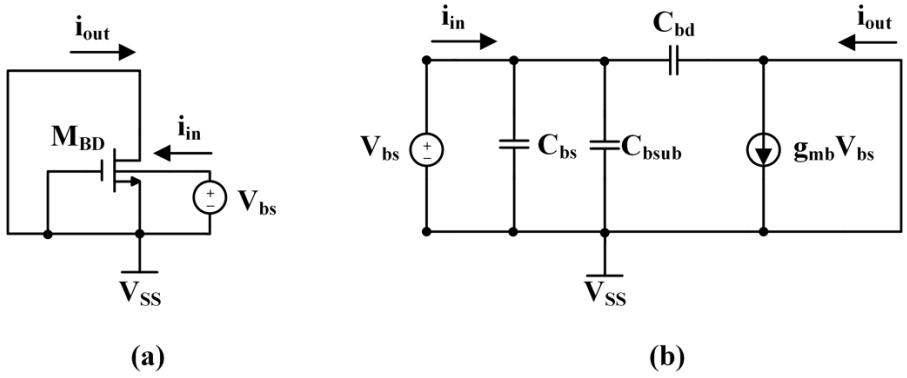


Fig. 8. Schematic diagram (a) and small signal model (b) for the BD frequency analysis.

By inspection of the small signal model, the transfer function in terms of the current gain (equation 15) of a BD transistor is obtained.

$$\frac{i_{out}}{i_n} = \frac{g_{mb} V_{bs}}{j\omega(C_{bs} + C_{bsub} + C_{bd}) \cdot V_{bs}} \approx \frac{g_{mb}}{j\omega(C_{bs} + C_{bsub} + C_{bd})} \tag{15}$$

Consequently, the transition frequency of the BD transistor can be expressed as follows:

$$f_{T,BD} = \frac{1}{2\pi} \cdot \omega_{T,BD} = \frac{g_{mb}}{2\pi(C_{bs} + C_{bsub} + C_{bd})} \approx (0.2 \div 0.3) \cdot f_{T,GD} \tag{16}$$

This means that the transition frequency of a BD MOS transistor is lower than that obtained by a GD MOS configuration.

To conclude, other important parameters to take into account in an amplifier analysis are the noise introduced by the active component and the small signal output resistance. The input referred noise of a GD transistor depends on the ratio between the current i_{ds} and the transconductance g_m, as can be seen from equation (17).

$$v_{noise}^2 = \frac{i_{ds}^2}{g_m^2} \tag{17}$$

On the other hand, the input referred noise of a BD transistor is expressed by the equation (18). This parameter is higher than in the GD configuration because of the lower transconductance g_{mb}.

$$v_{noise,BD}^2 = \left(\frac{g_m}{g_{mb}}\right)^2 \cdot v_{noise}^2 \tag{18}$$

Finally, the expression of the small-signal output resistance is the same for both GD and BD configuration, as can be seen from equation (19).

$$r_o = \frac{1}{\lambda I_{DS}} = \frac{V_A}{I_{DS}} \tag{19}$$

where V_A is the Early voltage and I_{DS} is the drain-source current flowing the MOS transistor.

The main disadvantages of the BD approach in comparison to the traditional GD ones are: (1) body transconductance g_{mb} lower than the gate-transconductance g_m which consequently leads to a reduced gain-bandwidth product, (2) a higher input capacitance, (3) an increased input noise, (4) the presence of the latch-up effect on MOS transistor in CMOS process. However, these drawbacks can be mitigated by the adoption of a lower value of the supply voltage below the threshold voltage of the PN junction of the MOS transistor.

Finally, the main advantages of a BD design technique include:

- The possibility to operate with a lower supply voltage.
- The reduced input voltage needed to overcome the transistor threshold voltage which leads to an increased voltage headroom suitable for low-voltage and rail-to-rail applications.
- The easy chance to be implemented in a standard CMOS technology [10].

1.3.5 Floating-gate MOS transistors

Floating-gate MOS transistors have been mainly used in digital EPROM or EEPROM in the past years. Only in the last decades, floating-gate technique has been involved also in analog circuits design such as amplifiers, D/A converters, analog trimming circuits and so on [9]. The layout, the schematic symbol and the equivalent circuit of a multi-input floating-gate MOS transistor are shown in Fig. 9. The floating-gate MOS transistor is quite equivalent to a conventional one except for the control mode of the gate voltage. In a conventional MOS transistor, the gate voltage V_G is directly applied to the gate terminal while in a floating-gate transistor, this voltage V_{FG} is applied to the gate terminal through a capacitance coupling.

The floating-gate voltage can be expressed as:

$$V_{FG} = \left(Q_{FG} + C_{FG,D}V_D + C_{FG,S}V_S + C_{FG,B}V_B + \sum_{i=1}^{n} C_{Gi}V_{Gi}\right)/C_{\Sigma} \tag{20}$$

where Q_{FG} is the static charge on the floating-gate and $C_{\Sigma} = C_{FG,D} + C_{FG,S} + C_{FG,B} + \sum_{i=1}^{n} C_{Gi}$ is the total capacitance seen at the floating-gate.

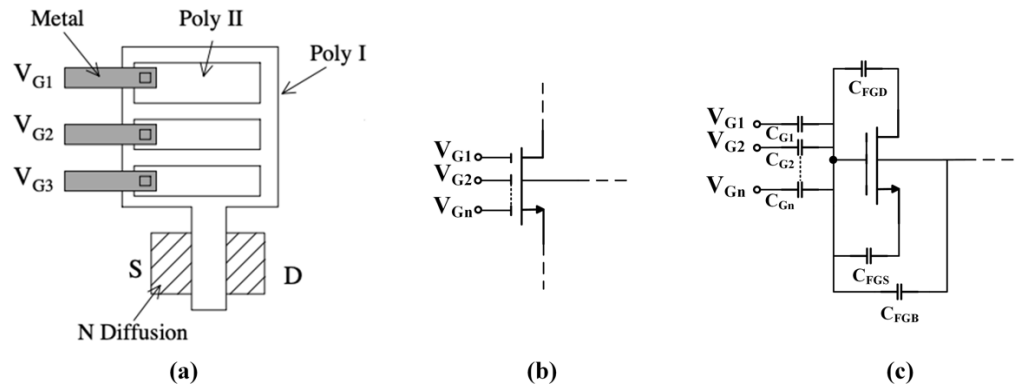


Fig. 9. Multi-input floating-gate MOS transistor: (a) layout, (b) schematic symbol, (c) equivalent circuit.

If the voltage $V_{FG\text{-}S}$ is set equal to V_{GS}, the drain current versus the gate-source voltage (I_D vs V_{GS}) characteristic achieved by a conventional MOS is similar to the one used by a floating-gate MOS. It is necessary to observe that the voltage V_{FG} is dependent on the drain voltage V_D due to the parasitic capacitance $C_{FG\text{-}D}$. Consequently, the output impedance of a floating-gate MOS transistor is degraded and lower to that achieved by a conventional MOS transistor one. The main feature of the floating-gate approach is to change the equivalent threshold voltage seen from the gate terminal by varying the level of the static charge Q_{FG} on the floating-gate. The static charge can be controlled in several ways like:

- ultra-violet light shining that causes a temporary conductivity of the isolation S_iO_2 layer and consequently the static charge can leak away.
- hot-electrons injection with a large programming current.
- Fowler- Nordheim (FN) tunnelling with a high programming voltage thus however the low-voltage applications are limited.

Under the assumption that the MOS transistors have both the same aspect ratio and the bias drain current, the bulk-driven and multi-input floating-gate transistors have the same drain current noise as a traditional MOS and a smaller equivalent transconductance thus resulting in a higher input referred noise voltage. However, it can be noted that floating gate techniques are becoming impractical in modern technologies due to the large gate leakage.

1.3.6 Dynamic-threshold MOS transistors

Dynamic-Threshold (DT) technique is derived from BD technique with only one simple difference in the gate biasing condition. DT transistor has the gate and bulk electrodes connected to each other while the biasing is realized dynamically. In this way, the potential of the conductive channel is controlled by both the gate and bulk terminals simultaneously thus resulting in a higher transconductance ($g_m + g_{mb}$) and a faster current transfer function [8]. The schematic and the small signal equivalent circuit of a DT MOS transistor are shown in Fig. 10 (a) and Fig. 10 (b), respectively.

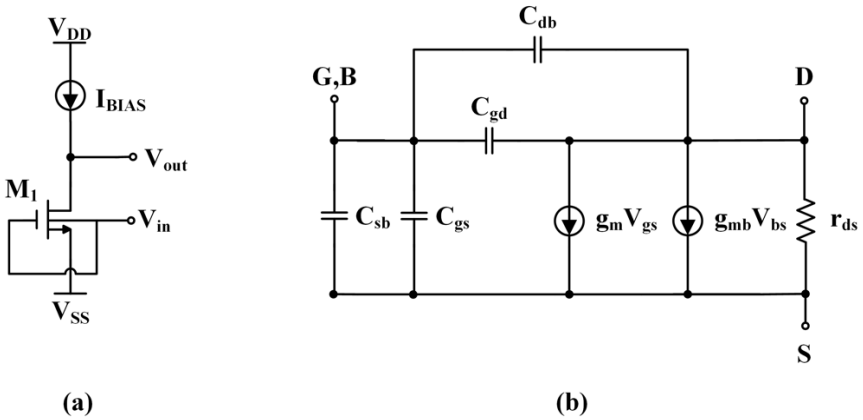


Fig. 10. DT MOS transistor: (a) schematic and (b) small-signal equivalent circuit.

The threshold voltage V_{TH} and the relationship between the transconductances g_m and g_{mb} have already been shown in equations (8), (11) and (12), respectively [8]. The main difference between DT and BD approach consists of the maximum input frequency which can be expressed as follows:

$$f_{T(DT)} = \frac{g_m + g_{mb}}{2\pi(C_{GD} + C_{BD} + C_{GS} + C_{BS})} \quad (21)$$

1.4 Comparison of Low-Voltage analog circuit design techniques

The main characteristics of the discussed low-voltage design techniques are summarized and compared in Table I. Although self-cascode, level shifter and floating-gate approaches represent good design options, their higher value reached by the power consumption is not suitable for ultra-low power applications.

Subthreshold approach represents the best way to achieve low power consumption by using standard CMOS technologies at the expense of a lower GBW value. The same performances can be also reached by a bulk-driven approach despite it required a triple-well technology.

TABLE I: Comparison of low-voltage design techniques.

Technique	Supply Voltage	Power Consumption	GBW	Technology
Subthreshold	$< V_{TN} + \lvert V_{TP} \rvert$	Low	Low	Standard
Self-cascode	$< V_{TN} + \lvert V_{TP} \rvert$	Medium	Medium	Multi-threshold
Level shifter	$< V_{TN} + \lvert V_{TP} \rvert$	Medium	High	Standard
Bulk-Driven	$< V_{TN} + \lvert V_{TP} \rvert$	Low	Low	Standard (triple-well)
Floating-gate	$< V_{TN} + \lvert V_{TP} \rvert$	High	Medium	2x Polysilicon
Dynamic-threshold	$< V_{TN} + \lvert V_{TP} \rvert$	Low	Medium	Standard (triple-well)

Chapter 2

Ultra-Low Power CMOS Analog Voltage References

2.1 Introduction to Analog Voltage References

The most widely used analog building blocks in an integrated circuit is the voltage reference. High-resolution analog-to-digital (A/D) and digital-to-analog (D/A) converters, smart sensors, battery management systems, measurement systems, and many other precise control systems require a precise reference voltage in their core to work properly. Therefore, the best performances achieved by an electronics system are strictly related to the accuracy with which the reference voltage is reached.

A voltage reference is a circuit that generates an exact output voltage which doesn't depends on the Process, supply Voltage and Temperature variations (PVT), the load current, and the passing time. It is essential not to confuse a voltage reference with a voltage regulator. Although both are used to precisely set the output voltage, a voltage regulator provides a higher output current than that of a voltage reference circuit. Consequently, a voltage regulator is less accurate than a voltage reference providing a higher output noise and not accurate stability over time. In fact, a voltage regulator requires a precisely voltage reference in its core. Different circuit topologies have been developed to provide an accurate reference voltage which are distinguished on how the reference voltage is set.

In the following paragraphs, an essential review on traditional topologies of voltage references will be carried out firstly taking into account some performance parameters introduced to precisely evaluate the accuracy with which the reference voltage is reached.

By considering the emerging low-power and low-voltage trend in the context of the voltage reference circuits, the analysis will be carried out analyzing the most efficient low-power voltage references taking from the state of art.

At the end, the aim of this research will be satisfied through the proposal of two low-power voltage reference architectures. An accurate analysis of the circuit topologies will be carried out also validated by exhaustive schematic and post-layout simulations and whenever possible experimental results. In conclusion, a needed comparison with the state of the art in this field will be made proving the goal of this research.

2.2 Performance Parameters of an Analog Voltage Reference

A wide variety of circuits require a fixed reference voltage to achieve the overall system best performances. The accuracy and the reliability at which the voltage reference is reached can be evaluated through some performance parameters and they are strictly related to the application in which the reference is placed. For example, an A/D converter require a reference voltage independent of the supply voltage variations to achieve a high conversion accuracy. In fact, the good accuracy of

a voltage reference is not only evaluated through the temperature compensation, but it also requires an exhaustive analysis on the stability of the refence voltage by varying the supply voltage, manufacturing and process variations, and load noise. Therefore, accurate reference circuits are guaranteed though the analysis of statical performances as well as dynamic performances. The static performances are related to the limited line regulation, load regulation, manufacturing and process variations resulting in variations on both the device characteristics and its main parameters, (mismatches and some second-order effects such as channel length modulations among others.). Moreover, the static performances have a great impact on the reference voltage accuracy which can be improved using several strategies including the most used that is known as trimming technique. On the other hand, to carry out a simplified discussion on the dynamic performances we have to consider the nominal reference voltage $V_{REF\ (nom)}$, which is the desired voltage at the nominal operating conditions. The nominal operating condition is reached by setting a fixed temperature (in this case room temperature) and a fixed supply voltage that in the nominal condition can be expressed as $V_{DD(nom)}$. The dynamic performances of a voltage reference can be evaluated though the following parameters: (1) the Temperature Coefficient (TC) within a temperature range in which the circuit operates, (2) the Line Sensitivity (LS) of the reference voltage within a input voltage range in which the circuit operates, (3) the PSRR under a maximum input ripple, and (4) the peak-to-peak output noise of the reference voltage over the operating frequency spectrum.

Finally, all the performance parameters are based on the definition of sensitivity parameter. The parameter S_x^y measures the sensitivity of the parameter y with respect to a change in parameter x as follows:

$$S_x^y = \lim_{\Delta x \to 0} \left(\frac{\Delta y / y}{\Delta x / x} \right) = \frac{\partial y}{\partial x} \frac{x}{y} \tag{22}$$

where Δx indicates how much the parameter x change with respect to the nominal value and Δy indicates how much the parameter y change with respect to the nominal value.

2.2.1 Line regulation

The line regulation indicates the variations of the nominal reference voltage $V_{REF\ (nom)}$ with respect to a variation on the input supply voltage V_{IN} at the nominal temperature. The line regulation is defined according to equation (23), and it is specified as $[\mu V/V]$ or as a percentage.

$$S_{LR,T\ (nom)} = \frac{\Delta V_{REF,T\ (nom)}(\Delta V_{IN})}{\Delta V_{IN}} \tag{23}$$

where $\Delta V_{REF,T\ (nom)}(\Delta V_{IN})$ is the variation of the reference voltage within the input voltage range $\left[V_{IN\ (\min)}, V_{IN\ (\max)}\right]$ and $\Delta V_{IN} = V_{IN\ (\max)} - V_{IN\ (\min)}$.

The test-bench used to evaluate the line regulation of a voltage reference circuit is shown in Fig. 11. The steady-state output current, the output capacitive load and the output resistive load are indicated with I_{OUT}, C_{LOAD} and R_{LOAD}, respectively where $I_{OUT} = V_{REF\ (nom)} / R_{LOAD}$. The output voltage of the reference circuit $V_{REF\ (nom)}$ is evaluated by varying the input voltage V_{IN} from 0 V to the maximum value $V_{IN\ (max)}$ for a fixed steady-state output current and the output capacitive load at nominal temperature.

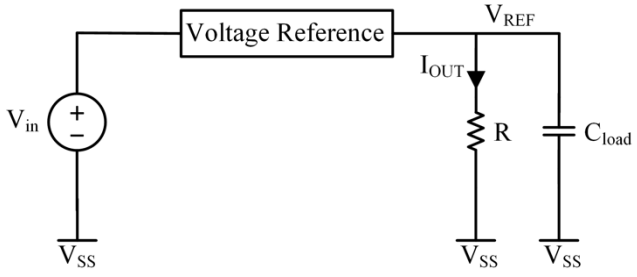


Fig. 11. Test-bench for the evaluation of the line sensitivity of a voltage reference circuit.

A typical voltage reference dependence on the input voltage is shown in Fig. 12. The desired reference voltage is defined taking also into account some tolerance reflecting the inaccuracy of real measurement. Consequently, the output of the voltage reference is redefined as $V_{REF\ (nom)} \pm \frac{\Delta V_{REF}}{2}$ at nominal temperature $T_{(nom)}$. The operating range defined as the input voltage range has a great impact on the reference voltage measurement and hence is defined during the line regulation evaluation. Therefore, $V_{IN\ (min)}$ represent the minimum value of the input voltage in which the reference circuit works. Another important parameter is the dropout voltage V_{DROP} which consists in the difference between the input voltage and the output voltage of the reference circuit. The $V_{DROP\ (min)}$ which is the difference between the reference voltage $V_{REF\ (nom)}$ and minimum operating voltage $V_{IN\ (min)}$ ($V_{DROP\ (min)} = V_{IN\ (min)} - V_{REF\ (nom)}$) can be also introduced to specify, for example, the minimum operating voltage of a given reference circuit.

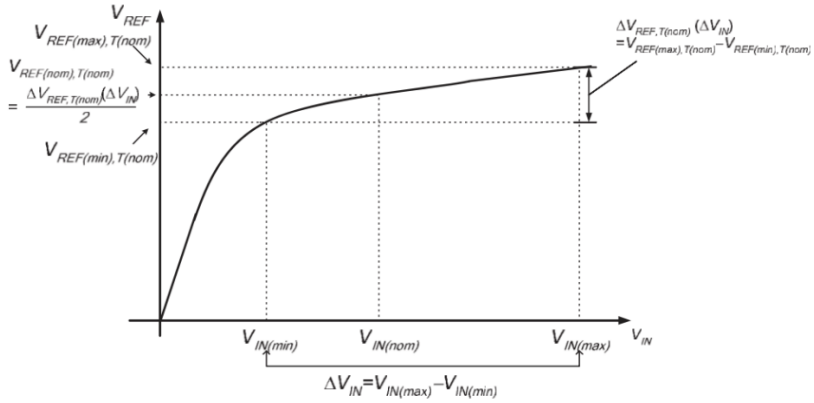


Fig. 12. Typical reference voltage V_{REF} dependence on the input voltage V_{IN} at room temperature.

2.2.2 Temperature Coefficient

Temperature variation has a great impact on the physical characteristics of the device and consequently this creates a temperature dependence on the output voltage in a reference circuit. The temperature sensitivity S_{TC} in a circuit can be expressed by the Temperature Coefficient once the operating temperature range $[T_{(\min)}, T_{(\max)}]$ in which the reference voltage drift has been set. The expression of the TC is shown in equation (24), and it is specified as (ppm/°C).

$$TC = S_{TC,V_{IN\ (nom)}} = \frac{\left(V_{REF\ (\max),V_{IN\ (nom)}} - V_{REF\ (\min),V_{IN\ (nom)}}\right)}{(T_{(\max)} - T_{(\min)}) \times V_{REF\ (nom)}} \times 10^6 = \frac{\Delta V_{REF,V_{IN\ (nom)}}(\Delta T)}{\Delta T \times V_{REF\ (nom)}} \times 10^6 \quad (24)$$

Where $\Delta V_{REF,V_{IN\ (nom)}}(\Delta T)$ is the reference voltage variation within the temperature range $[T_{(\min)}, T_{(\max)}]$ and $\Delta T = T_{(\max)} - T_{(\min)}$.

The test-bench required for the temperature coefficient evaluation can be the same already shown in Fig.11 for the line regulation evaluation. For a fixed nominal input voltage $V_{in\ (nom)}$, a typical reference voltage dependence on the temperature in the operating range $[T_{(\min)}, T_{(\max)}]$ is shown in Fig. 13.

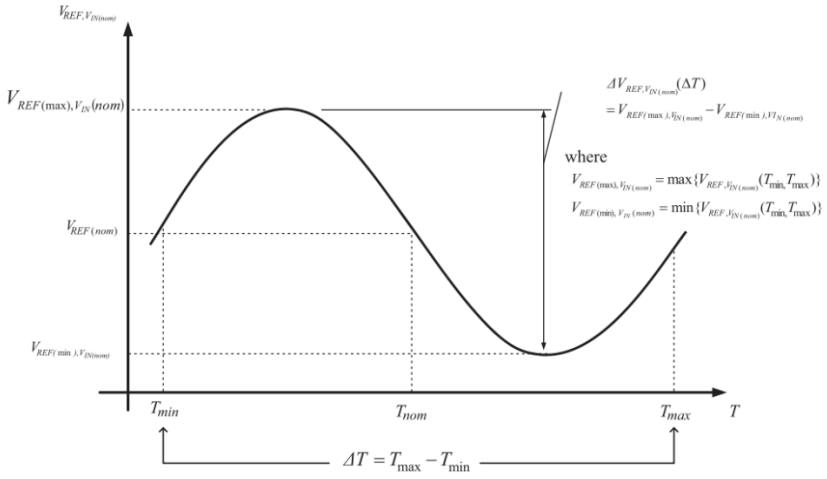


Fig. 13. Typical reference voltage V_{REF} dependence on the temperature at nominal input voltage V_{IN}.

The temperature dependence is carried out by placing the chip under measurement in a hot/cold bath or a thermal chamber while the input and output source are kept out and maintained at the nominal conditions. The only analysis of the curvature of the reference voltage can sometimes be misleading and it makes difficult the comparison of the temperature dependence between different reference topologies. With the purpose of a fine comparison, firstly it is recommended to choose the temperature range suitable for the specific application and after that center the reference voltage at a certain point stated as $V_{REF,V_{IN\,(nom)}}(T)$ equal to the average between $V_{REF\,(\min),V_{IN\,(nom)}}$ and $V_{REF\,(\max),V_{IN\,(nom)}}$.

2.2.3 Power Supply Rejection Ratio

The high frequency noise due to the signal coupling, power surge, feedback among others hurts the silicon power rail in the real applications. The ability of the reference voltage circuit to reject the noise and the other undesirable signals at a certain frequency on the power rail shall be determined by the Power Supply Rejection Ratio (PSRR). This parameter proofs the robustness of a reference voltage, and its frequency dependence can be expressed as follows:

$$PSRR\,(f) = S_{PSRR,f} = 20\log\frac{V_{REF,AC}(f)}{V_{IN,AC}(f)}\ [dB] \tag{25}$$

The PSRR over a wide range of frequency can be used to describe the reference voltage variations corrupted by the supply noise.

2.2.4 Quiescent current

The quiescent current I_q is an alternative way to indicate the supply current and it represents the current required by the voltage reference circuit to operate at steady-state and without resistive load. Under the nominal condition for the input voltage $V_{IN\,(nom)}$ and temperature $T_{(nom)}$, the quiescent current is indicated as $I_{q\,(nom)}$ (with the load resistance ideally equal to infinite such as the load current is zero). Consequently, the steady-state power consumption of the reference circuit is given by the product between the input supply voltage and the quiescent current as follows: $V_{IN\,(nom)} \times I_{q\,(nom)}$.

A low quiescent current in a voltage reference is advantageous for two reasons: (1) it implies high-power efficiency and long working time of the voltage reference circuit that can be useful in application with power supply restriction such as battery-powered systems; (2) it leads a small power dissipation resulting in a small self-heating effect which helps to maintain the accuracy and the stability of the output voltage in a voltage reference circuit.

2.2.5 Output noise

The output noise is another frequency dependent parameter in a voltage reference circuit. It is usually specified as the peak-to-peak voltage at low-frequency bandwidth (from 0.1 Hz to 10 Hz) which is particularly useful for low-frequency systems such as voltage references. The output noise can be also specified at higher frequency (from 10 Hz to 20 kHz) to investigate the broadband noise known as thermal noise or "*white noise*" which is useful for the noise consideration in A/D and D/A converters. The output noise is measured with respect to its root mean square (RMS) value and under the assumption of truly random noise, the peak-to-peak noise voltage is expressed by multiplying the RMS value by 6. In addition, the best way to define the high frequency noise is given by the inspection of the noise voltage spectral density behavior in frequency. In this way, it is possible to calculate the noise according to the desired bandwidth specific to the system application.

2.2.6 Design considerations

Design considerations in a voltage reference circuit shall be taken into account together with the already discussed performance parameters. In fact, these considerations are particularly important since they have a direct impact on the performance parameters. These remarks concern the circuit size, power dissipation, device mismatch and trimming on the output voltage among others. These considerations have a great impact on the final product and shall be considered during the design phase of the reference circuit. Circuit sizing and power consumption are design constrains for target application and they also affect performance parameters such as output noise. Indeed, the thermal noise is strictly dependent both on the quiescent current and on the overall sizing of the devices being the *1/f* noise inversely proportional to the sum of the square root of the MOS's gate are in the circuit.

Additionally, devices are affected by process variations which consequently lead to parameter variations and device mismatches. A good reference circuit should be insensitive to device mismatches in order to provide a reference voltage at the desired operating point. At this purpose, a trimming on the device parameters can be included to achieve this goal. Furthermore, the design of a high-performance voltage reference needs to consider the effect of the component mismatches on the output voltage accuracy. Hence, once again the circuit should include a trimming network impervious to temperature and stability variations. On the other side, trimming strategy requires a large silicon area occupation, thus increasing the intrinsic silicon cost as well as the manufacturing cost due to the added trimming step in post-fabrication process. Consequently, larger area occupations result in an increased noise and other performance degradation.

Although the market decision determines the final price of the product, a trade-off between silicon area occupation and performance parameters is recommended during the design phase [11].

2.3 Traditional Analog Voltage Reference Topologies

As it already stated, the principal purpose of a voltage reference circuit is to generate a fixed voltage V_{REF} independent of PVT variations. Sometimes, the generate output voltage in a reference circuit changes according to the temperature. At this purpose, a voltage reference in which the V_{REF} increases with temperature and at the same time is proportional to absolute temperature is stated PTAT. In contrast, a voltage reference in which the V_{REF} decrease increasing temperature is stated as complementary to absolute temperature or CTAT. Both PTAT and CTAT voltage references require the use of the parasitic diodes which arises with the p-n junction in the CMOS process. Anyway, unfortunately their electrical characteristic cannot be controlled during the manufacturing process. Being the accuracy of the reference voltage very important, it is recommended the design of a reference voltage by using only MOS transistors or at the most MOS transistors together with resistors. Furthermore, PTAT and CTAT behavior can be used in conjunction to design a voltage.

With a view to make a brief comparison between the traditional voltage reference topologies it is possible to divide them into different categories as follows: (1) parasitic diode-based voltage references, (2) MOSFET-Resistor voltage references and (3) bandgap voltage references.

2.3.1 Parasitic Diode-Based Voltage Reference

Parasitic diode is naturally created in a CMOS process where it is formed between the p+ implant and the n-well. Otherwise, in several applications the parasitic vertical PNP bipolar device is created between p+, n-well and p-substrate generates a current to be injected into the substrate. For this purpose, guard rings surrounding p+, n-well and p-substrate are placed to collect this current by ensuring that the injected carriers are collected without causing substrate current to flow elsewhere in the chip. Another practical parasitic diode available in CMOS process creates the lateral bipolar PNP junction transistor as shown in Fig. 14. In this case, it is necessary to consider the orientation of the device as follows: the p+ forms the emitter/collector of the device while the n-well constitutes the base. Being the vertical PNP still present, a significant portion of the emitter current of this device will flow into the substrate.

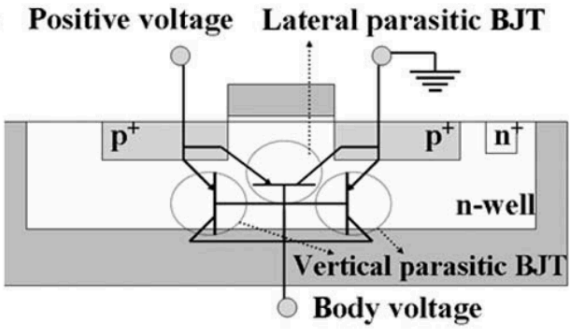


Fig. 14. A lateral and vertical parasitic bipolar junction transistor.

To better understand the behavior of the parasitic diode in CMOS process in terms of voltage to current relationship, it is necessary to firstly consider a general diode model. Indeed, the current flowing through a forward-biased diode can be expressed as follows:

$$I_D = I_S \cdot e^{V_D/nV_T} \tag{26}$$

where V_D is the voltage across the diode, n is the emission coefficient and I_S is the inversion saturation current.

The temperature dependence of the diode voltage can be evaluated by taking out the expression of the diode voltage from (26) and by deriving it with respect to the temperature. In the diode case, the voltage changes are complementary to the absolute temperature or CTAT.

2.3.2 MOSFET-Resistor Voltage Reference

A voltage divider formed by only two resistors is shown in Fig. 15 (a). This simple architecture has the advantage of temperature and process insensitivity since that a change in the sheet resistance has no impact on the voltage division. The main limitation of this topology lies in larger resistors required to reduce the power dissipation (or to reduce the current flowing into the resistors). Large resistors result in large area occupation making this type of voltage divider not practical in many applications.

Therefore, a solution to derive a reference voltage from the supply voltage can be given by combining the resistor together with the MOSFET transistor, as shown in Fig. 15 (b). A voltage divider like this can be used to bias the current in some current mirror topologies. The reference voltage in a MOSFET-resistor divider is equal to the V_{GS} of the MOS device. By inspection of the circuit in Fig. 15 (b) it is possible to write the drain current flowing into the MOS transistor (equation 27) and consequently the expression of the reference voltage (equation 28).

$$I_D = \frac{V_{DD}-V_{REF}}{R} = \frac{\mu C_{OX}\frac{W}{L}}{2}(V_{REF}-V_{TH})^2 \tag{27}$$

$$V_{REF} = V_{TH} + \sqrt{\frac{2I_D}{\mu C_{OX}\frac{W}{L}}} = V_{TH} + \sqrt{\frac{2(V_{DD}-V_{REF})}{R\mu C_{OX}\frac{W}{L}}} \tag{28}$$

If the chosen value of the V_{REF} is close to the threshold voltage V_{TH}, the reference voltage becomes insensitive to the supply voltage variations. On the other hand, the temperature behavior follows the threshold voltage, and the temperature coefficient can be extracted from equation (29).

$$TC = \frac{1}{V_{REF}} \cdot \frac{\partial V_{REF}}{\partial T} \tag{29}$$

Finally, a voltage divider based on a NMOS and PMOS transistors which leads to the great advantage of reduced area occupation is shown in Fig. 15 (c). Being the drain current of M_1 equal to the drain current of M_2, the reference voltage is related to the voltages at the gate of both transistors as follows.

$$V_{REF} = \frac{V_{DD} - V_{THP} + \sqrt{\frac{\mu_n C_{OX}\left(\frac{W}{L}\right)_1}{\mu_p C_{OX}\left(\frac{W}{L}\right)_2}} \cdot V_{THN}}{\sqrt{\frac{\mu_n C_{OX}\left(\frac{W}{L}\right)_1}{\mu_p C_{OX}\left(\frac{W}{L}\right)_2}} + 1} \tag{30}$$

where μ_n and μ_p are the electron mobility in the NMOS transistor and in the PMOS transistor respectively, and V_{THN} and V_{THP} are the threshold voltages in the NMOS transistor and in the PMOS transistor respectively.

Once again, the temperature coefficient can be expressed by deriving the reference voltage with respect to the temperature as shown in equation (29). Consequently, once the reference voltage is fixed, a zero temperature coefficient can be obtained setting the TC's expression equal to zero [12].

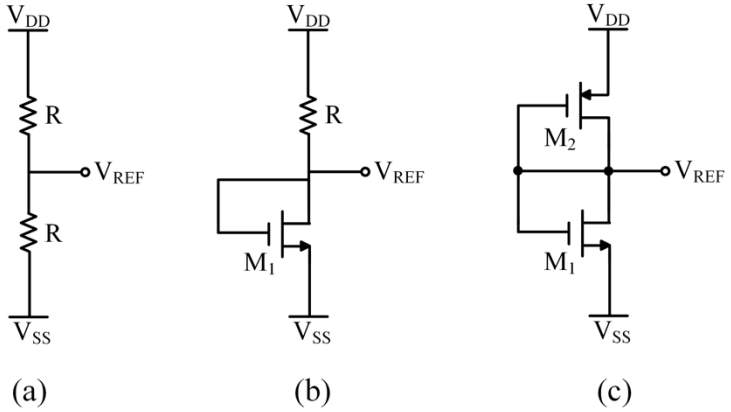


Fig. 15. Voltage dividers in CMOS technology: (a) resistor-only, (b) MOSFET-resistor and (c) MOSFET-only references

2.3.3 Bandgap Voltage Reference

The adjective bandgap has its roots in the physical nature of the Silicon (Si). A brief analysis regards the diagram of energy bands of a semiconductor is necessary to better understand the physical phenomenon. As illustrated in Fig. 16, the energy level E_C indicates the lower edge of the conduction band while the energy level E_V indicates the upper edge of the valence band. The gap between these two levels constitutes the bandgap energy E_g which can be expressed as a function of temperature as follows:

$$E_g(T) = E_g(0) - \frac{\alpha T^2}{T + \beta} \tag{31}$$

where $E_g(0)$, α, β are parameters related to the considered semiconductor.

In other words, the results of the expression of the bandgap energy indicates the value of the energy which the electrons should have to overcome the energy gap and transit from the valence band to the conduction band. Furthermore, by inspection of equation (31), it can be noted that the bandgap energy decreases with increasing the temperature.

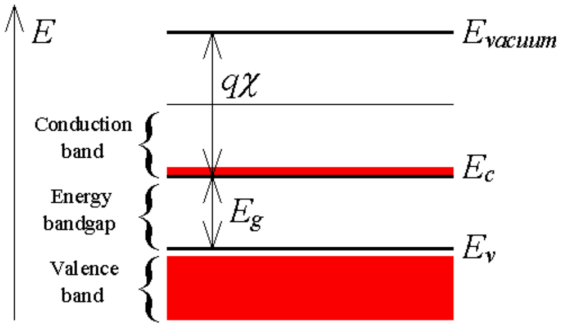


Fig. 16. Diagram of energy bands of a semiconductor

Under this premise, the idea behind the bandgap voltage reference topology lies in the mutual compensation of a voltage/current PTAT term and a CTAT voltage/current term with the aim to achieve a reference voltage with zero temperature coefficient. Temperature compensation can be reached by a simple weighted sum between these two voltages as follows:

$$V_{REF}(T) = m_1 V_{PTAT}(T) + m_2 V_{CTAT}(T) \tag{32}$$

Consequently, the temperature compensation described by equation (33) and shown in Fig. 17, can be achieved by deriving the reference voltage expressed above with respect to the temperature.

$$\frac{\partial V_{sum}(T)}{\partial T} = m_1 \frac{\partial V_{PTAT}(T)}{\partial T} + m_2 \frac{\partial V_{CTAT}(T)}{\partial T} = 0 \tag{33}$$

A zero TC is obtained by setting $\frac{\partial V_{PTAT}(T)}{\partial T} > 0$ and $\frac{\partial V_{CTAT}(T)}{\partial T} < 0$, and by choosing an appropriate value of m_1 and m_2.

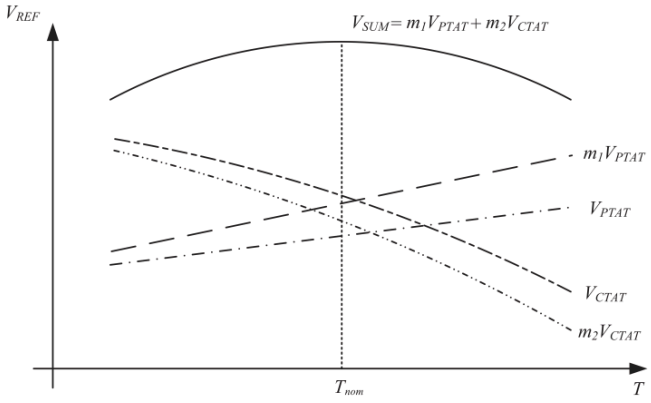


Fig. 17. Temperature compensation of a bandgap voltage reference

A bandgap voltage reference in which the output voltage is described by equation (32) is known as first order compensation reference circuit. This means that a small temperature coefficient ideally close to zero over a wide range of temperature can be achieved by compensating the nonlinear terms of the PTAT and CTAT voltages. However, the associated error between these two nonlinear voltages give rise an error known as *curvature error*. Therefore, a high order compensation method should be added to proper compensate temperature variations. Besides the curvature error, parameter variations in the devices affects the accuracy of the voltage reference and consequently should be take them into account during the design with devices matching, proper layout technique, and post-processing trimming technique.

One of the first bandgap voltage reference circuit implemented by using the conventional junction isolated bipolar technology was proposed by Robert Widlar in 1971 [13]. This circuit takes the invertor's name, and it generates a 1 V reference voltage with a low stable temperature coefficient.

Furthermore, the most well-known traditional bandgap voltage references have been proposed by Brokaw [14], Kujik [15] and Banba [16].

2.4 Low-Voltage and Low-Current Analog Voltage References State of Art

In the recent years the main trend in the integrated circuit fabrication has been focused both on the reduced silicon area occupation and on the reduced power consumption. Smaller transistors dimension results in low parasitic capacitances which allow to increase speed and decrease power consumption. At the same times, the circuit functionality for the same substrate area increases by reducing the devices size. On the other hand, although the low operating voltage is certainly a way to reduce the power consumption it involves an increased electric field and a reduced breakdown voltage in the transistors. Moreover, the consequences of the voltage downscaling are exacerbated in small devices where the doping profile are quite high.

All these considerations must be considered during the low-power circuit design thus increasing the circuit complexity. Therefore, the design of a low-power voltage reference becomes very challenging since low operating voltage forces two constrains. The first one is related to the value of the output voltage of the reference circuit which can be lower than the supply voltage. This becomes really challenging when the supply voltage is lower than 1 V that means to achieve an output of a reference circuit below to this magnitude. To give an example, traditional bandgap voltage references typically provide an output voltage around 1.2 V and consequently require a supply voltage higher than this value. A way to achieve low value of reference voltage can be given by the use of nanotechnologies together with resistive subdivision methods with the disadvantages of the increased current consumption [17]. Alternatively, voltage references based on the difference between the MOS transistor's threshold voltages have been exploited which however require an additional fabrication step in a standard CMOS technology. The second constrain is related to the ability of the reference circuit to work properly with a low supply voltage. Consequently, these restrictions make the traditional voltage reference topologies not suitable both to low-voltage operation and to generate low value of the reference voltage [11]. Furthermore, traditional bandgap voltage references are not suitable for low-power applications for two reasons. Firstly, large resistors are required to achieve low biasing current thus resulting in large silicon area occupation. Secondly, the diodes used to produce CTAT and PTAT currents require a voltage around 700 mV to turn-on the p-n junction thus severely limiting the minimum supply voltage.

Several low-current and low-voltage voltage references have been proposed in literature with the aim to overcome the restrictions given by the traditional approaches. A brief analysis of low-power voltage reference taken from the state of art can be carried out by dividing the approaches with which the reference voltage has been achieved as follows: (1) voltage references based on MOS transistors, (2) voltage references based on MOS and BJT transistors and (3) voltage references based on MOS transistors together with resistors.

MOS-based voltage references can be easily implemented with a standard CMOS technology making the voltage reference integration possible. By the way, the complete absence of bipolar transistors and resistors allow to further reduce the power consumption maintaining little the silicon area occupation. Consequently, MOS-based voltage reference has become particularly suitable for biomedical applications such as implantable devices which require both small size and small power consumption. Long lifetime is also required in IoT and energy harvesting applications in which the small power consumption is mandatory due to the small or even non-existent battery. Among different approaches, the most promising way to implement voltage references besides in the adoption of MOS transistors operating in subthreshold (weak and strong inversion) region. This approach allows to achieve power consumption in picowatts or nanowatts order of magnitude while the supply voltage can be reduced below 1 V. On the other hand, subthreshold approach has one disadvantage due to the

exponential relationship between drain current and threshold voltage in subthreshold region thus resulting in a higher process sensitivity that represent the most important process-dependent parameter. Moreover, low-power voltage reference topologies which exploits the operation in subthreshold region combined with other design techniques have been proposed in literature. One of the most important approach have been exploited in [18]–[23] where MOS-based reference circuit in which the reference voltage is based on the difference between the threshold voltages of the MOS transistor are used to achieve a CTAT and PTAT reference voltage with a low TC. Unfortunately, subthreshold approach results in a higher threshold voltage variation thus leading a higher sensitivity across process corners. For this reason, trimming strategies need to be added with the aim to achieve high-precision circuit by reducing the process corner variations. Additionally, different body-bias voltage though current trimming has been exploited in [24] to dynamically control the threshold voltage of the transistor resulting in a low-power MOS-based voltage reference insensitive to process variation without adopting a traditional trimming strategy. Another trimming-less voltage reference which exploits body biasing technique to compensate voltage and temperature fluctuations has been proposed in [25]. Finally other approaches to achieve low power consumption have been proposed in [26]–[29] where different design approaches MOS transistor based allow to avoid the presence of resistors and the nano-ampere operation. It is evident that CMOS-based reference circuit in which the reference voltage is obtained by the difference between MOS threshold voltages are strongly affected by process variations and consequently process compensation schemes must be added to the reference circuit. An alternative approach to overcome this limitation lies in hybrid architecture composed of BJT and MOS transistors to produce a reference voltage based on the difference between both bandgap and threshold voltage. Voltage reference based on the hybrid approach have been proposed in literature [30]–[32] in which BJT are used to both create a CTAT and process insensitive reference voltage while MOS transistors are used to create the PTAT and temperature insensitive reference voltage. Finally, a reference voltage based on MOS transistors in which the current generator section contains resistors has been proposed in [33]. The temperature independence is reached by a temperature-insensitive reference voltage divided by temperature-insensitive resistors thus resulting in a reference circuit with small TC with low area occupation.

Table II summarized the main performance parameters of the low-power voltage references taken by the state of art with the aim to make a comparison between the proposed solutions. As can be seen by inspection of Table II, the smallest power consumption of 2.2 pW is achieved by the MOS-based solution proposed in [20] while the smallest temperature coefficient TC of 7 ppm/°C and line sensitivity of 0.002 %/V are achieved by [26].

TABLE II: Comparison between low-voltage low-power voltage references taken from the state of art.

Reference	[23]	[18]	[20]	[19]	[21]	[22]	[24]	[25]	[29]	[26]	[27]	[28]	[30]	[31]	[32]	[33]
Year	2007	2011	2012	2013	2013	2018	2015	2021	2006	2009	2012	2018	2015	2019	2019	2019
Type	MOS (VTH difference)	MOS (VTH difference)	MOS (VTH difference)	MOS (VTH difference)	MOS (VTH difference)	MOS (VTH difference)	MOS (bulk-driven)	MOS (body-biased)	MOS (other)	MOS (other)	MOS (other)	MOS (other)	MOS+BJT	MOS+BJT	MOS+BJT	MOS+RES
Technology (nm)	350	180	130	180	180	180	180	180	350	350	90	180	130	180	180	180
VDD (V)	0.9 to 4	0.45 to 2	0.5 to 3	0.6 to 1.8	0.45 to 1.8	0.6 to 2	0.45 to 1.8	0.25 to 1.8	1.5 to 4.3	1.4 to 3	1.6 to 3.6	0.45 to 2.4	0.9 to 1.2	1 to 1.8	0.9 to 3.3	0.7 to 2
Current consumption (nA)	40@0.9V 55@4V	7@0.45V 8@1.8V	0.0044@0.5V	37@0.6V 37@1.8V	0.089@0.45V 0.1@1.8V	50.8@0.6V	32@0.45V	0.02@0.25V 0.02@1.8V	80@1.5V 110@4.3V	36@1.4V	68@1.6V 173@3.6V	7@2.4V	39@0.9V	0.192@1V	0.035@0.9V 0.041@3.3V	40@0.7V
Power (nW)	36@0.6V 220@4V	3.15@0.45V 14.4@1.8V	0.0022@0.5V	22.2@0.6V 22.2@1.8V	0.040@0.45V 0.18@1.8V	30.5@0.6V	14.4@0.45V	0.005@0.25V 0.042@1.8V	120@1.5V 473@4.3V	54@1.4V	109@1.6V 623@3.6V	16.8@2.4V	35@0.9V	0.192@1V	0.0314@0.9V 0.134@3.3V	28@0.7V
Vref (mV)	670	263.5	176.8	259	275.4	218.3	118.5	91.4	891.1	754	771	263.5	559	693	740	368
Temperature range (°C)	[0÷80]	[0÷125]	[−20÷80]	[0÷125]	[0÷120]	[−20÷125]	[−40÷125]	[0÷120]	[0÷80]	[−20÷80]	[−40÷125]	[0÷125]	[0÷125]	[−20÷100]	[0÷170]	[−40÷125]
TC (ppm/°C)	10	142	124	462	105.4	23.5	63.6	265	12	7	7.5	142	83	33	27	43.1
Line sensitivity (%/V)	0.27	0.44	0.033	0.065	0.46	0.4	8.77	0.16	0.46	0.002	1.65	0.44	1.33	0.02	0.27	0.027
PSRR (dB)	−47@100Hz −40@10kHz	−45@100Hz −12@10MHz*	−53@100Hz −62@10MHz	−44@100Hz* −43.3@10MHz*	−48@100Hz −29.2@10kHz	−42.4@1kHz −42.3@10MHz	−44.2@100Hz	−70@100Hz	−59@100Hz −52@10MHz	−45@100Hz	--	--	−41@100Hz*	−55@100Hz	–	−59@10Hz −39@1MHz
Die Area (mm2)	0.045	0.043	0.00135	0.0298	0.018	0.075	0.012	0.0022	0.015	0.055	0.03	0.043	0.0022	0.0045	0.0076	0.055

By inspection of Fig. 18 that shows the area occupation as a function of the minimum power consumption, it is apparent that the minimum achieved area occupation (that is 0.00135 mm^2) with the smallest power consumption (2.2 pW) is given by [20]. Anyway, generally a good compromise between these two parameters is achieved by hybrid MOS and BJT approach while as expected the addiction of resistors increase the area occupation.

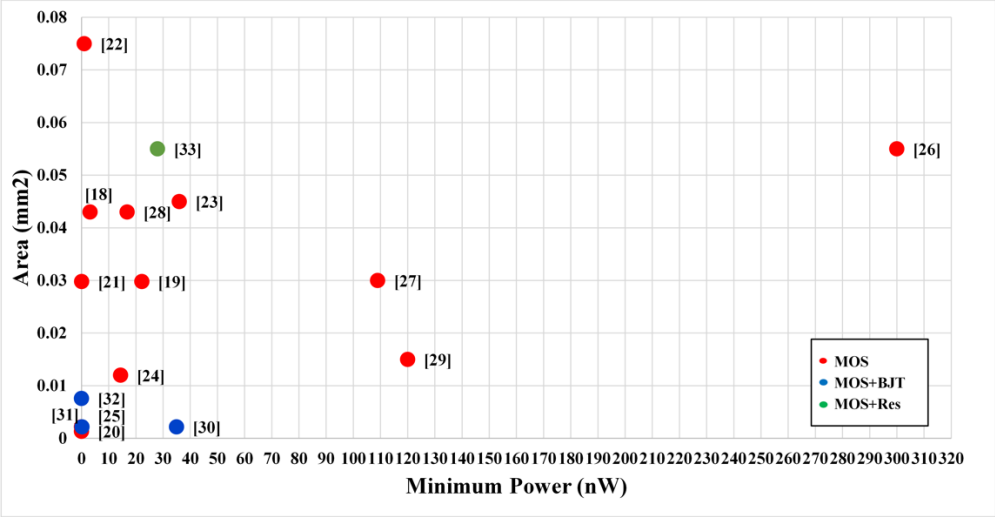


Fig. 18. Voltage reference area occupation as a function of the minimum power consumption.

Minimum supply voltage V_{DD} as a function of the minimum power consumption is shown in Fig. 19 proving that MOS-based voltage references allow to achieve the minimum power consumption thanks to the ability to reach the minimum supply voltage. It can be noted that the lowest supply voltage value of 0.25 V is reached by the MOS-based voltage reference proposed in [25] which combine subthreshold region with body-driven approach thus resulting in the lowest power consumption value.

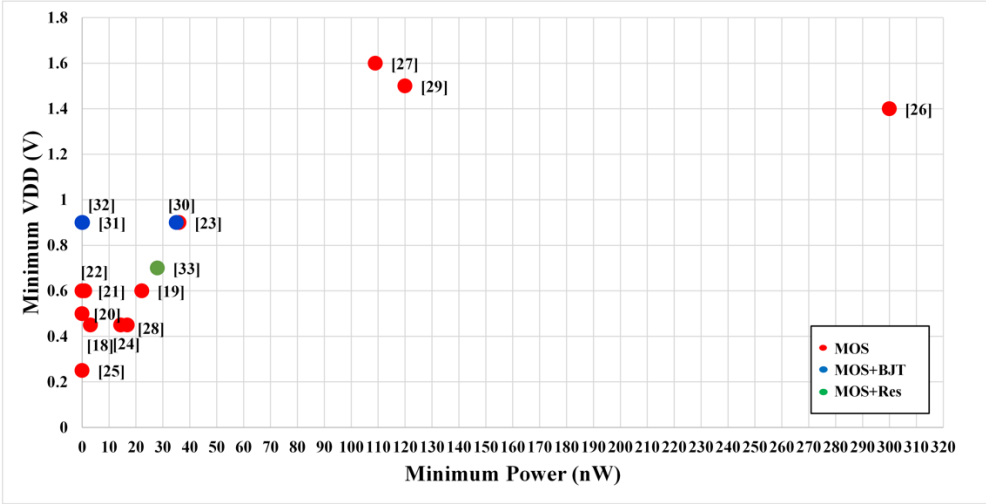


Fig. 19. Voltage reference minimum supply voltage V_{DD} as a function of the minimum power consumption.

Two of the main voltage reference performance parameters are the Temperature Coefficient TC and the line sensitivity which are shown in Fig. 20 and Fig. 21 as a function of the minimum power consumption. The best trade-off between TC and power consumption is reached by the MOS-based reference proposed in [23] in which a TC of 10 ppm/°C is reached with only 36 nW of power consumption. On the other hand, the best trade-off between line sensitivity and power consumption

is reached by the MOS-based reference proposed in [20] where a line sensitivity of 0.033 %/V is achieved with 0.0022 nW of power consumption.

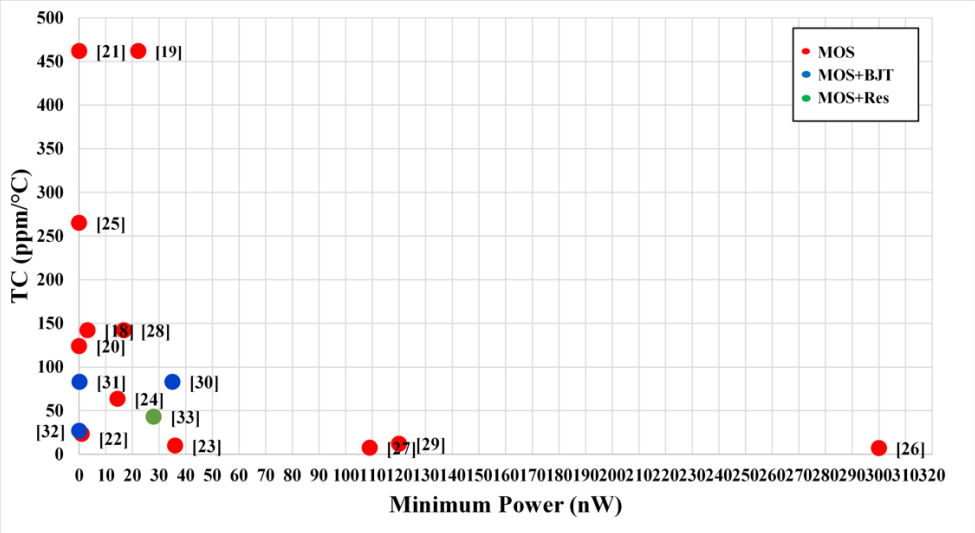


Fig. 20. Temperature Coefficient TC as a function of the minimum power consumption.

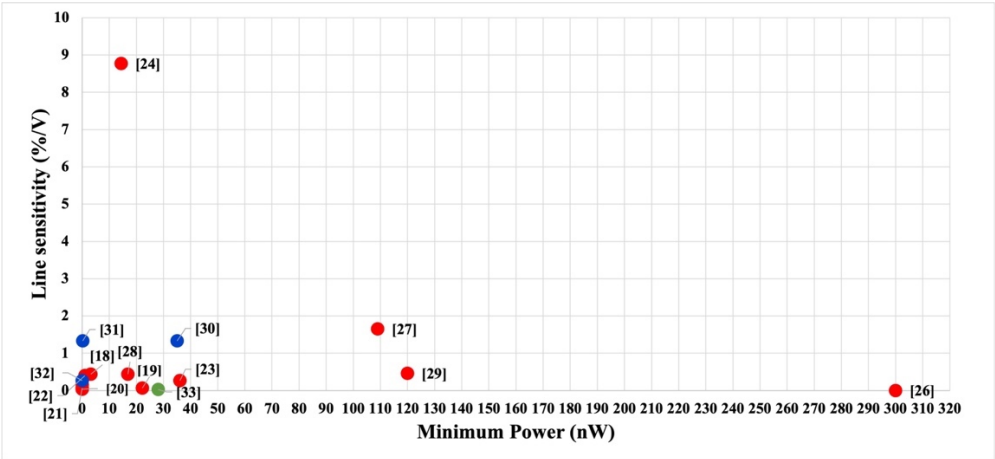


Fig. 21. Line sensitivity as a function of minimum power consumption.

At the end, the voltage reference which turn out to have a good temperature coefficient TC of 10 ppm/°C in a wide range of temperature [0÷80] °C and at the same time a good line sensitivity of 0.27 %/V in a wide range of supply voltage of [0.9÷4] V seems to be the MOS-based one proposed in [23].

Once the ultra-low power voltage references taken from the state of art have been reviewed, some proposed voltage reference architectures will be presented in the following paragraph by analyzing the circuit topology, the main post-layout simulation results and whenever possible also some measurement results.

2.5 CMOS Resistor-Less Nano Power Voltage Reference with Trimming Strategy

The aim of this work is to present a solution of nano-power CMOS voltage reference with low-current consumption in which the subthreshold operating region was exploited to achieve a low-current consumption over a wide range of temperature and supply voltages. This bandgap voltage reference is based on the difference between MOS threshold voltages to achieve a reference voltage with a good temperature behavior and insensitive of PVT variations. At this purpose, MOS transistors with different threshold voltages together with design consideration have been carefully considered to achieve good performances and to avoid some criticalities due to the low-power operation.

2.5.1 Circuit Description

The simplified schematic of the proposed low-power voltage reference is show in Fig. 22 which is made up by a start-up circuit, a current generator section and an active load. This self-biased current reference section does not require resistors and it generates a current insensitive to PVT variations to be injected into the active load. A start-up circuit is needed to ensure the biasing into desired stable state and to avoid the zero-current state at the start-up of the circuit while a capacitor C_1 is needed to ensure a trade-off between time response, PSRR and transient line regulation.

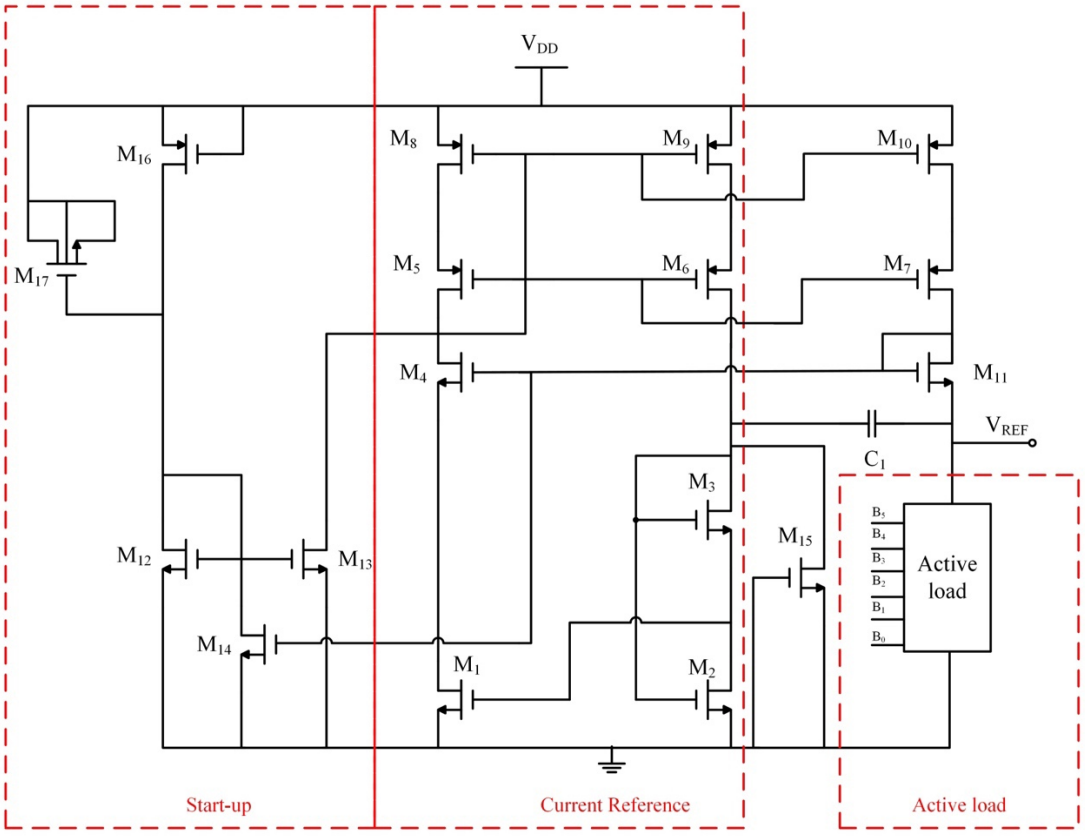


Fig. 22. Simplified schematic of the CMOS proposed low-power voltage reference.

All the transistors are biased in subthreshold region and all the bulk terminals are connected to V_{DD} and to ground for PMOS and NMOS transistor respectively. Transistor with different threshold voltages have been exploited as follows: transistors M_1 and M_3 and transistors into the active load are 1.8 V natural MOS transistors (NLVTMOS and PLVTMOS), transistor M_2 is 1.8 V MOS transistor (NLLMOS and PLLMOS) while all the other transistors are 5 V MOS transistors (MN5V and PN5V).

Table III summarized information regard the chosen technology and the typical threshold voltages value of the different type of transistors. Transistor sizes of the overall simplified voltage reference schematic are shown in Table IV while the value of the capacitance C_1 is 12 pF.

TABLE III: Voltage ranges and threshold voltages of the BCD8sp technology.

Technology	BCD8sp 160 nm CMOS technology		
	Voltage range	**V_{TH}-NMOS**	**$\lvert V_{TH}\rvert$-PMOS**
NLVTMOS, PLVTMOS	$V_{GS} \geq 0\ V$, $V_{DS} \leq 2\ V$	174.7 mV	201.9 mV
NLLMOS, PLLMOS	$V_{GS} \geq 0\ V$, $V_{DS} \leq 2\ V$	611 mV	553 mV
MN5V, PN5V	$V_{GS} \geq 0\ V$, $V_{DS} \leq 5\ V$	684 mV	736 mV

TABLE IV: Transistor sizes of the overall simplified voltage reference schematic.

Transistor	**W/L (μm / μm)**
M_1	9 / 200
M_2	35 / 30
M_3	2.5 / 46
M_4	27.5 / 3
$M_{5\text{-}6\text{-}7}$	10 / 40
$M_{8\text{-}9\text{-}10}$	8 / 50
M_{11}	55 / 3
$M_{12\text{-}13\text{-}14\text{-}15}$	5 / 0.8
M_{16}	70 / 0.6
M_{17}	55 / 55
M_{18}	2 / 207
M_{19}	2 / 69

2.5.2 Current Reference

The current reference section shown in Fig. 22 is used to generate and to provide a reference current insensitive to supply voltage variations which also compensate the temperature effects on the reference voltage V_{REF}. It can be noted that this current reference has been taken from the state of art [18] where the same circuit has been used to produce a reference current for a reference circuit.

By inspection of the circuit, the self-biased configuration is made up by MOS transistors $M_{1\text{-}3}$ among which a linear combination between their gate-source voltages is generated. This relationship can be expressed as follows:

$$V_{GS2} = V_{GS1} + V_{GS3} \tag{34}$$

The I-V characteristic of the MOS transistor operating in subthreshold region is given by equation (35) while the expression of the gate-source voltage shown in equation (36) can be obtained under the assumption of $V_{DS} \geq 4\ V_T$.

$$I_D = \frac{W}{L} C_{ox} \mu V_T^2 exp\left(\frac{V_{GS}-V_{TH}}{nV_T}\right)\left[1 - exp\left(-\frac{V_{DS}}{V_T}\right)\right] \tag{35}$$

$$V_{GS} = V_{TH} + nV_T \ln\left(\frac{L}{W}\frac{I_D}{\mu C_{ox} V_T^2}\right) \tag{36}$$

By using (36), equation (34) can be rewritten as follows:

$$n_2 V_T \ln\left(\frac{L_2}{W_2}\frac{I_{D2}}{\mu_2 C_{ox} V_T^2}\right) = \Delta V_{TH} + n_1 V_T \ln\left(\frac{L_1}{W_1}\frac{I_{D1}}{\mu_1 C_{ox} V_T^2}\right) + n_3 V_T \ln\left(\frac{L_3}{W_3}\frac{I_{D3}}{\mu_3 C_{ox} V_T^2}\right) \quad (37)$$

where $\Delta V_{TH} = V_{TH1} + V_{TH3} - V_{TH2}$.

Assuming the electron mobilities in (37) identical ($\mu = \mu_1 = \mu_2 = \mu_3$) and the same aspect ratio of the cascode current mirror made up by transistors $M_{5\text{-}6}$ and $M_{8\text{-}9}$, the generated current can be expressed in the following form:

$$I_{D1} = Q^{1/\Sigma_n} \mu V_T^2 \exp\left(-\frac{\Delta V_{TH}}{V_T \Sigma_n}\right) \quad (38)$$

where $Q = a^{m_2 - m_3}\left[\frac{(W/L)_1^{n_1}\cdot(W/L)_3^{n_3}}{(W/L)_2^{n_2}} \cdot C_{ox}\right]$, $\Sigma_n = n_1 + n_2 + n_3$ and $a = (W/L)_{5,8} = (W/L)_{6,9}$.

To avoid the breakdown of the natural transistor M_1 when the supply voltage V_{DD} will be higher than 1.8 V (breakdown voltage), an additional clamping transistor M_4 which is a 5-V NMOS has been included.

Additionally, the ability of the reference circuit to work properly when the supply voltage is above the breakdown voltage of the low-threshold voltage MOS transistors belonging to the current reference has been reached thanks to the adoption of 5-V MOS into the cascode current mirror $M_{5\text{-}10}$. Furthermore, the reason to choose a cascode current mirror instead a simple mirror lies in its greater robustness against supply voltage variations.

2.5.3 Active Load and Temperature Compensation

The nominal active load is made up by the series of two diode-connected transistors M_{18} and M_{19} which are used to provide the nominal reference voltage around 400 mV. Once again, an additional clamping transistor M_{11} is placed to avoid the breakdown of the native transistors into the active load when the supply voltage becomes high.

The generated current obtained in equation (38) is mirrored by the cascode current mirror $M_{5\text{-}10}$ into the active load branch. Under the assumption of $(W/L)_{5-7} = (W/L)_{8-10}$, the nominal reference voltage provided by the diode-connected transistors M_{18} and M_{19} into the active load section can be expressed as follows:

$$V_{REF} = V_{GS18} + V_{GS19} = V_{TH18} + n_{18} V_T \ln\left(\frac{I_{D10}}{\left(\frac{W}{L}\right)_{18} C_{ox}\mu_n V_T^2}\right) + V_{TH19} + n_{19} V_T \ln\left(\frac{I_{D10}}{\left(\frac{W}{L}\right)_{19} C_{ox}\mu_n V_T^2}\right) =$$

$$V_{TH18} + n_{18} V_T \ln\left(\frac{Q^{1/\Sigma_n}\mu V_T^2 \exp\left(-\frac{\Delta V_{TH}}{V_T \Sigma_n}\right)}{\left(\frac{W}{L}\right)_{18} C_{ox}\mu_n V_T^2}\right) + V_{TH19} + n_{19} V_T \ln\left(\frac{Q^{1/\Sigma_n}\mu V_T^2 \exp\left(-\frac{\Delta V_{TH}}{V_T \Sigma_n}\right)}{\left(\frac{W}{L}\right)_{19} C_{ox}\mu_n V_T^2}\right) \quad (39)$$

Consequently, the final expression of the nominal reference voltage is given by equation (40).

$$V_{REF} = V_{TH18} + V_{TH19} + n_{18} V_T \ln\left(\frac{Q^{1/\Sigma_n}}{\left(\frac{W}{L}\right)_{18} C_{ox}}\right) + n_{19} V_T \ln\left(\frac{Q^{1/\Sigma_n}}{\left(\frac{W}{L}\right)_{19} C_{ox}}\right) - \frac{n_{18}}{\Sigma_n}\Delta V_{TH} - \frac{n_{19}}{\Sigma_n}\Delta V_{TH} \quad (40)$$

Temperature dependence of the reference voltage is related to the threshold voltage and to the thermal voltage temperature dependence. In fact, temperature relationship of these two voltages is shown in equation (41) and (42) respectively.

$$V_{TH} = V_{TH0}(T_0) + (k_{t1} + k_{t2} V_{BS})\left(\frac{T}{T_0} - 1\right) \quad (41)$$

$$V_T = \frac{kT}{q} \quad (42)$$

where T_0 is the absolute temperature and k_{t1}, k_{t2} are the negative temperature coefficients.

Under this premises, temperature coefficients of threshold and thermal voltages can be obtained by deriving these two voltages with respect to temperature and by setting the obtained values equal to zero. Finally, temperature dependence of the reference voltage can be achieved by setting $\frac{\partial V_{REF}}{\partial T} = 0$ and $V_{BS} = 0$, thus obtaining the expression of the TC of the reference circuit.

$$TC = \frac{k_{t18}}{T_0} + \frac{k_{t19}}{T_0} + \frac{n_{18}k}{q}\ln\left(\frac{Q^{1/\Sigma_n}}{\left(\frac{W}{L}\right)_{18}C_{ox}}\right) + \frac{n_{19}k}{q}\ln\left(\frac{Q^{1/\Sigma_n}}{\left(\frac{W}{L}\right)_{19}C_{ox}}\right) - \frac{n_{18}}{\Sigma_n}\left(\frac{k_{t1}}{T_o} + \frac{k_{t3}}{T_o} - \frac{k_{t2}}{T_o}\right) - \frac{n_{19}}{\Sigma_n}\left(\frac{k_{t1}}{T_o} + \frac{k_{t3}}{T_o} - \frac{k_{t2}}{T_0}\right) \quad (43)$$

where k_{t18} and k_{t19} are temperature coefficient of MOS transistor M_{18} and M_{19}, respectively while k_{t1}, k_{t2} and k_{t3} are temperature coefficient of MOS transistors M_1, M_2 and M_3, respectively.

Temperature coefficient of the reference voltage depends on the combination between technological parameter and design parameter. Once the process has been chosen, technological parameters were set, and they cannot be absolutely modified.

A simplified expression of TC can be obtained by considering MOS transistors operating in subthreshold region which have the same value of *n* parameters, it can be possible to set $n_{18} \approx n_{19}$ and consequently: $\frac{n}{\Sigma_n} \approx 1$. At the same time, by considering the same temperature coefficient of the MOS transistors operating in subthreshold region, it can be possible to set: $k_{t1} \approx k_{t2} \approx k_{t3} \approx k_{t18} \approx k_{t19}$. Therefore, the simplified expression of the Temperature Coefficient becomes:

$$TC = \frac{nk}{q}\ln\left(\frac{Q^{1/\Sigma_n}}{\left(\frac{W}{L}\right)_{18}C_{ox}}\right) + \frac{nk}{q}\ln\left(\frac{Q^{1/\Sigma_n}}{\left(\frac{W}{L}\right)_{19}C_{ox}}\right) \quad (44)$$

By inspection of equation (44), temperature coefficient is logarithmically dependent on the MOS transistors sizes of the transistor in the active load. Therefore, temperature compensation can be achieved by choosing large lengths value of the diode connected transistor M_{18} and M_{19} into the active load section which constituted the main temperature compensation approach followed in this design.

2.5.4 Trimming Strategy

Integrated circuits are affected to non-idealities associated with the fabrication of the circuit in any technological process. To give some examples, these non-idealities appear in the form of current mirror mismatches, resistors' tolerances, channel-length modulations, input offset voltages, early voltages among other. Some of these errors are systematic and consequently can be predicted during the simulation phase. However, process variations must be added to the systematic ones resulting in devices mismatches, die-to-die variations, wafer-to-wafer variations, and lot-to-lot variations. These kinds of variations are random with a great and negative impact to the performance parameters of an integrated circuit. Therefore, these variations must be considered during the design phase by planning adjustment (trim) to fix the errors which may arise. After-silicon fine-tuning with a trimming accuracy represent a simple solution to drastically reduce process variations and to improve the affected performance parameters. Unfortunately, trimming strategies that can be performed after the silicon has been done results in a little flexibility and increased costs. Anyway, the robustness of the trimming network is strictly related to the pre-fabrication design and consequently integrated trimming strategies can be represent a good solution to achieve a trade-off between accuracy and costs. In the voltage reference contest process variation may be affect the precision with which reference voltage has been reached. Additionally, it was proved that these variations linearly depend on temperature thus impacting the temperature behavior of the related reference voltage. Nevertheless, these errors can be mitigated by adding or subtracting a component to the reference voltage at any single temperature setting provided by a trimming strategy. Therefore, the obtained value of the refence

voltage consists of the combination between the nominal reference voltage $V_{ref,nom}$, the offset voltage V_{offset} and the trimming voltage $V_{trimming}$ as shown in equation (45).

$$V_{ref} = V_{ref,nom} \pm V_{offset} \pm V_{trimming} \quad (45)$$

With the aim to compensate process variation on the reference voltage, trimming strategy on the active load has been added to the proposed CMOS voltage reference. At this purpose, Fig. 23 shows the complete schematic of the proposed CMOS voltage reference comprehensive of trimming network while Table V shows the transistors sizes of the active load.

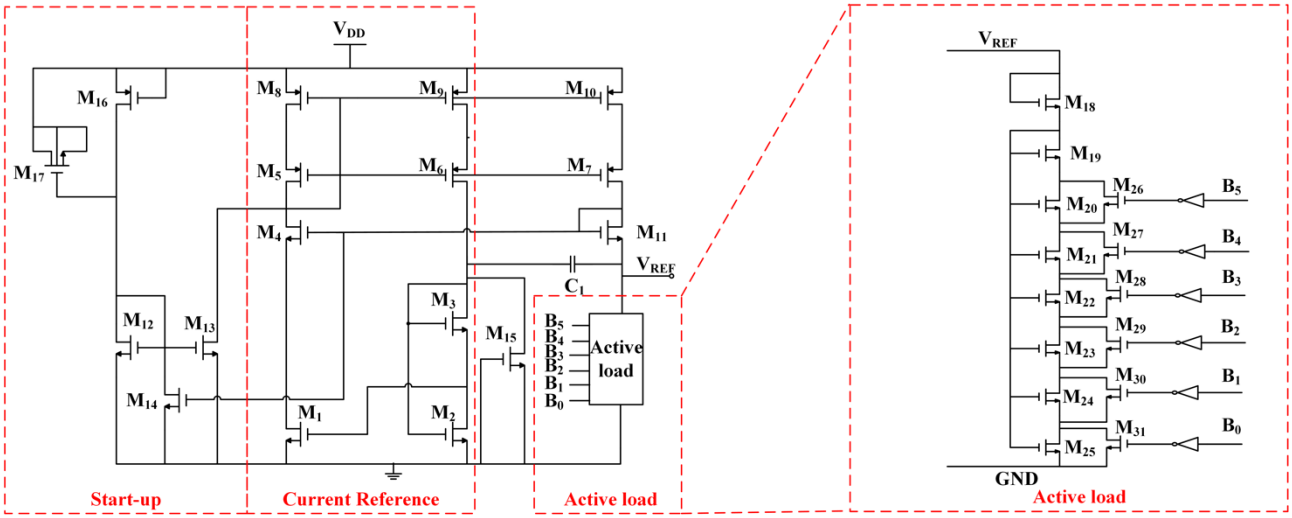


Fig. 23. Schematic of the CMOS proposed low-power voltage reference with trimming strategy on the active load.

TABLE V: Transistor sizes of the active load.

Transistor	**W/L (μm / μm)**
M_{18}	2 / 207
M_{19}	2 / 69
M_{20}	2 / 138
M_{21}	2 / 112
M_{22}	2 / 52.5
M_{23}	2 / 25
M_{24}	2 / 12.5
M_{25}	2 / 6
$M_{26\text{-}31}$	5 / 1

The active load consists of two diode-connected transistors $M_{18\text{-}19}$ which are used to provide the nominal reference voltage while transistors $M_{20\text{-}25}$ which shall be enabled by switch transistors $M_{26\text{-}31}$ and by six trimming bits $B_{0\text{-}6}$ has been added with the aim to trim the reference voltage.

Once the achieved reference voltage is far from the nominal as a result to the process variations, additional diode-connected transistors in parallel to the nominal active load can be enabled by both switch transistors and trimming bits to restore the nominal reference voltage.

The design of this trimming strategy [34] is based on the accuracy with which the reference voltage is to be reached and on the expected tolerance of the untrimmed reference voltage. The required number of trimming bits are related to the least significant bit value (LSB) and by the full-scale tolerance expected (FS) as follows:

$$\#Bits \geq \frac{\ln\left(\frac{V_{FS}}{V_{LSB}}+1\right)}{\ln 2} \quad (46)$$

where $V_{LSB} \geq \frac{V_{\pm\%accuracy} \cdot V_{ref}}{2}$ and $V_{FS} = V_{LSB}\left(2^{\#Bits} - 1\right)$.

The trimming network of the proposed voltage reference was designed to reach an accuracy on the reference voltage of 0.05 % which leads a voltage variation of 2 mV and it has been achieved by fixing five trimming bits multiples of the less significant bit. An additional bit has been added to fix the sign which need to be equal to the amount of the trimming voltages as much as possible. The choice of only one bit for the sing correction instead of choosing five bits allow to save area at the price of less accuracy.

2.5.5 Start-up Circuit

A start-up section made up by transistors $M_{12\text{-}17}$ has been added to the voltage reference schematic shown in Fig. 22 and in Fig. 23 to avoid the zero-current condition in the current generator section at the starting time. In this time interval, the current generator has not yet achieved the reference current shown in equation (38) and, consequently the active load does not have sufficient current to generate the desired reference voltage. The working principle of the proposed start-up circuit is based on leakage current together with capacitance approach to force the current into the current generator section at the starting time t = 0. At the start-up, when the supply voltage V_{DD} is still zero PMOS transistor M_{16} is turned on and a leakage current start flowing into M_{16} and consequently is mirrored by $M_{12\text{-}13}$ thus forcing the drain voltage of M_{13} low. When the leakage current flows in M_{13}, the drain terminal of M_{13} which is connected to the gate of M_8 will be forced to ground and consequently M_8 is forced to turn-on. In this way, the start-up circuit force the current generator section to quickly turn-on. Once the current generator section has been reached the stable state, the voltage at the gate of M_4 will be high and consequently M_{14} is forced to turn-on. Therefore, the leakage current will be forced to ground through transistor M_{14} and finally the start-up circuit gets disconnected to the reference circuit. Time constant of the start-up circuit is provided by MOS capacitor M_{17} in which drain, source and bulk terminals are shorted all together.

The relationship between the leakage current and the time constant of this circuit is given by the following equation:

$$i(t) = \frac{V_{DD}}{R} e^{-t/\tau} \tag{47}$$

where the time constant of the circuit is $\tau = RC$, R is the small-signal resistance of M_{16} and C is given by the sum of the parasitic capacitance which insist on M_{17}.

A fast response of the start-up circuit can be achieved with high values of R and C which can be achieved by setting high values of W and L thus resulting in higher area occupation. Proper size dimensions of these two transistors are chosen during the design to achieve a trade-off between fast response and low-area occupation.

At the end, once the reference circuit has achieved the steady-state and the start-up has turned-off, a potential leakage current may be flow into the start-up section. This leakage current may affect the reference current resulting in an additional current into the left branch of the current generator section (where transistor M_1 is) thus unbalancing the current generator section. This possible leakage current can be balanced by an additional transistor M_{15} with the same dimension of M_{13} that is added to the right branch of the current generator section (where transistor M_2 is).

2.5.6 Sensitivity to Supply Voltage Variations

The evaluation of the reference voltage sensitivity to supply voltage V_{DD} variations is expressed through the Line Sensitivity LS. The simplified expression of the LS can be defined as follows:

$$LS = \frac{(\Delta V_{REF}/\Delta V_{DD})}{V_{REF,nom}} \tag{48}$$

where ΔV_{REF} is the reference voltage variation within the supply voltage operating range ΔV_{DD} and $V_{REF,nom}$ is the nominal value of the reference voltage.

It is apparent that line sensitivity is strictly related to ΔV_{REF} and consequently to the current variations of the current flowing into the active load. Therefore, line sensitivity optimization can be achieved by minimizing reference voltage variations through minimizing the current variations. The basic scheme of the active load branch is shown in Fig. 24 in which the current generator generates the reference current I flowing into the active load and the diode-connected transistor M_1 represent the simplified active load.

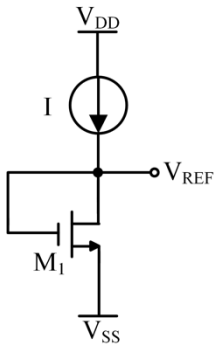


Fig. 24. Basic scheme of the simplified voltage reference.

The relationship between the subthreshold current flowing toward the active load and the drain-source voltage is highlighted in equation (49).

$$I = \mu_n C_{ox} \frac{W}{L} V_T^2 e^{\frac{V_{GS}}{nV_T}} e^{\frac{\lambda_D V_{DS}}{nV_T}} \tag{49}$$

where λ_D is the drain-induced-barrier-lowering factor.

Transistor operating in subthreshold region do not suffer from the channel-length modulation which means that the current dependence on V_{DS} is only due to a second-order effect known as drain-induced-barrier-lowering (DIBL). This effect can be significantly reduced by increasing the transistor's channel length.

Supply voltage variations ΔV_{DD} results in a drain-source voltage variations ΔV_{DS} which can be expressed as follows: $\Delta V_{DS} = V_{DSMAX} - V_{DSMIN}$. Under the assumption of a constant V_{GS}, the current variation due to the drain-source voltage can be summarized in the following ratio:

$$\frac{I_{DMAX}}{I_{DMIN}} = e^{\frac{\lambda_D V_{DS}}{nV_T}} \tag{50}$$

Being the simplified expression of the reference voltage $V_{REF} = V_{GS} = V_{TH} + nV_T \ln\left(\frac{I_D}{W/LC_{ox}\mu_n V_T^2}\right)$, reference voltage variations ΔV_{REF} are expressed as follows:

$$\Delta V_{REF} = nV_T \ln\left(\frac{I_{DMAX}}{I_{DMIN}}\right) = nV_T \frac{\lambda_D V_{DS}}{nV_T} = \lambda_D V_{DS} \tag{51}$$

Therefore, reference voltage variations are related to the supply voltage variations through the $\lambda_D V_{DS}$ dependence highlighted in equation (51). Under this assumption, the final expression of the line sensitivity, which is usually expressed as a percentage, can be written as follows:

$$LS = \frac{(\Delta V_{REF}/\Delta V_{DD})}{V_{REF,nom}} = \frac{(\lambda_D V_{DS}/\Delta V_{DS})}{V_{REF,nom}} = \frac{\lambda_D}{V_{REF,nom}} \ [\% / V] \tag{52}$$

Line sensitivity can be optimized by minimizing the reference voltage variations and consequently the current variations. The stability of the generated current has been achieved by setting large length values for transistors $M_{5\text{-}10}$ together with a cascode mirror structure which represent the main approach followed during the design to reduce the sensitivity to supply voltage variations. Large length values have been achieved by using staked transistors thus resulting in an increased minimum

supply voltage V_{DD}, therefore a trade-off between minimum supply voltage and robustness against supply voltage variations shall be achieved.

2.5.7 Mismatch and Process Variations

The reference voltage expressed in equation (40) is the results of a linear combination of threshold voltages of the MOS transistors in the current reference section and in the active load. Although this equation provides the evaluation of the nominal reference voltage, the presence of two type of variations may leads to the variation of the nominal expected value. The first one type of variations can be indicated as process variations which are generally distinguished in within die or intra-die variations and die-to-die variations. These kind of variations causes mismatch between transistors affecting the relative and absolute accuracy of the transistor parameters. In this design, mismatch variations have been mitigated by using careful layout techniques well described in Section II while process variations have been mitigated thanks to the adoption of the already described trimming strategy.

With the aim to evaluate the effect of the process variation to the mean value of the reference voltage, the standard deviation of the reference voltage has been analyzed. The standard deviation of the reference voltage is related to the standard deviation of the threshold voltage of the different threshold voltage transistors adopted, as shown in equation (53).

$$\sigma_{V_{REF}} = \sqrt{\sigma_{LVTMOS}^2 + \sigma_{LLMOS}^2} \tag{53}$$

where σ_{LVTMOS} and σ_{LLMOS} are the threshold voltage standard deviations of the natural LVTMOS and standard LLMOS, respectively.

The covariance of these two threshold voltages is zero and these two voltages are also statistically independent by simplifying the reference voltage standard deviation as follows:

$$\sigma_{V_{REF}} = \sqrt{2}\sigma_{V_{TH}} \tag{54}$$

Being the $\sigma_{V_{TH}}$ the threshold voltage standard deviations, it is apparent that the main contribution of reference voltage accuracy is affected by the threshold voltages variations.

2.5.8 Pre-Layout and Post-Layout Simulation Results

The proposed voltage reference was designed and simulated by using the BCD8sp technology which is a 160-nm CMOS bulk-technology provided by STMicroelectronics. Simulations were carried out in two phases: initially the performances of the proposed voltage reference have been simulated at the schematic level and once the robustness of the circuit schematic was proved and the layout done the same simulations have been repeated at layout level. The realization of the layout may compromise some parameters and consequently the performance of the circuit, therefore it represents a crucial part of the design to be carefully taken into account. Performances can be preserved by adopting layout design rules respecting first of all the minimum distances and then by trying to avoid crosstalk between the critical signal paths and to minimize parasitics.

The layout of the voltage reference is shown is Fig. 25 where the occupied area is equal to $340\ \mu m \times 127\ \mu m = 43180\ \mu m^2$. Besides the mandatory design rules which are the minimum distances among others, some important layout considerations have been applied during the layout realization of the proposed circuit. Subthreshold approach together with current in the range of nano-ampere require close attention during the layout of the core of the circuit which are the current generator section and the active load in this design. A slight variation of the current even under a 1 nA may be compromise the operation of the overall system. A proper matching between transistors into the current reference section with an accurate matching between MOS transistor into the cascode current mirror $M_{5\text{-}10}$ has been adopted during this layout design. Furthermore, long metal connections

which bring critical signal such as supply voltage, ground and reference voltage may introduce parasitics which can compromise some performance especially in terms of time response and noise. In fact, long line of metallization near the metal that brings the reference voltage shall be avoided so as not to compromise the performances of the design. The robustness of metal which lead the reference voltage has been achieved by reducing to the essential the metallization of the active load by positioning all the transistors into the active load close to each other.

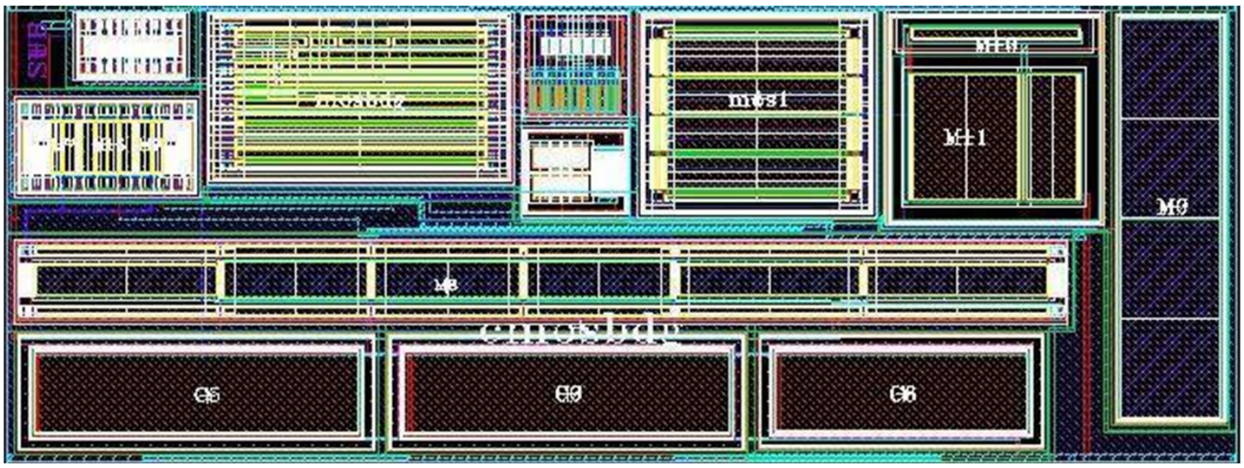


Fig. 25. Layout of the proposed CMOS voltage reference.

Pre-layout and post-layout simulations were carried out by using CADENCE Virtuoso tool under a wide range of supply voltage [1.2÷5] V and temperature [–40÷125] °C. The BCD8sp technology also provide different models of the transistors: typical (TYP), maximum (MAX), minimum (MIN) and statistical (stat). Where possible, all the simulations have been carried out by using not only the typical model of the transistor but also the other ones to prove the robustness of the proposed reference circuit over corner and process variations.

In the following analysis, nominal case will be used to indicate the operating condition under this constraint: supply voltage V_{DD} = 3 V, temperature T = 25 °C and TYP model.

Pre-layout simulation results of the reference voltage at different value of supply voltage, temperature and models are summarized in TABLE VI, VII and VIII. The nominal value of the reference voltage V_{REF} is 404.9 mV while the minimum simulated value is 372 mV (at V_{DD} = 1.2 V, T = 125 °C and MOD. MIN.) and the maximum simulated value is 468 mV (at V_{DD} = 5 V, T = 125 °C and MOD. MAX.).

TABLE VI: Simulated reference voltage at different supply voltage and models (T = 25 °C).

V_{REF} (mV) (T = 25 °C)	**V_{DD} = 1.2 V**	**V_{DD} = 3 V**	**V_{DD} = 5 V**
MOD.TYP.	404.92392	405.14486	406.47909
MOD.MAX.	447.4355	447.96304	449.42314
MOD.MIN.	374.2421	374.45406	375.64836

TABLE VII: Simulated reference voltage at different supply voltage and models (T = –40 °C).

V_{REF} (mV) (T = –40 °C)	**V_{DD} = 1.2 V**	**V_{DD} = 3 V**	**V_{DD} = 5 V**
MOD.TYP.	410.54654	410.9937	411.9708
MOD.MAX.	451.42722	454.3718	455.5117
MOD.MIN.	384.0137	384.29261	385.1384

TABLE VIII: Simulated reference voltage at different supply voltage and models (T = 125 °C).

V_{REF} (mV) (T = 125 °C)	V_{DD} = 1.2 V	V_{DD} = 3 V	V_{DD} = 5 V
MOD.TYP.	411.2741	413.5264	417.9249
MOD.MAX.	455.403	460.6576	468.2468
MOD.MIN.	372.8361	374.1797	377.379

Temperature dependence of the reference voltage in the range [–40÷125] °C for different supply voltages (V_{DD} = 1.2 V, V_{DD} = 3 V and V_{DD} = 5 V) and models (TYP., MAX., and MIN.) is shown in Fig. 26 in which the peak-to-peak voltage variations of the reference voltage are additionally highlighted. As already stated, with the aim to investigate the Temperature Coefficient (TC) of the proposed architecture temperature behavior of the reference voltage has been analyzed. TC has been evaluated by using the well-known box method whose equation is the following one:

$$TC = \left(\frac{V_{REF,max}|_T - V_{REF,min}|_T}{V_{REF}|_{T=25°C}}\right) \cdot \left(\frac{1}{T_{max} - T_{min}}\right) \cdot 10^6 \quad (55)$$

where $V_{REF,max}|_T$ and $V_{REF,min}|_T$ are the maximum and the minimum value of the reference voltage in the considered Temperature range T = $T_{max} - T_{min}$ while $V_{REF}|_{T=25°C}$ is the reference voltage at room temperature T = 25 °C. Therefore, peak-to-peak reference voltage can be defined as follows: $V_{REF,peak-to-peak} = V_{REF,max}|_T - V_{REF,min}|_T$.

Table IV, X and XI summarized the simulated reference voltage peak-to-peak variations and the achieved TC values for different value of supply voltage and models.

In the nominal condition, a slight reference voltage variation of only 9 mV occurs in the temperature range between –40 °C and 125 °C thus leading a TC of only 137 ppm / °C. The minimum and maximum achieved value of the reference voltage peak-to-peak which consequently leads to the minimum and maximum values of TC are 7 mV with TC of 106 ppm / °C (at MOD. TYP. and V_{DD} = 1.2 V) and 20 mV with TC of 275 ppm / °C (at MOD. MAX. and V_{DD} = 5 V) respectively.

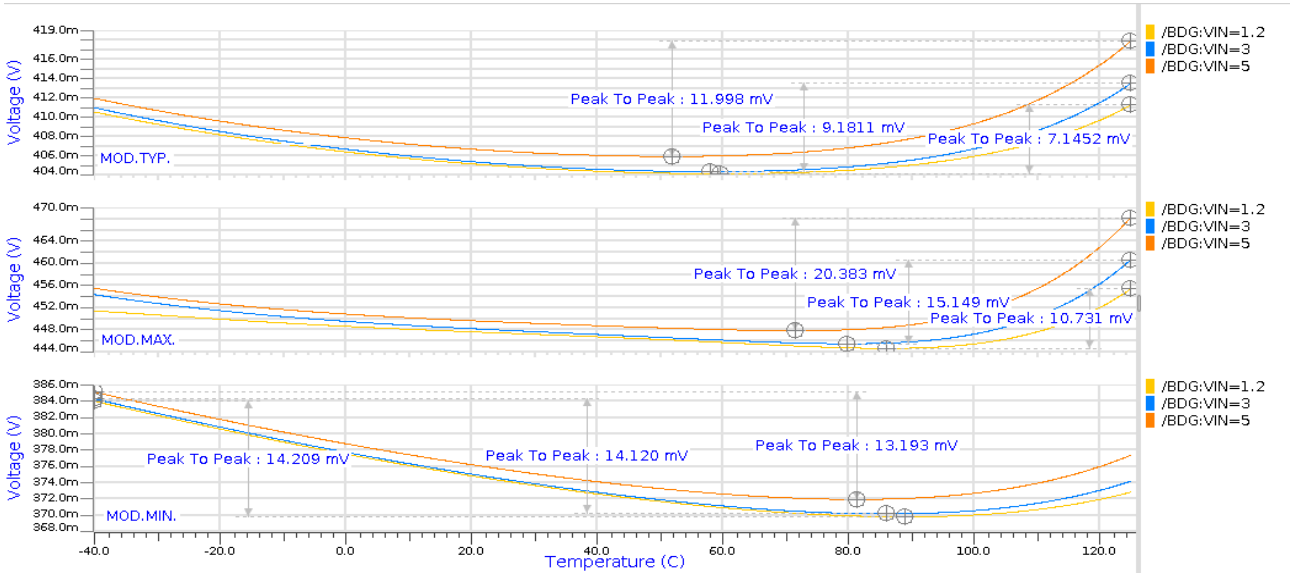


Fig. 26. Temperature dependence of the reference voltage for different supply voltages and models.

TABLE IX: Simulated reference voltage peak-to-peak variations and TC in the T range [–40÷125] °C (MOD. TYP.).

MOD.TYP.	$V_{REF(peak\text{-}to\text{-}peak)}$ (mV)	TC (ppm / °C)
V_{DD} = 1.2 V	7.1452	106.94
V_{DD} = 3 V	9.1811	137.34
V_{DD} = 5 V	11.998	178.89

TABLE X: Simulated reference voltage peak-to-peak variations and TC in the T range [–40÷125] °C (MOD. MAX.).

MOD.MAX.	$V_{REF(peak\text{-}to\text{-}peak)}$ (mV)	TC (ppm / °C)
V_{DD} = 1.2 V	10.731	145.35
V_{DD} = 3 V	15.149	204.95
V_{DD} = 5 V	20.383	274.87

TABLE XI: Simulated reference voltage peak-to-peak variations and TC in the T range [–40÷125] °C (MOD. MIN.).

MOD.MIN.	$V_{REF(peak\text{-}to\text{-}peak)}$ (mV)	TC (ppm / °C)
V_{DD} = 1.2 V	14.209	230.11
V_{DD} = 3 V	14.12	228.53
V_{DD} = 5 V	13.193	212.85

Post-layout simulations of the temperature dependence of reference voltage have been carried out only by using the typical model of the transistors. A comparison between the temperature behavior of the reference voltage for different value of supply voltage V_{DD} reached at schematic and layout level are shown in Fig. 27. Green curve represents the simulation results achieved at schematic level while yellow curve represents the results of the same simulation achieved at layout level. Table XI summarized the achieved post-layout reference voltage at different value of supply voltage by using typical model. The post-layout nominal reference voltage V_{REF} is 404.7 mV while the one achieved at schematic level was 404.9 mV.

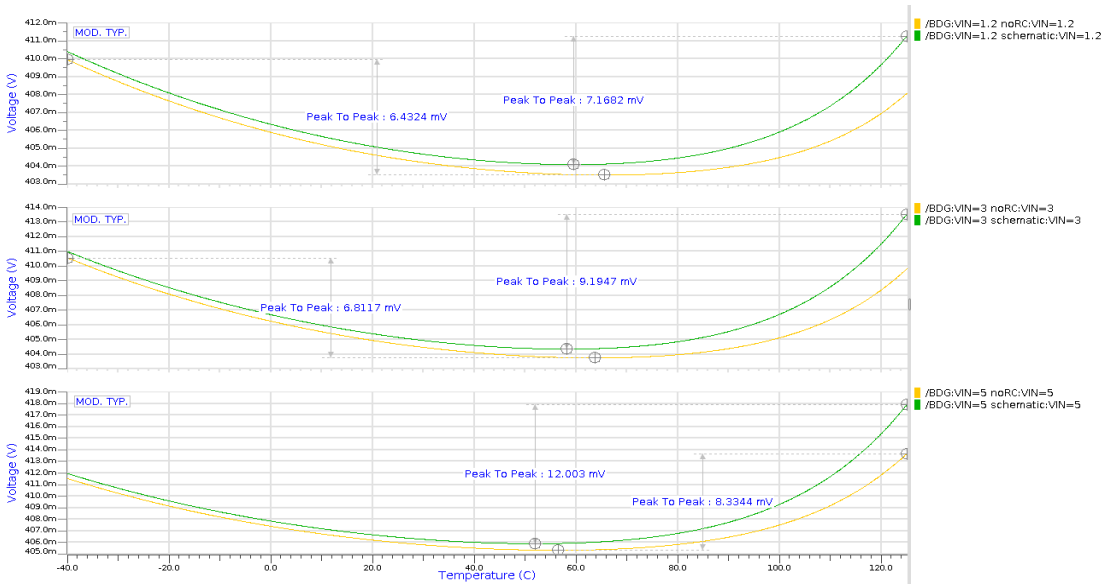


Fig. 27. Temperature dependence of the reference voltage for different value of supply voltage V_{DD} reached at schematic (green curves) and layout level (yellow curves) (MOD. TYP.).

In the nominal condition the peak-to-peak reference voltage variations change from 9.19 mV to 6.81 mV switching between schematic and layout level. Therefore, post-layout TC value becomes equal to 102.01 ppm / °C.

TABLE XII: Post-layout reference voltage V_{REF} at different value of supply voltage (MOD.TYP.).

MOD.TYP.	V_{REF} (mV)
V_{DD} = 1.2 V	404.42054
V_{DD} = 3 V	404.68271
V_{DD} = 5 V	405.99148

Temperature dependence of the supply current I_q for different supply voltage and models is show in Fig. 28 in which the achieved value of the current at different value of temperature (T = –40 °C, 25 °C, 125 °C and 150 °C) are highlighted. Note that this is an extensive simulation in which the temperature range was boosted until reaching the maximum temperature value of 150 °C. Additionally, Fig. 19 shows the same simulation results regarding the current temperature dependence by highlighting the peak-to-peak current variations.

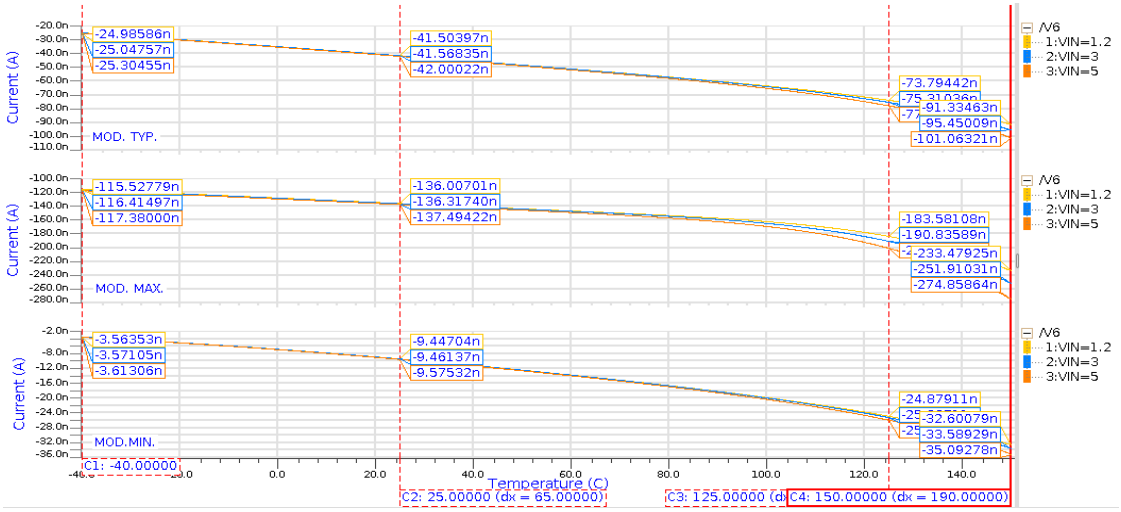


Fig. 28. Temperature dependence of the overall current at different supply voltage and models (current values).

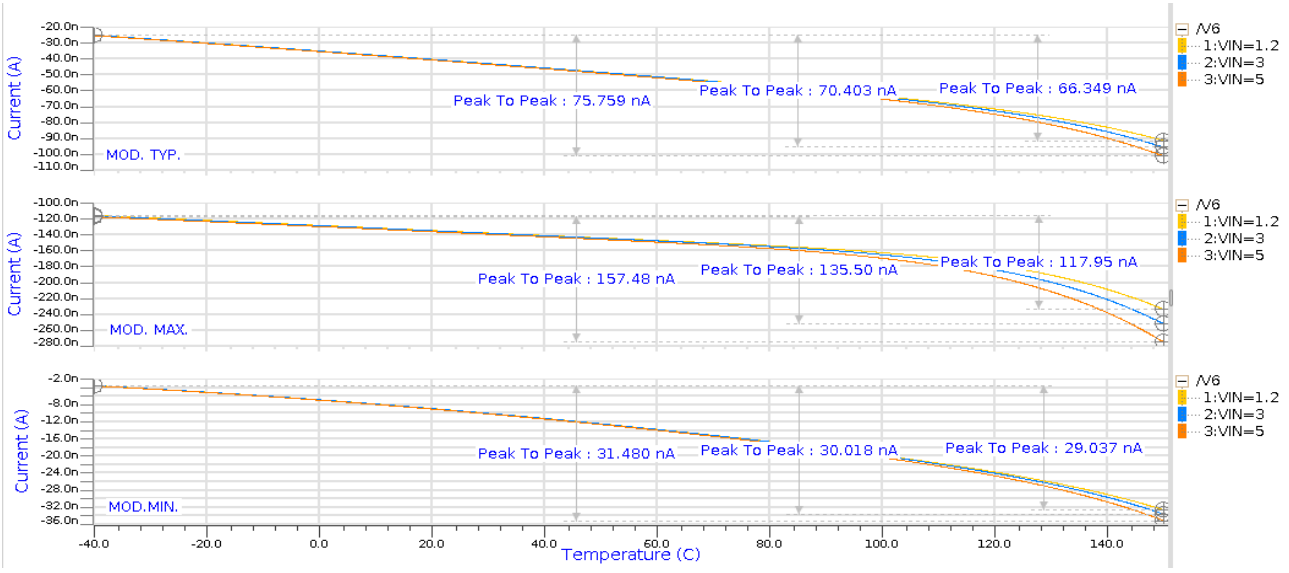


Fig. 29. Temperature dependence of the overall current at different supply voltage and models (peak-to-peak current variations)

Simulated supply current I_q at different value of supply voltage, temperature and model are summarized in Table XII, XIV and XV. The nominal value of the supply current is 41.57 nA while the values of the current variation are 50.26 nA in the temperature range [–40÷125] °C (at V_{DD} = 3 V and MOD. TYP.) and 70.40 nA in the temperature range [–40÷150] °C (at V_{DD} = 3 V and MOD.

TYP.). At room temperature (T = 25 °C), the supply current I_q changes from 41.5 nA to 42 nA by changing the supply from 1.2 V to 5 V which means that the total supply current variation is only 494 pA in the overall supply voltage range.

TABLE XIII: Simulated supply current I_q at different value at different value of temperature and model (V_{DD} = 1.2 V).

I_q (nA) (V_{DD} = 1.2 V)	**T = – 40 °C**	**T = 25 °C**	**T = 125 °C**	**T = 150 °C**
MOD.TYP.	24.98586	41.50397	73.79442	91.33463
MOD.MAX.	115.52779	136.00701	183.58108	233.47925
MOD.MIN.	3.56353	9.44704	24.87911	32.60079

TABLE XIV: Simulated supply current I_q at different value at different value of temperature and model (V_{DD} = 3 V).

I_q (nA) (V_{DD} = 3 V)	**T = – 40 °C**	**T = 25 °C**	**T = 125 °C**	**T = 150 °C**
MOD.TYP.	25.04757	41.56835	75.31036	95.45009
MOD.MAX.	116.41497	136.3174	190.83589	251.91031
MOD.MIN.	3.57105	9.46137	25.22711	33.58929

TABLE XV: Simulated supply current I_q at different value at different value of temperature and model (V_{DD} = 5 V).

I_q (nA) (V_{DD} = 5 V)	**T = – 40 °C**	**T = 25 °C**	**T = 125 °C**	**T = 150 °C**
MOD.TYP.	25.30455	42.00022	77.80262	101.0632
MOD.MAX.	117.38	137.4942	200.8553	274.8586
MOD.MIN.	3.61306	9.57532	25.91444	35.09278

Post-layout simulations of the temperature dependence of supply current have been carried out only by using the typical model of the transistors in the T range [–40÷150] °C. A comparison between the temperature behavior of the supply current for different value of supply voltage V_{DD} reached at schematic level and layout level are shown in Fig. 30. and in Fig. 31 in which supply current values at different value of temperature and peak-to-peak variations are highlighted. Once again, green curves represent the simulation results achieved at schematic level while yellow curves represent the results of the same simulation achieved at layout level. The nominal value of the supply current simulated at layout-level is 41.42 nA while the one achieved at schematic level was 41.57 nA. In the nominal condition, the supply current changes from 51 nA to 47.69 nA switching between schematic and layout level in the T range [–40÷150] °C. At room temperature (T = 25 °C), the post-layout supply current I_q changes from 41.36 nA to 41.85 nA by varying the supply from 1.2 V to 5 V which means that the total supply current variations is only 488 pA in the overall supply voltage range.

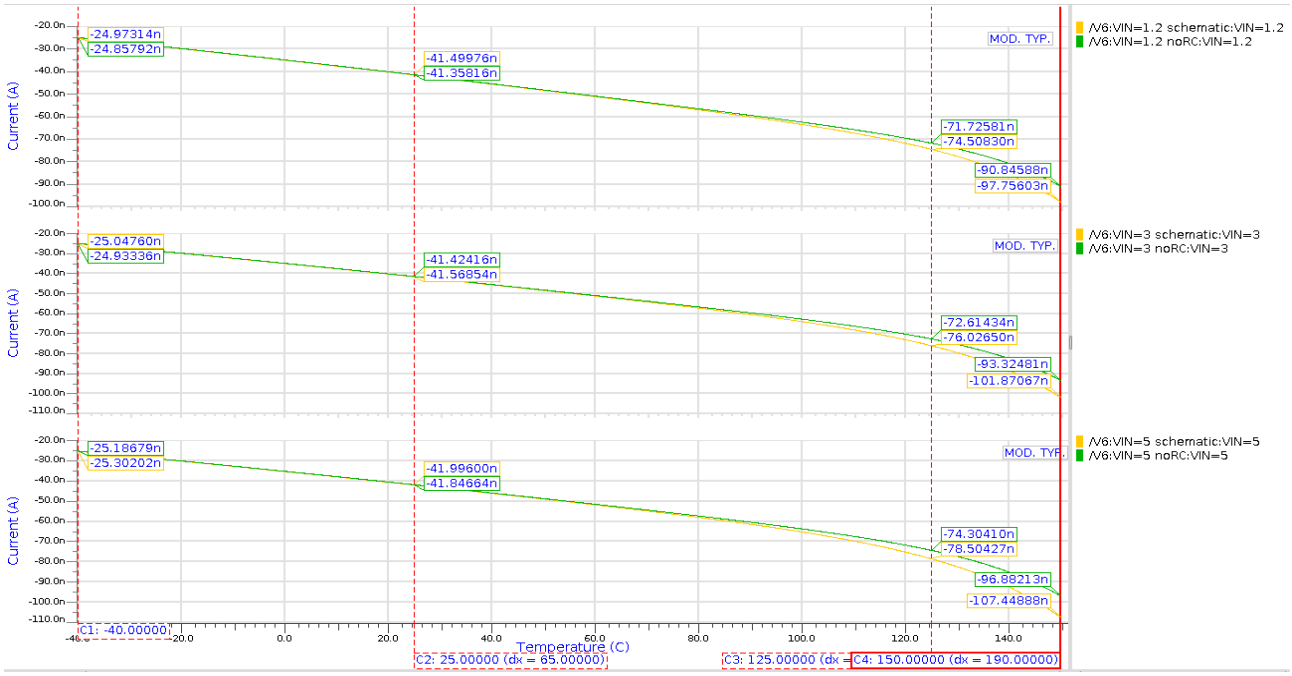


Fig. 30. Temperature dependence of the supply current for different value of supply voltage V_{DD} (MOD. TYP.) reached at schematic (yellow curves) and layout level (green curves) (current values).

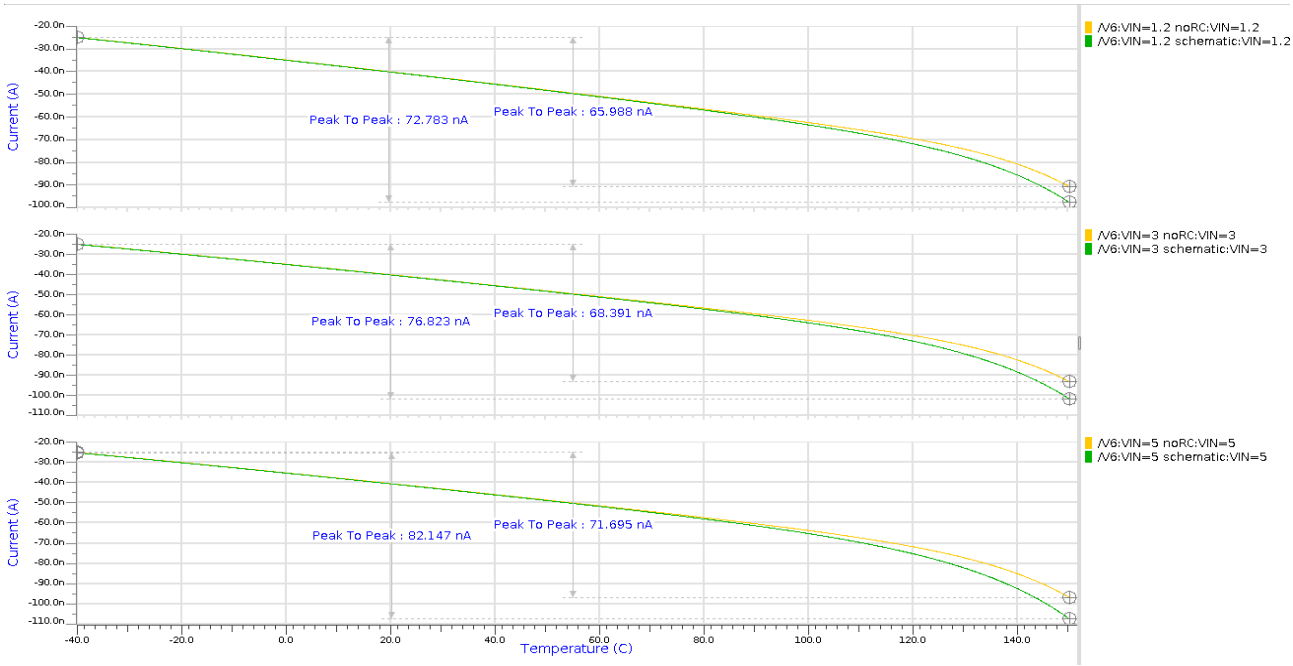


Fig. 31. Temperature dependence of the supply current for different value of supply voltage V_{DD} (MOD. TYP.) reached at schematic (green curves) and layout level (yellow curves) (peak-to-peak current variations).

Additionally, Table XVI summarized the achieved post-layout supply current values achieved with different supply voltage value by using typical model.

TABLE XVI: Post-layout supply current I_q at different value of supply voltage and temperature (MOD.TYP.).

I_q (nA) (MOD. TYP.)	T = – 40 °C	T = 25 °C	T = 125 °C	T = 150 °C
V_{DD} = 1.2 V	24.85792	41.35816	71.72581	90.84588
V_{DD} = 3 V	24.9336	41.42416	72.61434	93.32481
V_{DD} = 5 V	25.186789	41.84664	74.3041	96.88213

Supply voltage dependence of the reference voltage in the range [1.2 ÷ 5] V at different value of temperature (T = –40 °C, 25 °C and 125 °C) and models (TYP., MAX., and MIN.) are shown in Fig. 32 in which the peak-to-peak variations of the reference voltage are additionally highlighted. As already stated, with the aim to investigate the supply voltage dependence of the proposed architecture, the Line Sensitivity (LS) of the reference voltage has been analyzed by using the equation (56).

$$LS = \frac{(\Delta V_{REF}/\Delta V_{DD})}{V_{REF,nom}} \tag{56}$$

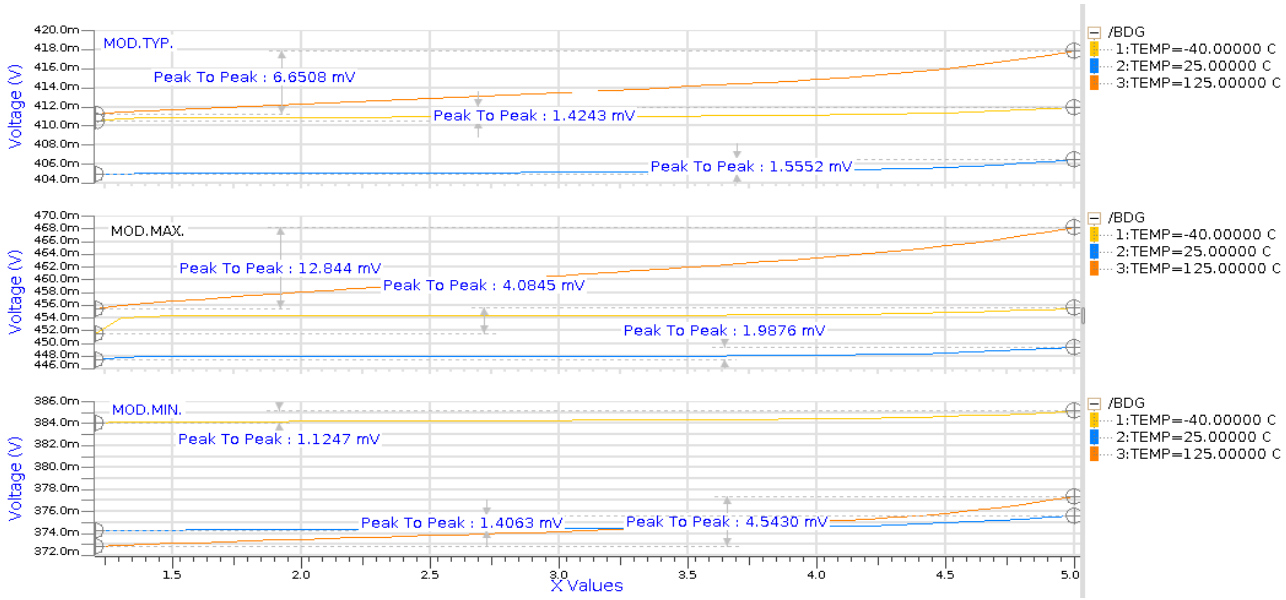


Fig. 32: Supply voltage dependence of the reference voltage for different temperature and model.

In the nominal condition, the reference voltage variation in the supply range [1.2 ÷ 5] V is 1.56 mV which consequently leads a LS value of only 0.102 % / V.

Post-layout simulations of the supply voltage dependence of reference voltage have been carried out by using only the typical model of the transistors in the supply range [1.2 ÷ 5] V. A comparison between the supply voltage dependence of the reference voltage for different value of temperature T reached at schematic and layout level are shown in Fig. 33. in which peak-to-peak variations are highlighted. Green curves represent the simulation results achieved at schematic level while yellow curves represent the results of the same simulation achieved at layout level. In the nominal condition,

post-layout simulation results shown a reference voltage variation of 1.57 mV thus leading a LS equal to 0.102 % / V which are basically the same results achieved at schematic level.

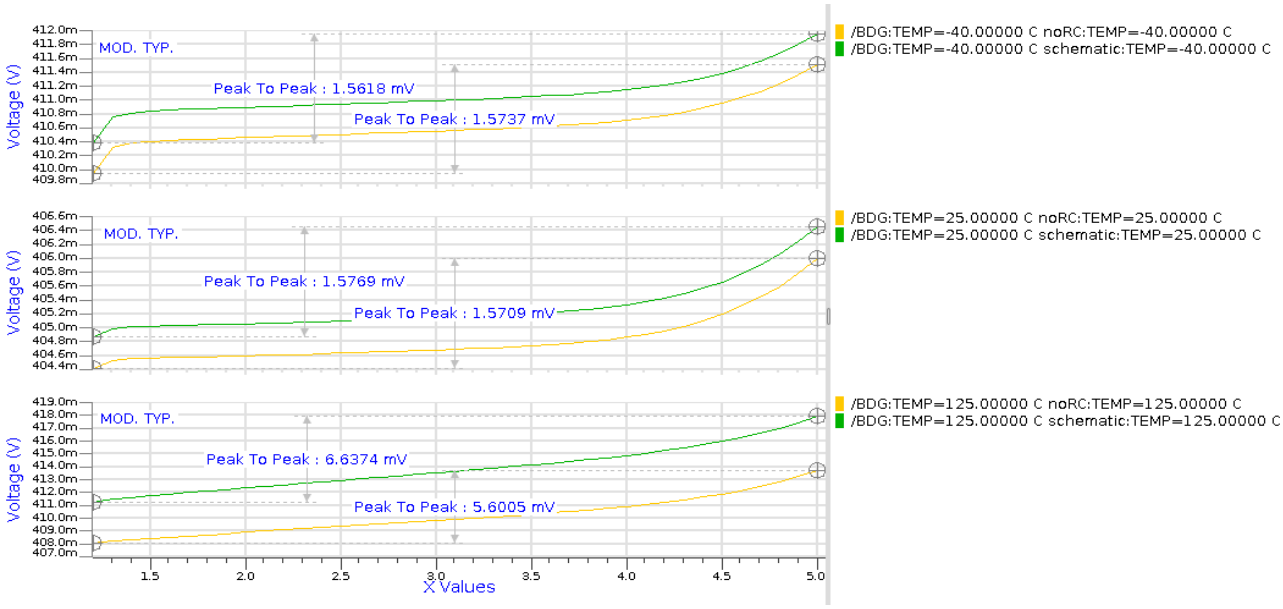


Fig. 33. Supply voltage dependence of the reference voltage for different value of temperature T (MOD. TYP.) reached at schematic (green curves) and layout level (yellow curves).

As already stated, the accuracy of the reference voltage is mainly affected by the variations on threshold voltage. These variations can be evaluated during the design making two different analyses: the effect of the mismatches on the accuracy of the reference voltage and the effect of the process variations on the reference voltage.

The impact of the mismatches on the reference has been investigated during the design and it has been mitigated by choosing large length value of the transistor in the core of the reference current section of the circuit. Simulation results at schematic level of the impact of the mismatch in terms of standard deviation on the reference voltage are shown in Fig. 34. The total standard deviation is given by the sum of the standard deviation of the threshold voltages of the transistors in the overall system. The simulated mean value of the reference voltage is 405.14 mV while the standard deviation due to the mismatch is only 1.19 mV which is the results of the optimized schematic.

```
#.DCMISMATCH  V(BDG) SORT_REL = 1.000000e-03 NSIGMA = 1.000000e+00

Analysis results:

Output DC value                     :     4.0514E-01 Volt
Total output deviation              : +/- 1.1897E-03 Volt
Output deviation due to the
contributors in the report table    : +/- 1.1897E-03 Volt
```

Fig. 34. Mismatch impact on the reference voltage at schematic level.

The impact of the mismatch on the reference voltage has been also evaluated at layout level and the obtained results are shown in Fig. 35. The mean value of the reference voltage is 404.68 mV while the standard deviation due to the mismatch is 1.19 mV thus proving that good layout rule allow to preserve schematic-level performances.

```
#.DCMISMATCH  V(BDG) SORT_REL = 1.000000e-03 NSIGMA = 1.000000e+00

Analysis results:

Output DC value                      :     4.0468E-01 Volt
Total output deviation               : +/- 1.1893E-03 Volt
Output deviation due to the
contributors in the report table     : +/- 1.1893E-03 Volt
```

Fig. 35. Mismatch impact on the reference voltage at layout level.

The effect of the process variation on the reference voltage has been evaluated by using the statistical model of the MOS transistors. At this purpose, Monte Carlo simulations of the reference voltage under 1000 iterations which involve both process and mismatch variations have been carried out. Fig. 36, 37 and 38 show the Gaussian distribution of the simulated reference voltage at different value of supply voltage (V_{DD} = 1.2 V, 3 V and 5 V) and temperature (T = –40 °C, 25 °C, 125 °C and 150 °C).

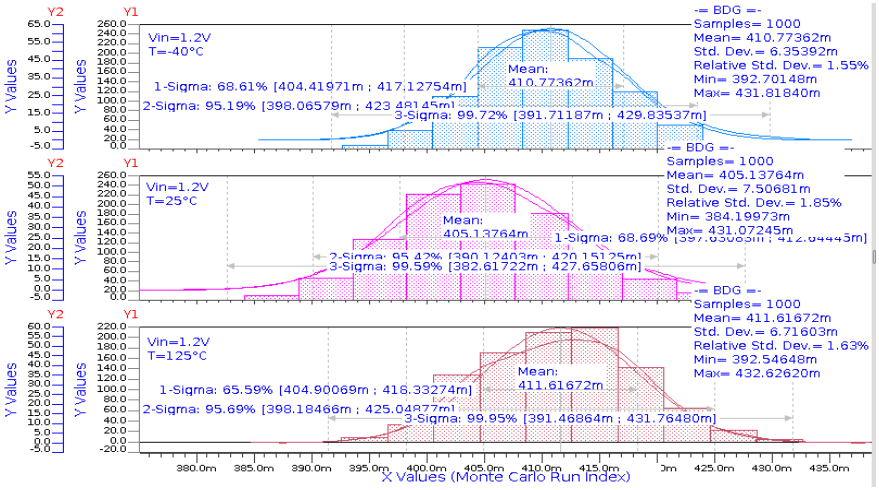


Fig. 36. Gaussian distribution of the reference voltage for different value of temperature (V_{DD} = 1.2 V).

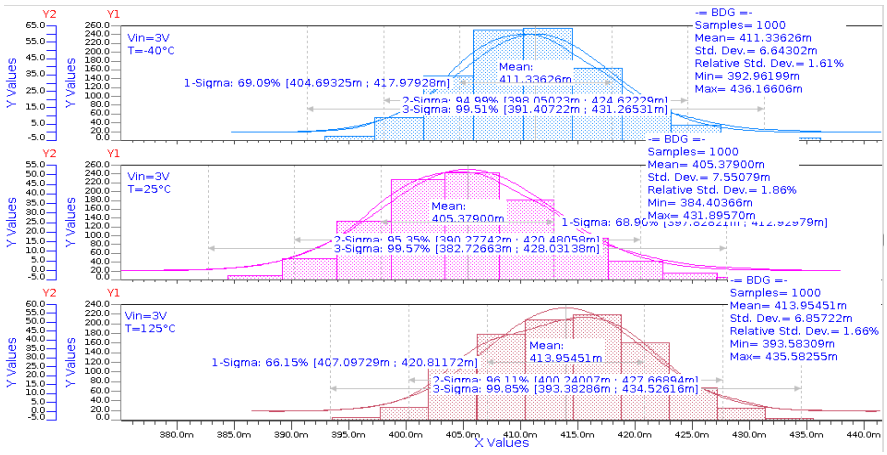


Fig. 37. Gaussian distribution of the reference voltage for different value of temperature (V_{DD} = 3 V).

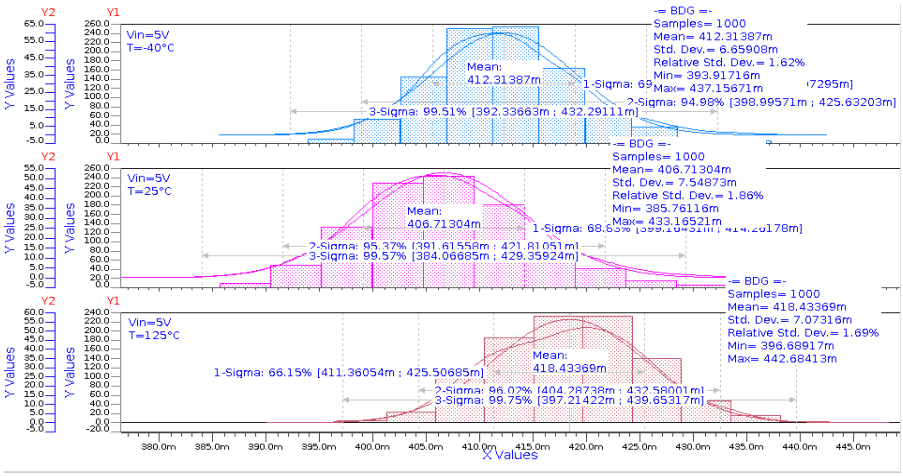


Fig. 38. Gaussian distribution of the reference voltage for different value of temperature (V_{DD} = 5 V).

The simulated standard deviation for different value of supply voltage and temperature are summarized in Table XVII. In the nominal condition the mean value of the reference voltage is 405.38 mV with a standard deviation of 7.55 mV. Anyway, the standard deviation is almost the same by varying supply voltage and temperature as shown in Table XVII.

TABLE XVII: Standard deviation of the reference voltage (process and mismatch variations).

σ (mV)	T = – 40 °C	T = 25 °C	T = 125 °C
V_{DD} = 1.2 V	6.35392	7.50681	6.71603
V_{DD} = 3 V	6.64302	7.55079	6.85722
V_{DD} = 5 V	6.65908	7.54873	7.07316

MonteCarlo simulations of the reference voltage at layout level at supply V_{DD} = 3 V and at different value of temperature (T = –40 °C, 25 °C, 125 °C and 150 °C) are shown in Fig. 39. At room temperature (T = 25 °C), the mean value of the reference voltage is 404.64 mV with a standard deviation of 7.20 mV. Once again, the impact of the process variation remains unaffected going from schematic to layout level.

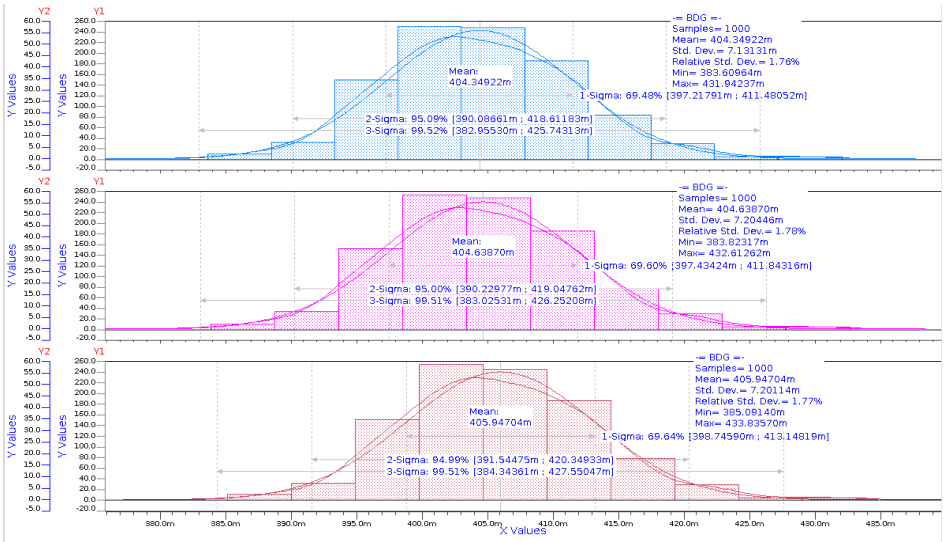


Fig. 39. Gaussian distribution of the reference voltage for different value of temperature at layout level (V_{DD} = 3 V).

Process variations are strongly affected by temperature variations thus having an impact on temperature behavior of the reference voltage. At this purpose, Monte Carlo simulations of the curvature in temperature have been carried out under 100 iterations. Fig. 40, 41 and 42 show the effect of both process and mismatch variations on the temperature behavior of the reference voltage for different value of supply voltage (V_{DD} = 1.2 V, 3 V and 5 V).

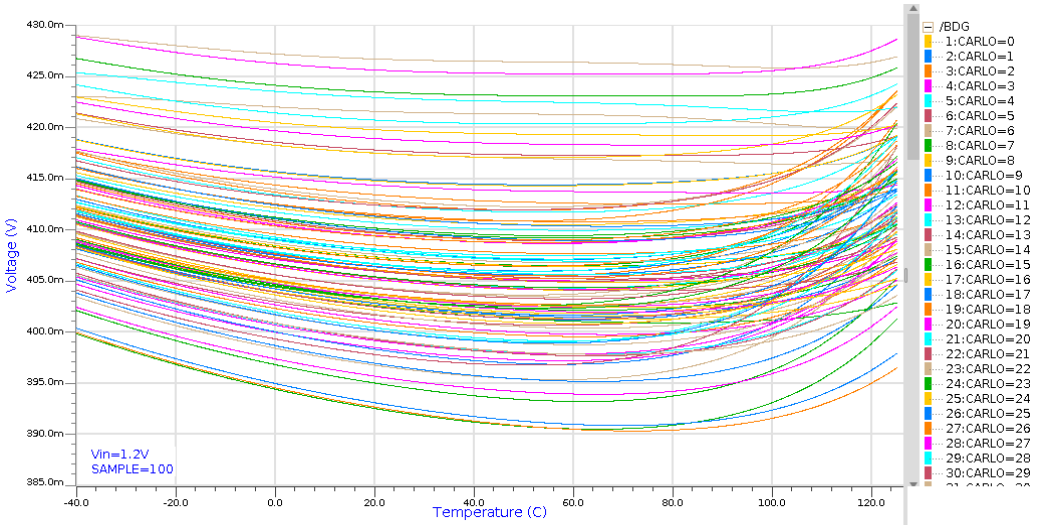


Fig. 40. Monte Carlo simulation result of the curvature in temperature of the reference voltage at V_{DD} = 1.2 V.

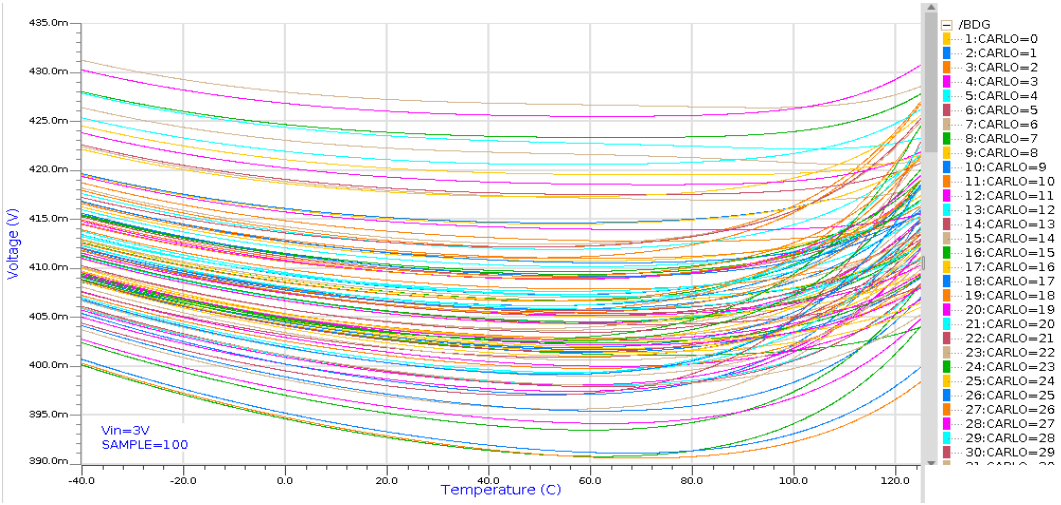


Fig. 41. Monte Carlo simulation result of the curvature in temperature of the reference voltage at V_{DD} = 3 V.

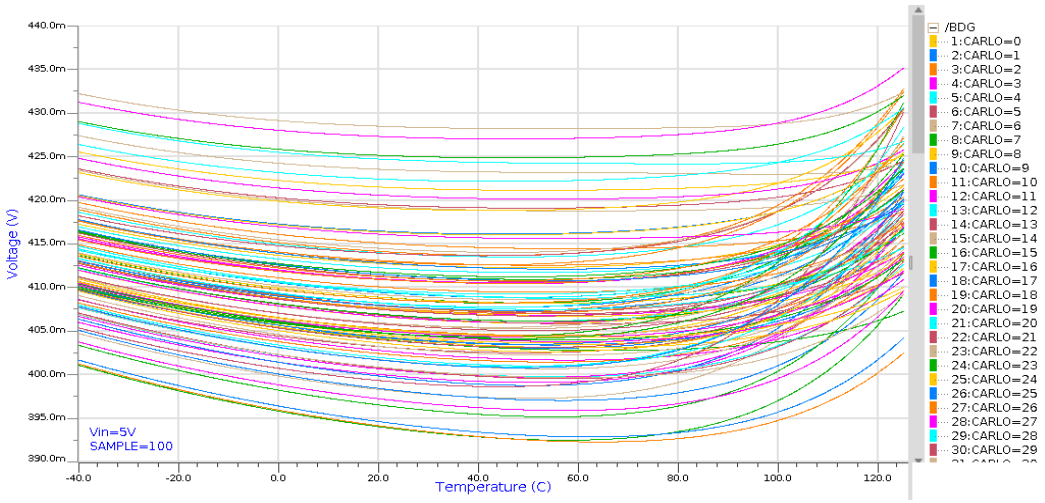


Fig. 42. Monte Carlo simulation result of the curvature in temperature of the reference voltage at V_{DD} = 5 V.

As expected, the reference voltage achieved by different samples is not always around the mean value due to the process variations. By inspection of Fig. 41, the variation of the reference voltage achieved by different sample change within the range of approximately 40 mV (from 390 mV to 420 mV). The design of trimming strategy on the active load was added with the purpose to fix the effects of the process variation on the reference voltage. The designed trimming strategy allow to reduce the drift in temperature by bringing all the samples around the mean value which is 421.6 mV. As already stated, the chosen accuracy of the least significant bit was fixed around 2 mV thus resulting in voltage reference variation of 0.5 %. Consequently, the accuracy achieved by the following bits $B_{1\text{-}4}$ is the multiple than the previous ones. The bit B_5 has been added to correct the sign and its accuracy is given by the sum of the accuracy given by bits $B_{0\text{-}4}$. Table XVIII summarized the accuracy of the bits in terms of both percentage and voltage variation.

TABLE XVIII: Accuracy on the reference voltage achieved with trimming bits.

BIT	**ΔV_{ref} (%)**	**ΔV_{ref} (mV)**
B_0	0.5287	2.22894
B_1	1.0834	4.56759
B_2	2.1158	8.920140001
B_3	4.2482	17.91023
B_4	8.4390	35.57869
B_5	–16.4555	–69.37582522

When the value reached by the reference voltage is far from the mean value, transistors in parallel into the active load can be added to the nominal ones to restore the mean value of the reference voltage. Parallel transistors can be enabled through trimming bit $B_{0\text{-}4}$ whose combination of the depend on the variations for what one wants to achieve. Table XIX summarized both the accuracy percentage and voltage variations which can be achieved by the combination of the six trimming bits. By inspection of Table XIX, it is evident that the addition of voltage variation ΔV_{ref} on the reference voltage V_{RFE} depending on the trimming bit combinations allow to always restore the mean value of 421.6 mV.

TABLE XIX: Accuracy percentage and voltage variations which can be achieved with the six trimming bits combination.

B5	B4	B3	B2	B1	B0	%	ΔVref (mV)	Vref
0	1	1	1	1	1	16.4151	69.20559	0.35239
0	1	1	1	1	0	15.8864	66.97665	0.35462
0	1	1	1	0	1	15.3317	64.63800	0.35696
0	1	1	1	0	0	14.8030	62.40906	0.35919
0	1	1	0	1	1	14.2993	60.28545	0.36131
0	1	1	0	1	0	13.7706	58.05651	0.36354
0	1	1	0	0	1	13.2159	55.71786	0.36588
0	1	1	0	0	0	12.6872	53.48892	0.36811
0	1	0	1	1	1	12.1669	51.29536	0.37030
0	1	0	1	1	0	11.6382	49.06642	0.37253
0	1	0	1	0	1	11.0835	46.72777	0.37487
0	1	0	1	0	0	10.5548	44.49883	0.37710
0	1	0	0	1	1	10.0511	42.37522	0.37922
0	1	0	0	1	0	9.5224	40.14628	0.38145
0	1	0	0	0	1	8.9677	37.80763	0.38379
0	1	0	0	0	0	8.4390	35.57869	0.38602
0	0	1	1	1	1	7.9761	33.62690	0.38797
0	0	1	1	1	0	7.4474	31.39796	0.39020
0	0	1	1	0	1	6.8927	29.05931	0.39254
0	0	1	1	0	0	6.3640	26.83037	0.39477
0	0	1	0	1	1	5.8603	24.70676	0.39689
0	0	1	0	1	0	5.3316	22.47782	0.39912
0	0	1	0	0	1	4.7769	20.13917	0.40146
0	0	1	0	0	0	4.2482	17.91023	0.40369
0	0	0	1	1	1	3.7279	15.71667	0.40588
0	0	0	1	1	0	3.1992	13.48773	0.40811
0	0	0	1	0	1	2.6445	11.14908	0.41045
0	0	0	1	0	0	2.1158	8.92014	0.41268
0	0	0	0	1	1	1.6121	6.79653	0.41480
0	0	0	0	1	0	1.0834	4.56759	0.41703
0	0	0	0	0	1	0.5287	2.22894	0.41937
0	**0**	**0**	**0**	**0**	**0**	**0.0000**	**0.00000**	**0.42160**
1	1	1	1	1	1	-0.0404	-0.17024	0.42177
1	1	1	1	1	0	-0.5691	-2.39918	0.42400
1	1	1	1	0	1	-1.1238	-4.73783	0.42633
1	1	1	1	0	0	-1.6525	-6.96677	0.42856
1	1	1	0	1	1	-2.1562	-9.09038	0.43069
1	1	1	0	1	0	-2.6849	-11.31932	0.43292
1	1	1	0	0	1	-3.2396	-13.65797	0.43525
1	1	1	0	0	0	-3.7683	-15.88691	0.43748
1	1	0	1	1	1	-4.2886	-18.08047	0.43968
1	1	0	1	1	0	-4.8173	-20.30941	0.44191
1	1	0	1	0	1	-5.3720	-22.64806	0.44424
1	1	0	1	0	0	-5.9007	-24.87700	0.44647
1	1	0	0	1	1	-6.4044	-27.00061	0.44860
1	1	0	0	1	0	-6.9331	-29.22955	0.45083
1	1	0	0	0	1	-7.4878	-31.56820	0.45316
1	1	0	0	0	0	-8.0165	-33.79714	0.45539
1	0	1	1	1	1	-8.4794	-35.74893	0.45735
1	0	1	1	1	0	-9.0081	-37.97787	0.45957
1	0	1	1	0	1	-9.5628	-40.31652	0.46191
1	0	1	1	0	0	-10.0915	-42.54546	0.46414
1	0	1	0	1	1	-10.5952	-44.66907	0.46627
1	0	1	0	1	0	-11.1239	-46.89801	0.46849
1	0	1	0	0	1	-11.6786	-49.23666	0.47083
1	0	1	0	0	0	-12.2073	-51.46560	0.47306
1	0	0	1	1	1	-12.7276	-53.65916	0.47526
1	0	0	1	1	0	-13.2563	-55.88810	0.47748
1	0	0	1	0	1	-13.8110	-58.22675	0.47982
1	0	0	1	0	0	-14.3397	-60.45569	0.48205
1	0	0	0	1	1	-14.8434	-62.57930	0.48418
1	0	0	0	1	0	-15.3721	-64.80824	0.48640
1	0	0	0	0	1	-15.9268	-67.14689	0.48874
1	0	0	0	0	0	-16.4555	-69.37583	0.49097
B5	B4	B3	B2	B1	B0	%	ΔVref (mV)	Vref

Transient response of the reference voltage has been evaluated with the aim to simulate how long the reference voltage takes to achieve the steady state value. In these simulations, turn-on evaluation was made by using the rise time which is the time taken by the reference voltage to rise from 10 % to 90 % of its final value. Turn-on times achieved at schematic level are summarized in Table XX, XXI and XXII in which the supply voltage V_{DD} was stepped from 0 V to 1.2 V, 3 V and 5 V by using all the transistor models and temperatures. Additionally, simulation results of the turn-on of the reference

voltage at the schematic level are shown in Fig. 43 in which the supply voltage was stepped from 0 to 3 V for different value of temperature and model. As expected, the slowest turn-on time is achieved by using the minimum value of supply voltage, lower temperature, and MIN. model. However, the nominal value of the turn-on time is quite good, and its value is 1.91 μs.

TABLE XX: Turn-on time of the reference voltage for different supply voltage and models (T = 25 °C).

Turn-on time (μs)	MOD. TYP.	MOD. MAX.	MOD. MIN.
V_{DD} = 1.2 V	278.47	7.50681	6.71603
V_{DD} = 3 V	1.9108	98.826	1.5706
V_{DD} = 5 V	1.1814	1.7685	1.0223

TABLE XXI: Turn-on time of the reference voltage for different supply voltage and models (T = – 40 °C).

Turn-on time (μs)	MOD. TYP.	MOD. MAX.	MOD. MIN.
V_{DD} = 1.2 V	517.08	130.51	1078.3
V_{DD} = 3 V	1.7341	75.704	1.5147
V_{DD} = 5 V	1.0463	1.5165	0.9352

TABLE XXII: Turn-on time of the reference voltage for different supply voltage and models (T = 125 °C).

Turn-on time (μs)	MOD. TYP.	MOD. MAX.	MOD. MIN.
V_{DD} = 1.2 V	263.04	163.65	490.58
V_{DD} = 3 V	2.5061	116.11	1.892
V_{DD} = 5 V	1.5069	2.2088	1.2422

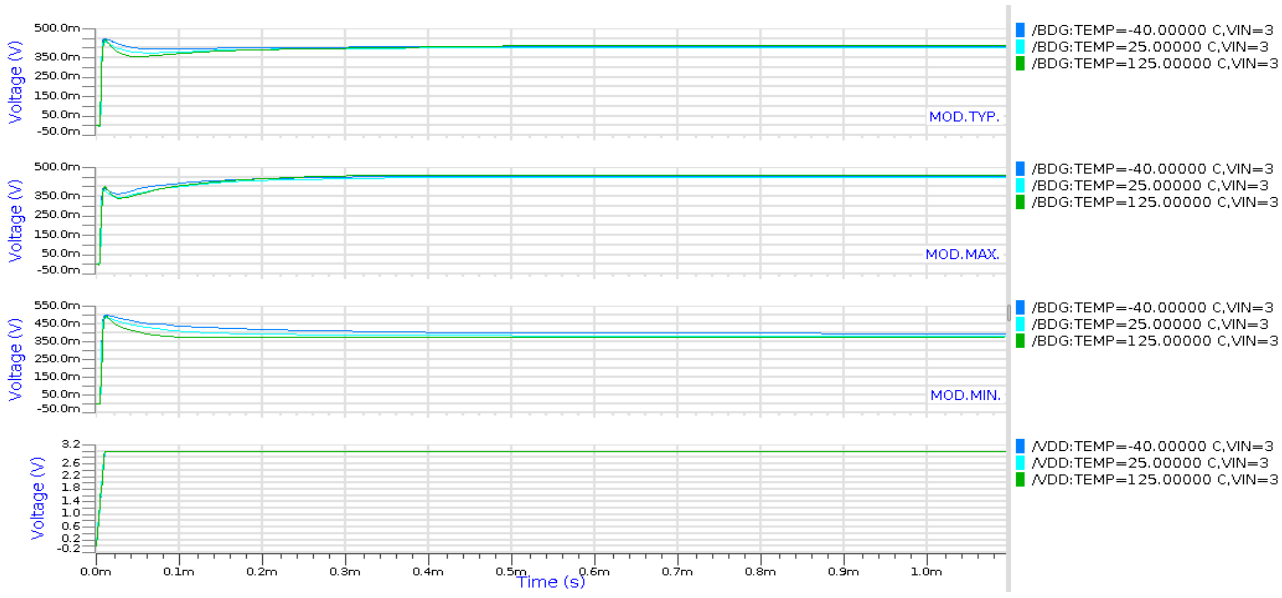


Fig. 43. Turn-on of the reference voltage at the schematic level for different value of temperature and model (the supply voltage step from 0 to 3 V).

Transient response of the reference voltage was repeated at layout level and under the following condition: supply voltage step from 0 V to 3 V, room temperature (T = 25 °C) and TYP. MOD. the turn-on time achieved is equal to 1.98 μs. The value achieved a layout level is approximately equal

to than achieved at schematic level proving that proper design and good layout rule allow to maintain the same time behavior.

Additionally, time behavior of the reference circuit has been investigated by analyzing the transient line regulation of the reference voltage. This type of transient response concerns the analysis of the undershoot and overshoot of the reference voltage that occurs when the supply voltage is stepped above 1 V than the chosen one and vice-versa. To give an example, Fig. 44 shows the transient line regulation of the reference voltage by stepping the supply voltage from 3 V to 4 V and vice-versa for different temperature and model.

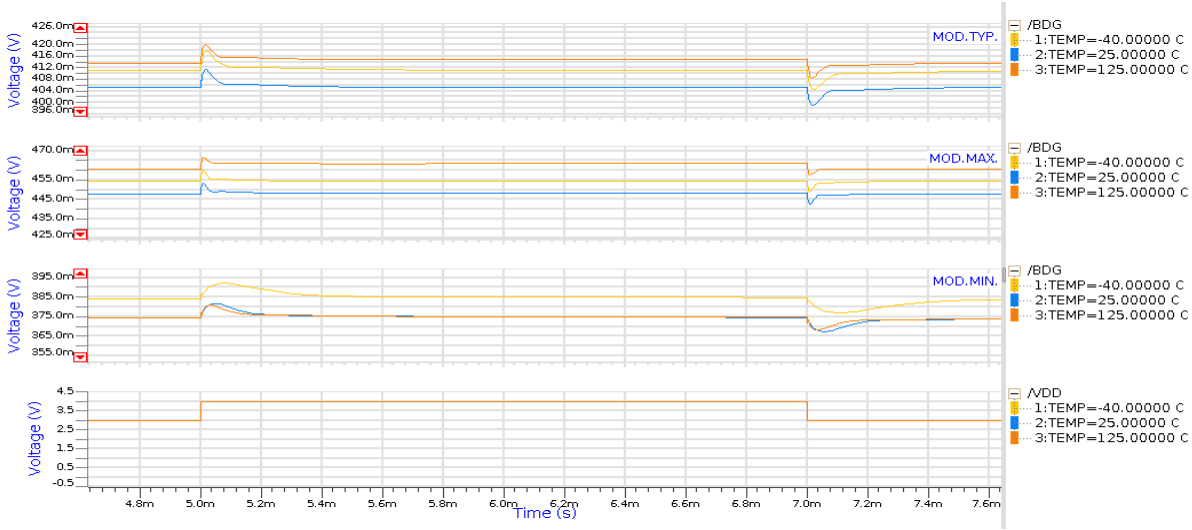


Fig. 44. Transient line regulation of the reference voltage for different temperature and model (supply voltage step from 3 V to 4 V).

This analysis was carried out by setting the rise time and the fall time of the step on the supply voltage equal to 1 μs, as shown in Fig. 45 with regards to the nominal condition. This allows to demonstrate how much is the overshoot and undershoot of the reference voltage compared to the steady state value during the transient line regulation. At room temperature, the overshoot is 6.3354 mV while the overshoot is 5.79782 mV.

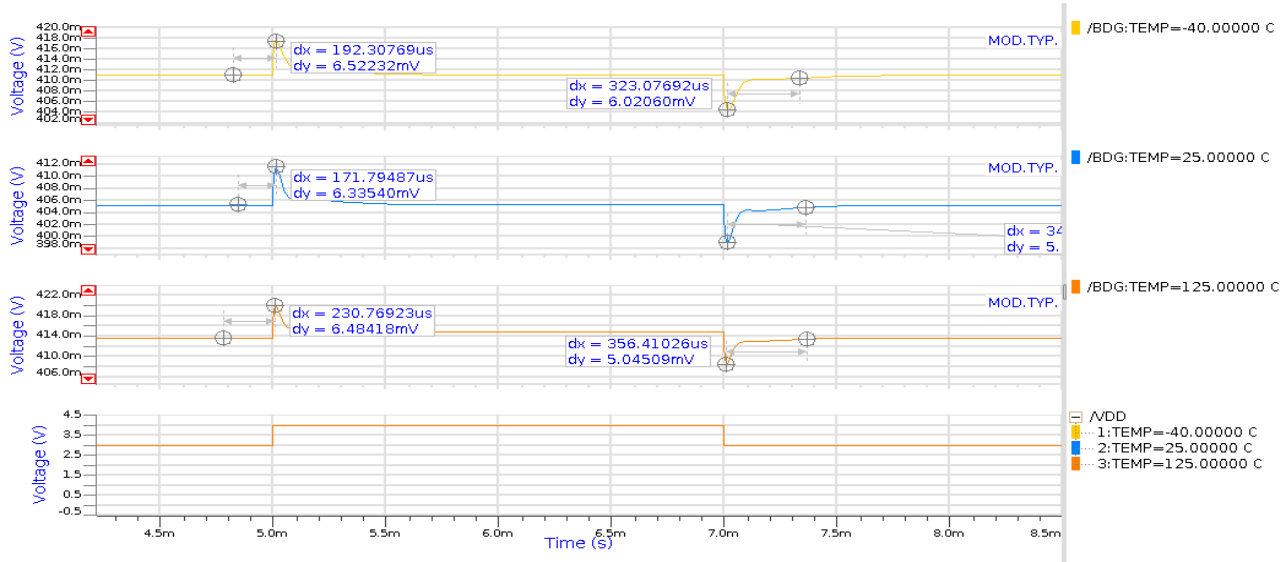


Fig. 45. Transient line regulation of the reference voltage for different temperature and MOD. TYP. (supply voltage step from 3 V to 4 V).

The comparison between the transient line regulation of the reference voltage achieved at schematic (green) and layout (yellow) level (MOD. TYP.) for different value of temperature are shown in Fig. 46 in which the differences between the achieved undershoot and overshoot values are also

highlighted. At room temperature, the difference between the two overshoot voltage is 2.44 mV while the difference between the two undershoot voltage is 3.11 mV. Although a slight variation, the post-layout simulations confirm what has been achieved at schematic level.

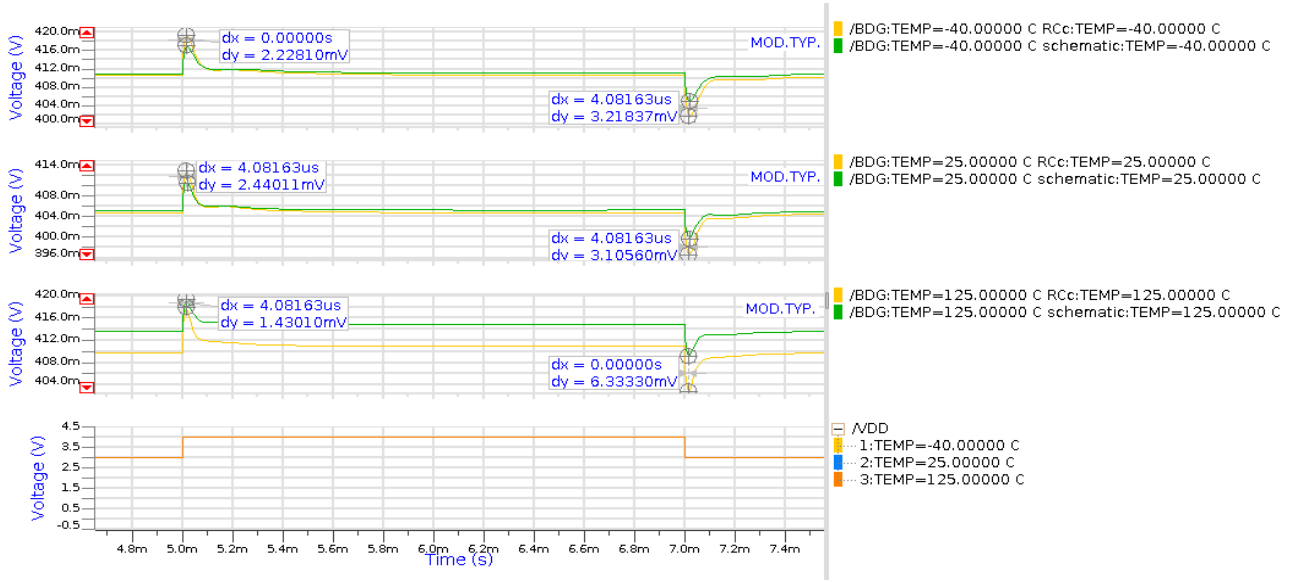


Fig. 46. Comparison between the transient line regulation of the reference voltage achieved at schematic and layout level for different value of temperature (supply voltage step from 3 V to 4 V and MOD. TYP.).

Additional simulations concerning the supply voltage rejection and the spectral output noise have been also carried out. These simulations were made with the only aim to show the voltage reference behavior with respect of these two performance parameters without taking into account any kind of improvement during the design phase.

Supply voltage rejection (SVR) for different value of supply voltage, temperature and model are shown in Fig. 47, 48. and 49. in which the SVR at different value of frequency (1 kHz, 100 kHz and 1 MHz) are highlighted. The SVR values at different frequency and supply voltage achieved at room temperature are summarized in Table XXIII. In the nominal condition the SVR values at different frequency 1 kHz, 100 kHz and 1 MHz are –51.91 dB, –57.60 dB and –42.63 dB, respectively.

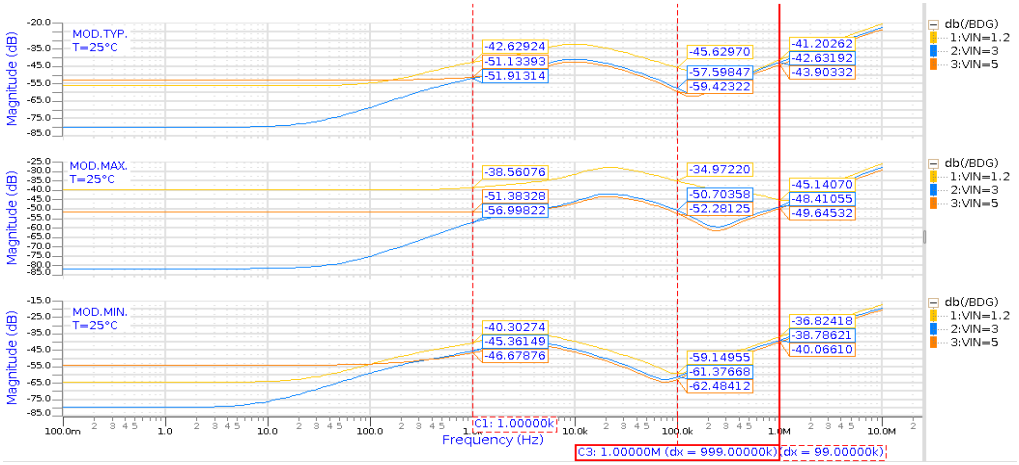


Fig. 47. SVR for different value of supply voltage and model (T = 25 °C).

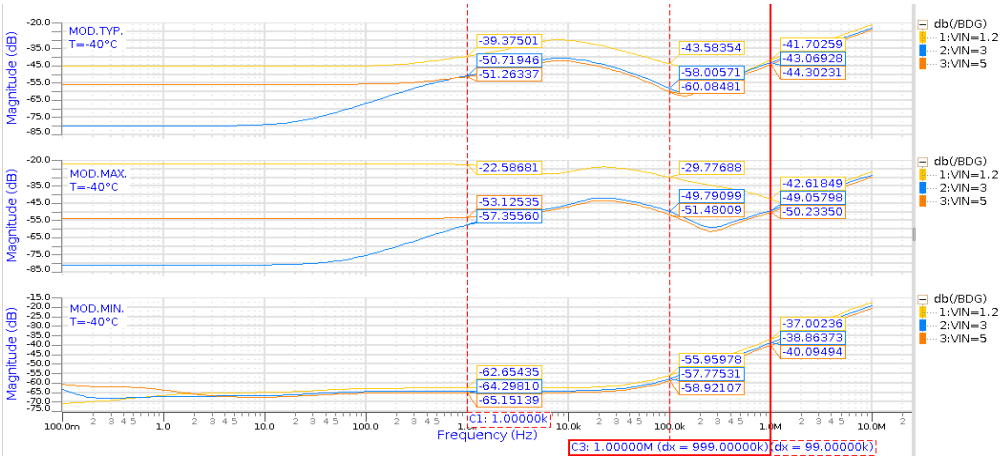


Fig. 48. SVR for different value of supply voltage and model (T = – 40 °C).

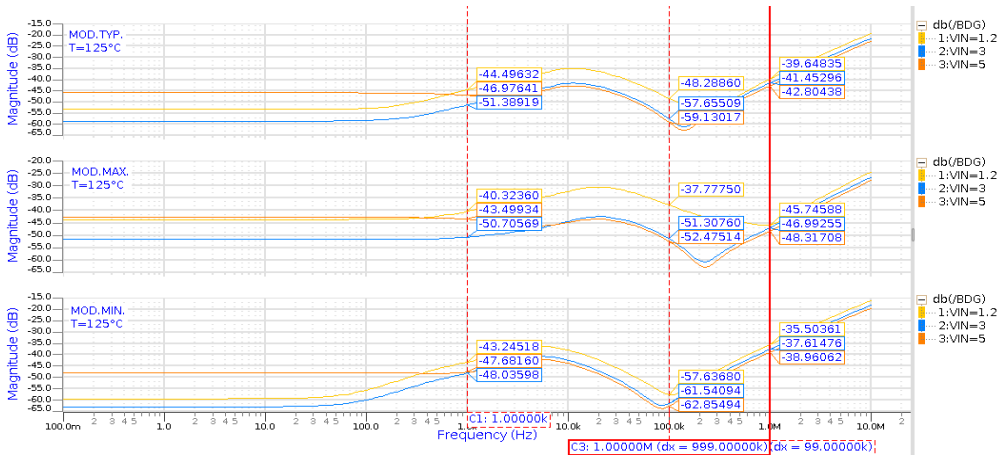


Fig. 49. SVR for different value of supply voltage and model (T = 125 °C).

TABLE XXIII: The SVR values at different frequency and supply voltage (T = 25 °C).

SVR (dB)	MOD.TYP.	MOD.MAX.	MOD.MIN.
V_{DD} = 1.2V f = 1kHZ	–42.62924	–38.56076	–40.30274
V_{DD} = 1.2V f = 100kHZ	–45.6297	–34.9722	–59.14955
V_{DD} = 1.2V 1MHz	–41.20262	–45.1407	–36.82418
V_{DD} = 3 V f = 1kHZ	–51.91314	–56.99822	–45.36149
V_{DD} = 3 V f = 100kHZ	–57.59847	–50.70358	–61.37668
V_{DD} = 3 V f = 1MHZ	–42.63192	–48.41055	–38.78621
V_{DD} = 5 V f = 1kHZ	–51.13393	–51.38328	–46.67876
V_{DD} = 5 V f = 100kHZ	–59.42322	–52.28125	–62.48412
V_{DD} = 5 V f = 1MHZ	–43.90332	–49.64532	–40.0661

Comparison between the SVR achieved at schematic and layout level are shown in Fig. 50 for different value of supply voltage at room temperature by adopting the typical model of the transistor while all the SVR values achieved at layout level are summarized in Table XXIV. In the nominal condition the SVR values at different frequency are: –49.88 dB instead of –52.90 at 1 kHz, –49.22dB instead of –55.68 at 100 kHz and –48.88 dB instead of –51.08 at 1 MHz.

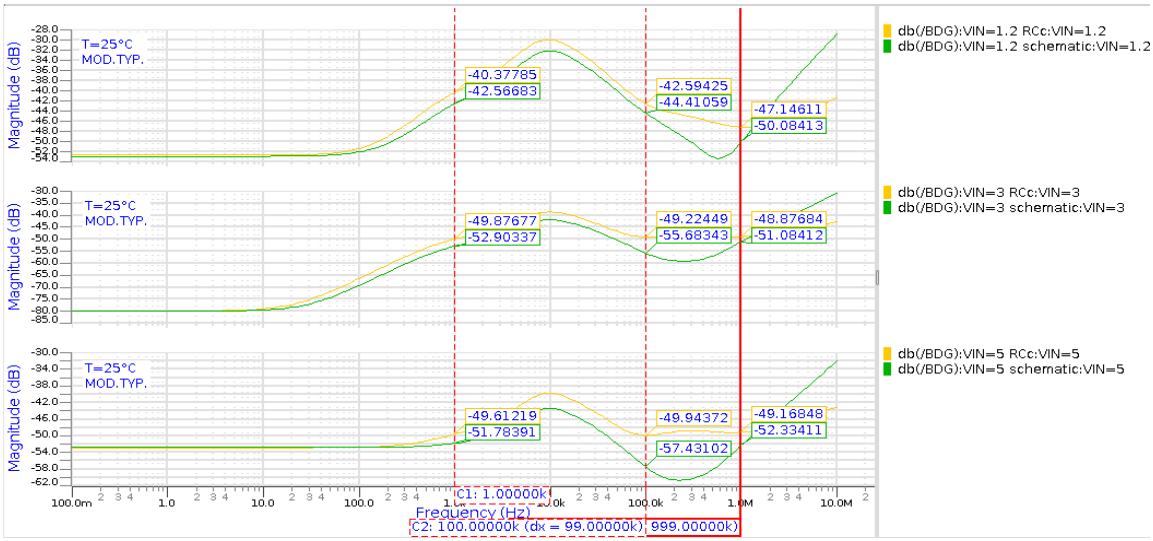


Fig. 50. Comparison between the SVR achieved at schematic and layout level for different value of supply voltage (T = 25 °C and MOD. TYP.).

TABLE XXIV: SVR values at layout level for different value of supply voltage (T = 25 °C and MOD. TYP.).

SVR (dB)	***MOD.TYP. (T = 25 °C)***
V_{DD} = 1.2V f = 1kHZ	–40.37785
V_{DD} = 1.2V f = 100kHZ	–42.59425
V_{DD} = 1.2V 1MHz	–47.14611
V_{DD} = 3 V f = 1kHZ	–49.87677
V_{DD} = 3 V f = 100kHZ	–49.22449
V_{DD} = 3 V f = 1MHZ	–48.87684
V_{DD} = 5 V f = 1kHZ	–49.61219
V_{DD} = 5 V f = 100kHZ	–49.61219
V_{DD} = 5 V f = 1MHZ	–49.16848

The behavior of the spectral output noise for different value of supply voltage, temperature and model is shown in Fig. 51 while the achieved output noise values at different conditions are summarized in Table XXV, Table XXVI and XXVII. Under nominal condition, the value of the spectral noise is equal to 57.783 µVrms.

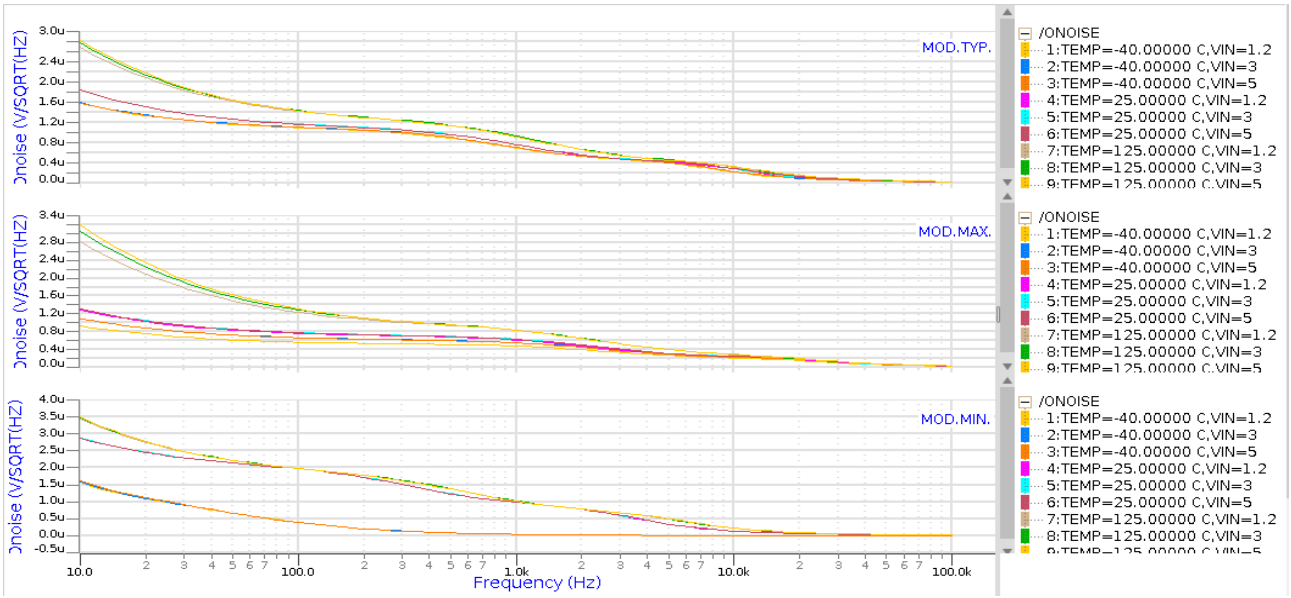


Fig. 51. Spectral output noise for different value of supply voltage, temperature, and model.

TABLE XXV: Spectral output noise for different supply voltage and model (T = 25 °C).

Output noise (µVrms)	MOD.TYP.	MOD.MAX.	MOD.MIN.
V_{DD} = 1.2V	56.997	50.212	63.619
V_{DD} = 3V	57.783	52.017	64.012
V_{DD} = 5V	57.738	51.944	63.993

TABLE XXVI: Spectral output noise for different supply voltage and model (T = – 40 °C).

Output noise (µVrms)	MOD.TYP.	MOD.MAX.	MOD.MIN.
V_{DD} = 1.2V	51.353	41.548	8.3758
V_{DD} = 3V	52.572	46.995	8.3996
V_{DD} = 5V	52.57	46.956	8.4359

TABLE XXVII: Spectral output noise for different supply voltage and model (T = 125 °C).

Output noise (µVrms)	MOD.TYP.	MOD.MAX.	MOD.MIN.
V_{DD} = 1.2V	66.007	63.021	72.406
V_{DD} = 3V	67.546	64.637	72.465
V_{DD} = 5V	67.354	64.361	72.706

A comparison between the spectral output noise achieved at schematic (green) and layout (yellow) level is shown in Fig. 52 where different value of supply voltage and the typical model of the transistors have been adopted. Under nominal condition, the value of the spectral noise achieved at

layout level is equal to 59.04 µVrms instead of 57.783 µVrms which is the value achieved at schematic level.

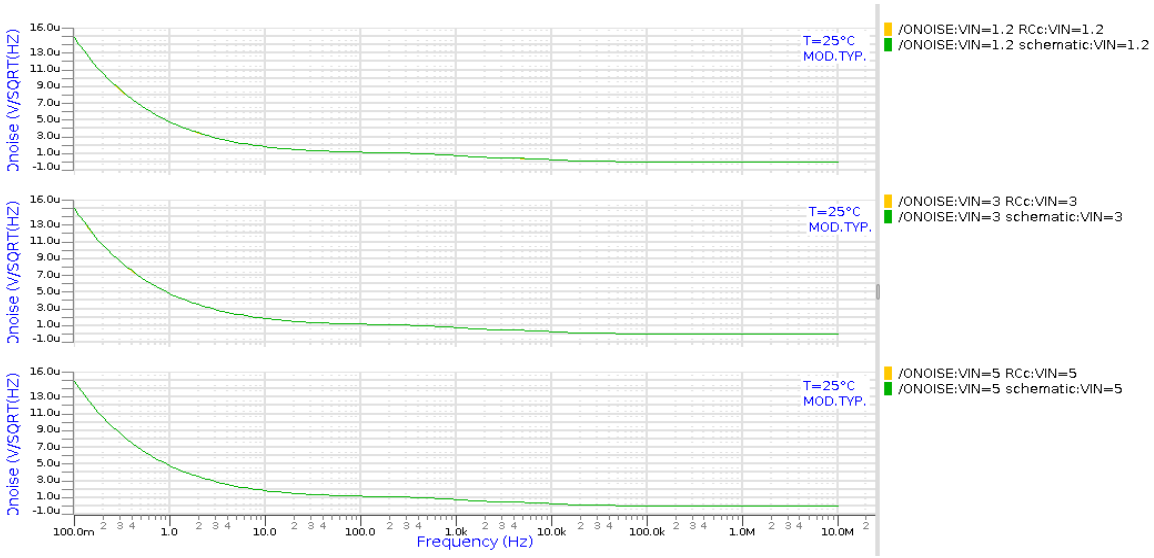


Fig. 52. Comparison between the spectral output noise achieved at schematic (green) and layout (yellow) level for different value of supply voltage (T = 25 °C and MOD. TYP.).

At the end, the frequency response of the voltage reference has been also evaluated only at schematic level for different value of supply voltage, temperature and model as shown in Fig. 53, 54 and 55 in which the phase margin and the gain crossover (which is the gain-bandwidth product) are highlighted. The simulation results show the stability of the circuit thanks to the achieved phase margin greater than 70 dB in all conditions. Anyway, in the nominal condition the phase margin is equal to 85 dB whit a gain-bandwidth product equal to 9 kHz.

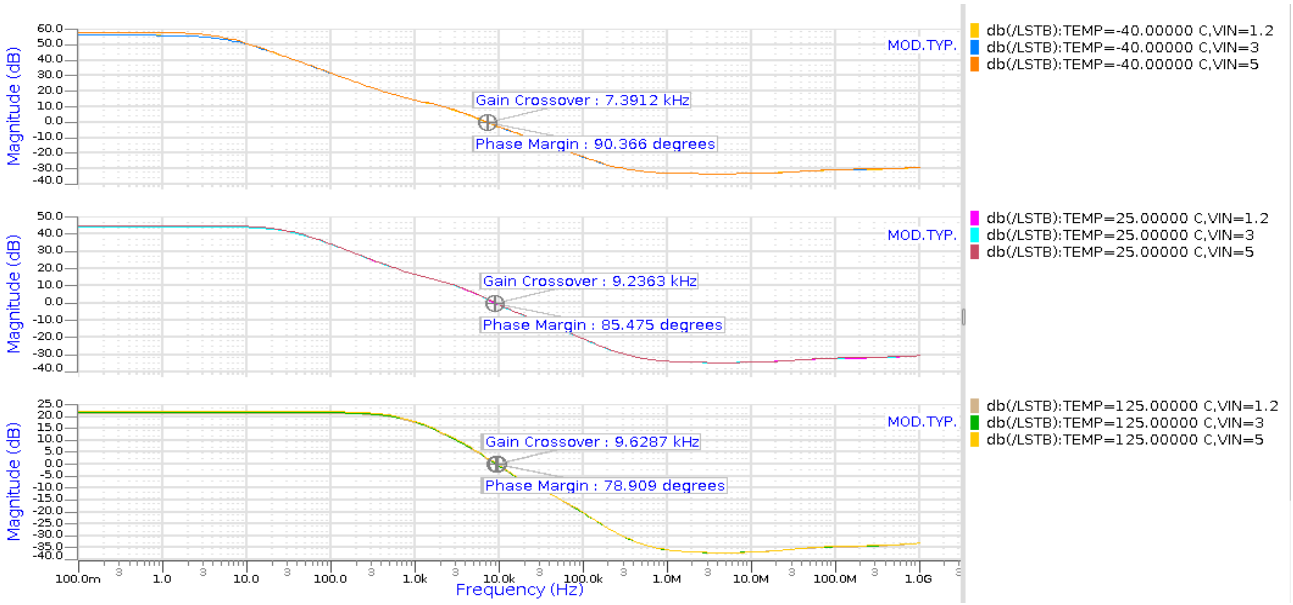


Fig. 53. Frequency response of the voltage reference for different value of supply voltage and temperature (MOD. TYP.).

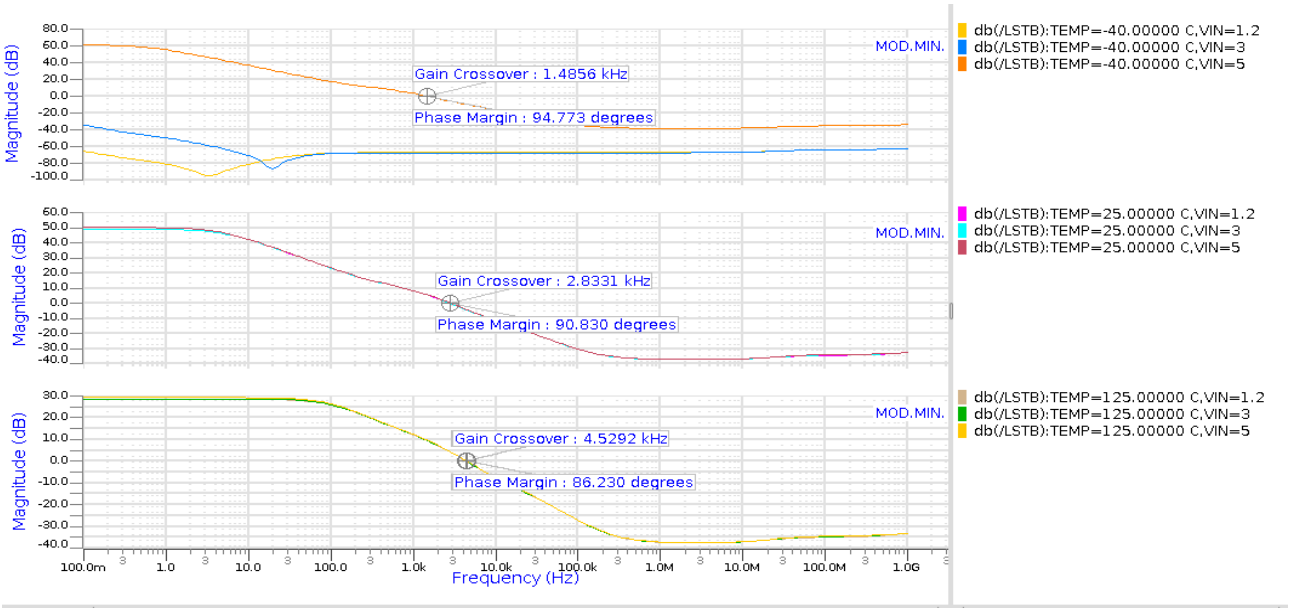


Fig. 54. Frequency response of the voltage reference for different value of supply voltage and temperature (MOD. MIN.).

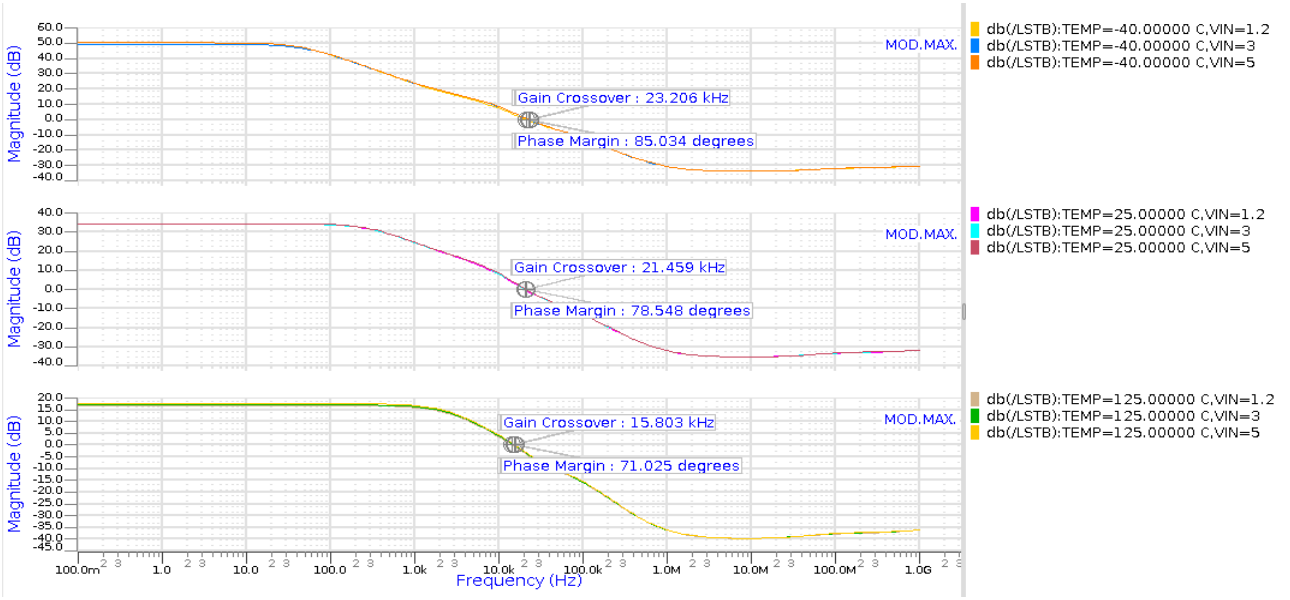


Fig. 55. Frequency response of the voltage reference for different value of supply voltage and temperature (MOD. MAX.).

All the performances of the proposed ultra-low power voltage reference that has been discussed above are summarized in Table XXVIII. Extensive simulation results at schematic and post-layout level shall be divided as follows: (1) simulation results achieved in the nominal condition of supply voltage, temperature and model are categorized as Typ., (2) minimum values obtained by considering all conditions in terms of supply voltage, temperature and model are categorized as Min., and (3) maximum values obtained by considering all conditions in terms of supply voltage, temperature and model are categorized as Max..

TABLE XXVIII: Proposed ultra-low power voltage reference performance.

SYMBOL	PARAMETER	TEST CONDITION: supply voltage VDD (V), temperature T (°C), frequency f (Hz)	Unit	Simulation results Pre - Layout			Simulation results Post - Layout		
				Min.	Typ.	Max.	Min.	Typ.	Max.
VDD	Operating input voltage		V	1.2	3	5	1.2	3	5
Iq	Quiescent Current	VDD = 1.2 V, 3 V, 5 V @ T = 25 °C	nA	9.44704	41.56835	137.49422		41.42416	
		VDD = 1.2 V, 3 V, 5 V @ T = −40 °C	nA	3.56353	25.04757	117.38	3.54197	24.9336	
		VDD = 1.2 V, 3 V, 5 V @ T = 125 °C	nA	24.87911	75.31036	200.85534		72.61434	
		VDD = 1.2 V, 3 V, 5 V @ T = 150ºC	nA	32.60079	95.45009	274.85864		93.32481	255.9722
Vref	Reference Voltage	Vref @ T = 25 °C, VDD = 1.2 V, 3 V, 5 V	V	0.3742421	0.40514486	0.44942314	0.37382412	0.40468271	0.44884088
		σ @ T = −40 °C, VDD = 1.2 V, 3 V, 5 V	mV	6.35392	6.64302	6.65908		6.32467	
		σ @ T = 25 °C, VDD = 1.2 V, 3 V, 5 V	mV	7.50681	7.55079	7.55079		7.20446	
		σ @ T = 125 °C, VDD = 1.2 V, 3 V, 5 V	mV	6.71603	6.85722	7.07316		6.45153	
T range	Temperature Range	VDD = 1.2 V, 3 V, 5 V	ºC	-40	25	125	-40	25	125
TC	Temperature Coefficent	VDD = 1.2 V, 3 V, 5 V	ppm / ºC	106.94	137.34	274.87		102.01	
LS	Static line regulation	1.2 V ≤ VDD ≤ 5V, T = 25 °C	%/V	0.09883	0.10102	0.110206		0.10215	
		1.2 V ≤ VDD ≤ 5V, −40 °C ≤ T ≤ 125 °C	%/V	0.096301	0.10102	0.73373	0.0752	0.10215	0.67597
Vref variations (overshoot and undershoot)	Transient Line Regulation	VDD = 1.2 V to 2.2 V and vice-versa , tr = tf = 1 µs		9.60559 | 6.10086	9.84204 | 9.53447	12.0032 | 10.31369	10.92738 | 7.76742	11.46934 | 11.15936	14.38594 | 12.13504
		VDD = 3 V to 4 V and vice-versa , tr = tf = 1 µs	mV	5.57684 | 3.3461	6.3354 | 5.79782	7.93217 | 6.85737	7.20307 | 5.01035	8.35871 | 8.15483	10.26991 | 9.47992
Ton	Turn on time	10 % < Vref < 90 %, VDD = 1.2 V, 3 V, 5 V @ T= 25 °C	µs	1.0223	1.9108	682.24		1.9817	
		10 % < Vref < 90 % , VDD = 1.2 V , 3 V, 5 V @ T = −40 °C	µs	0.9352	1.7341	1078.3	0.97182	1.8273	988.51
		10 % < Vref < 90 %, VDD = 1.2 V, 3 V, 5 V @ T = 125 °C	µs	1.2422	2.5061	490.58		2.5361	
SVR	Supply Voltage Rejection	VDD = 3 V, f = 1 kHz, T = 25 °C	dB	-45.36149	-51.91314	-56.99822		-49.87677	
		VDD = 3 V, f = 100 kHz, T = 25 °C	dB	-50.70358	-57.59847	-61.37668		-49.22449	
		VDD = 3 V, f = 1 MHz, T = 25 °C	dB	-38.78621	-42.63192	-48.41055		-48.87684	
		VDD = 1.2 V, f = 1 kHz, T = 25 °C	dB	-38.56076	-42.62924	-42.62924		-40.37785	
		VDD = 1.2 V, f = 100 kHz, T = 25 °C	dB	-34.9722	-45.6297	-59.14955	33.60825	-42.59425	
		VDD = 1.2 V, f = 1 MHz, T = 25ºC	dB	-36.82418	-41.20262	-45.1407		-47.14611	
		VDD = 5 V, f = 1 kHz, T = 25 °C	dB	-46.67876	-51.13393	-51.38328		-49.61219	
		VDD = 5 V, f = 100 kHz, T = 25 °C	dB	-52.28125	-59.42322	-62.48412		-49.61219	-49.45156
		VDD = 5 V, f = 1 MHz, T = 25 °C	dB	-40.0661	-43.90332	-49.64532		-49.16848	
eN	Output noise voltage	1.2 V ≤ VDD ≤ 5 V, −40 °C ≤ T ≤ 125°C, 10 Hz < f < 100kHz	µVrms	8.3758	57.783	72.706	58.748	59.039	74.428
Die area	Die area		mm2					0.04318	

2.5.9 Comparison With the State of Art

The proposed ultra-low power voltage reference can be compared with the other architecture taken from the state of art already analyzed in the previous paragraph and summarized in Table II. Therefore, the performance of the proposed voltage reference can be added to earlier ones with the aim to make an extensive table of comparison (Table XXIX). Since the proposed solution is realized only by using MOS transistor and it is based on the difference between threshold voltages, it has been added to the category indicated as MOS (V_{TH} differences).

The proposed solution represents the only one able to cover both the widest range of supply voltage and temperature which are [1.2 ÷ 5] V and [–40÷125] °C, respectively. The greatest goal of this proposed solution besides of having reached a small value of Line Sensitivity (LS) which is 0.102 %/V with a supply voltage variation of 3.8 V. A value of LS smaller than this one has been achieved in literature only with smaller value of supply voltage. The analysis of the LS based only on its value worth nothing if its value is not compared to the supply voltage range. Therefore, one could say that a good value of LS is reached not when its value is the smallest one but when it is at the same time small, and it is included in a wide range of supply voltage.

The consideration made for the LS can be also done for the Temperature Coefficient (TC). Once again, smaller value of TC worth nothing if its value is not compared to the temperature range and consequently a good TC is not the smallest one but the small one in a wide range of temperature.

The proposed solution shown a TC equal to 102 ppm/°C in the temperature range [–40÷125] °C. The reached value is not the smallest one as it can be seen by inspection of Table XXIX. Smallest TC has been achieved in literature by considering small temperature range that [–40÷125] °C or by using high value of supply current. To conclude, the TC achieved by the proposed solution is not the smallest one achieved in literature but at the same time is the only one that is achieved with the smaller supply current which is less than 42 nA by considering the widest range of temperature.

Good result besides in the achieved values of both reference voltage and minimum supply current which are 404.68 mV and 41.318 nA respectively. This means that the proposed solution is the only one in literature able to reach the highest value of reference voltage with the smallest supply current.

Additionally, it can be noted that the value of the current is almost the same by varying the supply voltage thus obtaining 41.38 nA when the supply voltage is 1.2 V and 41.85 nA when the supply voltage is 5 V. This means that this proposed solution works properly over a wide range of supply voltage without changing the value of the supply current.

TABLE XXIX: Comparison with low voltage and low-power voltage references.

Reference	23	18	20	19	21	22	24	This work*	25	29	26	27	28	30	31	32	33
Year	2007	2011	2012	2013	2013	2018	2015	2023	2021	2006	2009	2012	2018	2015	2019	2019	2019
Type	MOS (VTH difference)	MOS (VTH difference)	MOS (VTH difference)	MOS (VTH difference)	MOS (VTH difference)	MOS (VTH difference)	MOS (bulk-driven)	MOS (VTH difference)	MOS (body-biased)	MOS (other)	MOS (other)	MOS (other)	MOS (other)	MOS+BJT	MOS+BJT	MOS+BJT	MOS+RES
Technology (nm)	350	180	130	180	180	180	180	160	180	350	350	90	180	130	180	180	180
Minimum VDD (V)	0.9	0.45	0.5	0.6	0.45	0.6	0.45	1.2	0.25	1.5	1.4	1.6	0.45	0.9	1	0.9	0.7
VDD (V)	0.9 to 4	0.45 to 2	0.5 to 3	0.6 to 1.8	0.45 to 1.8	0.6 to 2	0.45 to 1.8	1.2 to 5	0.25 to 1.8	1.5 to 4.3	1.4 to 3	1.6 to 3.6	0.45 to 2.4	0.9 to 1.2	1 to 1.8	0.9 to 3.3	0.7 to 2
Current consumption (nA)	40@0.9V 55@4V	7@0.45V 8@1.8V	0.0044@0.5V	37@0.6V 37@1.8V	0.089@0.45V 0.1@1.8V	50.8@0.6V	32@0.45V	41.38@1.2 V 41.85@5V	0.02@0.25V 0.02@1.8V	80@1.5V 110@4.3V	214@1.4V	68@1.6V 173@3.6V	7@2.4V	39@0.9V	0.192@ 1V	0.035@0.9V 0.041@3.3V	40@0.7V
Power (nW)	36@0.6V 220@4V	3.15@0.45V 14.4@1.8V	0.0022@0.5V	22.2@0.6V 22.2@1.8V	0.040@0.45V 0.18@1.8V	30.5@0.6V	14.4@0.45V	49.66@1.2 V 209.25@5V	0.005@0.25V 0.042@1.8V	120@1.5V 473@4.3V	300@1.4V	109@1.6V 623@3.6V	16.8@2.4V	35@0.9V	0.192@ 1V	0.0314@0.9V 0.134@3.3V	28@0.7V
Minimum Power (nW)	36	3.15	0.0022	22.2	0.04	30..5	14.4	49.66	0.005	120	300	109	16.8	35	0.192	0.0314	28
Vref (mV)	670	263.5	176.8	259	275.4	218.3	118.5	404.68	91.4	891.1	754	771	263.5	559	693	740	368
Temperature range (°C)	[0÷80]	[0÷125]	[−20÷80]	[0÷125]	[0÷120]	[−20÷125]	[−40÷125]	[−40÷125]	[0÷120]	[0÷80]	[−20÷80]	[−40÷125]	[0÷125]	[0÷125]	[−20÷100]	[0÷170]	[−40÷125]
TC (ppm/°C)	10	142	124	462	105.4	23.5	63.6	102	265	12	7	7.5	142	83	33	27	43.1
Line sensitivity (%/V)	0.27	0.44	0.033	0.065	0.46	0.4	8.77	0.102	0.16	0.46	0.002	1.65	0.44	1.33	0.02	0.27	0.027
PSRR (dB)	−47@100Hz −40@10kHz	−45@100Hz −12@10MHz*	−53@100Hz −62@10MHz	−44@100Hz* −43.3@10MHz*	−48@100Hz −29.2@10kHz	−42.4@100Hz −42.3@10MHz	−44.2@100Hz	−49.88@1kHz −49.88@1MHz	−70@ 100Hz	−59@100Hz −52@10MHz	−45@100Hz	–	--	−41@100Hz*	−55@100Hz	–	−59@10Hz −39@1MHz
Die Area (mm2)	0.045	0.043	0.00135	0.0298	0.018	0.075	0.012	0.04318	0.0022	0.015	0.055	0.03	0.043	0.0022	0.0045	0.0076	0.055

Furthermore, a comprehensive analysis can be done by adding the proposed solution to the comparison previously shown in Fig. 18 and 19. LS and TC as a function of the minimum power consumption are shown in Fig. 56 and 57, respectively. As already stated, the proposed solution represents a good trade-off between both LS and TC and minimum power consumption if compared with the other solution taken from the state of art. Although the power consumption is not the smallest one, the LS achieved with the proposed reference lies among the smallest achieved ones. At the same time, the proposed reference represents one of the best solutions among the MOS-based that allow to achieve low TC while maintaining low the power consumption.

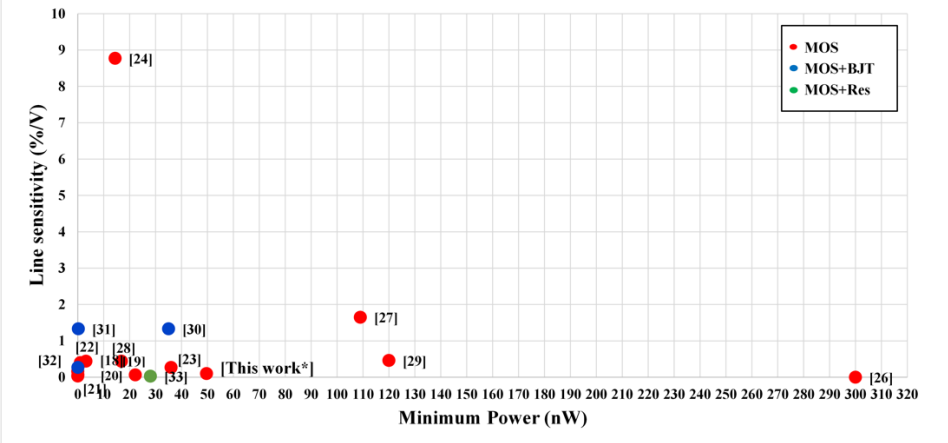


Fig. 56. Comparison of the Line sensitivity LS as a function of the minimum power consumption.

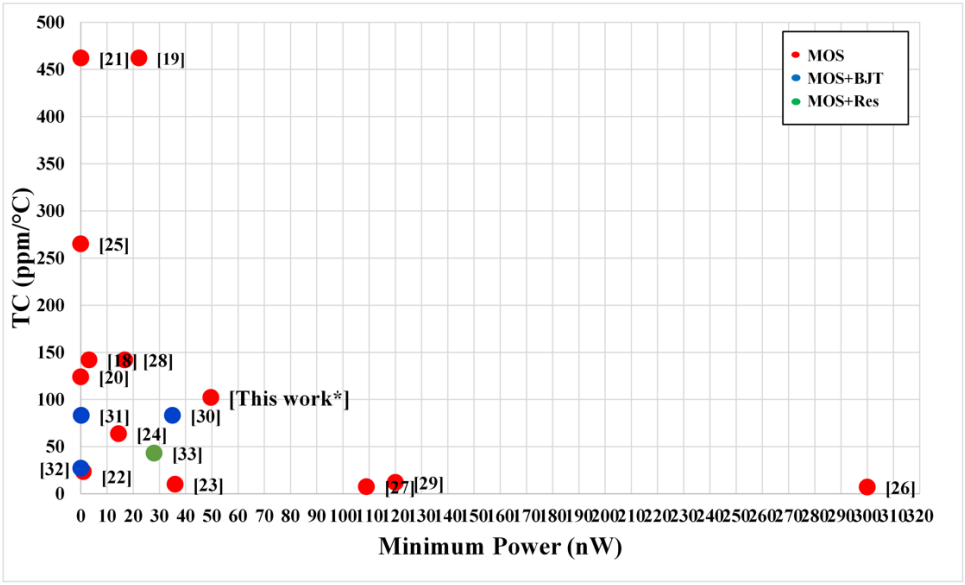


Fig. 57. Comparison of the Temperature Coefficient TC as a function of the minimum power consumption.

2.5.10 Experimental Results

The chip photo of the proposed ultra-low power voltage reference with an occupied area equal to $340\ \mu m \times 127\ \mu m = 43180\ \mu m^2$ is shown in Fig. 58. A set of five different die of the same run were implemented by using the BCD8sp technology which is a 160-nm CMOS bulk-technology provided by STMicroelectronics. Measurement at chip level have been performed to evaluate the performances of the reference voltage under different supply voltage and temperature conditions. The overall measurement has been carried out by using a power supply generator to precisely set the supply voltage of both the voltage reference and its related PCB while a multimeter has been used to measure the reference voltage. Additionally, the temperature behavior of the reference voltage has

been measured by using a temperature chamber consisting of a Thermostream tool which is able to precisely set the temperature during the measurement.

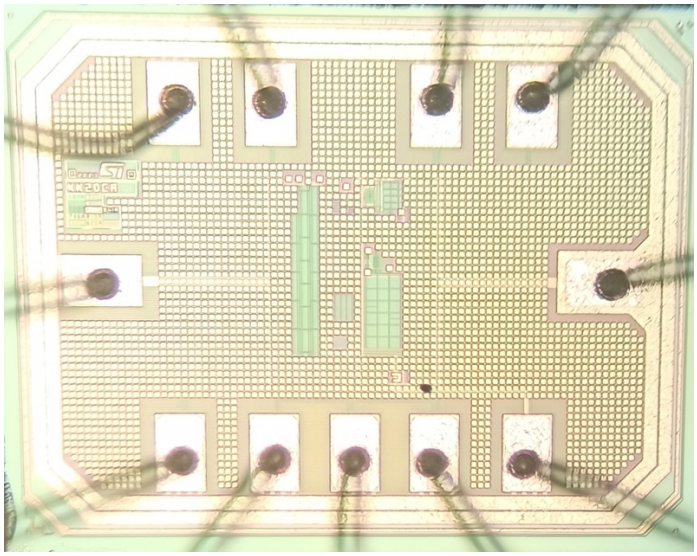


Fig. 58. Chip photo.

The reference voltage has been measured in the supply range from 1.2 to 5 V in steps of 200 mV (Fig. 59) at room temperature and the measured values are summarized in Table XXX.

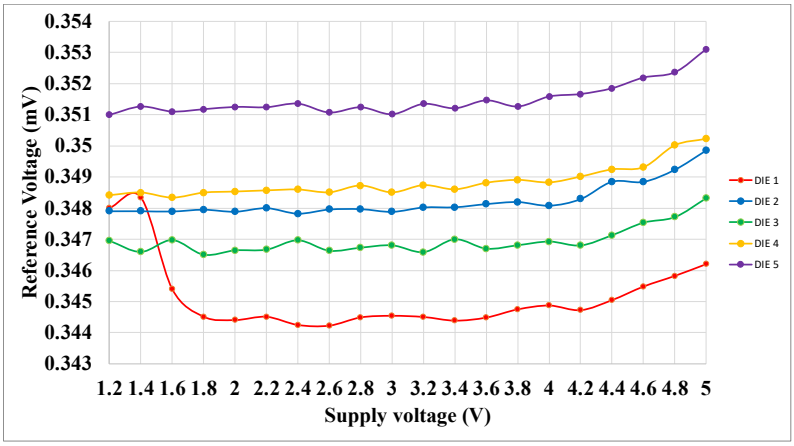


Fig. 59. Reference voltage as a function of the supply voltage.

The average nominal value of the reference voltage is 348 mV while the simulated value of the average reference voltage was 404.68 mV. This means that the measured reference voltage is less than 57 mV of the simulated one, this possibly related to the variation on the transistor's model. MOS transistors that are used in low-current design as the proposed one, are not well-modeled and consequently affect the accuracy with which the reference voltage is achieved. The problem is exacerbated in this design where not-well mature native MOS transistors has been added as well. The reference voltage variations in the supply voltage range [1.2÷5] V and the values of the line sensitivity are summarized in Table XXXI. In the nominal condition, post-layout simulation results shown a reference voltage variation of 1.57 mV thus leading a LS equal to 0.102 % / V while measurement results show a reference voltage variation of 1.81 mV (average value) thus leading a LS equal to 0.14 % / V (average value) thus proving that silicon results are perfectly aligned to the simulation results.

TABLE XXX: Reference voltage as a function of the supply voltage.

	DIE 1	DIE 2	DIE 3	DIE 4	DIE 5
VDD	VREF (V)	VREF (V)	VREF (V)	VREF (V)	VREF (V)
1.2	0.348001	0.347902	0.346951	0.348411	0.350999
1.4	0.348346	0.347903	0.346594	0.348497	0.351265
1.6	0.345396	0.347894	0.346974	0.348334	0.351107
1.8	0.344511	0.347952	0.346503	0.348494	0.35118
2	0.344404	0.347886	0.346642	0.348528	0.351254
2.2	0.344508	0.348001	0.346666	0.348565	0.351244
2.4	0.344246	0.347824	0.346966	0.348593	0.351358
2.6	0.344224	0.347958	0.346631	0.348504	0.351074
2.8	0.344489	0.347969	0.346729	0.348722	0.351242
3	0.34454	0.347883	0.346804	0.348502	0.351019
3.2	0.344502	0.348024	0.346587	0.348734	0.351352
3.4	0.344385	0.34803	0.346999	0.348599	0.351211
3.6	0.344484	0.348132	0.346698	0.348811	0.351464
3.8	0.344747	0.348199	0.346808	0.348902	0.351267
4	0.34487	0.348081	0.346926	0.348822	0.351588
4.2	0.344722	0.348293	0.346802	0.349009	0.351666
4.4	0.345045	0.348853	0.34713	0.34924	0.351851
4.6	0.34548	0.348849	0.347534	0.349309	0.352192
4.8	0.345823	0.349239	0.347714	0.350014	0.352363
5	0.346201	0.349861	0.348322	0.350221	0.353103

TABLE XXXI: Reference voltage variations and line sensitivity in the supply voltage range [1.2÷5] V

	ΔVREF (V)	LS (%/V)
DIE 1	0.001800344	0.001375
DIE 2	0.00195921	0.001482
DIE 3	0.001370829	0.00104
DIE 4	0.001809974	0.001367
DIE 5	0.002104431	0.001578

Reference voltage and the supply current for two different dies as a function of the temperature in the range [–40÷125] °C are shown in Fig. 60 and 61, respectively. Experimental results of the reference voltage variation (in terms to peak-to-peak voltage) and Temperature Coefficient (TC) for different value of supply voltage and for two different dies are summarized in Table XXXII and Table XXXIII, respectively. In the nominal condition, post-layout simulation results showed a reference voltage variation in temperature of 9.18 mV and a TC of 137.34 ppm/°C. Experimental results show a reference voltage variation in temperature of 7.7 mV and a TC 134. 37 ppm/°C thus confirming the robustness of the silicon as a function of temperature variation.

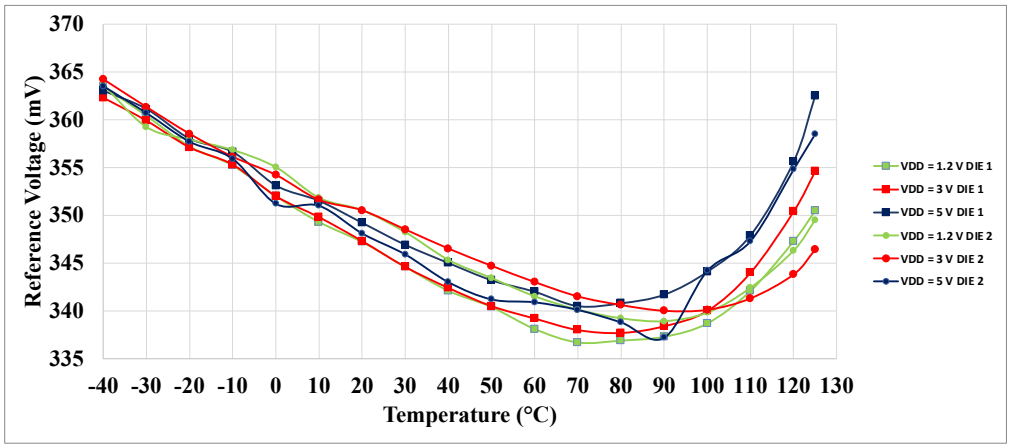


Fig. 60. Temperature dependence of the reference voltage for two different dies.

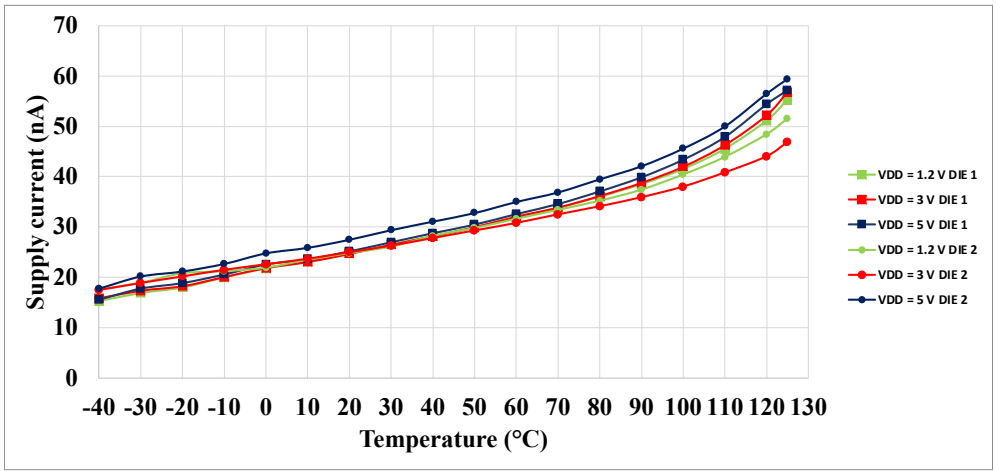


Fig. 61. Temperature dependence of the supply current for two different dies.

TABLE XXXII: Reference voltage variations and TC as a function of temperature for different value of supply voltage (DIE 1)

DIE 1	VREF(peak-to-peak) (mV)	TC (ppm / °C)
VDD = 1.2 V	13	226.923614
VDD = 3 V	7.7	134.3699011
VDD = 5 V	0.5	8.677843729

TABLE XXXIII: Reference voltage variations and TC as a function of temperature for different value of supply voltage (DIE 2)

DIE 2	VREF(peak-to-peak) (mV)	TC (ppm / °C)
VDD = 1.2 V	14.1	243.8075477
VDD = 3 V	17.8	307.7854148
VDD = 5 V	5	87.05265815

Experimental results on the supply current I_q at different value of supply voltage and temperature for two dies under measurement are summarized in Table XXXIV and Table XXXV, respectively.

TABLE XXXIV: Measured supply current at different value of supply voltage and temperature (DIE 1)

Iq (nA) DIE 1	T = – 40 °C	T = 25 °C	T = 125 °C
VDD = 1.2 V	15.3	24.7	55.2
VDD = 3 V	15.9	24.7	56.8
VDD = 5 V	15.6	25.2	57.2

TABLE XXXV: Measured supply current at different value of supply voltage and temperature (DIE 2)

Iq (nA) DIE 2	T = – 40 °C	T = 25 °C	T = 125 °C
VDD = 1.2 V	17.6	24.8	51.5
VDD = 3 V	17.5	25	46.8
VDD = 5 V	17.8	27.5	59.4

The simulated nominal value of the supply current was 41.57 nA while the value of the current variation was 50.26 nA in the temperature range [–40÷125] °C (at V_{DD} = 3 V). The measured value of the supply current is 24.7 nA while the current variation is 40.9 nA in the temperature range [–40÷125] °C (at V_{DD} = 3 V).

At room temperature (T = 25 °C), the simulated supply current I_q changes from 41.5 nA to 42 nA by changing the supply from 1.2 V to 5 V showing a total current variation of 494 pA in the overall supply voltage range. This result is confirmed by experimental results where the supply current Iq changes from 24.7 nA to 25.2 nA thus showing a total current variation of 500 pA in the overall supply range.

To conclude, experimental results performed on the ultra-low power voltage reference are perfectly aligned to the simulation results allowing to maintain the same performance in temperature and supply voltage defined by the two main parameter TC and LS, respectively. A slight variation occurs on the nominal value of the reference voltage which is less than 57 mV compared to the simulated one. This variation is justified by the small current consumption adoption together whit subthreshold region in which the transistors are forced to work and consequently related to the transistor's model not well accurate to manage these smallest current values.

Finally, the proposed ultra-low power voltage reference can be compared with the other architecture taken from the state of the art already shown in the previous paragraph and summarized in Table XXIX. Table XXXVI represent the same comparison at the state of art shown in Table XXIX in which the simulation results of the proposed work have been replaced to the experimental results.

TABLE XXXVI: Comparison to the ultra-low power voltage reference at the state of the art

Reference	23	18	20	19	21	22	24	This work	25	29	26	27	28	30	31	32	33
Year	2007	2011	2012	2013	2013	2018	2015	2023	2021	2006	2009	2012	2018	2015	2019	2019	2019
Type	MOS (VTH difference)	MOS (VTH difference)	MOS (VTH difference)	MOS (VTH difference)	MOS (VTH difference)	MOS (VTH difference)	MOS (bulk-driven)	MOS (VTH difference)	MOS (body-biased)	MOS (other)	MOS (other)	MOS (other)	MOS (other)	MOS+BJT	MOS+BJT	MOS+BJT	MOS+RES
Technology (nm)	350	180	130	180	180	180	180	160	180	350	350	90	180	130	180	180	180
Minimum VDD (V)	0.9	0.45	0.5	0.6	0.45	0.6	0.45	1.2	0.25	1.5	1.4	1.6	0.45	0.9	1	0.9	0.7
VDD (V)	0.9 to 4	0.45 to 2	0.5 to 3	0.6 to 1.8	0.45 to 1.8	0.6 to 2	0.45 to 1.8	1.2 to 5	0.25 to 1.8	1.5 to 4.3	1.4 to 3	1.6 to 3.6	0.45 to 2.4	0.9 to 1.2	1 to 1.8	0.9 to 3.3	0.7 to 2
Current consumption (nA)	40@0.9V 55@4V	7@0.45V 8@1.8V	0.0044@0.5V	37@0.6V 37@1.8V	0.089@0.45V 0.1@1.8V	50.8@0.6V	32@0.45V	24.7@1.2 V 25.2@5V	0.02@0.25V 0.02@1.8V	80@1.5V 110@4.3V	214@1.4V	68@1.6V 173@3.6V	7@2.4V	39@0.9V	0.192@1V	0.035@0.9V 0.041@3.3V	40@0.7V
Power (nW)	36@0.6V 220@4V	3.15@0.45V 14.4@1.8V	0.0022@0.5V	22.2@0.6V 22.2@1.8V	0.040@0.45V 0.18@1.8V	30.5@0.6V	14.4@0.45V	29.64@1.2 V 126@5V	0.005@0.25V 0.042@1.8V	120@1.5V 473@4.3V	300@1.4V	109@1.6V 623@3.6V	16.8@2.4V	35@0.9V	0.192@1V	0.0314@0.9V 0.134@3.3V	28@0.7V
Minimum Power (nW)	36	3.15	0.0022	22.2	0.04	30..5	14.4	29.64	0.005	120	300	109	16.8	35	0.192	0.0314	28
Vref (mV)	670	263.5	176.8	259	275.4	218.3	118.5	348	91.4	891.1	754	771	263.5	559	693	740	368
Temperature range (°C)	[0÷80]	[0÷125]	[−20÷80]	[0÷125]	[0÷120]	[−20÷125]	[−40÷125]	[−40÷125]	[0÷120]	[0÷80]	[−20÷80]	[−40÷125]	[0÷125]	[0÷125]	[−20÷100]	[0÷170]	[−40÷125]
TC (ppm/°C)	10	142	124	462	105.4	23.5	63.6	134.37	265	12	7	7.5	142	83	33	27	43.1
Line sensitivity (%/V)	0.27	0.44	0.033	0.065	0.46	0.4	8.77	0.14	0.16	0.46	0.002	1.65	0.44	1.33	0.02	0.27	0.027
PSRR (dB)	−47@100Hz −40@10kHz	−45@100Hz −12@10MHz*	−53@100Hz −62@10MHz	−44@100Hz* −43.3@10MHz*	−48@100Hz −29.2@10kHz	−42.4@100Hz −42.3@10MHz	−44.2@100Hz	−49.88@1kHz* −49.88@1MHz*	−70@100Hz	−59@100Hz −52@10MHz	−45@100Hz	--	--	−41@100Hz*	−55@100Hz	--	−59@10Hz −39@1MHz
Die Area (mm2)	0.045	0.043	0.00135	0.0298	0.018	0.075	0.012	0.04318	0.0022	0.015	0.055	0.03	0.043	0.0022	0.0045	0.0076	0.055

2.6 Ultra-Low Power Voltage Reference with Ultra-Low Power Analog Output Voltage Buffer

Integrated circuits (ICs) require analog voltage buffers to drive out-of-chip loads that can be either low resistances in the range of a few ohms or large capacitors of several tens or even hundreds of picofarads. Therefore, analog voltage buffers are fundamental building blocks in mixed-signal designs that are also used for signal testing or monitoring [35]. Key performance parameters are accuracy in the voltage transfer and wide bandwidth, other than small input capacitance and high input resistance. Other features like linearity and dynamic range must be also considered [36].

As already stated, the ultra-low-power and low-voltage requirements make power consumption one of the distinctive parameters in modern ICs. Following this trend, output buffers must also operate under low supply voltages and low current consumption, ensuring the same performances as the overall integrated system [37]. Moreover, growing applications such as energy-harvested systems, wearable electronics, battery-less IoT, and Wireless Sensor Networks (WSNs), generally require buffer amplifiers with the following characteristics: small size matched with DC, AC, and transient specifications, ultra-low current, low supply voltage, and rail-to-rail input-output voltage swing [38]. To this purpose, several CMOS voltage buffers have been presented in the literature [36]–[43] combining the analog buffer's distinctive parameter with the low-power requirement.
Besides, it is well known that voltage references are fundamental blocks widely used in analog and digital systems to generate a DC voltage independent of PVT variations and the main approach to implementing ultra-low power CMOS analog building blocks lies in the use of MOS transistors in weak inversion (or subthreshold) region [10].
Under these premises, a buffer amplifier, mandatory for off-chip operations, can be necessary also on chip in the case of ultra-low current reference circuits that do not have sufficient current drive capability even for a fraction of picofarads. In this context, the buffer must keep the same PVT performances and power consumption of the input voltage reference circuit.
Based on the above, a solution of analog voltage buffer with ultra-low current consumption, insensitive to PVT variations and suitable to drive a capacitive load up to 20 pF, expressly designed to complement the ultra-low-current reference voltage circuit presented above has been proposed. Most importantly, the main goal of the proposed analog output buffer is to preserver all the performances of ultra-low current voltage reference related to it.
Fig. 62 shows the block diagram in which a voltage reference circuit (REF) generating the reference voltage V_{REF}, is followed by a voltage buffer implemented as a closed-loop high gain differential amplifier providing output voltage V_{OUT} to a capacitive load C_L external to the IC.

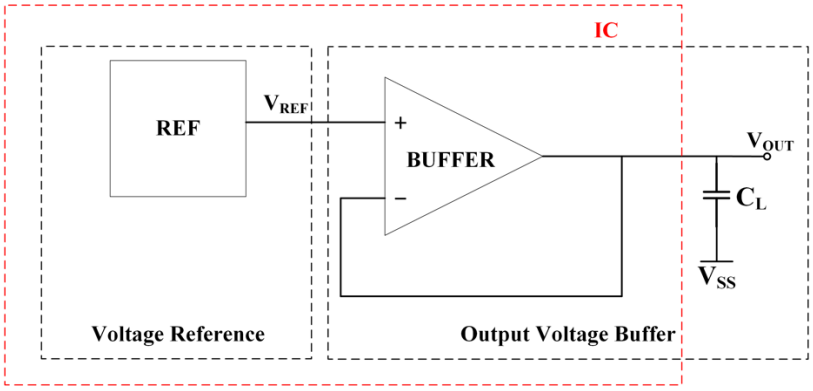


Fig. 62. Block diagram of a reference voltage circuit followed by a voltage buffer driving a load capacitor.

It is apparent that the characteristics of block REF, especially in terms of insensitivity to PVT variations and area, could be compromised or even destroyed by an output buffer that is not properly designed and does not match the reference circuit performance. Moreover, for low-current references,

the required buffer current driving capability should be achieved with the minimum required standby current, to avoid increasing excessively the power consumption of the overall reference-buffer sub-system.

2.6.1 Circuit Description, Operating Point and Circuit Analysis

The circuit schematic of the adopted voltage buffer, consisting in a two-stage CMOS Operational Transconductance Amplifier, is shown in Fig. 63. Although the topology is quite conventional, the novelty is due to the deep subthreshold and nanoamp design that allows to provide the required insensitivity against PVT variations, while ensuring large operating supply and temperature range, accuracy and driving capability.

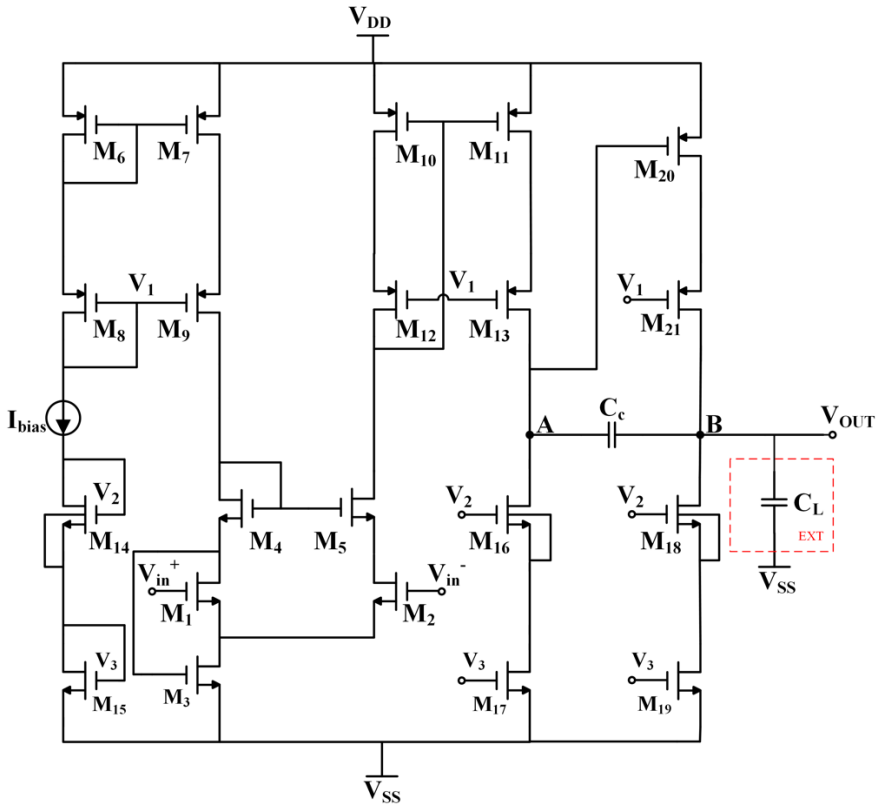


Fig. 63. Circuit schematic of the proposed CMOS voltage buffer (open loop).

The buffer topology includes a first high-gain stage constituted by a class-AB input differential stage $M_{1\text{-}3}$ biased by current source $M_{6\text{-}9}$, followed by a high-impedance cascode current mirror $M_{10\text{-}13}$ and $M_{14\text{-}17}$. The second gain stage is made up of (cascoded) common-source transistor M_{20} (M_{21}) with cascode active load $M_{18\text{-}19}$. Extensive cascoding is used to provide large DC open-loop gain and to allow proper buffer operation under 1.2 V to 5 V supply range. Miller capacitor C_C provides frequency compensation and C_L is the equivalent load capacitance. All the MOS transistors are biased in subthreshold region and their bulk terminals are connected to ground or to V_{DD}, for n-MOS and p-MOS transistors, respectively, except for M_{14}, M_{16}, and M_{18} whose body is shorted to the source terminal, to increase the drain-source voltage of M_{17} and M_{19}, avoiding the triode region. Therefore p-wells are required in the process to allow these bulk connections to a different potential than ground. The input differential pair in the first stage is implemented using a Flipped-Voltage-Follower (FVF) structure [42].

The biasing current I_{bias} is mirrored by the cascode current mirrors $M_{6\text{-}9}$, $M_{14\text{-}19}$, and by the low-voltage cascoded mirror $M_{10\text{-}13}$. Consequently, the drain-current flowing into the differential pair, assuming M_2 matched with M_1, is given by (57) and (58).

$$I_{D2} = I_{D1} = \frac{(W/L)_7}{(W/L)_6} I_{bias} \tag{57}$$

$$I_{D17} = \frac{(W/L)_{11}}{(W/L)_{10}} I_{D2} \tag{58}$$

Hence the current that flows in M_3 is given by equation (59).

$$I_{D3} = I_{D1} + I_{D2} \tag{59}$$

Current I_{bias} is then mirrored by $M_{18\text{-}19}$ in the output stage thus obtaining:

$$I_{D18} = \frac{(W/L)_{19}}{(W/L)_{15}} I_{bias} \tag{60}$$

The open-loop DC gain of the buffer is the product of the first and second stage gains, T_{oA} and T_{oB}, as follows:

$$T_o = T_{oA} \cdot T_{OB} = g_{m1,2} R_{oA} \cdot g_{m20} R_{oB} \tag{61}$$

Where $R_{oA} = (g_{m13} r_{d13} r_{d11}) // (g_{m16} r_{d16} r_{d17})$ and $R_{oB} = (g_{m21} r_{d21} r_{d20}) // (g_{m18} r_{d18} r_{d19})$.

Dominant pole is obtained through capacitor C_C and is equal to:

$$\omega_P = 1/(g_{m20} R_{oB} R_{oA} C_C) \tag{62}$$

The output buffer shown in Fig. 59. was designed by using the same technology of the voltage reference which is a standard 160-nm CMOS bulk technology provided by STMicroelectronics. MOS transistors with different thresholds were exploited, all the n-MOS and p-MOS are 5-V transistor (MN5V, PN5V in Table III) with a threshold voltage $V_{thn} \cong |V_{thp}| \cong 700\ mV$ except for M_1, M_2 and M_3 that are 1.8-V transistors (NLLMOS, PLLMOS in Table III) with a 600 mV threshold. Table XXXVII summarizes the sizes of the transistor in the output buffer, the value of the capacitors and the value of the current in the ideal generator I_{bias}. It should be noted that transistors' sizes were set to achieve a proper matching with the transistors into the reference circuit. Therefore, large length values that characterize transistors M_3 and $M_{6\text{-}7\text{-}10\text{-}11}$ are required to both obtain current values of nanoamperes in a wide range of temperatures and to properly match the transistor in the current reference section of the voltage reference. Additionally, M_3 has been divided into 10 series devices with an aspect ratio of $W/L = (4\ \mu m/\ 50\ \mu m)$ while $M_{6\text{-}7\text{-}10\text{-}11}$ have been divided into 15 series devices with $W/L = (8\ \mu m/\ 50\ \mu m)$.

TABLE XXXVII: Component sizes of output analog voltage buffer.

Component	Value	Unit
$M_{1\text{-}2}$	200 / 10	W / L (μm/μm)
M_3	4 / 500	
$M_{4\text{-}5}$	25 / 3	
$M_{6\text{-}7\text{-}10\text{-}11}$	8 / 750	
$M_{8\text{-}9\text{-}12\text{-}13}$	10 / 40	
$M_{14\text{-}16}$	1.2 / 1.2	
$M_{15\text{-}17}$	20 /20	
M_{20}	8 /2	
M_{21}	200 /10	
M_{18}	16.8 / 1.2	
M_{19}	280 / 20	
C_C	20	pF
C_L	30	
I_{bias}	1	nA

A final note concerns the time domain operation of the buffer. At the start-up, V_{DD} is quickly increased while the input voltage V_{in}^{+} (the reference voltage provided by the voltage reference) and I_{bias} are still zero. Therefore, M_{20} is turned on (its gate voltage is zero) and C_L is charged to V_{DD}. Once the reference voltage is stable at terminal V_{in}^{+}, the buffer will reach the steady state discharging C_L. In this time interval it is also necessary to quickly turn off M_{20} through the current provided by M_{11} flowing onto C_C. At this purpose, the class-AB behaviour of the FVF differential pair is favourable as the maximum current in M_2 is not limited by any tail current, as in conventional differential pairs.

It should be noted that I_{bias} does not actually come from an ideal generator, but it is actually mirrored from the current reference section of the voltage reference circuit shown in Fig. 22 while the generated reference voltage V_{REF} drives the non-inverting input of the output buffer (V_{in}^{+}). To better understand, a more detailed analysis will be carried out in the following section.

2.6.2 Ultra-Low Power Voltage Reference with Output Voltage Buffer

The complete schematic consisting of the proposed ultra-low power voltage reference followed by the ultra-low power output buffer is shown in Fig. 64 where the output of the voltage reference V_{REF} is connected to the non-inverting input of the output buffer. Therefore, the buffer output voltage is consequently indicated as V_{BDG}. The voltages previously indicated with V_1, V_2 and V_3 shown in Fig. 63 has been taken by branches of the reference voltage which have similar values and they are now indicated as a, b, and c respectively (Fig. 64).

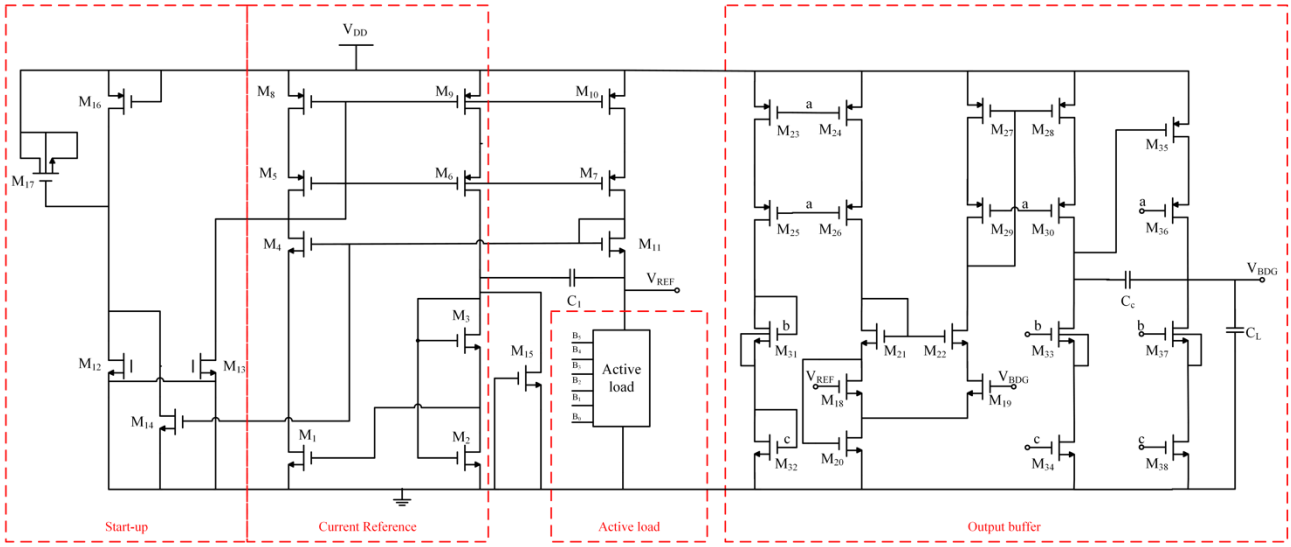


Fig. 64. Schematic of the proposed ultra-low power voltage reference with output buffer.

The biasing current generated into the current reference section is then mirror through the cascode current mirror made up by $M_{5\text{-}10}$ into the cascode current mirror made up by $M_{23\text{-}26}$ and $M_{27\text{-}30}$ to achieve the chosen biasing current. Proper matching between transistor in the cascode current mirror of the reference voltage and of the output buffer is mandatory to properly set the correct value of the current and at the same time to preserve the performance achieved by the reference circuit.

In the proposed output buffer, the desired current flowing into the differential pair was fixed as 1 nA while the current flowing into the voltage reference branches is around 15 nA. Therefore, the aspect ratio between the transistor in the current mirror $M_{8\text{-}10}$ and the transistor in the cascode current mirror $M_{23\text{-}24}$ and $M_{27\text{-}28}$ has been set as:

$$\left(\frac{W}{L}\right)_{M_{8-10}} = \frac{1}{15}\left(\frac{W}{L}\right)_{M_{23-24}} = \frac{1}{15}\left(\frac{W}{L}\right)_{M_{27-28}} \tag{63}$$

By choosing the length of the transistors $M_{23\text{-}24}$ and $M_{27\text{-}28}$ 15 times greater than the length of the transistors $M_{5\text{-}10}$, it is possible to achieve 1 nA per branch in the output buffer which is the desired value. Additionally, fine matching has been achieved by setting the same aspect ratio of the cascode transistors $M_{5\text{-}7}$ in the reference circuit and cascode transistors $M_{25\text{-}26}$ and $M_{29\text{-}30}$ in the output buffer.

2.6.3 Post-Layout Simulation Results

The proposed output voltage buffer was designed and simulated by using the BCD8sp technology which is a 160 nm CMOS bulk-technology provided by STMicroelectronics. The layout of the buffer is shown in Fig. 65 whose area occupation of 56324 μm^2.

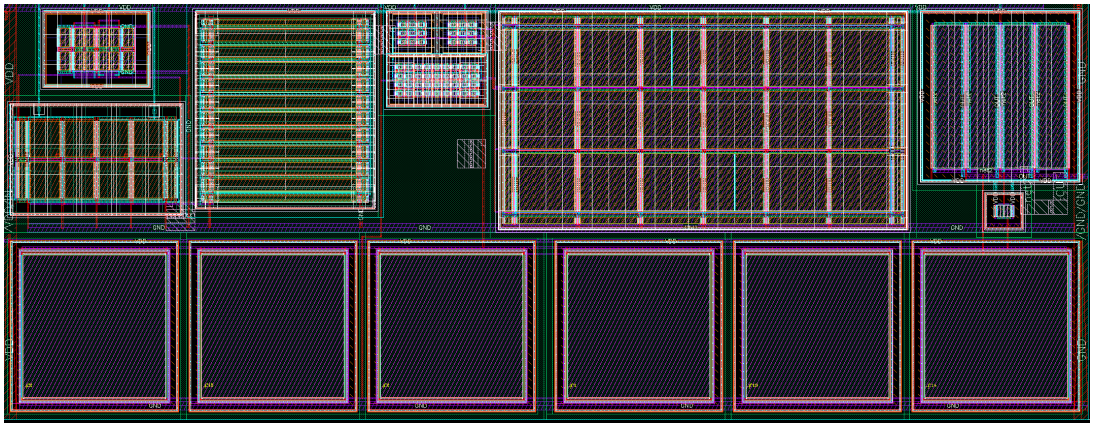


Fig. 65. Layout of the proposed ultra-low power analog voltage buffer.

The proposed output voltage buffer has been designed to be used only in conjunction with the proposed voltage reference to preserve its performances and to be insensitive to PVT variations. Therefore, the frequency analysis of the buffer was carried out during the design with the aim to ensure the stability of the buffer, but the frequency performance have not been optimized since they are not the subject of this work. At this purpose, preliminary simulation (not shown) of the open-loop DC gain of the amplifier was carried out by showing a DC-gain higher than 80 dB with sufficient phase margin in all condition.

Fig. 66. show the layout of the circuit composed of the proposed ultra-low power voltage reference together with the proposed ultra-low power output buffer, resulting in a total area occupation of 145927 μm^2.

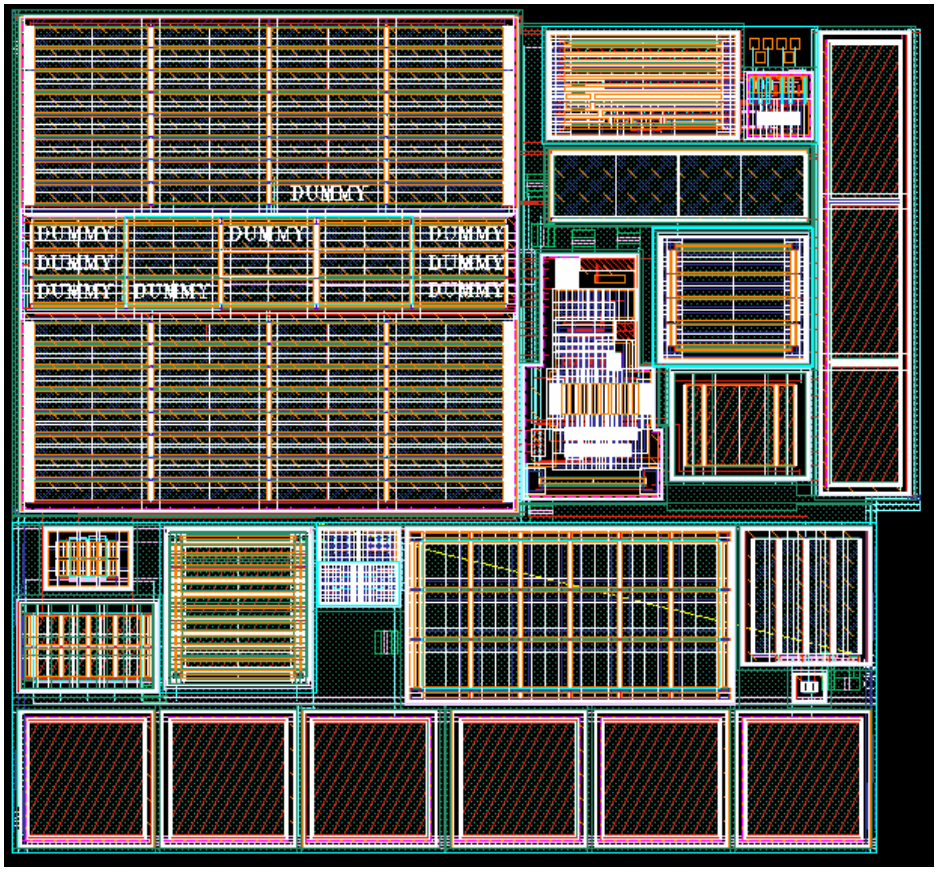


Fig. 66. Layout of the proposed ultra-low power voltage reference with the ultra-low power output buffer.

Post-layout simulations of the overall circuit were carried out in the same supply voltage V_{DD} and temperature T range of the voltage reference which are [1.2÷5] V and [–40÷125] °C, respectively. Additionally, all the post-layout simulations were carried out by taking into account the different models of the transistors: typical (TYP), maximum (MAX), minimum (MIN) and statistical (stat). In the following analysis, nominal condition has been used to indicate the condition achieved with a supply voltage equal to 3 V and a temperature equal to 25 °C (room temperature).
Table XXXVIII, XXXIX and XL show the achieved value of output voltage V_{BDG} by varying the supply voltage, temperature, and model with the aim to prove the insensitivity of the buffer to PVT variations. The nominal simulated value of the V_{BDG} is equal to 405.15 mV which is basically comparable to the nominal value of the reference voltage V_{REF} which is 404.68271 mV.

TABLE XXXVIII: Buffer output voltage V_{BDG} for different temperatures and models (V_{DD} = 1.2 V).

V_{BDG} (mV) (V_{DD} = 1.2 V)	**T= –40 °C**	**T= 25 °C**	**T= 125 °C**
MOD. TYP.	410.48	404.91	411.86
MOD. MAX.	449.46	447.63	462.93
MOD. MIN.	384.00	374.24	372.91

TABLE XXXIX: Buffer output voltage V_{BDG} for different temperatures and models (V_{DD} = 3 V).

V_{BDG} (mV) (V_{DD} = 3 V)	**T= –40 °C**	**T= 25 °C**	**T= 125 °C**

MOD. TYP.	410.97	405.15	412.42
MOD. MAX.	454.37	447.94	452.22
MOD. MIN.	384.37	374.45	374.10

TABLE XL: Buffer output voltage V_{BDG} for different temperatures and models (V_{DD} = 5 V).

V_{BDG} (mV) (V_{DD} = 5 V)	**T= –40 °C**	**T= 25 °C**	**T= 125 °C**
MOD. TYP.	411.77	406.19	415.19
MOD. MAX.	455.31	449.10	450.78
MOD. MIN.	379.29	375.37	376.75

By inspection of Table XXXVIII, XXXIX and XL is it apparent that V_{BDG} is quite insensitive to PVT variations and the value achieved in the worst case are 372.91 mV (at T = 125 °C, V_{DD} = 1.2 V and MOD. MIN.) and 462.93 mV (at T = 125 °C, V_{DD} = 1.2 V and MOD. MAX.).
Additionally, Monte Carlo simulations were carried out under 1000 iterations by using the statistical model of the transistor. Table XLI, XLII and XLIII summarized the achieved mean value and standard deviation of the buffer output voltage at different supply voltage and temperature. In the nominal condition the achieved mean value and the standard deviation of the voltage V_{BDG} are 405.65 mV and 7.44 mV, respectively.

TABLE XLI : Monte Carlo post-layout simulation results of the buffer output voltage V_{BDG} at V_{DD} = 1.2 V.

V_{BDG}	**V_{DD} = 1.2 V T = -40 °C**	**V_{DD} = 1.2 V T = 25 °C**	**V_{DD} = 1.2 V T = 125 °C**
μ (mV)	410.84	405.42	412.84
σ (mV)	6.05	7.42	7.46

TABLE XLII: Monte Carlo post-layout simulation results of the buffer output voltage V_{BDG} at V_{DD} = 3 V.

V_{BDG}	**V_{DD}= 3 V T= –40 °C**	**V_{DD}= 3 V T= 25 °C**	**V_{DD}= 3 V T= 125 °C**
μ (mV)	411.58	405.65	413.08
σ (mV)	6.56	7.44	6.49

TABLE XLIII : Monte Carlo post-layout simulation results of the buffer output voltage V_{BDG} at V_{DD} = 5 V.

V_{BDG}	**V_{DD}= 5 V T= –40 °C**	**V_{DD}= 5 V T= 25 °C**	**V_{DD}= 5 V T= 125 °C**
μ (mV)	412.36	406.71	415.74
σ (mV)	6.58	7.44	6.34

Extensive post-layout simulations were carried out to show the dependence on both temperature and supply voltage of current consumption of the output buffer by using the TYP model of the transistor. The achieved results are shown in Table XLIV in which it is apparent that the current is almost constant by changing supply voltage and temperature and its value is around 15 nA.

TABLE XLIV: Buffer current consumption for different value of supply voltage and temperature.

Current consumption (nA)	**T =–40 °C**	**T = 25 °C**	**T = 125 °C**
V_{DD} = 1.2 V	13.96	14.57	15.19
V_{DD} = 3 V	13.97	14.57	15.20
V_{DD} = 5 V	13.97	14.57	15.20

The obtained results prove that the output voltage of the buffer is quite insensitive to PVT variations and the achieved voltage values are comparable to that one obtained by the reference voltage. This is a great result because the aim to preserve the PVT variations that is a mandatory requirement for a voltage reference could be achieved. On the other side, the current consumption add by the output buffer is only 15 nA thus without compromising the current consumption achieved with the voltage reference voltage.

The following analysis will be based on the comparison between pre-layout and post-layout simulation results of the buffer output voltage V_{BDG} with the main purpose to verify if adding an output buffer preserve the performances previously obtained.

Firstly, temperature dependence of V_{BDG} has been investigated in the temperature range [–40÷125] °C for different value of supply voltage (V_{DD} = 1.2 V, V_{DD} = 3 V and V_{DD} = 5 V) by using the TYP. model of the transistor. The achieved results are shown in Fig. 67 in which the voltage variations in terms of peak-to-peak voltages are highlighted. Under 3-V supply, the peak-to-peak variations at schematic and layout level are 6.72 mV and 6.85 mV, respectively. Consequently, the TC achieved by the overall circuit become equal to 102.47 ppm/°C.

Recalling that the post-layout voltage variation in temperature of V_{REF} was 6.81 mV and the achieved TC was equal to 102.01 ppm/°C, these obtained results underline that output buffer preserve the temperature behavior of the voltage reference.

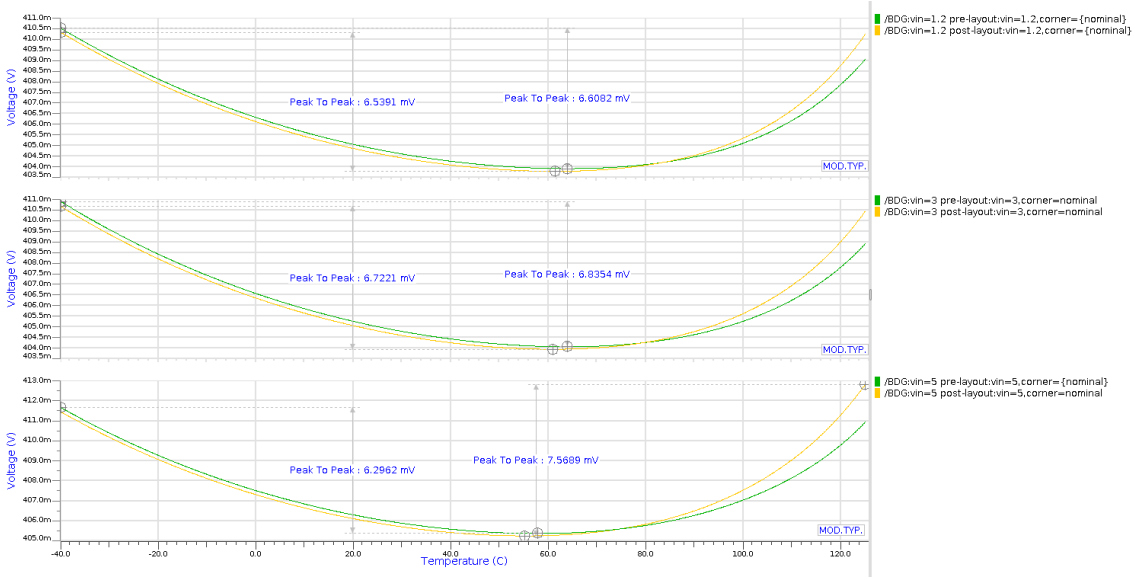


Fig. 67. Temperature dependence of V_{BDG} in the temperature range [–40÷125] °C at TYP. MOD. for different value of supply voltage (V_{DD} = 1.2 V, V_{DD} = 3 V and V_{DD} = 5 V).

Temperature dependence of the supply current in the overall circuit (voltage reference and output buffer) has been investigated in the temperature range [–40÷150] °C for different value of supply voltage (V_{DD} = 1.2 V, V_{DD} = 3 V and V_{DD} = 5 V) by using the TYP. model of the transistor. The achieved results are shown in Fig. 68 in which the achieved current values at different temperatures (T= –40 °C, 25°C, 125°C and 150°C) are highlighted. In the nominal condition, the values of overall supply current achieved at schematic and layout level are 67.62 nA and 68.14 nA, respectively. In the nominal condition, the supply current variation achieved at layout level is 80 nA within the range of [–40÷125] °C by changing from 41.11 nA at –40 °C to 121.74 nA at 125 °C.

Therefore, the nominal value of the supply current change from 41.57 nA to 68.14 nA passing from the reference circuit to the overall circuit.

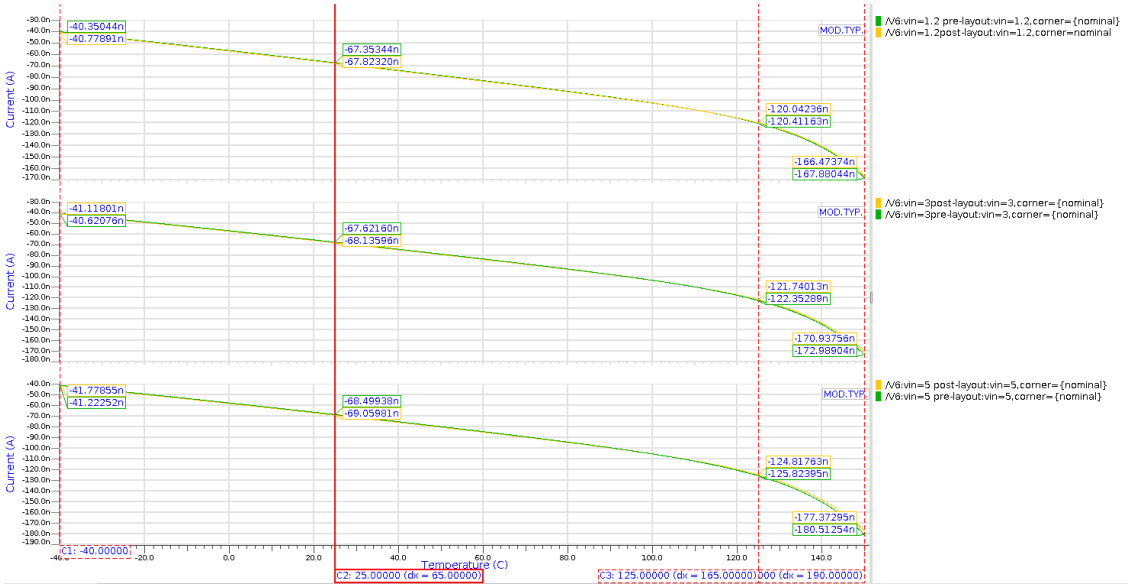


Fig. 68. Temperature dependence of the supply current in the temperature range [–40÷150] °C at TYP. MOD. for different value of supply voltage (V_{DD} = 1.2 V, V_{DD} = 3 V and V_{DD} = 5 V).

The supply voltage dependence of V_{BDG} has been investigated on the supply range [1.2÷5] V for different value of temperature (T = –40 °C, 25 °C and 125 °C) by using the TYP. model of the transistor. The achieved results are shown in Fig. 69 in which also the voltage variations in terms of peak-to-peak voltages are highlighted. Under 25 °C, the peak-to-peak voltage variations at schematic and layout level are 1.259 mV and 1.263 mV, respectively. Consequently, the LS achieved by the overall circuit become equal to 0.082 %/V.

Post-layout simulation results of the reference circuit shown a reference voltage variation of 1.57 mV and a LS equal to 0.102 % / V. Therefore, these results prove that output buffer also preserve the supply voltage dependence obtained by considering only the voltage reference circuit.

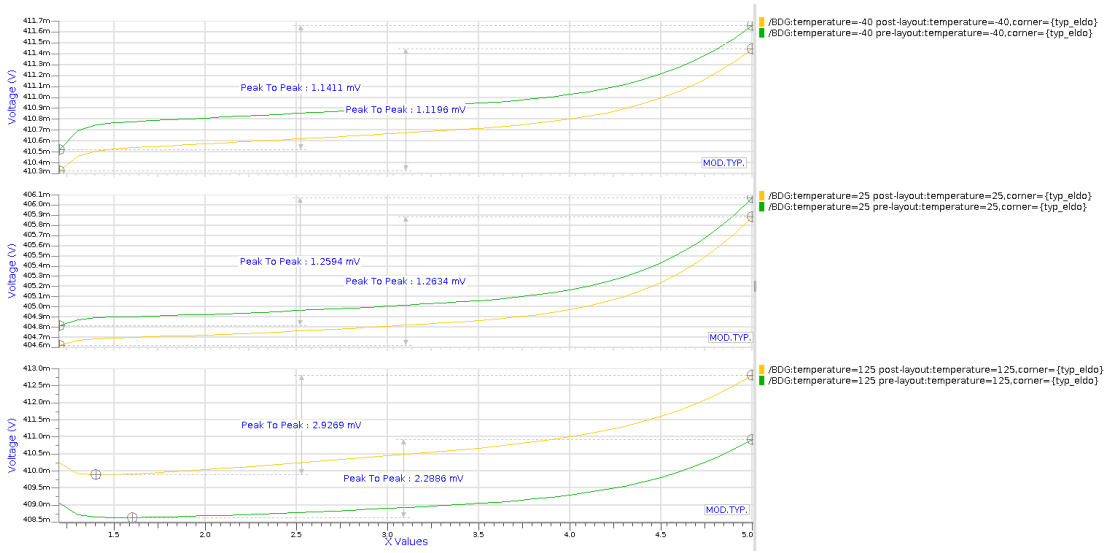


Fig. 69. Supply voltage dependence of V_{BDG} in the supply voltage range [1.2÷5] V for different value of temperature (T = –40 °C, T = 25 °C and T = 125 °C) by using the TYP. model of the transistor.

Similarly, the supply voltage dependence on the supply current has been exploited for different value of temperature (T = –40 °C, 25 °C and 125 °C) by using the TYP. model of the transistor. The achieved results are shown in Fig. 70 in which the supply current variations in terms of peak-to-peak voltages are highlighted. In the nominal condition, the supply current variations achieved at schematic and layout level are 1.14 nA and 725.55 pA, respectively.

The post-layout supply current variations achieved by considering only the reference circuit was 488 pA which is 234 pA less than that achieved by considering the overall circuit.

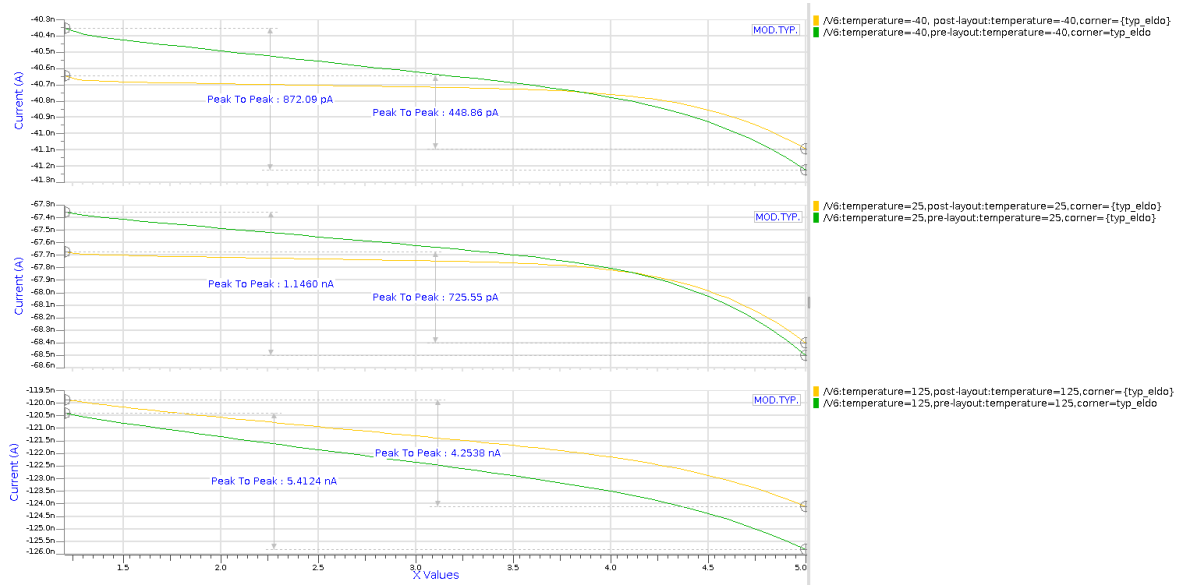


Fig. 70. Supply voltage dependence of the supply current in the supply voltage range [1.2÷5] V for different value of temperature (T = –40 °C, T = 25 °C and T = 125 °C) by using the TYP. model of the transistor.

The impact of the mismatch on the buffer output voltage V_{BDG} has been evaluated in the nominal condition at schematic and layout level. The results achieved at schematic level and layout level are the same by showing a mean value of the output voltage equal to 404.78 mV with a standard deviation of 1.04 mV.

The impact of the mismatch on V_{REF} turned out in a mean value of the reference voltage equal to 404.68 mV with a standard deviation of 1.19 mV which are close to the values achieved by

considering the overall circuit. These results also prove that the mismatch due to the transistor into the output buffer does not have any impact on the reference voltage.

```
#.DCMISMATCH  V(BDG) SORT_REL = 1.000000e-03 NSIGMA = 1.000000e+00

Analysis results:

Output DC value                     :     4.0478E-01 Volt
Total output deviation              : +/- 1.0352E-03 Volt
Output deviation due to the
contributors in the report table    : +/- 1.0352E-03 Volt


```

Fig. 71. Mismatch impact on the V_{BDG} at schematic level.

```
#.DCMISMATCH  V(BDG) SORT_REL = 1.000000e-03 NSIGMA = 1.000000e+00

Analysis results:

Output DC value                     :     4.0478E-01 Volt
Total output deviation              : +/- 1.0352E-03 Volt
Output deviation due to the
contributors in the report table    : +/- 1.0352E-03 Volt


```

Fig. 72. Mismatch impact on the V_{BDG} at layout level.

Transient response of the overall circuit has been investigated by stepping the supply voltage from 0 to 1.2 V, 3 V and 5 V for three different temperatures (T = –40 °C, 25 °C and 125 °C) by using the typical model of the transistor. Fig. 73 shows the post-layout simulation results of the transient response at the start-up. As expected, the buffer output voltage follows the supply initially, and then, after the start-up of the voltage reference circuit, settles to the expected steady state value. For instance, at 25 °C the reference voltage provided by the overall circuit V_{BDG} settles to 405.15 mV for an input value of 405.17 mV in less than 100 ms, proving that the buffer output voltage follows the input reference voltage with good accuracy thanks to the high open-loop gain.

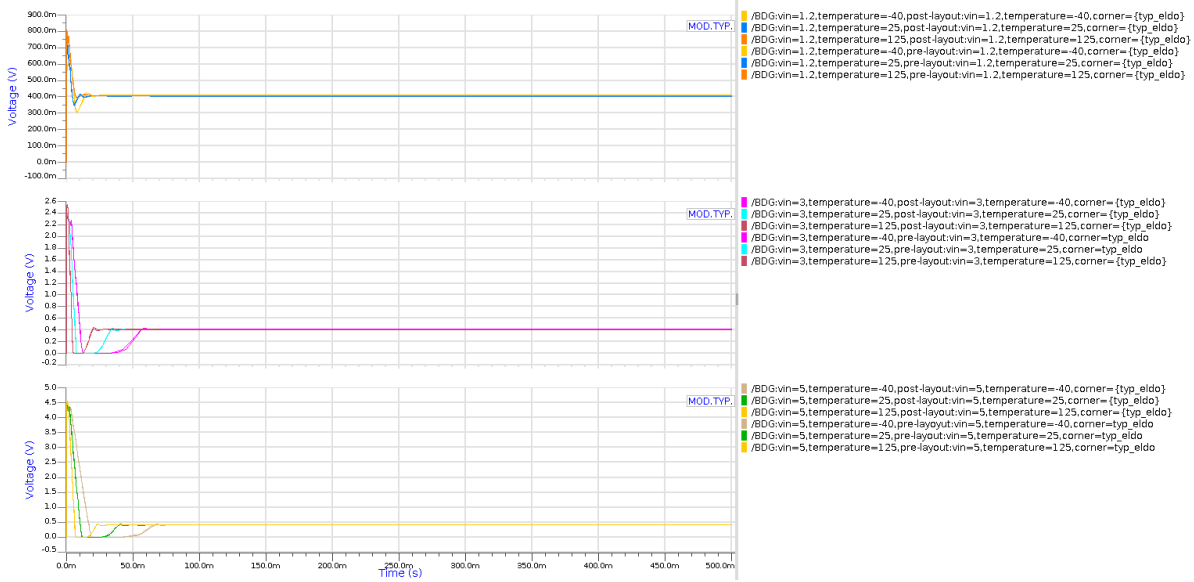


Fig. 73. Post-layout simulation results of the transient response of the V_{BDG} at the start-up for different value of supply voltage and temperature (MOD. TYP.).

The proposed output buffer has been added to this design with the only purpose to be able to measure the reference voltage provided by the voltage reference circuit. Without an output buffer the high-impedance of the test probe would destroy the reference voltage which is in a low-impedance node. Furthermore, the test probe could add an additional current on the branch in which the reference voltage lies thus resulting in a great issue in nano-ampere design like the proposed one. Therefore, the output buffer must guarantee its operation also when an additional current could be provided in the output node.

At this purpose, extensive simulations regarding the transient response of the buffer output voltage V_{BDG} have been carried out adding a load current to the output node of the buffer by stepping the supply voltage from 0 to 1.2 V, 3 V and 5 V for three different temperatures (T = –40 °C, 25 °C and 125 °C) in the typical corner at both schematic and layout level.

The achieved results (Fig. 74) show that the voltage V_{BG} settled the expected steady state under all condition also by adding a current on the output branch up to the maximum value of 1 μA.

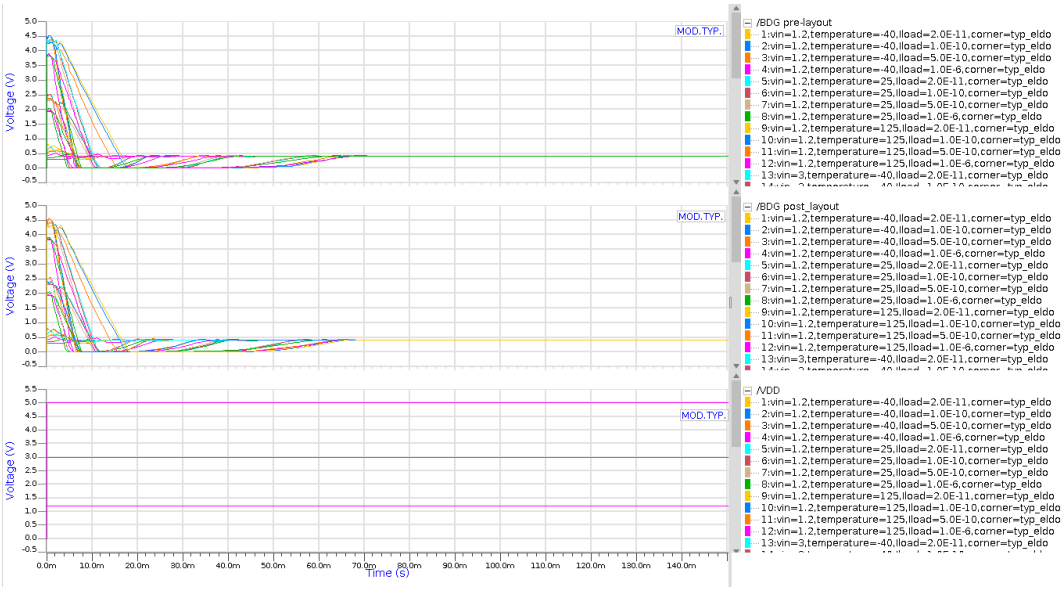


Fig. 74. Post-layout simulation results of the transient response at the start-up of the V_{BDG} for different value of supply voltage, temperature, and load current (MOD. TYP.).

To conclude, the performance parameters achieved by the reference voltage previously shown in Table XXVIII can be compared with those achieved by the circuit composed of voltage reference with the output buffer. At this purpose, Table XLV show the comparison between the main performance parameters achieved by the two proposed architecture. As it already stated, the two main parameters which are TC and LS are perfectly preserved by the overall circuit proving that the addition of the output buffer preserve the dependence on the temperature and supply voltage of the reference circuit. The reference voltage achieved by the overall system is the desired one, but the addition of the output buffer results in an obvious increase of current. Anyway, the additional current is only 26 mV more than the one achieved by the reference circuit, and it does not change by changing the supply voltage. The achieved results underline that the proposed low-power output buffer could be a good solution to complement the proposed low-power voltage reference thanks to its insensitive to PVT variations and to the possibility to preserve the supply voltage and temperature dependence of the reference circuit.

TABLE XLV: Performance comparison between the proposed voltage reference and the proposed voltage reference with the proposed output buffer.

	Proposed Voltage Reference	Proposed Voltage Reference with Output Buffer
Technology (nm)	160	160
Minimum VDD (V)	1.2	1.2
VDD (V)	1.2 to 5	1.2 to 5 V
Current consumption (nA)	41.38@1.2 V 41.85@5V	67.35@1.2 V 68.50@5V
Power (nW)	49.66@1.2 V 209.25@5V	80.82@1.2 V 342.5@5V
Minimum Power (nW)	49.66	80.82
Vref (mV)	404.68	405.15
Temperature range (°C)	[−40÷125]	[−40÷125]
TC (ppm/°C)	102	102
Line sensitivity (%/V)	0.102	0.082
PSRR (dB)	−49.88@1kHz −49.88@1MHz	--
Die Area (mm2)	0.04318	0.145927

2.6.4 Alternative Solution of The Proposed Analog Voltage Output Buffer (3-nA version and 8-nA version)

The proposed solution of the analog voltage output buffer previously discussed was designed and simulated under the assumption of 1 nA of current flowing into the input differential pair. Although the simulations have proven the stability of the obtained current over PVT variations, it is quite obvious that the simulated value can be change by passing from simulation to silicon measurement. In addition, handling current in the nano-amper range by using native transistor with a very-low threshold voltage in a subthreshold design can lead a second-order effect not modelized into the transistor model thus resulting into current variation which could be destroy the nano-amper design.

Alternative solutions of the proposed output voltage buffer have been designed which differ from the previous one only in terms of the current flowing into the differential pair but preserve that same simulation results already obtained. This means that the proposed output buffer can preserve its performances also by changing the current flowing into the differential pair.

The circuit schematic of the output buffer and the overall circuit are the same previously shown in Fig. 63 and 64, respectively. The difference with regard to the previous output buffer design besides in the dimension of the transistors $M_{23\text{-}24}$ and $M_{27\text{-}28}$ whose aspect ratio are related to the aspect ratio of the transistor in the current generator section of the voltage reference. In this alternative proposed solution that is the 3 nA version of the output buffer, the aspect ratio between the transistor in the current mirror $M_{8\text{-}10}$ and the transistor in the cascode current mirror $M_{23\text{-}24}$ and $M_{27\text{-}28}$ has been set as:

$$\left(\frac{W}{L}\right)_{M_{8-10}} = \frac{1}{7}\left(\frac{W}{L}\right)_{M_{23-24}} = \frac{1}{7}\left(\frac{W}{L}\right)_{M_{27-28}} \quad (64)$$

By choosing the length of the transistors $M_{23\text{-}24}$ and $M_{27\text{-}28}$ seven times greater than the length of the transistors $M_{5\text{-}10}$, it is possible to achieve 3 nA per branch in the output buffer which is the desired value. Therefore, the aspect ratio of $M_{23\text{-}24}$ and $M_{27\text{-}28}$ was set equal to $8\ \mu m/350\ \mu m$ while the other transistor continue to maintain the same size. The proposed output voltage buffer in its 3 nA version was designed and simulated by using the BCD8sp technology which is a 160 nm CMOS bulk-technology provided by STMicroelectronics. The layout of the buffer is shown in Fig. 75 whose area occupation of 89603 μm^2.

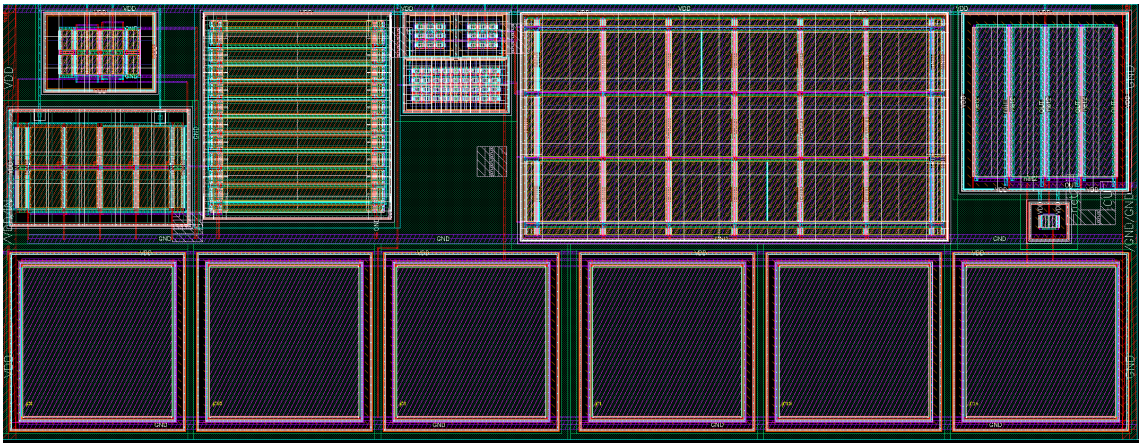


Fig. 75. Layout of the proposed ultra-low power analog voltage buffer (3 nA version).

Fig. 76. show the layout of the circuit composed of the proposed ultra-low power voltage reference and the proposed ultra-low power output buffer in its 3 nA version, resulting in a total area occupation of 145927 μm^2.

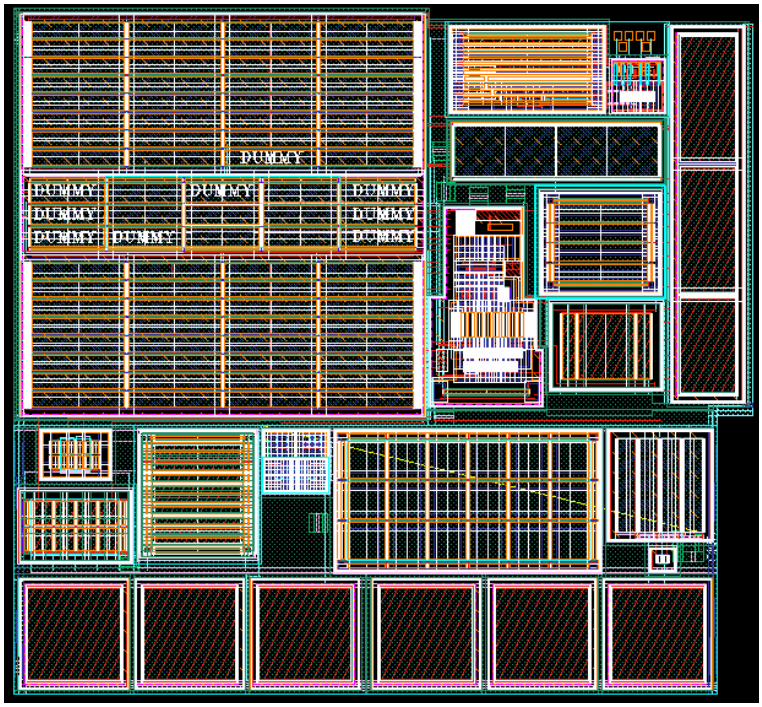


Fig. 76. Layout of the proposed ultra-low power voltage reference with the ultra-low power output buffer (3 nA version).

Once again, the pre and post-layout simulations of the overall circuit were carried out in the supply voltage V_{DD} and temperature T range equal to [1.2÷5] V and [–40÷125] °C, respectively. In the following analysis, the nominal condition has been used to indicate the condition achieved with a supply equal to 3 V and a temperature equal to 25 °C (room temperature).

The following analysis will be based on the comparison between pre-layout and post-layout simulation results of the buffer output voltage V_{BDG} with the purpose to verify if adding an alternative configuration of the proposed output buffer preserve the performances previously obtained by the voltage reference.

Firstly, the temperature dependence of V_{BDG} has been investigated in the temperature range [–40÷125] °C for different value of supply voltage (V_{DD} = 1.2 V, 3 V and 5 V) by using the TYP. model of the transistor. The achieved results are shown in Fig. 77 in which the voltage variations in terms of peak-to-peak voltages are highlighted. Under 3-V supply, the peak-to-peak variations at

schematic and layout level are 6.82 mV and 7.58 mV, respectively. Consequently, the TC achieved by the overall circuit become equal to 113 ppm/°C.Recalling that the post-layout voltage variation in temperature of V_{REF} was 6.81 mV and the achieved TC was equal to 102.01 ppm/°C, these obtained results underline that output buffer preserve the temperature behavior of the voltage reference with a slight deviation on TC of 10 ppm / °C.

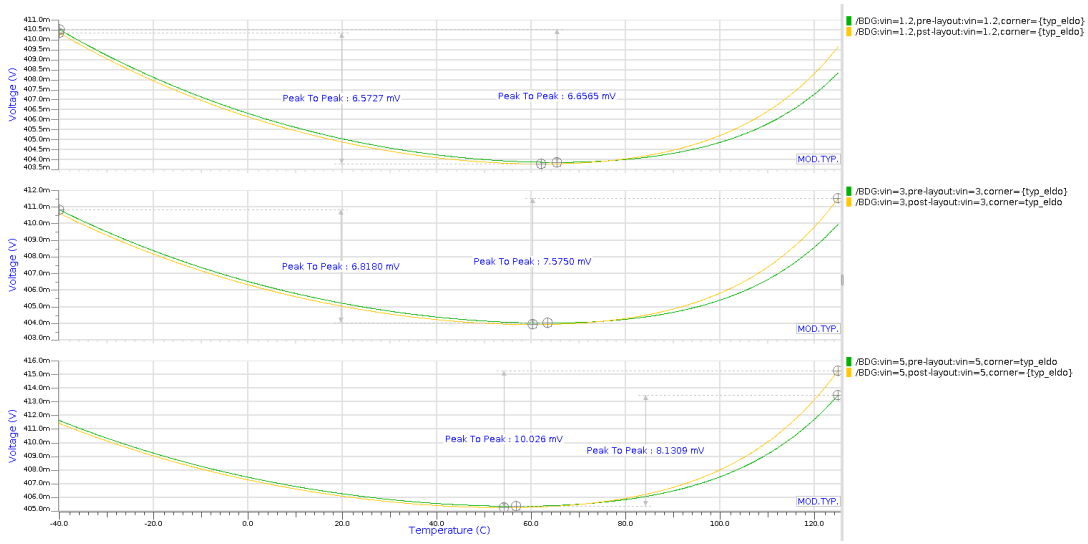


Fig. 77. Temperature dependence of V_{BDG} (3nA version) in the temperature range [–40÷125] °C at TYP. MOD. for different value of supply voltage (V_{DD} = 1.2 V, V_{DD} = 3 V and V_{DD} = 5 V).

Temperature dependence of the supply current in the overall circuit (voltage reference and output buffer in its 3 nA version) has been investigated in the temperature range [–40÷150] °C for different value of supply voltage (V_{DD} = 1.2 V, V and 5 V) by using the TYP. model of the transistor. The achieved results are shown in Fig. 78 in which the achieved current values at different temperatures (T= –40 °C, 25°C, 125°C and 150°C) are highlighted. In the nominal condition the values of overall supply current achieved at schematic and layout level are 94.05 nA and 95.01 nA, respectively. In the nominal condition, the supply current variation achieved at layout level is 111 nA within the range of [–40÷125] °C by changing from 57.09 nA to 168.21 nA.

Therefore, the nominal value of the supply current change from 41.57 nA to 95.01 nA passing from the reference circuit to the overall circuit.

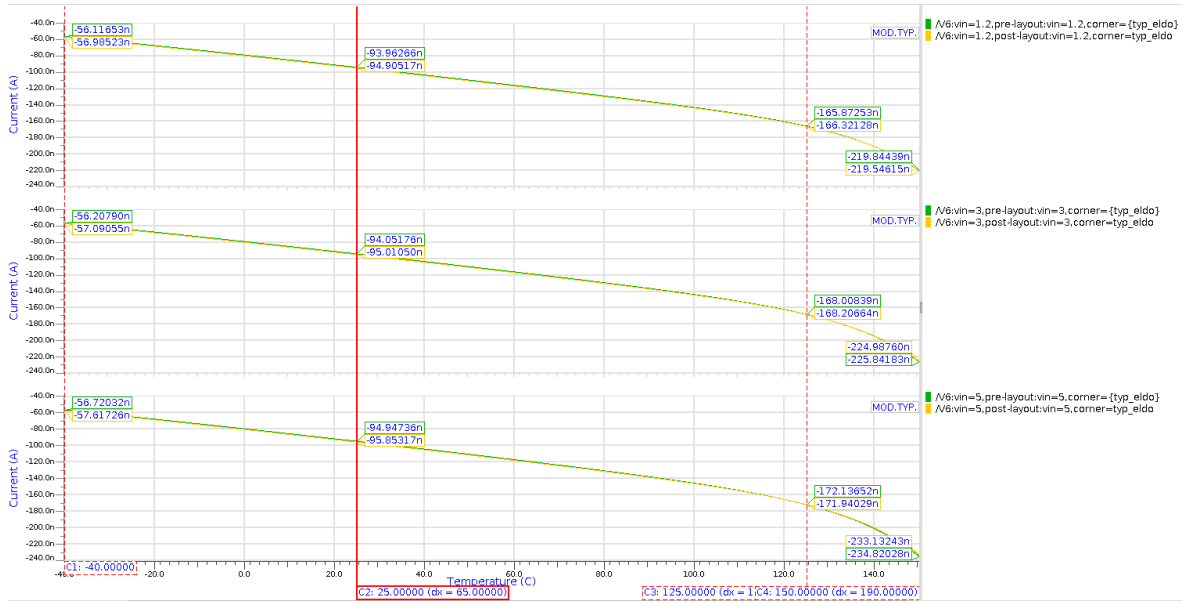


Fig. 78. Temperature dependence of the supply current (3 nA version) in the temperature range [–40÷150] °C at TYP. MOD. for different value of supply voltage (V_{DD} = 1.2 V, V_{DD} = 3 V and V_{DD} = 5 V).

The supply voltage dependence of V_{BDG} has been investigated on the supply voltage range [1.2÷5] V for different value of temperature (T = –40 °C, 25 °C and 125 °C) by using the TYP. model of the transistor. The achieved results are shown in Fig. 79 in which also the voltage variations in terms of peak-to-peak voltages are highlighted. Under 25 °C of temperature, the peak-to-peak variations at schematic and layout level are 1.258 mV and 1.243 mV, respectively. Consequently, the LS achieved by the overall circuit become equal to 0.081 %/V.

Post-layout simulation results of the reference circuit shown a reference voltage variation of 1.57 mV and a LS equal to 0.102 % / V. Therefore, these results prove that the 3 nA version of the output buffer also preserve the supply voltage dependence obtained by considering only the voltage reference circuit.

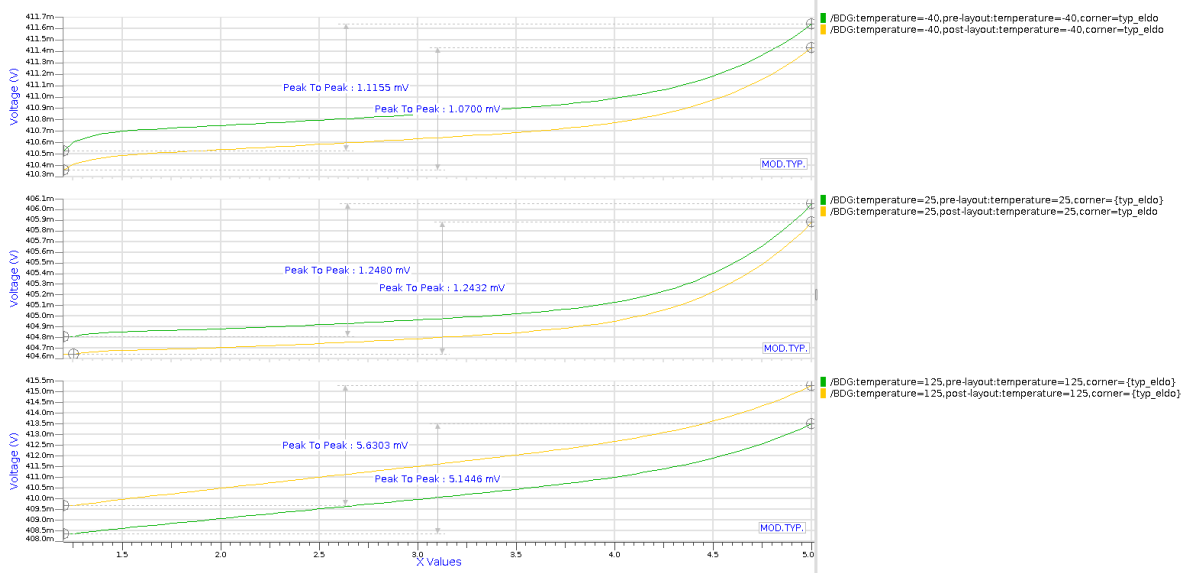


Fig. 79. Supply voltage dependence of V_{BDG} (3 nA version) in the supply voltage range [1.2÷5] V for different value of temperature (T = –40 °C, T = 25 °C and T = 125 °C) by using the TYP. model of the transistor.

Similarly, the supply voltage dependence on the supply current has been exploited for different value of temperature (T = –40 °C, 25 °C and 125 °C) by using the TYP. model of the transistors. The achieved results are shown in Fig. 80 in which the supply current variations in terms of peak-to-peak

voltages are highlighted. In the nominal condition, the supply current variations achieved at schematic and layout level are 984.71 pA and 990.49 pA, respectively.

The post-layout supply current variations achieved by considering only the reference circuit was 488 pA which is 502 pA less than that achieved by considering the overall circuit.

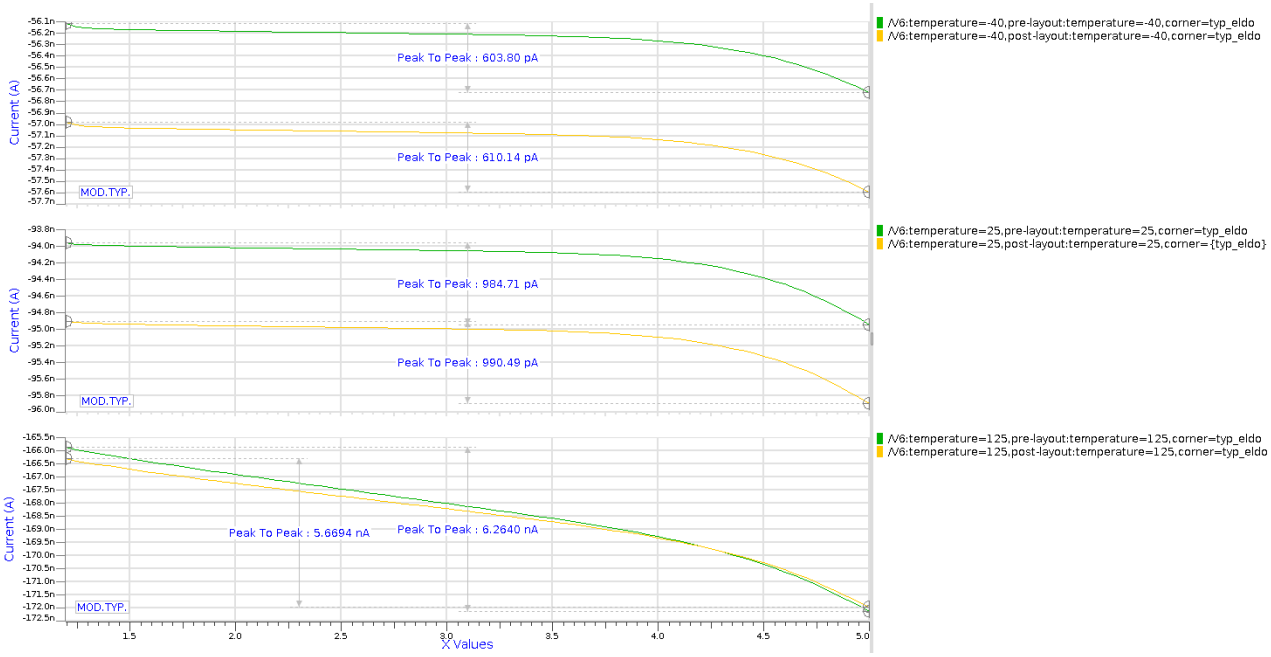


Fig. 80. Supply voltage dependence of the supply current (3 nA version) in the supply voltage range [1.2÷5] V for different value of temperature (T = –40 °C, T = 25 °C and T = 125 °C) by using the TYP. model of the transistor.

Fig. 81 and 82 shown the impact of the mismatch on the buffer output voltage V_{BDG} (3 nA version) has been evaluated in the nominal condition at schematic and layout level. The results achieved at schematic level show a mean value of the reference voltage equal to 404.78 mV with a standard deviation of 1.04 mV that are equal to the layout-level achieved ones.

The impact of the mismatch on V_{REF} turned out in a mean value of the reference voltage equal to 404.68 mV with a standard deviation of 1.19 mV which are close to the values achieved by considering the overall circuit. These results also prove that the mismatch due to the transistor into the output buffer does not have any impact on the reference voltage.

```
1 #.DCMISMATCH  V(BDG) SORT_REL = 1.000000e-03 NSIGMA = 1.000000e+00
2
3 Analysis results:
4
5 Output DC value                    :     4.0478E-01 Volt
6 Total output deviation             : +/- 1.0352E-03 Volt
7 Output deviation due to the
8 contributors in the report table   : +/- 1.0352E-03 Volt
9
10
```

Fig. 81. Mismatch impact on the V_{BDG} (3nA version) at schematic level.

```
#.DCMISMATCH  V(BDG) SORT_REL = 1.000000e-03 NSIGMA = 1.000000e+00

Analysis results:

Output DC value                     :     4.0478E-01 Volt
Total output deviation              : +/- 1.0352E-03 Volt
Output deviation due to the
contributors in the report table    : +/- 1.0352E-03 Volt


```

Fig. 82. Mismatch impact on the V_{BDG} (3nA version) at layout level.

Transient response of the overall circuit has been investigated by stepping the supply voltage from 0 to 1.2 V, 3 V and 5 V for three different temperatures (T = –40 °C, 25 °C and 125 °C) in the typical corner. Fig. 83 shows the post-layout simulation results of the transient response at the start-up. As expected, the buffer output voltage in its 3 nA version follows the supply initially, and then, after the start-up of the voltage reference circuit, settles to the expected steady state value.

Fig. 83. Post-layout simulation results of the transient response of the V_{BDG} (3nA version) at the start-up for different value of supply voltage and temperature (MOD. TYP.).

Once again, extensive simulations regarding the transient response of the buffer output voltage V_{BDG} in its 3nA version have been carried out adding a load current to the output node of the buffer by stepping the supply voltage from 0 to 1.2 V, 3 V and 5 V for three different temperatures (T = –40 °C, 25 °C and 125 °C) in the typical corner at schematic and layout level.

The achieved results (Fig. 84) show that the voltage V_{BG} settled the expected steady state under all condition also by adding a current on the output branch up to the maximum value of 1 μA.

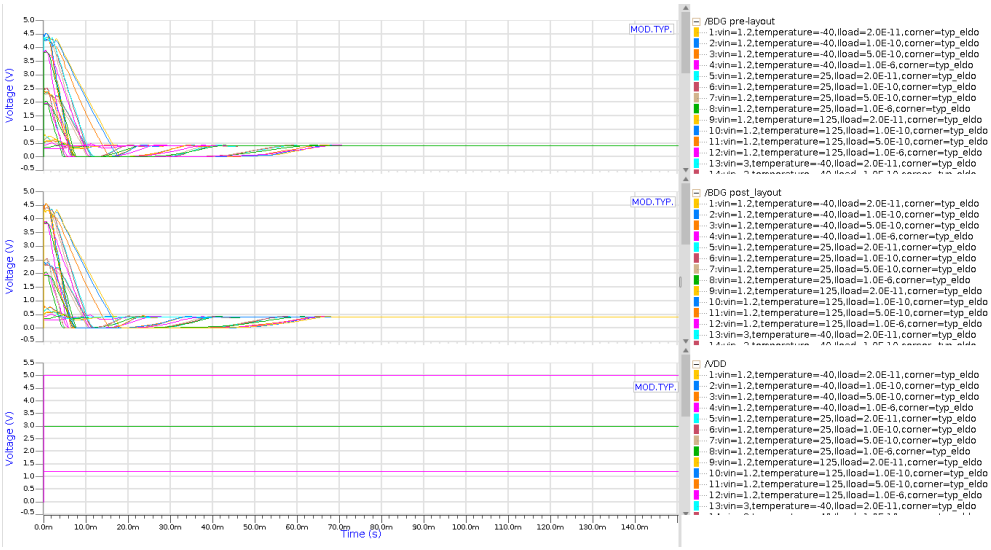


Fig. 84. Post-layout simulation results of the transient response at the start-up of the V_{BDG} (3nA version) for different value of supply voltage, temperature, and load current (MOD. TYP.).

To conclude, the performance parameters achieved by the reference voltage previously shown in Table XXVIII can be compared with those achieved by the circuit composed of the voltage reference with the output buffer in its two versions (1nA and 3nA). Table XLVI show the comparison between the main performance parameters achieved by the three proposed architecture. Although the current consumption and consequently the power dissipation have doubled compared to the voltage reference circuit, the achieved performance of the alternative version of the output voltage buffer are quite good. LS is perfectly preserved in all the proposed configuration while TC shows a little variation of only 10 ppm/°C passing from the voltage reference topology to the overall circuit composed of the voltage reference with the output buffer in its 3 nA version.

The achieved results underline the robustness of the proposed output voltage buffer and consequently to the overall system that shown to preserve its performance by changing from the different proposed topologies.

TABLE XLVI: Performance comparison between the proposed voltage reference and the proposed voltage reference with the proposed output buffer (1 nA and 3 nA versions).

	Proposed Voltage Reference	**Proposed Voltage Reference with Output Buffer (1 nA version)**	**Proposed Voltage Reference with Output Buffer (3 nA version)**
Technology (nm)	160	160	160
Minimum VDD (V)	1.2	1.2	1.2
VDD (V)	1.2 to 5	1.2 to 5 V	1.2 to 5
Current consumption (nA)	41.38@1.2 V 41.85@5V	67.35@1.2 V 68.50@5V	94.91@1.2 V 95.85@5 V
Power (nW)	49.66@1.2 V 209.25@5V	80.82@1.2 V 342.5@5V	113.89@1.2 V 479.25@5 V
Minimum Power (nW)	49.66	80.82	113.89
Vref (mV)	404.68	405.15	404.96
Temperature range (°C)	[−40÷125]	[−40÷125]	[−40÷125]
TC (ppm/°C)	102	102	113
Line sensitivity (%/V)	0.102	0.082	0.081
PSRR (dB)	−49.88@1kHz −49.88@1MHz	--	--
Die Area (mm2)	0.04318	0.145927	0.145927

The alternative proposed solution is the 8 nA version of the output buffer in which the only one difference besides in the current flowing into the differential pair in the input stage which is 8 nA instead of 1 nA or 3 nA compared to the previous version of the output buffer.

The circuit schematic of both the output buffer and the overall circuit are the same previously shown in Fig. 63 and 64, respectively. The difference with regard to the previous output buffer design besides in the dimension of the transistors $M_{23\text{-}24}$ and $M_{27\text{-}28}$ whose aspect ratio are related to the aspect ratio of the transistor in the current generator section of the voltage reference. In the 8 nA proposed version of the output buffer, the aspect ratio between the transistor in the current mirror $M_{8\text{-}10}$ and the transistor in the cascode current mirror $M_{23\text{-}24}$ and $M_{27\text{-}28}$ has been set as:

$$\left(\frac{W}{L}\right)_{M_{8-10}} = \frac{1}{2}\left(\frac{W}{L}\right)_{M_{23-24}} = \frac{1}{2}\left(\frac{W}{L}\right)_{M_{27-28}} \tag{64}$$

By choosing the length of the transistors $M_{23\text{-}24}$ and $M_{27\text{-}28}$ two times greater than the length of the transistors $M_{5\text{-}10}$, it is possible to achieve 8 nA per branch in the output buffer which is the desired value. Therefore, the aspect ratio of $M_{23\text{-}24}$ and $M_{27\text{-}28}$ was set equal to $8\ \mu m/100\ \mu m$ while the other transistor continue to maintain the same size. The proposed output voltage buffer in its 8 nA version was designed and simulated by using the BCD8sp technology which is a 160 nm CMOS bulk-technology provided by STMicroelectronics. The layout of the buffer is shown in Fig. 85 whose area occupation of 55646 μm^2.

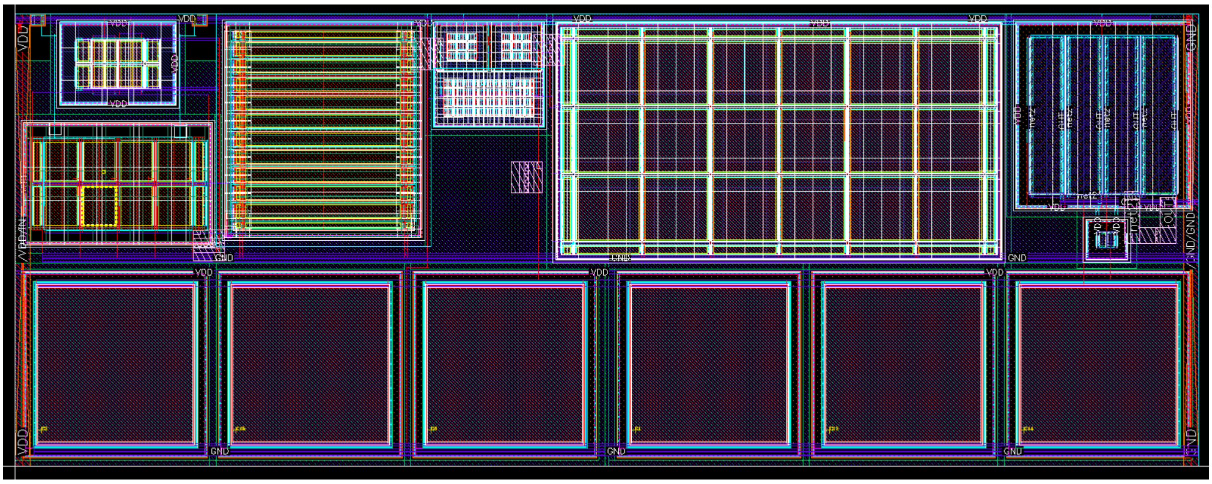


Fig. 85: Layout of the proposed ultra-low power analog voltage buffer (8 nA version).

Fig. 86. shows the layout of the circuit composed of the proposed ultra-low power voltage reference and the proposed ultra-low power output buffer in its 8 nA version, resulting in a total area occupation of 124326 μm^2.

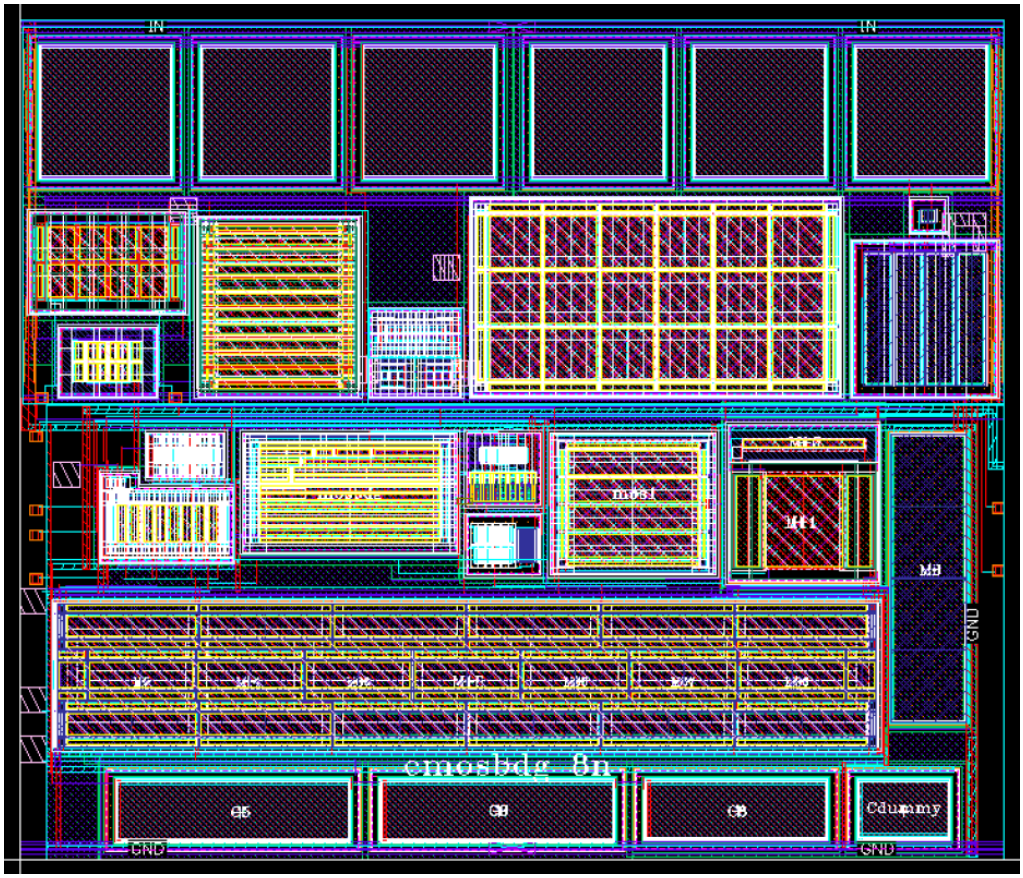


Fig. 86. Layout of the proposed ultra-low power voltage reference with the ultra-low power output buffer (8 nA version).

Even in this case, the pre and post-layout simulations of the overall circuit were carried out in the supply voltage V_{DD} and temperature T range [1.2÷5] V and [–40÷125] °C, respectively. In the following analysis, the nominal condition has been used to indicate the condition achieved with a supply voltage equal to 3 V and a temperature equal to 25 °C (room temperature).

The following analysis will be based on the comparison between pre-layout and post-layout simulation results of the buffer output voltage V_{BDG} with the purpose to verify if adding an alternative configuration of the proposed output buffer preserve the performances previously obtained with the proposed reference voltage.

Firstly, temperature dependence of V_{BDG} has been investigated in the temperature range [–40÷125] °C for different value of supply voltage (V_{DD} = 1.2 V, 3 V and 5 V) by using the TYP. model of the transistor. The achieved results are shown in Fig. 87 in which the voltage variations in terms of peak-to-peak voltages are highlighted. Under 3-V supply, the peak-to-peak variations at schematic and layout level are 7.95 mV and 7.97 mV, respectively. Consequently, the TC achieved by the overall circuit become equal to 119 ppm/°C.

Recalling that the post-layout voltage variation in temperature of V_{REF} was 6.81 mV and the achieved TC was equal to 102.01 ppm/°C, these obtained results underline that output buffer preserve the temperature behavior in terms of TC of the voltage reference with a contained variations on TC of 17 ppm / °C. As can be seen by inspection of Fig. 27, the temperature dependence of V_{REF} show a bell-shaped behavior that is a canonical trend of a reference voltage. It is apparent that this shape is not preserved if the output buffer in its 8 nA version is added to the voltage reference. In fact, as seen in Fig. 87, the bell-shaped form is preserved until 100 °C of temperature after which the output voltage decreases rather than increase. Nevertheless, the voltage variation of V_{BDG} is quite contained and its value is only 1 mV above than the voltage variation achieved by V_{REF}.

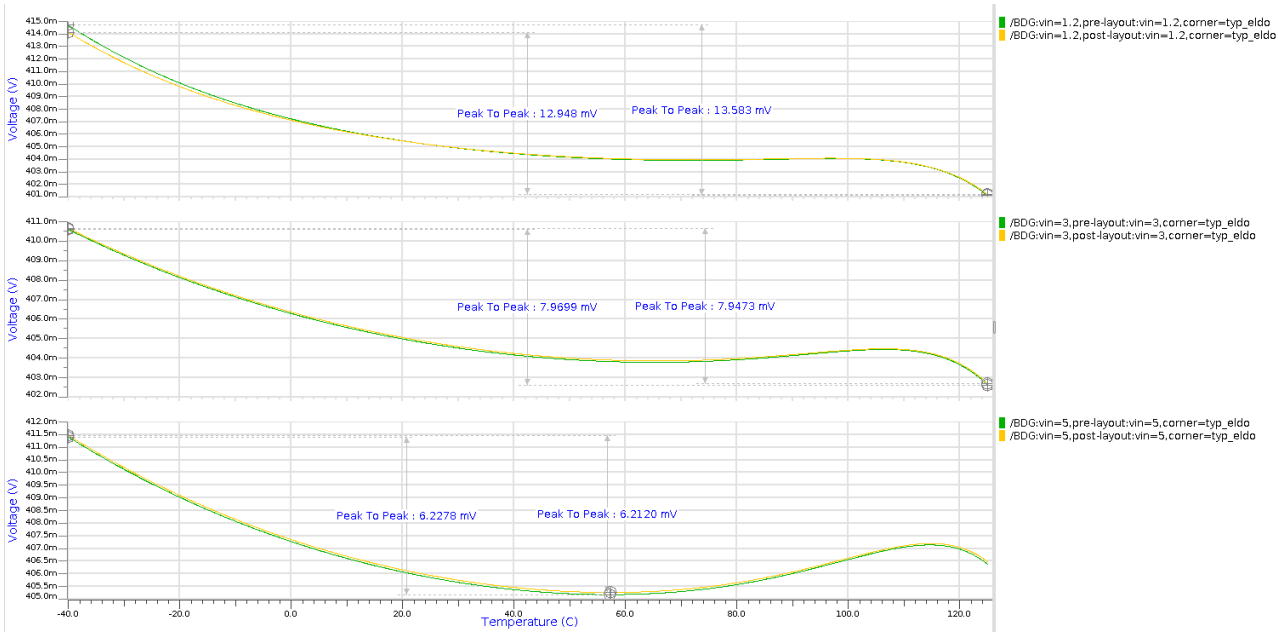


Fig. 87. Temperature dependence of V_{BDG} (8nA version) in the temperature range [–40÷125] °C at TYP. MOD. for different value of supply voltage (V_{DD} = 1.2 V, V_{DD} = 3 V and V_{DD} = 5 V).

Temperature dependence of the supply current in the overall circuit (voltage reference and output buffer in its 8 nA version) has been investigated in the temperature range [–40÷150] °C for different value of supply voltage (V_{DD} = 1.2 V, 3 V and 5 V) by using the TYP. model of the transistor. The achieved results are shown in Fig. 88 in which the achieved current values at different temperatures (T= –40 °C, 25°C, 125°C and 150°C) are highlighted. In the nominal condition the values of overall supply current achieved at schematic and layout level are 196.50 nA and 194.03 nA, respectively. In the nominal condition, the supply current variation achieved at layout level is 221 nA within the range of [–40÷125] °C by changing from 116.38 nA to 336.90 nA.

Therefore, the nominal value of the supply current change from 41.57 nA to 194 nA passing from the reference circuit to the overall circuit.

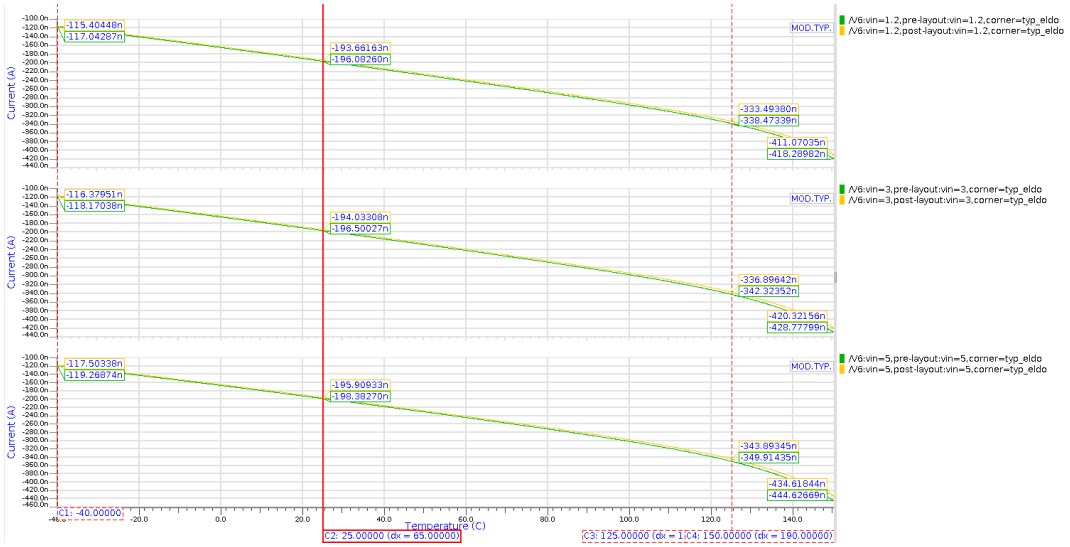


Fig. 88. Temperature dependence of the supply current (8 nA version) in the temperature range [–40÷150] °C at TYP. MOD. for different value of supply voltage (V_{DD} = 1.2 V, V_{DD} = 3 V and V_{DD} = 5 V).

The supply voltage dependence of V_{BDG} has been investigated on the supply range [1.2÷5] V for different value of temperature (T = –40 °C, 25 °C and 125 °C) by using the TYP. model of the transistor. The achieved results are shown in Fig. 89 in which also the voltage variations in terms of

peak-to-peak voltage are highlighted. Under 25 °C, the peak-to-peak voltage variations at schematic and layout level are 1.224 mV and 1.228 mV, respectively. Consequently, the LS achieved by the overall circuit become equal to 0.080 %/V.

Post-layout simulation results of the reference circuit shown a reference voltage variation of 1.57 mV and a LS equal to 0.102 % / V. Therefore, these results prove that the 8 nA version of the output buffer also preserve the supply voltage dependence obtained by considering only the voltage reference circuit.

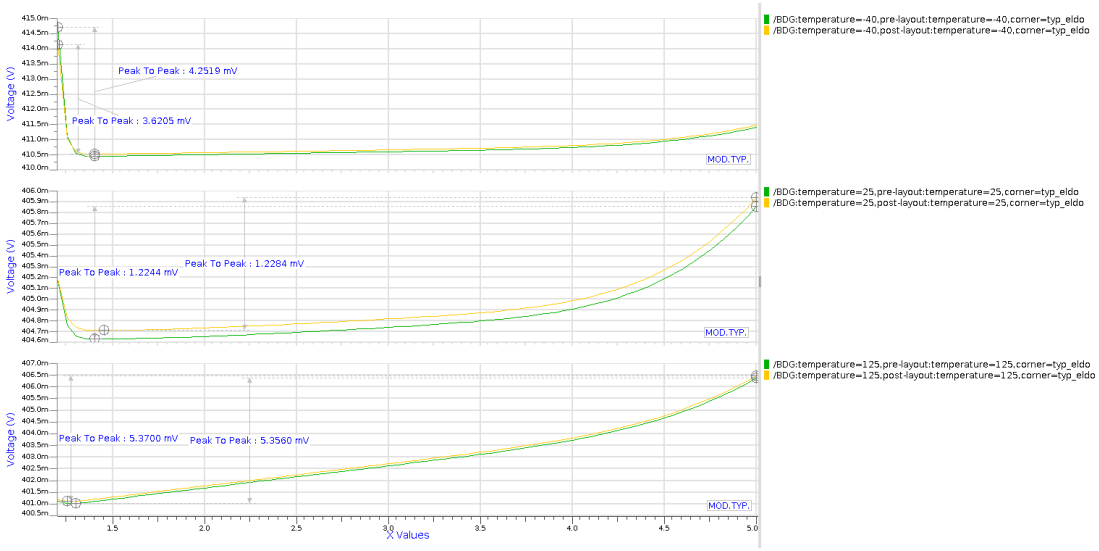


Fig. 89. Supply voltage dependence of V_{BDG} (8 nA version) in the supply voltage range [1.2÷5] V for different value of temperature (T = –40 °C, T = 25 °C and T = 125 °C) by using the TYP. model of the transistor.

Similarly, the supply voltage dependence on the supply current has been exploited for different value of temperature (T = –40 °C, 25 °C and 125 °C) by using the TYP. model of the transistors. The achieved results are shown in Fig. 90 in which the supply current variations in terms of peak-to-peak voltages are highlighted. In the nominal condition, the supply current variations achieved at schematic and layout level are 310.61 nA and 303.94 nA, respectively. The achieved results in terms of supply current underline that the 8 nA version of the proposed output buffer is not insensitive to supply voltage variations.

In fact, the post-layout supply current variations achieved by considering the reference circuit was only 488 pA. This means that the proposed 8 nA version of the output buffer leads to a current variation of 303 nA higher than that achieved by considering only the reference voltage circuit.

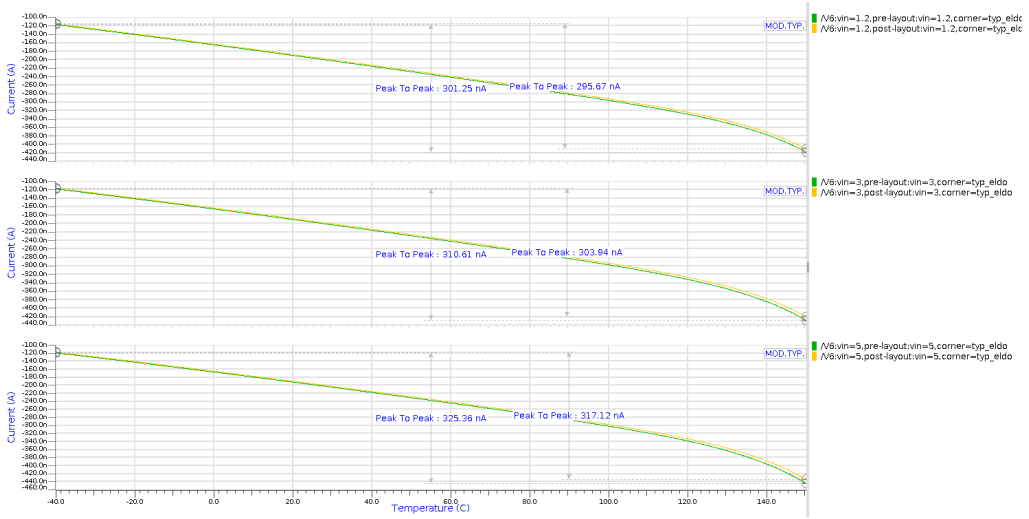


Fig. 90. Supply voltage dependence of the supply current (8 nA version) in the supply voltage range [1.2÷5] V for different value of temperature (T = –40 °C, T = 25 °C and T = 125 °C) by using the TYP. model of the transistor.

Fig. 91 and 92 shown the impact of the mismatch on the buffer output voltage V_{BDG} in its 8 nA version achieved at schematic and layout level and in the nominal condition. The results achieved at schematic level show a mean value of the reference voltage equal to 404.78 mV with a standard deviation of 1.04 mV that are equal to the layout-level achieved ones.

The impact of the mismatch on V_{REF} turned out in a mean value of the reference voltage equal to 404.68 mV with a standard deviation of 1.19 mV which are close to the values achieved by considering the overall circuit. These results also prove that the mismatch due to the transistor into the output buffer does not have any impact on the reference voltage.

```
1 #.DCMISMATCH  V(BDG) SORT_REL = 1.000000e-03 NSIGMA = 1.000000e+00
2
3 Analysis results:
4
5 Output DC value                    :     4.0478E-01 Volt
6 Total output deviation             : +/- 1.0352E-03 Volt
7 Output deviation due to the
8 contributors in the report table   : +/- 1.0352E-03 Volt
9
10
```

Fig. 91. Mismatch impact on the V_{BDG} (8 nA version) at schematic level.

```
1 #.DCMISMATCH  V(BDG) SORT_REL = 1.000000e-03 NSIGMA = 1.000000e+00
2
3 Analysis results:
4
5 Output DC value                    :     4.0478E-01 Volt
6 Total output deviation             : +/- 1.0352E-03 Volt
7 Output deviation due to the
8 contributors in the report table   : +/- 1.0352E-03 Volt
9
10
```

Fig. 92. Mismatch impact on the V_{BDG} (8 nA version) at layout level.

Transient response of the overall circuit has been investigated by stepping the supply voltage from 0 to 1.2 V, 3 V and 5 V for three different temperatures (T = –40 °C, 25 °C and 125 °C) in the typical corner. Fig. 93 shows the post-layout simulation results of the transient response at the start-up. As expected, the buffer output voltage in its 8 nA version follows the supply initially, and then, after the start-up of the voltage reference circuit, settles to the expected steady state value.

Fig. 93. Post-layout simulation results of the transient response of the V_{BDG} (8 nA version) at the start-up for different value of supply voltage and temperature (MOD. TYP.).

Once again, extensive simulations regarding the transient response of the buffer output voltage V_{BDG} in its 8nA version have been carried out adding a load current to the output node of the buffer by stepping the supply voltage from 0 to 1.2 V, 3 V and 5 V for three different temperatures (T = –40 °C, 25 °C and 125 °C) in the typical corner at schematic and layout level.

The achieved results (Fig. 94) show that the voltage V_{BG} settled the expected steady state under all condition also by adding a current on the output branch up to the maximum value of 1 μA.

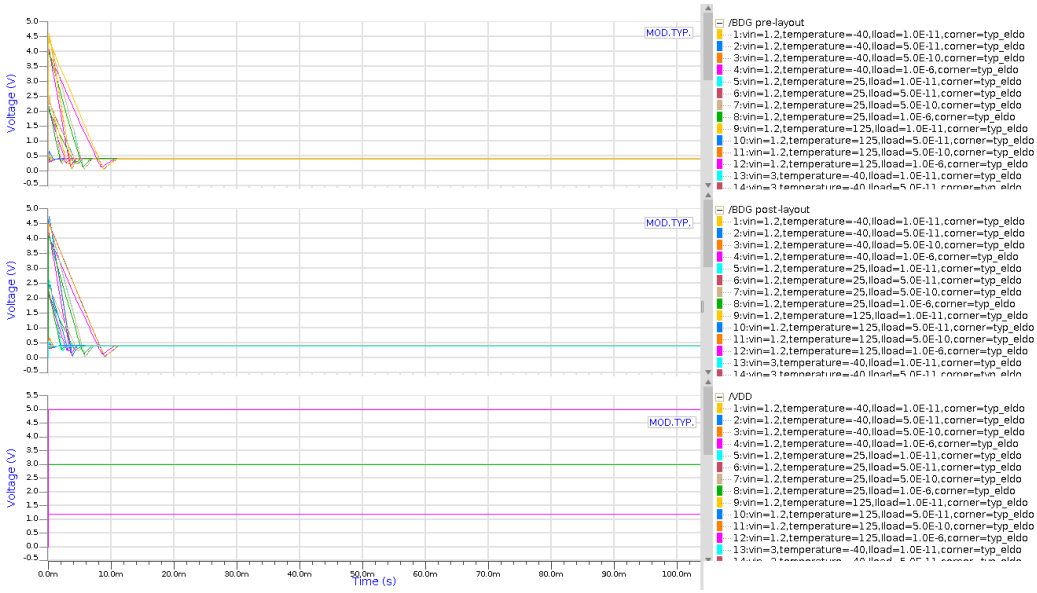


Fig. 94. Post-layout simulation results of the transient response at the start-up of the V_{BDG} (8 nA version) for different value of supply voltage, temperature, and load current (MOD. TYP.).

The performance parameters achieved by the reference voltage previously shown in Table XXVIII can be compared with those achieved by the circuit composed of voltage reference with the output buffer in its three versions (1nA, 3nA and 8 nA). Table XLVII show the comparison between the main performance parameters achieved by the four proposed architecture.

Although the current consumption and consequently the power dissipation have been doubled compared to the 3 nA version of the output buffer and quadrupled compared to the voltage reference circuit, the achieved performances of the alternative version of the output voltage buffer remain good. LS is perfectly preserved in all the proposed configuration while TC showing a little variation of only 17 ppm/°C passing from the voltage reference topology to the overall circuit composed of the voltage reference with the output buffer in its 8 nA version.

To conclude, although there is a considerable increase of current, the achieved results underline the robustness of the 8 nA of the proposed output voltage buffer and in general the robustness of the overall circuit.

TABLE XLVII: Performance comparison between the proposed voltage reference and the proposed voltage reference with the proposed output buffer (1 nA, 3 nA and 8 nA version).

	Proposed Voltage Reference	**Proposed Voltage Reference with Output Buffer (1 nA version)**	**Proposed Voltage Reference with Output Buffer (3 nA version)**	**Proposed Voltage Reference with Output Buffer (8 nA version)**
Technology (nm)	160	160	160	160
Minimum VDD (V)	1.2	1.2	1.2	1.2
VDD (V)	1.2 to 5	1.2 to 5 V	1.2 to 5	1.2 to 5
Current consumption (nA)	41.38@1.2 V 41.85@5V	67.35@1.2 V 68.50@5V	94.91@1.2 V 95.85@5 V	193.66@1.2 V 195.91@5 V
Power (nW)	49.66@1.2 V 209.25@5V	80.82@1.2 V 342.5@5V	113.89@1.2 V 479.25@5 V	232.39@1.2 V 979.55@5 V
Minimum Power (nW)	49.66	80.82	113.89	232.39
Vref (mV)	404.68	405.15	404.96	404.81
Temperature range (°C)	[−40÷125]	[−40÷125]	[−40÷125]	[−40÷125]
TC (ppm/°C)	102	102	113	119
Line sensitivity (%/V)	0.102	0.082	0.081	0.08
PSRR (dB)	−49.88@1kHz −49.88@1MHz	--	--	--
Die Area (mm2)	0.04318	0.145927	0.145927	0.124326

2.6.5 Experimental Results

The chip photo of the proposed ultra-low power voltage reference with the proposed output buffer (1nA version) with an occupied area equal to $0.145\ mm^2$ is shown in Fig. 95. A set of five different die of the same run were implemented by using the BCD8sp technology which is a 160-nm CMOS bulk-technology provided by STMicroelectronics. Measurement at chip level have been performed to evaluate the performances of the proposed circuit under different supply voltage and temperature conditions. The overall measurement has been carried out by using a power supply generator to precisely set the supply voltage of both the voltage reference and its related PCB while a multimeter has been used to measure the reference voltage. Additionally, the temperature behavior of the reference voltage has been measured by using a temperature chamber consisting of a Thermostream tool which is able to precisely set the temperature during the measurement.

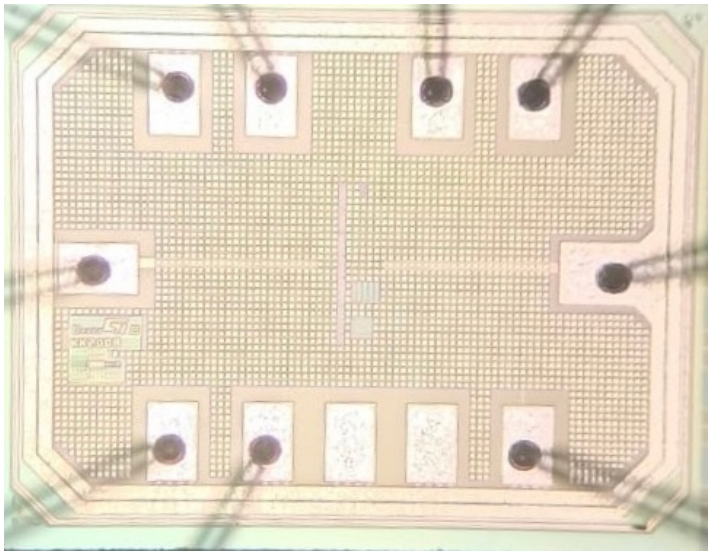


Fig. 95. Chip photo.

The output voltage of the proposed voltage reference with output buffer has been measured in the supply range from 1.2 to 5 V in steps of 200 mV (Fig. 96) at room temperature and the measured values are summarized in Table XLVIII.

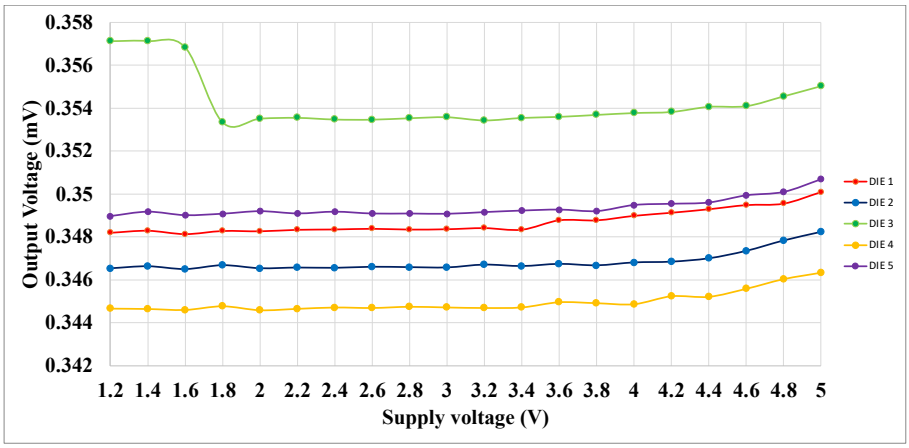


Fig. 96. Output voltage as a function of the supply voltage.

The average nominal value of the output voltage is 348.47 mV while the simulated value of the average reference voltage was 405.15 mV. This means that the measured reference voltage is less than 57 mV of the simulated one. This voltage variation is equal to that one that occurs on the measures of the voltage reference circuit. The reason of this slight variation besides in the MOS transistor used in low-current design as the proposed one which are not well-modeled and consequently affect the accuracy with which the output voltage value is reached. The output voltage variations in the supply voltage range [1.2÷5] V and values of the line sensitivity are summarized in Table XLVIII and Table XLIX, respectively. In the nominal condition, post-layout simulation results shown an output voltage variation of 1.57 mV and a LS equal to 0.102 % / V. 1.57 mV while measurement results show a reference voltage variation of 1.81 mV (average value) thus leading a LS equal to 0.14 % / V (average value) thus proving that silicon results are perfectly aligned to the simulation results.

TABLE XLVIII: Output voltage as a function of the supply voltage.

	DIE 1	DIE 2	DIE 3	DIE 4	DIE 5
VDD	**VOUT (V)**	**VOUT (V)**	**VOUT (V)**	**VOUT (V)**	**VOUT (V)**
1.2	0.348206	0.346535	0.357136	0.344665	0.34897
1.4	0.348301	0.346632	0.357141	0.344648	0.349175
1.6	0.348146	0.346501	0.356847	0.344604	0.349012
1.8	0.348289	0.346681	0.353353	0.344774	0.349081
2	0.348276	0.346539	0.353528	0.34459	0.3492
2.2	0.348345	0.346571	0.353564	0.344655	0.349094
2.4	0.348361	0.346558	0.353486	0.344718	0.349176
2.6	0.348393	0.346608	0.353479	0.344695	0.34909
2.8	0.348356	0.346589	0.353546	0.344752	0.349091
3	0.348372	0.346577	0.353592	0.344719	0.349077
3.2	0.348424	0.346709	0.353444	0.344695	0.349157
3.4	0.348351	0.346642	0.35356	0.344722	0.349229
3.6	0.348786	0.346743	0.35361	0.344964	0.349276
3.8	0.348785	0.346676	0.353701	0.344919	0.349204
4	0.348994	0.346812	0.353789	0.344873	0.349491
4.2	0.349138	0.346848	0.353838	0.345244	0.349549
4.4	0.349301	0.347006	0.354076	0.345219	0.349609
4.6	0.349493	0.347356	0.354109	0.345594	0.349945
4.8	0.349562	0.347844	0.354566	0.346046	0.350107
5	0.350098	0.348249	0.355041	0.346348	0.350701

TABLE XLIX: Reference voltage variations and line sensitivity in the supply voltage range [1.2÷5] V

	ΔVOUT (V)	LS (%/V)
DIE 1	0.00189172	0.001429
DIE 2	0.00171397	0.001301
DIE 3	0.00209443	0.001559
DIE 4	0.00168303	0.001285
DIE 5	0.00173048	0.001305

The output voltage and the supply current for two different dies as a function of the temperature in the range [–40÷125] °C are shown in Fig. 98 and 99, respectively. Experimental results of the reference voltage variation (in terms to peak-to-peak voltage) and Temperature Coefficient (TC) for different value of supply voltage and for two different dies are summarized in Table LI and Table LII, respectively. In the nominal condition, post-layout simulation results have been shown a reference voltage variation in temperature of 6.85 mV thus allowing to a achieve a TC equal to 102.47 ppm/°C. Experimental results shows an output voltage variation in temperature of 23.7 mV with a TC of 406 ppm/°C. The achieved results turn out in a TC four times higher than the simulated one which results to compromise the temperature behavior of the voltage reference circuit. The large variation is essentially due to the assumption of 1 nA of current flowing into the differential pair of the output buffer which force transistor to work in a deep-subthreshold region. MOS transistor operating with this limited amount of current are not well modeled and they give rise large variations on the temperature behavior passing by simulation to measurement results.

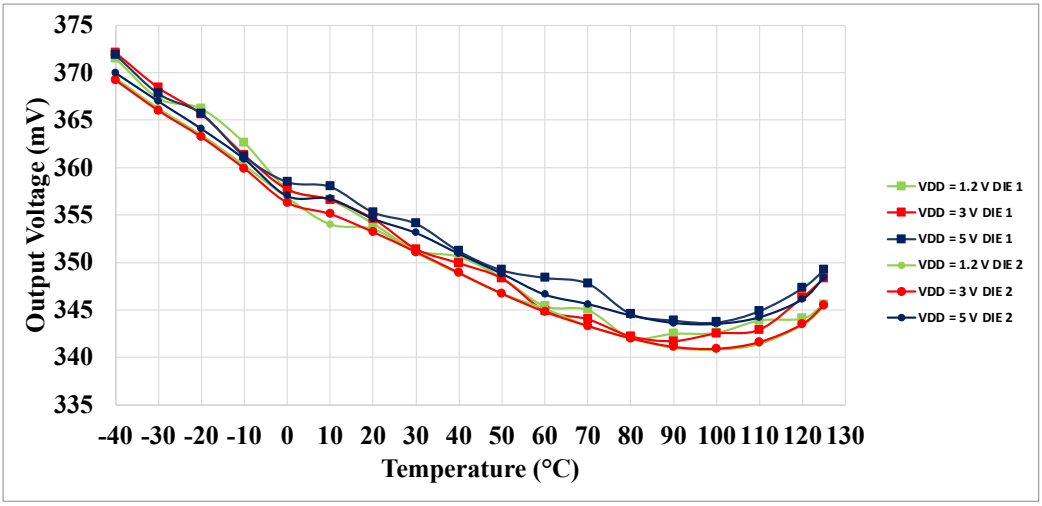


Fig. 97. Temperature dependence of the reference voltage for two different dies.

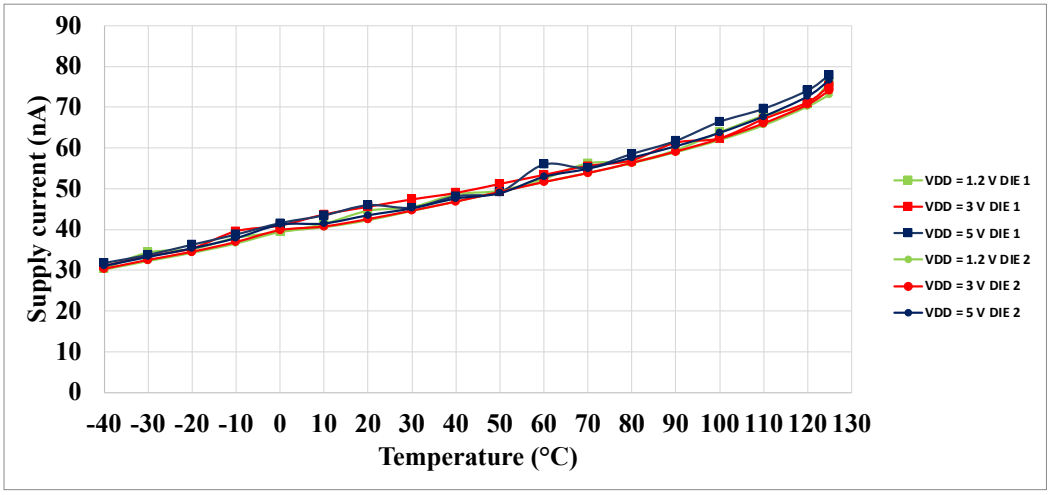


Fig. 98. Temperature dependence of the supply current for two different dies.

TABLE L: Reference voltage variations and TC as a function of temperature for different value of supply voltage (DIE 1)

DIE 1	VOUT (peak-to-peak) (mV)	TC (ppm / °C)
VDD = 1.2 V	25.9	443.2919993
VDD = 3 V	23.8	406.7750261
VDD = 5 V	22.7	387.2101255

TABLE LI: Reference voltage variations and TC as a function of temperature for different value of supply voltage (DIE 2)

DIE 2	VOUT (peak-to-peak) (mV)	TC (ppm / °C)
VDD = 1.2 V	24.1	413.1841756
VDD = 3 V	23.7	406.6714712
VDD = 5 V	21.6	369.1739732

Experimental results on the supply current I_q at different value of supply voltage and temperature for two dies under measurement are summarized in Table XXXIV and Table XXXV, respectively.

TABLE LII: Measured supply current at different value of supply voltage and temperature (DIE 1)

Iq (nA) DIE 1	T = – 40 °C	T = 25 °C	T = 125 °C
VDD = 1.2 V	30.4	44.6	76
VDD = 3 V	31	45.5	75.1
VDD = 5 V	31.7	45.9	77.9

TABLE LIII: Measured supply current at different value of supply voltage and temperature (DIE 2)

Iq (nA) DIE 2	T = – 40 °C	T = 25 °C	T = 125 °C
VDD = 1.2 V	30.2	42.3	73.1
VDD = 3 V	30.3	42.5	74.1
VDD = 5 V	31.1	43.5	76.6

The simulated nominal value of the supply current of the overall circuit was 68.14 nA while the value of the current variation was 80 nA in the temperature range [–40÷125] °C (at V_{DD} = 3 V). The measured value of the supply current is 44 nA while the current variation is 44 nA in the temperature range [–40÷125] °C (at V_{DD} = 3 V). The measured supply current is the half of the simulated one thus justifying the reason why temperature behavior is not preserved in the overall circuit.

At room temperature (T = 25 °C), the simulated supply current I_q (DIE 1) changes from 68.5 nA to 67.35 nA by changing the supply from 1.2 V to 5 V showing a total current variation of 1.15 nA in the overall supply voltage range. This result is confirmed by experimental results where the supply current Iq changes from 44.6 nA to 45.9 nA thus showing a total current variation of 1.3 nA in the overall supply range.

To conclude, the performance parameters achieved by the reference voltage has been compared to the one achieved by the circuit composed of voltage reference with the output buffer in Table XLV. The same comparison can be made by adding the measurement results as shown in Table LIV. The ultra-low power output buffer preserves the measured reference voltage value which is 348 mV in both circuits. The goal of the circuit is given by the supply current consumption which is always stable by changing the supply current and equal to 45 nA by considering the overall circuit (voltage reference and output buffer). The current consumption given by the overall circuit is 20 nA higher compared to the one achieved by the reference circuit which means that the output buffer adds only 20 nA to the reference circuit. Another important result of the proposed topology besides in the achieved LS which is always 0.14 %/V also by considering the overall circuit that means that the output buffer preserves the supply voltage behaviour of the voltage reference.

The achieved measurement results underline that the proposed low-power output buffer could be a good solution to complement the proposed low-power voltage reference thanks to its insensitive to process and supply voltage variations and to the possibility to preserve the power consumption of the reference circuit.

TABLE LIV: Performance comparison between the proposed voltage reference and the proposed voltage reference with the proposed output buffer (simulation and experimental results)

	Proposed Voltage Reference (simulated)	**Proposed Voltage Reference with Output Buffer (simulated)**	**Proposed Voltage Reference (measured)**	**Proposed Voltage Reference with Output Buffer (measured)**
Year	2023	2023	2023	2023
Technology (nm)	160	160	160	160
Minimum VDD (V)	1.2	1.2	1.2	1.2
VDD (V)	1.2 to 5	1.2 to 5 V	1.2 to 5	1.2 to 5 V
Current consumption (nA)	41.38@1.2 V 41.85@5V	67.35@1.2 V 68.50@5V	24.7@1.2 V 25.2@5V	44.6@1.2 V 45.9@5V
Power (nW)	49.66@1.2 V 209.25@5V	80.82@1.2 V 342.5@5V	29.64@1.2 V 126@5V	53.52@1.2 V 229.5@5V
Minimum Power (nW)	49.66	80.82	29.64	53.52
Vref (mV)	404.68	405.15	348	348.47
Temperature range (°C)	[−40÷125]	[−40÷125]	[−40÷125]	[−40÷125]
TC (ppm/°C)	102	102	134.37	406
Line sensitivity (%/V)	0.102	0.082	0.14	0.14
PSRR (dB)	−49.88@1kHz −49.88@1MHz	--	−49.88@1kHz* −49.88@1MHz*	--
Die Area (mm2)	0.04318	0.145927	0.04318	0.145927

2.7 28-nm CMOS Resistor-Less Voltage Reference with Process Corner Compensation for Biomedical Application

A resistor-less voltage reference which exploits the difference between the threshold voltage of different transistor operating in subthreshold region together with the use of a very scaled technology to achieve both power consumption in the nano-Watt range and low area occupation has been investigated. Since the process sensitivity of the reference voltage is mainly due to the susceptibility of the threshold voltage to PVT variations, trimming is necessary to get rid of these variations. A simple fully analog compensation approach suitable to cover the four basic corners has been proposed to complement the resistor-less voltage reference.

2.7.1 Circuit Description

The architecture of the proposed voltage reference that consists of a current reference and a programmable active load is shown in Fig. 100. The circuit is a modified version of the solution proposed in [18] where a fixed load and an additional start-up circuit have been adopted. In this proposed solution, the start-up circuit is replaced by a single capacitor C_1 which is charged by a time constant imposed by the diode-connected transistor M_5 which acts like a resistor. Additionally, the compensation of the process corner is achieved by a programmable active load which consists of three different branches $M_{8\text{-}9}$, $M_{11\text{-}12}$ and $M_{14\text{-}16}$ enabled by the switch M_{10}, M_{13} and M_{14} together with their control voltages V_1, V_2 and V_3, respectively.

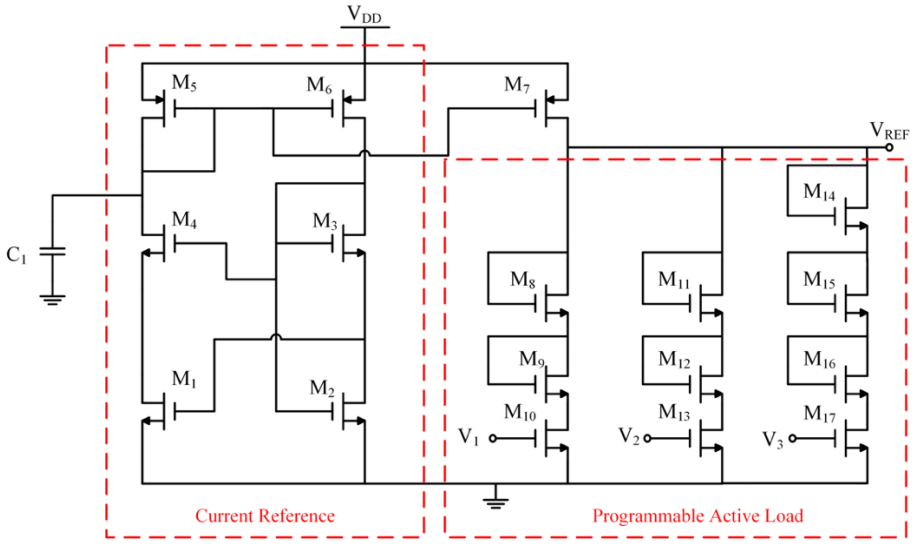


Fig. 99. Schematic of the voltage reference with the proposed programmable active load.

All MOSFET transistors are biased in their subthreshold region and the bulk terminals are connected to V_{DD} and to ground for PMOS and NMOS, respectively. Additional transistor M_4 with the function of shielding M_1 from the supply voltage and consequently to avoid its breakdown has been added. In this way, the drain current flowing into M_1 become quite insensitive to supply voltage variations thus decreasing the overall line sensitivity of the voltage reference. Transistor with different threshold voltages have been exploited, particularly all the devices are ultra-low voltage threshold (ULVT) transistor except M_2 which is a standard voltage threshold (SVT) transistor. Table LVI summarized information regard the chosen technology and the typical threshold voltages value of the different chosen transistors. Additionally, transistor sizes of the overall voltage reference schematic are shown in Table LVII while the value of the integrated capacitor C_1 is 121.3 fF.

TABLE LV: Voltage ranges and threshold voltages of TSMC technology.

Technology	TSMC 28 nm CMOS technology		
	Voltage range	**V_{TH}-NMOS**	**$\lvert V_{TH}\rvert$-PMOS**
ULVT-MOSFET	$V_{GS} \geq 0\ V$, $V_{DS} \leq 0.9\ V$	358 mV	332 mV
SVT-MOSFET	$V_{GS} \geq 0\ V$, $V_{DS} \leq 2\ V$	542 mV	445 mV

TABLE LVI: Transistor sizes of the 28-nm proposed voltage reference

Transistor	**W/L (μm / μm)**
M_1	0.2 / 0.7
M_2	0.64 / 1.6
M_3	0.3 / 0.04
M_4	10 / 0.3
$M_{5\text{-}6\text{-}7}$	0.64 / 2
$M_{8\text{-}9}$	0.46 / 0.6
$M_{10\text{-}13\text{-}17}$	0.32 / 0.15
M_{11}	0.28 / 0.3
M_{12}	0.1 / 0.19
M_{14}	0.32 / 1
$M_{15\text{-}16}$	0.1 / 0.5

2.7.2 Current Reference

The current reference section shown in Fig. 100 is used to generate a refence current insensitive to both supply voltage and temperature variations which consequently leas to a reference voltage V_{REF} insensitive to these variations. It can be noted that this current section has been proposed in [18] and it is also the same previously shown and analyzed in the last paragraph 2.5. However, a brief analysis shall be made specific to this proposed reference voltage.

By inspection of the circuit in Fig. 100, the self-biased configuration is composed of MOS transistor $M_{1\text{-}3}$ among which a linear combination between their gate-source voltages is generated and expressed in equation (65).

$$V_{GS2} = V_{GS1} + V_{GS3} \tag{65}$$

By using the expression of the gate-source voltages of the transistors operating in subthreshold region shown in equation (36), equation (65) can be rewritten as follows:

$$n_2 V_T \ln\left(\frac{L_2}{W_2}\frac{I_{D2}}{\mu_2 C_{ox} V_T^2}\right) = \Delta V_{TH} + n_1 V_T \ln\left(\frac{L_1}{W_1}\frac{I_{D1}}{\mu_1 C_{ox} V_T^2}\right) + n_3 V_T \ln\left(\frac{L_3}{W_3}\frac{I_{D3}}{\mu_3 C_{ox} V_T^2}\right) \tag{66}$$

where $\Delta V_{TH} = V_{TH1} + V_{TH3} - V_{TH2}$.

Assuming the electron mobilities in (37) identical ($\mu = \mu_1 = \mu_2 = \mu_3$) and the same aspect ratio of the current mirror made up by transistors $M_{5\text{-}6}$, the generated current can be expressed in the following form:

$$I_{D1} = Q^{1/\Sigma_n} \mu V_T^2 \exp\left(-\frac{\Delta V_{TH}}{V_T \Sigma_n}\right) \tag{67}$$

where $Q = a^{m_2 - m_3}\left[\frac{(W/L)_1^{n_1}\cdot(W/L)_3^{n_3}}{(W/L)_2^{n_2}} \cdot C_{ox}\right]$, $\Sigma_n = n_1 + n_2 + n_3$ and $a = (W/L)_{5,6}$.

To avoid the device breakdown of ultra-low voltage threshold voltage transistor M_1 when the supply voltage V_{DD} will be higher than 0.9 V, an additional clamping NMOS standard voltage transistor M_4 has been included. Additionally, NMOS transistor $M_{5\text{-}6}$ in the current mirror are also standard threshold voltage transistor to allow to allow the voltage reference to operate for higher supply voltage value greater than the 0.9 V (breakdown voltage of the ULVT MOSFET).

2.7.3 Active Load and Temperature Compensation

The nominal active load is made up by two diode-connected transistors in series $M_{8\text{-}9}$ which are used to provide the nominal reference voltage around 600 mV. The reference current expressed in equation (67) is mirror by M_7 into the nominal active load branch. Assuming the same aspect ratio of transistor $M_{5\text{-}7}$ as follows $(W/L)_5 = (W/L)_6 = (W/L)_7$, the current flowing into the drain of M_7 became equal to the current flowing into the drain of M_5 which is the reference current. The expression of the nominal reference voltage provided by the two diode-connected transistor $M_{8\text{-}9}$ can be expressed as follows:

$$V_{REF} = V_{GS8} + V_{GS9} = V_{TH8} + n_8 V_T \ln\left(\frac{I_{D7}}{\left(\frac{W}{L}\right)_8 C_{ox}\mu_n V_T^2}\right) + V_{TH9} + n_9 V_T \ln\left(\frac{I_{D7}}{\left(\frac{W}{L}\right)_{19} C_{ox}\mu_n V_T^2}\right) = V_{TH8} +$$

$$n_8 V_T \ln\left(\frac{Q^{1/\Sigma_n}\mu V_T^2 \exp\left(-\frac{\Delta V_{TH}}{V_T\Sigma_n}\right)}{\left(\frac{W}{L}\right)_8 C_{ox}\mu_n V_T^2}\right) + V_{TH9} + n_9 V_T \ln\left(\frac{Q^{1/\Sigma_n}\mu V_T^2 \exp\left(-\frac{\Delta V_{TH}}{V_T\Sigma_n}\right)}{\left(\frac{W}{L}\right)_9 C_{ox}\mu_n V_T^2}\right) \tag{68}$$

Being both NMOS transistors M_8 and M_9 ULVT devices with the same sizes, their design and process parameters are identical. Therefore, the expression of the reference voltage became:

$$V_{REF} = 2\,V_{GS8,9} = \; 2\,V_{TH8,9} + n_{8,9}V_T \ln\left(\frac{I_{D7}}{\left(\frac{W}{L}\right)_{8,9} C_{ox}\mu_n V_T^2}\right) =$$

$$= 2\,V_{TH8,9} + 2\,n_{8,9}V_T \ln\left(\frac{Q^{1/\Sigma_n}\mu V_T^2 \exp\left(-\frac{\Delta V_{TH}}{V_T \Sigma_n}\right)}{\left(\frac{W}{L}\right)_{8,9} C_{ox}\mu_n V_T^2}\right) \tag{69}$$

Consequently, the final expression of the nominal reference voltage is given by equation (70).

$$V_{REF} = 2\,V_{TH8,9} + \; 2n_{8,9}V_T \ln\left(\frac{Q^{1/\Sigma_n}}{\left(\frac{W}{L}\right)_{8,9} C_{ox}}\right) - 2\,\frac{n_{8,9}}{\Sigma_n}\Delta V_{TH} \tag{70}$$

Temperature dependence of the reference voltage is related to the temperature dependence of both threshold voltage and thermal voltage previously shown in equation (41) and (42), respectively.

Under these premises, temperature coefficients of threshold and thermal voltages can be obtained by deriving these two voltages with respect to temperature and by setting the obtained values equal to zero. Finally, temperature dependence of the reference voltage can be achieved by setting $\frac{\partial V_{REF}}{\partial T} = 0$ and $V_{BS} = 0$, thus obtaining the expression of the TC of the proposed reference circuit.

$$TC = 2\,\frac{k_{t8,9}}{T_0} + 2\,\frac{n_{8,9}k}{q} \ln\left(\frac{Q^{1/\Sigma_n}}{\left(\frac{W}{L}\right)_{8,9} C_{ox}}\right) - 2\,\frac{n_{8,9}}{\Sigma_n}\left(\frac{k_{t1}}{T_o} + \frac{k_{t3}}{T_o} - \frac{k_{t2}}{T_o}\right) \tag{71}$$

where $k_{t8,9}$ is temperature coefficient of MOS transistor $M_{8,9}$ while k_{t1}, k_{t2} and k_{t3} are temperature coefficient of MOS transistors M_1, M_2 and M_3 respectively.

Temperature coefficient of the reference voltage depends on the combination between technological parameter and design parameter. Technological parameters are connected to the process technology and once it has been chosen, they cannot be modified.

At the end, the simplified expression of TC can be obtained by considering MOS transistors operating in subthreshold region having the same value of *n* parameters. In this way, it can be possible to set $n_{18} \approx n_{19}$ and consequently $\frac{n}{\Sigma_n} \approx 1$. At the same time, by considering the same temperature coefficient of the MOS transistors operating in subthreshold region, it can be possible to set: $k_{t1} \approx k_{t2} \approx k_{t3} \approx k_{t18} \approx k_{t19}$. Therefore, the simplified expression of the Temperature Coefficient becomes:

$$TC = 2\,\frac{nk}{q} \ln\left(\frac{Q^{1/\Sigma_n}}{\left(\frac{W}{L}\right)_{8,9} C_{ox}}\right) \tag{72}$$

By inspection of equation (72), temperature coefficient is logarithmically dependent on the MOS transistors sizes of the transistor in the active load. Therefore, temperature compensation can be achieved by choosing large lengths value of the diode connected transistor M_8 and M_9 into the nominal active load section which constituted the main temperature compensation approach followed in this design.

2.7.4 Process Corner Compensation

Transistors working in subthreshold region show a significant variation of their threshold voltages due to the process corner that may result in a considerable reference voltage variation which can be up to 65% in the worst process corner. To mitigate this problem a trimming strategy that consist of a programmable active load has been added to the proposed voltage reference.

In the proposed design, the reference voltage is strictly related to the threshold voltage of the MOS transistors as shown in equation (70). This means that any variations on the threshold voltage due to

the process corner may result in the variation on the reference voltage. Process variation can be verified within the same wafer as in the case of die-to-die (or inter-die) variations or within the same die as in the case of within-die (or intra-die) variations. In any case, the problematic is not trivial and may lead to a yield decrease of the voltage reference performances. A way to ease process variation is to prevent them during the simulation phase of the design by using the corner model of the transistor. In fact, the simulation cannot be carried out taking into account only the typical model of the transistor but also the unfavorable ones. In the proposed solution, the corner models represent the case where threshold voltage of the transistors is higher or lower than the nominal one. For the same overdrive, the fast (F) corner occurs when the threshold voltage is the smallest one thus resulting in a higher current. On the contrary, the slow (S) corner occurs when the threshold voltage is highest one thus leading a smallest current. Fast and slow models of the transistors with their possible combination which are: SS (slow NMOS and slow PMOS), FS (fast NMOS and slow PMOS), SF (slow NMOS and fast PMOS), and FF (fast NMOS and fast PMOS) allow to identify the worst case as regards the threshold voltage. To guarantee the proper operation of the voltage reference it must be ensure the optimization of the circuit in all the corner models.

In the favorable condition, the die lies in its typical corner and consequently the reference voltage V_{REF} is the expected one. When the die lies in the worst corner the reference voltage is subject to a variation around its nominal value and a trimming strategy need to be added to overcome this variation. The proposed trimming solution on the active load allow to overcome corner variations on the nominal reference voltage.

The programmable active load is composed of three branches as shown in Fig. 91 which can be enable though switches $M_{10,}$ M_{13} and M_{17} driven by external voltage V_1, V_2 and V_3, respectively. The first branch (transistor M_8 and M_9) is enabled by the switch M_{10} driven by the external voltage V_1 and is used to provide the reference voltage V_{REF} int the nominal corner (NOM).

The second branch (transistor M_{11} and M_{12}) is enabled by the switch M_{13} driven by the external voltage V_2 and is used to provide the reference voltage V_{REF} into the corners where the NMOS transistor is slow (SS and SF). Similarly, the third branch (transistor M_{14}, M_{15} and M_{16}) is enabled by the switch M_{17} driven by the external voltage V_3 and is used to provide the reference voltage V_{REF} into the corners where the NMOS transistor is fast (FF and FS). The trimming process require that only one voltage among V_1, V_2 and V_3 will be set to V_{DD} while the other two voltages will be grounded. When the nominal case occurs the first branch is enabled while the other two are grounded otherwise when the reference voltage is far from the nominal one its value can be restored by enable the second or the third branches, respectively.

The analytical expression of V_{REF} related to the second and third load and consequently their expression of the TC can be found by using (70) and (71), respectively thus resulting in equation (73) (74) for the SS and SF models and in equation (75) and (76) for the FF and FS models.

$$V_{REF(SF,SF)} = V_{GS11} + V_{GS12} =$$

$$= V_{TH11} + V_{TH12} + n_{11}V_T \ln\left(\frac{I_{D7}}{\left(\frac{W}{L}\right)_{11} C_{ox}\mu_n V_T^2}\right) + n_{12}V_T \ln\left(\frac{I_{D7}}{\left(\frac{W}{L}\right)_{12} C_{ox}\mu_n V_T^2}\right) =$$

$$= V_{TH11} + V_{TH12} + n_{11}V_T \ln\left(\frac{Q^{1/\Sigma_n}\mu V_T^2 \exp\left(-\frac{\Delta V_{TH}}{V_T \Sigma_n}\right)}{\left(\frac{W}{L}\right)_{11} C_{ox}\mu_n V_T^2}\right) + n_{12}V_T \ln\left(\frac{Q^{1/\Sigma_n}\mu V_T^2 \exp\left(-\frac{\Delta V_{TH}}{V_T \Sigma_n}\right)}{\left(\frac{W}{L}\right)_{12} C_{ox}\mu_n V_T^2}\right) \quad (70)$$

$$TC_{(SF,FS)} = \frac{k_{t11}}{T_0} + \frac{k_{t12}}{T_0} + \frac{n_{11}k}{q}\ln\left(\frac{Q^{1/\Sigma_n}}{\left(\frac{W}{L}\right)_{11} C_{ox}}\right) + \frac{n_{12}k}{q}\ln\left(\frac{Q^{1/\Sigma_n}}{\left(\frac{W}{L}\right)_{12} C_{ox}}\right) - \frac{n_{11}}{\Sigma_n}\left(\frac{k_{t1}}{T_o} + \frac{k_{t3}}{T_o} - \frac{k_{t2}}{T_o}\right) - \frac{n_{12}}{\Sigma_n}\left(\frac{k_{t1}}{T_o} + \frac{k_{t3}}{T_o} - \frac{k_{t2}}{T_o}\right) \quad (71)$$

$$V_{REF(FF,FS)} = 2\,V_{GS15,16} + V_{GS14} =$$

$$= 2\,V_{TH15,16} + V_{TH14} + n_{15,16}V_T \ln\left(\frac{I_{D7}}{\left(\frac{W}{L}\right)_{15,16} C_{ox}\mu_n V_T^2}\right) + n_{14}V_T \ln\left(\frac{I_{D7}}{\left(\frac{W}{L}\right)_{14} C_{ox}\mu_n V_T^2}\right) =$$

$$= 2\,V_{TH15,16} + 2\,n_{15,16}V_T \ln\left(\frac{Q^{1/\Sigma_n}\mu V_T^2 \exp\left(-\frac{\Delta V_{TH}}{V_T \Sigma_n}\right)}{\left(\frac{W}{L}\right)_{15,16} C_{ox}\mu_n V_T^2}\right) + V_{TH14} + n_{11}V_T \ln\left(\frac{Q^{1/\Sigma_n}\mu V_T^2 \exp\left(-\frac{\Delta V_{TH}}{V_T \Sigma_n}\right)}{\left(\frac{W}{L}\right)_{14} C_{ox}\mu_n V_T^2}\right)$$

(72)

$$TC_{(SF,FS)} = 2\frac{k_{t15,16}}{T_0} + \frac{k_{t14}}{T_0} + 2\frac{n_{15,16}k}{q}\ln\left(\frac{Q^{1/\Sigma_n}}{\left(\frac{W}{L}\right)_{11} C_{ox}}\right) + \frac{n_{14}k}{q}\ln\left(\frac{Q^{1/\Sigma_n}}{\left(\frac{W}{L}\right)_{12} C_{ox}}\right) - 2\frac{n_{15,16}}{\Sigma_n}\left(\frac{k_{t1}}{T_o} + \frac{k_{t3}}{T_o} - \frac{k_{t2}}{T_o}\right) - \frac{n_{14}}{\Sigma_n}\left(\frac{k_{t1}}{T_o} + \frac{k_{t3}}{T_o} - \frac{k_{t2}}{T_o}\right) \quad (73)$$

Unlike the nominal case, in the worst condition the optimization of the transistor sizes of the various load was executed during simulation and not before. This is because all the temperature effect are modelized in the transistor model and their effects can be precisely analyzed only during the simulation phase.

2.7.5 Sensitivity to Supply Voltage Variations

The evaluation of the reference voltage sensitivity to supply voltage variation can be evaluated by using the Line Sensitivity LS already shown in equation (52). Once again, the LS can be optimized by reducing the sensitivity to supply voltage variation on the reference current which results in the variation of the reference voltage. This variation has been mitigated during the design by choosing large length value of the transistor belonging to the current reference and to the current mirror ($M_{5\text{-}7}$).

2.7.6 Post-Layout Simulation Results

The voltage reference with proposed programmable active load was designed by using a standard 28-nm CMOS bulk technology provided by TSMC while post-layout simulation results have been carried out by using Cadence Virtuoso tool. The layout of the overall circuit is shown in Fig. 101 and its occupied area is 15.32 μm x 10.21 μm.

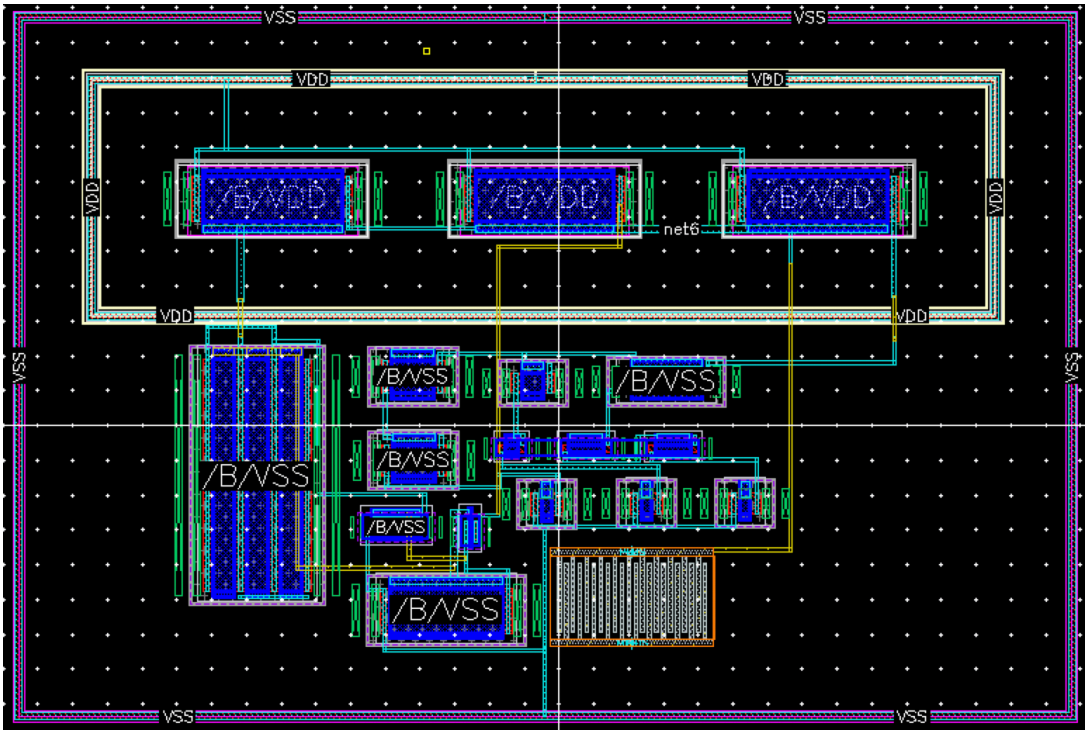


Fig. 100. Layout of the voltage reference with proposed programmable active load.

This voltage reference has been designed to be embedded in an implantable and biomedical electronic device. The overall circuit was designed to be implanted in the cerebral cortex with the main purpose to help the diagnosis of neurodegenerative disease. Implantable devices impose two bigger constraints: (1) a biomedical system must be least invasive as possible therefore low-area occupation is mandatory to reduce the impact to a minimum; (2) it must be operating without (or with a very small) battery by requiring the minimum power consumption in the nano-ampere range of the overall system. The adoption of a very scaled technology that is a 28-nm in the proposed design together with subthreshold approach represent the main approach followed in the proposed to overcome these restrictions. Additionally, since the system has been designed to be implanted in the human body, both the supply voltage and temperature range are not very wide as an industrial design. Although, the temperature is always stable and the average body temperature is around 36.5 °C, the proposed voltage reference has been simulated to work properly in the temperature range [20÷60] °C. At the same time, the adoption of a very scaled technology imposes limitation on the maximum value of the supply voltage which can be reached without achieve the device breakdown. Therefore, the supply range in which the voltage reference has been simulated was restricted to [0.8÷2] V.

Preliminary post-layout simulation of the reference voltage in the supply voltage operating range has been carried out at room temperature (T = 27 °C) by using the nominal model of the transistor as shown in Fig. 102. The nominal value of the reference voltage is equal to 628 mV and the maximum reference voltage variation is equal to 7 mV in the supply range [0.8÷2] V, thus leading to a line sensitivity of 0.009 %/V.

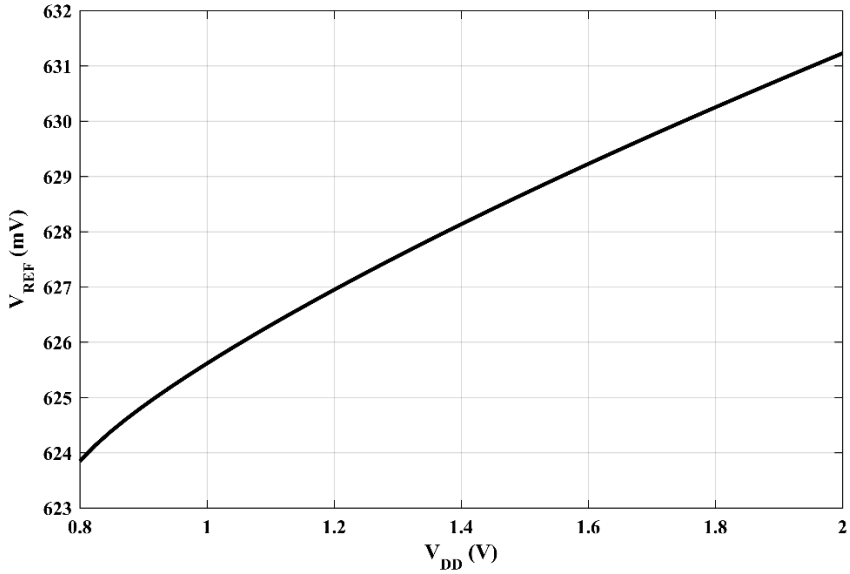


Fig. 101. Voltage reference V_{REF} as a function of the supply voltage.

Additionally, the reference voltage behavior in temperature is shown in Fig. 103 by setting the supply equal to 1.4 V and by using the nominal model of the transistor. The reference voltage variation on temperature is quite restricted and it is only 145 μV in the temperature range from 20 °C to 60 °C. Once again, it is worth nothing that this temperature range is adequate for the target application being the average body temperature equal to 36.5 °C. At the same time, the evaluation of the temperature coefficient can be made by using equation (55) which leads a value of 6 ppm/°C. The highest value of the TC in a very small range of temperature highlight that this voltage reference is not highly performing in temperature. Anyway, biomedical application like this one does not require a voltage reference which work in a wide range of temperature since the temperature is always around the temperature of the human body which is the reason why temperature behavior is not optimized during the design.

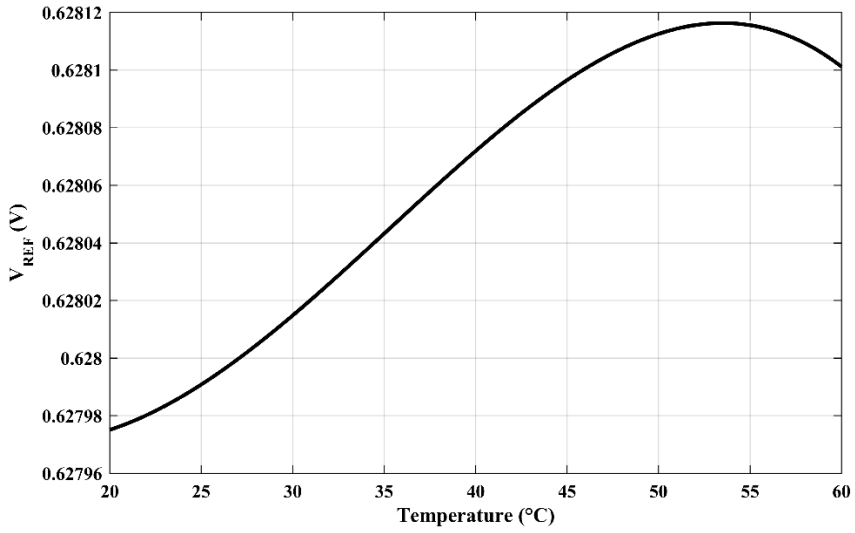


Fig. 102. Temperature behavior of the reference voltage V_{REF}.

Temperature dependence of the reference voltage V_{REF} in the temperature range from 20 °C to 60 °C for different supply voltage (V_{DD} = 0.8 V, 1.1 V, 1.4 V, 1.7 V and 2 V) by using the nominal model of the transistor has been exploited and the achieved results are shown in Fig 104. The reference voltage value at T = 25°C, the voltage variations in temperature and their related TC are summarized

in Table LVIII. The achieved results shown a slight deviation on the nominal value of the reference voltage which is less than 10 mV thus not affecting the TC in a clear manner.

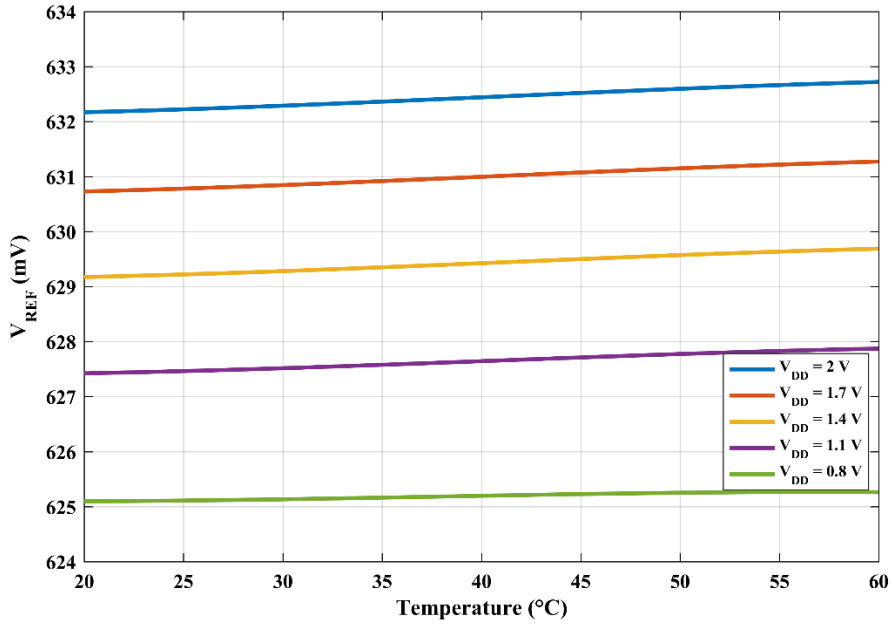


Fig. 103. Temperature dependence of the reference voltage in the nominal corner by changing the supply voltage.

TABLE LVII: The nominal reference voltage value at T = 25°C, voltage variations in the temperature range and TC.

	V_{DD} = 0.8 V	V_{DD} = 1.1 V	V_{DD} = 1.4 V	V_{DD} = 1.7 V	V_{DD} = 2 V
V_{REF} (mV)	623	626	628	630	632
ΔV_{REF} (μV)	139	84	127	142	145
TC (ppm/°C)	6	4	5	6	6

where $\Delta V_{REF} = V_{REF}$ (T = 60 °C) − V_{REF} (T = 20 °C).

Corner analysis has been carried out by using the corner models provided by the technology owner which are categorized has follows: nominal (NOM), slow-slow (SS), slow-fast (SF), fast-slow (FS), and fast-fast (FF).

The effect of the process corner on the reference voltage V_{REF} has been exploited by carrying out the corner analysis for V_{DD} ranging from 0.8 to 2 V at room temperature equal to 27 °C. By inspection of the Fig. 105, the nominal behavior of the reference voltage V_{REF} is around 600 mV as expected while a voltage variation of the reference voltage around 411 mV appears going from the slow corner of the NMOS transistor to the fast corner of the NMOS transistor. Particularly, a reference voltage value around 800 mV occurs under the SS and SF corners of the NMOS transistor while a reference voltage value around 400 mV occurs under the FF and FS corners of the NMOS transistor. The nominal value of the reference voltage achieved at V_{DD} = 1.4 V and the voltage variation for the different corners are summarized in Table LIX.

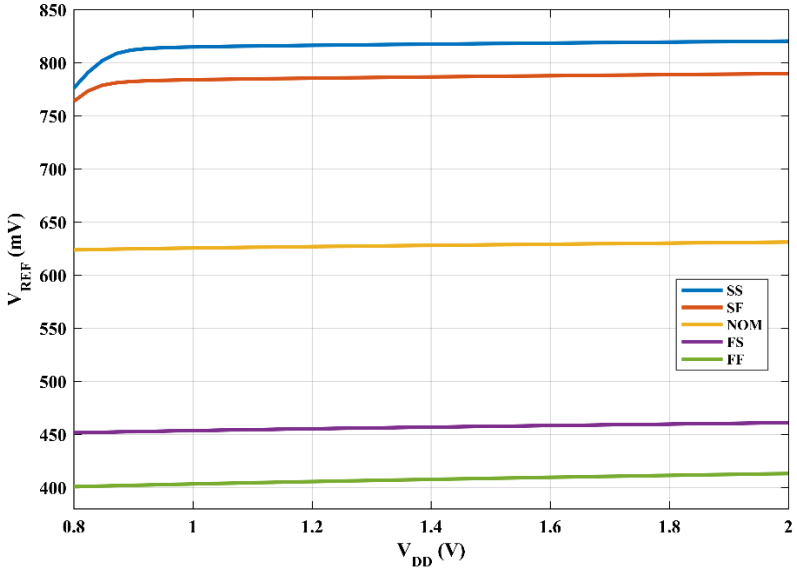


Fig. 104. Supply voltage dependence of the reference voltage V_{REF} over four basic corners without trimming strategy.

TABLE LVIII: Nominal value of the reference voltage and voltage variation in the supply voltage operating range by using different models (without trimming strategy).

	NOM	**SS**	**SF**	**FS**	**FF**
V_{REF} (mV)	628	818	787	456	406
ΔV_{REF} (mV)	7	44	26	10	12
LS (%/V)	0.009	0.04	0.03	0.02	0.02

where $\Delta V_{REF} = V_{REF}\ (V_{DD} = 2\ V) - V_{REF}\ (V_{DD} = 0.8\ V)$.

It is apparent that without process corner compensation the reference voltage is not process corner independent thus leading a wide variation around its nominal expected value. Table XLIII shows that the nominal value of the reference voltage changes from the minimum value of 406 mV under the FF corner to a maximum value of 818 mV under the SS corner thus leading a variation of the nominal reference voltage of 412 mV. The reference voltage dependence on the supply voltage shown in Table XLII highlight a minimum variation equal to 7 mV by using the nominal corner and a maximum voltage variation equal to 44 mV by using the SS corner. Therefore, the minimum value of the LS of 0.009 %/V was achieved by using the nominal corner while the maximum value of 0.04 %/V was achieved by using the SS corner.

Once the silicon is done, it is possible that the corner is not the nominal one thus impacting the nominal value of the reference voltage V_{REF}. At this aim, the proposed process corner compensation has been introduced on the active load to compensate these variations once the silicon is already done and to restore the nominal reference voltage. The effect of the trimming strategy on the reference voltage is shown in Fig. 106, where the reference voltage variation in the supply voltage operating range is exhibited.

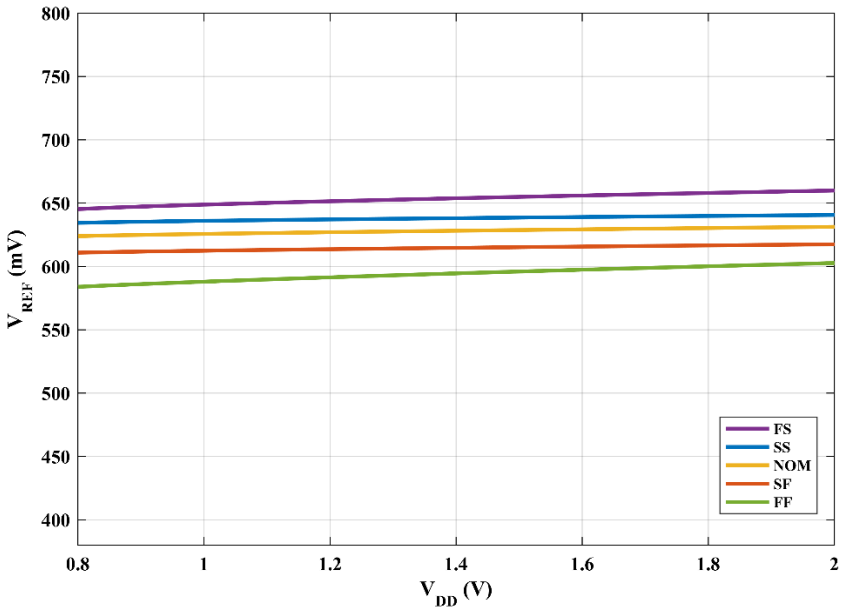


Fig. 105. Supply voltage dependence of the reference voltage V_{REF} over four basic corners with trimming strategy.

The nominal behavior of the reference voltage was achieved by using the first branch of the active load enabled by voltage V_1. The reference voltage under SS and SF corner was restored from 800 mV to the nominal one by using the second branch of the active load enabled by voltage V_2 while the reference voltage under FF and FS corners was restored from 400 mV to the nominal one by using the third branch of the active load enabled by voltage V_3. The nominal value of the reference voltage achieved at V_{DD} = 1.4 V and the voltage variation for the different corners obtained by using the trimming strategy are summarized in Table LX.

By passing form the FF to the SF corner which are related to the maximum and the minimum value of the nominal reference voltage, the voltage variation is contained within 40 mV which is 10.3 times lower than the voltage variation achieved without trimming strategy. The related results in terms of voltage dependence on the supply voltage are mitigated by trimming strategy thus leading a maximum voltage variation of 19 mV under FF corner and a minimum voltage variation of 6 mV under the SS (SF) corner. Therefore, the minimum value of the LS of 0.009 %/V was achieved by using the nominal corner while the maximum value of 0.01 %/V was achieved by using the FS corner.

TABLE LIX: Nominal value of the reference voltage and voltage variation in the supply voltage operating range by using different models (with trimming strategy).

	NOM	**SS**	**SF**	**FS**	**FF**
V_{REF} (mV)	628	638	615	651	590
ΔV_{REF} (mV)	7	6	6	14	19
LS (%/V)	0.009	0.008	0.008	0.01	0.03

where $\Delta V_{REF} = V_{REF}$ (V_{DD} = 2 V) − V_{REF} (V_{DD} = 0.8 V).

The temperature dependence on the supply current Iq has been also investigated in the T range from 20 °C to 60 °C for different value of supply voltage (V_{DD} = 0.8 V, 1.1 V, 1.4 V, 1.7 V and 2 V) by using the typical model. As shown in Fig 107, the nominal value of the supply current has been reached at V_{DD} = 1.4 V and T = 25 °C and it is equal to 19 nA with a total variation in the chosen

temperature range of 44 nA. The supply current values at different value of supply voltage and temperature are shown in Table LXI in which the supply current variations in these different cases are highlighted. It is apparent that the current consumption increases with temperature with a current variation around 44 nA in all conditions and it reach the maximum value of 61.6 nA under V_{DD}= 2 V and T = 60 °C. The supply current dependence on supply voltage is fairly small and its value is only 1.5 nA in the supply range from 0.8 V to 2 V at room temperature, while the maximum and the minimum variation equal to 4 nA and 1.2 nA are achieved under T equal to 60 °C and 20 °C, respectively.

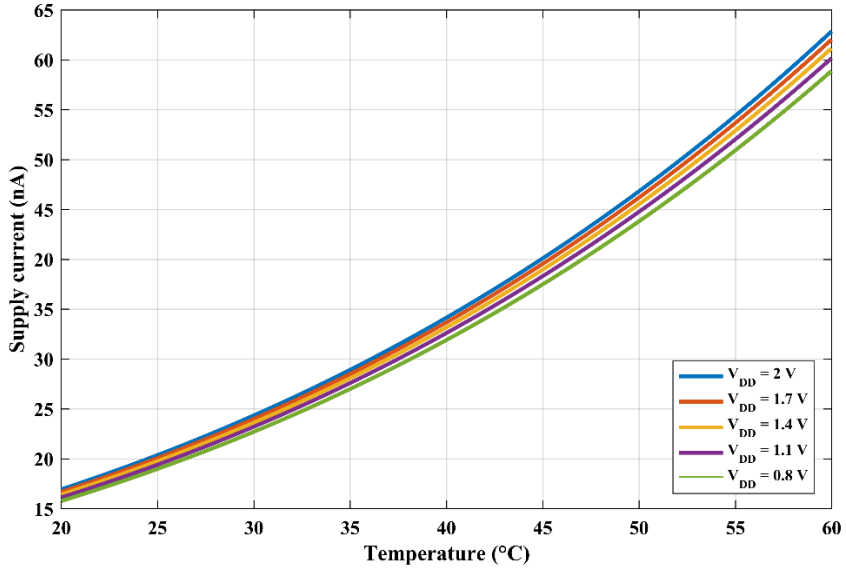


Fig. 106. Temperature dependence on the supply current at different value of supply voltage in the nominal corner.

TABLE LX: Supply current value at different supply voltage and temperature and overall current variations.

	V_{DD} = 0.8 V	**V_{DD} = 1.1 V**	**V_{DD} = 1.4 V**	**V_{DD} = 1.7 V**	**V_{DD} = 2 V**
I_q (nA) at T=20°C	15.5	15.8	16.1	16.4	16.7
I_q (nA) at T=25°C	18.6	19.1	19.4	19.8	20.1
I_q (nA) at T=60°C	57.6	58.8	59.8	60.7	61.6
ΔI_q (nA)	44	44	44	43	42

where $\Delta I_q = I_q$ (T=60°C) − I_q (T=20°C).

Post-layout simulation result of the equivalent output noise is shown in Fig. 108. The value of 25.04 $\mu V/\sqrt{H_z}$ has been reached at 10 Hz while the root mean square voltage noise is 158 μV in a bandwidth from 0.1 Hz to 10 Hz.

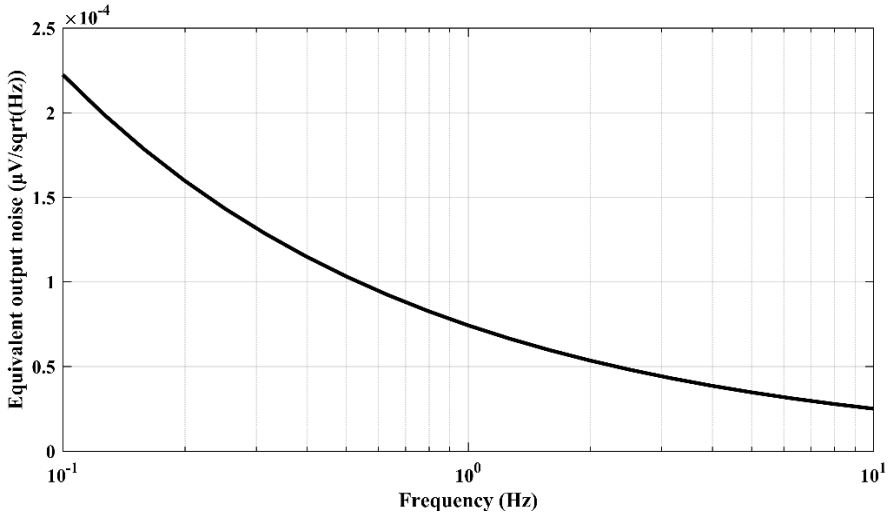


Fig. 107. Simulated equivalent output noise of the proposed voltage reference.

Finally, a Monte Carlo simulation on the reference voltage has been carried out under 1000 iteration by setting the supply voltage in the nominal condition. The distribution of the reference voltage is shown in Fig. 109 where it can be observed that the mean value of the reference voltage is 625 mV whit a standard deviation of 131 mV which leads to a variation on the reference voltage equal to 21 %.

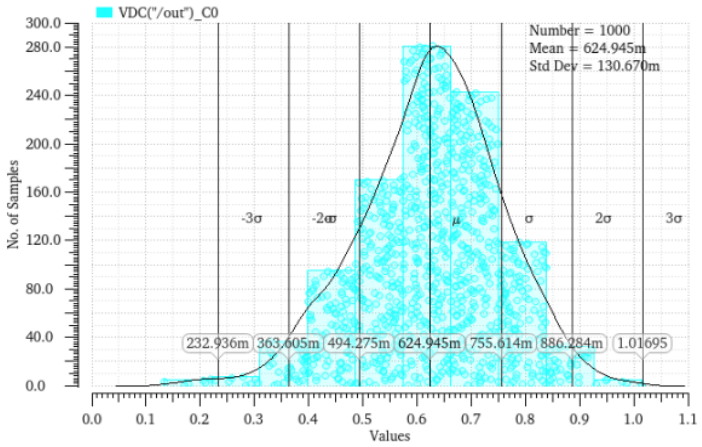


Fig. 108. Monte Carlo simulation result of the reference voltage.

2.7.7 Comparison With the State of Art

The performances achieved by the discussed reference voltage with proposed trimming strategy can be compared to other similar solutions taken from the literature [18], [19], [23], [25], [29], [31], [44]. The results are shown in Table LXII in which the main performance parameters of a voltage reference TC and LC together with achieved current (power) consumption, supply and temperature range and area occupation has been evaluated. Thanks to the adoption of a 28-nm CMOS technology, the proposed voltage reference results in the smallest area occupation which was one of the great benefits. Temperature coefficient and line sensitivity are the smallest one even if they are defined in the tightest range of supply voltage and temperature. Despite this, TC and LS results comparable with the other ones achieved by other solution taken from the state of art.

At the end, the small power consumption insensitive to the supply voltage variations together with the small area occupation make the proposed voltage reference suitable for the proposed biomedical and implantable device. Additionally, the main novelty of the proposed topology besides in the

proposed trimming strategy in the active load which allows to reduce by a factor of 10 the reference voltage variation across corners than ones achieved without trimming strategy.

TABLE LXI: Performance comparison with the state of art.

Reference	29	23	18	19	31	25	44	This work*
Year	2006	2007	2011	2013	2019	2021	2021	2021
Technology (nm)	350	350	180	180	180	180	180	28
Minimum VDD (V)	1.5	0.9	0.45	0.6	1	0.25	0.9	0.8
VDD (V)	1.5 to 4.3	0.9 to 4	0.45 to 2	0.6 to 1.8	1 to 1.8	0.25 to 1.8	0.9 to 1.8	0.8 to 2
Current consumption (nA)	80@1.5V 110@4.3V	40@0.9V 55@4V	7@0.45V 8@1.8V	37@0.6V 37@1.8V	0.192@1V	0.02@0.25V 0.02@1.8V	2@0.9 2@1.8	18.6@0.8V 20.1@2V
Power (nW)	120@1.5V 473@4.3V	36@0.6V 220@4V	3.15@0.45V 14.4@1.8V	22.2@0.6V 22.2@1.8V	0.192@1V	0.005@0.25V 0.042@1.8V	1.8@0.9 3.6@1.8	14.8@0.8V 40.2@2V
Minimum Power (nW)	120	36	3.15	22.2	0.192	0.005	1.8	14.8
Vref (mV)	891.1	670	263.5	259	693	91.4	261	628
Temperature range (°C)	[0÷80]	[0÷80]	[0÷125]	[0÷125]	[−20÷100]	[0÷120]	[−40÷130]	[20÷60]
TC (ppm/°C)	12	10	142	462	33	265	7	5
Line sensitivity (%/V)	0.46	0.27	0.44	0.065	0.02	0.16	0.013	0.009
Die Area (mm2)	0.015	0.045	0.043	0.0298	0.0045	0.0022	0.0059	0.000156

2.7.8 Experimental Results

The chip photo and the corresponding voltage reference layout are shown in Fig. 110. The occupied chip area is equal to 6 mm^2 while the area occupation of the voltage reference is only 0.000156 mm^2. A set of ten different die of the same run were implemented by using a standard 28-nm CMOS bulk technology provided by TSMC. Measurement at chip level have been performed to evaluate the performances of the reference voltage under different supply voltage and temperature conditions. The overall measurement has been carried out by using a power supply generator to precisely set the supply voltage of both the voltage reference and its related PCB while a multimeter has been used to measure the reference voltage. Additionally, the temperature behavior of the reference voltage has been measured by using a temperature chamber consisting of a Thermostream tool which is able to precisely set the temperature during the measurement.

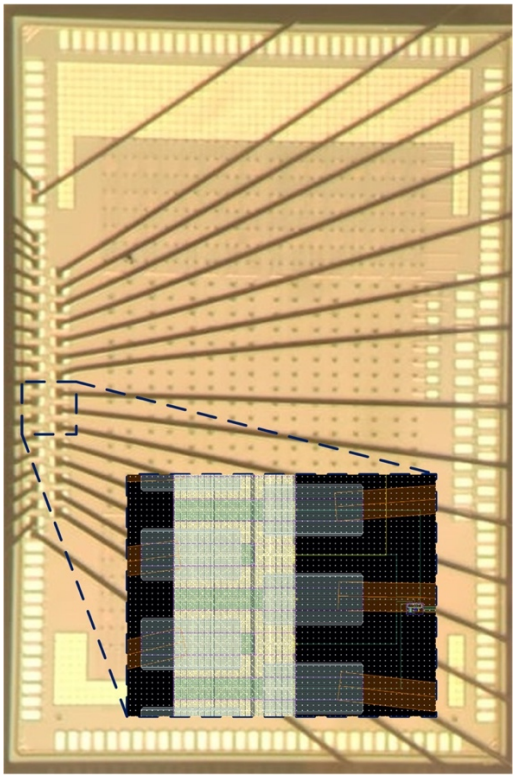


Fig. 109. Chip photo.

First, the trimming strategy has been tested by enabling the three different active load branches by using their three related switches named V_1, V_2 and V_3. All the seven different combinations of the switches have been tested by evaluating if the reference voltage remain stable around the mean value. The obtained results shows that all the combinations of switch provide the same value of the reference voltage except the case where the switch V_2 is not enable. In that case, the reference voltage is higher than the other measured one thus indicating that the corner of the die is the slow for the NMOS transistor (SS or SF). Therefore, trimming strategy on the measured voltage properly works allowing to set the reference voltage around the mean value by compensating the unfavorable corner which can be done in this case by enabling always the second branch of the active load.

The reference voltage has been measured in the supply range from 0.8 to 2 V in steps of 100 mV at room temperature and the measured values are summarized in Table LXIII. The average nominal value of the reference voltage is 863.8 mV while the simulated value of the average reference voltage was 628 mV. This means that the measured reference voltage is higher than 200 mV of the simulated one, this possibly related to the variation on the current generated by the current reference circuit. Indeed, a higher reference current than the expected one implies a higher reference voltage. The simulated current value of the overall circuit was only 20 nA which means that the current generated by the reference circuit section is around 7 nA. Very small current like the simulated one are difficult to manage and implies accurate model of the transistor to prevent second-order effect due to the low-current operation. Beside this, all the devices in the reference voltage except M_2 are ultra-low voltage threshold transistor whit a threshold voltage around 350 mV. This kind of transistors is not well-modelled and consequently their use is often avoided or restricted to low-voltage and low-current design like this. Therefore, the adoption of ultra-low voltage-threshold transistor not well-modelled to generate a current low than 10 nA implies some secondary-order effect which leads a variation on the reference current thus impacting the generated reference voltage. However, the measured reference voltage around 800 mV still remains an appropriate value which allow to the overall biomedical system to work properly.

TABLE LXII: Measured reference voltage at different value of supply voltage in the range [0.8÷2] V.

	VDD = 0.8 V	VDD = 0.9 V	VDD = 1 V	VDD = 1.1 V	VDD = 1.2 V	VDD = 1.3 V	VDD = 1.4 V	VDD = 1.5 V	VDD = 1.6 V	VDD = 1.7 V	VDD = 1.8 V	VDD = 1.9 V	VDD = 2 V
VREF (DIE 1) (mV)	782	848	877	880	882	883	884	885	886	885	885	886	886
VREF (DIE 2) (mV)	779	839	851	852	853	853	853	853	854	854	854	855	855
VREF (DIE 3) (mV)	775	833	844	845	847	848	848	848	849	849	850	850	850
VREF (DIE 4) (mV)	782	853	873	877	878	878	879	880	880	880	881	881	881
VREF (DIE 5) (mV)	778	837	850	851	852	852	853	853	854	854	854	854	854
VREF (DIE 6) (mV)	780	847	865	867	868	868	869	870	870	870	870	871	871
VREF (DIE 7) (mV)	783	855	878	880	881	881	882	883	883	883	884	884	884
VREF (DIE 8) (mV)	777	840	856	857	858	858	859	859	860	860	861	861	861
VREF (DIE 9) (mV)	778	842	858	861	861	862	862	863	863	864	864	864	864
VREF (DIE 10) (mV)	778	837	845	847	847	849	849	849	850	850	851	851	851

By inspection of Table LXIII, it can be noted that the steady state on the reference voltage occurs when the supply voltage is equal to 1 V which is higher than 200 mV than the minimum simulated one of 0.8 V. This is further confirmed by Fig. 111 where the measured output voltage as a function of the supply voltage is shown.

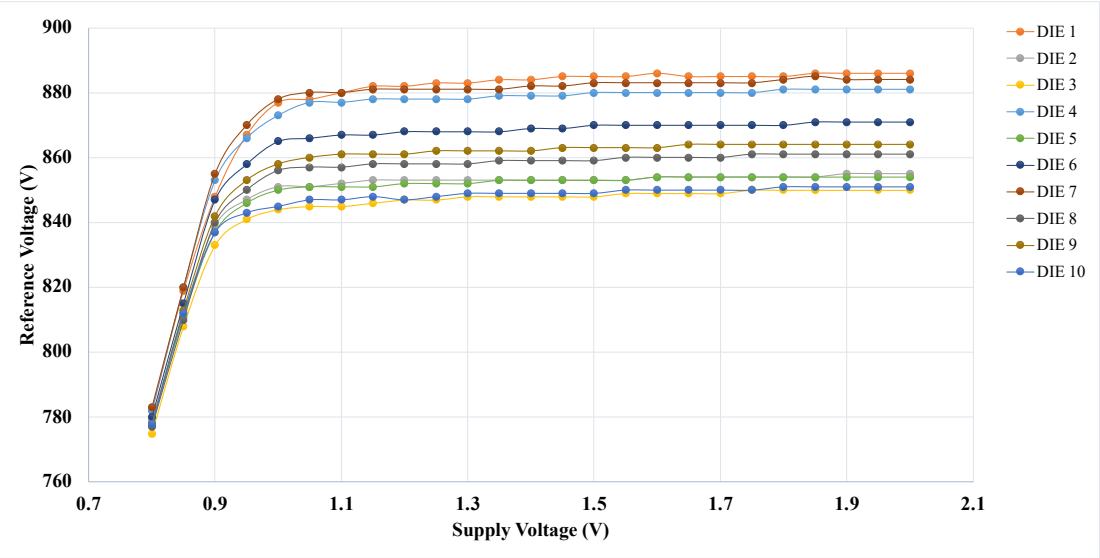


Fig. 110. Measured output voltage as a function of the supply voltage in the range [0.8÷2] V.

Therefore, an accurate analysis of the line sensitivity of the measured reference voltage can be carried out by restricting the supply voltage range from 1 to 2 V as shown in Fig. 112. The measured reference voltage variation ΔV_{REF} as a function of the supply voltage in the range [1 ÷2] V for different DIE is summarized in Table LXIV. The average value of the reference voltage variation is 6 mV thus leading a measured line sensitivity of 0.0069 %/V. Additionally, the spread of the measured reference voltage by changing the DIE is around 40 mV which is less than the simulated spread obtained through the Monte Carlo simulation.

TABLE LXIII: Measured reference voltage variations ΔVREF in the supply voltage range [1÷2] V.

ΔVREF	Value (mV)
ΔVREF (DIE 1) (mV)	9
ΔVREF (DIE 2) (mV)	4
ΔVREF (DIE 3) (mV)	6
ΔVREF (DIE 4) (mV)	8
ΔVREF (DIE 5) (mV)	4
ΔVREF (DIE 6) (mV)	6
ΔVREF (DIE 7) (mV)	6
ΔVREF (DIE 8) (mV)	5
ΔVREF (DIE 9) (mV)	6
ΔVREF (DIE 10) (mV)	6

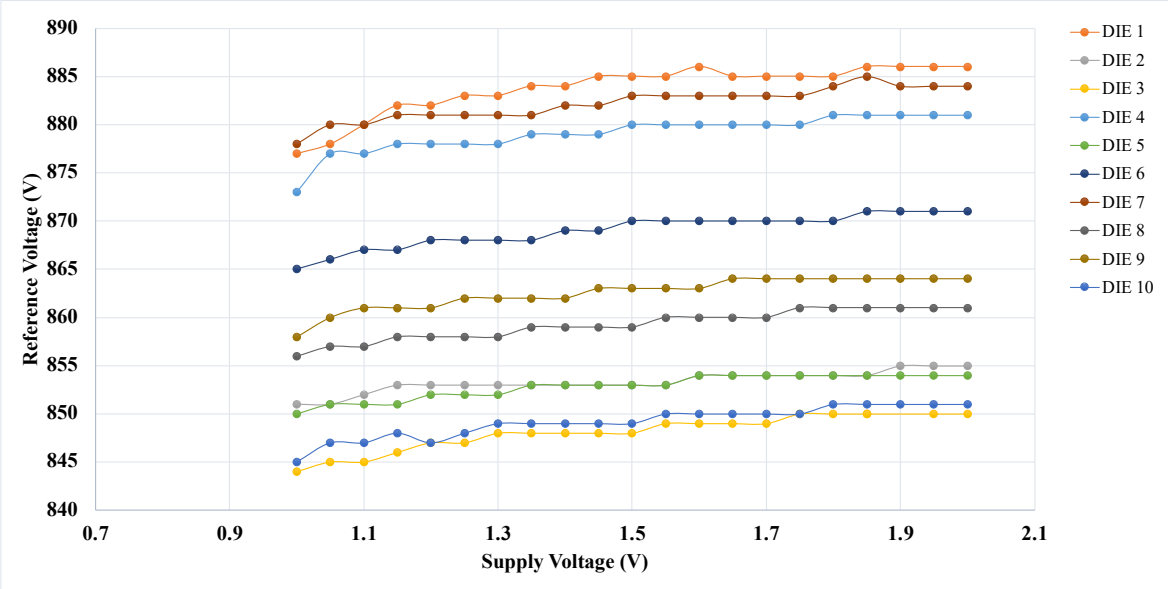


Fig. 111. Measured output voltage as a function of the supply voltage in the range [1÷2] V.

The reference voltage has been measured in the temperature range [20÷ 60] °C in steps of 5 °C and by setting the supply voltage equal to 1.4 V. The measured values are summarized in Table LXV and the average value of the measured reference voltage is 862 mV (at room temperature).

TABLE LXIV. Measured reference voltage at different value of temperature in the range [20÷60] °C.

	T = 20 °C	T = 25 °C	T = 30 °C	T = 35 °C	T = 40 °C	T = 45 °C	T = 50 °C	T =55 °C	T = 60 °C
VREF (DIE 1) (mV)	883.3	884.7	885.5	885.6	886.6	887.8	889.4	890.1	891.5
VREF (DIE 2) (mV)	846.4	850	852.2	853.8	856.7	857.3	858.7	860.4	863.1
VREF (DIE 3) (mV)	845.5	846.5	848.8	850.4	852.4	854	855.5	857.3	859.2
VREF (DIE 4) (mV)	875.2	876.3	878.7	880	881.8	884.4	886.4	877.8	889.8
VREF (DIE 5) (mV)	848.8	850.3	852.2	853.8	855.2	856.7	858.9	860.4	861.7
VREF (DIE 6) (mV)	867	869	870.2	871.5	872.9	874.7	875.4	877.7	879.8
VREF (DIE 7) (mV)	879.7	880.5	880.9	883.4	884.9	886.1	887.6	889.2	890.9
VREF (DIE 8) (mV)	856.1	858.2	861.2	862.1	865.1	867.8	869.8	871.6	874.5
VREF (DIE 9) (mV)	860.6	862.4	863.3	864.6	865.4	867.3	888.8	871.1	872.3
VREF (DIE 10) (mV)	838.4	841.7	844.7	847.5	848.5	851.8	853.8	855.7	856.6

The measured output voltage variations as a function of the temperature are shown in Fig. 113 while the voltage variation value ΔV_{REF} in the considered temperature range achieved for the different die are summarized in Table LXVI. The average value of the reference voltage variation is 13.84 mV thus leading a measured temperature coefficient equal to 401.39 ppm/°C. By inspection of the Fig, 113, it is apparent that the behavior of the reference voltage is only PTAT while the simulated one was the results of the combination between PTAT and CTAT behaviors which result in the temperature compensation of the reference voltage. The measured results suggest that the part of the circuit which generate the CTAT reference voltage is not correctly working thus impacting the temperature behavior of the reference voltage. However, the use of the reference voltage is restricted to a biomedical application in which the temperature is almost constant around 36 °C. Therefore, although the measured temperature behavior is not particularly advantageous, this proposed voltage reference still be used in the biomedical application for which it was designed.

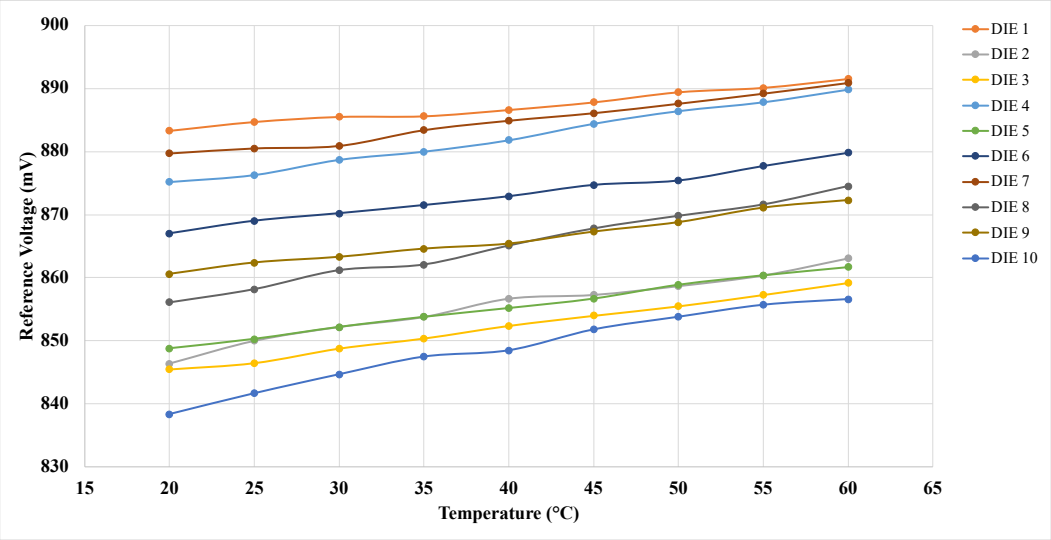


Fig. 112. Measured output voltage as a function of the temperature in the range [20÷60] °C.

TABLE LXV. Measured reference voltage variations ΔVREF in the temperature range [20÷60] °C.

ΔVREF	Value (mV)
ΔVREF (DIE 1) (mV)	8.2
ΔVREF (DIE 2) (mV)	16.7
ΔVREF (DIE 3) (mV)	13.7
ΔVREF (DIE 4) (mV)	14.6
ΔVREF (DIE 5) (mV)	12.9
ΔVREF (DIE 6) (mV)	12.8
ΔVREF (DIE 7) (mV)	11.2
ΔVREF (DIE 8) (mV)	18.4
ΔVREF (DIE 9) (mV)	11.7
ΔVREF (DIE 10) (mV)	18.2

Chapter 3

Ultra-low Power CMOS Operational Transconductance Amplifiers

3.1 Introduction to Operational Transconductance Amplifiers

The Operational Transconductance Amplifier (OTA) is a device that generates an output current which is a function of the difference between the two input voltages V_1 and V_2 typically indicated as differential input voltage. The input voltage controls the output current by means of the device transconductance denoted by g_m. This makes the OTA a voltage-controlled current source which is the main difference with the traditional operational amplifier which is a voltage-controlled voltage source. Additionally, being the OTA a current source it leads to a high output impedance of the device unlike the traditional op-amp which has a low output impedance.

The circuit schematic of a simple transconductance amplifier is shown in Fig. 114 and consists of a differential pair M1-M2 and a current mirror M3-M4, acting as an active load.

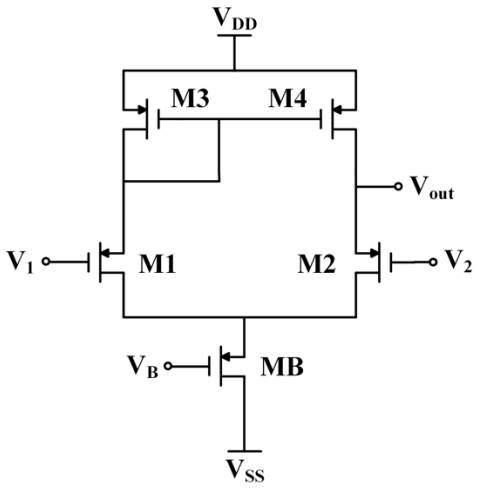


Fig. 113. Circuit schematic of a simple transconductance amplifier.

The main performance parameters of an OTA can be divided into two groups depending on if they are related to the small-signal or to the large-signal of the amplifier. The small-signal performance parameters are open-loop gain, gain-bandwidth product, noise, while the large-signal performance parameters are output swing, linearity, noise, offset, supply rejection and common mode rejection. Besides these, the frequency analysis needs to be carried out especially for multi-stage amplifiers in which a compensation scheme should be added to achieve the stability of the system with an appropriate value of phase margin.

3.2 Low-Voltage and Low-Current Operational Transconductance Amplifiers State of Art

Various OTA design approach has been proposed in literature to overcome the limitations due the low-voltage operation including subthreshold (or weak inversion) region, bulk driving (or body

driving) [45]–[62], body biasing [63]–[65], inverter-based [66]–[75] and fully digital approaches [76]–[83]. Floating-gate and quasi-floating-gate techniques can be also mentioned [92],[93]. These last unfortunately employ non-conventional transistors which are not included in the commercial design kit. Additionally, the temperature dependence of the pseudo-resistor adopted (not adequately modelled in CAD tools) limits the use of this approach making realistic simulation models difficult to construct. Therefore, floating-gate and quasi-floating-gate transistor solutions will not be considered by analyzing the state of art by thus restricting the field to approaches suitable for standard CMOS technologies.

A comparison of the low-power OTA in the state of art will be made below by dividing the proposed solution into categories depending on their working principle which are subthreshold, body driving, body biasing, inverter-based, and digital techniques. The analysis will be carried out highlighting advantages and trade-offs of the mentioned approaches by taking into account the primary performance parameters and evaluating specific figures of merit often used in the literature.

3.2.1 Subthreshold Approach

As already stated, the utilization of transistors operating in weak inversion or subthreshold region has become the primary technique for low-voltage and low-power analog design in CMOS technology. Beside this, saturation region in subthreshold region is reached when $V_{DS} \cong 4\ V_T$ in which an exponential behavior between the drain current and the gate-source voltage is found. Small-signal parameter of gate-driven NMOS transistor operating in subthreshold and saturation region are shown in the second column of Table XLVIII where a bipolar-like behavior is apparent by the linear dependence of the transconductance g_m on the drain current I_D (76a). Subthreshold devices also show the highest transconductance efficiency (gm / I_D) while the intrinsic voltage gain A_V which is given by the reciprocal of λ_D results in a minimization of the distortion.

The main drawback of this approach lies in a larger drain current error between two otherwise ideally matched transistors. This question is particularly exacerbated in the implementation of an OTA thus resuling in increased offset and noise so that overcoming this issue may results in a complex design. Moreover, since subthreshold operation implies very low standy currents, the reduced transconductance leads to a limited bandwidth which is only partially compensated by the lower MOS parasitic capacitances provided by the scaled technologies. . However, this is not a main issue because most of the sensor node applications such as monitoring pressure, temperature, humidity, acceleration or biosignals, usually involve frequencies around the kilohertz. For these reasons, the subthreshold region is widely exploited in the implementation of analog building blocks including OTAs supplied from 1-V under very limited current budgets [47], [86]–[91].

As an example, a CMOS OTA operating in the subthreshold region proposed in [87] is shown in Fig. 115. The solution clearly illustrates that conventional circuit topologies are employed by this approach. In this case we have a folded-cascode differential stage M_1-M_8, followed by common-source stage M_9-M_{10}, and as a final non inverting stage common-source M_{11} transistor with current mirror load M_{12}-M_{13}. The biasing point of the transistors is here the key aspect and, in addition, the use of three gain stages to compensate for the diminished intrinsic stage gain. C_1 and C_2 nested frequency compensation capacitors provide closed-loop stability.

The DC gain and the gain-bandwidth product (GBW) are

$$A = g_{m1,2} g_{m9} g_{m11} r_{o1} r_{02} r_{03} \tag{74}$$

$$GBW = \frac{g_{m1,2}}{C_1} \tag{75}$$

where r_{oi} is the equivalent small-signal resistance at the output of the i-th stage ($r_{o1} \approx r_{d8}$, $r_{o2} = r_{d9} // r_{d10}$, and $r_{o3} = r_{d13} // r_{d14}$).

The solution is supplied with 1 V and allows driving high capacitive loads up to 200 pF with only 170 nA of standby current. The DC gain is 120 dB.

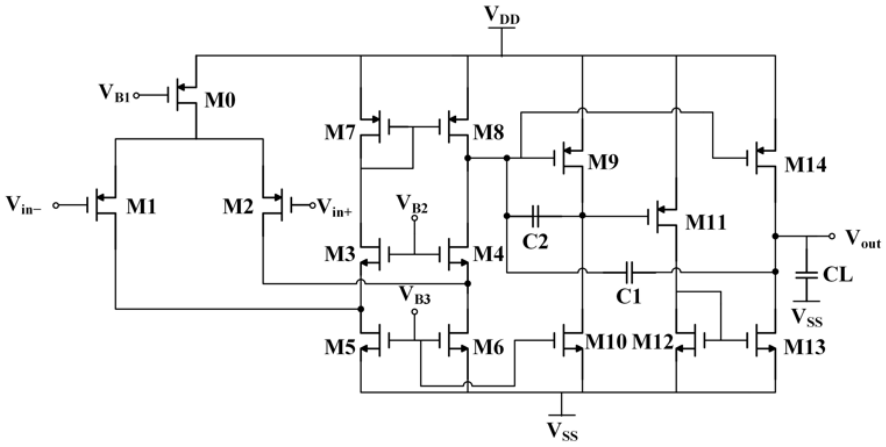


Fig. 114. Schematic of the three-stage CMOS OTA operating in the subthreshold region proposed in [87].

3.2.2 Body-Driven Approach

The conductivity of the channel and consequently the drain current I_D is controlled by the gate-source voltage in traditional gate-driven approach, either above or belove the subthreshold. In contrast, in the bulk-driven or body-driven approach I_D is controlled by the bulk-source voltage V_{BS}. The two different ways to implement p-channel differential pair which differ according to the approach gate-driven or bulk-driven are shown in Fig. 116 (a) and (b), respectively. In the latter case, the differential input signal is applied to the bulk terminals of the transistors couple M2B and M3B while the gate terminals are kept to a reference voltage (V_{SS} in this case) [49]. Removing the limitation given by the threshold voltage associated with the gate terminal, the input common-mode range of the BD pair is maximized since the input voltages can span from V_{SS} to V_{DD}. The main advantage of this approach is, indeed, the ability to achieve rail-to-rail input operation under supply voltages comparable to or even less than the threshold voltage. It is of course mandatory that the bulk-source junction is not turned on and this means that the approach is particularly profitable for supplies (V_{DD}-V_{SS}) below 0.5 V. Otherwise, the bulk source junction start to draw a non-negligible current. Observe that the gates of M_{2B}-M_{3B}, connected to V_{SS} in Fig. 116 (b), can be instead used to set the standby current of M_{2B}-M_{3B} through a conventional current mirror and by eliminating the tail current generator M_{1B}. In this manner supply demand is further reduced at the cost of a lower *PSRR* [92]. The body-driven approach requires the use of a triple-well technology if the body terminal of both *p*- and *n*-channel MOS devices must be exploited. As a drawback, this results in greater area occupation.

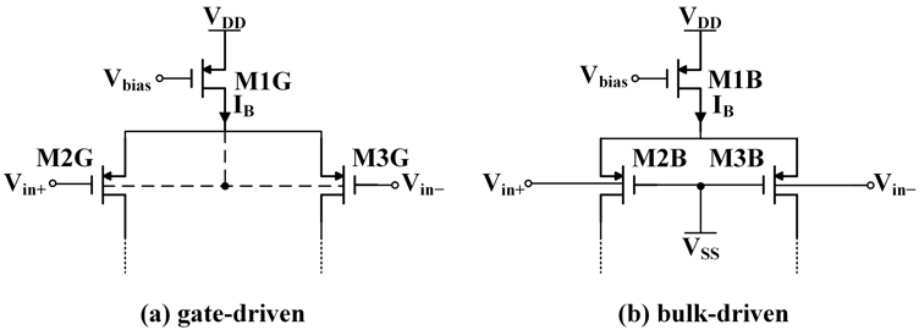


Fig. 115. (a) Minimum-supply differential pair (b) common-mode control circuit proposed in [63].

The third column of Table LXVII shows the small-signal parameters of a body-driven transistor operating in saturation, above the threshold region. Since the bulk transconductance g_{mb} is only about 10% to 20% of g_m as highlighted by (77b), bulk-driven configurations are characterized by reduced values of the intrinsic gain A_v and transition frequency f_T.

TABLE LXVI: Small-signal parameters of an N-channel MOS transistor (saturation region).

	Subthreshold		**Above threshold Bulk-driven**	
$\boldsymbol{g_m = \frac{\partial I_D}{\partial V_{GS}}}$	$\frac{I_D}{nV_T}$	(76a)	$\sqrt{\frac{2KWI_D}{L}}$	(76b)
$\boldsymbol{g_{mb} = \frac{\partial I_D}{\partial V_{BS}}}$	$\lambda_B g_m$	(77a)	$\frac{C_{BC}}{C_{GC}} g_m$	(77b)
$\boldsymbol{g_{ds} = \frac{\partial I_D}{\partial V_{DS}}}$	λI_D	(78a)	λI_D	(78b)
$\boldsymbol{f_T}$	$\frac{g_m}{2\pi(C_{GS}+C_{GD}+C_{GB})}$	(79a)	$\frac{g_{mb}}{2\pi(C_{SB}+C_{DB}+C_{b-sub})}$	(79b)
$\boldsymbol{A_v}$	$\frac{1}{\lambda_D}$	(80a)	$\frac{g_{mb}}{g_m}\sqrt{\frac{2kW}{I_D L}}$	(80b)

where g_{ds} is the drain-source transconductance, $K = \mu_n C_{ox}$ is the transconductance factor, λ_B is the body effect coefficient, C_{GS} is the gate-source capacitance, C_{GD} is the gate-drain capacitance, C_{GB} is the gate-bulk capacitance, C_{SB} is the source-bulk capacitance, C_{DB} is the drain-bulk capacitance, $C_{B\text{-}sub}$ is the bulk-substrate capacitance, C_{BC} is the bulk-channel capacitance and C_{GC} is the gate-channel capacitance.

Several bulk-driven OTAs have been proposed in the literature [45]–[62] where most of these employ transistors in subthreshold to minimize the supply voltage requirements. Moreover, multistage architectures are often utilized to overcome the lower value of the DC gain. Positive feedback is exploited to increase both the input transconductance and the gain-bandwidth product. To give an example of such technique, the schematic of the OTA proposed [61] is shown in Fig. 117. The resulting differential gain and gain-bandwidth product can be expressed as follows:

$$A = \frac{\beta}{1-\alpha} g_{mb1,2} r_o \tag{81}$$

$$GBW = \frac{\beta}{1-\alpha} \frac{g_{mb1,2}}{C_L} \tag{82}$$

At the same purpose, combination of body-driven and AC-coupled gate-driven approaches has been also proposed in [93]. As it already stated, this solution cannot be taken into account in this discussion due to the QFG technique limitation in CMOS process.

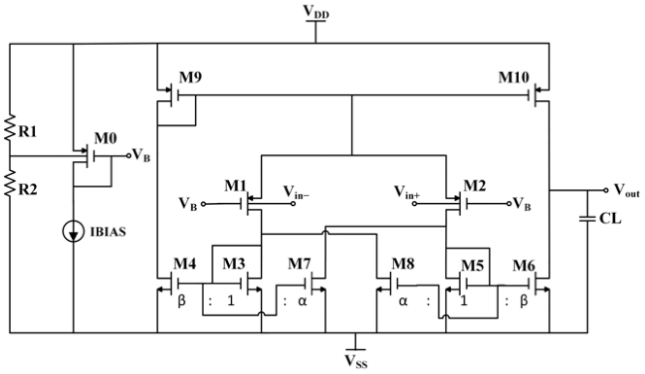


Fig. 116. Schematic of the OTA with positive feedback proposed in [61].

3.2.3 Body-Biased Approach

The body-biased (BB) approach belongs to a class of methods to design CMOS sub 1-V low-power OTAs aimed to overcoming the limitations of the CMOS technology and/or of the conventional OTA topologies through threshold lowering [46], [88], level shifting [48], body-driven gain boosting [51] and non-tailed differential pairs [64], [65], [92]. Additionally, these techniques can be also combined together. The body-biased approach followed in [63], exploits a gate-driven differential pair, thus providing a high gate transconductance, but 1) the tail current source is eliminated giving extra room for input swing and 2) the body terminals of the pair are used both to control the common-mode (and hence also DC) current and to reduce the threshold voltage through the body effect. Fig. 118 (a) and 118 (b), shows respectively the minimum-supply gate-driven differential pair and the simplified schematic of the common-mode control circuit. The common-mode control voltage V_b is generated in circuit of Fig. 118 (b) forcing $I_B/2$ to flow in M_{1R} (M_{2R}) when $V_{in+}=V_{in-}=V_{icm}$. Then, V_b is applied to the main circuit of Fig. 118 (a). It is apparent that the quiescent (and common mode) current in M_1-M_2 is mirrored from that of M_{1R}-M_{2R} and hence M_1-M_2 act as a differential pair but without the tail current source. Moreover, under suitable values of $W/L)_{1R\text{-}2R}$ and I_B, voltage V_b is less than V_{DD} and the threshold voltage of M_{1R}-M_{2R} is diminished.

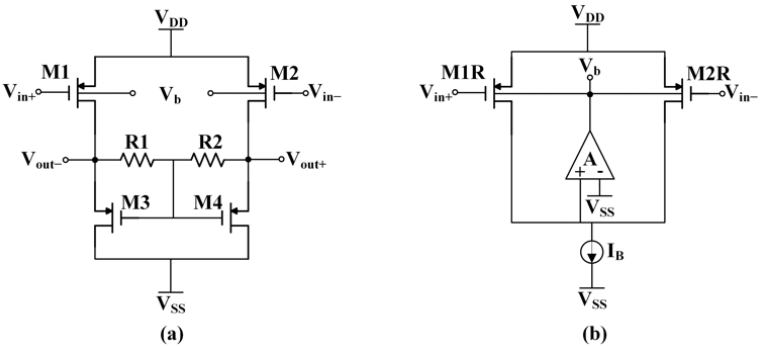


Fig. 117. (a) Minimum-supply differential pair (b) common-mode control circuit proposed in [63].

Based on this approach, an optimized solution that provides relatively low noise around 65 nV/$\sqrt{H_z}$ and total current consumption of 27 μA, with a good trade-off between DC gain (65 dB) and gain-bandwidth product (1 MHz) has been experimentally validated in [65].

3.2.4 Inverter-Based Approach

The previous OTAs approaches require manual design form the schematic level to the layout and routing level. Moreover, especially bulk-driven approach, result in considerable area occupation, because separate wells are required. On the contrary, digital designs, and specifically inverter-based designs would take full advantage from automatic design and from the CMOS technology evolution

in terms of speed and transconductance to overcome some of the current problems in the implementation of analog amplifiers in scaled technologies. The inverter-based (INV) method exploits CMOS inverters as transconductance stage elements in an attempt to take advantage of the digital world. An early implementation of this approach is the so-called Nauta transconductor and further derivations [66]–[74]. By considering the inverter in Fig. 110 and neglecting for the moment resistor R_F, it can be seen that the inverter works as an amplifier if it is biased in its switching threshold. Under this biasing condition, the small-signal transconductance of the inverter is equal to the sum of the transconductances of both the nMOS and pMOS transistor, *i.e.* $g_m=g_{m1}+g_{m2}$. In addition, the absence of the active load reduces the input equivalent noise if compared to a standard differential pair. The bias point can be obtained through self-biasing using the resistive feedback provided by R_F, as shown in Fig. 119, or with more complex higher-efficient topologies [40], even exploiting the body terminal [69].

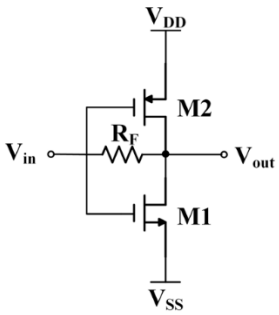


Fig. 118. The CMOS inverter used an analog amplifier self-biased at the switching threshold.

The circuit in Fig. 119 can be used as a transimpedance amplifier due to its a relatively low input resistance. To obtain a transimpedance amplifier, we can return to a conventional single stage OTA, as exemplified in Fig. 111 (a). The key concept is here to replace each transistor in the signal path (M_1-M_4) with an inverter. The gate and the drain of the original transistors correspond to the input and output of the associated inverter. The source terminal is not important, as it is a fixed potential. This is true for active load transistors M_3 and M_4, but also for the pair M_1 and M_2 since, as well known, the common source is grounded if the input signal is purely differential. As result, the circuit in Fig. 120 (b) is derived thus obtaining the basic inverter-based single-stage OTA that unfortunately suffers from low gain, poor *CMRR* and absence of DC current control [94].

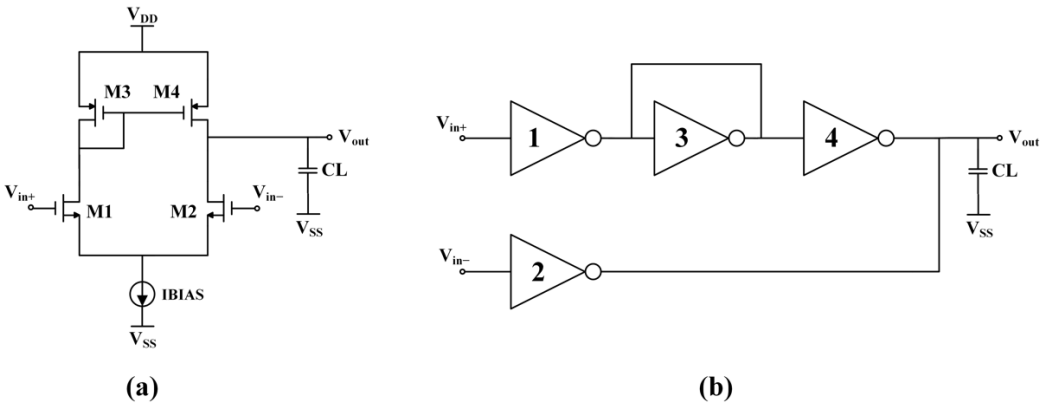


Fig. 119. Conventional single stage OTA (a) and inverter-based single stage OTA.

From this basic circuit, several pseudo-differential inverter-based amplifiers have been proposed. In general, modern inverter-based OTAs try to exploit the digital standard-cell design approach to extend the digital design flow to the analog domain, keep low the design effort and provide portability across technologies. The solution in [75] is a four-stage OTA which uses the bulk terminals of both the p-channel and n-channel MOS transistors of the standard-cell inverter as current and voltage control inputs. This approach is similar to that used in digital applications to

handle process variations. All the standard-cell inverters used for analog functions are connected to an analog building block generator which provides the bulk voltages and which in turn enables each cell's static output voltage to be adjusted to half the supply voltage and to set the quiescent current to a multiple of a reference current. The schematic of the OTA proposed in [75] is shown in Fig. 121 where inverters 1-5 are single inverter (x1) while inverter 6 is made up by two parallel inverters (x2) and inverter 7 is made up by 4 parallel inverters (x4). This solution operates at 0.5 V supply and allows achieving a DC gain of around 70 dB, a gain-bandwidth product around 7 MHz and a slew rate of 1.51 V/μs, while the power consumption is only 0.88 μW.

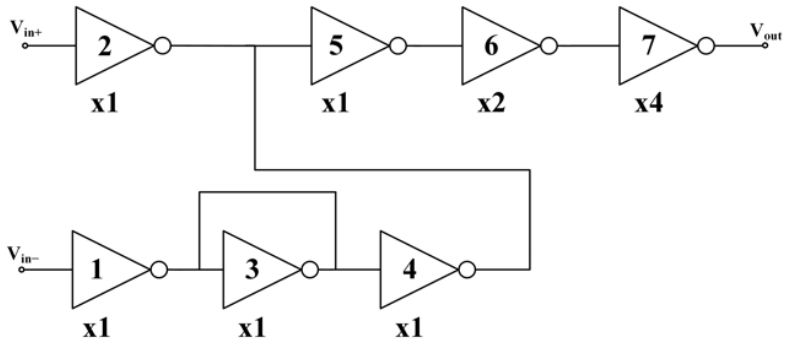


Fig. 120. Schematic of the inverter-based OTA proposed in [75].

3.2.5 Digital Approach

Analog processing requires a well-defined biasing point for the active devices which in turn requires a well-defined quiescent current, setting the lower limit for the DC power consumption. With the digital-based approach, it is possible to eliminate any quiescent bias current and to ensure low-power consumption, low area occupation and low-complexity. Several fully-digital OTAs (DIGOTA) with sub-1 V supply and nanowatt power consumption have been presented in the literature [75]–[83]. These solutions do not require a DC current as they are essentially digital standard cell-based OTAs and share with the inverter-based approach the advantages of both simple design and portability over technologies. In this context, a passive-less fully-digital operational transconductance amplifier (DIGOTA) that employs time-domain processing, zero bias current and passive-less self-oscillation common-mode compensation has been proposed in [77], [78] and finally improved in [83]. The principle of operation of the DIGOTA relies on the observation that a simple pair of digital inverters, as shown in Fig. 122 (a), under a differential condition ($V_{IN+}-V_{IN-}>0$) ($V_{IN+}-V_{IN-}<0$) at the input generates a high (low) output differential voltage, provided that the input common-mode voltage, V_{CM}, is close to the inverter trip point, V_{trip}. If V_{CM} is away from V_{trip}, the digital outputs of the inverters are equal and cannot discriminate whether ($V_{IN+}-V_{IN-}>0$) or ($V_{IN+}-V_{IN-}<0$). However, the information related to the signal $V_{CM}< V_{trip}$ or $V_{CM}< V_{trip}$ still provides a useful information that can be exploited to correct the common-mode input signal and enforce the desired condition $V_{CM}= V_{trip}$ through the negative-feedback compensation. The schematic of the DIGOTA recently introduced in [83] is shown in Fig. 122 (b). The common-mode compensation is achieved by the introduction of an input stage based on the Muller C-element driven by the two input voltages V_{IN+} and V_{IN-} and by the digital common-mode compensation signal V_{PD}. The differential-to-single ended (D2S) output stage is implemented in this work by inverters only. In particular, inverters INV1B and INV2B constitute an inverting voltage buffer while inverters INV1A and INV3B act as a transconductance amplifier driving the same output node. As a result, the DIGOTA can be considered as the cascade of three gain stages, namely the Muller C-element, the inverter, and the output stage. Interestingly, in [83] it has been demonstrated that the equivalent small-signal model can be reduced to that of a conventional three-stage OTA, as shown in Fig. 122 (c). Assuming that V_{PD} is almost constant, the small signal parameters in Fig. 1 (c) can be expressed as:

$$G_{m1} = g_{m,N1} + g_{m,P1} \quad (83)$$

$$G_{m2} = g_{m,N3} + g_{m,P3} \quad (84)$$

$$G_{m3} = 2\left(g_{m,INV1A} + g_{m,INV3B}\right) \quad (85)$$

$$C_{01} = C_{par1} + C_M \quad (86)$$

$$C_{02} = C_{par2} + C_{MUL} \quad (87)$$

$$C_{03} = C_{par3} + C_L \quad (88)$$

$$R_{01} = R_{01,N} \,||\, R_{01,P} \quad (89)$$

$$R_{02} = r_{d,N3} \,||\, r_{d,P3} \quad (90)$$

where $C_{par\,i}$ is the parasitic capacitance at the output of the i-th stage while $R_{O1,N}$ and $R_{O1,P}$ are the resistances of a cascode gain stage.

Under a 0.3-V supply and a load of 250 pF, the power consumption of the OTA is 44 nW while the occupied area is 625 µm^2.

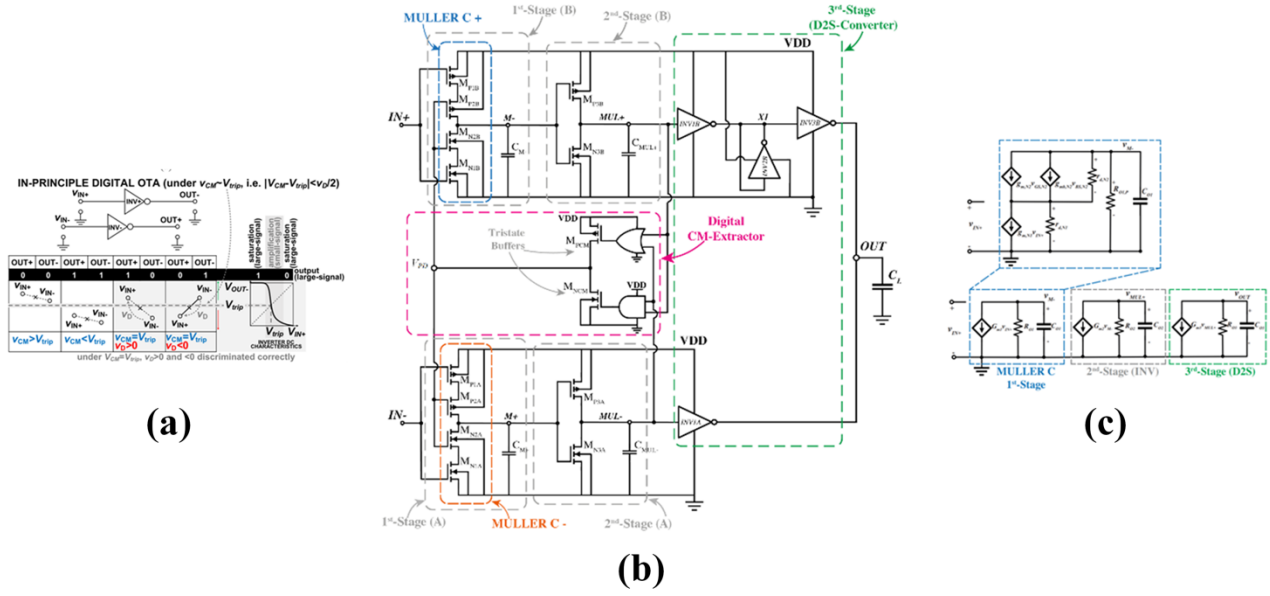


Fig. 121. (a) principle of operation of the DIGOTA introduced in [78]; (b) schematic of the DIGOTA proposed in [83]; (c) small-signal model.

3.2.6 Comparison of Ultra-Low Power OTAs

After having examined the main approaches towards low voltage and low power designs, with a view to making a more detailed comparison among them, we will consider only the ultra-low power OTAs with a supply equal to or less than 0.7 V which are summarized in Table LXVIII. The main OTA parameters such as DC gain, gain-bandwidth product (ω_{GBW}), Phase Margin (PM), Slew-Rate (SR), white noise, Common Mode Rejection ratio (CMRR) and Power Supply Rejection ratio (PSRR), together with well-known Figures of Merit $IFOM_S$ and $IFOM_L$ (91)-(92) are evaluated.

$$IFOM_s = \frac{\omega_{GB}}{I_T} C_L \quad (91)$$

$$IFOM_L = \frac{SR}{I_T} C_L \quad (92)$$

For a specified capacitance load, (91) and (92) show a trade-off between small-signal and large-signal parameters and total bias current (and consequently total power consumption). If we also consider the area occupation, we can define the following two additional Figures of Merit ($IFOM_{AS}$ and $IFOM_{AL}$) (93) and (94).

$$IFOM_{AS} = \frac{\omega_{GB}}{Area \cdot I_T} C_L \quad (93)$$

$$IFOM_{AL} = \frac{SR}{Area \cdot I_T} C_L \quad (94)$$

By inspection of Table LXVIII, the lowest value of the power consumption, that is around 1 nW, was achieved by [71] and [69] , which used a digital and an inverter-based approach, respectively. The highest value of the DC gain is 98 dB and was achieved by [60], which combines body-driven and subthreshold approach, while the highest ω_{GBW} of 38 MHz was achieved by [74] (with minimum C_L of 3 pF) that exploited the combination of the subthreshold and bulk-driven approaches. The highest $IFOM_S$ was achieved by the digital-based OTA proposed in [79] while the highest $IFOM_L$ was achieved by the body-driven OTA proposed in [61]. It is also apparent that the inverter-based approach results in the lowest area occupation.

TABLE LXVII: COMPARISON OF ULTRA-LOW-POWER OTAS.

	[48]	[49]	[50]	[58]	[62]	[63]	[64]	[66]	[68]	[67]	[69]	[70]	[73]	[85]	[87]	[86]	[89]*	[65]*	[81]*	[79]*	[83]	[82]*
Year	2005	2014	2016	2007	2014	2015	2016	2018	2020	2020	2021	2023	2017	2020	2021	2021	2021	2016	2020	2020	2022	2022
Technology (um)	0.18	0.18	0.18	0.35	0.13	0.065	0.18	0.18	0.18	0.065	0.18	0.065	0.35	0.18	0.18	0.18	0.13	0.18	0.18	0.18	0.065	0.13
Area (mm2)E+02	1.7	5.7	3.6	6	8.3	0.5	2	0.9	0.9	0.2	0.09	0.12	1.4	0.098	0.15	0.09	0.009	--	0.08	0.073	0.02	0.022
Supply (V)	0.5	0.5	0.5	0.6	0.25	0.5	0.7	0.3	0.3	0.25	0.4	0.3	0.7	0.3	0.3	0.5	0.55	0.5	0.5	0.3	0.5	0.3
CL (pF)	20	30	40	15	15	3	20	20	30	15	150	50	10	150	80	150	250	20	10	10	0.5	2
DC gain (dB)	62	70	77	69	60	46	57	63	98.1	70	37	38	65	30	30	73	87	91	25.2	51	64	34.97
Ibias (uA)	150	0.15	0.14	0.9	0.072	366	36	0.056	0.043	0.104	0.081	8.5	27	0.008	0.002	0.215	14.9	26	0.558	0.0017	1.75	20.3
Power (uW)	75	0.075	0.07	0.54	0.018	183	25.2	0.0168	0.013	0.026	0.0324	2.55	18.9	0.0024	0.0005	0.1075	8.2	13	0.279	0.0005	0.875	6.1
GBW (KHz)	0.01	18	4	11	2	38000	3000	2.8	3.1	9.5	5.6	1650	1000	0.3	3.7	57.5	3150	394	132	0.74	6850	12690
PM (°)	60	55	56	65	53	57	60	61	54	88	79	70.3	60		54.35	--	65	59	87	90	62.1	62.56
SR (V/us)	2	0.003	0.002	0.015	0.0007	43	2.8	0.0071	0.0091	0.002	0.007395	0.18	0.25	0.000085	0.000181	0.019	0.0027	--	--	--	1.505	5.68
VDD/VTHa	1.14	--	1.18	1.02	1.16	1.66	1.75	0.6	0.6	0.68	--		1.03	--	--	--	--	1	--	--	--	--
Noise (nV/sqrt(Hz))	280	310	--	290	3300	926	100	1850	1800	--	--	250	65	21000	--	--	175	31.8	--	809	--	--
CMRR (dB)	65	--	55	74.5	--	35	19	72	60	62.5	36	39.8	45	41	--	65	46	--	--	37	--	27
PSRR (dB)	43	--	52	--	--	37	52	62	61	38	30	44.7	50	30	--	50	39	122.3	76.8	41	--	--
Operation mode	SUB	SUB	SUB	SUB, BD	SUB, BD	SUB, BD	BD	SUB, BD	SUB, BD	SUB, BD	SUB, BD	BD	BB	DIG	DIG	DIG	DIG	INV	INV	INV	INV	INV
# stages	2	2	2	2	2	3	3	2	3	3	1	3	2	--	--	--	--	--	--	--	4	--
Simulated (S) /Measured (M)	M	M	M	M	M	M	M	M	M	M	M	M	M	M	M	M	S	S	S	S	M	S
FOMS	0.00	7200.00	2285.71	305.56	1666.67	622.95	2380.95	3333.33	7153.85	5480.77	25925.93	32352.94	529.10	18750.00	592000.00	80232.56	96036.59	606.15	4731.18	14800.00	3914.29	4160.66
FOML	0.53	1.20	1.14	0.42	0.58	0.70	2.22	8.45	21.00	1.15	34.24	3.53	0.13	5.31	28.96	26.51	0.08	--	--	--	0.86	1.86
IFOMS	0.00	3600.00	1142.86	183.33	416.67	311.48	1666.67	1000.00	2146.15	1370.19	10370.37	9705.88	370.37	5625.00	177600.00	40116.28	52820.12	303.08	2365.59	4440.00	1957.14	1248.20
IFOML	0.27	0.60	0.57	0.25	0.15	0.35	1.56	2.54	6.30	0.29	13.69	1.06	0.09	1.59	8.69	13.26	0.05	--	--	--	0.43	0.56
IFOMAS	0.00	631.58	317.46	30.56	50.20	622.95	833.33	1111.11	2384.62	6850.96	115226.34	80882.35	264.55	57397.96	1184000.00	445736.43	5868902.44	--	29569.89	60821.92	97857.14	56736.21
IFOMAL	0.16	0.11	0.16	0.04	0.02	0.70	0.78	2.82	7.00	1.44	152.16	8.82	0.07	16.26	57.92	147.29	5.03	--	--	--	21.50	25.39

Fig. 123 and Fig. 124 show the plot of $IFOM_S$ and $IFOM_L$ (on a logarithmic scale) of the different OTAs as a function of the technology node. From this comparison it is apparent that the best small-signal performance is achieved using the digital approach, while the best large-signal performance is achieved using the subthreshold approach. In both cases, it is also apparent that $IFOM_S$ and $IFOM_L$ have been improved during the years thanks to the technology scaling.

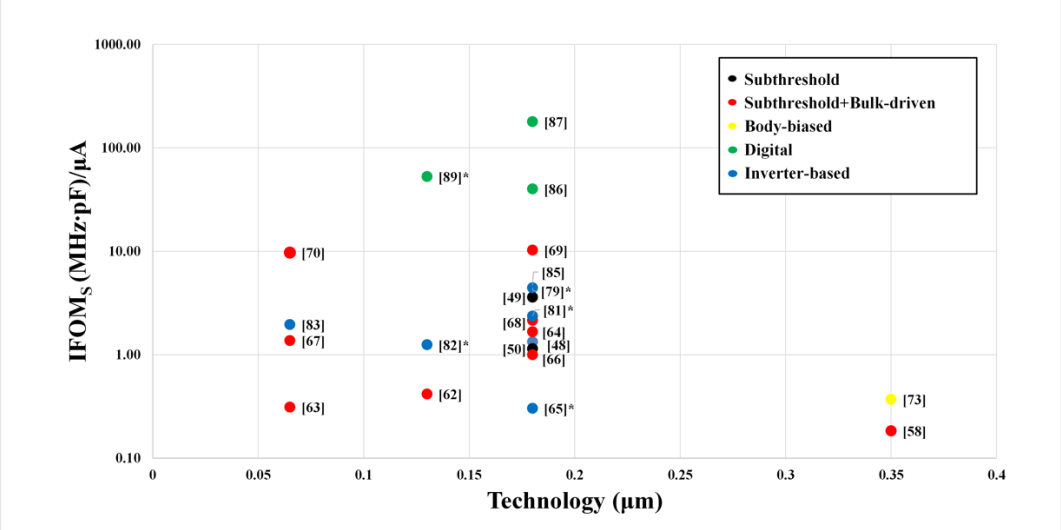


Fig. 122. IFOM$_S$ vs Technology (*simulated).

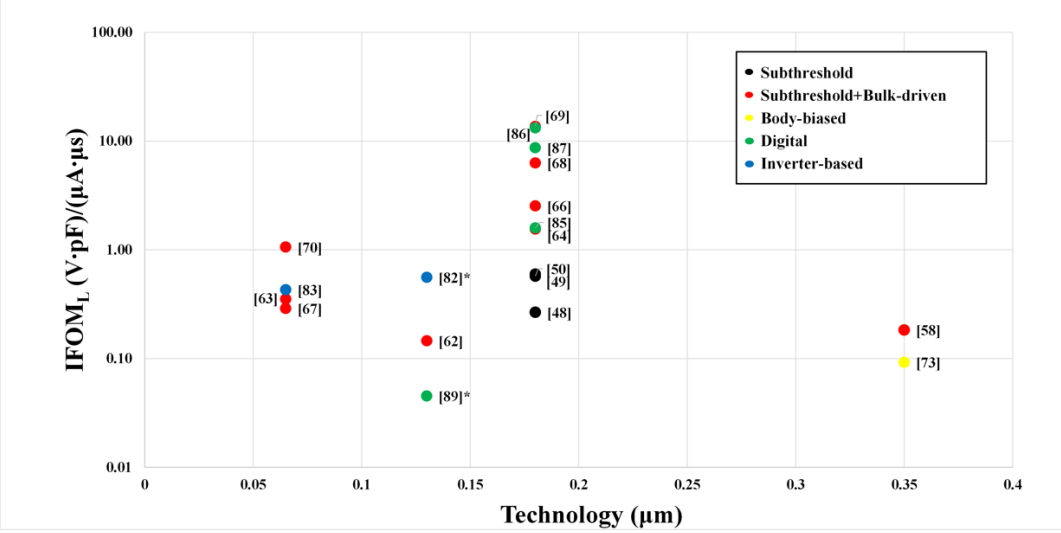


Fig. 123. IFOM$_L$ vs Technology (*simulated).

Fig. 125 and Fig. 126 show also $IFOM_{AS}$ and $IFOM_{AL}$ (on a logarithmic scale) as a function of the technology node. It is apparent that the highest values are achieved with a digital and inverter-based approaches thanks to the fact that these approaches allow to reduce the area occupation. On the other side, it is clear that subthreshold and bulk-driven approaches don't suffer from technology scaling which still maintain good performances in terms of $IFOM_{AS}$ and $IFOM_{AL}$. The results found above are useful as design general rules. However, an accurate comparison must consider other performance not included into the previous figures of merit. For example, OTAs based on a digital approach do not have any control of the bias current and consequently on the power dissipation and on the gain-bandwidth product, resulting in the highest PVT variability. Therefore, in applications where a current control is required, analog approaches are preferred.

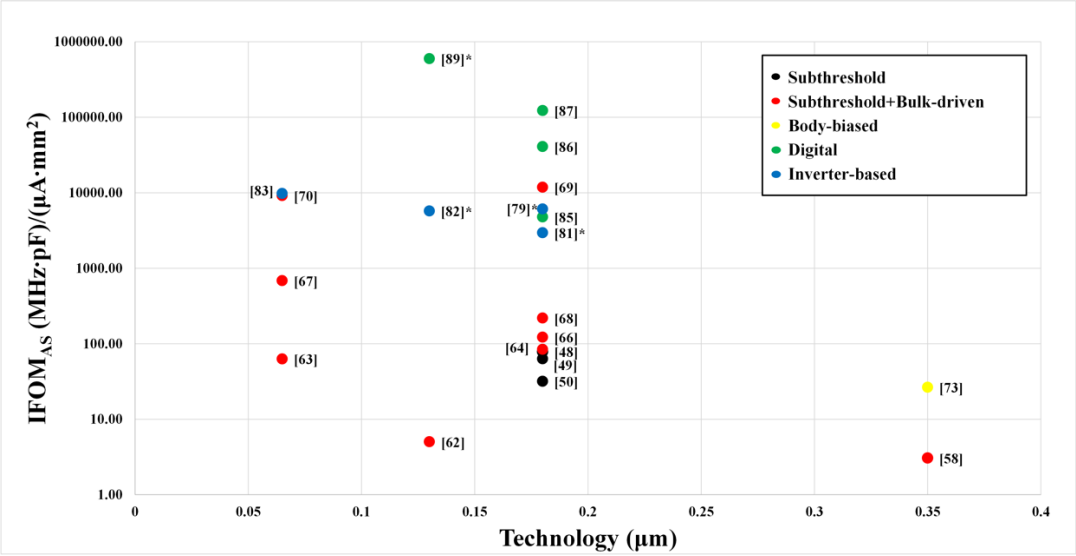


Fig. 124. IFOM$_{AS}$ vs Technology (*simulated).

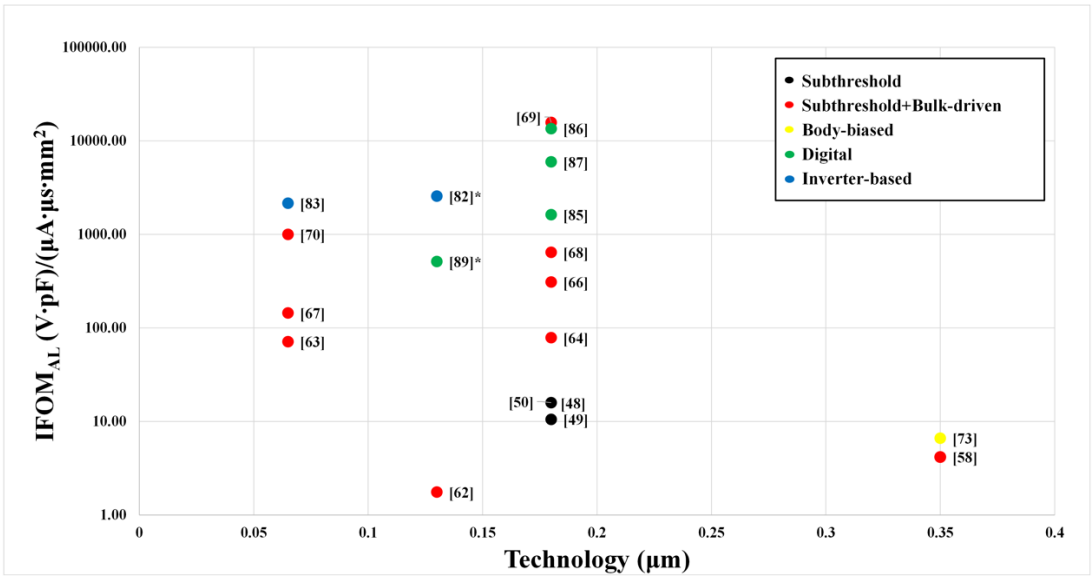


Fig. 125. IFOM$_{AL}$ vs Technology (*simulated).

Another comparison can be carried out taking into account the effect of the supply voltage reduction of the already mentioned Figure Of Merits. At this purpose, Fig. 127 and Fig. 128 show the *IFOM$_S$* and *IFOM$_L$* (on a logarithmic scale) achieved by the OTAs as a function of the supply voltage. Subthreshold and bulk-driven approaches together with digital approach allow to achieve good performances even when the value of the supply voltage is reduced under 0.5 V.

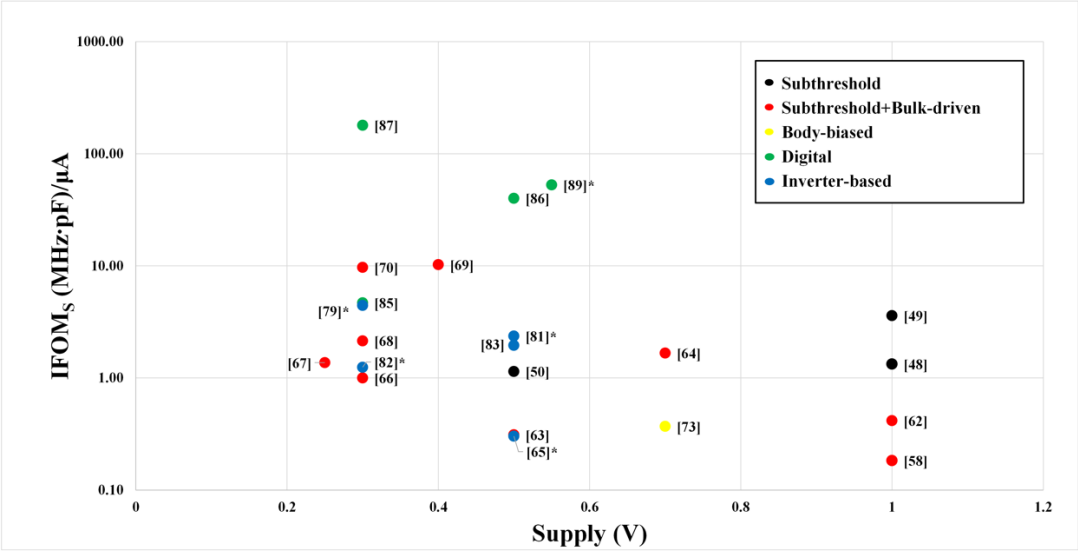


Fig. 126. IFOMs vs Supply voltage (*simulated).

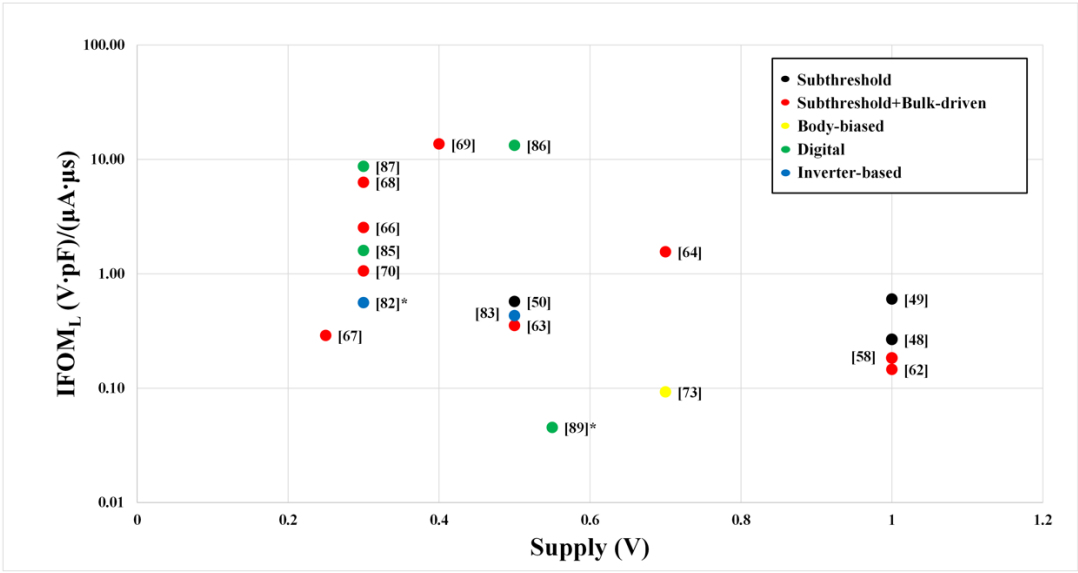


Fig. 127. IFOM$_L$ vs Supply voltage (*simulated).

Taking into account also the area occupation, Fig. 129 and Fig. 130 show the *IFOM$_{AS}$* and *IFOM$_{AL}$* (on a logarithmic scale) achieved by the OTAs as a function of the supply voltage. Once again, these results further confirm what has been described previously proving that the best performances in terms of *IFOM$_{AS}$* and *IFOM$_{AL}$* are achieved with a digital and inverter-based approaches thanks to their lowest area occupation. In comparison to these two approaches, it must be also noted that subthreshold and bulk-driven approaches allow to achieve good results despite the area occupation is greater. At the end this achieved results prove the strength of the subthreshold and bulk-driven approaches to work under 1-V supply.

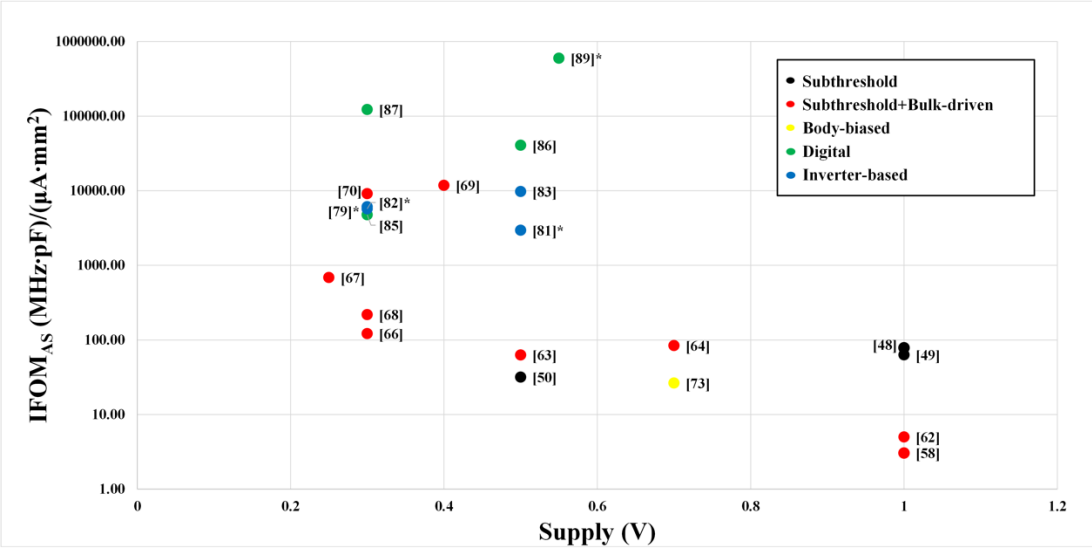


Fig. 128. IFOM$_{AS}$ vs Supply voltage (*simulated).

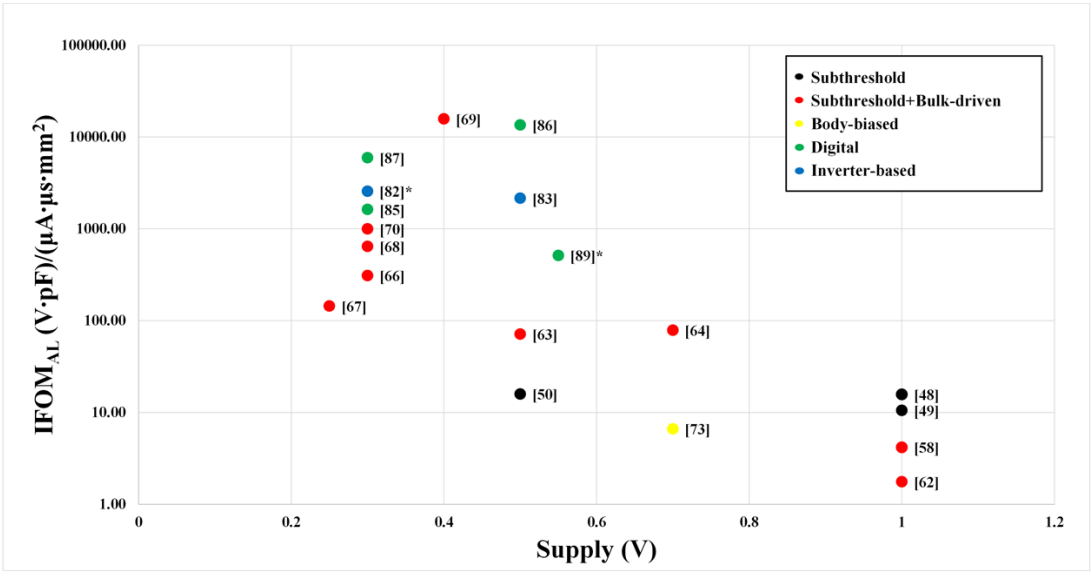


Fig. 129. IFOM$_{AL}$ vs Supply voltage (*simulated).

Once the OTAs state of art has been investigated, two proposed architectures of low-current and low-voltage OTA will be presented below. Based on subthreshold and body driven approaches with additional design techniques, they allow to achieve good performances in terms of both small and large signal parameters together with low-power consumption.

3.3 50pF-400pF 0.4-V Subthreshold Bulk-Driven Rail-to-Rail CMOS Operational Transconductance Amplifier

A high-performance bulk-driven three stage class AB operational transconductance amplifier (OTA) able to work under 0.5-V supply has been designed. The proposed solution employs three stages of gain operating in subthreshold region. An additional positive feedback loop at the input stage obtained through by the bulk cross connection technique has been used to boost the DC gain. Moreover, time response of the OTA has been improved by filling the circuit with a slew-rate enhancer with the aim to raise the slew-rate without changing both small-signal performances and power consumption.

3.3.1 Topology and Operating Point

The simplified schematic of the proposed bulk-driven OTA is shown in Fig. 131 while transistor sizes of the overall circuit and device values are summarized in Table LXIX. The first stage is based on the bulk-driven differential pair M_1-M_2 whose gate voltages are fixed by transistor M_B and current generator I_B, as was proposed by [64]. Transistors M_3-M_4 together with resistors R constitute the load of the differential pair. The body and drain terminals of M_3 and M_4 are cross-connected as proposed in [95] for a gate-driven OTA. In the proposed design, the bulk cross-connection technique allows to increase the differential gain and to decrease the common-mode gain, as will appear clear in the following.

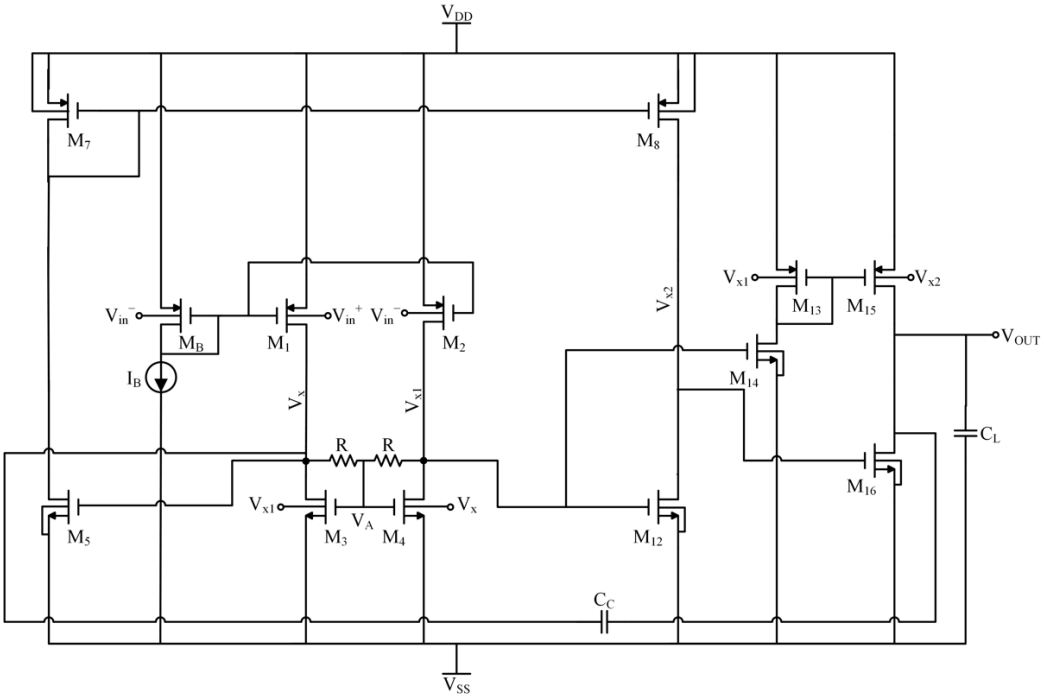


Fig. 130. Simplified schematic of the proposed bulk-driven three-stage OTA.

Transistor M_B, whose body is connected to the virtual ground i.e., $(V_{DD} + V_{SS})/2$, set the quiescent current of the differential pair M_1-M_2 and of its active load M_3-M_4 through the current mirror aspect ratio $(W/L)_{1,2}/(W/L)_B$. Indeed, transistors M_B-M_1 and M_B-M_2 whose body terminal are connected to the analog ground, form two current mirrors which accurately set the DC current into the differential pair. Considering that no DC current flows through the resistor R, the drain terminals of M_3-M_4 are at the same potential of their gate terminals thus acting like a diode-connected transistors. Therefore, transistors M_5-M_{12} have the same gate-source voltage of transistors M_3-M_4 which can be expressed as V_{SG}. Since the complete expression of the threshold voltage of a PMOS transistor can written in the following form: $V_{TH} = V_{THO} - \gamma\left(\sqrt{2\Phi_F + V_{SB}} - \sqrt{2\Phi_F}\right)$ and by neglecting the channel length modulation, the DC current ratio $I_{D5,12}/I_{D3,4}$ by assuming the operation in saturation became:

$$\frac{I_{D5,12}}{I_{D3,4}} = \frac{(W/L)_{5,12}}{(W/L)_{3,4}}\left[1 - \frac{\gamma\left(\sqrt{2\Phi_F+V_{SB}}-\sqrt{2\Phi_F}\right)}{V_{SG}+V_{THO}}\right]^2 \quad (95)$$

where transistors M_3-M_4 have $V_{SB} = V_{SG}$ due to the circuit topology.

Regarding the current flowing into M_{14}, it stands in a current mirror aspect ratio with M_{12} and allow to set the quiescent current flowing in the output stage (M_{16}) through the current mirror M_{13}-M_{14}, as follows:

$$\frac{I_{D16}}{I_{D4}} = \frac{(W/L)_{16}}{(W/L)_4} \tag{96}$$

A final note concerns the class AB behavior of the third stage in which both transistors M_{15} and M_{16} can delivered the maximum current which is not limited by any DC value. Indeed, the current flowing into M_{16} increase when V_{in}^+ increase because also the V_{GS} of M_{14} increase.

TABLE LXVIII: Transistor sizes and device values

Transistor	W / L (μm / μm)	Parameter	Value
M_R	(12.5 / 0.5) × 4	I_B	200 nA
$M_{1\text{-}2}$	(12.5 / 0.5) × 4	R	250 kΩ
$M_{3\text{-}4}$	(15 / 4) × 4	C_C	6 pF
$M_{5\text{-}12}$	(15 / 4) × 16	C_L	300 pF
$M_{6\text{-}11}$	(10 / 4) × 6	V_{DD}–V_{SS}	0.4 V
$M_{7\text{-}8}$	(12.5 / 1) × 16		
$M_{9\text{-}10}$	(12.5 / 0.5) × 8		
M_{13}	(10 / 0.5) × 4		
M_{14}	(10 / 2) × 5		
M_{15}	(10 / 0.5) × 56		
M_{16}	(10 / 2) × 15		

In the following section the main behaviour of the proposed design will be analyzed and design equations derived.

3.3.2 Input Stage: Differential Pair with Bulk Cross-Connected Active Load

The first stage shows a differential output behavior even if the input voltage is applied only to the bulk of M_1 (or equivalently to the bulk of M_2) as has been dimostrated in [64]. Additionally, the differential-mode transconductance of the first stage can be boost by the positive feedback of the cross-connection of the bulk-drain terminals of transistors M_3-M_4. The equivalent circuit of the bulk-driven differential pair used at the input stage of the proposed OTA is shown in Fig. 132 (a). It is composed by transistors M_1 and M_2 whose quiescent current are set by transistor M_B whose body is connected to the virtual ground (i.e., $(V_{DD} + V_{SS})/2$). Consequently, M_B-M_1 and M_B-M_2 form two accurate current mirrors as long as the bulk terminals of M_1 and M_2 are connected to the analog ground. The active load is made up by transistors M_3-M_4 together with the two resistors R. This stage is particularly suitable for ultra-low voltage design due to the minimum supply voltage ($V_{DD} - V_{SS}$) which can be as low as $V_{DS1,2}$+$V_{GS3,4}$. A significant issue is given by resistors R which accurately set the DC common-mode output voltage which does not happen in the traditional version of a bulk-driven differential pair.

Furthermore, the bulk-driven differential pair with bulk cross-connected active load is shown in Fig. 132 (b). The difference from the standard one besides in the bulk terminals of transistor M_3 and M_4. Specifically, the bulk of M_3 (M_4) is cross-connected to the drain of M_4 (M_3). It can be noted that the bulk cross-connection causes a positive feedback loop and consequently some condition must be taken into account to avoid the instability of the circuit.

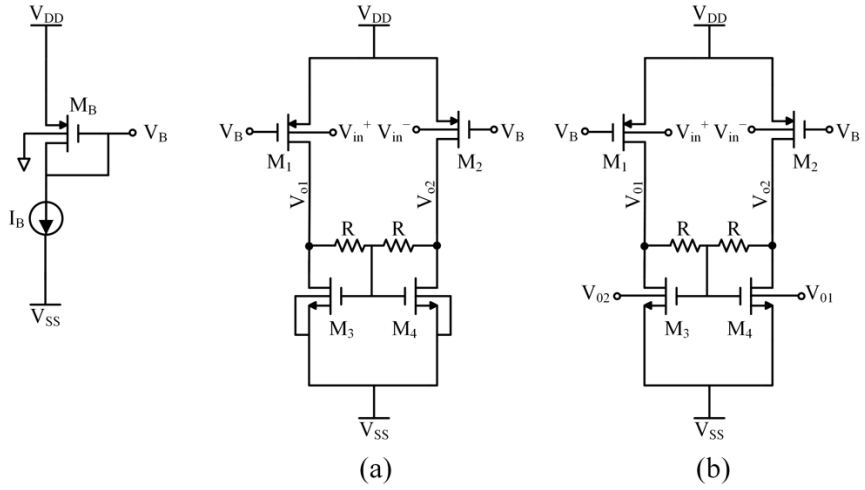


Fig. 131. (a) Bulk-driven differential pair (b) Bulk-driven differential pair with bulk cross-connected active load.

The use of resistors R in the active load of the input stage enables fully differential operation of a pseudo-differential pair M_1-M_2. To better understand, by considering the bulk-driven differential pair shown in Fig. 132 (a) a single-ended small-signal voltage V_d is applied at one input (for example the bulk of M_1) while the second input (the bulk of M_2) is grounded as shown in Fig. 133.

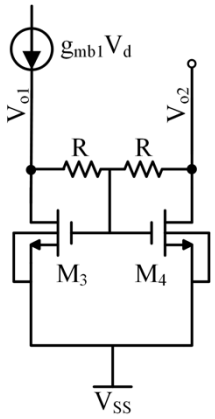


Fig. 132. Equivalent circuit used to prove the differential behavior of the adopted solution.

Referring to Fig. 133, voltage v_d is converted into a current $g_{mb}v_d$, half of which flows through the resistor series and the other half flows through transistor M_3 that having the same v_{gs} and the same transconductance of M_4, they must carry the same current. By inspection of Fig. 133, it is apparent that a differential output voltage $v_{o1}- v_{o2}$ occurs. The expression of the individual output voltages can be approximated as follows:

$$v_{o1} = v_{gs} - g_{mb1}R\frac{v_d}{2} \tag{97}$$

$$v_{o2} = v_{gs} + g_{mb}R\frac{v_d}{2} \tag{98}$$

under the assumption of $g_{mb1} = g_{mb2} = g_{mb1,2}$ and $g_{m3} = g_{m4} = g_{m3,4}$.

The output resistances of transistor M_1 (M_2) and M_3 (M_4) have been neglected but an accurate expression of the output voltage should include the resistors in parallel with R, r_{ds1} and r_{ds3} (R// r_{d1}// r_{d3}) instead of R alone.

By assuming $g_{mb1}R\frac{v_d}{2} = g_{m3}v_{gs}$, equation (97) and (98) can be rewritten in the following form:

$$v_{o1} = g_{mb1}\left(\frac{1}{g_{m3}} - R\right)\frac{v_d}{2} \tag{99}$$

$$v_{o2} = g_{mb1}\left(\frac{1}{g_{m3}} + R\right)\frac{v_d}{2} \tag{100}$$

By assuming $g_{m3,4}R \gg 1$, (99) and (100) provide $v_{o1} = -v_{o2} \cong g_{mb1,2}R\frac{v_d}{2}$ thus demonstrating that a differential operation appear when a voltage v_d is applied to one input terminal by producing a differential output voltage. The same result has been achieved if the input signal was applied to the body of the transistor M_2, thanks to the symmetry of the circuit.

At the end, the single-ended gain of this first stage can be approximated as:

$$A_{d,dp} = \frac{v_{o2}}{v_d} = \frac{g_{mb1,2}R}{2} \tag{101}$$

Therefore, the differential-mode gain of the first stage shown in Fig. 132 (a) can be expressed by (102).

$$A_{d,dp} = g_{mb1,2}(\mathrm{R}//\, r_{o1}) \tag{102}$$

where r_{01} is the equivalent output resistance of the first stage.

In the proposed design, the differential transconductance of the first stage has been enhanced by the positive feedback of the bulk-drain cross-connection of transistor M_3 and M_4. The bulk-driven differential pair with bulk cross-connected active load is shown in Fig. 123 (b). Due to the bulk cross-connection, the differential gain of the first stage expressed in (102) became:

$$A_d = \frac{g_{mb1,2}(\mathrm{R}//\, r_{o1})}{1-g_{mb3,4}(\mathrm{R}//\, r_{o1})} = \frac{A_{d,dp}}{1-g_{mb3,4}(\mathrm{R}//\, r_{o1})} \tag{103}$$

where $g_{mb1,2}$ and $g_{m3,4}$ are the bulk-transconductance of M_1-M_2 and M_3-M_4, respectively and r_{o1} is the parallel of $r_{d1,2}$ and $r_{d3,4}$.

The effect of the positive feedback appears from the negative sign in the denominator of equation (103). Therefore, to preserve the gain and to avoid the generation of a negative resistance, the following condition must be satisfied: $g_{mb3,4}(\mathrm{R}//\, r_{o1}) < 1$ which also implies an increased differential gain than that achieved without bulk cross-connection technique.

3.3.3 Common Mode Rejection Ratio of the Input Stage

The schematic differential input stage used for the analysis of the CMRR is shown in Fig. 134.

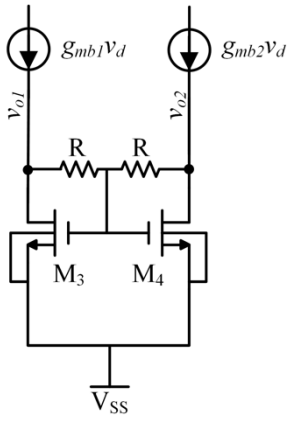


Fig. 133. Differential input stage for the CMRR evaluation.

Resistors R have the additional role to set the common-mode voltage at the drain of transistors M_3-M_4 equal to their gate voltage since under a common-mode input no current flows along them. In reference to Fig. 134, thanks to the absence of the current flowing into R and under a common mode input the common mode gain is given by (104).

$$A_{cm,dp} = \frac{v_{o2}}{v_{cm}} = \frac{g_{mb1,2}}{g_{m3,4}} \tag{104}$$

under the assumption of $g_{mb1} = g_{mb2} = g_{mb1,2}$ and $g_{m3} = g_{m4} = g_{m3,4}$ and $g_{mb1,2}v_{cm} = g_{m3,4}v_{gs}$.

The achieved common-mode in (104) can be easily understood by considering that if no current flows through the resistors R, transistors M_3 and M_4 can be treated as a diode-connected transistors which offer an equivalent resistance equal to $1/g_{m3,4}$.

Consequently, the single-ended common mode rejection ratio is given by (105).

$$CMRR_{dp} = \left|\frac{A_d,dp}{A_{cm,dp}}\right| = \frac{1}{2}\frac{g_{mb1,2}(\mathrm{R}//r_{o1})}{\frac{g_{mb1,2}}{g_{m3,4}}} = \frac{1}{2}g_{m3,4}(\mathrm{R}//r_{o1}) \tag{105}$$

Once again, in the proposed design the bulk-driven differential pair with bulk cross-connected active load has been adopted. Due to the bulk cross-connection, the single-ended common-mode gain become:

$$A_{cm} = \frac{g_{mb1,2}}{g_{m3,4}}\frac{1}{1+g_{mb3,4}(\mathrm{R}//r_{o1})} \tag{106}$$

It can be noted that common-mode gain does not cause any positive feedback since no negative sign appears in the denominator of (106). Consequently, the CMRR for a differential pair with a cross-connected active load became:

$$CMRR = \left|\frac{A_d}{A_{cm}}\right| = \frac{\frac{g_{mb1,2}(\mathrm{R}//r_{o1})}{1-g_{mb3,4}(\mathrm{R}//r_{o1})}}{\frac{g_{mb1,2}}{g_{m3,4}}\frac{1}{1+g_{mb3,4}(\mathrm{R}//r_{o1})}} = CMRR_{dp}\frac{1+g_{mb3,4}(\mathrm{R}//r_{o1})}{1-g_{mb3,4}(\mathrm{R}//r_{o1})} \tag{107}$$

By assuming $g_{mb3,4}(\mathrm{R}//r_{o1})$ close to 1, it is apparent that an improved CMRR has been achieved thanks to the proposed topology.

To conclude, the proposed design thanks to the adoption of a differential input stage with a cross-connected active load allow to increase both the differential gain and the CMRR.

Additionally, the symmetry of the circuit is highly recommended to improve the CMRR and at this purpose, transistor M_5-M_7 shown in the schematic of the proposed OTA (Fig. 131) has been added to the design. Under perfect symmetry conditions which means that the current flowing into M_5 must be equal to the current flowing into M_{12} and a unity current gain of M_7-M_8, the common-mode gain is ideally nullifies.

3.3.4 Frequency Analysis

The small-signal model of the proposed OTA is shown in Fig. 135 where the parasitic capacitance has been neglected for simplicity and R_{oi} represent the output resistance of the i^{th} stage. Additionally, the transconductances and the output resistance values are summarized in Table LXX.

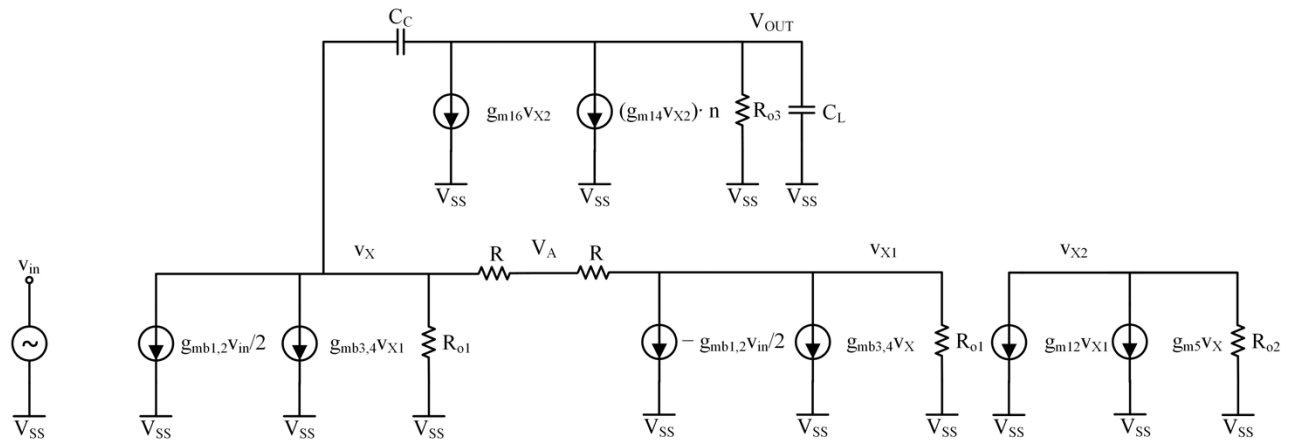


Fig. 134: Small-signal model of the proposed CMOS OTA.

TABLE LXIX: Transconductances and output resistance values of the proposed OTA.

Transconductance	Value (μA / V)	Output Resistance	Value (MΩ)
$g_{mb1,2}$	1.055	$R_{o1} = r_{d1,2}//r_{d3,4}$	5.36
$g_{mb3,4}$	1.145	$R_{o2} = r_{d12}//r_{d8}$	1.10
g_{m12}	6.503	$R_{o3} = r_{d15}//r_{d16}$	1.48
g_{m5}	6.629		
g_{m16}	19.64		
g_{m14}	1.883		

Among the possible frequency compensation strategy, single Miller has been chosen. Therefore, frequency compensation of the proposed OTA has been obtained through capacitor C_C between the output node and the drain of M_3.

Through the small-signal analysis the open-loop transfer function can be approximated as:

$$A(s) \approx A_0 \frac{\left(1+\frac{s}{z_1}\right)}{\left(1+\frac{s}{p_1}\right)(1+a_1 s+a_2 s^2)} \tag{108}$$

where the DC gain A_0, the dominant pole p_1,the zero z_1 and the other parameters are given in the following:

$$A_o \approx \frac{g_{mb1,2} g_{m12} g_{m16} (R_{01}//R) R_{02} R_{o3}}{(1-g_{mb3,4})(R_{01}//R)} \tag{112}$$

$$p_1 = \frac{1}{g_{m12} g_{m16} (R//r_{01}) r_{02} r_{03} C_{c1}} \tag{113}$$

$$z_1 = \frac{g_{m12} g_{m3}}{2C_{C1} g_{m12} - C_{gd12} g_{m3}} \tag{114}$$

The coefficient of the polynomial (108) used to extract the remaining complex conjugate poles are defined as follows:

$$a = \frac{C_{gd12} C_L (2g_{m12}+g_{m3})}{g_{m3} g_{m12} g_{m16}} \tag{115}$$

$$b = \frac{C_c C_L + C_{gd12} C_L g_{m12} r_{02}}{C_c g_{m12} g_{m16} r_{02}} \tag{116}$$

For the non-dominant complex conjugate poles, the damping coefficient is consequently given by:

$$\xi = \frac{b}{2\sqrt{a}} = \frac{C_C + C_{gd12} g_{m12} r_{02}}{2C_c r_{02}} \sqrt{\frac{C_L g_{m3}}{g_{m12} g_{m16} C_{gd12} (2g_{m12}+g_{m3})}} \tag{117}$$

Finally, the gain-bandwidth product ω_{GBW} is given by:

$$\omega_{GBW} = \frac{g_{mb1,2}}{C_c} \tag{118}$$

3.3.5 Slew-Rate

In a multistage-amplifier, the slew-rate (SR) is almost dictated to the slowest stage and is defined through the following expression $SR = min[I_x/C_x]$, where I_x is the maximum current which charge or discharge the capacitor C_x of the x-th stage. Usually, the load capacitor is the largest one, therefore the output node is the most critical as concern the slew-rate performance. In the proposed OTA design, this issue is partially alleviated by adopting the operation in class AB for the last stage thus leading the SR essentially determined by the first stage which drives the compensation capacitor C_C. By assuming the bulk-terminal of transistors M_{13}-M_{15} connected to V_{DD} for the moment, slew-rate can be expressed by equation (119).

$$SR \approx \frac{I_{D1}-I_{D1,MAX}}{C_C} \quad (119)$$

where I_{D1} is the quiescent current of M_1, $I_{D1,MAX}$ is the maximum instantaneous value of I_{D1} and $I_{D1} - I_{D1,MAX}$ is the maximum current with which the capacitor C_C is charged.

However, under large signal the current which drives C_C may be different than the quiescent current $I_{D1,2}$. By assuming the OTA in its buffer configuration, for a positive step on the input the current available from M_1 decrease otherwise for a negative step on the input the current available from M_1 increase. Consequently, this yields to an unbalanced SR performance thus resulting in $SR^+ < SR^-$.

In the proposed OTA design, the additional bulk connection of transistors M_{13} and M_{15} to the internal node V_{x1} and V_{x2} respectively, allow to balance the positive and negative slew-rate by providing an additional current to M_{15} to charge the load capacitor C_L. This happens when a positive step is given to the input terminal, by considering the OTA in its voltage follower configuration. A positive step on V_{in}^+ implies that the voltages on V_{X1} and V_{OUT} go high while the voltage on V_{X2} goes down. The expression of current flowing through M_{13} and M_{15} can be expressed as follows:

$$I_{D13} = \frac{\beta_{13}}{2}(V_{GS} - V_{TH13})^2 \quad (120)$$

$$I_{D15} = \frac{\beta_{15}}{2}(V_{GS} - V_{TH15})^2 \quad (121)$$

where $\beta_{13} = \mu_n C_{ox}\left(\frac{W}{L}\right)_{13}$ and $\beta_{15} = \mu_n C_{ox}\left(\frac{W}{L}\right)_{15}$.

In a current mirror the gate-source voltages are the same while the threshold voltages differ due to their bulk connections thus leading $V_{TH13} \neq V_{TH15}$. The expression of the V_{GS} can be obtained by (120) and substituted on (121) thus obtaining the current flowing into M_{15}.

$$I_{D15} = \frac{\beta_{15}}{2}\left(\frac{2I_{D13}}{\beta_{13}} + (V_{TH13} - V_{TH15})^2 + 2\sqrt{\frac{2I_{D13}}{\beta_{13}}}(V_{TH13} - V_{TH15})\right) \quad (122)$$

In a traditional current mirror, the body effect for each transistor is the same ($V_{TH13} - V_{TH15} = 0$) and the expression of the current become equal to the first term in the equation (122). In the proposed design, when the voltage V_{X1} goes high and V_{X2} goes down, the threshold voltage V_{TH13} goes high while the V_{TH15} goes down. This implies that term ($V_{TH13} - V_{TH15}$) in equation (122) become greater than zero, and consequently the current I_{D15} become higher than one achieved by a traditional current mirror.

Finally, the bulk connection of transistors M_{13} and M_{10} to the voltage V_{X1} and V_{X2}, respectively allow to provide an additional current to the output capacitor through transistor M_{15} during the rising edge of the step on the voltage input thus consequently enhancing the positive slew rate.

Despite the bulk terminal of the last stage has been connected to the internal voltages with the aim to improve the slew-rate performances, this OTA topology is intrinsically affected to an unbalanced SR. Consequently, a slew-rate enhancement technique proposed in [96] has been added to the proposed design with the aim to improve the driving capability of the circuit without affect the power consumption of the overall circuit. The schematic of the proposed OTA with the Slew-Rate Enhancer (SRE) section is shown in Fig. 136 while the transistor sizes in the SRE section are summarized in Table LXXI.

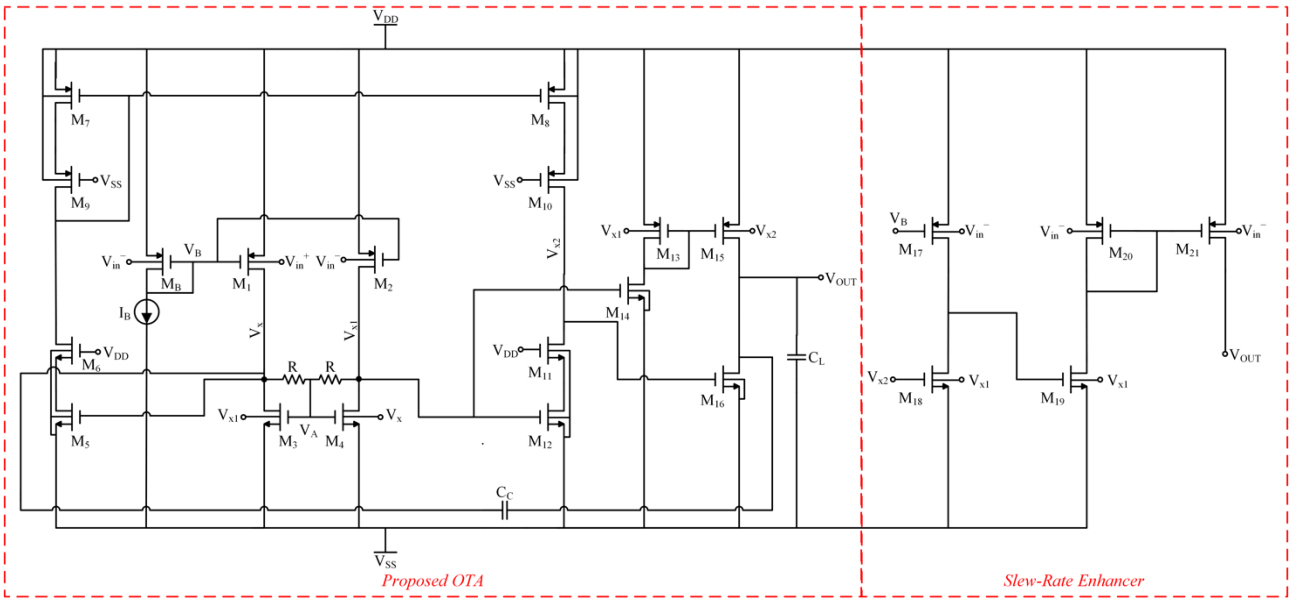


Fig. 135. Schematic of the proposed OTA with the slew-rate enhancer section.

TABLE LXX. Transistor sizes in the SRE section of the proposed OTA.

Transistor	W / L (μm / μm)
M_{17}	(2 / 0.5) × 1
M_{18}	(10 / 2) × 5
$M_{20\text{-}21}$	(10 / 0.5) × 10
M_{19}	(10 / 0.5) × 2

The SRE is made up by two sections implemented by transistors M_{17}-M_{18} and transistors M_{19}-M_{21}, respectively and is driven by voltage V_{X2}. Transistor M_{18} implements a voltage-controlled switch which is enabled during the input voltage transient to provide an additional current to the load. When a positive input step is provided at the input, voltage V_{X1} goes high while voltage V_{X2} goes down, consequently M_{18} is turned OFF since its gate-source voltage is almost zero. In this time interval, the current flows into M_{17} thus forcing its drain voltage high and leading M_{19} to turn on providing an additional charging current to the load capacitor through the mirror $M_{20\text{-}21}$. Otherwise, when a negative step is given to the input, V_{X2} goes high and M_{18} is turned on thus disconnecting the SRE section to the output. It can be noted that $M_{19\text{-}21}$ do not cause additional current dissipation to the OTA since they are OFF in standby condition and, consequently, their contribution to the small-signal transfer function of the OTA can be neglected.

3.3.6 Post-Layout Simulation Results

The proposed bulk-driven three stage class AB OTA with slew-rate enhancer was designed by using a standard 65-nm CMOS bulk technology provided by TSMC while post-layout simulation results have been carried out by using Cadence Virtuoso tool. Two different layout versions have been implemented: one version of the OTA without the slew rate enhancer and another one version of the OTA with the slew-rate enhancer section. Fig. 137 shows the layout of the OTA without the slew-rate enhancer section having an area occupation of 222.77 µm x 235.01 µm while Fig. 138 shows the layout of the OTA together with the slew-rate enhancer section having an area occupation of 253.40 µm x 235.01 µm.

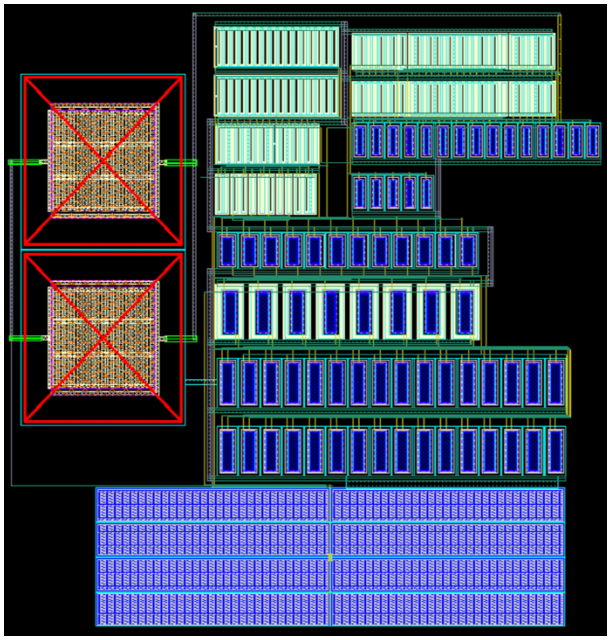


Fig. 136. Layout of the proposed bulk-driven OTA without slew-rate enhancer section.

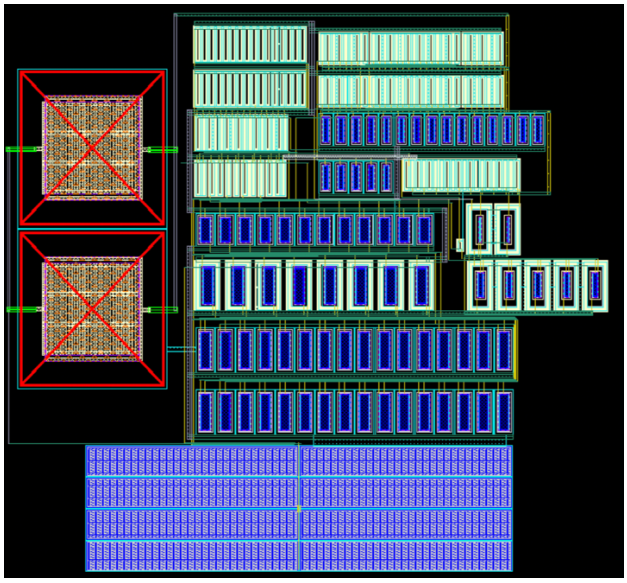


Fig. 137. Layout of the proposed bulk-driven OTA with slew-rate enhancer section.

The simulated open loop frequency response (magnitude and phase) of the proposed bulk-driven OTA is shown in Fig. 139 where a DC gain of 55 dB and a GBW of 23 kHz have been achieved. The stability condition has been achieved through the single Miller compensation method and it was confirmed by the simulated phase margin equal to 60 °.

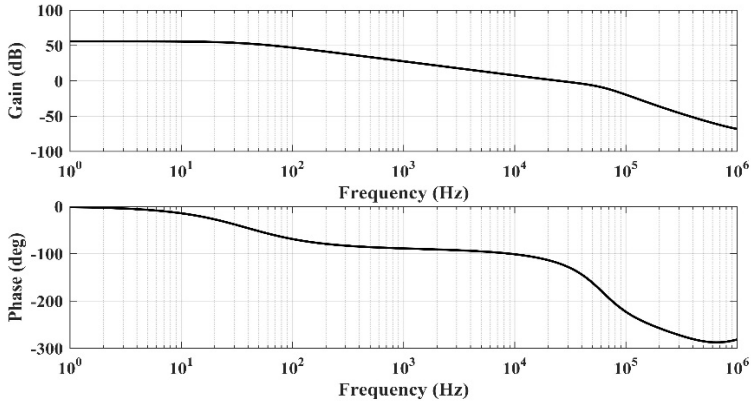


Fig. 138. Open loop frequency response (magnitude and phase) of the proposed bulk-driven OTA.

Temperature dependence of the simulated open loop frequency response (magnitude and phase) of the proposed bulk-driven OTA has been evaluated in the temperature range from 0 °C to 100 °C in the typical corner, as shown in Fig. 140. Additionally, the values achieved by the DC gain, GBW and phase margin as a function of the temperature are summarized in Table LXXII. Temperature insensitivity of the proposed OTA is evident since the main parameters do not change by varying the temperature. Furthermore, stability of the circuit continues to be provided in a wide range of temperature.

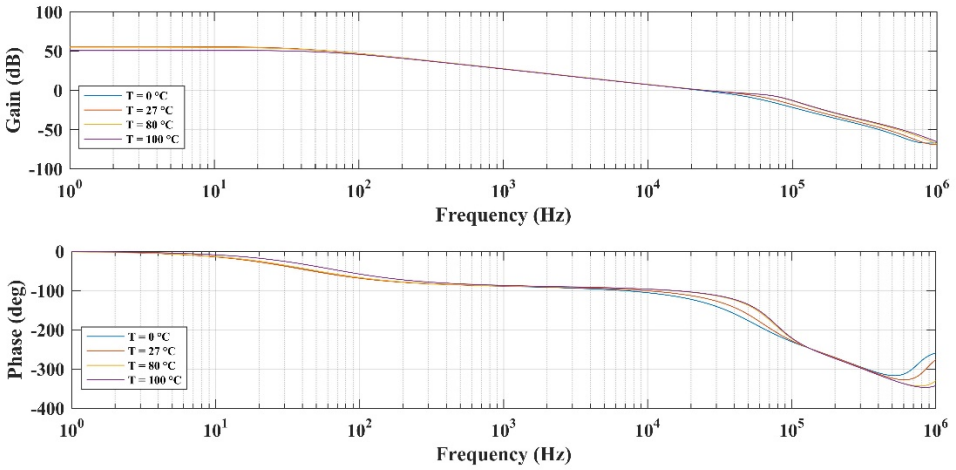


Fig. 139. Temperature dependence of the open loop frequency response (magnitude and phase) in the range [0÷100] °C.

TABLE LXXI: Temperature variations of the DC gain, GBW and phase margin in the typical corner.

Temperature	0 °C	27 °C	60 °C	80 °C	100 °C
DC gain (dB)	55.11	55.4	56.23	55.63	51.92
GBW (kHz)	23	23	26	26	25
Phase Margin (deg)	52	60	68	72	76

The open loop frequency response (magnitude and phase) over corners has been simulated at room temperature (T = 27 °C), as shown in Fig. 141. The achieved results of the DC gain, GBW and phase margin over corners are summarized in Table LXXIII. The achieved results over corners do not differ from that reached with the typical corner proving the corner insensitivity of the proposed OTA architecture.

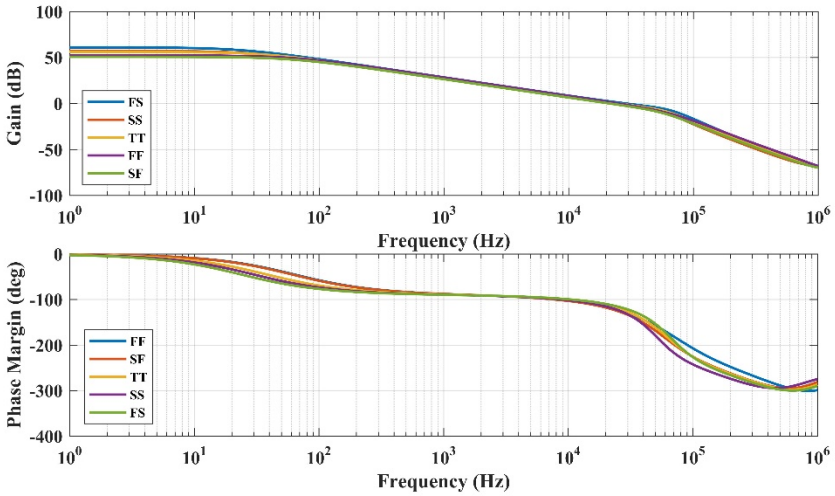


Fig. 140. Open loop frequency response (magnitude and phase) over corners of the proposed bulk-driven OTA.

TABLE LXXII: Corner analysis results of the of the DC gain, GBW and phase margin at room temperature (T = 27 °C)

Temperature	TT	FF	FS	SF	SS
DC gain (dB)	55.4	52.14	60.85	50.60	57.06
GBW (kHz)	23	25	29	21	24
Phase Margin (deg)	60	57	60	61	59

The robustness against process and mismatch variations of the proposed OTA were confirmed by MonteCarlo simulations under 1000 iterations. The Gaussian distribution of the DC gain, GBW and phase margin are shown in Fig. 142, 143 and 144, respectively. The mean value of the DC gain, GBW and phase margin are 55.61 dB, 25.05 kHz and 58.52 °, respectively while their related standard deviations are 2.17 dB, 2.07 kHz and 4.67 °, respectively.

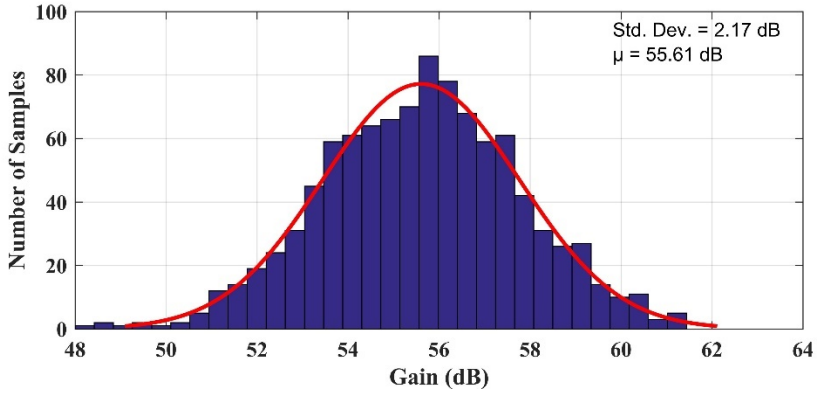


Fig. 141. MonteCarlo simulation of the OTA's DC gain.

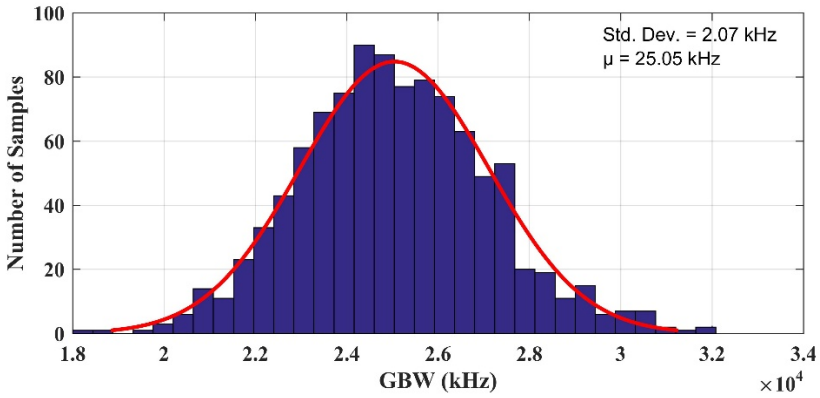


Fig. 142. MonteCarlo simulation of the OTA's GBW.

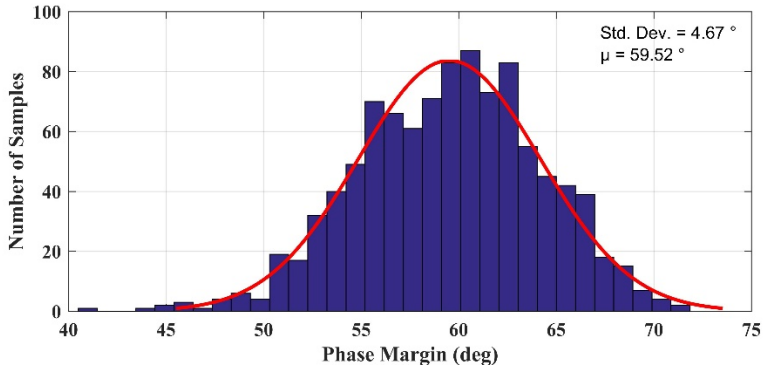


Fig. 143. MonteCarlo simulation of the OTA's phase margin.

Transient response of the proposed OTA in buffer configuration has been evaluated for an input step of 400 mV, as shown in Fig. 145. The achieved results shown the rail-to-rail operation of the bulk-driven OTA where the output voltage follows the input voltage in the overall range of the supply voltage. As expected, the proposed OTA topology is intrinsically affected to an unbalanced SR. Indeed, the achieved results highlight an unbalanced time behavior where the dynamic on the rise is slower than the dynamic on the fall.

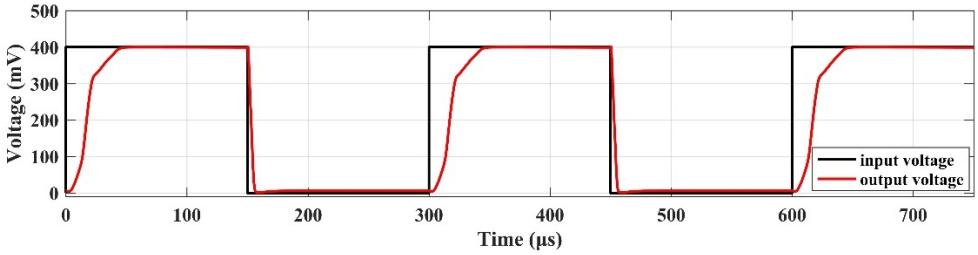


Fig. 144. Transient response of the proposed bulk-driven OTA in buffer configuration.

Beside this, transient response to a 200 mV_{pp} input step of the OTA in buffer configuration has been evaluated as shown in Fig. 146. The simulated positive and negative slew rate values are 0.021 V/μs

and 0.049 V/µs, respectively while the 1% settling time was 41 µs for the positive step and 33 µs for the negative step.

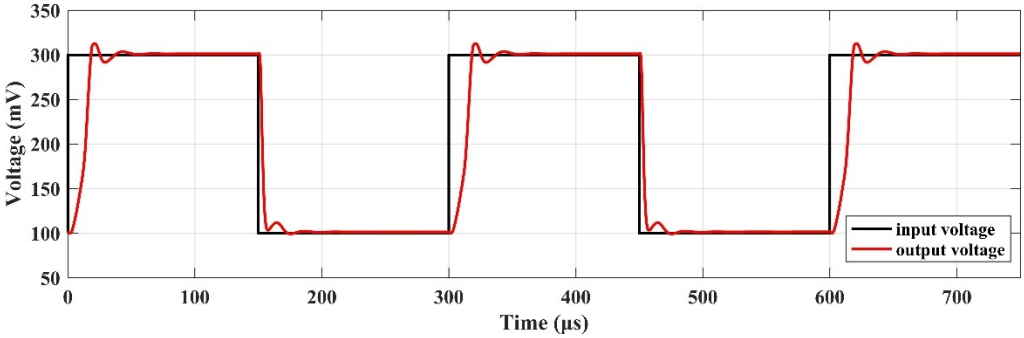


Fig. 145. Transient response of the proposed bulk-driven OTA in buffer configuration to an input step of 200 mV_{pp}.

Time response of the proposed OTA has been improved thanks to the addition of the slew-rate enhancer section to the overall circuit. Transient response comparison between the proposed bulk-driven OTA without and with the Slew-Rate Enhancer (SRE) section has been analyzed, as shown in Fig. 147. The red line shows the OTA's output voltage without SRE while the blue line shows the OTA's output voltage with SRE. The achieved results show the benefit given by the addition of the SRE section to the bulk-driven OTA circuit in terms of positive SR. Indeed, the value of the positive SR without SRE section is 0.005 V/µs while the value of the positive SR with SRE section in 0.021 V/µs.

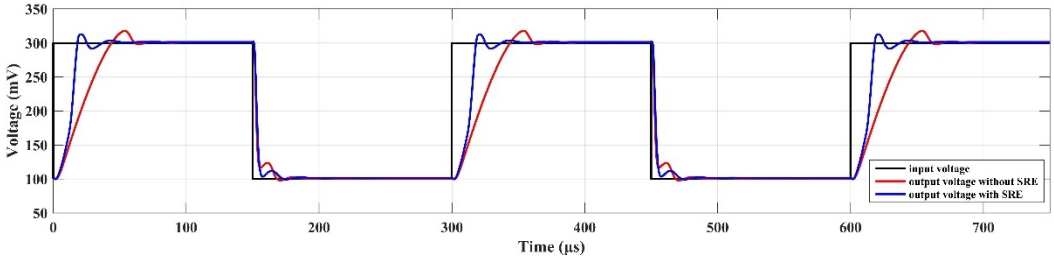


Fig. 146. Transient response of the OTA with and without SRE section in buffer configuration to an input step of 200 mV_{pp}.

Rail-to-rail transient response of the bulk-driven ORA in buffer configuration has been also evaluated for different values of the load capacitance C_L (50 pF, 100 pF, 200 pF, 300 pF and 400 pF), as shown in Fig. 148. The achieved results have proven the stability of the proposed OTA by varying the load capacitance in a wide range from 50 pF to 400 pF.

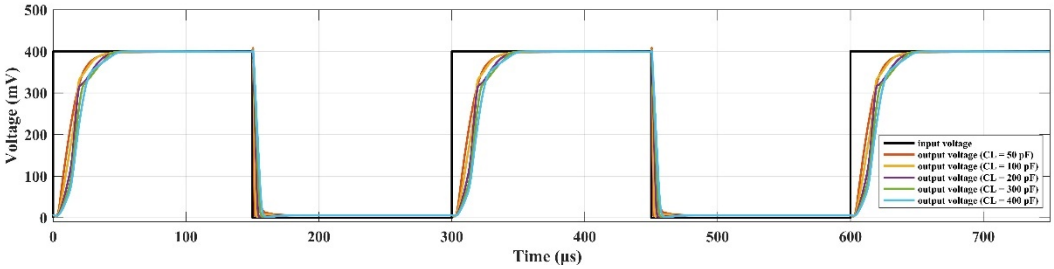


Fig. 147. Rail to rail transient response of the OTA in buffer configuration for different values of the load capacitance.

Temperature dependence of transient response of the OTA in buffer configuration for an input step of 200 mV_{pp} (Fig. 149) has been evaluated in the temperature range from 0 °C to 100 °C by using the typical corner. The achieved results in terms of SR and settling times as a function of temperature are summarized in Table LXXIV. The obtained values underline that temperature variations do not affect the transient behavior of the proposed bulk-driven OTA.

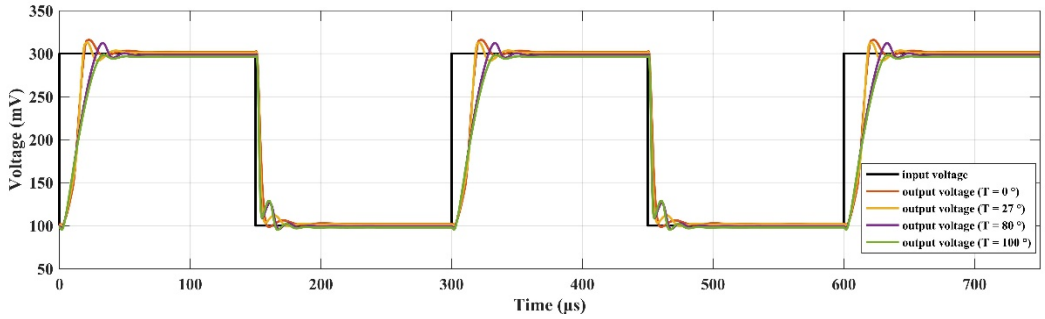


Fig. 148. Temperature dependence of transient response of the proposed bulk-driven OTA.

TABLE LXXIII: SR and settling times as a function of temperature of the proposed bulk-driven OTA.

Temperature	0 °C	27 °C	60 °C	80 °C	100 °C
SR+/SR− (V/µs)	0.018/0.040	0.021/0.049	0.016/0.063	0.009/0.075	0.008/0.080
1% Settling Time (+/−) (µs)	16/17	37/34	31/22	30/25	31/23

Transient response to a 200 mV_{pp} input step of the OTA in buffer configuration as a function of the five basic corners has been carried out at room temperature (T= 27 °C) as shown in Fig. 150. The achieved results in terms of SR and settling times as a function of the corner are summarized in Table LXXV proving that the corner variations do not affect the transient behavior of the proposed bulk-driven OTA.

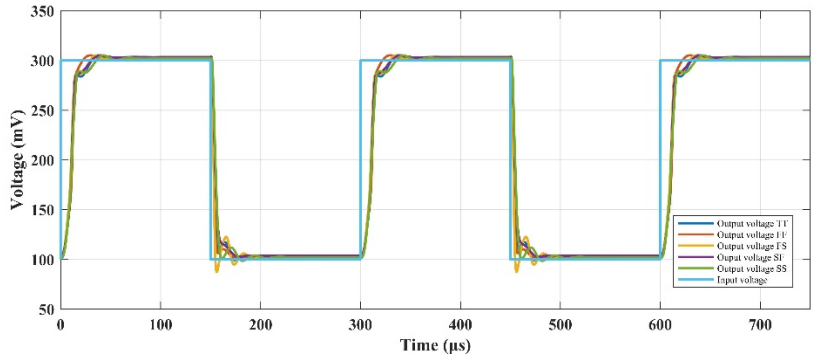


Fig. 149. Transient response of the proposed bulk-driven OTA as a function of the five basic corners.

TABLE LXXIV: SR and settling times as a function of the corner of the proposed bulk-driven OTA.

Corner	TT	FF	FS	SF	SS
SR+/SR− (V/µs)	0.023/0.051	0.022/0.061	0.021/0.076	0.022/0.033	0.018/0.032
1% Settling Time (+/−) (µs)	37/34	30/22	36/33	40/45	41/52

The Common Mode Rejection Ratio (CMRR) has been evaluated through MonteCarlo simulation under 1000 iterations, as shown in Fig. 151. The achieved mean value and standard deviation are 58. 12 dB and 1.73 dB, respectively.

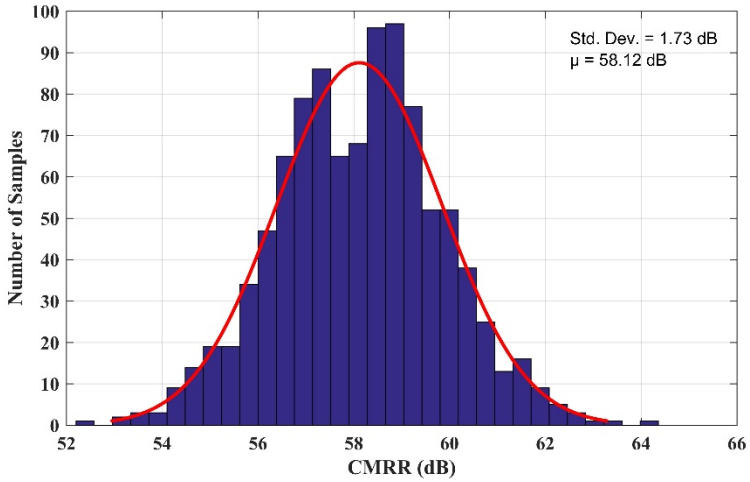


Fig. 150. MonteCarlo simulation of the OTA's CMRR.

Finally, additional simulation on the input noise spectral density of the proposed bulk-driven OTA has been carried out as shown in Fig. 152 and the value reached at 1 kHz is around 829 nV/√Hz.

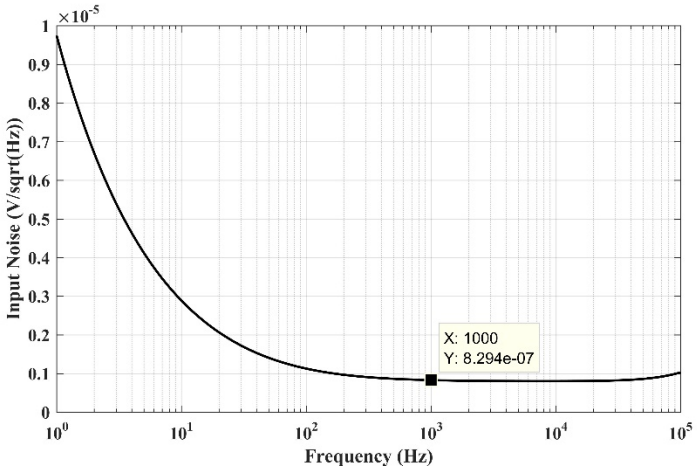


Fig. 151. Input noise of the proposed bulk-driven OTA.

To conclude, the main performances parameters of the proposed OTA are summarized in Table LXXVI where the second and the third column show the simulation results obtained at schematic level and at layout level, respectively. The post-layout simulation results confirm those obtained at the schematic level proving that the layout was made in a proper way. This could be possible by taking into account the design rules in terms of minimum distances and also by taking into account the matching of the transistors in the schematic during the layout design. In this way, the parasitics which could be compromise the performances have been minimized.

TABLE LXXV: Performance parameters of the proposed bulk-driven OTA (pre-layout and post-layout simulation results).

Parameter	Value (Pre-Layout)	Value (Post-Layout)
Supply Voltage (V_{DD}−V_{SS}) (V)	0.4	0.4
Power dissipation (µW)	0.63	0.63
Offset maximum (mV)	6.3	6.8
ICMR	Rail-to-rail	Rail-to-rail
Max Input Current (nA)	0.220	0.224
GBW (kHz)	25	23
CL (pF)	300	300
Phase Margin (deg)	60	60
Gain Margin (dB)	9.27	8.86
SR^+/SR^- (V/µs)	0.023/0.051	0.017/0.049
1% Settling Time (+/−) (µs)	37/34	42/38
CMRR@DC (dB)	58.29	57
$PSRR^+$@DC (dB)	26.14	26.49
$PSRR^-$@DC (dB)	26.07	26.44
Input Ref. Noise @1kHz (nV/√Hz)	829.35	829.35
THD@1kHz,200mV_{p-p}input (%)	0.8	0.8

3.3.7 Comparison With the State of Art

The performances achieved by the proposed OTA have been compared to other low-power OTA proposed at the state of art [46] [47] [50] [53] - [56] [65] [88] [97] - [102], as shown in Table LXXVII. The main OTA parameters such as DC gain, gain-bandwidth product (ω_{GBW}), Phase Margin (PM), Slew-Rate (SR), white noise, Common Mode Rejection ratio (CMRR) and input noise together with well-known Figures of Merit FOM_S and FOM_L (123)-(124) have been considered.

$$FOM_s = \frac{\omega_{GB}}{Power} C_L \quad (123)$$

$$FOM_L = \frac{SR}{Power} C_L \quad (124)$$

For a specified capacitance load, (124) and (125) show a trade-off between small-signal and large-signal parameters regarding the total power consumption.

The adoption of the low supply of 0.4 V together with small consumption of 1.58 µA give rise a small value of power consumption which is one of the advantages of the proposed OTA. The combination between low power consumption together with the small-signal performances give rise the best FOM_S at the state of art. Beside this, the large signal performances have been compared through the FOM_L where the proposed OTA reach one of the best results. A result better than the proposed one has been achieved only by [102] which results really close from that reached by the proposed architecture. Another great results to be considered is that the proposed OTA is able to drive a load capacitance in a range from 50 pF to 200 pF still maintaining the stability condition.

TABLE LXXVI: Performances comparison of the low-power OTA state of art.

Reference	Year	Technology (µm)	Supply Voltage (V)	Supply current (µA)	CL (pF)	DC gain (dB)	GBW (kHz)	PM (deg)	Average SR (V/ms)	CMRR (dB)	Input Noise @1MHz (nV/√Hz)	FOMs [MHz·pF/mW]	FOML [V·pF/(µs· mW)]
[46]	2001	500	1	40	20	69	20000	57	500	--	--	1000	250
[47]	2002	2500	0.9	0.5	12	70	56	62	--	26 min.	--	149	--
[97]	2003	2500	0.8	10	18	50	1200	60	200	--	--	2700	450
[88]	2005	180	0.5	220	20	52	2500	--	2890	78	80	455	525
[50]	2007	350	0.6	0.916	15	69	11	65	14	74.5	290	300	382
[98]	2009	350	0.9	11	2.5	62	540	52	--	129	--	136	--
[53]	2013	350	1	197	15	88	11670	66	1950	40	300	889	148
[54]	2014	130	0.25	0.072	15	40	20	52	0.7	--	3300	1667	583
[55]	2015	65	0.5	366	3	46	38000	57	43000	35	938	623	705
			0.35	49	3	43	3600	56	5600	46	926	630	980
[56]	2016	180	0.7	36.3	20	57.5	3000	60	2800	19	100	2361	2204
[65]	2017	350	0.9	27	10	65	1000	60	2500	45	65	417	104
[99]	2020	180	0.3	0.042	30	64.7	3	52	4150	110	1600	7047	9880
[100]	2021	180	0.5	0.091	15	78	7.5	59	8.6	113.8	650@1kHz	2473	2835
[101]	2022	130	0.3	2.36	100	15	--	11	--	63	722@1kHz	915	--
[102]	2022	180	0.4	0.06	30	60	7	60.2	79	85.4	310@1kHz	8750	98750
Proposed OTA	2023	65	0.4	1.58	300	55	23	60	33	57	829@1kHz	10952	15762

3.4 0.4-V Super Class AB Four-Stage Bulk-Driven CMOS OTA

A four-stage bulk-driven super class AB operational transconductance amplifier (OTA) has been proposed. The proposed solution is based on a modular topology in which additional stage of gain based on the same working principle can be added to the first one to boost the DC gain. Therefore, the core of the circuit is constituted by A first stage of gain based on a bulk-driven differential pair with an additional positive feedback loop implemented by the bulk cross-connection technique. The second stage and the third stage of gain are based on the bulk cross-connection topology and have been designed to boost the gain of the first one. Finally, a four-stage OTA has been designed by adding a last stage in a common-source topology. The great benefit of this topology lies in its auto-compensation indeed the proposed OTA achieves a sufficient phase margin in all condition without the addition of an internal compensation strategy. This is a great result for a four-stage OTA which typically require sophisticated compensation method to achieve the stability condition. Next to this, the proposed OTA is able to work with a 0.4-V supply by using subthreshold operation together with bulk-driven approach to achieve a low-power consumption.

3.4.1 Topology Description

The schematic of the proposed two-stages OTA is shown in Fig.153 in which the core of the circuit is constituted by the input stage. It is based on a bulk-driven differential pair M_1-M_2 whose gate voltages are fixed by transistor M_B and current generator I_B, as was proposed by [64]. Transistors M_3-M_4 together with resistors R constitute the load of the differential pair. The body and drain terminals of M_3 and M_4 are cross-connected as proposed in [95] for a gate-driven OTA. In the proposed design, the bulk cross-connection technique has been used to boost the differential gain and to decrease the common mode-gain. The second stage of gain consists in a common-source topology made up-by transistors M_5-M_8 while additional cascode transistors M_9-M_{11} has been added to improve the robustness of the circuit. It should be noted that the bulk terminals of transistor M_5-M_6 are connected to V_X and to V_{X1}, respectively to be perfectly matched with transistors M_3-M_4.

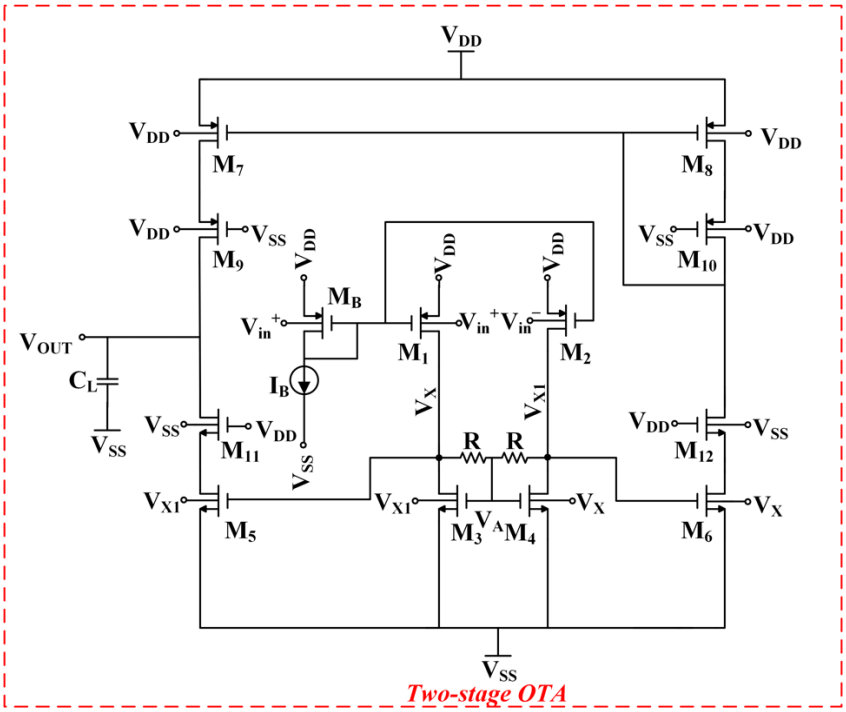


Fig. 152. Schematic of the proposed two-stage OTA.

Table LXXVIII summarized the transistor sizes and device parameters of the proposed two-stage OTA.

TABLE LXXVII: Transistor sizes and device parameters of the proposed two-stage OTA.

Transistor	W / L (μm / μm)	Parameter	Value
$M_{B\text{-}9\text{-}10}$	(30 / 0.5) x 10	I_B	200 nA
$M_{1\text{-}2}$	(90 / 0.5) x 30	R	250 kΩ
$M_{3\text{-}4\text{-}5\text{-}6}$	(60 / 0.5) x 20	C_L	500 pF
$M_{7\text{-}8\text{-}11\text{-}12}$	(30 / 0.25) x 10	V_{DD}–V_{SS}	0.4 V

The schematic of the proposed three-stage OTA is shown in Fig. 154, and it consists of: (1) a first stage of gain which is the core of the two-stage OTA, (2) a second stage of gain made-up by transistors M_5-M_{10}, and (3) a third stage of gain constituted by the common source topology made up by transistors M_{13}-M_{20}. Table LXXIX summarized the transistor sizes and device parameters of the proposed three-stage OTA.

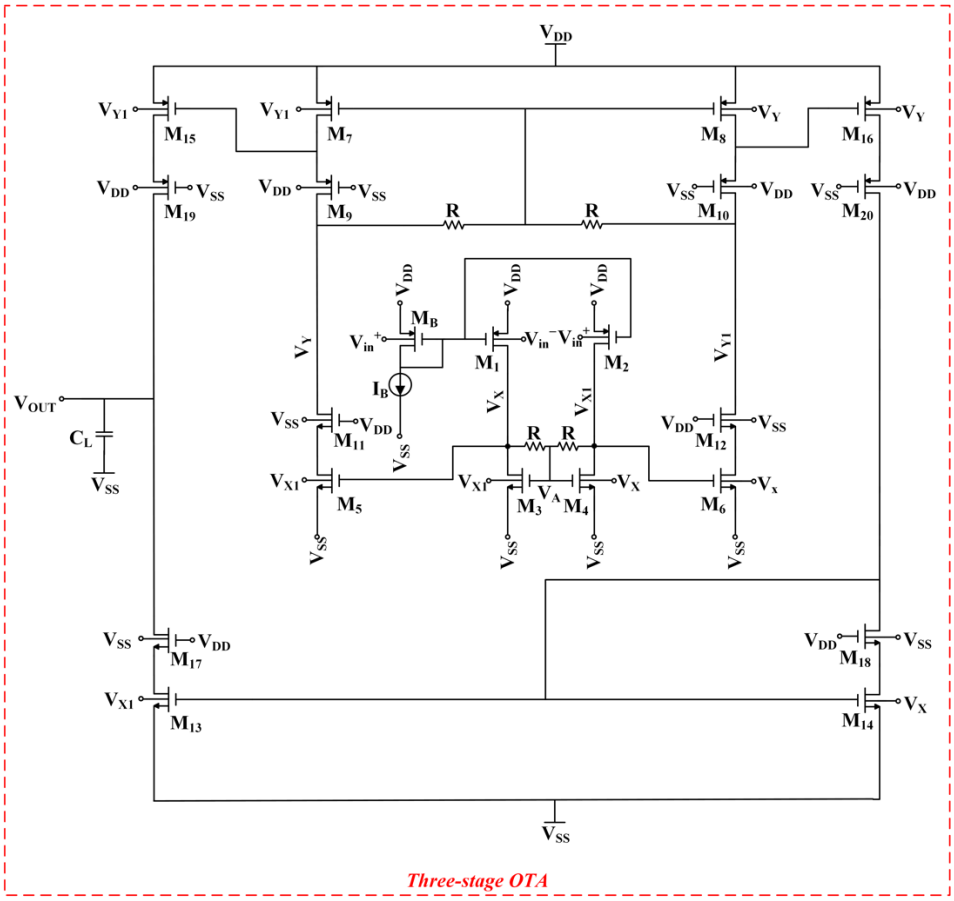


Fig. 153. Schematic of the proposed three-stage OTA.

TABLE LXXVIII. Transistor sizes and device parameters of the proposed three-stage OTA.

Transistor	W / L (μm / μm)	Parameter	Value
$M_{B\text{-}9\text{-}10}$	(30 / 0.5) x 10	I_B	200 nA
$M_{1\text{-}2}$	(90 / 0.5) x 30	R	250 kΩ
$M_{3\text{-}4\text{-}5\text{-}6\text{-}13\text{-}14}$	(60 / 0.5) x 20	C_L	500 pF
$M_{7\text{-}8\text{-}11\text{-}12\text{-}17\text{-}18\text{-}15\text{-}16}$	(30 / 0.25) x 10	V_{DD}–V_{SS}	0.4 V
$M_{19\text{-}20}$	(10 / 0.5) x 10		

The second stage of gain is constituted by transistors M_5-M_{10} which re-use the working principle adopted by transistors M_3-M_4 in the active load in the core of the circuit. Specifically, under a perfect matching, transistors M_3-M_5 and M_4-M_6 act like a current mirror by setting the current to the active load of the second stage which is implemented by transistors M_7-M_8 together with the resistors R. The body and the drain terminal of the transistors M_7-M_8 are cross-connected to boost the differential gain. Specifically, the body terminal of M_7 is connected to V_{Y1} that is the drain of M_8 while the body terminal of M_8 is connected to V_Y that is the drain of M_7. Additionally, cascode transistors M_{17}-M_{20} has been added to improve the robustness of the design.

The third stage of gain is implemented by a common-source structure made up by transistors M_{13}-M_{16} with additional cascode transistors M_{17}-M_{20}.

Finally, the circuit schematic of the proposed four-stage OTA is shown in Fig. 155, and it consists of: (1) the first two stage of gain which are the same used for the proposed three-stage OTA, (2) a third stage of gain made up by transistors M_{13}-M_{16} and (3) a fourth stage of gain made up by transistors M_{21}-M_{24} which implement a common-source structure. Table LXXX summarized the transistor sizes and the device parameters of four-stage OTA.

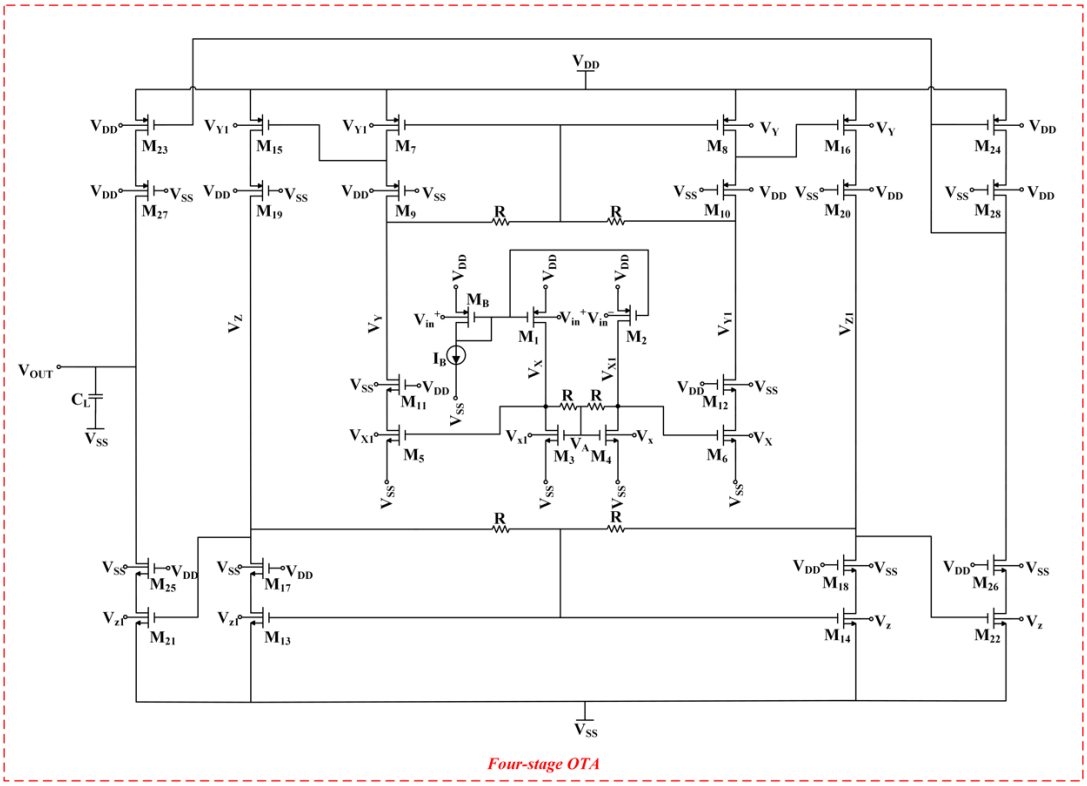


Fig. 154. Schematic of the proposed four-stage OTA.

TABLE LXXIX. Transistor sizes and device parameters of the proposed four-stage OTA.

Transistor	W / L (μm / μm)	Parameter	Value
$M_{B\text{-}9\text{-}10}$	(30 / 0.5) x 10	I_B	200 nA
$M_{1\text{-}2}$	(90 / 0.5) x 30	R	250 kΩ
$M_{3\text{-}4\text{-}5\text{-}6\text{-}13\text{-}14}$	(60 / 0.5) x 20	C_L	500 pF
$M_{7\text{-}8\text{-}11\text{-}12\text{-}17\text{-}18\text{-}15\text{-}16\text{-}25\text{-}26\text{-}23\text{-}24}$	(30 / 0.25) x 10	V_{DD}–V_{SS}	0.4 V
$M_{19\text{-}20\text{-}27\text{-}28}$	(10 / 0.5) x 10		
$M_{21\text{-}22}$	(15 / 0.5) x 5		

The third stage of gain is constituted by transistors M_{13}-M_{16} which re-use the working principle adopted by transistors M_3-M_4 in the active load of the core of the circuit and by transistors M_7-M_8 in the second stage of gain. Under a perfect matching, transistors M_7-M_{15} and M_8-M_{16} act like a current mirror by setting the current into the active load made up by transistors M_{13}-M_{14} together with the resistors R. The body and the drain terminals of transistors M_{13}-M_{14} are cross-connected to boost the differential gain of the third stage. Specifically, the body terminal of M_{13} is connected to V_{Z1} that is the drain of M_{14} while the body terminal of M_{14} is connected to V_Z that is the drain of M_{13}.

The fourth stage of gain has been implemented by a common-source topology constitutes by transistors M_{21}-M_{24}. It should be noted that under a perfect matching, transistors M_{21}-M_{13} and M_{14}-M_{22} act like a current mirror thus setting the current into transistors M_{23}-M_{24}.

Finally, additional cascode transistors M_{17}-M_{20} and M_{25}-M_{28} have been added to complement the proposed design.

3.4.2 Operating Point

By considering the circuit schematic in Fig. 155, transistor M_B, whose body is connected to the virtual ground i.e., $(V_{DD} + V_{SS})/2$, set the quiescent current of the differential pair M_1-M_2 and of its active load M_3-M_4 through the current mirror aspect ratio $(W/L)_{1,2}/(W/L)_B$. Indeed, transistors M_B-M_1 and M_B-M_2 whose body terminal are connected to the analog ground, form two current mirrors which accurately set the DC current into the differential pair M_3-M_4. Considering that no DC current flows through the resistor R, the drain terminals of M_3-M_4 are at the same potential of their gate terminals thus acting like a diode-connected transistors. Therefore, transistors M_3-M_6 have the same gate-source voltage of transistors M_3-M_4 which can be expressed as V_{SG}. Since the complete expression of the threshold voltage of a PMOS transistor can written in the following form: $V_{TH} = V_{THO} - \gamma\left(\sqrt{2\Phi_F + V_{SB}} - \sqrt{2\Phi_F}\right)$ and by neglecting the channel length modulation, the DC current ratio $I_{D5,6}/I_{D3,4}$ by assuming the operation in saturation became:

$$\frac{I_{D5,6}}{I_{D3,4}} = \frac{(W/L)_{5,6}}{(W/L)_{3,4}}\left[1 - \frac{\gamma\left(\sqrt{2\Phi_F+V_{SB}}-\sqrt{2\Phi_F}\right)}{V_{SG}+V_{THO}}\right]^2 \quad (125)$$

The current in (123) is then mirrored through the current mirror M_7-M_{15} and M_8-M_{16} into the third stage thus obtaining a DC current ratio $I_{D15,16}/I_{D7,8}$ in the following form:

$$\frac{I_{D15,16}}{I_{D7,8}} = \frac{(W/L)_{15,16}}{(W/L)_{7,8}}\left[1 - \frac{\gamma\left(\sqrt{2\Phi_F+V_{SB}}-\sqrt{2\Phi_F}\right)}{V_{SG}+V_{THO}}\right]^2 \quad (126)$$

where $I_{D7,8} = I_{D5,6}$.

Consequently, the current flowing into the fourth stage can be expressed through the following DC current ratio:

$$\frac{I_{D21,22}}{I_{D13,14}} = \frac{(W/L)_{21,22}}{(W/L)_{13,14}}\left[1 - \frac{\gamma\left(\sqrt{2\Phi_F+V_{SB}}-\sqrt{2\Phi_F}\right)}{V_{SG}+V_{THO}}\right]^2 \quad (127)$$

where $I_{D13,14} = I_{D15,16}$.

3.4.3 Slew-Rate

The slew-rate is defined through the following expression $SR = min\,[I_x/C_x]$, where I_x is the maximum current which charge or discharge the capacitor C_x of the x-th stage. In a multistage amplifier like this one, the slew-rate is dictated by the slowest stage. In the proposed OTA, the load capacitor the largest one therefore the output node is the most critical concerning the slew-rate performances. Hence, the expression of the SR is given as follows:

$$SR \approx \frac{I_{D23} - I_{D23,MAX}}{C_L} \quad (128)$$

where I_{D23} is the quiescent current of M_{23}, $I_{D23,MAX}$ is the maximum instantaneous value of I_{D23} and $I_{D1} - I_{D1,MAX}$ is the maximum current with which the capacitor C_L is charged. It can be noted that the current I_{D23} is related to the quiescent current $I_{D1,2}$ to within a factor given by the aspect ratio of the current mirror.

Consequently, under a large signal the current which drives the load capacitor may be different than the I_{D23} due to the variation on the quiescent current $I_{D1,2}$. By assuming the OTA in its buffer configuration, for a positive step on the input the current available from M_1 decrease otherwise for a negative step on the input the current available from M_1 increase. Consequently, this yields to an unbalanced SR performance thus resulting in $SR^+ < SR^-$.

3.4.4 Frequency Response

The small-signal model of the proposed OTA is shown in Fig. 156 where the parasitic capacitances have been neglected for simplicity and R_{oi} represent the output resistance of the i^{th} stage. The first stage provides an output gain in the form (103). The second and the third stage of gain replicate the same working principle of the first stage thus producing an output gain in its own form. Finally, the output gain of the fourth stage is the typical one for a common-source structure.

The expression of the output gain of each stage are shown in the following equations.

$$A_{o1} = \frac{g_{mb1,2}(\mathrm{R}//R_{o1})}{1-g_{mb3,4}(\mathrm{R}//R_{o1})} \tag{129}$$

$$A_{o2} = \frac{g_{mb5,6}(\mathrm{R}//R_{o2})}{1-g_{mb7,8}(\mathrm{R}//R_{o2})} \tag{130}$$

$$A_{o3} = \frac{g_{mb15,16}(\mathrm{R}//R_{o3})}{1-g_{mb13,14}(\mathrm{R}//R_{o3})} \tag{131}$$

$$A_{o4} = g_{mb21}\,R_{o4} \tag{132}$$

where A_{o1}, A_{o2}, A_{o3} and A_{o4} are the output gain of the first, the second, the third and the fourth stage of gain, respectively. The output resistances are given by: $R_{o1} = r_{d1,2}//r_{d3,4}$, $R_{o2} = r_{d5}//r_{d7}$, $R_{o3} = r_{d15}//r_{d13,}$ $R_{o4} = r_{d23}//r_{d21}$.

The overall gain of the proposed OTA is given by:

$$A_o = A_{o1} \cdot A_{o2} \cdot A_{o3} \cdot A_{o4} \tag{133}$$

It is clearly apparent by inspection of (133) that the great advantage of this topology lies in its replicability which allow to boost the gain of the OTA by adding supplementary stage of gain based on the same working principle.

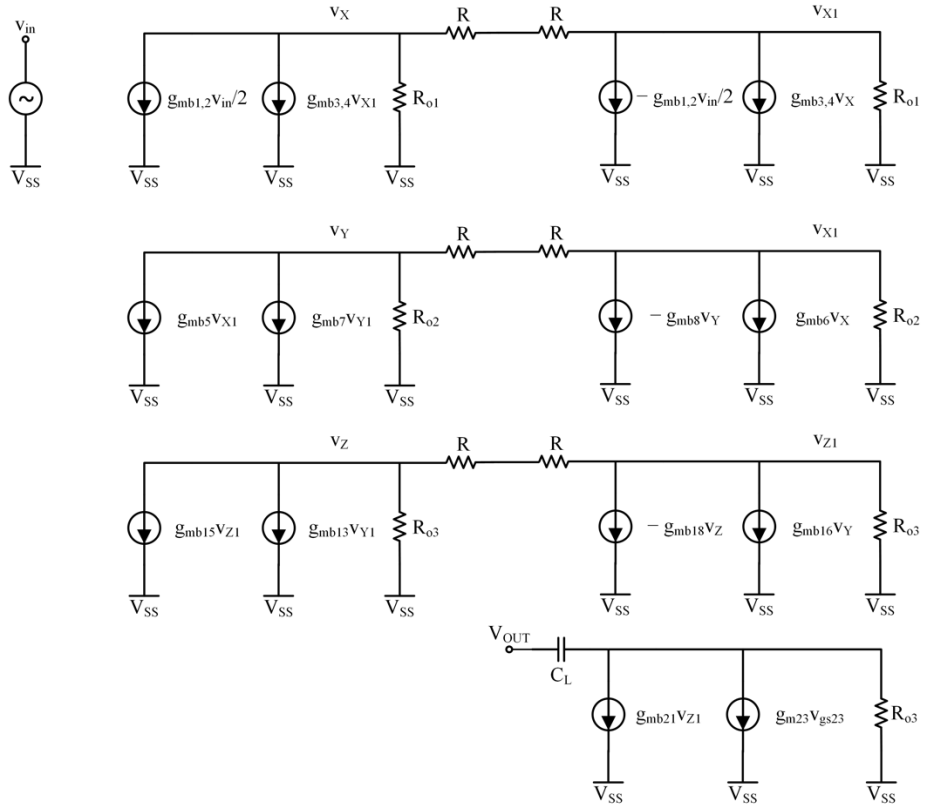


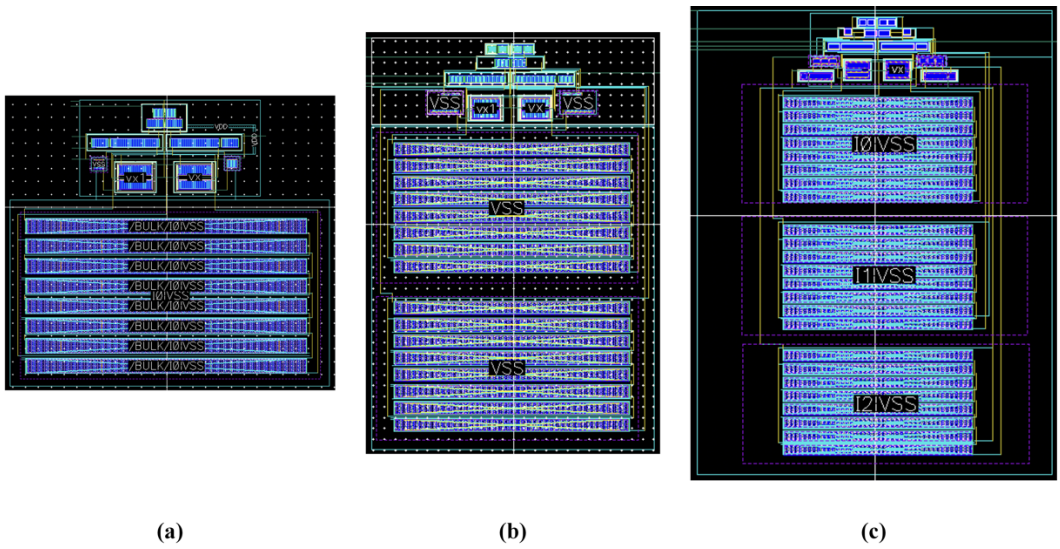
Fig. 155. Small-signal circuit of the proposed four-stage OTA.

The great advantage besides into the internal node compensation which results in a stability condition for the proposed four-stage OTA. The internal compensation is essentially due by the use of R values together with a positive feedback factor which makes the internal nodes to have relatively low impedance thus resulting in a “quasi” single stage OTA topology.

3.4.5 Post-Layout Simulation Results

The three different structure of bulk-driven class AB OTAs has been designed by using a standard 28-nm CMOS bulk technology provided by TSMC while post-layout simulation results have been carried out by using Cadence Virtuoso tool.

The layout of the proposed two-stage, three-stage, and four-stage OTAs are shown in Fig. 157. (a), (b) and (c), respectively. Table LXXXI summarized the information regarding the area occupation of the three topologies of OTA highlighting that resistors sizes occupying most of the area occupation.



(a) (b) (c)

Fig. 156. Layout of proposed OTAs: (a) two-stage, (b) three-stage, and (c) four-stage.

TABLE LXXX. Area occupation of the OTAs layout and resistor sizes.

	Two-stage OTA	**Three-stage OTA**	**Four-stage OTA**
Area occupation (µm x µm)	124.18 x 111.485	131.25 x 191.33	205.44 x 268.1
Resistor area occupation (µm x µm)	124.18 x 72.535	131.25 x 150.04	205.44 x 225.20

Fig. 158 show the post-layout simulation of the frequency response of the proposed OTAs at room temperature and 400 mV of supply, specifically: (1) the green line is the frequency response of the two-stage OTA, (2) the red line is the frequency response of the three-stage OTA, and (3) the black line is the frequency response of the four-stage OTA. It is apparent that the DC gain increase by passing from the two-stage to the four-stage structure. Particularly, the DC gain is 57.52 dB for the two-stage OTA, 71.39 dB for the three-stage OTA, and 88.08 dB for the four-stage OTA. This means that the DC gain has been increased of 14 dB by passing from the two-stage to the three-stage structure and has been increased of 17 dB by passing from the three-stage to the four-stage structure. Sufficient phase margin has been achieved by each OTAs, specifically: 89.19° for the two-stage OTA, 81.25° for the three-stage OTA and 69.72° for the four-stage OTA. Finally, the gain-bandwidth (GBW) of the two-stage OTA, three-stage OTA, and four-stage OTA are 6.97 kHz, 47.12 kHz, and 82.23 kHz respectively.

The achieved results underline that the DC can be boost by adding stage of gain made up by the same structure. Additionally, a good phase margin of any structure proof the stability of the OTAs which has been achieved without taking into account any internal compensation strategy.

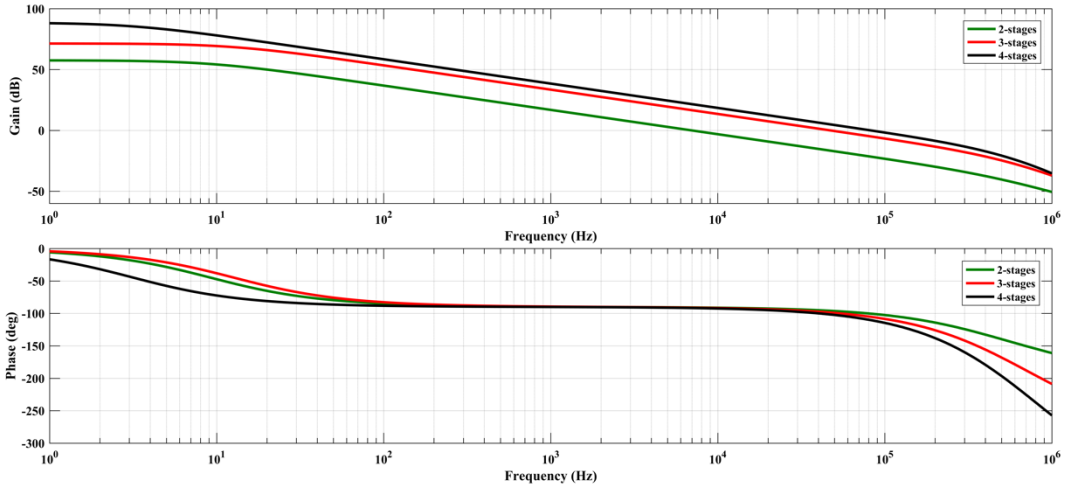


Fig. 157. Post-layout frequency response of the proposed OTAs: DC gain and phase.

DC gain, GBW and phase-margin have been simulated by changing the temperature from 0 to 100 °C by using the typical model of the transistors and by setting the supply equal to 400 mV. Table LXXXII, LXXXIII and LXXXIV summarized the simulation results obtained by the two-stage, three-stage, and four-stage structures, respectively. The achieved results prove the robustness of the proposed OTAs in a wide temperature range.

TABLE LXXXI. DC gain, GBW and phase margin over temperature for the proposed two-stage OTA.

Temperature	**0 °C**	**27 °C**	**60 °C**	**80 °C**	**100 °C**
DC gain (dB)	56.42	57.52	51.74	47.01	42.4
GBW (kHz)	7.59	6.97	6.11	5.64	5.21
Phase Margin (deg)	89.07	89.19	89.41	89.6	89.84

TABLE LXXXII. DC gain, GBW and phase margin over temperature for the proposed three-stage OTA.

Temperature	**0 °C**	**27 °C**	**60 °C**	**80 °C**	**100 °C**
DC gain (dB)	66.78	71.39	69.47	65.98	62.17
GBW (kHz)	34.42	47.12	46.11	41.72	35.97
Phase Margin (deg)	83.56	81.25	81.25	82.73	83.91

TABLE LXXXIII. DC gain, GBW and phase margin over temperature for the proposed four-stage OTA.

Temperature	**0 °C**	**27 °C**	**60 °C**	**80 °C**	**100 °C**
DC gain (dB)	87.68	88.08	82.4	78.08	73.18
GBW (kHz)	49.02	82.23	84.25	74.22	62.06
Phase Margin (deg)	78.1	69.72	69.53	72.12	75.14

Additional simulation of the DC gain, GBW and phase-margin have been carried out by changing the models of the transistors at room temperature (27 °C) under 400-mV of supply. The achieved results are summarized in Table LXXXV, LXXXVI and LXXXVII which underline that the proposed OTAs are robustness over corner variations.

TABLE LXXXIV. DC gain, GBW and phase margin over corners for the proposed two-stage OTA.

Corner	TT	FF	FS	SF	SS
DC gain (dB)	57.52	53.6	54.8	58.7	59.02
GBW (kHz)	6.97	5.16	6.86	7.03	9.62
Phase Margin (deg)	89.19	89.65	89.27	89.13	88.27

TABLE LXXXV. DC gain, GBW and phase margin over corners for the proposed three-stage OTA.

Corner	TT	FF	FS	SF	SS
DC gain (dB)	71.39	68.33	66.16	75.05	71.83
GBW (kHz)	47.12	30.67	35.7	53.65	60.05
Phase Margin (deg)	81.25	85.94	83.61	79.74	74.36

TABLE LXXXVI. DC gain, GBW and phase margin over corners for the proposed four-stage OTA.

Corner	TT	FF	FS	SF	SS
DC gain (dB)	88.08	79.46	82.04	91.64	93.02
GBW (kHz)	82.23	45.48	52.71	102.8	104.2
Phase Margin (deg)	69.72	81.86	77.63	63.65	55.39

The robustness of the proposed OTAs has been also evaluated by considering the process variation during preliminary Monte Carlo simulations under 100 samples (room temperature and 400-mV supply). Smallest process variations on frequency response parameters have been achieved by the two-stage structure while greater process variation have been achieved by the four-stage structure, as shown in Table LXXXVIII, LXXXIV and XC.

TABLE LXXXVII. Monte Carlo simulation under 100 samples of the two-stage OTA.

Two-stage OTA	Mean Value	σ
DC gain (dB)	57.24	0.99
GBW (kHz)	6.98	0.91
Phase Margin (deg)	89.18	0.22

TABLE LXXXVIII. Monte Carlo simulation under 100 samples of the three-stage OTA.

Three-stage OTA	Mean Value	σ
DC gain (dB)	71.16	2.37
GBW (kHz)	47.95	12.85
Phase Margin (deg)	80.88	3.93

TABLE LXXXIX. Monte Carlo simulation under 100 samples of the four-stage OTA.

Four-stage OTA	Mean Value	σ
DC gain (dB)	87.79	2.98
GBW (kHz)	84.95	28.65
Phase Margin (deg)	68.54	8.94

Gaussian distribution of the DC gain, GBW and phase margin of the four-stage OTA are shown in Fig. 159, 160, and 161 respectively. The mean value of the DC gain is 87.79 dB with a standard deviation of 2.98 dB, the mean value of the GBW is 84.95 kHz with a standard deviation of 28.65 kHz, and the mean value of the phase margin is 68.54° with a standard deviation of 8.93°.

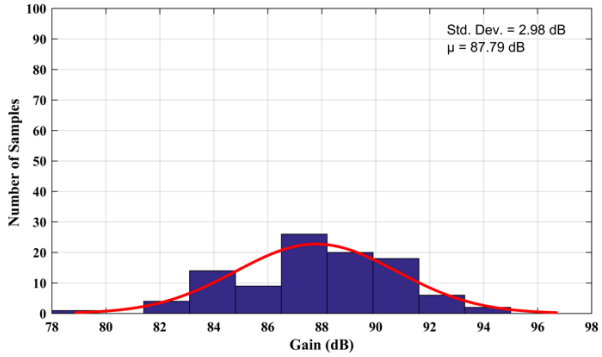


Fig. 158. Monte Carlo simulation of the DC gain of the proposed four-stage OTA.

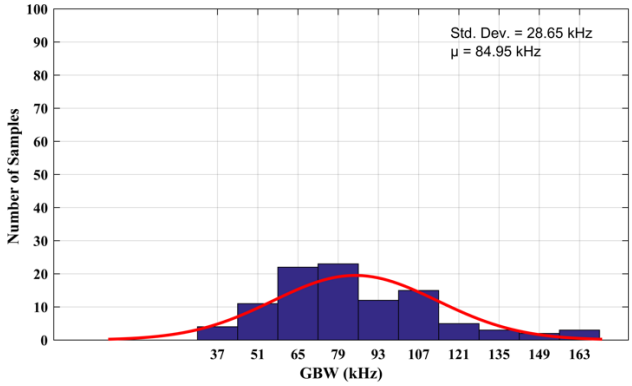


Fig. 159. Monte Carlo simulation of the GBW of the proposed four-stage OTA.

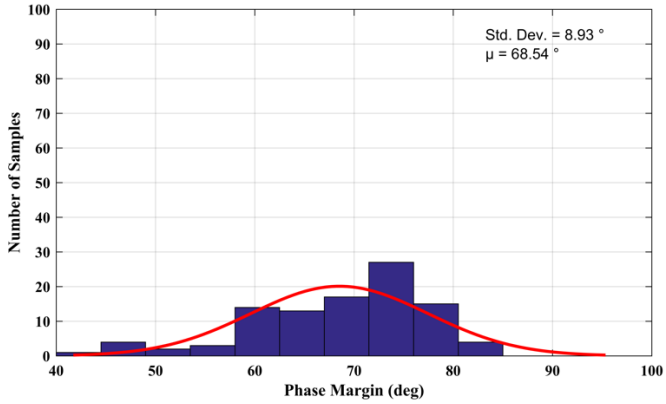


Fig. 160. Monte Carlo simulation of the phase margin of the proposed four-stage OTA.

Time response of the proposed OTAs have been evaluated by using the buffer configuration by considering an input step of 300 mV_{pp}, as shown in Fig. 162. The proposed OTA in its two-stage configuration do not work properly in a rail-to-rail input range due to an intrinsic offset of the structure. In that case, the output voltage is not able to reach the maximum value of the input voltage of 400 mV and the minimum of 0 V by showing an intrinsic offset. This do not happen for the three-stage and four-stage structures which shown a rail-to-rail operation.

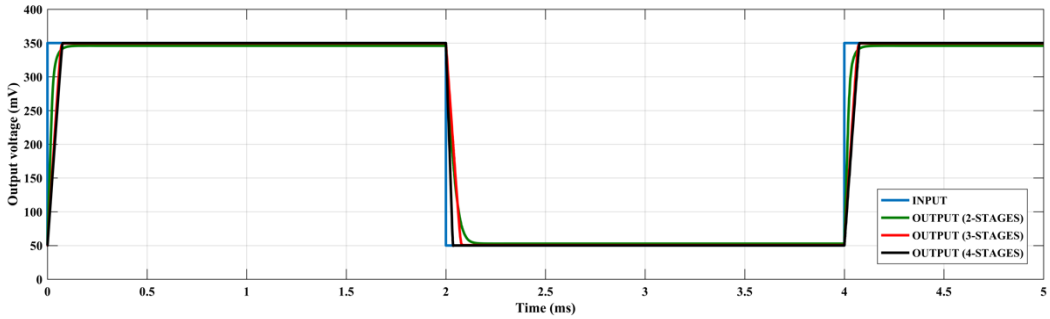


Fig. 161. Time response of the proposed OTAs to a 300-mV_{pp} input step.

Time response performances in terms of positive and negative slew-rate (SR) of the OTAs have been evaluated by considering a reduced input step of 200 mV_{pp}, as shown in Fig. 163. These results have been achieved by considering the typical model of the transistors at room temperature and under 400 mV of supply. The positive and negative SR are 4.64 V/ms and 4.64 V/ms for the two-stage configuration, 4.39 V/ms and 4.39 V/ms for the three-stage configuration, and 4.06 V/ms and 4.06 V/ms for the four-stage configuration. The achieved results shown that the SR is symmetrical by considering any configurations and also that the time response performances are always the same in all the configurations.

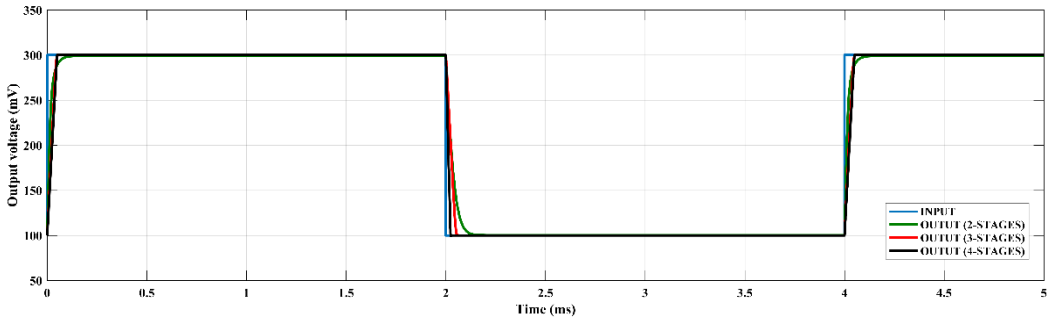


Fig. 162. Time response of the proposed OTAs to a 200-mV_{pp} input step.

Simulated values of the positive and negative SR have been evaluated over corners at room temperature and under 400-mV supply, as shown in Table XCI. The highest SR values have been achieved by the three-state OTA under FF models while the lowest SR values have been achieved by the four-stage OTA under SS models.

TABLE XC. Positive and negative slew rate over corners for the proposed OTAs (200-mV_{pp} input step).

Corner	TT	FF	FS	SF	SS
SR+/SR− (V/ms) (2-stage)	4.64/4.64	3.83/3.83	3.99/3.99	4.86/4.86	4.23/4.23
SR+/SR− (V/ms) (3-stage)	4.39/4.39	7.43/7.43	2.83/2.83	6.68/6.68	2.51/2.51
SR+/SR− (V/ms) (4-stage)	4.05/4.05	7.11/7.11	2.71/2.71	5.32/5.32	2.29/2.29

Temperature dependence of the positive and negative SR have been evaluated by changing the temperature from 0 to 100 °C, by using the typical model of the transistors as shown in Table XCII. The highest values of SR have been achieved at 100 °C by the three-stage OTA while the lowest SR values have been achieved at 0 °C by the four-stage OTA.

TABLE XCI. Positive and negative slew rate over corners for the proposed OTAs (200-mV_{pp} input step).

Temperature	0 °C	27 °C	60 °C	80 °C	100 °C
SR+/SR− (V/ms) (2-stage)	3.45/3.45	4.64/4.64	4.72/4.72	4.38/4.38	3.94/3.94
SR+/SR− (V/ms) (3-stage)	2.25/2.25	4.39/4.39	8.29/8.29	11.28/11.28	14.42/14.42
SR+/SR− (V/ms) (4-stage)	2.04/2.04	4.06/4.06	7.81/7.81	10.82/10.82	14.37/14.37

Finally, supply current I_q of the OTAs has been simulated by changing the corner models of the transistors as shown in Table XCIII. The simulations have been carried out at room temperature under 0.4-V supply. By considering the typical models, the current increase of only 1.27 µA by passing form the 2-stage to the 4-stage configuration. The current variations over corner are: 0.08 µA, 0.28 µA, and 0.32 µA for the 2-stage OTA, 3-stage OTA, and 4-stage OTA, respectively thus underlining that the current does not change over corner. This means that the addition of a stage of gain allow to boost the gain without significantly increasing the current consumption. Additionally, the minimum value of the supply current is 2.44 µA which has been achieved by 2-stage OTA under SS corner while the maximum value of the supply current is 3.79 µA which has been achieved by the 4-stage OTA under SF corner.

TABLE XCII. Supply current I_q of the OTAs over corner.

Corner	TT	FF	FS	SF	SS
I_q (µA) (2-stage)	2.48	2.52	2.49	2.46	2.44
I_q (µA) (3-stage)	3.49	3.61	3.43	3.52	3.33
I_q (µA) (4-stage)	3.75	3.88	3.66	3.79	3.56

Additional simulations on the supply current have been carried out by changing the temperature in the range [0÷100] °C under the typical model of the transistor and 0.4-V supply. The achieved results shown in Table XCIV prove the supply current insensitivity to temperature variations. Indeed, the current variations over temperature are: 0.26 µA, 0.62 µA, and 0.61 µA for the 2-stage OTA, 3-stage OTA, and 4-stage OTA, respectively.

TABLE XCIII: Supply current I_q of the OTAs over temperature.

Temperature	0 °C	27 °C	60 °C	80 °C	100 °C
I_q (µA) (2-stage)	2.40	2.48	2.57	2.61	2.66
I_q (µA) (3-stage)	3.24	3.49	3.68	3.77	3.86
I_q (µA) (4-stage)	4.36	3.75	3.96	4.06	4.16

All the performance parameters of the proposed OTAs are summarized in Table XCV where additional simulated parameters like CMRR, PSRR, input noise, total harmonic distortion (THD) and maximum input current have been included.

TABLE XCIV: Simulated performance parameter of the proposed OTAs.

Parameter	Two-stage OTA	Three-stage OTA	Four-stage OTA
Supply Voltage (V_{DD}−V_{SS}) (V)	0.4	0.4	0.4
Supply current (µA)	2.48	3.49	3.75
Power dissipation (µW)	0.99	1.40	1.50
Offset maximum (mV)	4	0.58	0.2
ICMR	50 mV-350 mV	rail to rail	rail to rail
DC gain	58	71	88
GBW (kHz)	7	48	85
Phase Margin (deg)	89	81	69
Gain Margin (dB)	61	28	17
SR^+/SR^- (V/ms)	4.64/4.64	4.39/4.39	4.05/4.05
CMRR@DC (dB)	57.02	57.37	57.99
$PSRR^+$@DC (dB)	38.99	26.14	78.75
$PSRR^-$@DC (dB)	40.24	26.14	82.55
Input Ref. Noise @1kHz (nV/√Hz)	528.38	829.35	529.5
THD@1kHz,200mV_{p-p}input (%)	3.26	1.10	0.358
Max Input Current (nA)	5.11	5.11	5.11

3.4.6 Additional 65-nm OTAs Design

All the OTA configurations have been also simulated only at schematic level by using a 65-nm CMOS bulk technology produced by TSMC. The schematics of the OTAs in 65-nm are the same previously shown in Fig. 144, 145 and 146. Transistor sizes and device parameters are always the same as used for the 28-nm designs.

The achieved results for the 2-stage OTA, 3-stage OTA and 4-stage OTA have been compared to those achieved ones by using a 28-nm technology as shown in Table XCVI, XCVII and XCVIII, respectively. The portability across technology has been proved thanks to the achieved comparable results in terms of the main design parameters. Indeed, power consumption and frequency response parameters remain quite similar. A slight deviation occurs in terms of time response parameters which result in a symmetric SR^+/SR^- by using a 28-nm technology and in a non-symmetric SR^+/SR^- by using a 65-nm technology.

TABLE XCV: Simulated performance parameter of the proposed 2-stage OTA in two different technologies.

Parameter	Two-stage OTA (28-nm)	Two-stage OTA (65-nm)
Supply Voltage (V_{DD}−V_{SS}) (V)	0.4	0.4
Supply current (µA)	2.48	2.15
Power dissipation (µW)	0.99	0.86
Offset maximum (mV)	4	16
ICMR	50 mV-350 mV	50 mV–350 mV
DC gain	58	45
GBW (kHz)	7	8
Phase Margin (deg)	89	89
Gain Margin (dB)	61	58
SR^+/SR^- (V/ms)	4.64/4.64	6/2
CMRR@DC (dB)	57.02	57.5
$PSRR^+$@DC (dB)	38.99	26.14
$PSRR^-$@DC (dB)	40.24	26.14
Input Ref. Noise @1kHz (nV/√Hz)	528.38	829.35
THD@1kHz,200mV_{pp}input (%)	3.26	0.9
Max Input Current (nA)	5.11	0.220

TABLE XCVI: Simulated performance parameter of the proposed 3-stage OTA in two different technologies.

Parameter	Three-stage OTA (28-nm)	Three-stage OTA (65-nm)
Supply Voltage (V_{DD}−V_{SS}) (V)	0.4	0.4
Supply current (µA)	3.49	3.13
Power dissipation (µW)	1.40	1.25
Offset maximum (mV)	0.58	7
ICMR	rail to rail	rail to rail
DC gain	71	63
GBW (kHz)	48	35
Phase Margin (deg)	81	83
Gain Margin (dB)	28	34
SR^+/SR^- (V/ms)	4.39/4.39	16/7
CMRR@DC (dB)	57.37	57.5
$PSRR^+$@DC (dB)	26.14	26.14
$PSRR^-$@DC (dB)	26.14	26.14
Input Ref. Noise @1kHz (nV/√Hz)	829.35	829.35
THD@1kHz,200mV_{pp}input (%)	1.10	0.9
Max Input Current (nA)	5.11	0.220

TABLE XCVII: Simulated performance parameter of the proposed 4-stage OTA in two different technologies.

Parameter	Four-stage OTA (28-nm)	Four-stage OTA (65-nm)
Supply Voltage (V_{DD}−V_{SS}) (V)	0.4	0.4
Supply current (µA)	3.75	3.4
Power dissipation (µW)	1.50	1.36
Offset maximum (mV)	0.2	1.53
ICMR	rail to rail	rail to rail
DC gain	88	75
GBW (kHz)	85	75
Phase Margin (deg)	69	68
Gain Margin (dB)	17	17
SR^+/SR^- (V/ms)	4.05/4.05	5/6
CMRR@DC (dB)	57.99	57.5
$PSRR^+$@DC (dB)	78.75	26.14
$PSRR^-$@DC (dB)	82.55	26.14
Input Ref. Noise @1kHz (nV/√Hz)	529.5	829.35
THD@1kHz,200mV_{pp}input (%)	0.358	0.9
Max Input Current (nA)	5.11	0.220

3.4.7 Comparison With the State of Art

The performances achieved by the proposed OTAs can be compared to other low-power OTA proposed at the state of art [46] [47] [50] [53] - [56] [65] [88] [97] - [102], as shown in Table XCIX. The main OTA parameters such as DC gain, gain-bandwidth product (ω_{GBW}), Phase Margin (PM), Slew-Rate (SR), white noise, Common Mode Rejection ratio (CMRR) and input noise together with well-known Figures of Merit FOM_S and FOM_L (134)-(135) have been considered.

$$FOM_s = \frac{\omega_{GB}}{Power} C_L \quad (134)$$

$$FOM_L = \frac{SR}{Power} C_L \quad (135)$$

For a specified capacitance load, (134) and (135) show a trade-off between small-signal and large-signal parameters regarding the total power consumption.

The proposed OTA solution in its 4-stage configuration shows the highest DC gain which is 88 dB obtained through the smallest supply current 3.75 µA and smallest supply voltage of 0.4 V. A trade-off between small-signal performances and current consumption has been done, the lowest value of ω_{GBW} is therefore warranted to the lowest current consumption. Although, the ω_{GBW} is not the smallest achieved one, the small-signal FOM_S is the highest one due to the combination of the smallest power consumption together with the higher load capacitance. The large-signal performances have been compared through the large-signal FOM_L. Although the proposed OTAs falling between those solutions with higher FOM_L, higher values have been achieved by [99], [100] and [102] which shown higher average SR together with low supply current and small load capacitance.

To conclude, it can be noted that the proposed OTAs is the only one implemented with a 28-nm technology which allows to further reduce the supply voltage together with the current consumption. By adding stage of gain, the proposed OTAs allow to boost the DC gain from 58 dB to 88 dB by passing form the 2-stage to the 4-stage configuration. This higher value of DC gain together with 0.4-V operation and 3.75-nA consumption represent the best results proposed in literature. This is further confirmed by the small-signal performances compared in terms of FOM_S

which is the best achieved one in the state of art. Beside this, the proposed OTAs shown a sufficient phase margin in all the configuration without require an internal compensation. This is a great result for a multi-stage amplifier which usually requires a tricky compensation strategy to ensure the stability condition.

TABLE XCVIII: Performances comparison of the low-power OTA state of art.

Reference	Year	Technology (µm)	Supply Voltage (V)	Supply current (µA)	CL (pF)	DC gain (dB)	GBW (kHz)	PM (deg)	Average SR (V/ms)	CMRR (dB)	Input Noise @1MHz (nV/√Hz)	Simulated (S) / Measured (M)	FOMs [MHz·pF/mW]	FOML [V·pF/(µs· mW)]
[46]	2001	500	1	40	20	69	20000	57	500	--	--	M	1000	250
[47]	2002	2500	0.9	0.5	12	70	56	62	--	26 min.	--	M	149	--
[97]	2003	2500	0.8	10	18	50	1200	60	200	--	--	M	2700	450
[88]	2005	180	0.5	220	20	52	2500	--	2890	78	80	M	455	525
[50]	2007	350	0.6	0.916	15	69	11	65	14	74.5	290	M	300	382
[98]	2009	350	0.9	11	2.5	62	540	52	--	129	--	S	136	--
[53]	2013	350	1	197	15	88	11670	66	1950	40	300	M	889	148
[54]	2014	130	0.25	0.072	15	40	20	52	0.7	--	3300	M	1667	583
[55]	2015	65	0.5	366	3	46	38000	57	43000	35	938	M	623	705
			0.35	49	3	43	3600	56	5600	46	926	M	630	980
[56]	2016	180	0.7	36.3	20	57.5	3000	60	2800	19	100	M	2361	2204
[65]	2017	350	0.9	27	10	65	1000	60	2500	45	65	M	417	104
[99]	2020	180	0.3	0.042	30	64.7	3	52	4150	110	1600	M	7047	9880
[100]	2021	180	0.5	0.091	15	78	7.5	59	8.6	113.8	650@1kHz	M	2473	2835
[101]	2022	130	0.3	2.36	100	15	--	11	--	63	722@1kHz	M	915	--
[102]	2022	180	0.4	0.06	30	60	7	60.2	79	85.4	310@1kHz	M	8750	98750
Proposed OTA (2-stage)	2023	28	0.4	2.48	500	58	7	89	4.64	57.02	528.38@1kHz	S	3535	2343
Proposed OTA (3-stage)	2023	28	0.4	3.49	500	71	48	81	4.39	57.37	829.35@1kHz	S	17143	1568
Proposed OTA (4-stage)	2023	28	0.4	3.75	500	88	85	69	4.05	57.99	529.5@1kHz	S	28333	1350

Conclusions

The rapid growth of low-power systems like portable and wearable medical electronic devices, smartphones, wireless smart systems, wireless sensor networks, wearable health care monitoring devices and so on have led modern systems on chip (SoC) to contain more and more functionalities which have to be smarter than ever before. Due to the limited energy storage of primary or secondary batteries, low-power design techniques are mandatory to significantly reduce power consumption. However, ultra-low voltage and ultra-low current analog and mixed-signal IC design, especially in nanometer technology, represents a great challenge.

Limitations due to the low-power operation in analog design has been analyzed together with the most-used low-voltage low-current analog design techniques which allow to overcome these restrictions. After that, the aim of this research work has been satisfied through the proposal of two fundamental low-power CMOS analog building blocks: (1) voltage references and (2) Operational Transconductance Amplifiers (OTAs). An accurate analysis of these circuit topologies has been carried out also validated by exhaustive schematic and post-layout simulations and whenever possible experimental results. Additionally, a needed comparison with the stat of art in their field has been made proving the goal of this research.

A first solution of CMOS resistor-less nano-power voltage reference with trimming strategy has been proposed, designed, and measured. The proposed solution represents the only one in literature able to cover both the widest range of supply voltage and temperature which are [1.2 ÷ 5] V and [–40÷125] °C, respectively. A measured reference voltage of 348 mV has been achieved with only 25-nA of consumption. The greatest goal of the proposed solution besides of having reached a small value of Line Sensitivity (LS) which is 0.14 %/V with a supply voltage variation of 1.81 V.

The proposed CMOS resistor-less nano-power voltage reference with trimming strategy has been filled with an analog output voltage buffer with ultra-low current consumption. The proposed circuit has been expressly designed to complement the ultra-low-current reference voltage circuit presented with the main goal to preserver all the performances of ultra-low current voltage reference related to it. Experimental results prove that the reference voltage and the LS are maintained equal to 348 mV and 0.14 %/V, respectively. The additional goal of the proposed design is given by the measured supply current consumption which is always stable by changing the supply current showing a value around 45 nA by considering the overall circuit.

Additionally, a 28-nm CMOS resistor-less voltage reference with process corner compensation for biomedical application has been proposed, designed, and measured. The main novelty of the proposed topology besides in the proposed trimming strategy in the active load which allows to reduce by a factor of 10 the reference voltage variation across corners than ones achieved without trimming strategy.

A 50pF-400pF 0.4-V subthreshold bulk-driven rail-to-rail CMOS Operational Transconductance Amplifier has been proposed. The adoption of the low supply of 0.4-V together with small consumption of 1.58-µA give rise a small value of power consumption which is one of the advantages of the proposed OTA. The combination between low power consumption together with the small-signal performances give rise the best FOM_S at the state of art. Beside this, the large signal performances have been compared through the FOM_L where the proposed OTA reach again one of the best results.

At the end, a four-stage bulk-driven super class AB operational transconductance amplifier (OTA) has been proposed. The proposed solution is based on a modular topology in which additional stage of gain based on the same working principle can be added to the first one to boost the DC gain. The proposed OTAs allow to boost the DC gain from 58 dB to 88 dB by passing form the 2-stage

to the 4-stage configuration. This higher value of DC gain together with 0.4-V operation and 3.75-nA consumption represent the best results proposed in literature. This is further confirmed by the small-signal performances compared in terms of FOMs which is the best achieved one in the state of art. Beside this, the proposed OTAs shown a sufficient phase margin in all the configuration without require an internal compensation.

This research work also touched the design of other analog fundamental building blocks which are constituted by a current-controlled ring oscillator and by an inverter-based comparator. Although they do not represent the main part of this research work, they contribute to the state of the art in the field of analog low-power design.

Appendix

Additional Ultra-low Power CMOS Building Blocks

This research work also touched the design of other analog fundamental building blocks which are constituted by a current-controlled ring oscillator and by an inverter-based comparator. Although they do not represent the main part of this research work, they contribute to the state of the art in the field of analog low-power design. For this reason, this chapter contains only the abstract of these two already published works and at the end of this dissertation the full text of these papers have been included.

4.1 A 0.5 V Sub-Threshold CMOS Current-Controlled Ring Oscillator for IoT and Implantable Devices [103]

A current-controlled CMOS ring oscillator topology, which exploits the bulk voltages of the inverter stages as control terminals to tune the oscillation frequency, is proposed and analyzed. The solution can be adopted in sub-1 V applications, as it exploits MOSFETS in the subthreshold regime. Oscillators made up of 3, 5, and 7 stages designed in a standard 28-nm technology and supplied by 0.5 V, were simulated. By exploiting a programmable capacitor array, it allows a very large range of oscillation frequencies to be set, from 1 MHz to about 1 GHz, with a limited current consumption. Considering, for example, the five-stage topology, a nominal oscillation frequency of 516 MHz is obtained with an average power dissipation of about 29 μW. The solution provides a tuneable oscillation frequency, which can be adjusted from 360 to 640 MHz by controlling the bias current with a sensitivity of 0.43 MHz/nA.

4.2 A 0.5-V 28-nm CMOS Inverter-Based Comparator with Threshold Voltage Control [104]

This paper proposes a novel solution for CMOS inverter-based comparators with threshold voltage control. The solution was simulated in a 28-nm bulk technology under 0.5- V supply. Extensive simulation results show that a reasonable accuracy in the threshold voltage setting is achieved regardless PVT variations. Outperformed average current consumption of about 125 nA, excluding reference circuitry, and rise/fall time of 7.9 μs suggest wide field of applications for the proposed circuit, ranging from A/D converters to sensors for biomedical applications.

Publications

A section of this research activity performed in the framework of low-power analog circuit design has resulted in six publication which are listed below.

- Ballo, A.; Grasso, A.D.; Pennisi, S.; Venezia, C. High-Frequency Low-Current Second-Order Bandpass Active Filter Topology and Its Design in 28-nm FD-SOI CMOS. J. Low Power Electron. Appl. 2020, 10, 27.
- A. D. Grasso, S. Pennisi and C. Venezia, "28-nm CMOS Resistor-Less Voltage Reference with Process Corner Compensation," 2021 28th IEEE International Conference on Electronics, Circuits, and Systems (ICECS), 2021, pp. 1-5.
- Ballo, A.; Pennisi, S.; Scotti, G.; Venezia, C. A 0.5 V Sub-Threshold CMOS Current-Controlled Ring Oscillator for IoT and Implantable Devices. J. Low Power Electron. Appl. 2022, 12, 16.
- C. Venezia, A. Ballo and S. Pennisi, "A 0.5-V 28-nm CMOS Inverter-Based Comparator with Threshold Voltage Control," 2022 17th Conference on Ph.D Research in Microelectronics and Electronics (PRIME), 2022, pp. 77-80.
- C. Venezia, A. Rizzo and S. Pennisi, "15 nA CMOS Analog Voltage Buffer Insensitive to PVT Variations," 2023 18th Conference on Ph.D Research in Microelectronics and Electronics (PRIME), Valencia, Spain, 2023, pp. 73-76, doi: 10.1109/PRIME58259.2023.10161803.
- Grasso, A.D.; Pennisi, S.; Venezia, C. A Survey of Ultra-Low-Power Amplifiers for Internet of Things Nodes. Electronics 2023, 12, 4361. https://doi.org/10.3390/electronics12204361.

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