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RF Harvesting System for Remotely Powered Wireless Sensor Nodes

Ph.D. Thesis

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Table of Contents

List of Figures

Chapter I

Chapter II

Chapter III

Chapter IV

Chapter V

Chapter VI

List of Tables

Chapter I

Chapter IV

Chapter VI

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Leandro Grasso

Abstract

Modern applications such as supply chain management and the Internet of Things (IoT) have addressed research efforts on improving the power efficiency in low power embedded devices. On the other hand, recent advances on ultra-low-power systems (1-100 μW) have enabled battery replacement with energy harvesters (or scavengers), which rely on external energy sources, such as vibration, solar, thermal, or the RF carrier of a power transmitter. Energy harvesting systems lead to further reduce complexity and costs for periodic maintenance. Among the harvesting approaches, RF solutions show the clear advantage of providing full controllable operation regardless environmental conditions. Unfortunately, propagation loss and relatively low harvester sensitivity greatly affect the operating distance of RF harvesting systems.

To this purpose, several circuit solutions have been recently proposed to increase RF-DC power conversion efficiency and input sensitivity, by exploiting Dickson-based charge pumps or CMOS differential-drive rectifiers. Although the power-up voltage of both topologies is affected by the transistor threshold voltage V_t, Dickson charge pumps generally exhibit lower efficiency because also the voltage drop across the transistor drain-source terminals must exceed V_t. To overcome this limitation, several approaches have been proposed, which perform threshold-voltage compensation. On the other hand, CMOS differential-drive rectifiers have an inherent threshold-voltage compensation topology that made

these solutions widely used in the last decade. Nevertheless, different techniques have been suggested to further enhance rectifier efficiency and sensitivity by reducing the reverse current in the rectifying stages, which is the main cause of efficiency limitation.

Although the differential-drive rectifier is a consolidate state-of-the-art solution, it is still difficult to draw up a complete design methodology, which clearly explains how to properly set design parameters to optimize performance for a given specification. Moreover, rectifiers cannot be designed without jointly consider the antenna. Indeed, the optimal operating point for the rectifier can result in a non-optimal operating point for the overall system, thus precluding best system efficiency to be achieved.

In this work, an effective co-design methodology for a harvesting system based on a CMOS differential-drive rectifier and an inductive coupled loop (ICL) antenna is discussed. It allows the overall system efficiency to be maximized for a given load and bandwidth specifications, which in turn means enhancing sensitivity as well. Moreover, the proposed co-design methodology was applied to an improved rectifier topology, which includes a body-voltage control strategy. It takes advantage of the voltage waveforms inherently generated by the circuit itself to dynamically vary the transistor threshold voltage. Finally, a relevant effort in terms of an accurate characterization of the harvesting system was paid, with a dedicated measurement set-up able to verify power efficiency and input impedance of antenna and rectifier.

This dissertation is organized as follows. In chapter I, after a brief overview about WSNs and their applications, main energy harvestings approach are

discussed. In particular, RF harvesting system is described along with related design constraints. The proposed rectifier and antenna are presented in chapter II and III, respectively. Then, an effective co-design methodology for RF harvesting systems is drawn up in chapter IV. Chapter V and VI report the measurement methods properly reshaped and the experimental results, respectively. Finally, conclusions are given in the last section.

This project was carried out within the RF-ADC (*Radio Frequency Advanced Design Center*), a joint research group supported by the University of Catania and *STMicroelectronics*.

Chapter I

Energy harvesting for wireless sensor networks

1.1 Wireless sensor networks

Wireless sensor networks (WSNs) mainly consist of a *base station* that communicates with several *sensor nodes* through a radio link, as shown in Fig. 1.1. Data is collected within each node, which re-transmits the processed information to the base station directly or via other nodes [1].

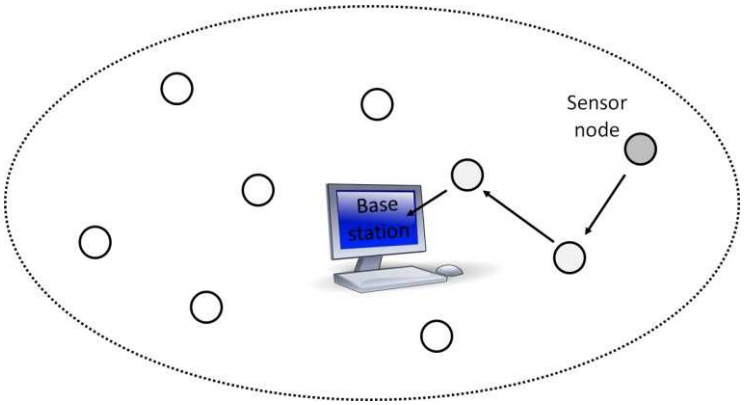

Fig. 1.1. Scheme of a generic wireless sensor network.

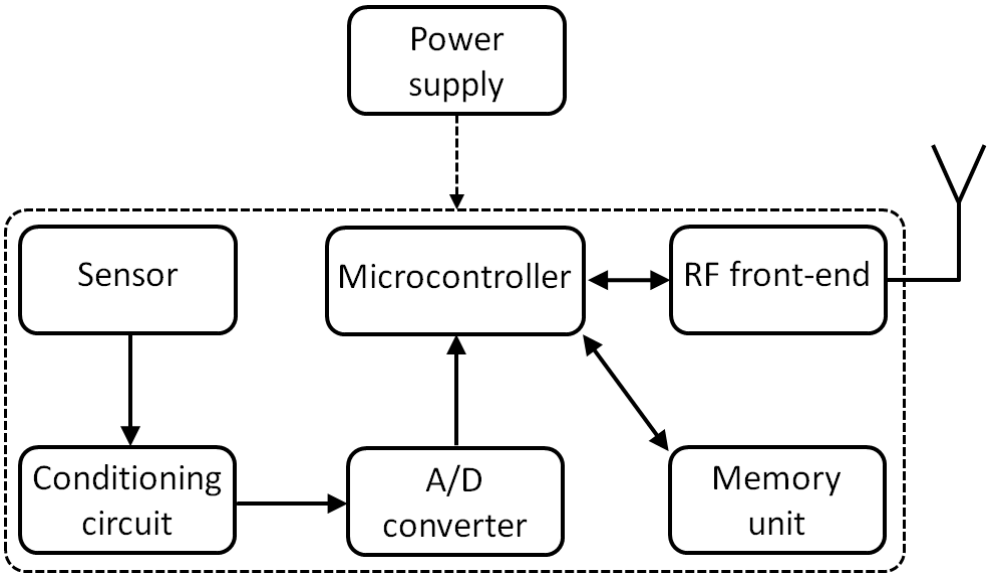

Fig. 1.2. Block diagram of a generic wireless sensor node.

Fig. 1.2 shows the block diagram of a generic wireless sensor node. As a first step, the *sensor* converts physical quantities into electric signals. Then, the signal is properly processed by an optional *conditioning circuitry* and converted into a digital signal by the *analog-to-digital converter*. The resulting digital signal goes to the *microcontroller* that manages the communications protocol, by interacting with the *RF front-end*. The latter processes the radio frequency signal coming from the antenna and can also perform the transmitting function. This block requires the largest amount of power, thus a duty-cycled operation is usually implemented [2]. A *memory unit* can be added to the system to store data from the base station or in correspondence of a particular event. Finally, the *power supply* circuitry manages the energy usually coming from a battery to supply the whole system. Although the battery energy density with respect to volume and weight has been substantially improved in the last decade, battery lifetime remains a crucial aspect within the increasingly smaller WSN devices.

1.1.1 Applications

Nowadays, WSNs are adopted in different areas, such as health-care, lifestyle, automotive, smart buildings, active RFID tags, etc. These devices mainly suffer from limited lifetime, because of their substantial power requirement, which is shown in Fig. 1.3.

Fig. 1.3. Power requirements and lifetime of typical WSN products.

Unfortunately, long lifetime does not match up with the small form factor of these devices, since large batteries would usually be required. Then, energy harvesting approach has been adopted in recent years, by taking advantage of different environmental energy sources. This leads to increase node lifetime and make WSNs autonomous, thus cutting down costs related to supervision, configurations or maintenance. Some device can be made even completely autonomous by replacing the battery with the harvesting system, as happens for passive RFID tags [3]. These tags take advantage of the electromagnetic energy

coming from the reader to wake up the circuitry, thus receiving data and transmitting the information required (Fig. 1.4).

Fig. 1.4. Passive RFID tag and reader.

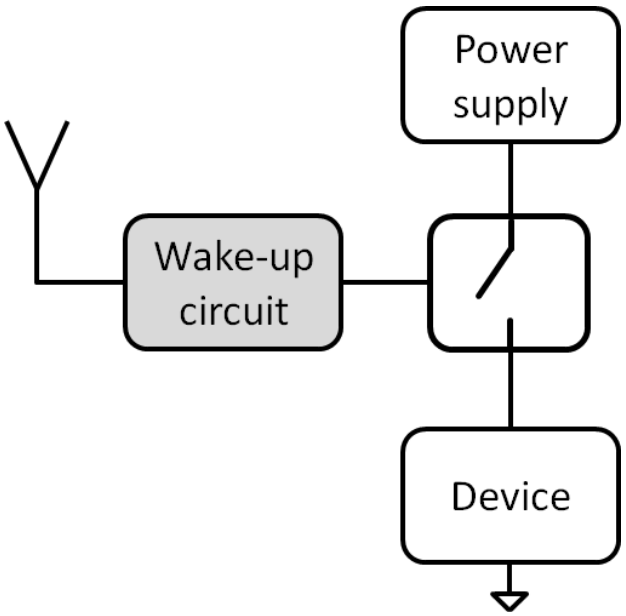

Fig. 1.5. RF harvesting for remotely-powered switch.

The RF circuitry can renounce transmitting functions, thus behaving as *wake-up circuits* only. As an example, among smart buildings applications, these circuits can be implemented to simply receive a code and then turning-on a remotely-powered switch that enable a generic device (Fig. 1.5) [4]. This results in cutting down power consumption related to stand-by mode in modern devices.

1.2 Energy harvesting

As previously mentioned, several environmental energy source can be taken into account to increase node lifetime of wireless sensor nodes, such as vibrational, thermal, photovoltaic, and RF energy.

1.2.1 Vibration harvesting

Vibration harvesting approach consists in adopting transduction mechanisms that convert motion to electric signals. These transducers are usually electrostatic, piezoelectric, or electromagnetic. Electrostatic transducers rely on the movement of one electrode of a polarized capacitor, thus causing a voltage across the capacitor with a resulting current flow to the load. In piezoelectric transducers, the voltage is generated by deformation of a piezoelectric capacitor. Electromagnetic transducers, instead, consists in the relative motion of a magnetic mass with respect to a coil. The resulting changing in the magnetic flux generates an ac voltage across the coil.

Vibration harvesting has been widely used nowadays. In particular, bi-stable and even tri-stable oscillators allow to scavenge energy from broadband, weak, random vibrations, thus overcoming the lower efficiency of traditional linear resonators (see Fig. 1.6) [5].

Unfortunately, this approach obviously needs particular environmental conditions or specific applications such as automotive, sport-related, etc.

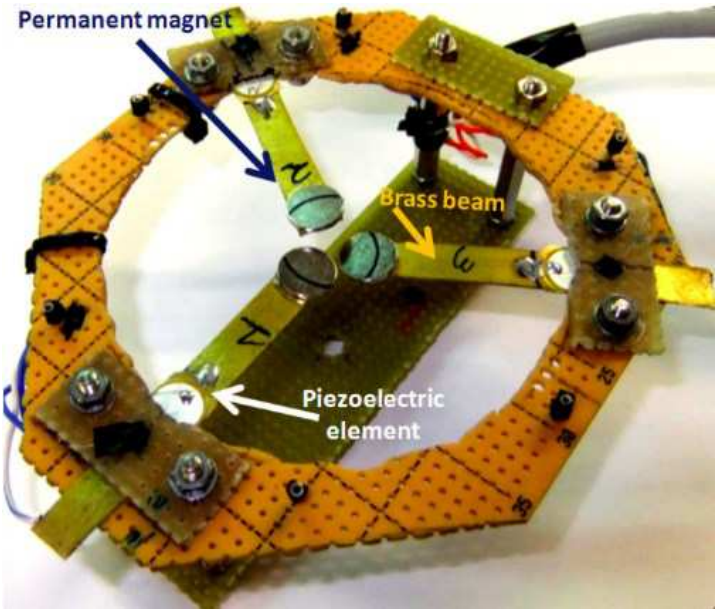

Fig. 1.6. Experimental prototype of tri-stable magnetically-coupled cantilevers having piezoceramic elements as active materials [5].

1.2.2 Thermal harvesting

Thermal harvesters are based on the *Seebeck effect*. This phenomenon produces a voltage difference between two dissimilar electrical conductors or semiconductors kept at different temperatures.

Thermoelectric scavengers were the first ones to appear on the market, since it is easy to fabricate these devices with solid-state technology. A thermoelectric microsystem is shown in Fig. 1.7, whose junctions at the bottom are heated to produce an electrical power current through the Seebeck effect. A large number of junctions can be connected in series to increase the operating voltage.

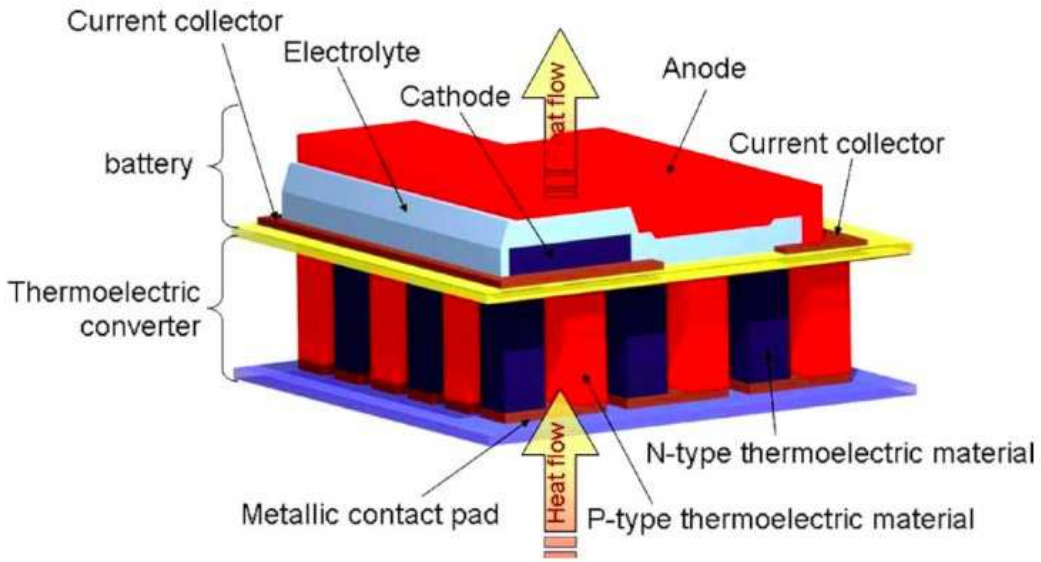

Fig. 1.7. Artwork of a thermoelectric microsystem [6].

Thermal approach is not widely used within harvesting applications, since it relies on the presence of heat sources.

1.2.3 Photovoltaic harvesting

Photovoltaic harvesting systems rely on *photovoltaic* (PV) *cells*, which convert incoming photons into electricity. Recent efforts move on improving PV cell design within indoor application, thus facing the different spectral composition of the light and the lower level of illumination (10-100 $\mu W/cm^2$).

A generic photovoltaic harvesting system is shown in Fig. 1.8. The power conditioning circuitry plays an important role within this system. In fact, it draws dc current from the PC cell and efficiently manages both energy storage and power delivering to the load [7].

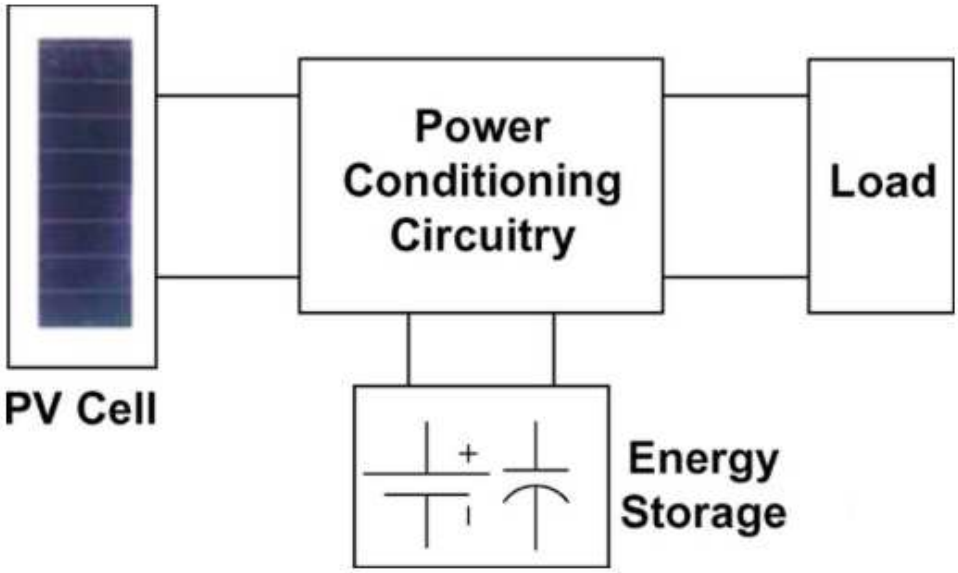

Fig. 1.8. Scheme of a generic photovoltaic harvesting system [7].

Outdoor photovoltaic harvesting is strongly affected by environmental and time conditions. On the other hand, indoor PV systems overcome the problem related to the environmental conditions but suffer from low efficiency and an artificial light source is also needed.

1.2.4 Radio-frequency harvesting

RF harvesting takes advantage of the incoming electromagnetic radiation from ambient or dedicated sources. Ambient sources relate to public

telecommunication services, such as GSM, WLAN, Wi-Fi, TV and military broadcasting [9]. That means having a constantly available power source, which makes RF harvesting systems widely used nowadays. Dedicated RF sources have been also exploited, e.g. RFID systems, but their power levels have to be set according to international regulations. In fact, although no licenses are needed from the telecommunication regulatory authorities, strict regulations regard the choice of operating frequencies, output powers, spurious emissions, etc.

Table 1.1. Frequency band restrictions for RFID applications.

	Frequency Band	Power	Duty Cycle / Tx type	Channel Spacing / BW	Region
a	2446-2454 MHz	500mW EIRP 4W EIRP	Up to 100% ≤ 15%	No spacing	Europe[a]
b1	865.0-865.6 MHz	100mW ERP		200kHz	Europe
b2	865.6-867.6 MHz	2W ERP		200kHz	Europe
b3	867.6-868.0 MHz	500mW ERP		200kHz	Europe
	902-928 MHz	4W EIRP	FH (≥50 channels) or DSSS		USA Canada
	2400-2483.5 MHz	4W EIRP	FH ((≥75 channels) or DSSS		USA Canada
	2400-2483.5 MHz	10mW EIRP		1MHz BW	Japan Korea

EIRP stands for Effective Isotropic Radiated Power and is the transmit power multiplied by the gain of the transmit antenna. ERP is Effective Radiated Power. EIRP is 1.64 times ERP. FH stands for Frequency Hopping. DSSS stands for Direct Sequence Spread Spectrum and BW indicates Band Width.

[a] Power levels above 500mW are restricted to use inside the boundaries of a building and the duty cycle of all transmissions shall in this case be ≤ 15% in any 200ms period (30ms on / 170ms off).

The *industrial, scientific and medical* (ISM) *bands*, have been defined by the *International Telecommunication Union Radiocommunication Sector* (ITU-R), in order to develop standards for radio-communication systems [11]. Frequency bands regulations for RFIDs are shown in Table 1.1 [12].

1.3 RF harvesting systems

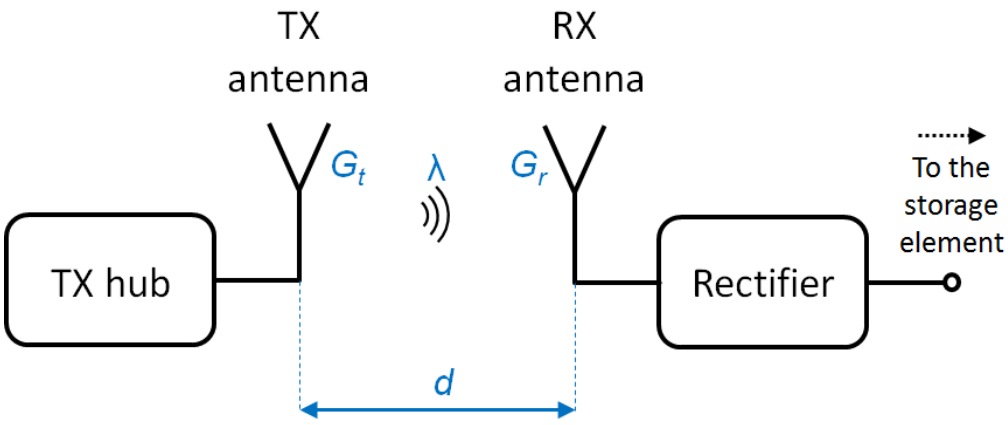

Fig. 1.9. Power propagation scheme between wireless sensor nodes .

A transmitting-receiving pair is shown in Fig. 1.9. By increasing the distance d between nodes, the output power P_t to the transmitting antenna suffers from higher power losses. This results in a lower power P_{AV} available at the output terminals of the receiving antenna, as given by the *Friis equation* [13]

$$P_{AV} = P_t G_t G_r \left(\frac{\lambda}{4\pi}\right)^2 \frac{1}{d^n} \tag{1.1}$$

where G_t and G_r are the gains of the transmitting and receiving antenna, respectively, λ is the wavelength of the transmitting signal and n is the path loss exponent. The latter goes from 1.6 to 3.3 depending on the propagation channel condition. In particular, n is equal to 2 when the nodes are ideally set into the vacuum.

1.3.1 Rectifier

Once an electric signal is available at the output terminals of the receiving antenna, a circuit is needed to perform the following functions:

- rectifying the ac signal to dc power
- boosting the dc output voltage to a level required by the application

The latter can be simply obtained by exploiting multi-stage implementations of typical RF envelop detectors, as happens for charge pump circuits used within VLSI design. However, transistor threshold voltage V_t becomes comparable to the rectifier input voltage within low-power applications, thus resulting in lowering the rectifier efficiency.

The simplest RF rectifier is the half-wave one, which is shown in Fig. 1.10. During the positive half wave of the input signal v_{in}, diode D_1 conducts, thus producing a positive voltage across the capacitor C_1. On the other hand, during the negative half wave of v_{in}, no current flows through diode D_1, and the charge into C_1 is delivered to the load. This results in producing a dc voltage V_{out} across C_1.

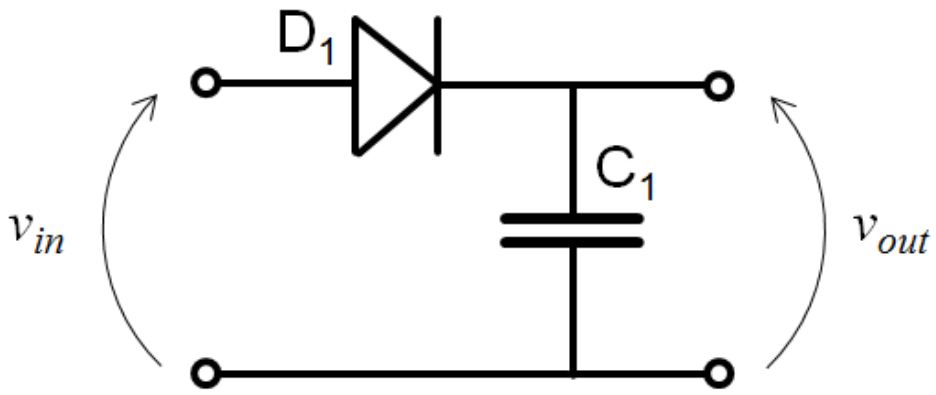

Fig. 1.10.Schematic of the half-wave rectifier.

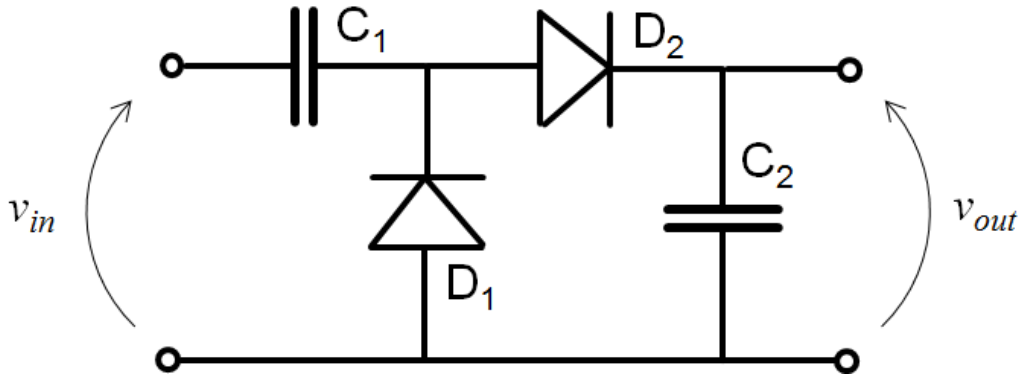

Fig. 1.11. Schematic of the full-wave rectifier.

Since the circuit in Fig. 1.10 only performs a half-wave rectification, the full-wave counterpart is generally preferred. By referring to Fig. 1.11, the additional two elements D_2 and C_2 provide a full-wave rectification, thus resulting in a more efficient power delivering.

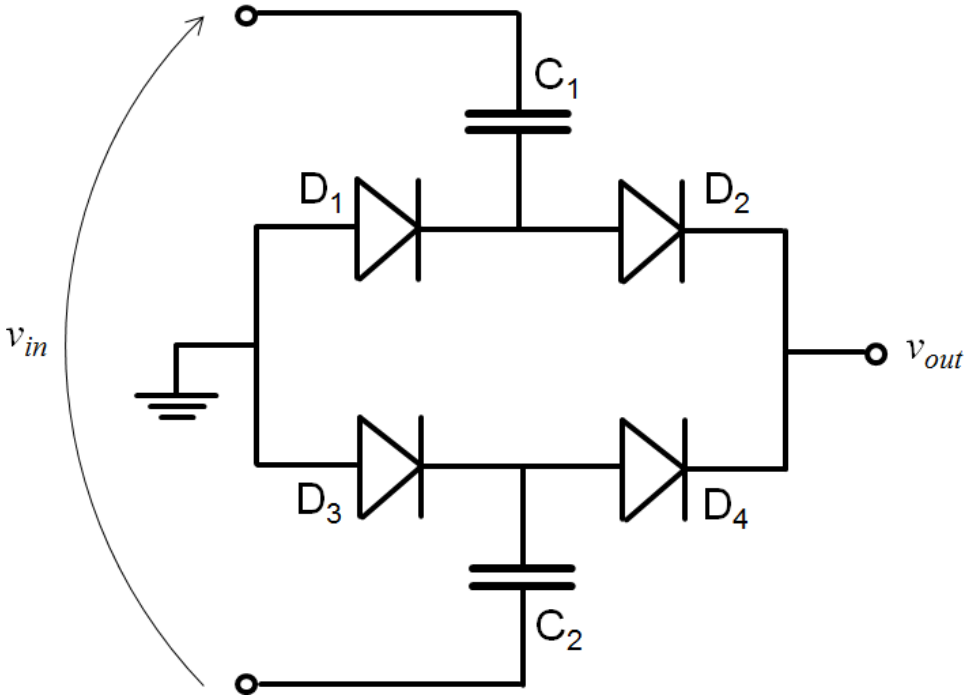

Fig. 1.12. Schematic of the Graetz Bridge.

Another improvement can be achieved by using the *Graetz Bridge* in Fig. 1.12. In fact, this circuit is able to deliver 2-times the output voltage of the previous rectifiers.

Diode connected transistors were introduced to substitute diodes in the rectifying circuits previously exposed. A MNOS arrangement of the full-wave rectifier is known as Dickson charge pump [14]. The CMOS counterpart based on the Dickson topology is shown, instead, in Fig. 1.13.

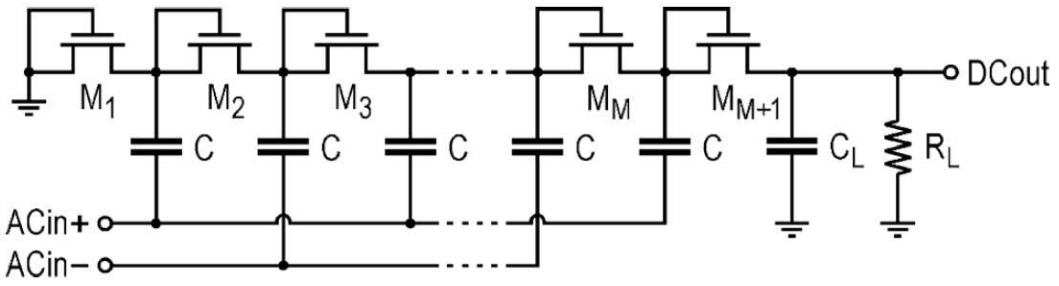

Fig. 1.13. Schematic of a Dickson multi-stage rectifier [15].

Although it has been widely used in the last decades, Dickson-based topologies generally exhibit lower power conversion efficiency due to the voltage drop across the rectifying transistors that must exceeds the threshold voltage, V_t. To this purpose, several compensation techniques have been developed [15]-[17]. In particular, in [15] each transistor gate is connected to proper nodes along the rectifying chain to compensate the threshold voltage drop, thus enhancing the efficiency.

On the other hand, CMOS differential-drive rectifier has been also proposed in the last decade for RF harvester implementations, since an inherent threshold-voltage compensation structure is performed by its cross-coupled connection structure. It consists in a CMOS arrangement based on the Graetz Bridge, as shown in Fig. 1.15.

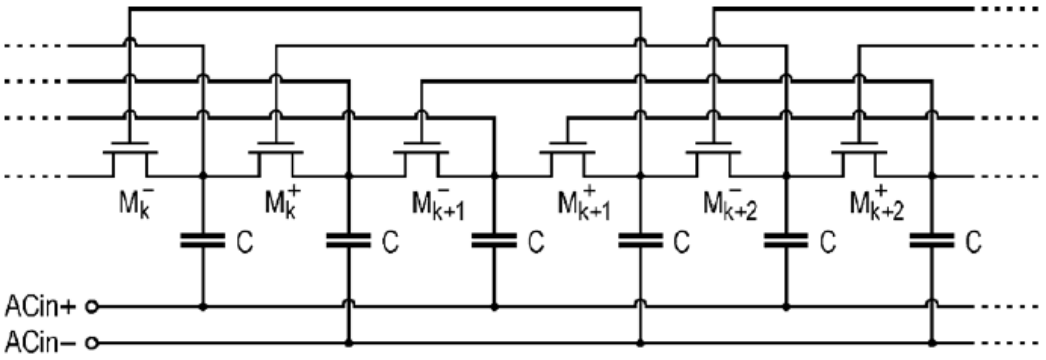

Fig. 1.14. Schematic of the Dickson-based self compensation topology proposed in [15].

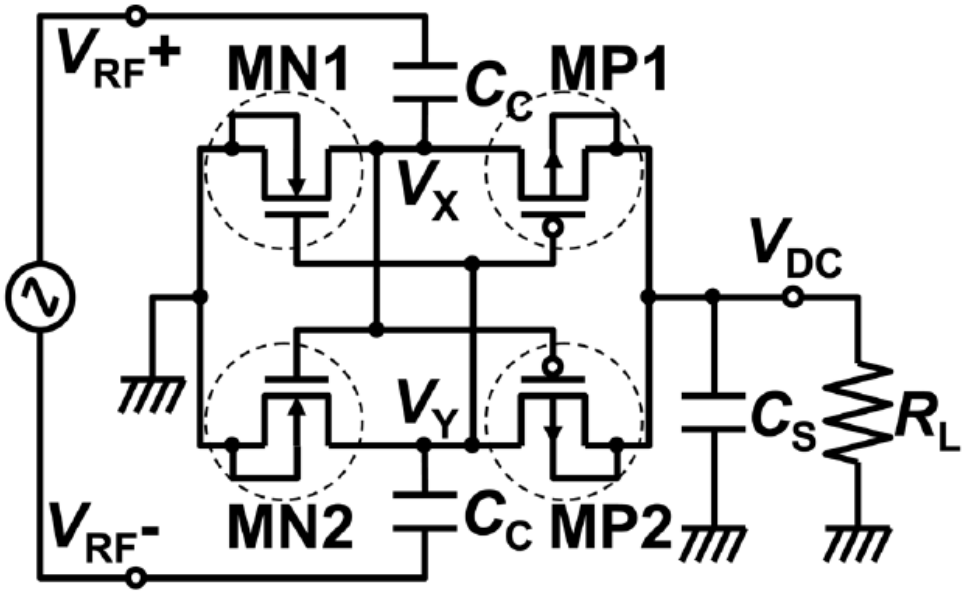

Fig. 1.15. Schematic of the CMOS differential-drive rectifier [18].

However, it suffers from a reverse conduction that affects both efficiency and sensitivity. Thus, several compensation strategies have been proposed to further improve performance of the differential-drive rectifier. In [19], an additional PMOS transistor was added to each main PMOS transistor to enhance the DC extraction capability, as shown in Fig. 1.16.

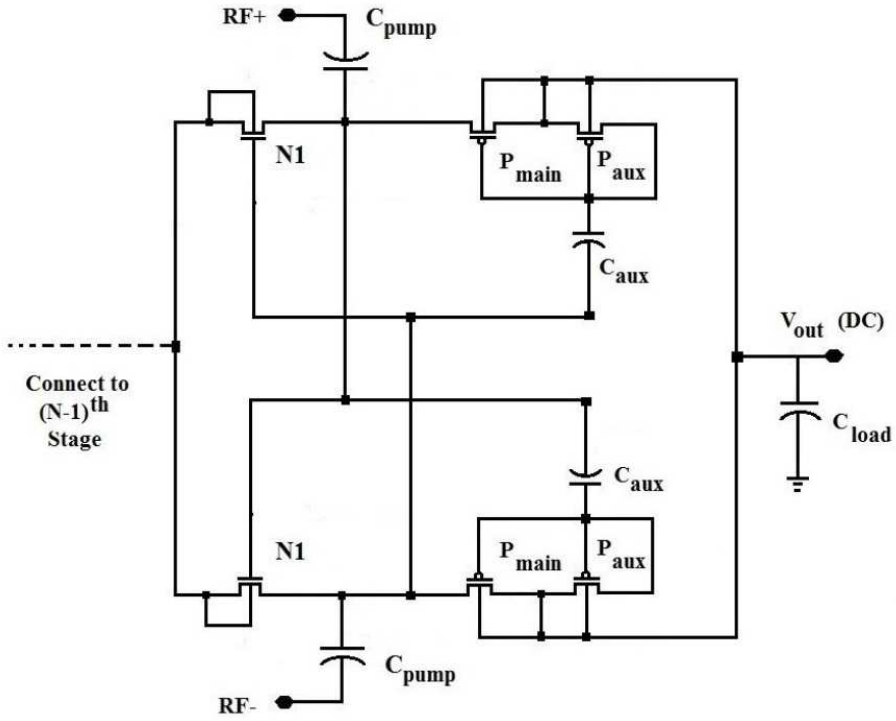

Fig. 1.16. Schematic of the CMOS differential-drive rectifier with auxiliary PMOS [19].

An auxiliary stage was used in [20], instead, to properly shift the gate voltage waveform of the basic cell. However, these solutions rely on additional active components, thus resulting effective only for relatively high input power levels. In [21], zero threshold-voltage transistors were used in a complementary CMOS differential-drive rectifier to enhance the efficiency, but silicon-on-sapphire (SOS) CMOS technology was used.

1.3.2 Antenna

Most of planar antennas for UHF tags are commonly designed as modified dipoles and printed on PCB substrates. Two main categories have been exploited in the last decades: T-match and inductively coupled loop (ICL) antennas [22].

T-match antennas consists in two dipoles connected together, as shown in Fig. 1.17 [23]. Although this is a highly efficient antenna, high values of input resistance are generally found, thus resulting inadequate for matching high-impedance-phase-angle chips, i.e. chips with high parallel input resistance and low capacitance.

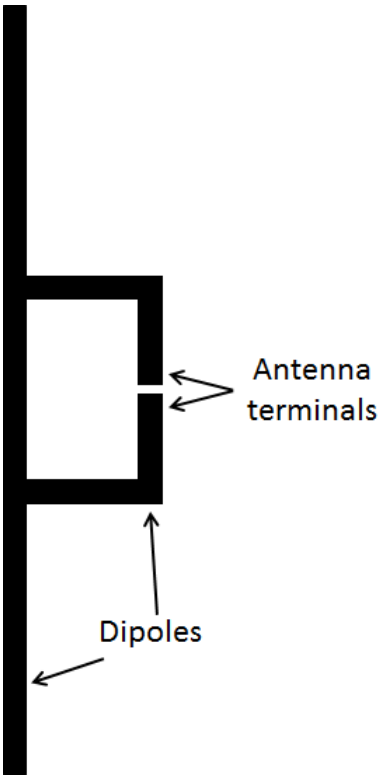

Fig. 1.17. Layout of a generic T-match antenna.

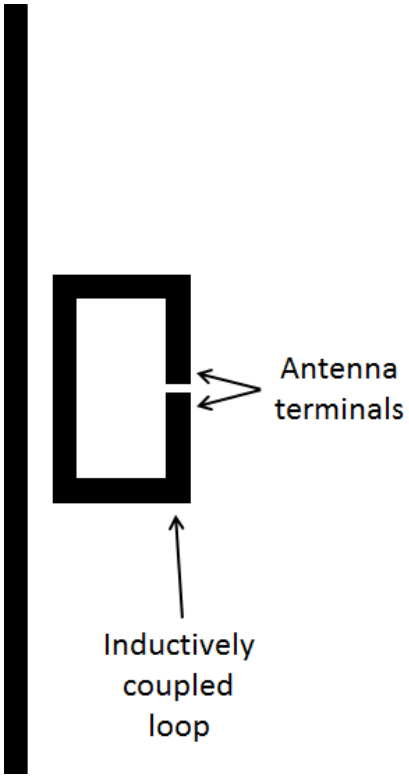

Fig. 1.18. Layout of a generic inductively couple loop (ICL) antenna.

ICL antenna, whose layout is shown in Fig. 1.18, is usually preferred due to its inductive coupling that allows a high equivalent inductance to be performed, while maintaining a low series resistance [24]. This feature is very suitable for impedance matching with typical integrated RF rectifiers for harvesting systems.

1.3.3 Design constraints

Although RF harvesting systems have become very popular in the last years, its denomination is not always correctly defined. Indeed, the antenna is often seen as an appendix within the design flow, although the harvesting function is performed by antenna and rectifier working together. Of course, the rectifier is

predominant in terms of design complexity, but accounting for the interaction between antenna and rectifier is mandatory for achieving the best performance of the overall harvesting system.

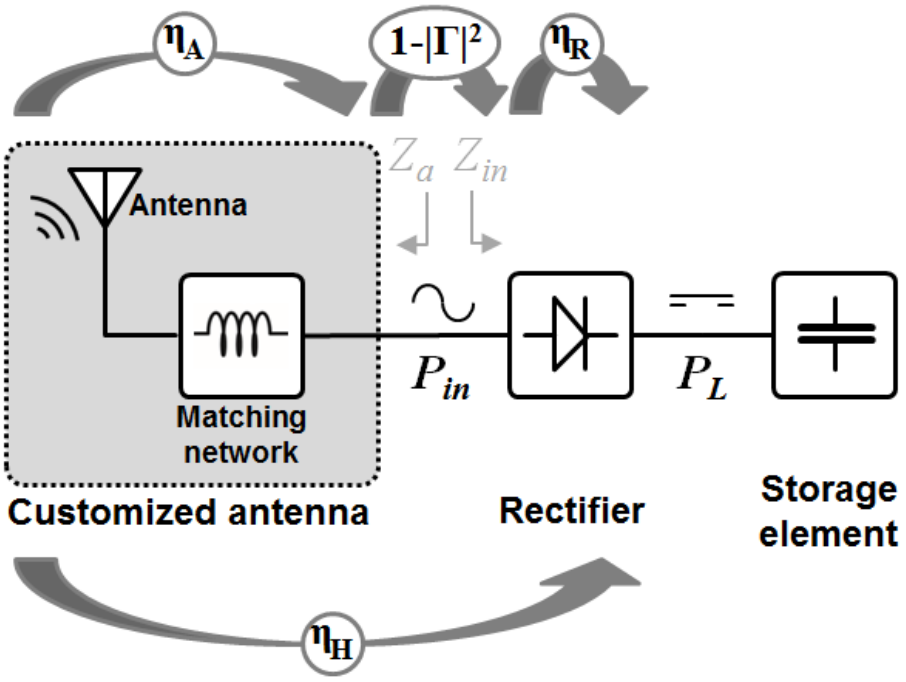

Fig. 1.19. Simplified representation of an RF harvesting system.

Fig. 1.19 shows a simplified block diagram of a generic RF harvesting system. The electromagnetic incident power is converted by the antenna in electric ac power P_{in} and made available to the rectifier input terminals. The rectifier converts the ac power into a dc power P_L and delivers it to the storage element, which can be a rechargeable battery or a capacitor. To minimize power losses, a customized antenna is preferred, which inherently performs impedance matching with the rectifier input impedance. The efficiency of the overall harvesting system η_H is defined as

$$\eta_H = P_L / P_{AV} \tag{1.2}$$

where P_{AV} is the available power assuming an ideally lossless and matched antenna. By considering non-ideal antenna and matching condition, input power P_{in} is given by

$$P_{in} = \eta_A \left(1 - |\Gamma|^2\right) P_{AV} \tag{1.3}$$

where η_A is the antenna efficiency and Γ is the reflection coefficient at the rectifier/antenna interface. Substituting (1.3) in (1.2) and defining the rectifier efficiency, η_R, as

$$\eta_R = P_L / P_{in} \tag{1.4}$$

the overall system efficiency becomes

$$\eta_H = \eta_A \left(1 - |\Gamma|^2\right) \eta_R \tag{1.5}$$

Since P_L is imposed by the application, a higher η_H translates into a lower requirement of P_{av}, which means better sensitivity.

A simplified impedance representation at the antenna and rectifier interface is shown in Fig. 1.20. The antenna is modelled as a first-order network, where resistance R_a and inductance L_a account for radiation/loss and reactance, respectively. The rectifier is instead represented by parallel resistance R_{in} and capacitance C_{in}. This model is valid for a narrow band approximation of typical ultra-high-frequency (UHF) applications around the operating frequency.

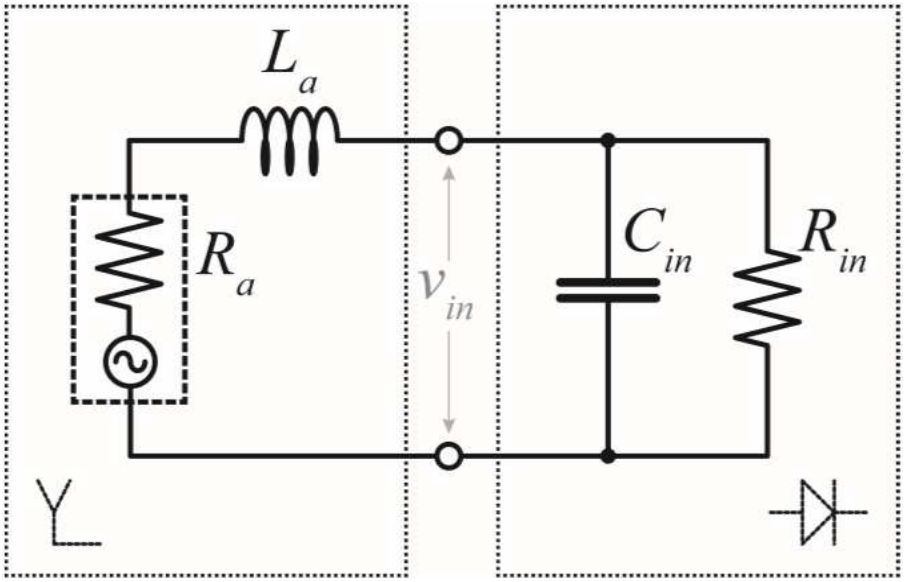

Fig. 1.20. Simplified impedance model of a RF harvesting system.

The input power, P_{in}, can be expressed as

$$P_{in} = \frac{V_{in}^{\ 2}}{2R_{in}} \tag{1.6}$$

where V_{in} is the voltage amplitude at the rectifier input terminals. Since the rectifier has a power-up threshold voltage, V_{in} cannot be lowered at will. Once the minimum V_{in} is set, a better sensitivity can be achieved by increasing R_{in}.

On the other hand, the application bandwidth B imposes an additional constraint on the rectifier input impedance through the quality factor, Q_L, which is given by

$$Q_L = 2\pi f_0 R_{in} C_{in} \tag{1.7}$$

where f_0 is the operating frequency. To this purpose, the Bode-Fano theory defines a maximum allowable value, $Q_{L,max}$, for the quality factor that is [7]

$$Q_{L,\max} = \frac{f_0}{B} \frac{2}{\sqrt{1/|\Gamma|^2 - 1}} \tag{1.8}$$

As far as the antenna is concerned, the constraint on the maximum substrate area greatly limits equivalent inductance L_a that has to match the rectifier input capacitance. Fortunately, several antenna design techniques can be exploited to reduce the antenna size, while providing the required input reactance.

All the previous aspects need an accurate design strategy, which is capable of efficiently meeting the specifications of the overall harvesting system.

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Chapter II

CMOS differential-drive rectifier

2.1 Operating principle

The operating principle of the single-stage CMOS differential-drive rectifier in Fig. 2.1 can be explained as follows [1]. Assuming a sinusoidal input signal

$$v_{in}(t) = v_{in}^{(+)}(t) - v_{in}^{(-)}(t) = V_{in}\sin(\omega t) \tag{2.1}$$

if v_{in} is positive (negative), M_{P1} and M_{N2} are on (off) and M_{P2} and M_{N1} are off (on). Therefore, a positive output current is generated in the storage capacitor, C_{str}, regardless the sign of v_{in}, thus producing a dc output voltage, $V_{out.}$

RF rectifiers for energy harvesting are typically designed to supply an output voltage, V_L, to the load, which is higher than the RF input amplitude. To achieve high values of V_L, a multi-stage rectifier is used as shown in Fig. 2.2, where N stages are coupled to the RF input signal through the pump capacitors, C_p [2]-[3].

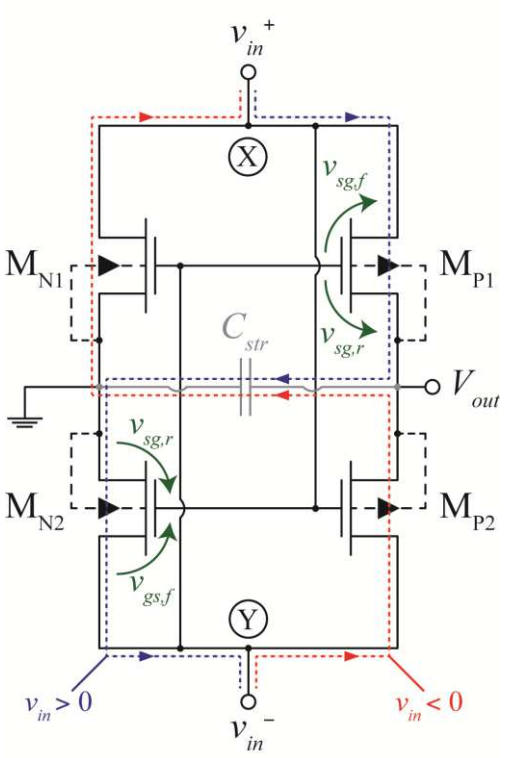

Fig. 2.1. Schematic of the single-stage CMOS differential-drive.

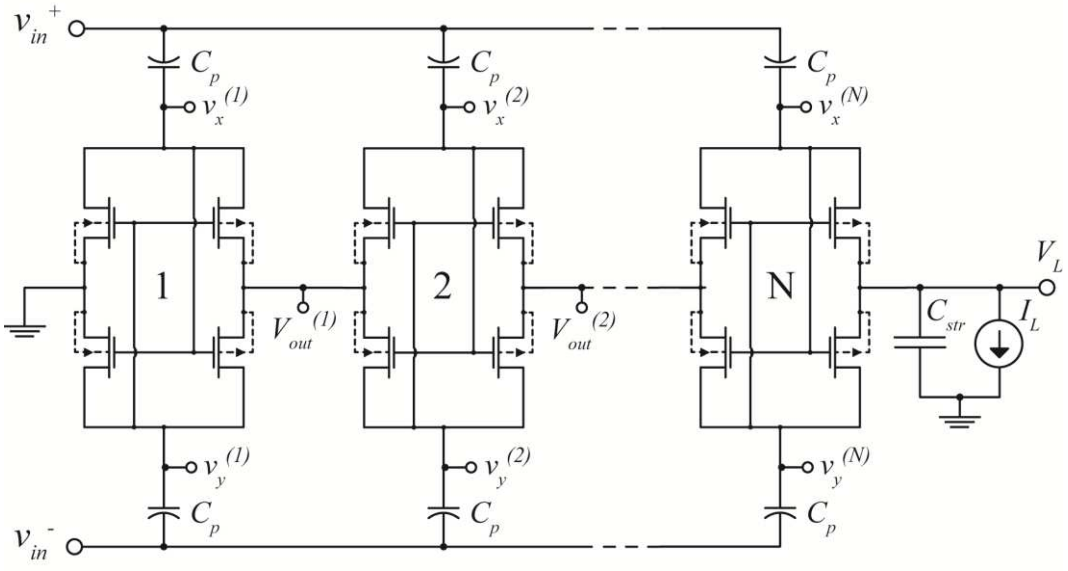

Fig. 2.2. Schematic of the multi-stage CMOS differential-drive.

In this way

$$V_{out}^{(n)} \approx nV_{out}^{(1)} \;;\; n = 1,2,\ldots,N \tag{2.2}$$

where

$$V_{out}^{(1)} = V_{out} = \alpha V_{in} - V_{on} \tag{2.3}$$

is the dc output voltage contribution of a single stage, being αV_{in} the amplitude of the transistor drive voltage and V_{on} the voltage drop across the couple of on-state transistors, i.e. M_{P1}/ M_{N2} or M_{P2}/M_{N1} depending on the sign of v_{in}. Coefficient α accounts for the capacitive partition between C_p and the parasitic capacitance C_{par} between nodes X and Y in Fig. 2.1 mainly due to the transistor size. By using (2.2) and (2.3), it results

$$V_{out}^{(N)} = V_L = N\left(\alpha V_{in} - V_{on}\right) \tag{2.4}$$

Equation (2.4) is valid under the assumption of symmetric stages, which means to isolate n-type transistor bulk by adopting a triple-well technology.

For the generic n^{th}-stage, the steady state behavior at nodes X and Y is approximately expressed by

$$v_x^{(n)}(t) = \left(n - \frac{1}{2}\right)V_{out} + \frac{1}{2}\alpha v_{in}(t) \tag{2.5}$$

$$v_y^{(n)}(t) = \left(n - \frac{1}{2}\right)V_{out} - \frac{1}{2}\alpha v_{in}(t) \tag{2.6}$$

The dc component in (2.5) and (2.6) can easily be explained by considering that nodes X and Y are alternatively connected to $V_{out}^{(n)}$ and $V_{out}^{(n-1)}$, thus resulting in a square wave at the same frequency of v_{in} and with an average value of $(n-1/2)V_{out}$. Considering an 868-MHz input signal with a 0.4-V amplitude, typical transient waveforms for v_x, v_y and V_{out} in the first stage are shown in Fig. 2.3.

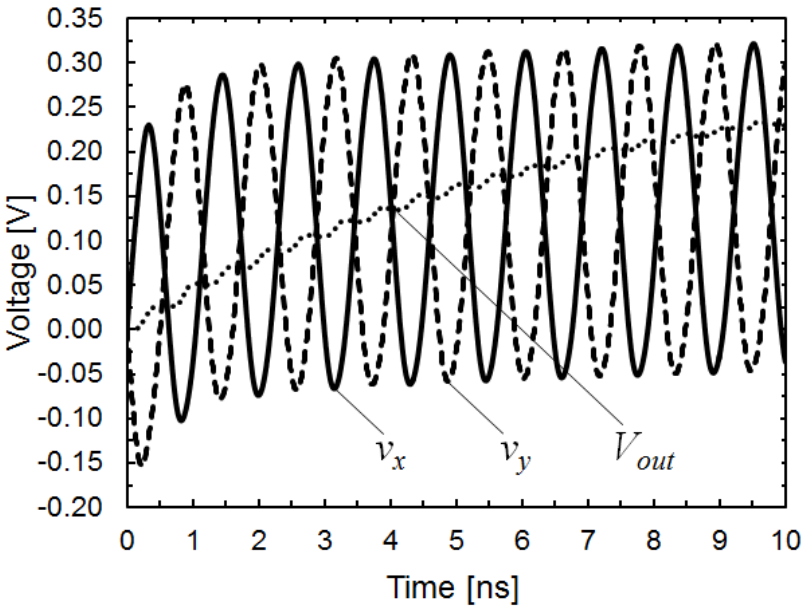

Fig. 2.3. Typical voltage waveforms in internal nodes, X and Y, of the first stage of a CMOS differential-drive rectifier.

By inspecting the basic cell in Fig. 2.1, a slightly positive v_{in} is not enough to charge C_{str}. Indeed, considering e.g. transistors M_{P1} and M_{N2}, a forward current charging C_{str} is produced only when $v_{sg,f} > v_{sg,r}$ and $v_{gs,f} > v_{gs,r}$ in M_{P1} and M_{N2},

respectively. Using (2.4-2.6), that include the effect of the pump capacitors, these conditions on gate-source voltages lead to

$$\alpha v_{in}(t) > V_{out} \tag{2.7}$$

On the other hand, a reverse current appears discharging the storage capacitor when $\alpha v_{in}(t) < V_{out}$, which is a typical loss mechanism of the full-wave rectifier affecting its efficiency.

2.2 Proposed topology

The proposed approach lies in the threshold-voltage variation techniques based on body-voltage control. Specifically, it reduces or increases V_t depending on whether the transistor in the rectifying stage is pushed in forward or reverse conduction, respectively. The improvement is achieved by properly driving the transistor bulk terminals with control signals inherently available in the original rectifier [4].

Fig. 2.4 shows the proposed approach, where only the generic n^{th}-stage of the rectifier is considered for simplicity. In the following, it is demonstrated that internal signals, v_x and v_y, in (2.5) and (2.6), can well be exploited as control signals since they provide a tunable dc component and a complementary variable component that are suitable to drive the bulk terminals. Specifically, the optimum dc component, $V_{opt,p}$ ($V_{opt,n}$), is the same for the two p-type (n-type) transistors of the n^{th}-stage and can be fulfilled by selecting the proper $n–i$ ($n–j$) stage from which signals v_x and v_y are derived.

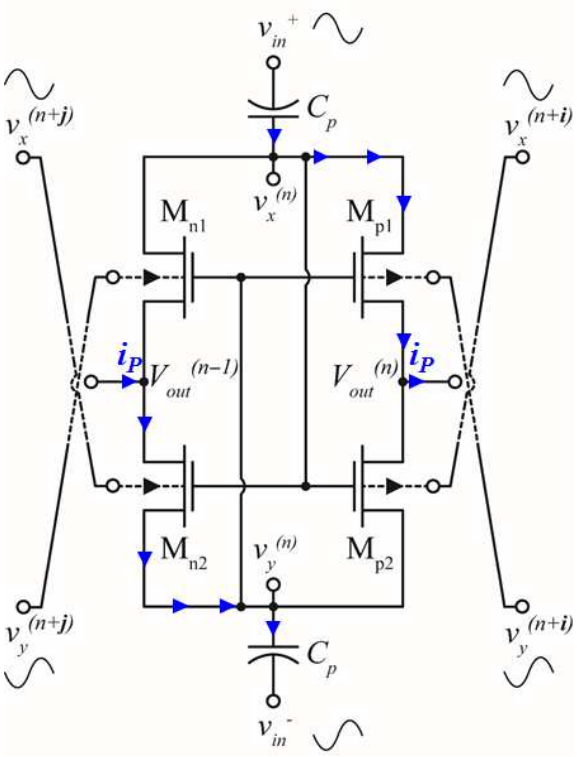

Fig. 2.4. Schematic of the generic n^{th}-stage with the proposed improvement.

The optimum index i (j) is valid for all the stages of the entire multi-stage rectifier, except for those stages in which the condition $1 \leq n\text{–index} \leq N$ is not satisfied. For these stages, the bulks of p-type and n-type transistors can be connected to V_L and ground, respectively.

Let us now evaluate the bulk-source voltages of the transistors for the n^{th}-stage. By referring to the transistor M_{P1}, the resulting expression for $v_{bs,P1}^{(n)}$ depends on the input signal. Indeed, the source voltage $v_{s,P1}^{(n)}$ is equal to $V_{OUT}^{(n)}$ when M_{P1} works in reverse conduction and coincides with $v_x^{(n)}(t)$ in forward conduction. Therefore, using (2.3-2.6), the proposed solution leads to

$$v_{bs,P1}{}^{(n)}(t)=\begin{cases}(i-1/2)V_{out}-\alpha v_{in}(t)/2 & \alpha v_{in}(t)<V_{out}\\ iV_{out}-\alpha v_{in}(t) & \alpha v_{in}(t)\geq V_{out}\end{cases} \tag{2.8}$$

whereas in the classic differential-drive rectifier

$$v_{bs,P1}{}^{(n)}(t)=\begin{cases}0 & \alpha v_{in}(t)<V_{out}\\ V_{out}/2-\alpha v_{in}(t)/2 & \alpha v_{in}(t)\geq V_{out}\end{cases} \tag{2.9}$$

During the overall conduction angle of the input signal, $v_{bs,P1}{}^{(n)}$ varies in a range given by

$$\Delta v_{bs,P1}{}^{(n)}(t)=v_{bs,P1}{}^{(n)}(t)\,|_{v_{in}=-V_{in}}-v_{bs,P1}{}^{(n)}(t)\,|_{v_{in}=V_{in}} \tag{2.10}$$

where V_{in} is the input amplitude according to (2.1). Using in (2.10) the values of $v_{bs,P1}{}^{(n)}$ in (2.8) for forward and reverse conduction, the proposed solution provides a maximum bulk-source variation equal to

$$\Delta v_{bs,P1}{}^{(n)}(t)=(3\alpha V_{in}-V_{out})/2 \tag{2.11}$$

that is much higher than

$$\Delta v_{bs,P1}{}^{(n)}(t)=(\alpha V_{in}-V_{out})/2 \tag{2.12}$$

derived from (2.9) and (2.10) for the classic solution. This results in a higher variation of V_t for the proposed rectifier, according to the body-effect equation.

Index *i (j)* can easily be found with simulations by properly applying signal $\alpha v_{in}(t)/2$ to the bulk terminals of the n^{th}-stage and sweeping its dc component to

maximize efficiency. Due to the modularity of the rectifier, index *i (j)* derived for the generic n^{th}-stage will be valid for all the rectifier stages and hence further simulations are not required. By equating the optimum dc component derived from simulation, $V_{opt,p}^{(n)}$, to the dc component in (2.4), we can find index *i* as

$$i = \left[\frac{V_{opt,p}^{(n)}}{V_{out}} + \frac{1}{2} - n \right] \tag{2.13}$$

where

$$V_{opt,p}^{(n)} = V_{opt,p}^{(1)} + (n-1)V_{out} \tag{2.14}$$

being $V_{opt,p}^{(1)}$ referred to the rectifier ground and remembering that $V_{OUT}^{(n-1)}$ is $(n-1)V_{OUT}$, according to (2.2). Index *j* can be derived in the same way by substituting $V_{OPT,p}^{(n)}$ with $V_{OPT,n}^{(n)}$ in (2.13).

Fig. 2.5 shows the shape of the steady-state pumping current, i_P, for the compensated n^{th}-stage in Fig. 2.4 during the positive half-wave of the input signal. In this simulation, the single-stage dc voltage contribution, V_{out}, and the average output current were set to 240 mV and 1 μA, respectively. Current i_P flows in M_{P1} and M_{N2} (thanks to the stage symmetry) and goes to the output terminals $V_{out}^{(n)}$ and $V_{out}^{(n-1)}$. Fig. 2.4 also shows the same current under equal output conditions for the uncompensated stage, i.e. with the bulk terminals connected as in Fig. 2.1. The current in the white area flows in the positive direction and hence will be transferred to next stages and finally delivered to the storage capacitor at the multi-stage rectifier output. The grey areas in Fig. 2.5 show instead the reverse

conduction windows where current i_P is negative and hence discharges the storage capacitor. Similar current waveforms are produced with the negative half-wave of the input signal thanks to M_{N1} and M_{P2}. Thanks to the reduced reverse current, a lower forward current is needed in the compensated stage to satisfy the same output conditions. This means lower power consumption and hence better efficiency and input sensitivity.

An example with $i = -j = 1$ is shown in Fig. 2.6, where the n-type transistors of the first stage and the p-type transistors of the last stage were connected to ground and output, respectively.

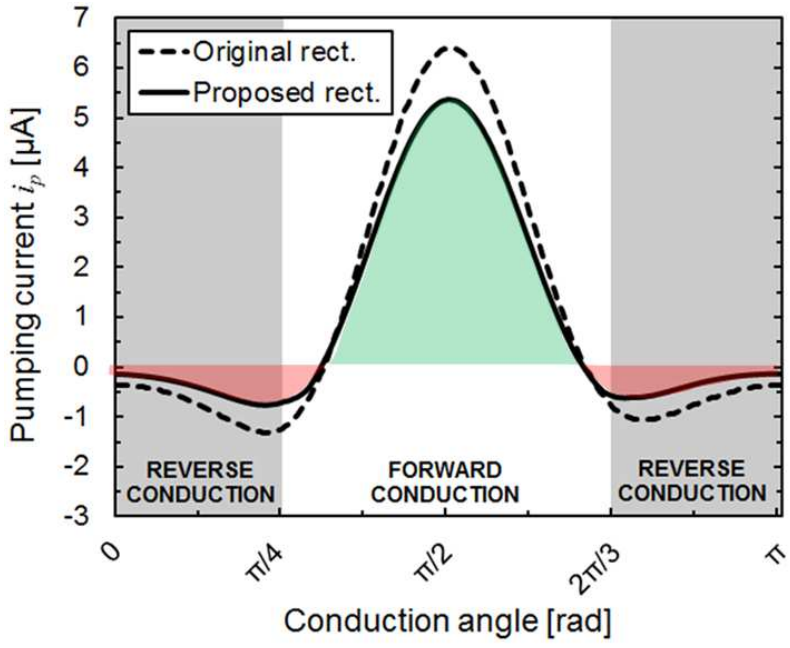

Fig. 2.5. Steady-state pumping current of the proposed and classic rectifier stage.

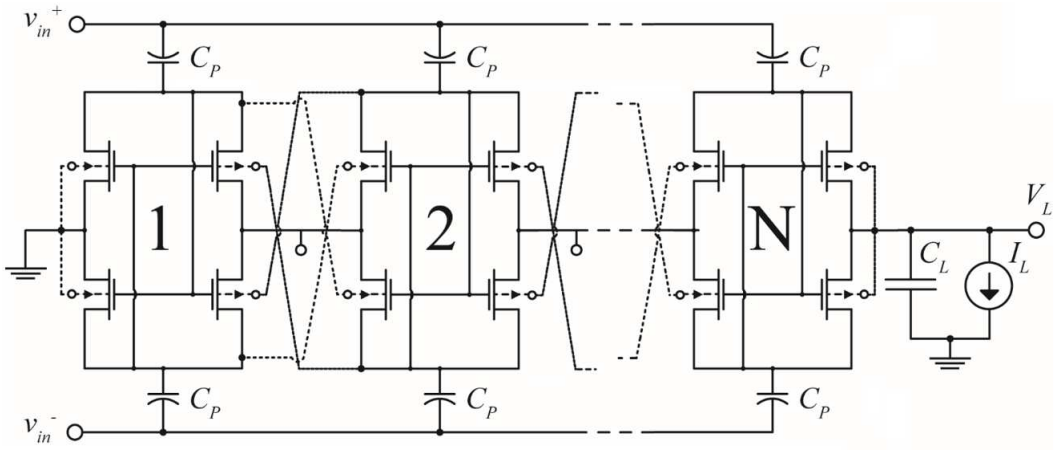

Fig. 2.6. Simplified example with $i = -j = 1$ of the proposed CMOS differential-drive rectifier with body voltage control.

2.3 Rectifier model

A model for the CMOS differential-drive rectifier is useful to well understand how design parameters are linked to specifications. Fig. 2.7 shows a linear model of a single-stage rectifier based on a voltage-controlled voltage source [1], where C_p and C_{par} have been already defined in previous section, R_{eq} is the equivalent resistance of the ideally lossless rectifier, R_{loss} accounts for losses mainly due to reverse current, and εC_p is the parasitic capacitance between the bottom plate of C_p and ground.

R_{eq} can be evaluated by equating the input ac power with the load power as follows

$$\frac{(\alpha V_{in})^2}{2R_{eq}} = \frac{V_{out}^{\ 2}}{R_L} \tag{2.15}$$

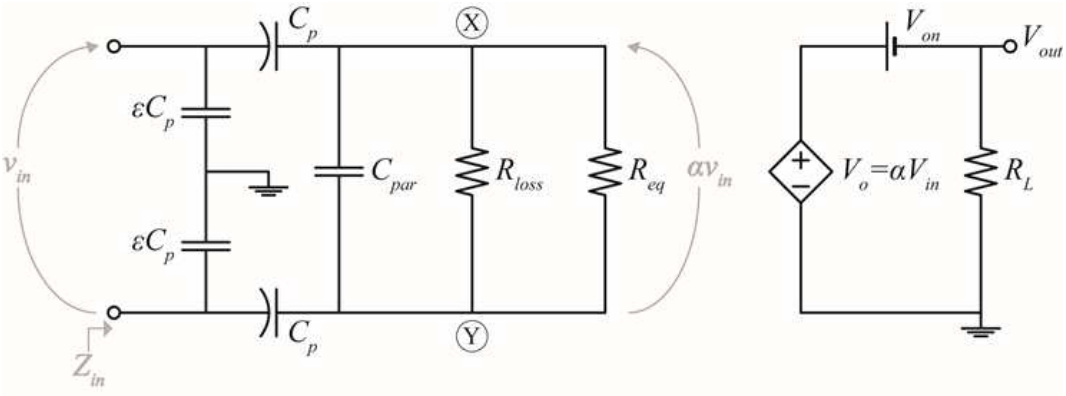

Fig. 2.7. Linear model of a single-stage full-wave rectifier.

where α is given by

$$\alpha = \frac{C_p}{C_p + 2C_{par}} \tag{2.16}$$

Therefore, R_{eq} in the ideal rectifier is approximately related to the ratio of V_{in} to V_{out} and to the load resistance. By substituting (2.3) in (2.15), an expression of R_{eq} dependent on V_{on} is achieved that is given by

$$R_{eq} = \frac{1}{2}\left(\frac{\alpha V_{in}}{\alpha V_{in} - V_{on}}\right)^2 R_L \tag{2.17}$$

By inspection of Fig. 2.7, the input resistance of the single-stage rectifier results

$$R_{in}^{(1)} = \left(R_{eq} \parallel R_{loss}\right)\left(1 + 2\frac{C_{par}}{C_p}\right) = \frac{R_{eq} \parallel R_{loss}}{\alpha} \tag{2.18}$$

Fig. 2.8 shows $R_{in}^{(1)}$ as a function of W for three values of C_p. It is apparent that $R_{in}^{(1)}$ slightly depends on W and becomes nearly constant for low C_p.

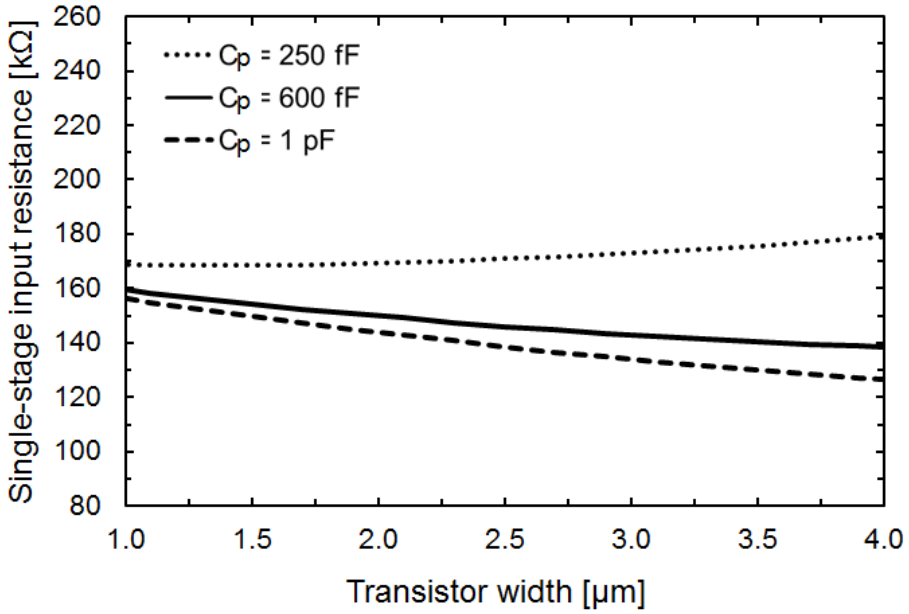

Fig. 2.8. Simulated input resistance of the single-stage rectifier versus transistor W for different C_p values.

As far as input capacitance $C_{in}^{(1)}$ is concerned, it can easily be calculated from the model in Fig. 2.7. It results

$$C_{in}^{(1)} = C_p\left(\frac{\varepsilon}{2} + \frac{C_{par}}{C_p + 2C_{par}}\right) = \frac{\varepsilon C_p}{2} + \alpha C_{par} \tag{2.19}$$

The dependence of $C_{in}^{(1)}$ on W is shown in Fig. 2.9. $C_{in}^{(1)}$ linearly depends on W but its dependence on C_p is low. Indeed, an increase of C_p by a factor of four (i.e., from 250 fF to 1 pF) increases $C_{in}^{(1)}$ by only 20%. This means that the input capacitance mainly depends on parasitic capacitances due to rectifying transistors, which are related to W.

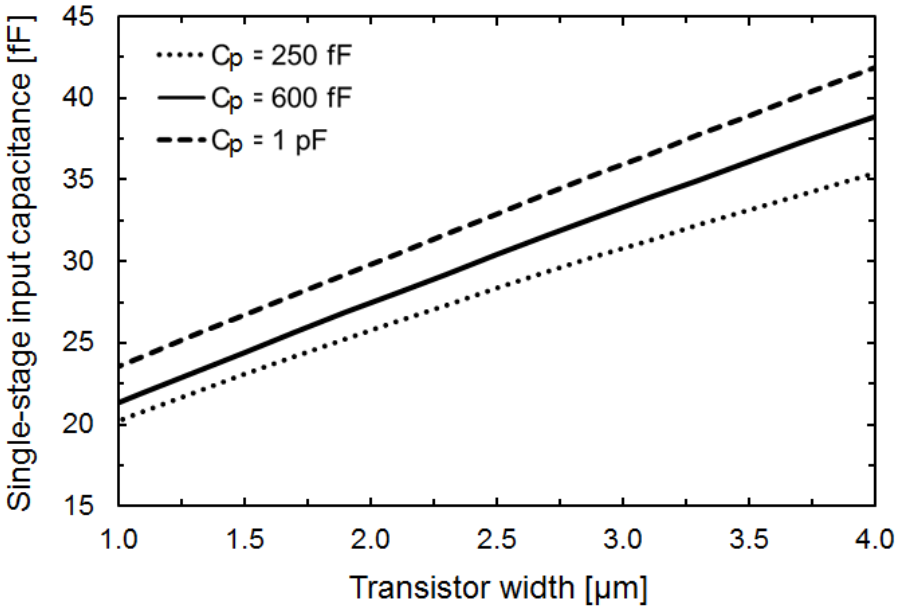

Fig. 2.9. Simulated input capacitance of the single-stage rectifier versus transistor W for different C_p values.

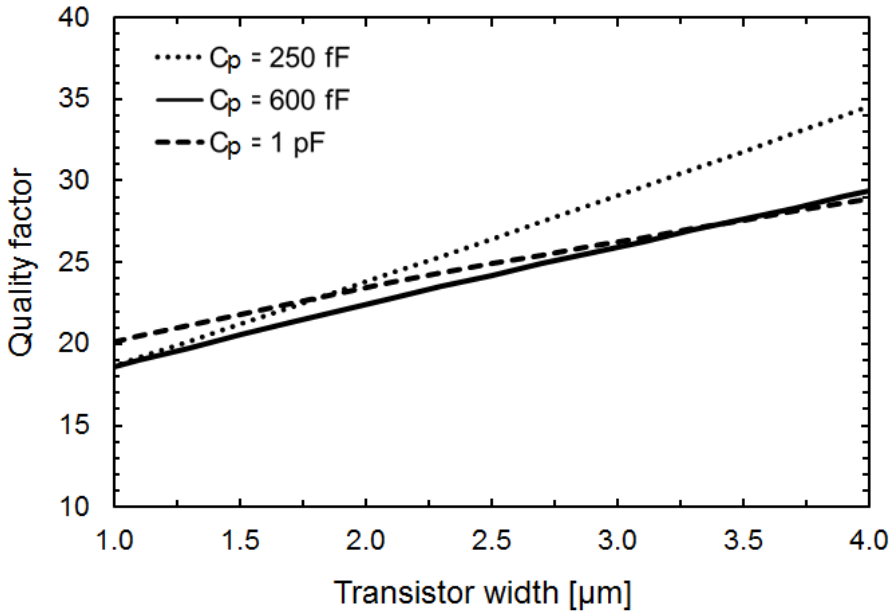

Fig. 2.10. Simulated quality factor of the single-stage rectifier versus transistor W for different C_p values.

Fig. 2.8 and Fig. 2.9 say that W impacts on $R_{in}^{(1)}$ much less than on $C_{in}^{(1)}$. Therefore, quality factor Q that is determined by the product of $R_{in}^{(1)}$ with $C_{in}^{(1)}$ exhibits the same linear dependence on W and the same slight dependence on C_p than $C_{in}^{(1)}$, as shown in Fig. 2.10.

Finally, the rectifying stages are placed in parallel in the multi-stage rectifier and hence the input resistance and capacitance, R_{in} and C_{in}, can simply be expressed as

$$R_{in} = \frac{R_{in}^{(1)}}{N} \tag{2.20}$$

$$C_{in} = NC_{in}^{(1)} \tag{2.21}$$

Therefore, Q does not depend on the number of rectifying stages. Of course, C_{in} should be corrected to account for both the input pad and layout parasitic capacitances. It is suggested to not use pump capacitors C_p too small to avoid that coefficient α, and hence the transistor drive voltage, greatly depends on the layout parasitic capacitances.

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Chapter III

Antenna

3.1 Proposed ICL antenna

An ICL antenna is made up of an inductive small loop, which is closely coupled to a radiating body, as shown in Fig. 3.1. Within the present system design, the substrate area was set to the credit card dimensions as defined by standard ISO/IEC 7810 ID-1, i.e. 85.6 x 54 mm. The two terminals of the loop are connected to the rectifier chip. Operating frequency and substrate permittivity set the length of the radiating body, which was folded to meet the area constraint 0-[2]. The inductive loop has a rectangular shape to enhance inductive coupling that needs length *a* much grater than width *b*. The bi-conical shape of the radiating body is generally adopted to increase bandwidth [3], but in this design it was mainly exploited to accurately set the impedance matching. Moreover, a slot was cut out from the radiating body to further enhance inductive coupling.

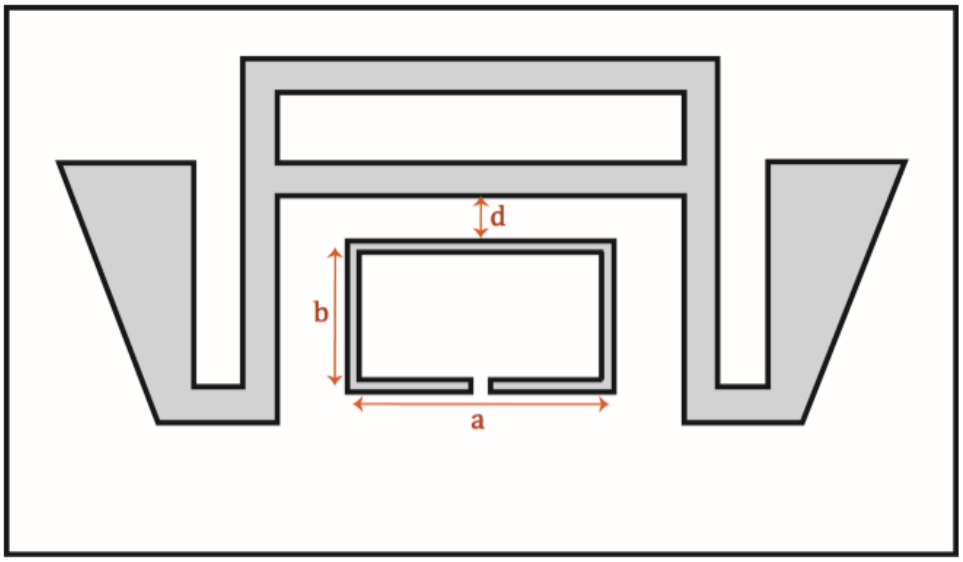

Fig. 3.1. Layout of the proposed inductively coupled loop antenna.

Loop perimeter $p=2(a+b)$ and distance d from the radiating body are the main design parameters, which determine the antenna output resistance and reactance, R_a and X_a, ($X_a = \omega L_a$) and the efficiency, η_A, as shown in Fig. 3.2 and Fig. 3.3, respectively, where also the impedance quality factor, Q, was plotted.

Specifically, Fig. 3.2 shows a family of curves of the antenna series resistance and reactance as function of parameters p and d. As apparent in Fig. 3.2, input reactance depends only on p (i.e., on the loop equivalent inductance), whereas input resistance is due to both inductive coupling and loop resistive losses mainly related to d and p, respectively. On the other hand, increasing d reduces coupling between the loop and the radiating body, thus leading to lower antenna efficiency.

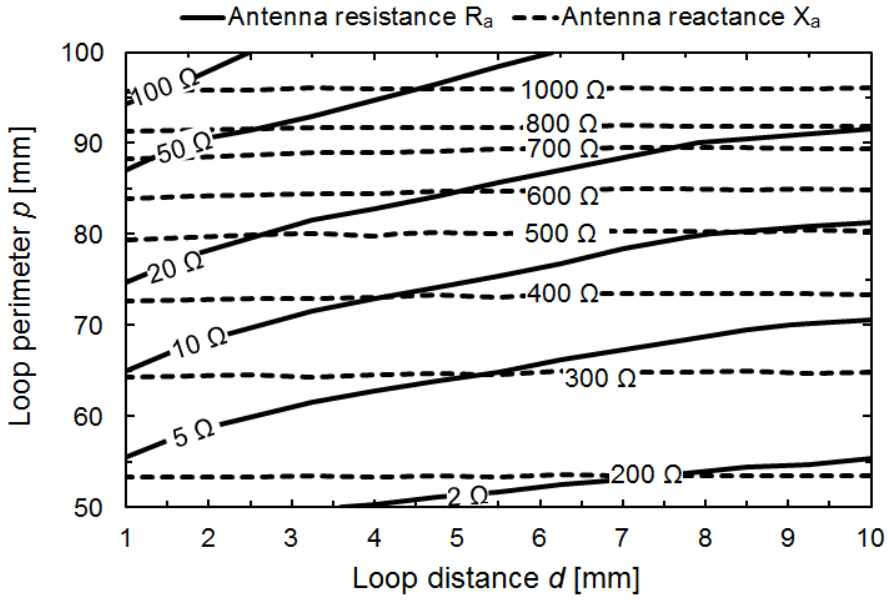

Fig. 3.2. Simulated level curves showing series resistance R_a and reactance X_a of the proposed ICL antenna.

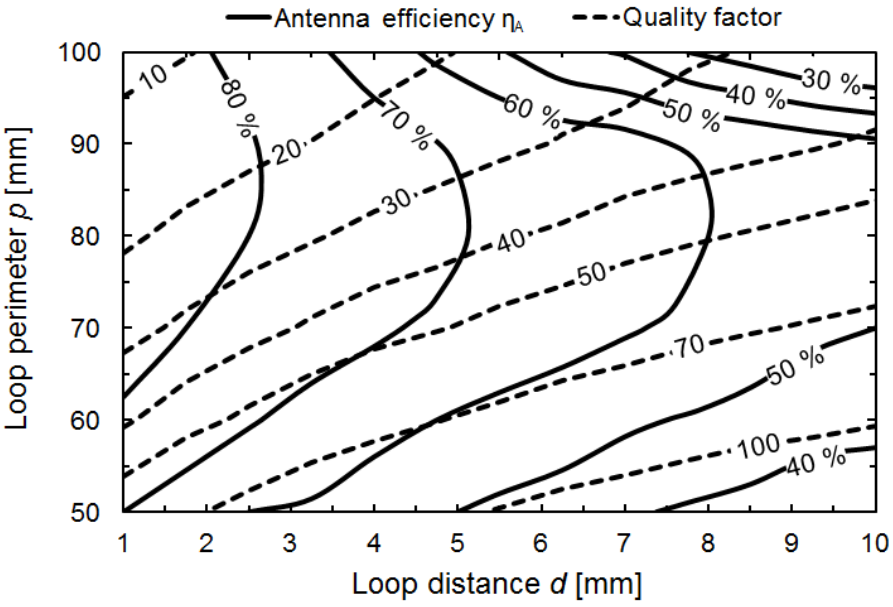

Fig. 3.3. Simulated level curves showing efficiency η_A and quality factor Q of the proposed ICL antenna.

Moreover, antenna efficiency reduces as quality factor increases. Indeed, the antenna quality factor Q is

$$Q = \frac{2\pi f_0 L_a}{R_a} \tag{3.1}$$

where R_a accounts for both radiation and loss resistances but it is usually dominated by the former. Therefore, Q can manly be increased by increasing L_a, which in turn means higher loss resistances and lower antenna efficiency. Finally, the efficiency degradation in the upper side of Fig. 3.3 is due to a high loop perimeter that reduces the distance of segments b from the radiating body for a given area constrain, thus introducing spurious coupling.

A 3D radiation pattern is shown in Fig. 3.4. The antenna is quite isotropic in the x-z plane, while no power is radiated along y axis.

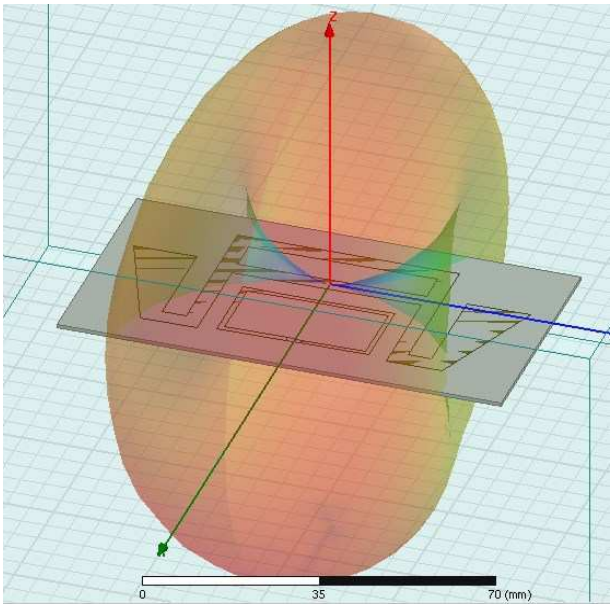

Fig. 3.4. Radiation pattern of the proposed ICL antenna.

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Chapter IV

Co-design methodology

4.1 General outline

The proposed co-design procedure provides a system design strategy to maximize the performance of the overall harvesting system once rectifier and antenna are connected together. As a first step, a preliminary design of the rectifier is carried out as starting point before proceeding with the co-design procedure. Then, an antenna matching chart is used, which shows antenna efficiency η_A and quality factor Q for each matching-impedance operating point. Finally, the rectifier is properly re-designed to achieve the best performance of the antenna-rectifier system. Importantly, harvester performance is maximized at sensitivity, since it sets the most important performance parameter of a harvesting system application that is maximum operating distance.

4.2 Rectifier design

Co-design procedure requires a lower number of iterations if the optimum stand-alone solution for the rectifier is assumed as starting point. For a given signal bandwidth and load specification, the optimum rectifier design is achieved by setting transistor size W, number of stages N, and pump capacitances C_p, which maximize efficiency η_R.

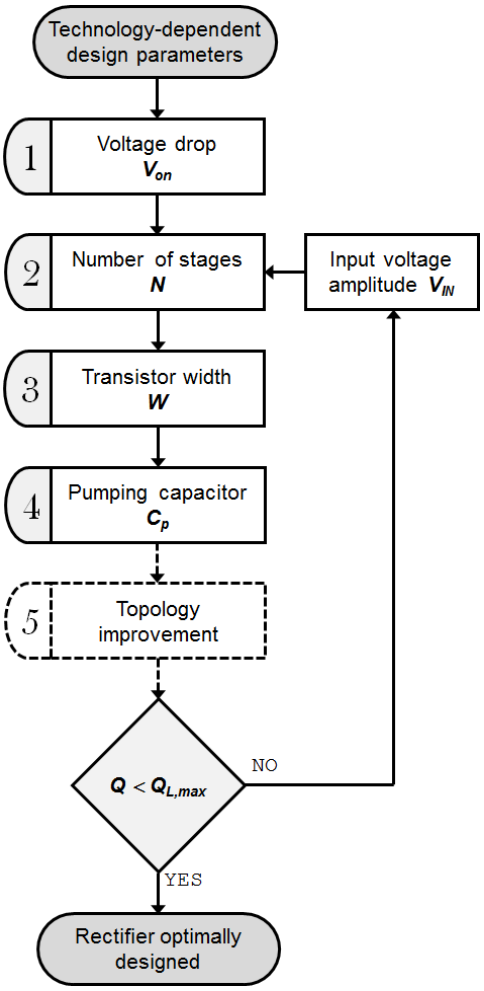

Fig. 4.1. Proposed design flow for the differential-drive rectifier.

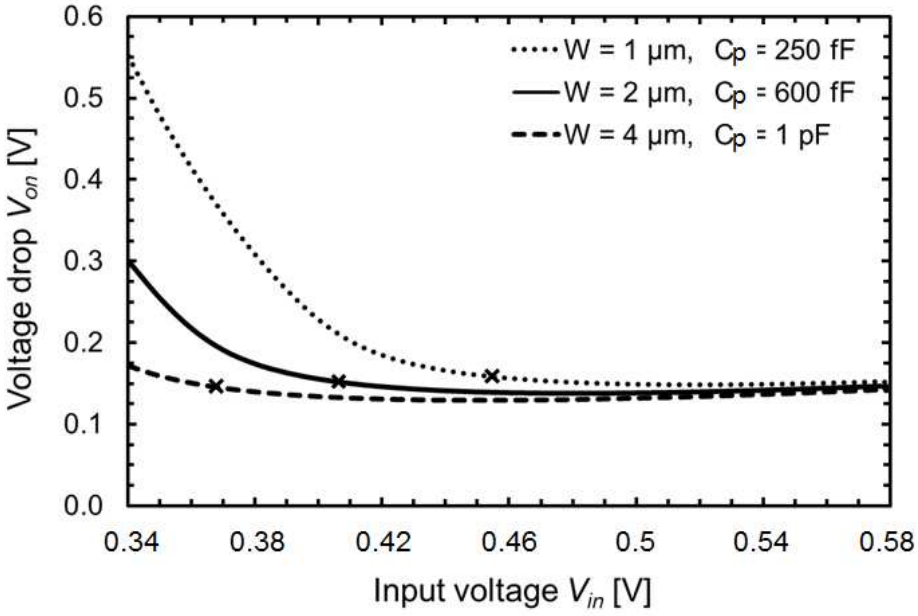

Fig. 4.2. Simulated curves of V_{on} versus V_{in} at different couples of width and pump capacitance values for a single-stage CMOS full-wave rectifier (V_{out} = 240 mV, I_L = 1 µA).

4.2.1 Technology-dependent design parameters

Fig. 4.1 shows the flow chart of the proposed design strategy for a differential-drive rectifier. As design constrain, the ratio of p-type and n-type transistor size is set according to the mobility ratio to guarantee conduction symmetry in both transistors.

4.2.2 Voltage-drop estimation

Step 1 in the design flow in Fig. 4.1 addresses the estimation of voltage V_{on}, which is required in step 2 to find the number of stages, N, for the optimum stand-alone rectifier. Voltage V_{on} depends on V_{in}, W, and C_p, as shown in Fig. 4.2 for a single-stage rectifier, where it is plotted for three different couples of W and

C_p, at I_L = 1 μm. Fig. 4.2 also shows for each couple of W and C_p the value of V_{in} that maximizes efficiency (see crosses). The related values of V_{on} fall in the knee regions where V_{on} approaches its asymptotic value, which is the same regardless the values of the design parameters. Therefore, V_{on} can well be estimated with this asymptotic value by simply increasing V_{in} at will.

4.2.3 Number of stages

If C_p is considerable higher than C_{par}, α in (2.16) is close to unity and the transistor drive voltage, αv_{in}, approaches v_{in}. It is recommended to work with an input amplitude voltage V_{in} as low as possible [1] to reduce reverse currents. However, by working with V_{in} below the threshold voltage, the rectifier output power becomes extremely low. As tradeoff between low reverse current and acceptable output power, input voltage amplitude V_{in} is set equal to the p-type threshold voltage, $V_{t,p}$, being it usually higher than the n-type one. Using (2.4), the number of stages, N, in step 2 is given by

$$N = \frac{V_L}{V_{th,p} - V_{on}} \tag{4.1}$$

4.2.4 Transistor width

Step 3 in the flow chart concerns transistor size W that is set for optimum rectifier efficiency. To this purpose, Fig. 4.3 shows the designs for an output voltage of 240 mV and four load currents, in which for each current an optimum W for maximum η_R is determined. As apparent in Fig. 4.3, higher load current

leads to higher η_R along with higher W. Fig. 4.4 shows η_R as function of input voltage for different values of W at $I_L = 1$ µm, where a voltage of 240 mV was considered as output specification. Despite the three curves have the same maximum η_R, only the design with $W = 2$ µm achieves this maximum, thanks to V_{in} that is almost equal to the transistor threshold voltage (i.e., 0.4 V).

It is worth noting that the curve with $W = 1$ µm gives the maximum η_R with a slightly higher V_{out}. However, exceeding the output specification leads to lower sensitivity. On the other hand, the curve with $W = 4$ µm achieves the maximum η_R with V_{out} and hence does not meet specification.

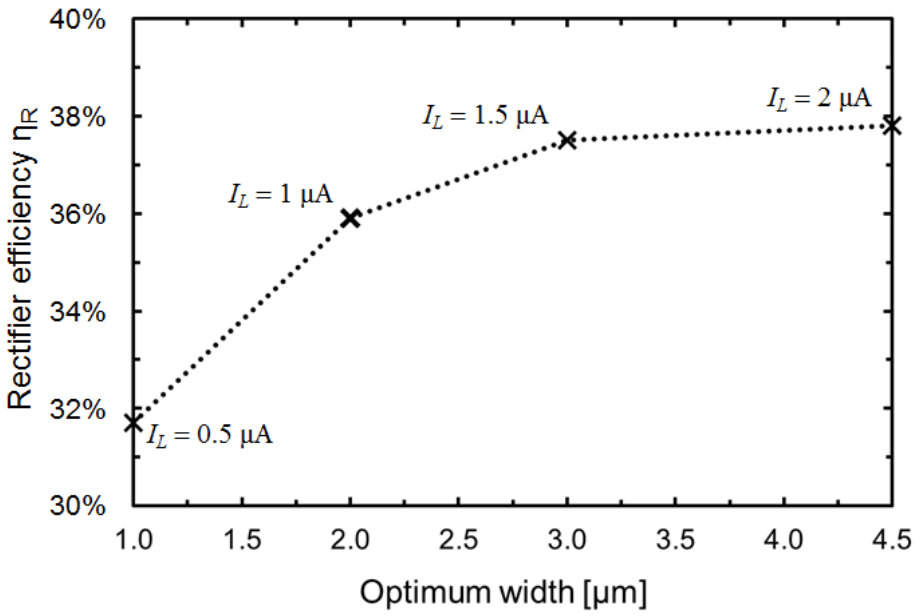

Fig. 4.3. Rectifier efficiency evaluated at different load currents ($V_{out} = 240$ mV).

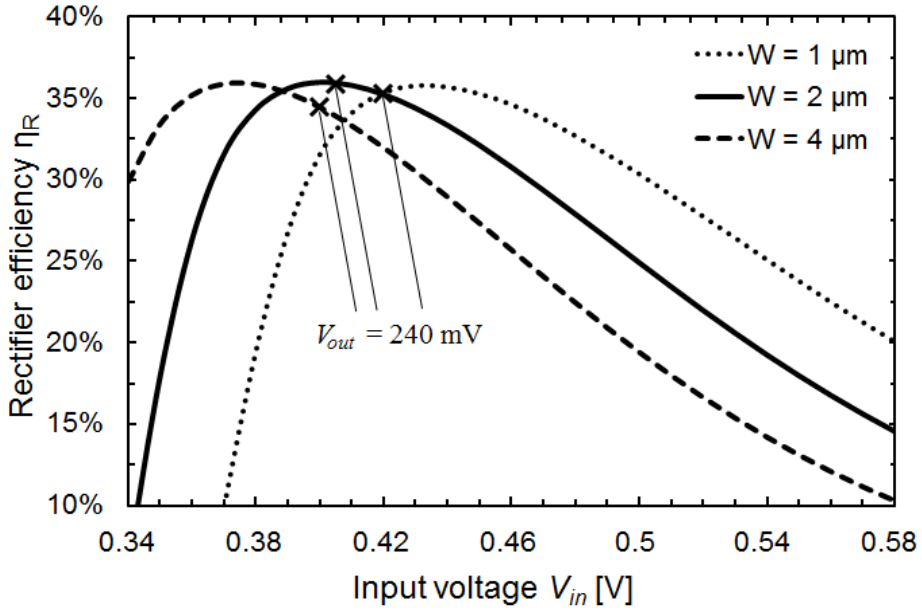

Fig. 4.4. Simulated curves of η_R versus V_{in} at different width values for a single-stage CMOS full-wave rectifier (V_{out} = 240 mV, I_L = 1 µA).

4.2.5 Pumping capacitors

Step 4 sets C_p. In principal, this capacitance can be set to a low value. Indeed, Q only slightly depends on C_p as discussed in Chapter II (see Fig. 2.10) and the same peak of η_R is still achieved with a low capacitance as shown in Fig. 4.5. However, robustness to layout parasitic capacitances and α suggests a value of C_p not too small, as mentioned before. Moreover, a Q with a low C_{in} and a high R_{in} results in a worse operating point in terms of η_A for the antenna.

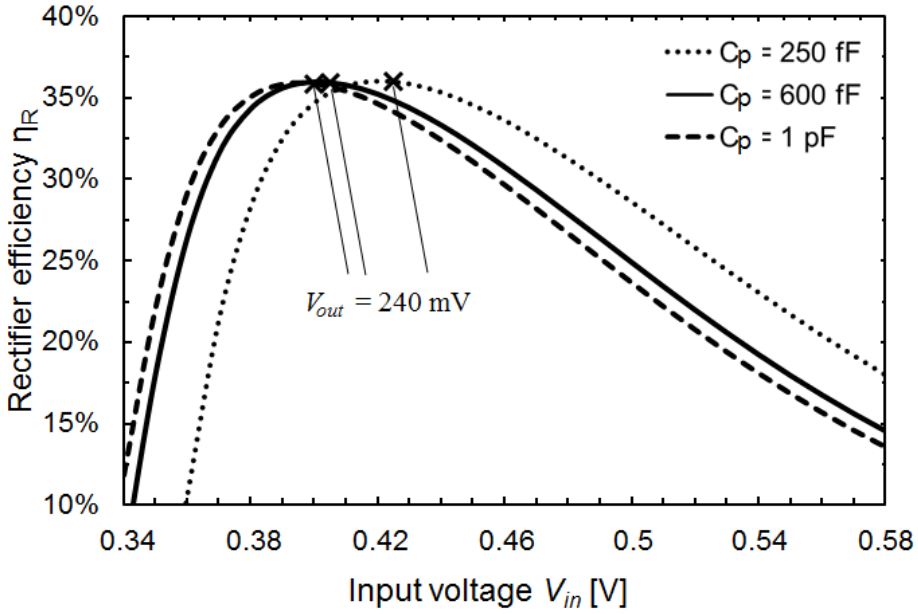

Fig. 4.5. Simulated curves of η_R versus V_{in} at different pump capacitance values for a single-stage CMOS full-wave rectifier (V_L = 240 mV, I_L = 1 µA).

4.2.6 Topology improvement

A step 5 is included that accounts for additional design parameters, if a different arrangement with respect to the conventional topology of differential-drive rectifier to improve its performance. In this work, the additional parameters is the index *i* (*j*), which defines how the connections between transistor bulks and internal nodes have to be accomplished [2].

4.2.7 Maximum allowable quality factor

In the final step, the Q of the rectifier input impedance is compared with the maximum allowable value, $Q_{L,max}$, for the bandwidth specification. If the quality

factor is higher than $Q_{L,max}$, a W lower than the optimum value defined in step 3 is needed according to Fig. 2.10, unavoidably leading to a lower sensitivity.

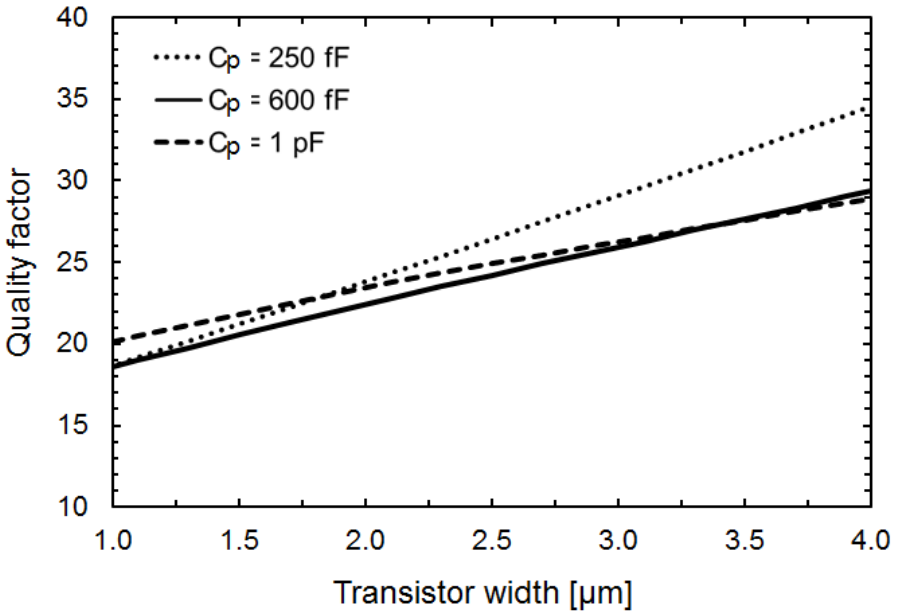

Fig. 4.6. Simulated curves of Q versus W at different pump capacitance values for a single-stage CMOS full-wave rectifier (V_L = 240 mV, I_L = 1 µA).

4.3 Co-design approach

Antenna chart is shown in Fig. 4.7, in which η_A and Q is plotted as a function of parallel input resistance R_p and reactance X_p. The matching chart is achieved by combining charts in Fig. 3.2 and Fig. 3.3. The operating point of the antenna/rectifier system identifies a point in the antenna chart. Since antenna and rectifier have to be matched together, each point in the chart in also the complex conjugate of the rectifier input impedance. The operating point provides the expected system efficiency, η_H, as a product of η_A and η_R.

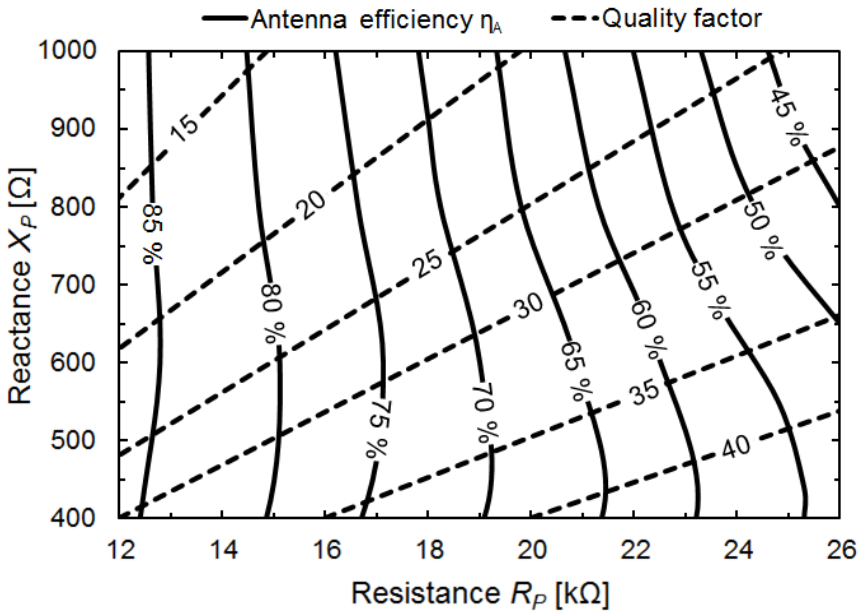

Fig. 4.7. Antenna matching chart adopted in the proposed co-design methodology.

To find the optimum system for the best performance in terms of efficiency, an effective way is to vary the number of stages, *N,* of the rectifier. Indeed, the variation of *N* does not affect *Q*, as can be found by multiplying (2.20) and (2.21), being

$$Q_L = 2\pi f_0 R_{in} C_{in} \tag{4.2}$$

and hence the bandwidth requirement is preserved. Moreover, the variation of *N* significantly changes the operating point in the antenna chart thus facilitating system performance optimization. Finally, the rectifier input impedance changes in a predictable way as apparent again from (2.20) and (2.21). Unfortunately, this behavior is not exactly true for the proposed rectifier topology due to the asymmetry induced by the body-voltage control. However, the impact of this

asymmetry on the impedance becomes negligible for a number of stages starting from 4. Fortunately, more than 5 stages are usually needed in common applications where output voltages higher than 1 V are required. Therefore, the proposed rectifier well fits with the co-design procedure discussed before.

Three designs were carried out to meet output specifications of typical applications. They are:

(A) V_L = 1.2 V and I_L = 1.2 μA;

(B) V_L = 2.4 V and I_L = 600 nA;

(C) V_L = 2.4 V and I_L = 1 μA.

Detailed iteration data of both antenna and rectifier efficiency for the three designs are reported in Table 4.2, Table 4.3 and Table 4.4. By referring to the co-design procedure for design A that is shown in Fig. 4.8, the rectifier starting point (i.e., the optimum stand-alone rectifier) is indicated with a filled circle in the antenna chart, while empty circles refer to the iterations. Instead, the concentric circle is the optimum harvesting system design (i.e., with maximum η_H). A handful legend regarding the iteration circles is shown in Table 4.1.

Table 4.1. Legend of the iteration circles shown in Fig. 4.8, Fig. 4.9, and Fig. 4.10.

	opt. η_R	opt. η_H
○	NO	NO
●	YES	NO
◎	NO	YES
◉	YES	YES

By increasing N from 5 to 7, η_R reduces by 5.5 percentage points but the overall efficiency η_H improves by more than 9 percentage points, as described in Table 4.2. Since the last iteration with $N = 8$ does not improve η_H, $N = 7$ sets the optimum system design.

Finally, according to (2.4), the higher is N the lower is the value V_{in} needed to obtain the required V_L. However, by increasing N above its optimum value, only little adjustments below $V_{th,p}$ occur on V_{in}. Thus, negligible improvements would be performed by re-designing W and C_P.

Design B, which is shown in Fig. 4.9, needs three iterations (i.e., one more than design A). Nevertheless, the final solution provides the same amount of improvement in terms of η_H. On the other hand, design C shows that the optimum design of the stand-alone rectifier also gives the best η_H, as shown in Fig. 4.10. Detailed data are reported in Table 4.3 and Table 4.4 for design B and C, respectively.

Table 4.2. Simulated antenna and rectifier PCE along with expected overall PCE within project A (V_L = 1.2 V, I_L = 1.2 μA).

Iteration number	***N***	**η_R**	**η_A**	**η_H**
1	5	**46.5 %**	42.5 %	19.8 %
2	6	44.5 %	61 %	27.1 %
3	7	41 %	71 %	**29.1 %**
4	8	37.5 %	**77.5 %**	29.1 %
5	-	-	-	-

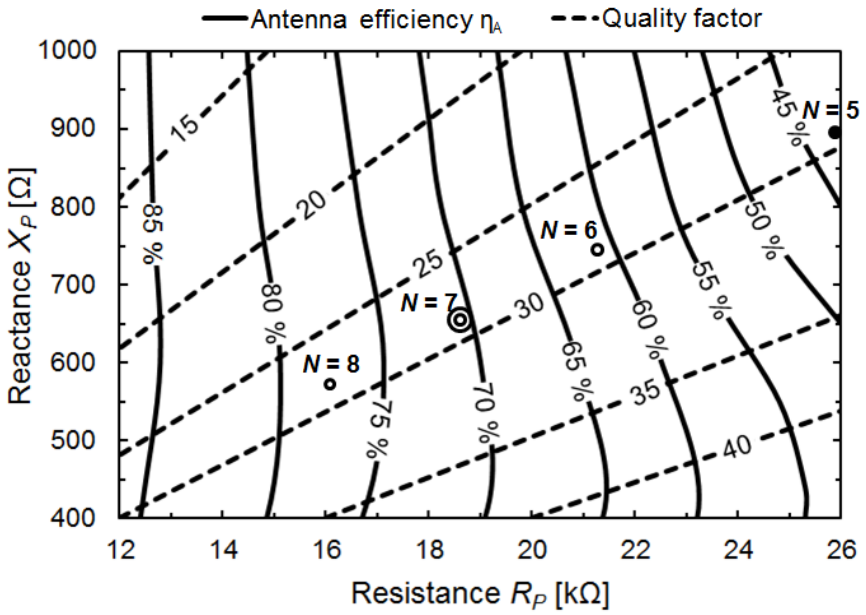

Fig. 4.8. Antenna matching chart adopted in design A.

Table 4.3. Simulated antenna and rectifier PCE along with expected overall PCE within project B (V_L = 2.4 V, I_L = 600 nA).

Iteration number	N	η_R	η_A	η_H
1	10	**46 %**	45.5 %	20.9 %
2	11	44 %	56 %	24.6 %
3	12	42.5 %	64 %	27.2 %
4	13	41 %	69 %	**28.3 %**
5	14	38 %	**74 %**	28.1 %

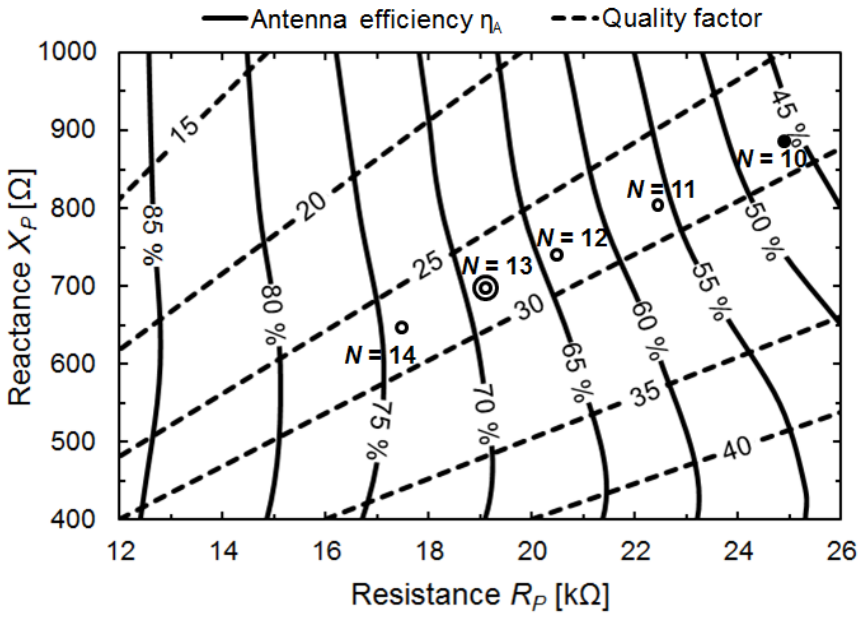

Fig. 4.9. Antenna matching chart adopted in design B.

Table 4.4. Simulated antenna and rectifier PCE along with expected overall PCE within project C (V_L = 2.4 V, I_L = 1 µA).

Iteration number	N	η_R	η_A	η_H
1	10	**46.5 %**	79 %	**36.7 %**
2	11	44.5 %	**82.5 %**	36.7 %
3	-	-	-	-
4	-	-	-	-
5	-	-	-	-

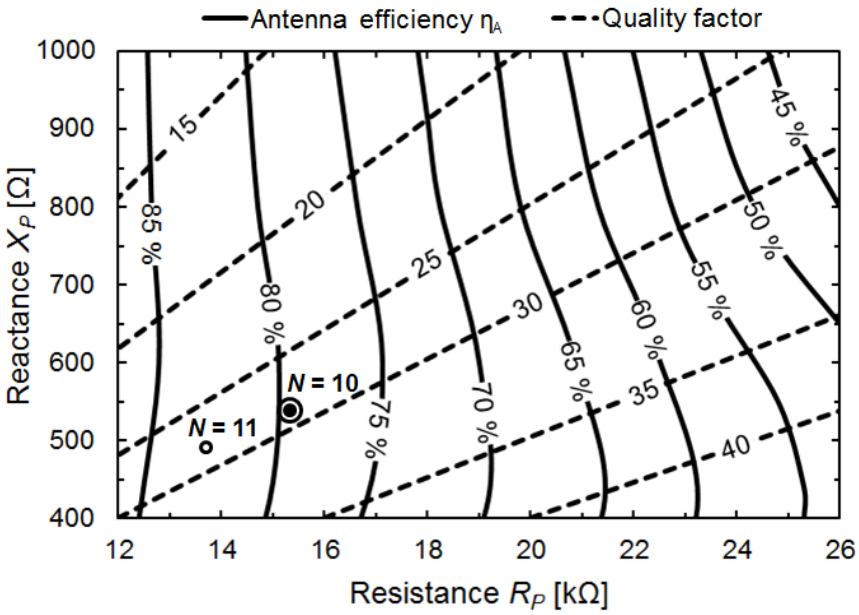

Fig. 4.10. Antenna matching chart adopted in design C.

References

[1] S. Mandal and R. Sarpeshkar, "Low-Power CMOS Rectifier Design for RFID Applications," *Circuits and Systems I: Regular Papers, IEEE Transactions on* , vol.54, no.6, pp.1177,1188, June 2007.

[2] L. Grasso, R. Guerra, and G. Palmisano, " A CMOS full-wave rectifer with threshold compensation based on inherent body-voltage control," To be published in *Microwave Conference (EuMC), 2016 European*, London, 2016.

Chapter V

Measurement methods

5.1 Rectifier measurement methods

A relatively high level of input resistance is essential for the rectifier operation, especially for high sensitivity systems where P_{in} is around −20 dBm or lower. In fact, by referring to (1.6), the resulting peak voltage of v_{in} cannot be lowered at will, since the intrinsic voltage threshold of the rectifier CMOS transistors have to be guaranteed. Thus, directly characterizing the rectifier with classical 50-Ω network analyzers is extremely imprecise because of the high impedance mismatch with Z_{in}, which produces an almost complete wave reflection.

The introduction of a passive matching network between the rectifier and the 50-Ω RF generator allows delivering the proper input power P_{in} to the circuit. However, a de-embedding technique is required to determinate the effective Z_{in} value along with the correct η_R.

Common Z_{in} impedances require an antenna with a relatively high equivalent inductance along with low series resistance, thus resulting adequate for matching high-impedance-phase-angle chips [1]. Thus, the antenna input impedance can be expressed as

$$Z_a = R_a + j\omega L_a = Z_{in}^* \tag{5.1}$$

A low R_a value makes difficult to obtain a high efficiency, η_A . Moreover, it also requires an adequate characterization.

A de-embedding technique was introduced to compensate the presence of the impedance matching network between the rectifier and the 50-Ω RF generator. We report the measurement results obtained for the 10-stage differential-drive rectifier (DUT) regarding project C (see Table 4.4), which was realized in a *STMicroelectronics* 130nm CMOS technology. The structure is fully differential and delivers a DC power P_L of 2.4 μW with a sensitivity level lower than –20 dBm. The circuit has been optimized at 868 MHz with a DC output voltage V_L equal to 2.4 V that can be easily interfaced with a power management circuitry [2].

As reported in Fig. 5.1 the basic idea consists in assembling the matching network and the rectifier (DUT) on different PCBs soldered together. Since our DUT is a fully differential circuit, the LC matching network also requires a balun, thus becoming a 3-port network.

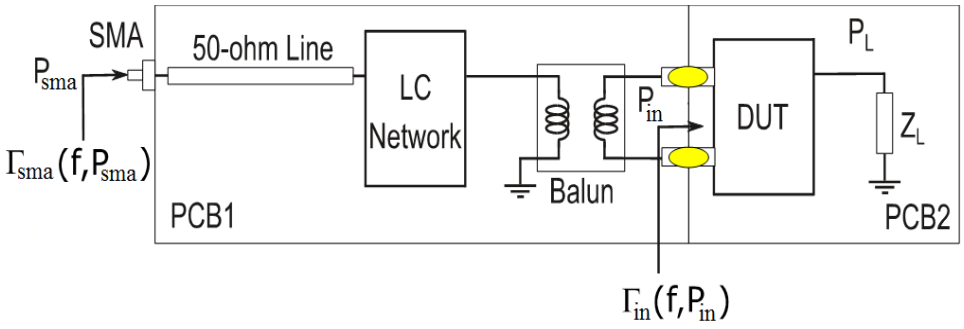

Fig. 5.1. Scheme of the rectifier measurement setup.

Once the DUT shows a good impedance matching, it is possible to measure the ratio P_L/P_{sma} at the operating frequency, thus characterizing the return loss $\Gamma_{sma}(f, P_{sma})$ at the input port.

Because of the dependency of the DUT input impedance from the incident RF power, it is very important to get the return loss behavior also as function of the P_{sma} values. Once the measurement data have been collected, the PCB1 passive network has to be completely characterized in terms of a 3x3 scattering matrix S^{nw}.

Two main theories have been implemented to perform the de-embedding technique: three-loads method and three-ports method.

5.1.1 Three-loads method

This method relies on the Short-Open-Load (SOL) technique, whose detailed analysis is presented in Appendix A.

As shown in Fig. 5.1, the impedance matching network (board PCB1) was connected to three different loads, i.e. short, open and 1 pF. By properly process the resulting reflection coefficients from the port 1 of the *Vector Network*

Analyzer (VNA), a scattering matrix of the impedance matching network was derived via software. Then, once the chip (board PCB2) was connected to the PCB1, the effect of the latter was cancelled by removing the 3x3 matrix previously obtained. Unfortunately, this procedure resulted strongly affected by load non-idealities and soldering, which differ for each measurement. Thus, the three-ports method was preferred.

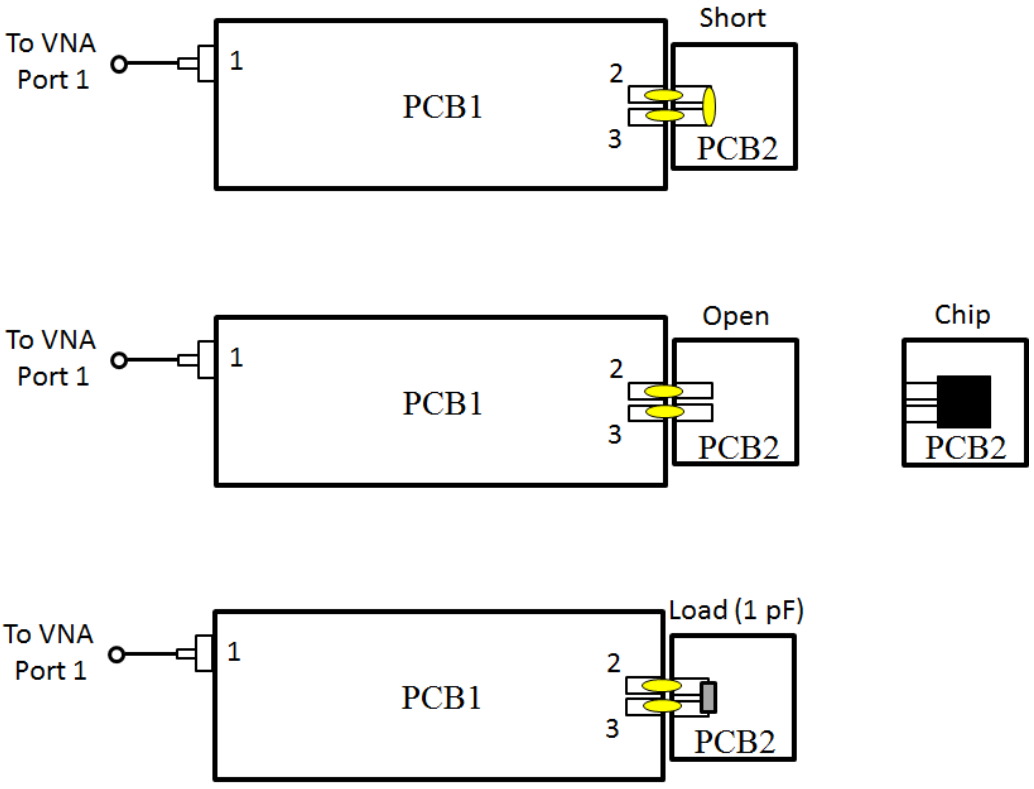

Fig. 5.1. Three-loads measurement setup.

5.1.2 Three-ports method

This procedure consists in soldering 2 coaxial cables with SMA connectors to the two output ports, as reported in Fig. 5.2. Then, three different measurements

are performed by closing in turn the free port on the 50-Ω broadband load. Because of the presence of the additional coaxial cables and the SMA connectors, port extension has to be properly applied to the network analyzer before performing the measurements [3]. Since the data collected are redundant, it can be recommended to check the consistency of the measurements by simply considering the structure symmetry. The resulting scattering matrix S^{nw} can be reduced to a more handful 2-port structure by using the following expression

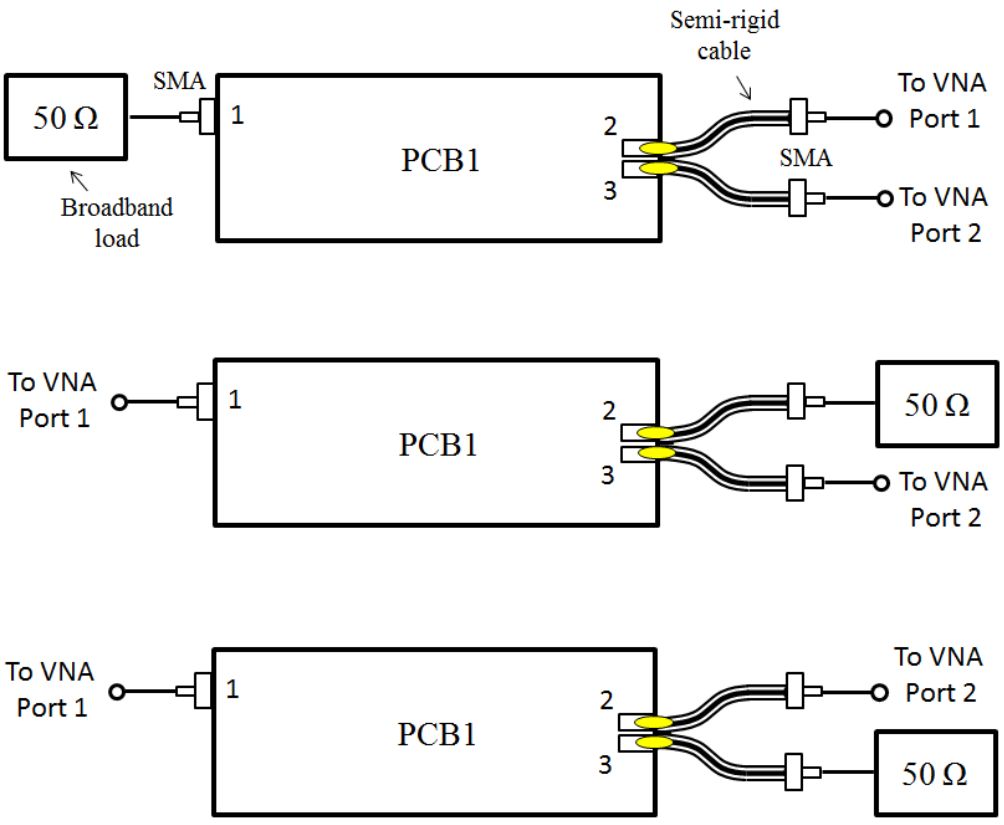

Fig. 5.2. Three-ports measurement setup.

$$S^{diff} = \begin{bmatrix} S_{11} & S_{1d2} \\ S_{d21} & S_{d2d2} \end{bmatrix} = \begin{bmatrix} S_{11}{}^{nw} & \frac{1}{\sqrt{2}}\left(S_{12}{}^{nw} - S_{13}{}^{nw}\right) \\ \frac{1}{\sqrt{2}}\left(S_{21}{}^{nw} - S_{31}{}^{nw}\right) & \frac{1}{\sqrt{2}}\left(S_{22}{}^{nw} + S_{33}{}^{nw} - S_{32}{}^{nw} - S_{23}{}^{nw}\right) \end{bmatrix} \quad (5.2)$$

in which the behavior of the passive network has been defined in term of a single ended signal (input port 1) and a differential signal (ports 2 and 3), thus neglecting the common mode component [4].

The behavior of the DUT impedance is directly available by using the expression

$$\Gamma_{sma}(f_0, P_{sma}) = S_{11} + \frac{S_{1d2} \cdot S_{d21} \cdot \Gamma_{in}}{1 - S_{d2d2} \cdot \Gamma_{in}} \quad (5.3)$$

which describes the input return loss as a function of the scattering matrix and the DUT load itself. Thus, Γ_{in} (and the DUT impedance Z_{in} as a consequence) can be easily obtained.

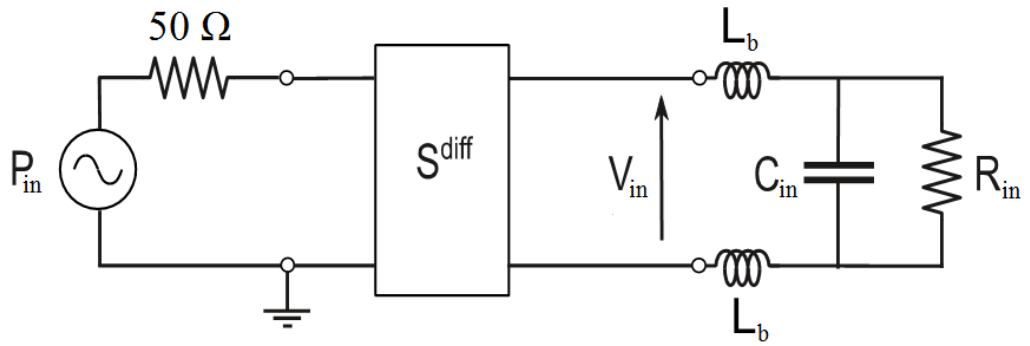

Fig. 5.3. Scheme of the rectifier measurement setup.

As far as the DUT efficiency η_R determination is concerned, it is necessary to calculate the input power P_{in} that is effectively available for the rectifier, by

taking into account the losses due to the matching network. By using the data collected, it is possible to model and simulate the structure as reported in Fig. 5.3. In particular, the DUT is represented by a parallel RC network that models the active circuitry at the operating frequency. An additional series inductance L_b, instead, represents the wire bonding. The RLC values are typically chosen to fit as much as possible the measured return loss Γ_{sma} in proximity of the operating frequency f_0. For each level of input power P_{in}, the R_{in} value has to be re-calculated without significantly changing the inductance and capacitance values.

By referring to Fig. 5.3, the incident power P_{in} can be calculated with the following expression

$$P_{in} = \frac{V_{in}^{\ 2}}{2R_{in}} \tag{5.4}$$

In Fig. 5.4 and Fig. 5.5, we report the behavior of the DUT power efficiency η_R and input resistance R_{in} as a function of the effective input power P_{in}. The capacitance C_{in} is around 352 fF, whereas the bonding inductance L_b is 3 nH, as derived from full-wave electromagnetic simulations.

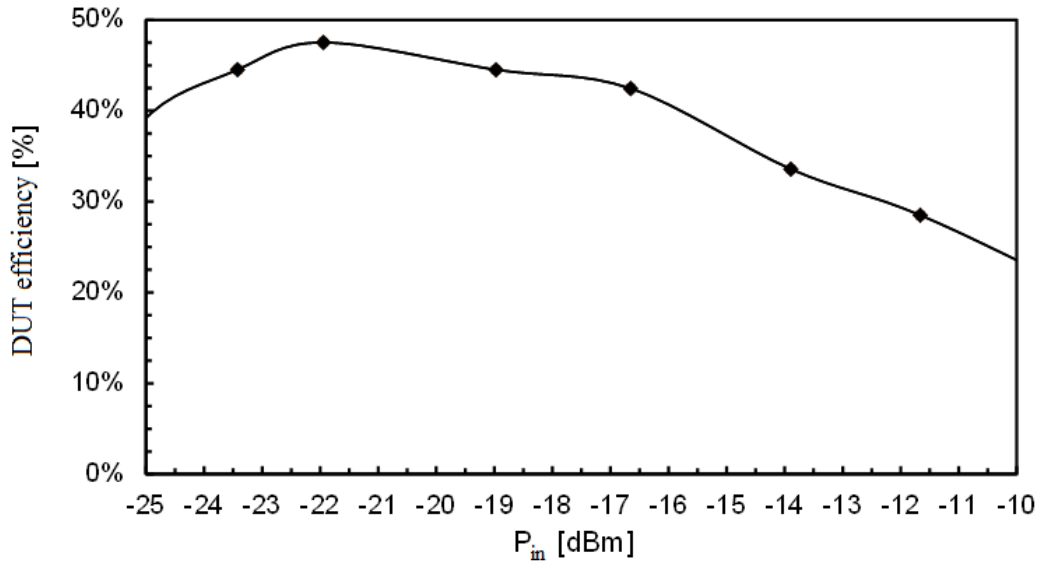

Fig. 5.4. Calculated efficiency η_R as a function of P_{in}.

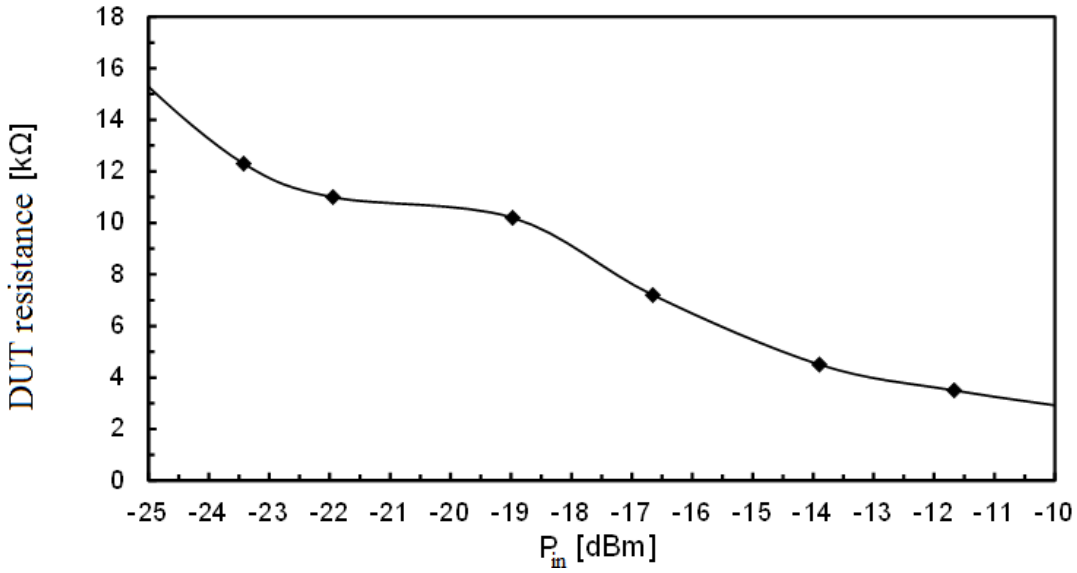

Fig. 5.5. Calculated resistance R_{in} as a function of P_{in}.

5.2 Antenna measurement methods

5.2.1 Impedance measurement

Most of the applications concerning RF harvesting systems – as RFID tags – relate to balanced antennas. Since measurement instruments usually exhibit unbalanced ports, a proper measurement method is needed.

The simplest method consists in using a balun, which forces equal currents to flow in each antenna terminal, as shown in Fig. 5.6. However, the antenna measurement accuracy is strongly affected by the balun itself.

In order to avoid using balun, half part of the antenna can be soldered on a ground plane, as shown in Fig. 5.7. This provides a mirror imaging of the other counterpart, thus obtaining the measured impedance by considering 2-times the value provided by the unbalanced port [5]. Unfortunately, the mirror imaging depends on the ground plane used, thus affecting the measurement accuracy.

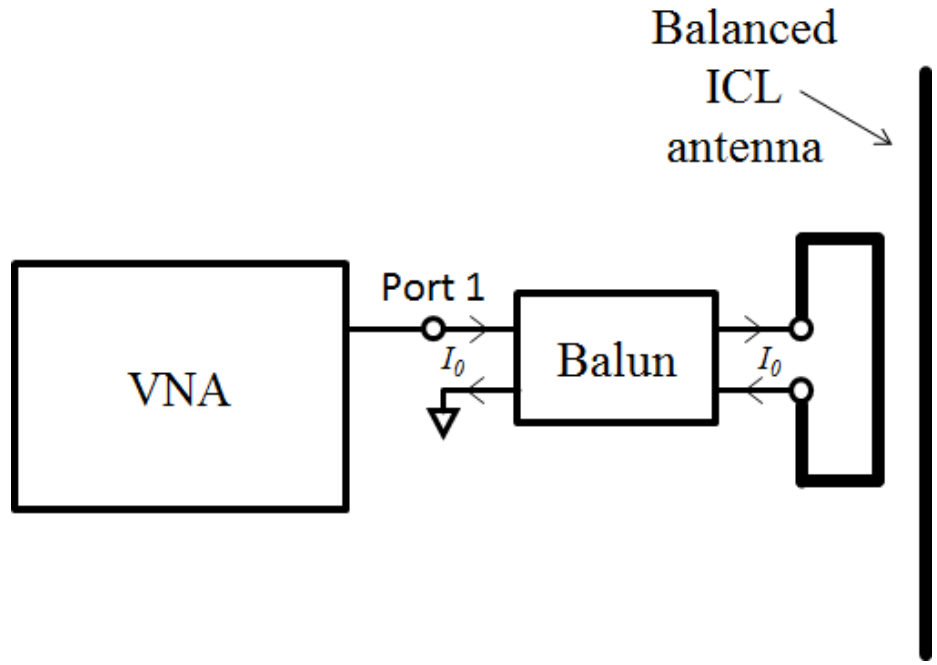

Fig. 5.6. Measurement setup with balun.

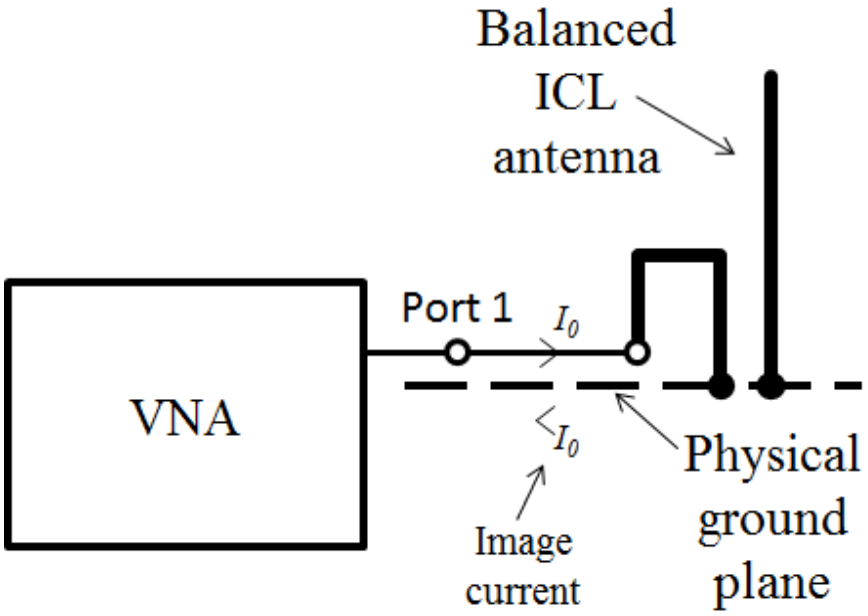

Fig. 5.7. Half antenna soldered on a ground plane.

In recent years, to overcome the previous problems, S-parameter-based method has been adopted [6]. This approach relies on a common two-port vector network analyzer (VNA). Since the test cables of the VNA have to be connected to the antenna terminals, a particular text fixture is needed, which is shown in Fig. 5.8. This fixture, which is commonly called "jig", usually consists in two semi-rigid cables whose outer conductors are soldered together. The inner conductor of each cable, instead, is connected to the test cable through an SMA connector to one end, while the other end is directly connected to the antenna terminal. The measurement setup is shown in Fig. 5.9.

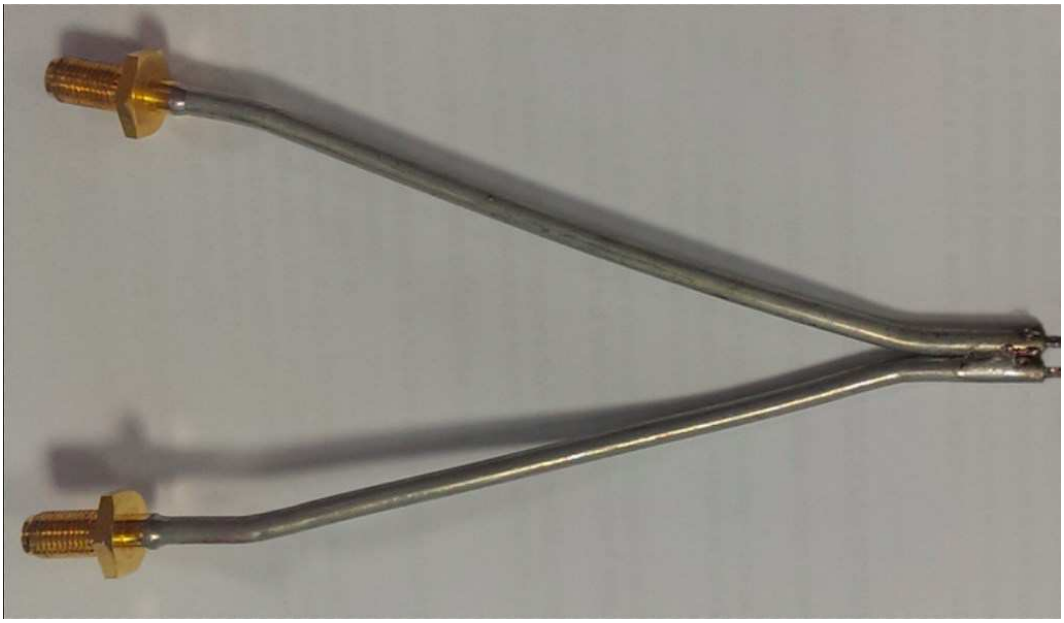

Fig. 5.8. Test fixture (jig) adopted within the measurement setup.

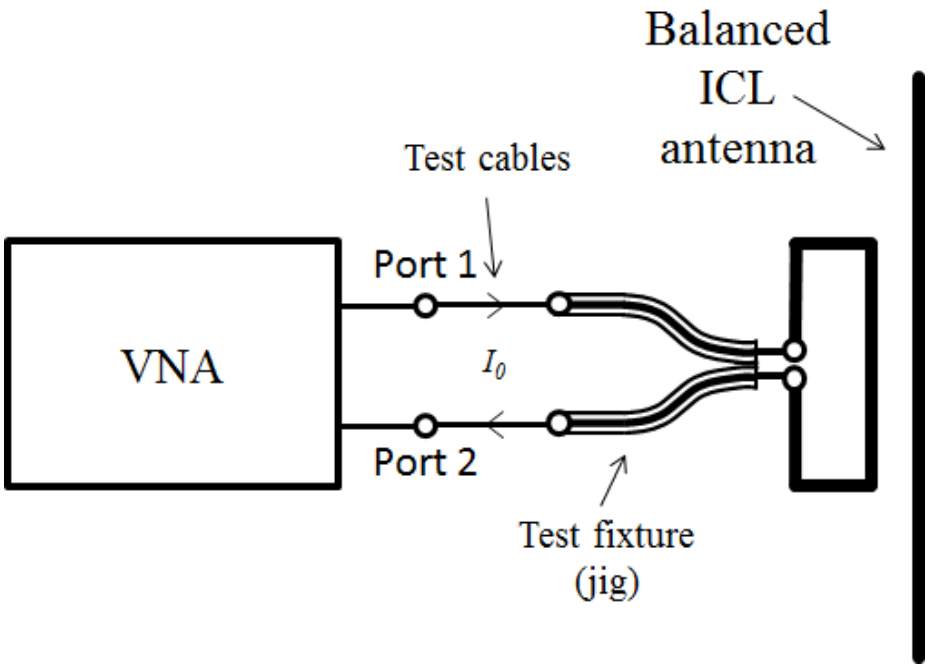

Fig. 5.9. Measurement setup with jig.

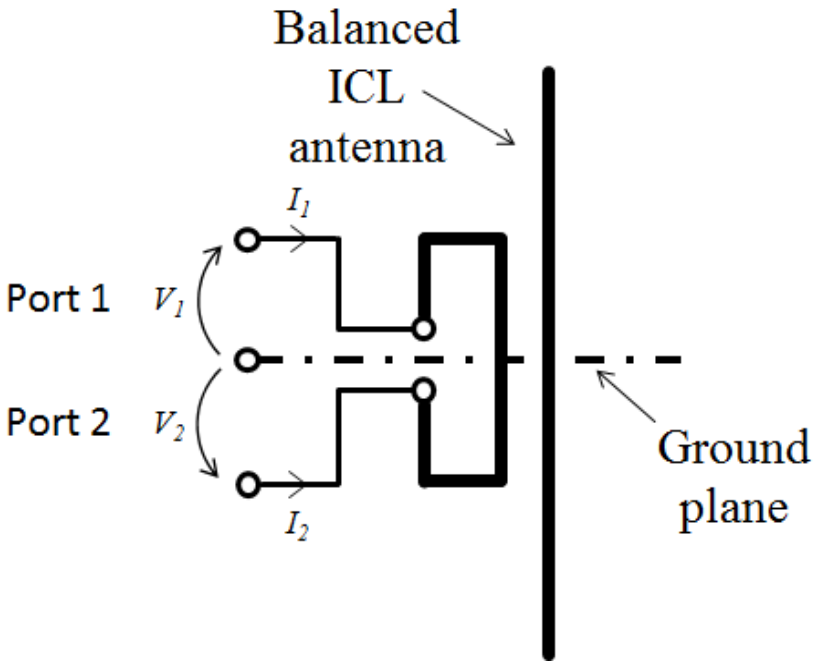

Fig. 5.10. Two-port network representation of the ICL antenna.

By referring to Fig. 5.10, the antenna can be seen as a two-port network. The S-parameters can be arranged to obtain the normalized impedance of the antenna, that is

$$Z_a = \frac{2Z_0\left(1 - S_{11}S_{22} + S_{12}S_{21} - S_{12} - S_{21}\right)}{\left(1 - S_{11}\right)\left(1 - S_{22}\right) - S_{21}S_{12}} \tag{5.5}$$

However, since the S-parameters provided by the VNA depend on the jig, a de-embedding procedure is needed. This can be simply achieved by using the port-extension function of the VNA [3]. By referring to Fig. 5.9, the calibration plane properly shifts to the tips of the fixture, thus de-embedding the influence of the semi-rigid cables. The fixture has to be open (or short) circuited before measuring S-parameters of the jig-antenna element. If port-extension function is not allowed in the VNA, the de-embedding process can be manually achieved by following the instruction depicted in Appendix B [7].

5.2.2 Efficiency measurement

Radiation efficiency measurement easily provides a large amount of errors if measurement method and setup are not properly carried out. Two main methods were taken into account in the last decade: directivity/gain and Wheeler cap.

The directivity/gain method relies on the following expression [8]

$$\eta_A = \frac{G_{real}}{\tau D} \tag{5.6}$$

where G_{real} is the maximum realized gain, τ is the power transfer coefficient and D is the maximum directivity. Thus, this method needs three different measurements in order to derive η_A. In particular, directivity D can only be obtained by approximation, once the E-plane power pattern is measured [9]. This results in lowering the accuracy of η_A.

On the other hand, the Wheeler cap method gives better accuracy, but a metallic cap has to be properly designed. Indeed, the antenna efficiency is estimated by measuring the antenna resistance in free space and Wheeler cap conditions, where the latter means measuring the antenna impedance by placing the antenna inside a cylindrical cavity [10]. Since the antenna resistance

$$R_a = R_l + R_r \tag{5.7}$$

depends on losses (R_l) and radiation (R_r), the metallic cap allows to derive R_l by blocking the radiation. Therefore, being R_{fs} the resistance obtained in free space condition and R_{wh} the one obtained with the Wheeler cap, the antenna efficiency can be derived as follows

$$\eta_A = \frac{R_r}{R_l + R_r} = \frac{R_{fs} + R_{wh}}{R_{fs}} \tag{5.8}$$

As previously said, sizing the Wheeler cap is a crucial aspect of this measurement method. In fact, if the distance between antenna and cap walls is lower than

$$d_{min} = \frac{\lambda}{2\pi} \tag{5.9}$$

the near field distribution results affected by the Wheeler cap. On the other hand, the bigger is the Wheeler cap, the higher is the number of resonant frequencies inside the cap, thus increasing the probability of having a resonant frequency lying near our operating frequency.

Fig. 5.11 shows the cylindrical cavity acting as a Wheeler cap within this project, in which two holes are cut out from the base to connect the test cables to the jig. This allows us to obtain the loss resistance R_l with the impedance measurement method previously explained. Dimensions a and h represent the radius and the height of the Wheeler cap, respectively. These values have to be high enough to satisfy the minimum distance d_{min} calculated in (5.9).

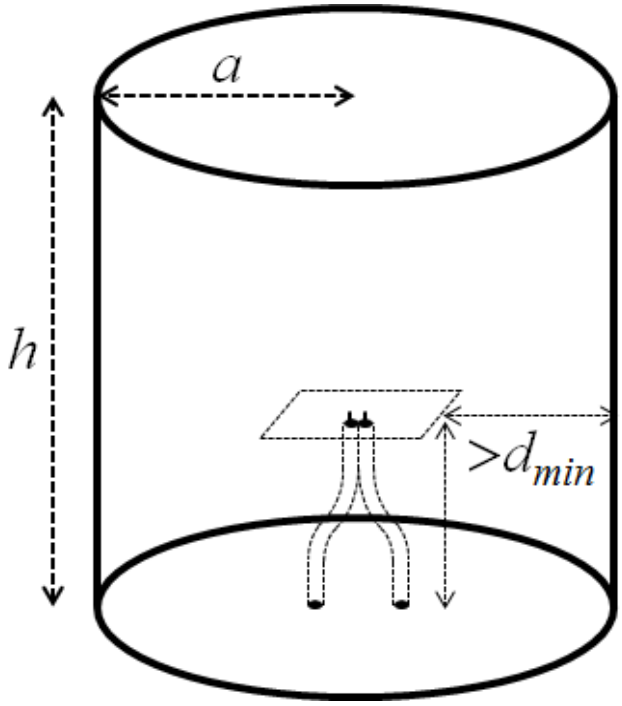

Fig. 5.11. Cylindrical cavity used as Wheeler cap.

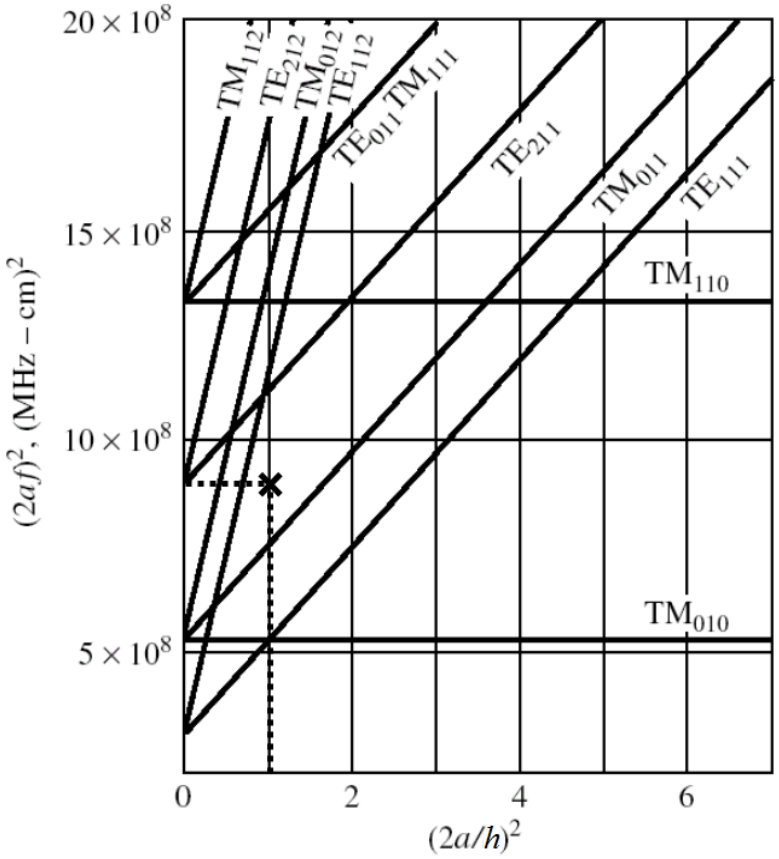

Fig. 5.12. Resonant mode chart for the cylindrical cavity in Fig. 5.11.

Then, by referring to the resonant mode chart for a cylindrical cavity in Fig. 5.12, *a* and *h* have to be fixed by choosing a point in the map. This point has to be far away from the modes represented by solid lines. However, we are not allowed to refer to the area of the map in which expression (5.9) is not satisfied. In particular, the following expressions have to be taken into account

$$a > \frac{x_{sub}}{2} + d_{min} \tag{5.10}$$

$$h > t_{sub} + 2d_{min} \approx 2d_{min} \tag{5.11}$$

where x_{sub} and t_{sub} are the base and the thickness of the antenna substrate, respectively.

Thus, a point in the map was chosen, which is represented as a cross in Fig. 5.12. By considering an operating frequency of 868 MHz, it results

$$r = \frac{\sqrt{9 \times 10^8}}{2f} \approx 17.3\,\text{cm} \tag{5.11}$$

$$h = 2r = 34.6\,\text{cm} \tag{5.12}$$

Additional driven modal simulations were carried out to check that sizing given in (5.11) and (5.12) is consistent with the mode chart shown in Fig. 5.12.

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Chapter VI

Experimental results

A harvesting system consisting in a 10-stage CMOS differential-drive rectifier with an inductively coupled loop antenna was implemented. It was designed to meet the same output specification of the system in [1], which adopted a threshold-compensated rectifier based on the Dickson approach. These specifications coincide with design C drawn up in chapter V.

6.1 Rectifier

The differential-drive rectifier with the proposed body-voltage control was implemented in a 0.13-μm CMOS technology by *STMicroelectronics*. A core die microphotograph is shown in Fig. 6.1, where the dc output pad is not apparent since it is far from the rectifier core within the MPW chip. The harvesting system was designed to perform a 20-MHz bandwidth to take into account frequency deviations due to process tolerances. This lead to a maximum allowable quality factor $Q_{L,max}$ of 30.

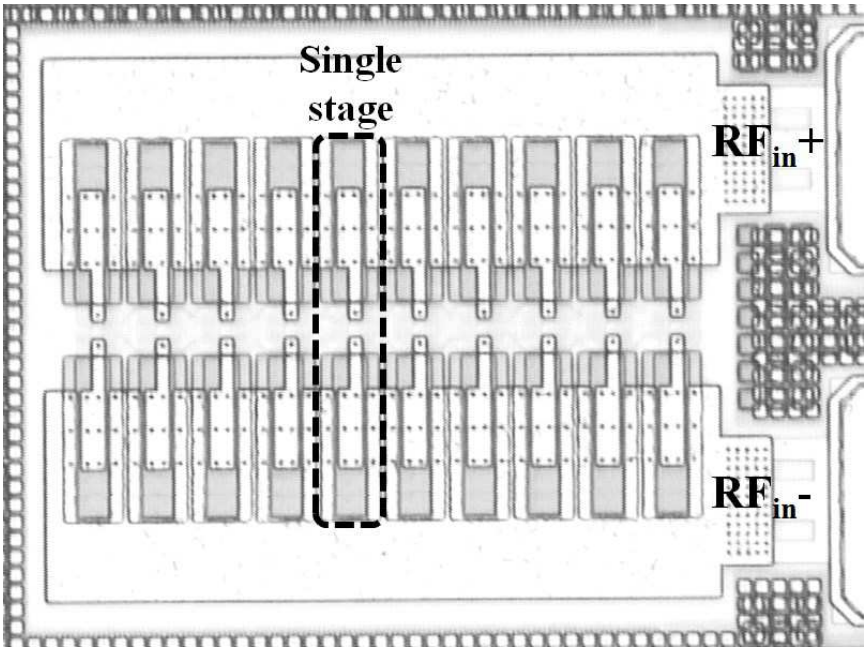

Fig. 6.1. Die microphotograph of the proposed rectifier.

The aspect ratios of n-type and p-type transistors were set to 2 μm/130 nm and 8 μm/130 nm, respectively, whereas the pump capacitor, C_p, was set to 600 fF. The n-type transistors of the first two stages and the p-type transistors of the last stage were connected to ground and output, respectively. The circuit ideally reaches its peak efficiency with i=1 and j=−2.

Fig. 6.2 shows the measured and post-layout efficiency of the rectifier versus the available input power, P_{AV}, along with output voltage V_L (I_L=1 μA). P_{in} is equal to P_{AV} only at sensitivity, where impedance matching is provided. A maximum efficiency of 43% when V_L of 2.4 V is achieved with a sensitivity of -22.5 dBm. De-embedded measurements give a rectifier input resistance R_{in} and capacitance C_{in} around 15.2 kΩ and 350 fF, respectively. C_{in} also accounts for a pad capacitance around 80 fF.

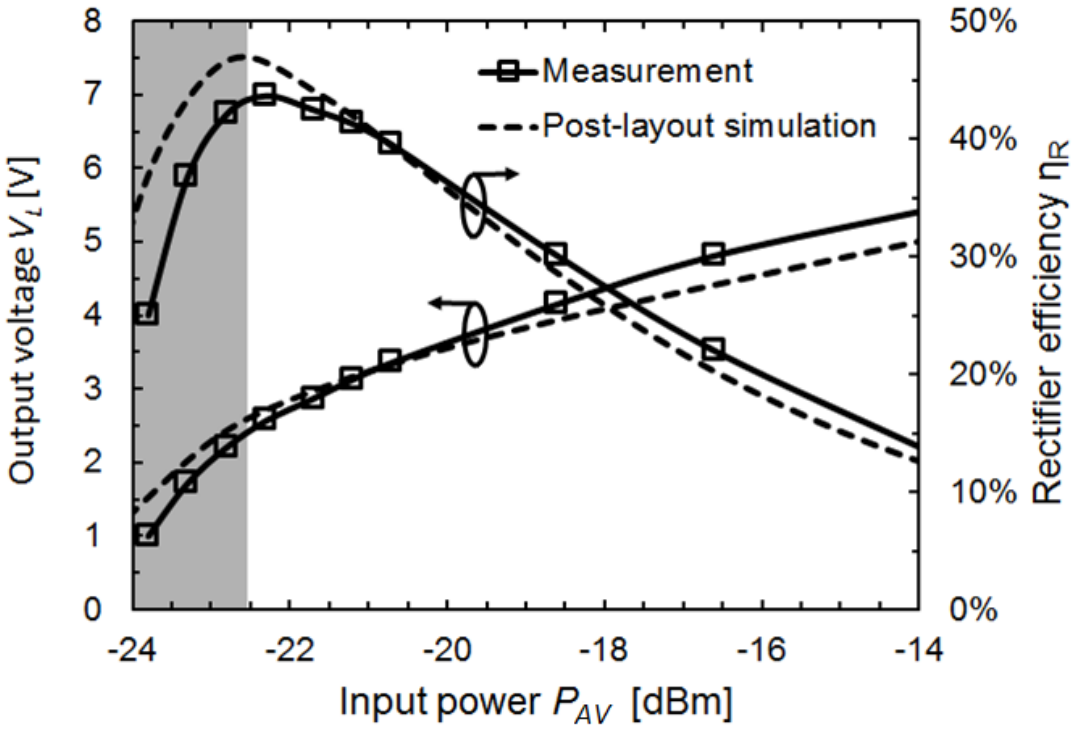

Fig. 6.2. Measured and post-layout efficiency η_R and output voltage V_L versus available input power P_{AV}.

6.2 Antenna

An ICL antenna was designed on a low cost FR-4 substrate. Antenna loop distance and perimeter were set to 1.8 mm and 8.4 cm, respectively, according to rectifier impedance. A photograph of the fabricated ICL antenna is shown in Fig. 6.3.

Fig. 6.4, Fig. 6.5 and Fig. 6.6 show simulations and measurements of the antenna output impedance and efficiency. Around the operating frequency, reactance and efficiency accurately match, whereas a little discrepancy exists between expected and measured resistance. The measurement setup for the efficiency estimation is shown in Fig. 6.7.

Fig. 6.3. Photograph of the fabricated ICL antenna.

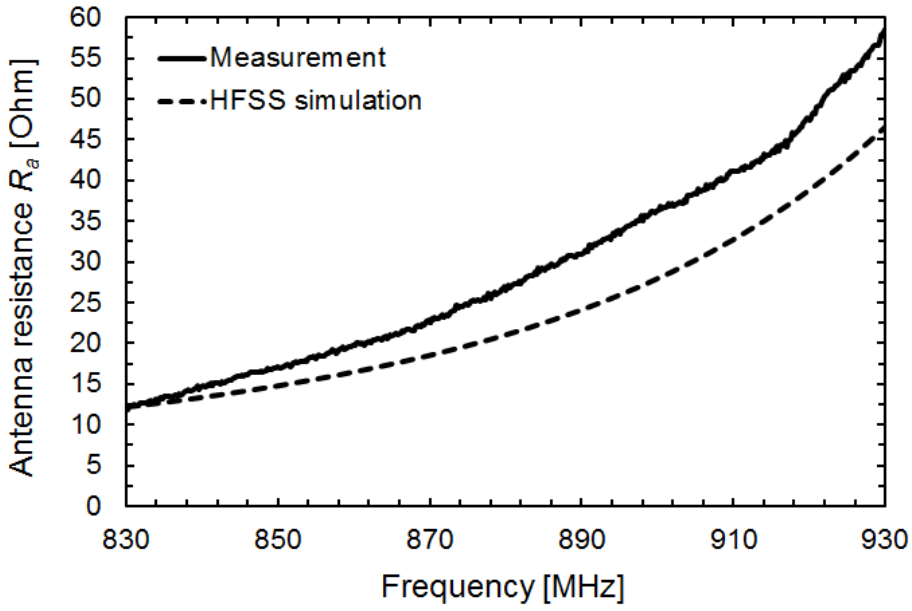

Fig. 6.4. Measured and simulated resistance R_a of the proposed ICL antenna versus frequency.

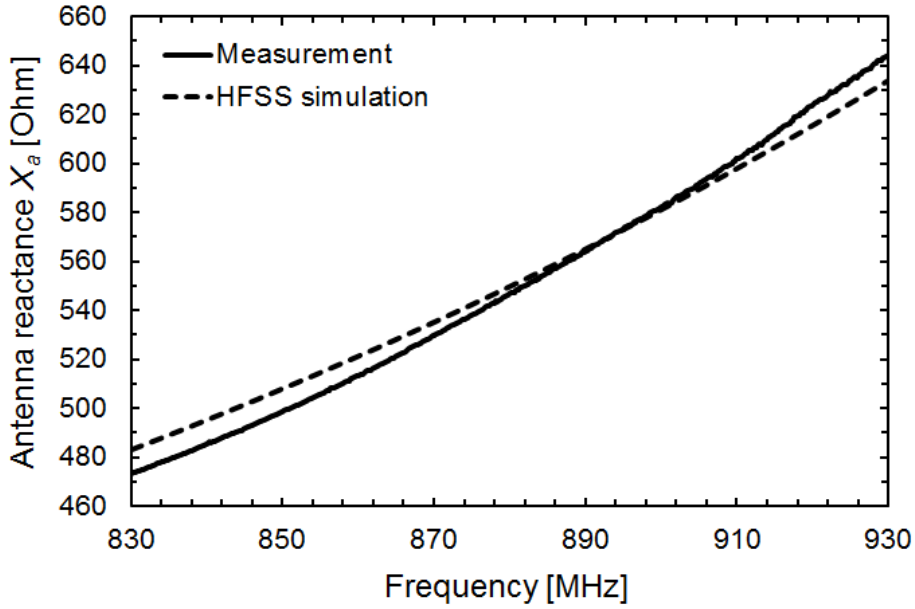

Fig. 6.5. Measured and simulated reactance X_a of the proposed ICL antenna versus frequency.

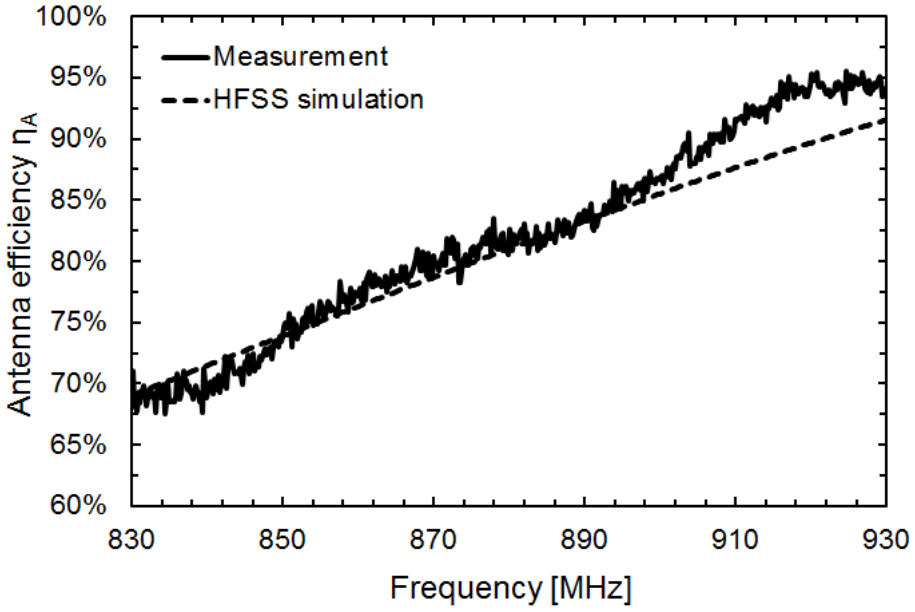

Fig. 6.6. Measured and simulated efficiency η_A of the proposed ICL antenna versus frequency.

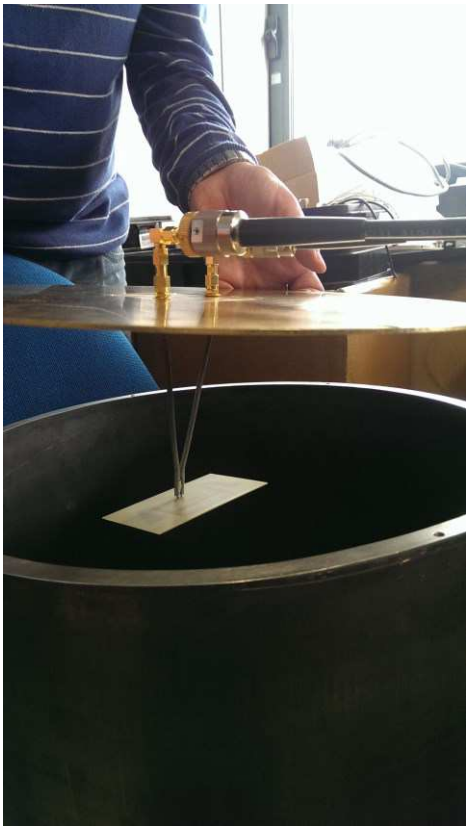

Fig. 6.7. Antenna efficiency estimation with the Wheeler cap method.

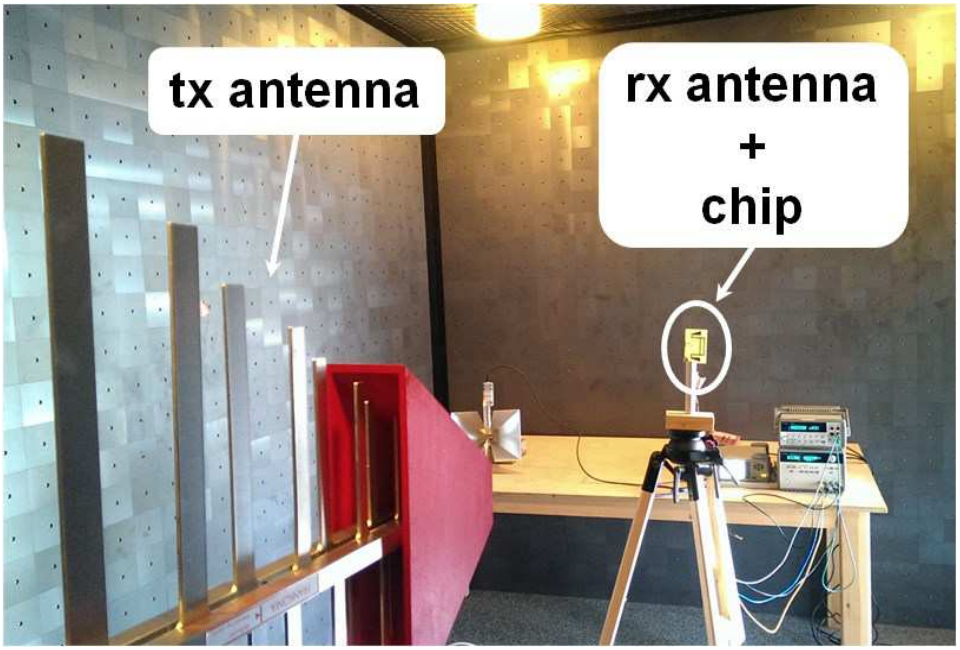

Fig. 6.8. Measurement setup into the anechoic chamber.

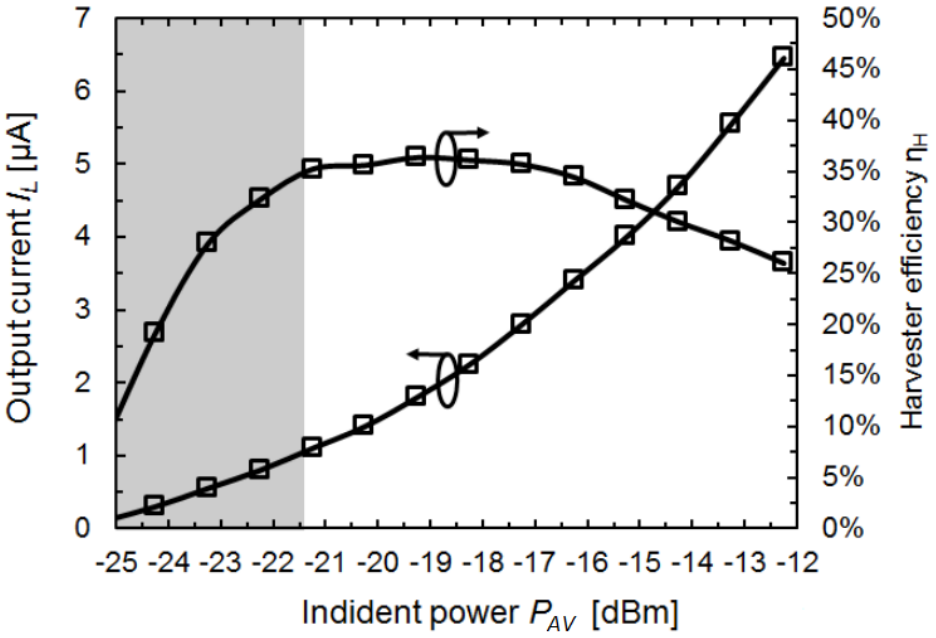

Fig. 6.9. Measured efficiency η_H and output current I_L versus incident power P_{AV} of the proposed harvesting system, with V_L = 2.4 V.

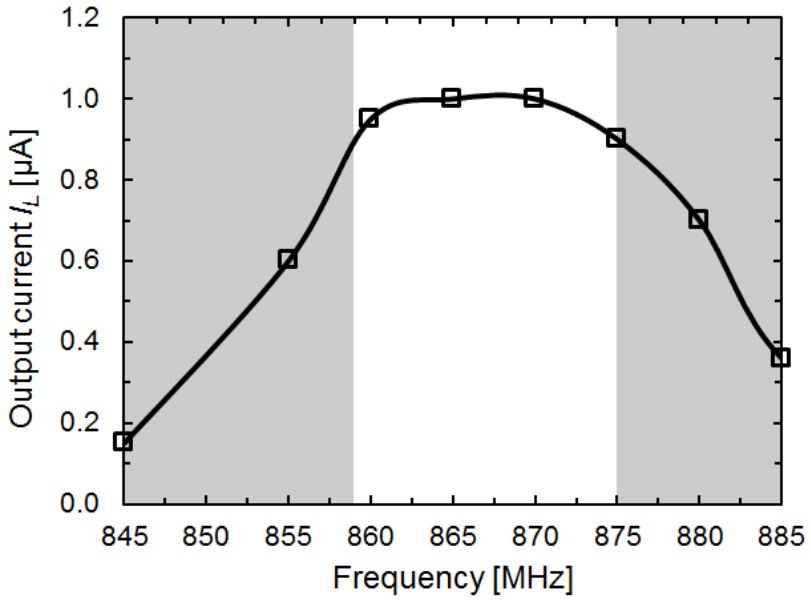

Fig. 6.10.Measured output current I_L versus frequency of the proposed harvesting system, with V_L = 2.4 V.

6.3 Overall system

The chip was connected via bonding to the antenna input terminals. The harvesting system was characterized into an anechoic chamber by properly transmitting power through a tx antenna and then deriving the available input power with a properly calibrated rx antenna. The measurement system is shown in Fig. 6.8.

Fig. 6.9 shows the overall harvester performance in terms of output current I_L and efficiency η_H as a function of available input power P_{AV} by fixing V_L to 2.4 V. With the target load current of 1 μA, the measured efficiency and sensitivity are 34 % and -21.5 dBm, respectively, at the operating frequency of 868 MHz. Moreover, an output current above 0.9 μA is delivered in a frequency bandwidth of 16 MHz, as shown in Fig. 6.10. It is worth nothing that the proposed design procedure allows maximum efficiency to be achieved at sensitivity level as shown in Fig. 6.2 and Fig. 6.9.

A comparison of the proposed harvesting system with most significant state-of-the-art solutions is shown in Table 6.1, in which each performance has been chosen to deliver almost the same output power level. This work shows an output power P_L greater than or equal to the other works, with the highest efficiency η_H. Although the system in [2] performs the same P_L with a comparable sensitivity, a lower output voltage V_L is delivered.

Table 6.1. Comparison between experimental results of the proposed harvesting system with the state-of-the-art solutions.

Reference	**This work**	**JSSC 2014 [2]***	**TCAS-I 2013 [3]**	**JSSC 2008 [4]***	**TCAS-I 2007 [5]**
CMOS technology	0.13 µm	90 nm	0.13 µm	0.25 µm	0.18 µm
Operating frequency	868 MHz	868 MHz	900 MHz	906 MHz	950 MHz
Overall efficiency η_H	34 %	25 %	9.1 %	8.7 %	23.5 %
Sensitivity	–21.5 dBm	-20 dBm	-19.3 dBm	-16 dBm	–20.7 dBm
Output power P_L (voltage V_L)	2.4 µW (2.4 V)	2.4 uW (1.6 V)	1.1 uW (1.15 V)	2.2 µW (3.5 V)	2 µW (0.5 V)

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Conclusions

Wireless sensor networks (WSNs) based on batteryless nodes have been attracting an increasing attention in the scientific and industrial communities, thanks to their interesting features to be a very low cost and free-of-maintenance network solutions. Energy to replace battery can be extracted from environmental sources such as vibration, solar, thermal, or provided by RF carrier of a power transmitter. The advantage of RF over other harvesting approaches lies in the full controllable operation that is independent from environmental conditions. On the other hand, RF harvesting suffers from a low operating distance due to the propagation loss and the relatively low harvester sensitivity.

An effective co-design approach for harvesting systems is described, which is based on a CMOS differential-drive rectifier and an inductively coupled loop (ICL) antenna. The proposed methodology acts on both rectifier and antenna, and aims at optimizing system performance in terms of efficiency and input sensitivity for a given load specification. Moreover, a rectifier solution is also proposed to enhance circuit performance by properly driving transistor bulks without additional components. An RF harvesting system operating at 868 MHz was implemented, which is made up of an ICL antenna on FR-4 substrate and a rectifier fabricated in a 0.13-μm CMOS technology. Measurements in the

anechoic chamber show an overall efficiency performance of 34% with an RF input power as low as –21.5 dBm, while considering 2.4 V and 1 μA as load specification.

Appendix

Appendix A

By referring to Fig. 5.1, the expression (5.3) regarding the return loss at the SMA level can also be written as

$$\Gamma_{sma} = \frac{a \cdot \Gamma_{in} + b}{1 + c \cdot \Gamma_{in}} \tag{A.1}$$

The coefficients a, b and c depend on the S-parameters of the impedance matching network. In particular

$$a = S_{21}S_{12} - S_{11}S_{22} \tag{A.2}$$

$$b = S_{11} \tag{A.3}$$

$$c = -S_{22} \tag{A.4}$$

If the DUT is substituted in turn with three characterized loads, the following return losses can be measured

$$\Gamma_{sma,1} = \frac{a \cdot \Gamma_{in,1} + b}{1 + c \cdot \Gamma_{in,1}} \tag{A.5}$$

$$\Gamma_{sma,2} = \frac{a \cdot \Gamma_{in,2} + b}{1 + c \cdot \Gamma_{in,2}} \tag{A.6}$$

$$\Gamma_{sma,3} = \frac{a \cdot \Gamma_{in,3} + b}{1 + c \cdot \Gamma_{in,3}} \tag{A.7}$$

Since are $\Gamma_{sma,1}$, $\Gamma_{sma,2}$ and $\Gamma_{sma,3}$ are known, coefficients *a*, *b* and *c* can be derived by solving the following matrix equation

$$\begin{bmatrix} \Gamma_{in,1} & 1 & -\Gamma_{in,1}\Gamma_{sma,1} \\ \Gamma_{in,2} & 1 & -\Gamma_{in,2}\Gamma_{sma,2} \\ \Gamma_{in,3} & 1 & -\Gamma_{in,3}\Gamma_{sma,3} \end{bmatrix} \begin{bmatrix} a \\ b \\ c \end{bmatrix} = \begin{bmatrix} \Gamma_{sma,1} \\ \Gamma_{sma,2} \\ \Gamma_{sma,3} \end{bmatrix} \tag{A.8}$$

thus obtaining the S-matrix through the expressions (A.2), (A.3) and (A.4).

Appendix B

By referring to Fig. 5.10 and Fig. 5.11, an equivalent block diagram is shown in Fig. A.1. The aim of the port-extension technique is to de-embed the effect of the jig on the VNA measurement, which means removing the cascade matrices J^{sx} and J^{dx} from the cascade matrix A^j, in order to obtain the antenna cascade matrix A. In fact, A^j represents the matrix effectively derived by VNA measurement, after SOLT calibrations have been performed, thus being affected by the jig.

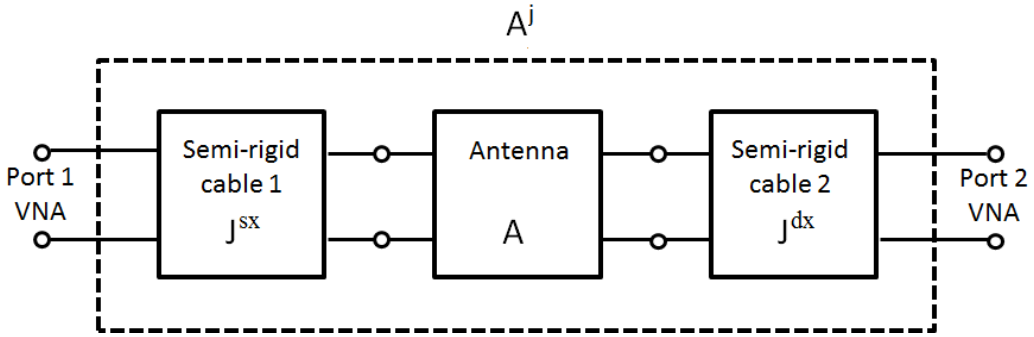

Fig. A.1. Block diagram of the system jig-antenna shown in Fig. 5.10.

As a first step, open-correction method is adopted for deriving matrices J^{sx} and J^{dx}. In fact, short-correction method would require soldering together the inner conductors of the semi-rigid cables. When the semi-rigid cable 1 is terminated in a generic load Z_L, its input impedance can be given by

$$Z^{sx} = Z_0 \frac{Z_L + Z_0 \tanh \beta_1}{Z_0 + Z_L \tanh \beta_1} \tag{B.1}$$

where Z_0 is the characteristic impedance. Since $Z_L = \infty$ in the open-correction method, the input impedance in (A.1) becomes

$$Z_0^{sx} = \frac{Z_0}{\tanh \beta_1} \tag{B.2}$$

Thus, $\tanh\beta_1$ can be easily derived. Then, by combining (B.2) with the following expression

$$\cosh^2 \beta_1 - \sinh^2 \beta_1 = 1 \tag{B.3}$$

the cascade matrix J^{sx} can be obtained as follows

$$J^{sx} = \begin{bmatrix} \cosh \beta_1 & \sinh \beta_1 \\ \sinh \beta_1 & \cosh \beta_1 \end{bmatrix} \tag{B.4}$$

The matrix J^{dx}, which regards the semi-rigid cable 2, is derived as J^{sx}.

Being S_{ij} the s-parameters derived from the VNA at the calibration plane, the matrix A^j can be expressed as follows

$$A^j = \begin{bmatrix} \frac{(1+S_{11})(1-S_{22})+S_{12}S_{21}}{2S_{21}} & \frac{(1+S_{11})(1+S_{22})-S_{12}S_{21}}{2S_{21}} \\ \frac{(1-S_{11})(1-S_{22})-S_{12}S_{21}}{2S_{21}} & \frac{(1-S_{11})(1+S_{22})+S_{12}S_{21}}{2S_{21}} \end{bmatrix} \tag{B.5}$$

Thus, the cascade matrix A can be derived from

$$A = J^{sx^{-1}} A^{j} J^{dx^{-1}} \tag{B.6}$$

Finally, the antenna input impedance is given by

$$Z_{in} = \frac{A_{11} + A_{22} + A_{12}A_{21} - A_{11}A_{22} - 1}{A_{21}} \tag{B.7}$$