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# Transformer-Based VCO for W-Band Automotive Radar Applications

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**Abstract:** A transformer-based voltage-controlled oscillator for a W-band frequency-modulated continuous-wave (FMCW) automotive radar application is presented. The design challenges imposed by the millimeter-wave frequency operation were faced through a circuit and layout co-design approach, supported by extensive electromagnetic simulations and accurate analysis of both the start-up condition and the tank quality factor. The oscillator was implemented in a 28-nm fully depleted silicon-on-insulator (SOI) complementary metal–oxide–semiconductor (CMOS) technology. It provided a 37 GHz oscillation frequency with a variation of around 4 GHz, thus achieving a tuning range of 11%. Moreover, a 77 GHz output signal was also delivered, which was extracted as a second harmonic from the input-pair common-mode node. The circuit exhibited low phase noises, whose average performances were  $-97$  dBc/Hz and  $-121$  dBc/Hz at 1 MHz and 10 MHz offset frequencies, respectively. It delivered a 77-GHz output power of  $-10.5$  dBm and dissipated 26 mW with a 1 V power supply. The silicon area occupation was  $300 \times 135 \mu\text{m}$ .

**Keywords:** automotive radar sensor; CMOS oscillator; electromagnetic simulations; FD-SOI CMOS technology; integrated transformers; millimeter-wave PLL; quality factor; transformer-based VCO



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## 1. Introduction

Long- and short-range sensing techniques have experienced strong development in recent years thanks to the growing interest expressed for them by the automotive industry. Presently, the implementation of the most common functions of an advanced driver assistance system (ADAS) for safety and security involves several kinds of sensors, such as light detection and ranging (LIDAR), camera, ultrasound, and millimeter-wave (mm-wave) radar. Among them, mm-wave radar sensors, which are mostly based on the frequency-modulated continuous-wave (FMCW) technique, have gained high interest due to their low size and robustness against environmental influences. Nowadays, complementary metal–oxide–semiconductor (CMOS) technologies with a low power supply and a high integration level that enables system-on-chip (SoC) solutions are the most promising candidates for low-cost mm-wave radar integrated circuits.

A common ADAS implementation involves radar sensors with different resolutions and operating distance requirements. To meet them while constraining the whole system cost, multimode radar solutions are preferred. They can support both long-range radar (LRR; from 76 to 77 GHz) and short-range radar (SRR; from 77 to 81 GHz) operation modes, thus avoiding the need for different radar devices. A multimode radar needs a frequency synthesizer with a wide frequency tuning range and high spectral purity to enable high-resolution sensing for short-range operation and accurate detection of low-level reflected signals for long-range operation, respectively. Specifically, modern radar sensors must be able to guarantee an operating distance ranging from a few meters to

about 250 m with a resolution better than 5 cm during short-range operation. This calls for a frequency synthesizer with a tuning range wider than 3 GHz and a phase noise better than  $-90$  dBc/Hz with a 1 MHz offset frequency [1,2].

In a voltage-controlled oscillator (VCO)-based frequency synthesizer, these requirements are largely determined by the VCO itself, which is one of the most critical building blocks in an integrated mm-wave radar transceiver. In truth, when designing a VCO, stringent tradeoffs between various performance parameters must be considered, such as the phase noise (PN), frequency tuning range (TR), start-up robustness, power consumption, and area. The design of VCOs that are capable of simultaneously achieving a low PN and a wide TR is a very challenging task, especially at mm-wave frequencies. Indeed, as the VCO oscillation frequency increases, the quality factor of passive components (capacitors, inductors, and varactors) decreases, with a negative impact on both the PN and power consumption. In addition, the need for larger transistors to support the oscillation and the consequent larger interconnection area give rise to heavy parasitic capacitance contributions, which greatly impact the TR, especially when a low supply voltage is used. Therefore, W-band CMOS VCOs exhibit a poor trade-off between PN and TR performance [1,3].

To partially overcome these limitations, a VCO followed by a frequency multiplier is used to produce the operating frequency [2,4]. By setting the VCO oscillation frequency to be much lower than the required operating frequency, it allows for passive components with a higher quality factor, thus guaranteeing a better PN/TR trade-off. Moreover, a VCO with a lower oscillation frequency simplifies the phase-locked loop (PLL) implementation since it relaxes the pre-scaler design and prevents the system from being affected by power amplifier (PA) pulling effects. For this purpose, a commonly adopted solution is to set the oscillation frequency at half the operating frequency (i.e., at around 38 GHz) and extract the second harmonic component from a common-mode node of the oscillator [5,6]. Moreover, transformer-based topologies can be profitably exploited at mm-wave frequencies since they show the advantage of a better PN, thanks to an enhanced resonator  $Q$ -factor, as is shown below. To increase the VCO tuning range, switched resonators (i.e., switched-capacitor or switched-inductor resonators) are used [7]. However, special care must be spent on the switch losses and parasitic capacitances, which could impact the resonator  $Q$ -factor and the tuning range, respectively. Moreover, most of these approaches introduce a delay in the frequency tuning, which is not compatible with an FMCW radar application.

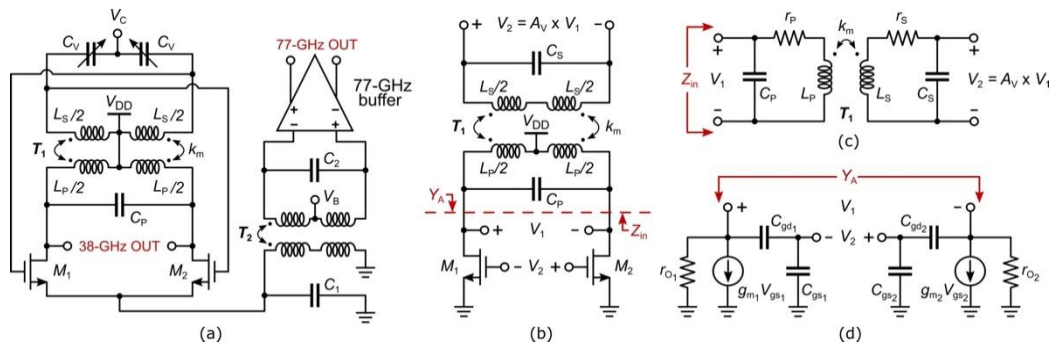
Several performance-enhancing techniques have been proposed in the literature in the last decade to improve the PN in the transformer-based VCO topology. Among them, waveform shaping using the second [8,9] and third [10,11] harmonic resonances in a harmonically tuned tank is the most interesting. Although these techniques can effectively improve the oscillator PN, their use at mm-wave frequencies is not so straightforward and does not always lead to reliable solutions.

In this paper, the design of a transformer-based VCO is presented, which was implemented in a 28-nm fully depleted silicon-on-insulator (FD-SOI) CMOS technology for W-band automotive radar applications. The paper is structured as follows. In Section 2, both the VCO start-up condition and the resonator  $Q$ -factor are analyzed with the aim of minimizing the PN while simultaneously guaranteeing a robust start-up. A design procedure for a mm-wave VCO and the details of the circuit implementation are discussed in Section 3. The measurements are presented in Section 4 and the conclusion follows in Section 5.

## 2. VCO Analysis

Figure 1a shows the schematic of the proposed VCO. It consists of a transformer-based topology with an oscillating core at 38 GHz. The resonator is built around the integrated transformer,  $T_1$ , which enhances the  $Q$ -factor and provides a positive feedback path from the drains to the gates of the cross-coupled differential pair,  $M_{1,2}$ . To compensate for the process, voltage and temperature (PVT) tuning reduction, the VCO was designed to cover about 4 GHz of frequency tuning range (37–41 GHz), which is higher than the nominal

tuning range of 2.5 GHz required by the radar application. Accumulation-MOS (A-MOS) varactors,  $C_V$ , and single-ended control voltage,  $V_C$ , were adopted.



**Figure 1.** (a) Simplified schematic of the proposed voltage-controlled oscillator (VCO). (b) Transformer-based VCO equivalent circuit. (c) Transformer-based tank. (d) Small-signal active core equivalent circuit.

As shown in Figure 1a, the 77-GHz signal is picked up at the common source node of  $M_{1,2}$  using transformer  $T_2$ , whose primary and secondary winding resonances are tuned at the second harmonic of the VCO oscillation frequency. This signal is applied to a buffer that delivers it to the output with the desired power level. Note that the resonance at the first coil of  $T_2$  provides a high-impedance path between the differential pair and ground at the second harmonic of the oscillation signal. This resonance prevents the differential pair from loading the tank when  $M_1$  or  $M_2$  are pushed into the triode region, thus avoiding PN degradation.

Finally, the 38-GHz VCO output that drives the PLL prescaler is drawn from the primary winding of transformer  $T_1$ .

### 2.1. Start-Up Condition

To analyze the start-up condition, the proposed VCO in Figure 1a can be replaced with the equivalent circuit in Figure 1b. Here, voltage  $V_2$  at the secondary side of  $T_1$  is equal to voltage  $V_1$  at the primary side multiplied by the voltage gain,  $A_V$ , provided by the transformer. Voltage  $V_2$  is also the voltage across the gates of transistors  $M_{1,2}$ . Therefore, the equivalent circuit in Figure 1b can be divided into the transformer-based tank and the active core, as shown in Figure 1c,d, respectively. The resistances  $r_P$  and  $r_S$  in Figure 1c account for the losses in the primary and secondary windings of  $T_1$ , whereas capacitors  $C_P$  and  $C_S$  include a resonant capacitor and the varactor at the primary and secondary winding, respectively, besides parasitic capacitance contributions at the gate and drain of the input pair. The MOS parameters in Figure 1d have the usual meaning.

The input impedance,  $Z_{in}$ , the transimpedance,  $Z_t$ , and the voltage gain,  $A_V$ , of this network are calculated in (1)–(3), respectively, for  $s = j\omega$ . They are fourth-order transfer functions with two pairs of complex conjugate poles, which account for the resonances at the primary and secondary windings. Assuming that the coupled inductors  $L_P$  and  $L_S$  have a sufficiently high quality factor at the operating frequency, i.e.,  $Q_P = \omega L_P / r_P \gg 1$  and  $Q_S = \omega L_S / r_S \gg 1$ , the two resonant frequencies can be written as in (4).

$$Z_{in}(s) = \frac{s^3[L_P L_S C_S (1 - k_m^2)] + s^2[C_S(L_S r_P + L_P r_S)] + s(L_P + r_S r_P C_S) + r_P}{s^4[L_P L_S C_P C_S (1 - k_m^2)] + s^3[C_P C_S(L_S r_P + L_P r_S)] + s^2(L_P C_P + L_S C_S + r_S r_P C_P C_S) + s(r_P C_P + r_S C_S) + 1} \quad (1)$$

$$Z_t(s) = \frac{sk_m \sqrt{L_P L_S}}{s^4[L_P L_S C_P C_S (1 - k_m^2)] + s^3[C_P C_S(L_S r_P + L_P r_S)] + s^2(L_P C_P + L_S C_S + r_S r_P C_P C_S) + s(r_P C_P + r_S C_S) + 1} \quad (2)$$

$$A_V(s) = \frac{V_2}{V_1} = \frac{Z_t(s)}{Z_{in}(s)} = \frac{sk_m \sqrt{L_P L_S}}{s^3[L_P L_S C_S (1 - k_m^2)] + s^2[C_S(L_S r_P + L_P r_S)] + s(L_P + r_S r_P C_S) + r_P} \quad (3)$$

$$\omega_{L,H}^2 = \frac{1 + \zeta \pm \sqrt{(1 + \zeta)^2 - 4\zeta(1 - k_m^2)}}{2(1 - k_m^2)} \omega_S^2, \tag{4}$$

where:

$$\zeta = \left(\frac{\omega_P}{\omega_S}\right)^2 = \frac{L_S C_S}{L_P C_P}, \tag{5}$$

and  $k_m$  is the magnetic coupling coefficient.

The transconductance that satisfies the start-up condition can be found by evaluating the small-signal admittance,  $Y_A$ , across the drain nodes of transistors  $M_{1,2}$ , as shown in Figure 1d. Considering the feedback provided by  $T_1$  that is expressed by gain  $A_V$ ,  $Y_A$  is given by:

$$Y_A(j\omega) = -\frac{g_m}{2} A_V + \frac{1}{2r_O} + j\omega \frac{C_{gd}}{2} (1 + A_V). \tag{6}$$

Equation (6) reveals that the equivalent transconductance of the differential pair is boosted by the transformer voltage gain. By evaluating (1) and (3) for  $s = j\omega$  and combining them with (6), the constraint on the couple pair transconductance,  $g_m$ , imposed by the start-up condition can be given as follows:

$$g_m > \frac{\omega}{\omega_P} \cdot \frac{\left[\left(\frac{\omega}{\omega_S}\right)^2 - 1\right] + \zeta \left[\left(\frac{\omega}{\omega_P}\right)^2 - 1\right] \frac{Q_P}{Q_S}}{\omega_P n k_m Q_P L_P}, \tag{7}$$

where  $n = \sqrt{L_S/L_P}$  is the transformer turn ratio. As expected, the primary coil inductance and quality factor play a key role in the start-up condition.

It is interesting to note that the transconductance in (7) is negative only for  $\omega = \omega_L$ . Therefore, the oscillation never occurs at the higher frequency  $\omega_H$ .

### 2.2. Tank Quality Factor

It is well-known that the tank Q-factor plays a key role in the start-up condition, as well as in the oscillator PN performance. PN at the oscillation frequency,  $\omega_0 = \omega_L$ , as a function of the offset frequency,  $\Delta\omega$ , is well described in the  $1/\Delta\omega^2$  region by the Leeson’s formula [12]:

$$\mathcal{L}(\Delta\omega) = 10 \log_{10} \left[ \frac{kTFR_T}{V_0^2} \cdot \left(\frac{\omega_0}{Q_T \Delta\omega}\right)^2 \right], \tag{8}$$

where  $F$  is the oscillator excess noise factor,  $V_0$  is the oscillation amplitude,  $R_T$  is the tank equivalent parallel resistance, and  $Q_T$  is the overall tank quality factor. As is apparent from (8), a tank with a high  $Q$  is mandatory for a low PN, and hence, it is very important to understand how the design parameters should be set to optimize the tank Q-factor.

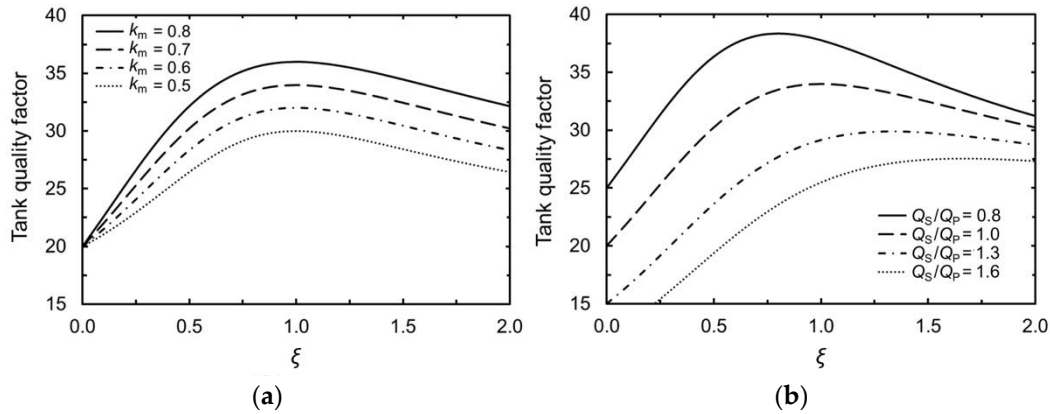
$Q_T$  can be evaluated from Figure 1c using  $Z_t$  from (2) and the following definition [13]:

$$Q_T = \frac{\omega}{2} \left| \frac{d}{d\omega} \angle Z_t(j\omega) \right|_{\omega=\omega_0}. \tag{9}$$

Considering that for  $\omega = \omega_0$ , the imaginary part of the frequency response in (2) is negligible and assuming  $Q_P Q_S \gg 1$ ,  $Q_T$  can be written as:

$$Q_T \approx Q_P \frac{2(1 - k_m^2) \left(\frac{\omega_0}{\omega_S}\right)^2 - 1 - \zeta}{\left[\left(\frac{\omega_0}{\omega_S}\right)^2 - 1\right] + \zeta \left[\left(\frac{\omega_0}{\omega_P}\right)^2 - 1\right] \frac{Q_P}{Q_S}}. \tag{10}$$

Equation (10) gives the resonator  $Q$ -factor as a function of the primary and secondary coil quality factors,  $Q_P$  and  $Q_S$ , coupling coefficient  $k_m$ , and parameter  $\xi$ . Figure 2 shows  $Q_T$ , evaluated at  $\omega_0$ , as a function of  $\xi$  and for different values of  $k_m$  and  $Q_S/Q_P$ .



**Figure 2.** Tank  $Q$ -factor evaluated at  $\omega_0$  as a function of  $\xi$  for different values of (a)  $k_m$  ( $Q_S = Q_P = 20$ ) and (b) the ratio  $Q_S/Q_P$  ( $k_m = 0.7$ ).

As is apparent in Figure 2a, the resonator  $Q$ -factor increases with  $k_m$ . In a typical design, the transformer coils are assumed to have the same  $Q$  (i.e.,  $Q_P = Q_S = Q_O$ ) [14], hence the maximum tank  $Q$ -factor,  $Q_{T,max}$ , is achieved for  $\xi = 1$  and is given by:

$$Q_{T,max} = Q_O(1 + k_m). \quad (11)$$

According to (11), the tank  $Q$ -factor is increased by a factor  $1 + k_m$  with respect to the single-inductor  $Q$ -factor. Moreover,  $Q_T$  is equal to  $Q_P$  when  $\xi = 0$ . Although  $Q_P = Q_S$  is a usual design condition, the value of  $\xi$  that maximizes  $Q_T$  depends in general on the ratio  $Q_S/Q_P$ , as is apparent in Figure 2b. Indeed, by keeping  $Q_S$  constant and increasing  $Q_P$ ,  $Q_T$  increases and reaches the maximum value for  $\xi = \xi_{opt} = Q_S/Q_P$  according to (10). Considering the optimal value of  $\xi$ , a useful design strategy for tank optimization can be drawn from (5). For a given transformer  $T_1$ , the maximum  $Q_T$  is achieved by properly setting the primary and secondary coil capacitances  $C_P$  and  $C_S$ . Specifically, rewriting (4) as a function of  $\xi_{opt}$ ,  $C_P$ , and  $C_S$  can be expressed as:

$$C_P = \frac{1 + \xi_{opt} - \sqrt{1 + \xi_{opt}^2 - 2\xi_{opt}(1 - 2k_m^2)}}{2(1 - k_m^2)(2\pi f_0)^2 \xi_{opt} L_P}, \quad (12)$$

$$C_S = \frac{1 + \xi_{opt} - \sqrt{1 + \xi_{opt}^2 - 2\xi_{opt}(1 - 2k_m^2)}}{2(1 - k_m^2)(2\pi f_0)^2 n^2 L_P}. \quad (13)$$

Finally, the minimum transconductance value,  $g_{min}$ , is given by:

$$g_{min} = -\omega_0 \cdot \frac{n C_S \sqrt{1 + \xi^2 - 2\xi(1 - 2k_m^2)}}{\xi k_m Q_T}. \quad (14)$$

Equation (14) is obtained by substituting (10) into (7). As expected, it shows the relationship of the inverse proportionality that binds  $g_{min}$  to  $Q_T$ .

### 3. VCO Design

As mentioned before, the VCO was designed as a 28-nm FD-SOI CMOS technology, which uses a general-purpose low-cost back-end-of-line (BEOL) consisting of eight copper metal layers, whose thicker ones are the last two (referred to as IB and IA) and an aluminum

metal layer (LB) at the top of the stack. The previous analysis was adopted, which is summarized in the design flow in Figure 3.

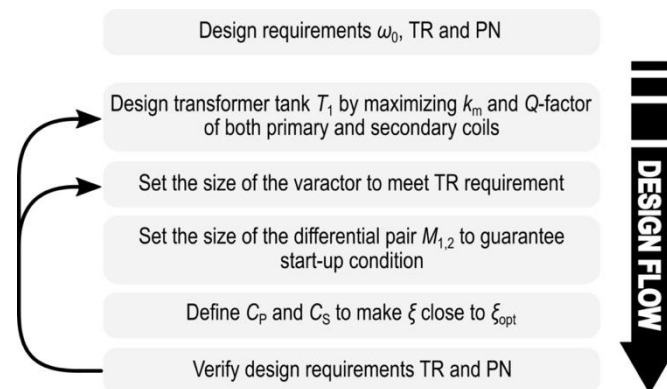


Figure 3. Proposed design flow.

Maximization of the resonator  $Q$ -factor is a key design point for low PN and a robust start-up condition, as highlighted in Section 2. For a given operating frequency,  $Q_T$  depends on the parameters  $k_m$  and  $\zeta$ , as shown in (10), and achieves its maximum,  $Q_{T,max}$ , if the condition  $\zeta = \zeta_{opt}$  is satisfied.

$Q_T$  increases with  $k_m$  and the  $Q$ -factor of both the primary and secondary windings of  $T_1$ . Moreover, a higher  $k_m$  also reduces the minimum transconductance for the start-up condition, as is apparent in (14). This, in turn, leads to a smaller size of the input pair and hence to smaller parasitic capacitances. To achieve a high  $k_m$ , the stacked configuration for the tank transformer was adopted.

As is well known, low inductance and large capacitance should be used in the tank to minimize PN [1,4]. However, this approach leads to a low equivalent parallel loss resistance in the tank, which reduces the oscillator loop gain and hence entails the use of larger transistors to guarantee the start-up. This results in an increase in the parasitic capacitances, which limit the oscillator tuning range. Therefore, the sizes of the primary and secondary coil inductances of the transformer tank must be considered as part of a trade-off between PN performance, tuning range, and power consumption.

Figure 4 shows a 3-D view of the VCO tank transformer, along with the adopted metal stack and its main parameters. The transformer was implemented by adopting a single turn octagonal winding with a stacked configuration, whose inner diameter and metal width were  $65 \mu\text{m}$  and  $25 \mu\text{m}$ , respectively.

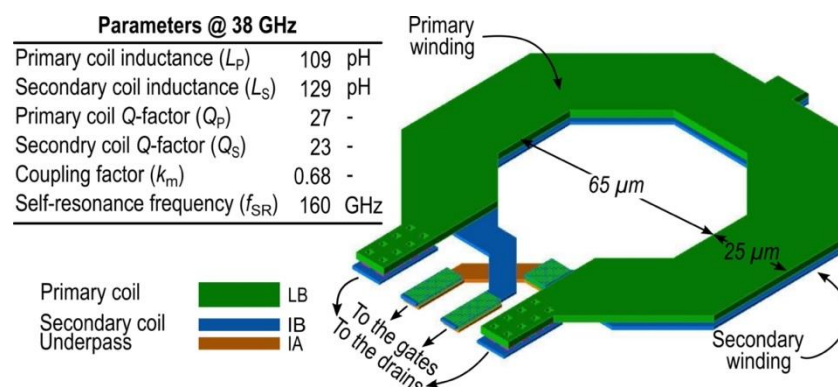


Figure 4. 3-D view of transformer  $T_1$  with the adopted metal stack.

To minimize both the resistive losses and parasitic capacitances from the substrate, an aluminum layer LB and an upper copper metal layer IB were used for the primary

and secondary windings, respectively, while a metal layer IA was used for the underpass. Moreover, neither polysilicon nor a metal patterned ground shield (PGS) was used in the transformer design since it has a negligible impact on substrate losses at mm-wave frequencies [15] but significantly reduces the self-resonant frequency. The whole transformer structure was designed using the 2.5-D electromagnetic (EM) simulator “Momentum,” by including interconnections and supply/ground paths, with the aim of maximizing the  $Q$ -factor of both primary and secondary coils.

A-MOS varactors were profitably used to meet the TR requirement. Unfortunately, varactors exhibit a poor  $Q$ -factor at mm-wave frequencies, which is the main hindrance regarding the resonator quality factor. Therefore, varactors must be designed to be as small as possible, even though this is in contrast with the TR performance. Thanks to the transformer tank implementation that was adopted, the transformer turn ratio,  $n$ , was slightly higher than 1, and hence the varactors could be advantageously placed between the transistor gates. Indeed, the capacitance variation at the secondary winding was equivalently increased by a factor  $n$ . This allowed for a smaller varactor to be used to cover the tuning range, with the benefit of a reduced amplitude-to-phase noise conversion due to the varactor nonlinearity [6]. According to the previous consideration, a small A-MOS varactor connected to the secondary winding of transformer  $T_1$  was used, which provided a capacitance ranging from 40 fF to 80 fF and a  $Q$ -factor around 14 at 38 GHz. Due to the underpass that performed the cross-connection of the transformer with the gates, the secondary winding of  $T_1$  exhibited higher losses, although the overall tank  $Q$ -factor was dominated by the varactors. Using (10) and assuming that  $\zeta$  was close to its optimal value, an equivalent tank  $Q$ -factor around 33 was achieved, which was higher than that of the transformer inductors.

As far as the differential pair is concerned, the size was set by considering that a larger transistor width provides a robust start-up condition but increases the thermal noise and parasitic capacitances, which affect PN and TR, respectively.

The layout at mm-wave frequencies greatly impacts the performance of a VCO in terms of PN and TR. Therefore, accurate layout design becomes mandatory to minimize parasitic effects, especially gate resistance and gate-to-drain capacitances [16]. For this purpose, extensive EM and post-layout simulations were carried out to select the size of the transistor pair, whose aspect ratio was set to 28  $\mu\text{m}/100\text{ nm}$ . Moreover, a multifinger transistor with double gate contacts was used in this design. Indeed, each transistor finger is a distributed RC network and a double contact reduces the resistance of each finger by a factor of four, thus reducing the equivalent thermal noise.

To set  $\zeta$  close to its optimal value,  $C_P$  and  $C_S$  must be set according to (12) and (13), respectively. For this design,  $C_P$  and  $C_S$  had overall values of 102 fF and 64 fF, respectively, which accounted for the parasitic, additional, and varactor capacitances, as mentioned before.

Transformer  $T_2$  at the source node of the differential pair was designed using similar layout considerations to those of  $T_1$  but with the aim of minimizing the insertion loss (IL) at 77 GHz. For this purpose, an interstacked configuration was preferred [15,17], whose 3-D view is shown in Figure 5, along with the transformer’s main parameters. Both the primary and secondary windings were implemented with upper metal layers IA, IB, and LB by adopting a spiral width of 5.5  $\mu\text{m}$ , which allowed for a good trade-off between the winding parasitic capacitances and series resistance to be achieved. The winding metal spacing was set to the minimum value (i.e., 2  $\mu\text{m}$ ) to improve the magnetic coupling coefficient that was involved in the signal transfer and the inner diameter was set to 30  $\mu\text{m}$ .

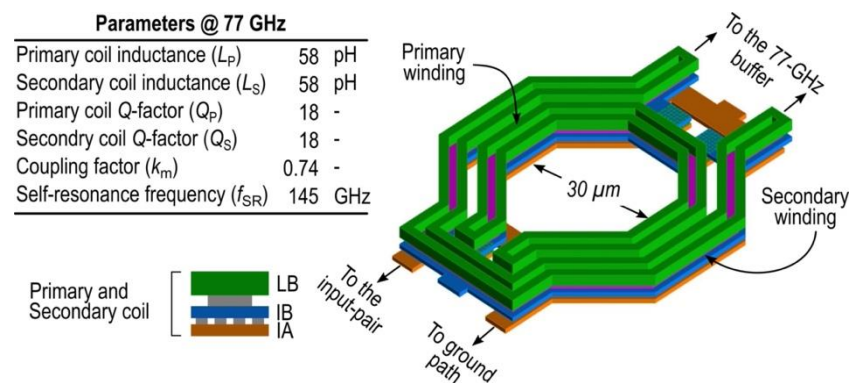


Figure 5. 3-D view of transformer  $T_2$  with the adopted metal stack.

#### 4. Experimental Results

The 38 GHz VCO was implemented in the 28-nm FD-SOI CMOS technology by STMicroelectronics, which provided a fast active device with  $f_T$  and  $f_{max}$  up to 300 GHz [18] and a general-purpose BEOL.

The chip was assembled with the chip-on-board approach in an FR4 printed circuit board (PCB). The measurement setup is shown in Figure 6. Frequency dividers and a buffer were also included in the test chip (see the dashed area in Figure 6), which was mounted in the PCB, together with a commercial phase-frequency detector and charge pump (PFD/CP) and a discrete loop filter (LF) to enable closed-loop measurements at 4.8 GHz.

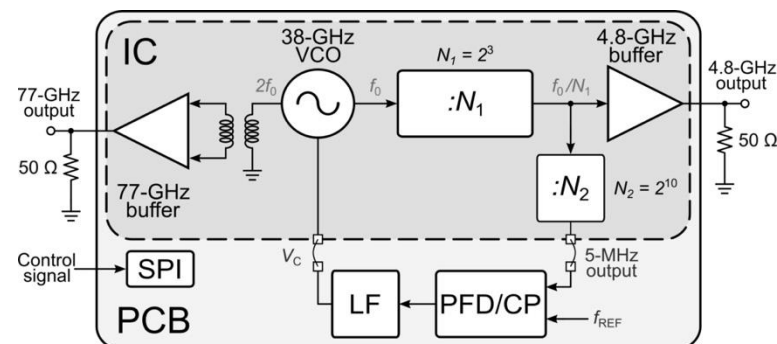


Figure 6. Simplified block diagram of the measurement setup.

Figure 7 shows the die microphotograph. The total die area was  $1660 \times 1280 \mu\text{m}$ , including the electrostatic discharge (ESD) protection ring and the radio frequency (RF) ground-signal-ground (GSG) pads, whereas the VCO core area was only  $300 \times 135 \mu\text{m}$ .

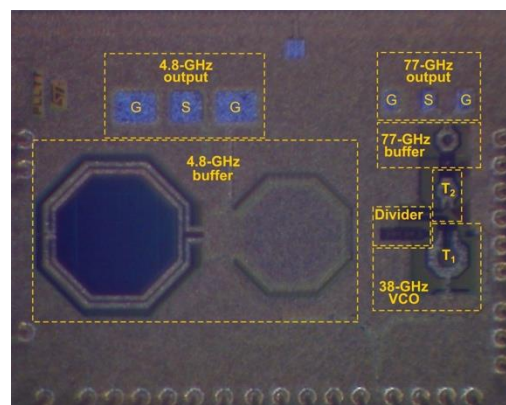
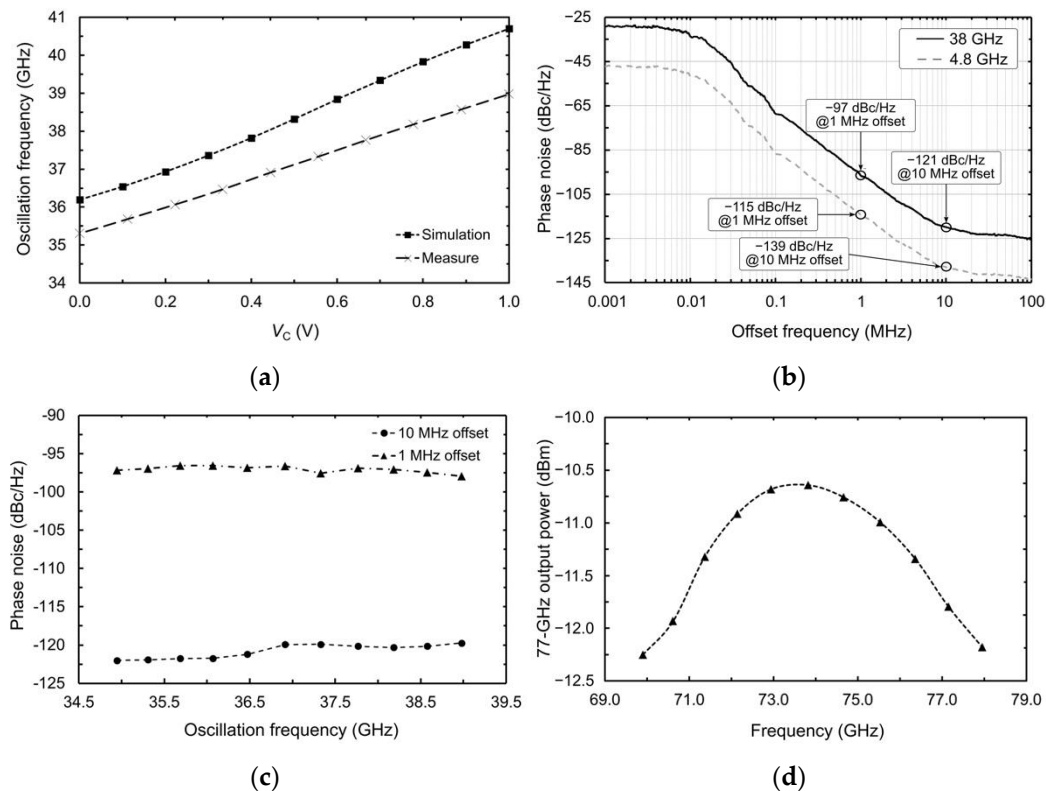


Figure 7. Die microphotograph.

The current consumptions of the VCO, divider, and testing buffer were 26, 30, and 4.5 mA, respectively, from a 1 V power supply. The measured tuning range was 4 GHz (i.e., from 35 to 39 GHz) when the varactor control voltage  $V_C$  swept from 0 to 1 V, as shown in Figure 8a. The comparison with the simulated curve highlighted a frequency shift of around 2 GHz, which could mainly be ascribed to the first tentative varactor model available at the time of the VCO design.



**Figure 8.** Measured (a) frequency tuning range, (b) phase noise, (c) phase noises at the 1 MHz and 10 MHz offset frequencies versus the VCO oscillation frequency, and (d) 77-GHz output power.

The measured VCO phase noise is illustrated in Figure 8b. The PNs at 4.8 GHz were  $-115$  dBc/Hz and  $-139$  dBc/Hz at the 1 MHz and 10 MHz offset frequencies, respectively. The extrapolated curve at 38 GHz is also shown in Figure 8b, which was calculated from the assumption of a PN degradation factor of  $N^2$  using a frequency division ratio of  $N$ . At a 38 GHz oscillation frequency, the equivalent PNs were about  $-97$  dBc/Hz and  $-121$  dBc/Hz at the 1 MHz and 10 MHz offset frequencies, respectively. The measured VCO phase noise at 1 MHz and 10 MHz over the whole frequency tuning range is shown in Figure 8c. In these curves, the best, average, and worst PNs at a 1 MHz offset frequency were  $-96.6$  dBc/Hz,  $-97$  dBc/Hz, and  $-98$  dBc/Hz, respectively, whereas the best, average, and worst PNs at a 10 MHz offset frequency were  $-122$  dBc/Hz,  $-121$  dBc/Hz, and  $-120$  dBc/Hz, respectively.

Figure 8d shows the measured second harmonic output power as a function of the tuning voltage. The output power at 77 GHz varied between  $-12.2$  dBm and  $-10.6$  dBm in the entire frequency range.

Table 1 provides a summary of the measured results and a comparison with state-of-the-art mm-wave CMOS VCOs. To consider the oscillator's main performance parameters, a comparison was also carried out by considering the well-known figure of merits, FoM and FoM<sub>T</sub>.

**Table 1.** Performance summary and comparisons with the state of the art.

Reference	[2]	[19]	[20]	[21]	[22]	This Work	Units
CMOS technology	65 nm	65 nm	28 nm	90 nm	32 nm	28 nm	–
Bias approach	Current	Voltage	Voltage	Current	Current	Voltage	–
$V_{DD}$	1	1	1	1	1	1	[V]
$P_{DD}$	11.7	6.2	22.5 <sup>2</sup>	8.1	9.8	26	[mW]
Frequency	39.6	55	29.25 <sup>1</sup>	20.85	40	37	[GHz]
Tuning range	12.12	18	14	15.8	31.6	11	[%]
PN @ 1 MHz <sup>3</sup>	−94	−93.3	−103	−95.7	−97.3	−97	[dBc/Hz]
PN @ 10 MHz <sup>3</sup>	−120.3	−115.4	−123.5	−120	−117.3	−121	[dBc/Hz]
FoM @ 1 MHz <sup>4</sup>	−175	−176.9	−180.5 <sup>2</sup>	−177.8	−178.7	−175	[dBc/Hz]
FoM @ 10 MHz <sup>4</sup>	−181	−178.9	−181 <sup>2</sup>	−182.3	−178.7	−181	[dBc/Hz]
FoM <sub>T</sub> @ 1 MHz <sup>5</sup>	−176	−181.9	−183.5 <sup>2</sup>	−181.8	−188.7	−176	[dBc/Hz]
FoM <sub>T</sub> @ 10 MHz <sup>5</sup>	−183	−184	−184 <sup>2</sup>	−186.3	−188.7	−182	[dBc/Hz]

<sup>1</sup> Third harmonic extraction from a 10 GHz oscillating core; <sup>2</sup> including the power consumption of the multiplier and buffer; <sup>3</sup> normalized around 37 GHz; <sup>4</sup> FoM =  $\mathcal{L}(\Delta f) - 20 \log_{10}(f_0/\Delta f) + 10 \log_{10}(P_{diss}/1\text{mW})$ ; <sup>5</sup> FoM<sub>T</sub> = FoM − 20 log<sub>10</sub>(TR(%)/10).

By normalizing the PN according to its typical dependence on the oscillation frequency expressed in (8), the proposed VCO exhibited the best performance regarding the PN, with the exception of [20], whose output frequency was achieved by exploiting the third harmonic of a 10 GHz oscillator. Specifically, the PN performance at a 10 MHz offset frequency, which is the most critical PN requirement for an automotive radar sensor, achieved an excellent value of −121 dBc/Hz. Regarding the FoMs, the proposed VCO showed similar values to the state-of-the-art oscillators.

## 5. Conclusions

A transformer-based VCO topology for FMCW automotive radar applications was discussed. Thanks to an accurate design strategy for the Q-factor maximization of the transformer-based tank, a low phase noise was achieved while preserving the oscillation tuning range, despite an oscillation frequency as high as 38 GHz. Indeed, the phase noise performance at a 10 MHz offset frequency achieved an excellent performance of −121 dBc/Hz, where this is the most important requirement for the radar maximum operating distance.

The VCO was implemented in a 28-nm FD-SOI CMOS technology, along with a prescaler and a frequency divider for test purposes. Although the technology adopted a standard BEOL to achieve low fabrication costs and a 38 GHz oscillation frequency was performed, the measured phase noise was better than that of most state-of-the-art mm-wave CMOS oscillators. The VCO was able to directly drive a PA stage since it provided a 77-GHz buffered signal with an output power higher than −12 dBm in the whole tuning range.

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