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RESEARCH ARTICLE

A High Efficiency and High Power Density Active AC/DC Converter for Battery-Less US-Powered IMDs in a 28-nm CMOS Technology

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ABSTRACT In this paper, the design and experimental validation of an active rectifier for ultrasound-based implanted biomedical devices are presented. One of the main contributions is the adoption of an optimized design procedure based on the g_m/I_D of the transistors. Implemented in a 28-nm CMOS technology and powered by a 0.5- mm thickness and 1- mm^2 surface area piezoelectric transducer, the rectifier delivers 1- mW of power to the output load. The adoption of a square wave to drive the transmitting power transducer is experimentally demonstrated to be more power effective. The rectifier exhibits a measured peak power conversion efficiency and a power density equal to 95% and 222 mW/mm^2, respectively, revealing itself as the best trade-off between measured power conversion efficiency and power density within the literature of US-powered AC/DC converters.

INDEX TERMS Active rectifier, energy harvesting, implanted biomedical device (IMD), power management, ultrasound (US).

I. INTRODUCTION

The recent developments in CMOS technological process have paved the way to nanometer-scale ICs and miniaturized implantable medical devices (IMDs). In fact, the necessity for continuous sensing of biological signals and the growing demand for electrical stimulation of human organs to support their operations have led to an increasing interest, both commercial and academic, in computer-human interfaces assisted by wireless body area networks (WBANs) [1].

The main factor limiting the miniaturization of an IMD is the adoption of a primary battery that occupies up to 90% of the device volume and, moreover, has the risk of leaking toxic hazardous substances. In order to reduce the volume of the implanted device and decrease invasiveness, the devices must be battery-less and the power supply delivered exploiting energy harvesting techniques.

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Among the various techniques, electromagnetic (EM) or ultrasound (US) can be profitably adopted for IMDs [2], [3], [4], [5], [6], [7], [8], [9]. While the FDA limits exposure to EM-fields around 100 $\mu W/mm^2$, US-waves can reach 7.2 mW/mm^2. Moreover, US waves can penetrate deeper into the body due to their lower frequency. Hence, US energy harvesting has recently been revealed to be a better option for deeply implanted IMDs requiring a power budget up to the milliWatt range [4], [5], [10].

Fig. 1 shows the typical block diagram of a US-powered IMD. The IMD embeds an illustrative abstract schematic description of the US-power link which is also exploited to implement a bi-directional data link [2], [10], [11]. While the former is made up of two piezoelectric (PZT) transducers (namely, TX-PZT and RX-PZT) electrically coupled and kept under electrical resonance condition together with an active rectifier and a LDO, the latter exploits US-waves to establish both data up/downlinks for the communication. Indeed, the out-of-body electronic system performs, via an FPGA (or a microcontroller), both the electrical excitation

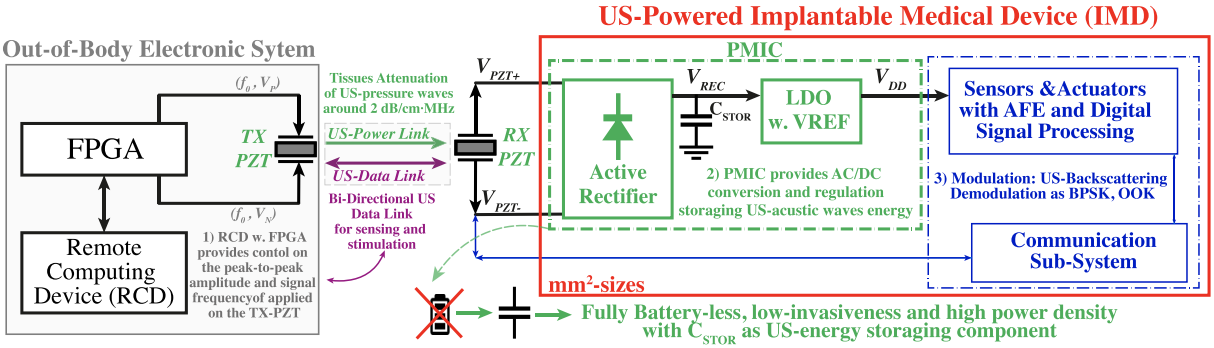

FIGURE 1. US-Powered battery-less system overview for IMDs.

of the TX-PZT transducer and the signal processing of incoming US-modulated signals (e.g., backscatter up-link for sensing [2], [10], [11], [12]) together with the modulation of bit-frames to be sent to the IMDs for stimulation purposes (i.e., BPSK [13] or OOK [2], [10], [11]).

In this scenario, this paper deals with the design and characterization of both the US-power link and the active AC/DC converter. The integrated circuit was implemented in a 28-nm bulk CMOS technology. This work is part of a wider project whose objective is the development of a single-chip, 4096-channel implantable Brain Machine Interface (BMI), surgically placed over the brain pia mater membrane, to sense neuronal action and local field potentials and stimulate neurons within a closed-loop system. The choice of a 28-nm technology is mainly dictated by the presence of a large digital section and by the multichannel time-sharing architecture of the analog front-end. The experimental results show that, under electrical resonance condition of both TX-PZT and RX-PZT, the electrical stimulation of the transmitting power transducer results more effective if a square-wave is applied, compared with a single sinusoidal tone, in terms of both output voltage and power. Moreover, it is important to underline that for a microcontroller or an FPGA it is easier to generate a square wave than a sine signal, requiring, hence, lower programming and design efforts.

The work is organized as follows. Section II reports the characterization of the US-power link, while Section III describes the active rectifier working principle and its implementation. Section IV deals with the measurements results together with the comparison with previous works in literature. Finally, in Section V conclusions are drawn.

II. US-POWER LINK CHARACTERIZATION

Before going through the design of the active rectifier for the US-powered IMD, the characterization of the US power link is required. Indeed, the electrical quantities, as the series resistance of the RX-PZT (modelled with Thévenin equivalent model), its resonance frequency, the maximum achievable received power and peak-to-peak AC voltage when in resonance conditions are the parameters necessary to design the rectifier.

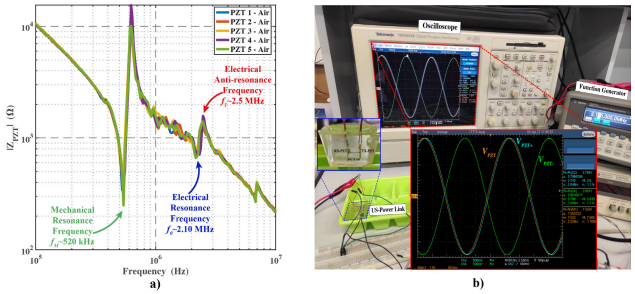

FIGURE 2. a) Frequency-domain characterization of $|Z_{PZT}|$ of five RX-PZT US-transducers in air. b) US-Power Link in ballistic gel under electrical resonance: characterization of electrical quantities in the time domain from [14].

As shown in Fig. 2a), the US-power link was characterized in the frequency domain. Indeed, the impedance, $|Z_{PZT}|$, of five RX-PZT transducers was first evaluated by exploiting a Vector Network Analyzer (VNA E5061B provided by Keysight Technologies) to detect their resonance frequency, f_0, and their impedance around the above-mentioned frequency. The employed RX-PZT is the 000065944 device provided by PI Ceramics with 0.5- mm thickness and 1- mm^2 surface area. The TX-PZT (PRY+0111) is also provided by PI Ceramics and it shows a diameter of 8 mm with a radial resonance frequency of 250 kHz and an electrical resonance frequency centered around 2.1 MHz. The measured resonance frequency (in air) is found around 2.1 MHz with an impedance $R_{PZT,air} \sim 800\,\Omega$. Furthermore, a time-domain experimental characterization of the US-power link packed in ballistic gel was carried out by using the oscilloscope Tektronik TDS5054B, as reported in Fig. 2b). It is worth noting that the mentioned gel allows to mimic the acoustic impedance of human tissues and the distance, d, between the power transmitting piezo (TX-PZT) and the power receiving piezo (RX-PZT) is assumed equal to 1.0 cm (i.e., superficial IMDs). Moreover, the tissue attenuation is estimated around 2 dB/cm·MHz [15], yielding an expected attenuation of the TX AC voltage of about 4-5 dB. The experimental results in Fig. 2b) are obtained by applying a 20-V_{pp} sine wave with $f_0 = 2.1$ MHz to the TX-PZT. The received AC voltages, namely V_{PZT+} and V_{PZT-}, are obtained with a

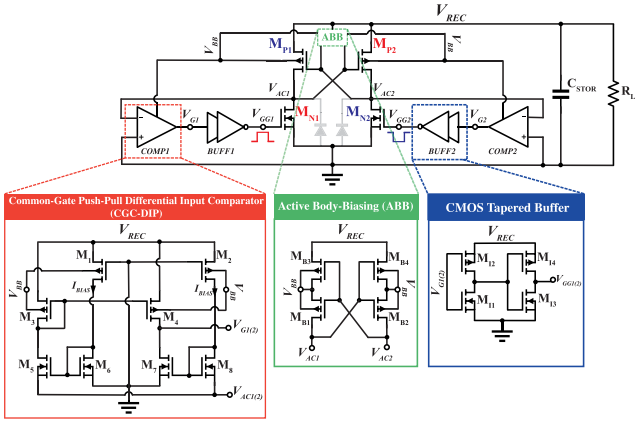

FIGURE 3. Schematic of the proposed active AC/DC converter with detailed views on the Common-Gate Comparator (CGC-DIP, COMP1,2), Active Body Biasing (ABB) and CMOS Tapered Buffers blocks (BUFF1,2).

matching series resistance $R_{EQ} = 1.65\,k\Omega$, leading, thus, to a maximum received power equal to about 4.2 mW.

III. ACTIVE AC/DC CONVERTER

A. CIRCUIT WORKING PRINCIPLE

The active AC/DC converter exploits the concept of *active diodes* to achieve the rectification of the received AC voltage from the US-energy source. The schematic in Fig. 3 reports the implemented active rectifier in which the two input phases are V_{AC1} and V_{AC2}, being $V_{AC} = V_{AC1} - V_{AC2}$. It presents three main sub-circuits: two common-gate comparators (COMP1,COMP2), an Active-Body Biasing Circuit (ABB) and two CMOS tapered buffers (BUFF1, BUFF2).

The core of the rectifier circuit is represented by two power NMOS transistors, $M_{N1,N2}$, and two power PMOS transistors, $M_{P1,P2}$. The two p-type active devices allow the energy transfer from the source to the load, represented by a storage capacitor, C_{STOR}, and a resistive load, R_L, to emulate the load circuitry. During the start-up phase ($V_{REC} = 0$), if $V_{AC1(2)} < |V_{tp}|$, being V_{tp} the threshold voltage of the PMOS transistors, $M_{P2(1)}$ works in triode region with an ON-resistance given by

$$R_{PMOS} = \frac{1}{\mu_p C_{ox}(W/L)_p(V_{SG} - |V_{tp}|)} \tag{1}$$

where $(W/L)_p$ is the aspect ratio of the power PMOS transistors, $M_{P1,2}$, while their source-to-gate voltage is given by $V_{SG1(2)} = V_{REC} - V_{AC1(2)}$. Moreover, the previous relation holds for both long-channels and short-channels devices. Using, then, short-channels models the p-type transistor conductance is derived in [16] as

$$G_{PMOS} = \mu_p C_{ox} \frac{\left[V_{OV,P} - \left(1 + \frac{1}{2}\frac{V_{SD}}{E_{cp}L}\right)V_{SD}\right]}{\left(1 + \frac{V_{SD}}{E_{cp}L}\right)^2}\left(\frac{W}{L}\right)_P \tag{2}$$

where $V_{OV,P} = V_{SG1(2)} - |V_{tp}|$, E_{cp} is the holes critic electric field and $V_{SD} = V_{SD1(2)} = V_{REC} - V_{AC1(2)}$. In addition, the same results can be applied on n-type transistors.

TABLE 1. Components sizes.

Block	Component	Size	Unit
CGC-DIP (COMP1,2)	M_1, M_2	0.32/0.15	$\mu m/\mu m$
	$M_3 \ldots M_8$	9.6/0.6	-
CMOS Tapered Buffer (BUFF1,2)	M_{I1}	0.32/0.15	$\mu m/\mu m$
	M_{I2}	0.96/0.15	-
	M_{I3}	1.6/0.15	-
	M_{I4}	4.8/0.15	-
Active Body-Biasing (ABB)	M_{B1}, M_{B2}	9.6/0.15	$\mu m/\mu m$
	M_{B3}, M_{B4}	9.6/0.3	-
Core Rectifier	M_{P1}, M_{P2}	240/0.15	$\mu m/\mu m$
	M_{N1}, M_{N2}	240/0.15	-

The start-up phase ends when $V_{REC} \simeq |V_{tp}|$. Indeed, as can be seen in Fig. 3, the comparators are self-current-biased by PMOS transistors M_1 and M_2 that generate the biasing current I_B by working in inversion region. COMP1 and COMP2 are Common-Gate Push-Pull Differential Input comparators (CGC-DIP) [17]. Therefore, the working principle of COMP1(2) is here summarized. When, $V_{AC1(2)} < GND$, with GND the ground potential, I_B enters transistor M_6 giving rise to its gate-to-source voltage, V_{GS6}. The same gate voltage is applied to transistor M_5, but its current, I_{D5} results larger than I_B, due to its higher gate-to-source voltage ($V_{GS5} > V_{GS6}$). I_{D5} is then mirrored by the PMOS current mirror, $M_{3,4}$, and pushed on COMP1(2) output node, $V_{G1(2)}$. In the same manner, I_B biases the gate voltages of transistors $M_{7,8}$. This results in a lower gate-to-source voltage for M_8 and the pulled current from the comparator output node is $I_{D7} < I_{D4}$ making $V_{G1(2)}$ goes high. In addition, the CMOS tapered buffers, BUFF1(2), made up by cascading two CMOS inverter, have been added to the comparator output, allowing both to restore the logic high/low logic level (corresponding to V_{REC} and GND, respectively) and to increase the driving capability. When $V_{GG1(2)}$ is high, the n-type transistor $M_{N1(2)}$ is short-circuited to ground with an on-resistance, R_{NMOS}. If R_{NMOS} is negligible compared with the equivalent series Thévenin resistance of the US-energy source, the incoming AC input phase, $V_{AC1(2)}$, results short-circuited to ground, while the other one, $V_{AC2(1)}$ is, with the same conditions, short-circuited to V_{REC}. These last considerations fully-accomplish to the definition of *active diodes*.

The Active Body Biasing Circuit (ABB) shown in Fig. 3 and proposed in [18] has been added to ensure that the bulk voltage, V_{BB}, for all the sub-circuits is always slightly lower or equal to the rectified one and to reduce, thus, the body-effect. Indeed, when V_{AC1} is low, V_{AC2} is high, the bulk voltage V_{BB} is given by the voltage divider made up by transistors $M_{B2,4}$ of the voltage drop between $V_{AC1(2)}$ and V_{REC}. Differently, from more common body-biasing structure exploited in both active and passive rectifiers (e.g., self-body biasing (SBB) [19], [20]), the proposed one allows to reduce the coupling effect through parasitic capacitances of the AC input phases, especially for frequencies higher than tens of MHz. By this, in SBB the bulk voltages of the PMOS transistors within the core rectifier could be quite higher than V_{REC} and the overall charge transferred to the output is,

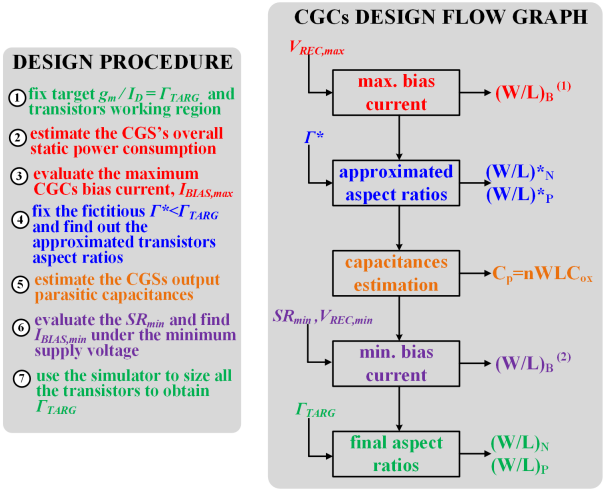

FIGURE 4. g_m/I_D-based design procedure and design flow graph for CGSs extracted from [21].

hence, reduced. As a result, the overall power transferred to the load is reduced too and the η_{REC} falls down.

B. G_M/I_D-BASED SIZING PROCEDURE FOR COMMON-GATE COMPARATORS

The CGCs transistor sizing, shown in Tab. 1, is carried out by exploiting the g_m/I_D-based procedure explained by the Authors in [21] and reported here as in Fig. 4, ensuring an overall post-layout simulated power conversion efficiency of the rectifier, η_{REC}, higher than 94%. It is worth noting that this design procedure cab be applied to any comparators working under power/delay constraints.

The design procedure and the constraints are here summarized as follows:

1) Fix a target $g_m/I_D = \Gamma_{TARG}$ to guarantee the proper working region of the active devices within the CGCs. In this prototype, $\Gamma_{TARG} = 26.5\,V^{-1}$ is chosen for both n-type and p-type transistors to maintain their weak-inversion operating region, indeed $\Gamma \approx 26.5V^{-1}$ leads to $|V_{GS}| - |V_{TH}| \sim -140$ mV, as reported in the g_m/I_D graphs for the adopted 28-nm technology node in [21].
2) The maximum allowed static current consumption of both the CGSs within the active rectifier is, then, estimated. Each CGC maximum static power consumption is defined as $P^{max}_{DD,COMP} = V^{max}_{REC} \cdot I^{max}_{COMP}$, where $I_{COMP} = 4 \cdot I_{BIAS}$ and I_{BIAS} is the self-bias current for each CGC. $P_{DD,comp}$ fixed, for instance, as the 5% of the minimum input power, P^{min}_{IN}, under load conditions.
3) Since the V^{max}_{REC} is fixed by the technology (i.e., 1.8 V for the adopted 28-nm node) and the minimum input power is linked to the harvested energy source, it is possible to find out the maximum bias current as

$$I^{max}_{BIAS} = \frac{1}{4} \cdot \frac{5\% \cdot P^{min}_{IN}}{V^{max}_{REC}} \tag{3}$$

Furthermore, by exploiting the behavioural laws of I_D vs. $|V_{GS}|$ for the active devices (i.e., exponential law in sub-threshold and square-law in super-threshold working region), the dimensions of the biasing p-type transistors, namely $M_{1,2}$ in Fig. 3, are found out.
4) Fix $\Gamma^* = \Gamma_{TARG} - 3V^{-1}$ as the fictitious g_m/I_D to be used under maximum output rectified voltage conditions, V^{max}_{REC}. By adopting this last parameter, the approximated aspect ratios of the active devices within CGCs are found, namely $(W/L)^*_N$ and $(W/L)^*_P$ for NMOS and PMOS respectively. This passage has to be verified with the use of the simulator.
5) Estimate the parasitic capacitances on the output node, namely $V_{G1(2)}$, of the comparators by using the equation $C_p = nWLC_{OX}$, where n depends on the number of transistors connected on the output node, $C_{OX} = \epsilon_{OX}/t_{OX}$ and W, L depend on the previous sizing step and on the device operating region. In this case, the weak-inversion region is taken into account, then the major capacitive contributes are given by the overlap. These capacitance is within 5-10 fF range.
6) Define, first, the minimum slew-rate, $SR_{min} = \Delta V^{min}_{G1(2)}/\Delta t^{max}_{rise,fall} = I^{min}_{BIAS}/C_p$, where $\Delta t^{max}_{rise,fall} \ll 1/(2f_0)$ and $\Delta V^{min}_{G1(2)} = V^{min}_{REC}$, usually around V_{tn} to allow the rectifier works in active mode. Furthermore, I^{MIN}_{BIAS} is the minimum self-generated bias current when the rectified voltage is the minimum too, V^{min}_{REC} and C_p was estimated in the previous design step. Then, by taking into account $f_0 = 2.1$ MHz and $SR_{min} \sim 20V/\mu s$, the minimum bias current is found out (around 200 nA) and, hence, the dimensions of $M_{1,2}$ in Fig. 3.
7) Finally, by adopting the previous minimum bias current and the fixed parameter Γ_{TARG} the aspect ratios of all the transistors in CGC1,2 are found out.

It is worth noting that this design strategy for CGCs in active AC/DC converter allows to achieve a PCE>90%, as shown in the simulation results of [21], without requiring the adoption of complex and power-hungry turn-on/off delay compensation circuit. Indeed, most of the literature of active rectifiers (i.e., [17], [22], [23], [24], [25]) maintains the basic structure of the AC/DC converter as shown in the proposed solution in Fig. 3; to increase the PCE they mainly adopt turn-on/off delay compensation/calibration strategies. Indeed, the turn-on/off delay of transistors $M_{N1,2}$ (see Fig. 3) increases the dynamic power consumption of the circuit and, hence, reduces the PCE, since both the *active diode* are turned-on simultaneously or they result turned-off for a quite long time interval compared with the AC input voltage. This main issue of active rectifiers is avoided and overcome by adopting the presented and experimental demonstrated design strategy for the CGCs. It is also worth noting that none of the cited paper within the literature of active rectifier show a design methodology for the sizing of the adopted comparators.

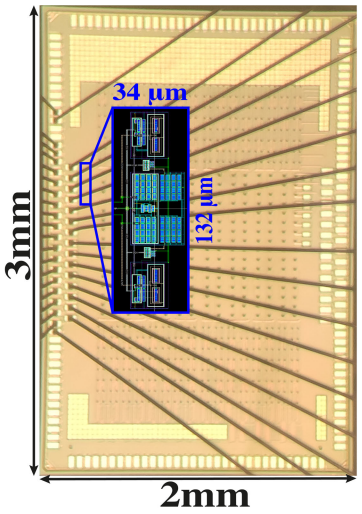

FIGURE 5. IC prototype microphotograph and proposed active rectifier layout.

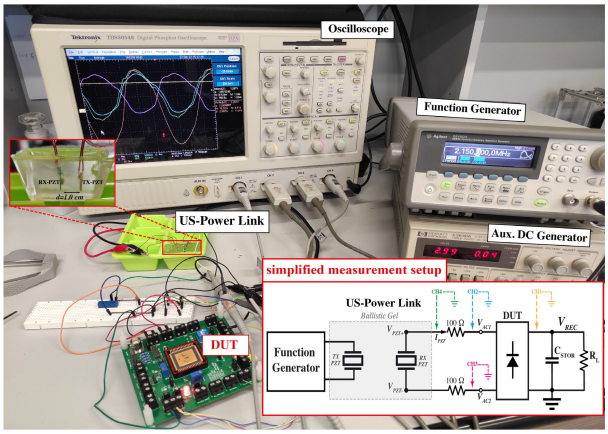

FIGURE 6. Experimental measurement setup photograph and simplified block-diagram.

C. EXPERIMENTAL RESULTS

The experimental results on the proposed active rectifier have been carried out by exploiting 10 test chip implemented in a 28-nm Bulk CMOS technology provided by TSMC. The sizes of the component have been reported in Tab. 1. SVT-18 thick-oxide transistors (with $L_{min} = 0.15\mu m$) have been used for their larger breakdown voltage (equal to 1.8 V); moreover, the threshold voltages are $V_{tn} \approx 560\,\text{mV}$ and $|V_{tp}| \approx 490\,\text{mV}$ for NMOS and PMOS transistors respectively. The chip microphotograph is show in Fig. 5. The proposed rectifier occupies an active area of $0.0045\,\text{mm}^2$ while the entire shared-block die occupies $6\,\text{mm}^2$ (pad pitch equals to 50 μm). The IC was bonded into a 64-pin ceramic CCLC package. In addition, it is worth noting that both the US-PZT transducers have been packed in ballistic gel with a fixed distance d=1.0 cm.

The experimental setup is reported in Fig. 6. A function generator (Agilent 33250A) was used to generate the AC input voltage for the TX-PZT transducer. Furthermore, both sine wave and square wave (with same peak-to-peak amplitude and frequency) have been applied to the power transmitting transducer. It was set the frequency of the sine and square voltage equal to 2.15 MHz, as the electrical resonance frequency of the US-PZT devices with gel and the amplitude was set equals to $V_{pp,TX} = 20\,V_{pp}$. The device under test (DUT) was placed on a FR4-substrate custom PCB prototyping board realized for the measurements and was supplied by an incoming AC input voltage received by the RX-PZT. Then, an auxiliary DC generator (HP E3630A) was also used to provide both the positive and the negative rails ($\pm 3.0\,V$) for the ESD pad protection devices embedded within the IC. Then, a 4-channel oscilloscope (Tektronix TDS5054B) was exploited to observe the main electrical quantities in the time domain, such as the input received voltage, V_{AC}, as the difference between V_{AC1} (CH2, blue) and V_{AC2} (CH3, purple), the rectified voltage V_{REC} (CH1, yellow). The dynamic time-domain response of the proposed active AC/DC converter is shown in Fig. 7. An AM modulated input (sine in Fig. 7(a) and square in Fig. 7(b)) voltage is then applied to the TX-PZT. The shape of the modulating signal is a square with 100-Hz frequency. The used storage capacitor was set to 1 nF to better emphasize the output ripple in both the conditions. Indeed, around 25 mV output ripple on V_{REC} is measured in Fig. 7(a) and around 35 mV on the DC rectified output voltage in Fig. 7(b). On the other side, Fig. 7(a) shows a rise time around 110 μs while Fig. 7(b) has a $t_{rise} \sim 70\,\mu$s. In both the sub-figures it is also underlined the transition from passive to active rectification given by transistors $M_{N1,2}$ (in Fig. 3) passing from weak-inversion to strong-inversion region since $V_{GG1,2}^{max} = V_{REC} > V_{tn}$ and transistors $M_{N1,2}$ are completely turned-on/off.

Moreover, the received input current, I_{PZT}, was evaluated by using the Ohm's law on a series 100 Ω resistance and its voltage drop is taken by the difference between CH4 (green) and CH2. It is worth noting that, since the AC current amplitudes are the order of hundreds of μA, a sense resistance of 100Ω is better suited for current measurement. In this way, the measured voltage drop between V_{PZT+} and V_{AC2} results in the order of magnitude of 100 mV. Furthermore, the vertical resolution of the adopted oscilloscope is equal to 1mV/div, that leads to a measured current resolution of 10 μA/div and an absolute current resolution equals to 2 μA. Concerning the load resistance, R_L, a trimmer was used within the range of 1-10 kΩ. A ceramic capacitor, with a nominal value of 10 nF, was used for the storage capacitor, C_{STOR}, in order to reduce the average ripple on V_{REC} is around 2.5 mV. In the case of square wave input voltage for the TX-PZT, due to reflected US-waves and thus reflected voltage, the ripple increases up to 4 mV. The scope acquisitions of one of the 10 measured samples are reported in Fig. 8 and Fig. 9 for both the cases.

The percentage power conversion efficiency of the rectifier, $\eta_{REC,\%}$ evaluated by the following equation

$$\eta_{REC,\%} = 100 \cdot \frac{P_{REC}}{P_{IN}} = \frac{V_{REC}^2/R_L}{\frac{1}{N \cdot T}\int_{t_0}^{t_0+N\cdot T} V_{AC}(t) \cdot I_{PZT}(t)\,dt} \tag{4}$$

TABLE 2. Measured parameters for different TX-PZT input voltages.

	Load	Param.	Mean	Max	Min	Std Dev.	Unit
Sine wave input	2.4 kΩ	V_{REC}	1.16	1.19	1.09	0.032	V
		P_{REC}	560	590	495	0.42	μW
		VCE	66.66	69.88	64.33	2.66	%
		η_{REC}	94.54	97.47	90.02	2.27	%
	10 kΩ	V_{REC}	1.62	1.67	1.52	0.048	V
		P_{REC}	262	279	231	0.23	μW
		VCE	90.0	92.77	84.44	2.66	%
		η_{REC}	59.27	63.84	49.23	4.51	%
Square wave input	2.4 kΩ	V_{REC}	1.50	1.63	1.29	0.10	V
		P_{REC}	0.94	1.10	0.69	0.12	mW
		VCE	75.21	77.92	78.63	6.34	%
		η_{REC}	94.1	97.71	90.32	2.5	%
	10 kΩ	V_{REC}	2.02	2.18	1.75	0.15	V
		P_{REC}	0.412	0.475	0.305	0.05	mW
		VCE	87.8	90.83	83.33	6.55	%
		η_{REC}	58.32	69.06	53.32	5.16	%

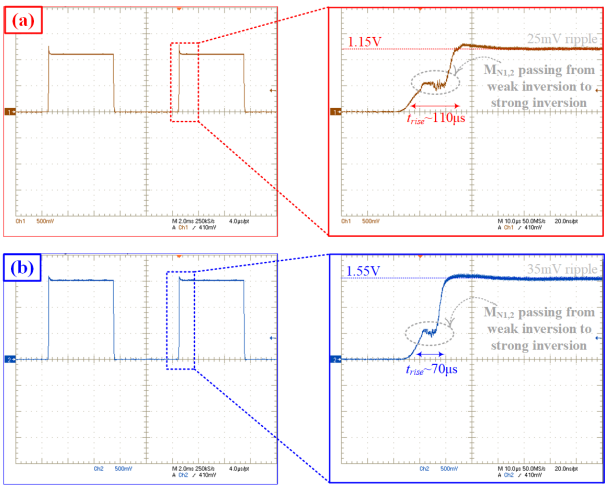

FIGURE 7. Measured dynamic response of the proposed active rectifier under $R_L = 2.4\,k\Omega$ and $C_{STOR} = 1$ nF for (a) input sine wave and (b) square sine wave. 100-Hz squared amplitude modulation is applied to V_{PZT} input voltage.

where P_{REC} is the output power and the overall time-observation period ($N \cdot T$) was set equals to 200μs, equivalent to 430 periods of the incoming AC US-energy source. Furthermore, it was also evaluated the voltage conversion efficiency, VCE by using the equation

$$VCE_{\%} = 100 \cdot \frac{V_{REC}}{|V_{AC}|} \tag{5}$$

where $|V_{AC}|$ is the value of the AC input amplitude.

The main power losses of the IC are due to the comparators, which show a static power consumption, the switching losses of transistors MN1,2 and MP1,2 and the dynamic power consumption of BUFF1,2. The CGCs power consumption is estimated through simulations and it is around 18 μW for $V_{REC} = 1.6\,V$ under 10-kΩ load resistance (sine input V_{PZT} voltage) and around 22.5 μW with the same load conditions and $V_{REC} = 2.0\,V$ with square input V_{PZT} voltage. Under $R_L = 2.4\,k\Omega$ the estimated static power consumption of CGCs is 13.5 μW and 17 μW for sine and square input voltage, respectively. The experimental results, summarized in Tab. 2 and Fig. 10 and Fig. 11, show an average maximum efficiency around 94.5% with a load resistance equal to

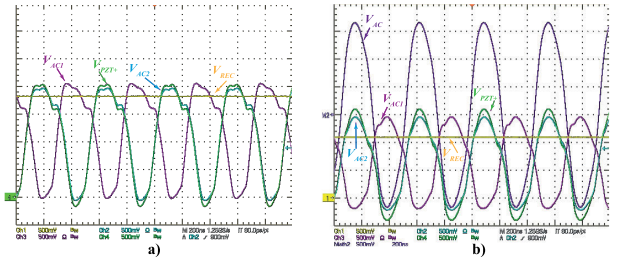

FIGURE 8. Measured voltage signals when stimulating TX-PZT with a sine wave and a) no load resistance; b) $R_L = 2.4\,k\Omega$.

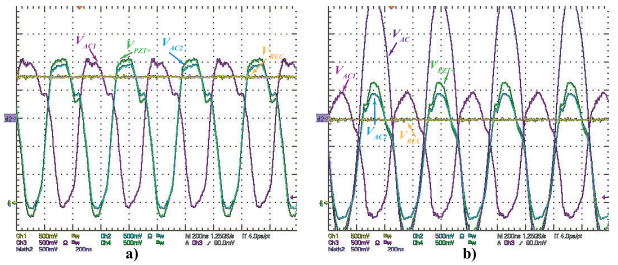

FIGURE 9. Measured voltage signals when stimulating TX-PZT with a square wave and a) no load resistance; b) $R_L = 2.4\,k\Omega$.

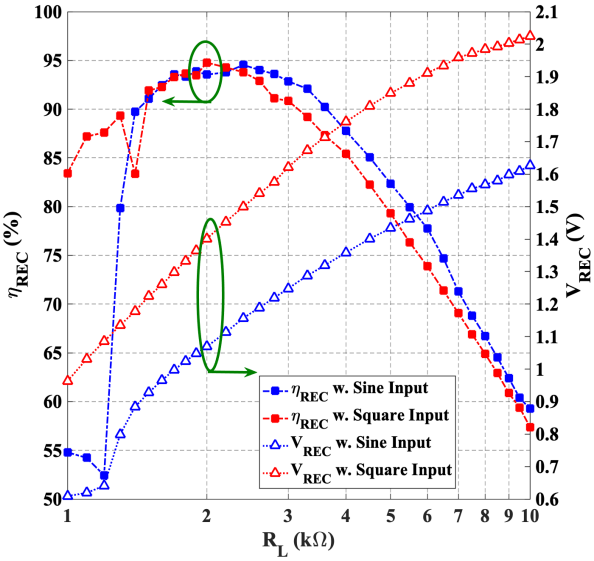

FIGURE 10. Measurements Results: η_{REC} and V_{REC} vs. load resistance, R_L. Curves for sine input voltage and square input voltage stimulation of the TX-PZT.

$R_L = 2.4\,k\Omega$ when stimulating the TX-PZT with a sine wave. It is worth noting that the average maximum η_{REC} is around 95 % when stimulating with square wave and with a load resistance is equal to $R_L = 2.0\,k\Omega$. Such result shows that square-wave TX-forcing, the simplest signal to be generated, induces the highest output power and efficiency in the receiver side. For that case, the resulting average output power is $P_{REC} \approx 1\,mW$. This improvement can be justified by the richer power spectrum generated by the TX-PZT. The error between post-layout simulations and measurement is lower than 2%. In particular, these two last performance parameters, namely η_{REC} and P_{REC} are in-line with the simulated maximum values, around 1.05 mW and

TABLE 3. State-of-the-art comparison.

Parameters	[20] TBCAS'14	[2] JSSC'15	[4] TBCAS'18	[3] CICC'18	[5] TBCAS'19	[6] TBCAS'20	[26] Access'22	[27] LSSC'23	This Work
Techn. (nm)	180	65	180	65	180	180	180	180	**28**
Freq. (MHz)	1.0	1.0	1.30	1.85	2.7	1.38	0.3	5.0	**2.15**
Distance (cm)	10.5	3.0	10.5	2.15	n.d.	n.d.	17	n.d.	**1.0**
Transd. Area (mm^2)	50.0	1.0	2.72	1.0	0.32	1.0	19.62	1.04	**1.0**
Adopt. Rect.	Half-Wave	Aux volt.	-	-	LR2RS	SR	Active	-	**ABB**
Improv.	w. ABB	Doubler	-	-	[y]	Latched	Bias-Flip	-	g_m/I_D tech.
$V_{IN,max}$ (V)	6.54	0.8	4.4	3.0	3.0	3.3	1.9	n.d.	**2.5**
VCE, max (%)	78.54 [a]	90 [b]	92 [c]	83.3 [d]	93.6 [e]	75.8 [f]	90 [g]	94.5 [h]	**87.8** [j]
P_{OUT} (mW)	25 [a]	0.1 [b]	2.14 [c]	0.12 [d]	2.27 [e]	2.29 [f]	0.40 [g]	2.405 [h]	**1.0** [i]
$\eta_{REC,max}$ (%)	82.45 [a]	89.4 [b]	71.4 [c]	82 [d]	94.5 [e]	91.8 [f]	90 [g]	92.5 [h]	**95** [i]
C_L (nF)	100	0.5	1.5	4000	10	0.1	10000	100	**10**
Area (mm^2)	0.114	0.2 [x]	0.64 [x]	NA [z]	0.09	0.0025 [x]	0.24 [x]	0.0026 [x]	**0.0045**
Power Dens. (mW/mm^2)	219.3	0.5	3.34	NA [z]	25.2	904	1.67	925	**222.2**
Fully Int.	No	Yes	Yes	No	No	Yes	No	No	**No**

[a]:@ $R_L = 10\,k\Omega$. [b]: @ $R_L = 5.1\,k\Omega$. [c]: Est. [d]: Est. $R_L = 52\,k\Omega$. [e]: @ $R_L = 30\,\Omega$. [f]: Est. @ $R_L = 2.77\,k\Omega$.
[g]:Est. $R_L = 7.25\,k\Omega$. [h]: Est. $R_L = 4.66\,k\Omega$. [i]: @ $R_L = 2.0\,k\Omega$ (average values-10 silicon prototypes). [j]: @ $R_L = 10\,k\Omega$. [x]: Est. rectifier area.
[y]: Lowering Rail-to-Rail Supply for Comparators. [z]: It can not be estimated.

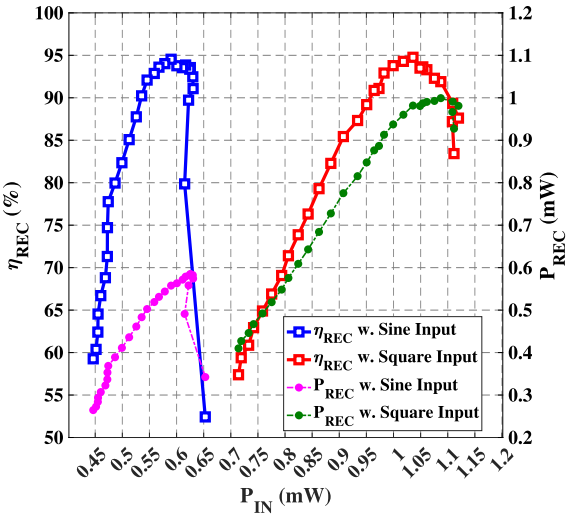

FIGURE 11. Measurements Results: η_{REC} and P_{REC} vs. input power, P_{IN}. Curves for sine input voltage and square input voltage stimulation of the TX-PZT.

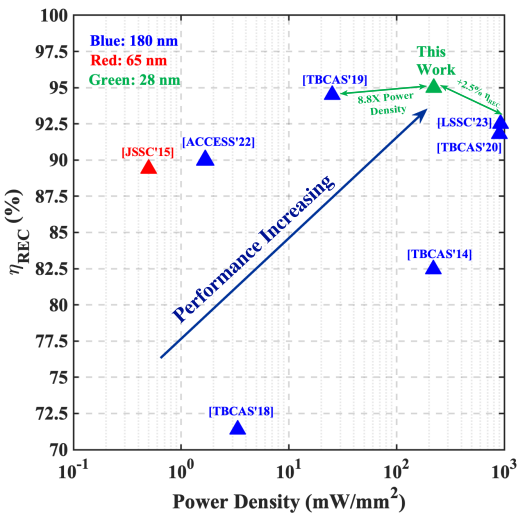

FIGURE 12. State-of-the-art comparison graph: η_{REC} vs output power density.

96 %, respectively. Furthermore, it is important to underline that no matching network is used for the RX-PZT transducer leading to the main cons of the reduction of the maximum available input power (i.e. Section II). On the other hand, the main pros is the reduction of the invasiveness of the entire electronic system avoiding, thus, the usage of bulky external capacitors and inductors or larger silicon prototype area occupation.

Tab. 3 compares the proposed active rectifier with other solutions in literature designed for the same application. From Fig. 12 it possible to observe that the proposed solution allows to obtain the best trade-off in terms of power density and power conversion efficiency within the state-of-the-art and the highest PCE compared to all the previous similar works. The adoption of US energy harvesting allows reaching higher distance of the implanted device, as confirmed by [4], [20], and [26]. In the proposed work the distance is constrained by the target application which, as detailed in Section I, is a Brain Machine Interface (BMI), surgically placed over the brain pia mater membrane.

IV. CONCLUSION

The paper reports the design and implementation of an active rectifier for implanted biomedical devices exploiting ultrasound waves for the power supply generation. Thanks to the adoption of a design procedure based on the g_m/I_D methodology, the AC/DC converter achieves the best trade-off between measured power conversion efficiency and power density. Interestingly, a better performance is measured when adopting a square-wave input to drive the transmitting piezoelectric device.

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