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RESEARCH ARTICLE

Analysis and Comparison in the Energy-Delay Space of Nanometer CMOS One-Bit Full-Adders

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ABSTRACT In this paper we analyze, design and compare six significant topologies of one-bit full adders in terms of their Energy-Efficient Curves in the Energy-Delay Space. We define the simulation strategies that are adopted to make a fair comparison even among cells with very different characteristics. Each topology is designed through a methodology which, thanks to the adoption of a circuit optimizer, allows to design the circuit under different energy-delay trade-offs and to derive the Energy-Efficient Curves. The comparison of the topologies is made using a 28 nm CMOS technology in terms of normalized Energy-Efficient Curves. In particular, plotting all these Energy-Efficient Curves in a single graph makes the comparison very effective and allows the designer to choose the best topology or discard the worst ones, at a glance.

INDEX TERMS Full adders, CMOS digital integrated circuits, energy-efficient curve, energy-delay space, VLSI.

I. INTRODUCTION

The one-bit Full Adder (OBFA) is the basic digital circuit for implementing arithmetic operations. It represents the building block to realize *n*-bit adders, fundamental structures used in DSPs and microprocessors as well as in digital compressors, comparators, parity checkers and, more in general, in digital system data-paths [1], [2]. The OBFA impacts on the critical path of the digital section that execute arithmetic operations and, since it can limit or strongly affects the overall system performance, the designer must choose the best topology conscientiously and its transistor-level design must be handled carefully. Several topologies or logic styles have been presented and used along the years for the implementation of OBFAs. At first, classical topologies used only one logic style but, in the last years, to improve the drive capability of transmission-function [3] or transmission-gate based OBFAs [1], several hybrid topologies have been proposed in the literature [4]–[10].

Since the nineties, the scientific community have tried to compare the different OBFA topologies proposed in the literature, as reported in [11], [12] or in [13], where a complete and in-depth analysis was carried out. Other systematic comparisons of more recent OBFA topologies was published in [4]–[10], [14]–[18]. All these comparisons have been carried out in terms of a single point in the Energy-Delay Space (EDS), that is, in terms of maximum speed, minimum energy, minimum power-delay product, or a combination of few similar trade-off parameters. In particular, none of them have been carried out considering the optimization of the OBFA cell in the whole EDS, which would have provided a much more complete, efficient and reliable comparison.

Due to the growing importance of energy consumption in digital systems (which, also in high-speed scenarios, leads to pursuing energy efficiency as a primary target [19], [20]) a deep understanding of the Energy-Delay (E-D) trade-offs has become crucial. To this end, since the early 2000s, the generalized figure of merit (FOM), E^iD^j, has been used to describe the performance of a digital circuit or system in the EDS, under various design trade-offs [21]–[25].

Despite the EDS should be the natural domain to compare digital circuits and systems, in the field of arithmetic operations, this approach was used in [26], only. The paper, however, managed the comparison on an architectural level

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and, in fact, it compared different architectures of n-bit full adders with no much further insight on the transistor level design of the elementary OBFA cell.

In this paper we propose a design methodology and a subsequent comparison of digital CMOS OBFA in the EDS. We consider the following six OBFA topologies

- Conventional Mirror CMOS (CMC) Full Adder;
- Complementary Pass-transistor Logic (CPL) Full Adder;
- Low-Power (LP) Full Adder;
- Transmission-Gate with Driving Capability (TGDC) Full Adder;
- New Hybrid Pass Static CMOS (NHPSC) Full Adder;
- Dual-Rail Domino (DRD) Full Adder.

They are representative of different logic styles (i.e., conventional, domino, pass transistors, hybrid, etc.) or other characteristics (i.e., single-ended versus differential structure, with versus without drive capability, etc.).

In the proposed design methodology, each OBFA topology is described in terms of appropriate parameters that are sought through a commercial optimization tool. The design process is tuned to find optimal transistor values that minimize the generalized FOM, E^iD^j, defined in terms of energy consumption per single transition and propagation delay. The optimized design leads to the Energy-Efficient Curve (EEC) that represents the locus of points in the EDS that minimize the FOM, E^iD^j, as the indices i and j vary. By a suitable normalization of the EDS, the resulting EEC is independent of the technology process and becomes a characteristic signature of the OBFA topology. Specifically, the EEC represents a powerful instrument for comparing two or more OBFA topologies under a design metric that concerns energy-delay trade-offs.

In section II we briefly describe how to use EECs to fairly compare two digital cells in the EDS. In section III we introduce a description of the six topologies under analysis. In section IV we outline the simulation strategies. In section V we exploit our design methodology to optimize each cell and derive its Energy-Efficient Curve. In section VI we make the comparison and, finally, draws the conclusion in section VII.

II. THE ENERGY-DELAY SPACE

In the digital circuit scenario, the use of FOMs that take into account trade-offs between speed and dissipation, such as the energy-delay product (ED) or the power-delay product, has always been a familiar design tool. Despite the adoption of a suitable FOM, the optimization of a digital circuit has long remained a strategy based on rules of thumb or on the designer's experience. Only in the early 2000s, an approach that allowed to explore (and optimize) a digital circuit in the various design points of the EDS was suggested in [21].

More specifically, [21] introduces the more general FOM, E^iD^j (or the equivalent ED^η, being $\eta = j/i$), so that, by changing the exponents $i \geq 0$ and $j \geq 0$ ($\eta \geq 0$), any

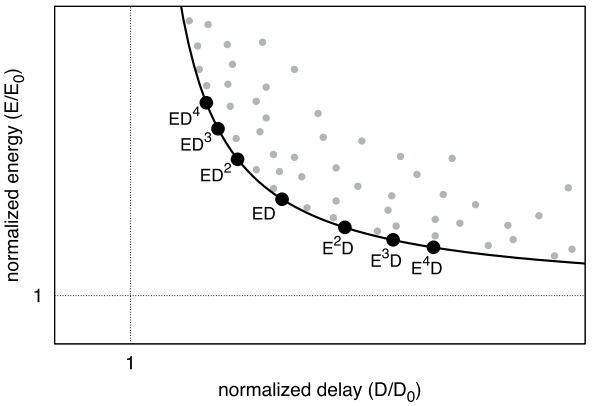


FIGURE 1. Generic energy-efficient curve (EEC) from (1). Black dots are optimum E^iD^j points. Gray dots are other possible design points in the EDS.

trade-off between power and speed could be explored. Under this FOM, the extreme cases $j/i = 0$ ($\eta = 0$) and $j/i = \infty$ ($\eta = \infty$) represent the designs with the minimum theoretical energy and delay, respectively. The paper also introduces the Energy-Efficient Curve (EEC) of a digital circuit that, for a given power supply and load, is defined as the set of points in which the circuit exhibits the minimum delay for a fixed energy dissipation or, equivalently, the minimum energy consumption for a fixed delay. Obviously, any other design point that lies above the EEC represents an inefficient design point since, for the same speed performance, a higher energy is wasted uselessly.

According to [21], the EEC in the EDS is represented by[1]

$$\left(\frac{E}{E_0} - 1\right)\left(\frac{D}{D_0} - 1\right) = 1 \tag{1}$$

and has the hyperbolic shape depicted in Fig. 1 where E_0 and D_0 are the asymptotes of the minimum theoretical energy and minimum theoretical delay, respectively. As investigated in [22], [23], real digital circuits may deviate from (1) so that the EEC was corrected into

$$\left(\frac{E}{E_0} - 1\right)\left(\frac{D}{D_0} - 1\right) = \gamma \tag{2}$$

where the constant factor γ is typically in the range $0 < \gamma \leq 1$.

As demonstrated in [21], [25], design solutions that minimize the FOM E^iD^j (or the equivalent ED^η), lie on the EEC or, which is the same, the EEC is the set of points that minimize E^iD^j (ED^η).

The EEC can be used to compare different digital circuit topologies or system architectures efficiently. Indeed, let us consider two OBFA with different transistor level topologies, named as OBFA A and B, whose EECs are plotted in Fig. 2, and focus on the delay performance, only. Assuming that the two adders A and B are represented by points A and B in the EDS, if we we limit the comparison to these two specific points, the OBFA A results faster than OBFA B,

[1]The EEC is often reported as $(E - E_0)(D - D_0) = E_0D_0$. Dividing both terms of the equation by E_0D_0 we obtain (1) in a dimensionless form.

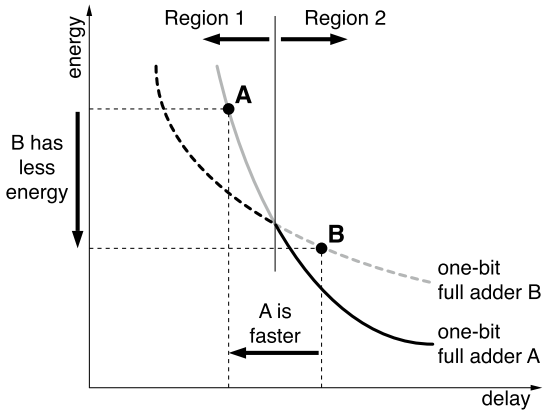


FIGURE 2. Energy-delay dependency. Continuous line: Energy-efficient curve of full adder A. Dashed line: Energy-efficient curve of full adder B.

thus leading to the erroneous conclusion that the topology A is better than B, at least in term of speed. Conversely, considering the energy-delay trade-offs outlined by the two EECs, it is apparent that not only the OBFA B has more room for speed improvement but also that the same speed can be achieved with a lower energy consumption than the OBFA A (see region 1 in Fig. 2). Similarly, if power consumption is the main design target, the OBFA A is more advantageous since it can be designed with the same energy consumption but with a lower delay than the OBFA B (see region 2 in Fig. 2).

In conclusion, to efficiently compare different OBFA topologies in term of speed, energy and energy-delay trade-offs a comparison in terms of the EECs has to be pursued.

III. FULL ADDER TOPOLOGIES ANALYZED

In this section we report and briefly describe the OBFA topologies that shall be analyzed in the rest of the paper.

The well-known *Conventional Mirror CMOS (CMC) Full Adder* is shown in Fig. 3. It is an evolution of the traditional *CMOS Full Adder* (not shown in this article) that exploits the relationship $S = ABC_i + \bar{C}_o(A + B + C_i)$ to generate the Sum output. With respect to the traditional CMOS adder, the CMC adder reduces the number of stacked transistors in both the Carry and the Sum circuits, making a better speed performance at the same power and silicon cost [27].

It is worth noting that the circuit generates the complementary signals, $\bar{S}$ and $\bar{C}_o$, that can be used directly by the subsequent adder stage thanks to the properties of the addition function

$$\bar{S} = S(\bar{A}, \bar{B}, \bar{C}_i) \tag{3a}$$

$$\bar{C}_o = C_o(\bar{A}, \bar{B}, \bar{C}_i) \tag{3b}$$

that is, the function of complemented inputs is the complement of the function. Hence, a multibit adder is implemented without any signal inversion in the carry path, as depicted in Fig. 4.

The *Complementary Pass-transistor Logic (CPL) Full Adder* is shown in Fig. 5 [28]. It is a fully differential circuit that exploits NMOS pass-transistors to process the digital signals. The Carry and the Sum signals are generated by two

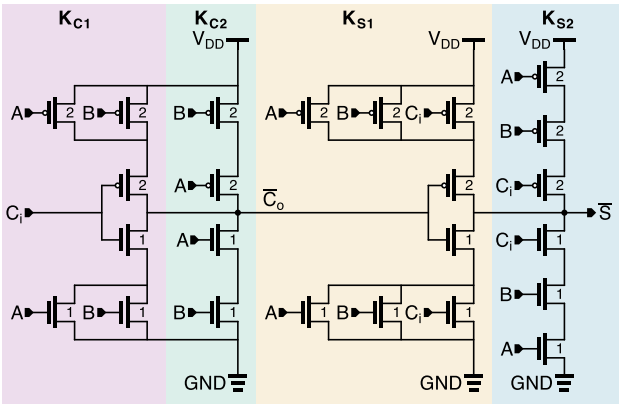


FIGURE 3. Conventional mirror CMOS (CMC) full adder. The Carry signal is generated first and is then used to generate the Sum signal. The cell generates the complementary signals, $\bar{S}$ and $\bar{C}_o$.

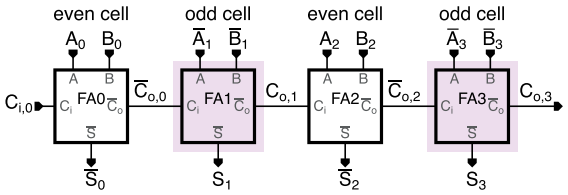
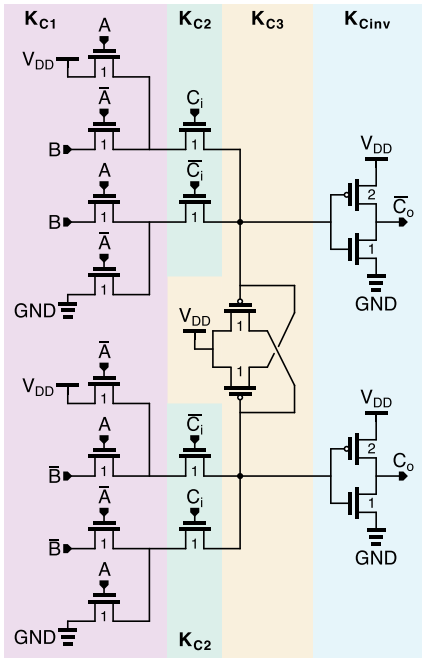


FIGURE 4. Implementation of a 4-bit adder without the inverter in the carry path.

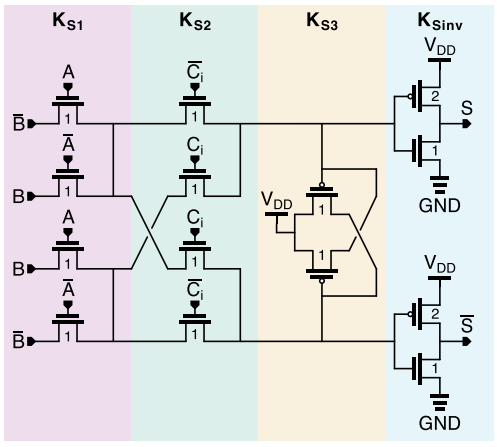
independent circuits shown in Figs. 5a and 5b, respectively. In both cases, two PMOS transistors in cross-coupled connection restore the digital levels of the processed signals before two CMOS inverters bring them to the output terminals.

The *Low-Power (LP) Full Adder* was introduced in [29] and is shown in Fig. 6. It exploits the low power xor and xnor gates reported in [30] to generate the required intermediate signals. Only two transistors of the cell are connected to the supply voltages (V_{DD} and *GND*), so, the current absorption from the supply line directly connected to the cell is very small. Most of the current (and power) comes from the input terminals that must be considered in the analysis of the power consumption. The cell, which is one of the former hybrid topology, is representative of the class of full adders without driving capability, where the output of the cell is not decoupled from the input of the subsequent one (as in pass-transistor or transmission-gate logic that do not include inverters). For this feature, the overall propagation delay of an n-bit adder, that requires the cascading connection of n full adders, is approximately proportional to n^2, a value that may become unreasonable when the summing operation involves a large number of bits [13].

The *Transmission-Gate with Driving Capability (TGDC) Full Adder* is shown in Fig. 7 [1]. It is an improved version of the original Transmission Gate cell (*TG Full Adder*, not shown in this article) introduced in [31] that, being a cell without driving capability, suffered from the propagation delay degradation problem already described for the LP case. The TGDC Full Adder solves this drawback by decoupling the output nodes with two inverters and uses a sightly better topology to obtain the intermediate signals.



(a)



(b)

FIGURE 5. Complementary pass-transistor logic (CPL) full adder. The carry and the sum signals are generated independently. The cell uses a differential logic and provides drive capability thanks to proper decoupling inverters. (a) Circuit for the generation of the Carry signal. (b) Circuit for the generation of the Sum signal.

The *NHPSC Full Adder* is shown in Fig. 8. It was proposed in [5] together with a thorough analysis of other full adder topologies having the common characteristic of being hybrid, that is, composed by a mix of transmission-gate, pass-transistor or static CMOS logic. Among the various topologies, this cell was presented as the best performing and, hence, it is chosen as representative of the class of hybrid full adders.

The *Dual-Rail Domino (DRD) Full Adder* is shown in Fig. 9 [32]. It is a fully differential topology that overcomes the limit of the classical Domino logic in the realization of inverting logic functions [33]. The Carry and the Sum signals are generated by two independent circuits shown in Figs. 9a

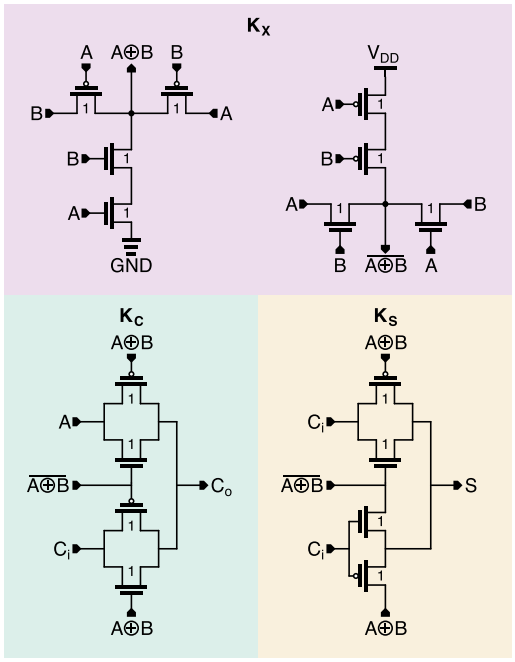


FIGURE 6. Low-power (LP) full adder. Pass-transistor logic is used to generate the Propagate signals, $P = A \oplus B$ and $\bar{P} = \overline{A \oplus B}$. They are used to drive transmission gates to generate the output signals, S and C_o.

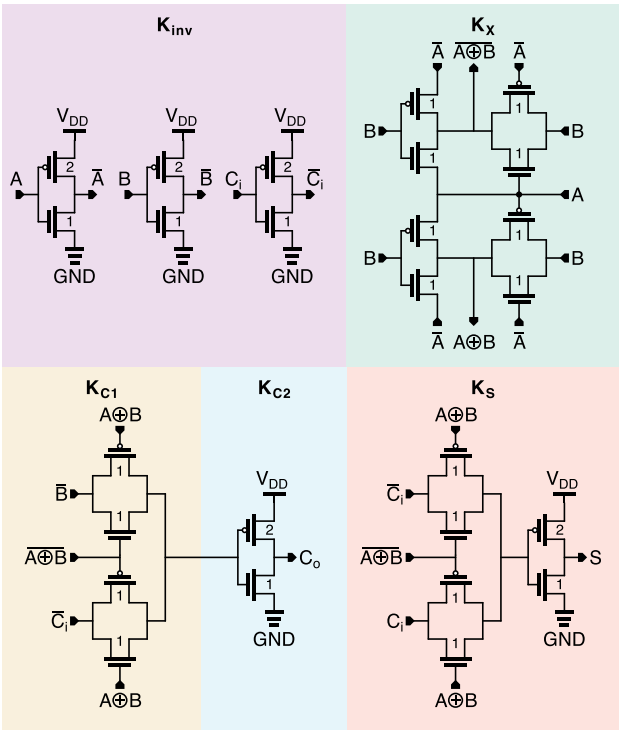


FIGURE 7. Transmission-gate with driving capability (TGDC) full adder. It uses complementary input signals that are internally generated. Transmission gate logic is used to generate the Propagate signals, $P = A \oplus B$ and $\bar{P} = \overline{A \oplus B}$. Inverters decouple the outputs from subsequent stages.

and 9b, respectively. As known, depending on the clock value, the dual-rail domino gate operates in precharge or evaluation mode. Specifically, when the clock is low, the pull-down network is disconnected from the ground, the two clock-driven

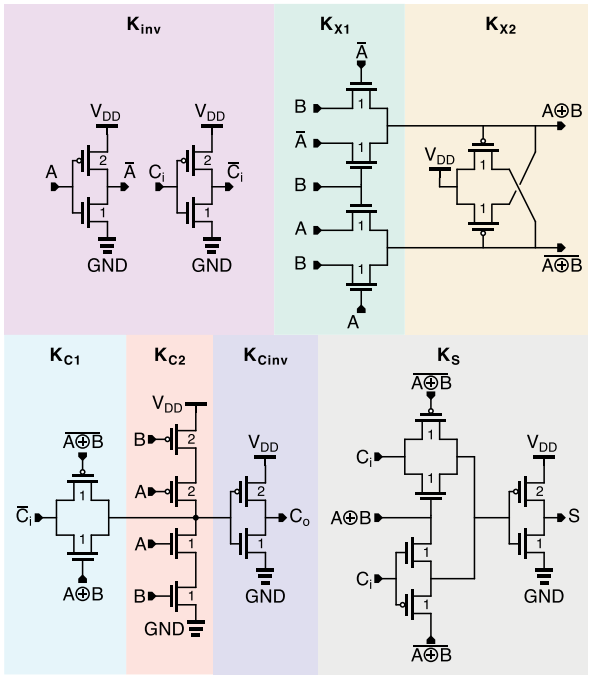


FIGURE 8. NHPSC full adder. It uses complementary input signals that are internally generated. After generating the propagate signals, $P = A \oplus B$ and $\bar{P} = \overline{A \oplus B}$, hybrid logic is used to generate the Carry and the Sum signals. Inverters decouple the outputs from subsequent stages.

PMOS transistors precharge the internal nodes to V_{DD} and the output signals are both low. When the clock rises, only one side of the pull-down network will be connected to ground and will set high the corresponding output node. The other output remains low because the corresponding node of the pull-down network is kept high thanks to a small keeper transistor [34]. It is a very fast topology that is used in high-performance circuits where power dissipation is not a concern.

IV. SIMULATION STRATEGIES

The OBFA circuits are designed in a 28-nm CMOS FD-SOI process provided by STMicroelectronics. The technology has several types of transistors but, to simplify the design and to make a fair comparison, we only use transistors with regular threshold voltage ($V_{Tn} = 330\,mV$, $V_{Tp} = -407\,mV$), for which the minimum channel size allowed by the process is $W_{min}/L_{min} = 80\,nm/30\,nm$. The power supply is maintained at the nominal level of 1 V.

As detailed in section V, each OBFA is described in terms of appropriate parameters whose values are sought through the optimization tool of the Cadence Virtuoso environment (i.e., ADE Assembler). By varying the parameter values within predefined ranges and running transient simulations, the optimization tool is able to find optimal transistor values that minimize a figure-of-merit (FOM) defined in terms of energy and delay performances. In this way, by defining a few proper FOMs as combinations of propagation delay and energy consumption per single transition, we can explore the EDS to find the Energy-Efficient Curve of the cell.

TABLE 1. Transitions that produce a commutation in C_o.

Transition #	A	B	C_i	Transition #	A	B	C_i
5	0	↑	↑	27	0	1	↑
6	0	↓	↓	28	0	1	↓
9	↑	0	↑	31	↑	↓	↑
10	↓	0	↓	32	↓	↑	↓
11	↑	↑	0	33	↑	1	0
12	↓	↓	0	34	↓	1	0
13	↑	↑	↑	35	↑	1	↑
14	↓	↓	1	37	↑	↓	↓
17	0	↑	1	38	↓	↑	↑
18	0	↓	1	44	1	↓	↓
21	↑	0	1	45	1	0	↑
22	↓	0	1	46	1	0	↓
23	↑	↑	↓	47	1	↑	0
24	↓	↓	↑	48	1	↓	0
25	↑	↑	1	49	1	↑	↑
26	↓	1	↓	56	↓	↓	↓

A. DELAY

The propagation delay is the time interval between the time the input crosses the 50% of the logic swing till the time the output crosses the same voltage level (50%). In our circuit we have three inputs and two outputs. Since the overall propagation delay of an n-bit adder is mainly determined by the carry output delay, we consider the Carry output as our relevant signal and neglect the delay between the inputs and the Sum signal. From the three inputs, we have 8 possible states each of which can commute to the remaining 7 states. So, following the procedure in [35], we have 56 relevant input transitions that can be used to compute the propagation delay. The resulting digital test pattern that generates these 56 transitions is reported in the shaded area of Fig. 10, for the input signals A, B and C_i.

Only 32 transitions of 56 toggle the Carry output signal and they are reported in Tab. 1. For example, referring to the first row of the table, in the 5th transition, signal A remains to zero while both B and C_i rise. So, the propagation delay of the 5th transition is

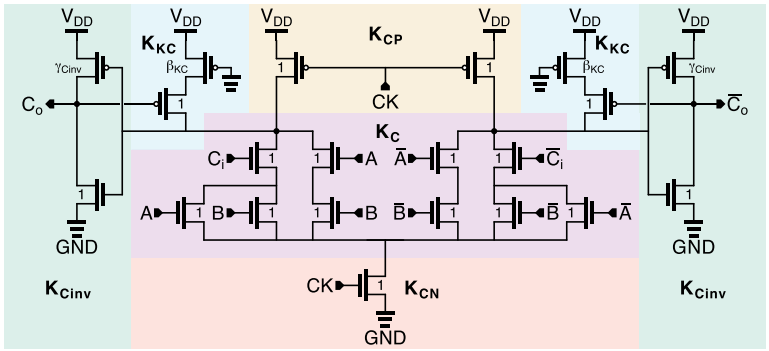
$$D_{(5)} = \min\left[\mathrm{del}(C_o, B), \mathrm{del}(C_o, C_i)\right] \tag{4}$$

being $\mathrm{del}(Y, X)$ the function that compute the propagation delay between signals Y and X and where the minimum operator ensures that the signal that toggles C_o is the closest one. Similar expressions hold for the other transitions of Tab. 1. The final propagation delay of the full adder is the maximum delay the occur considering all the transitions that toggle C_o, that is

$$D = \max_i D_{(i)} \tag{5}$$

where i refers to the i-th transition in Tab. 1 and $D_{(i)}$ is the corresponding propagation delay.

It is worth noting that the same test pattern in the shaded area of Fig. 10 is used to verify the correct functionality of each full adder cell, because it tests all possible input combinations and transitions.



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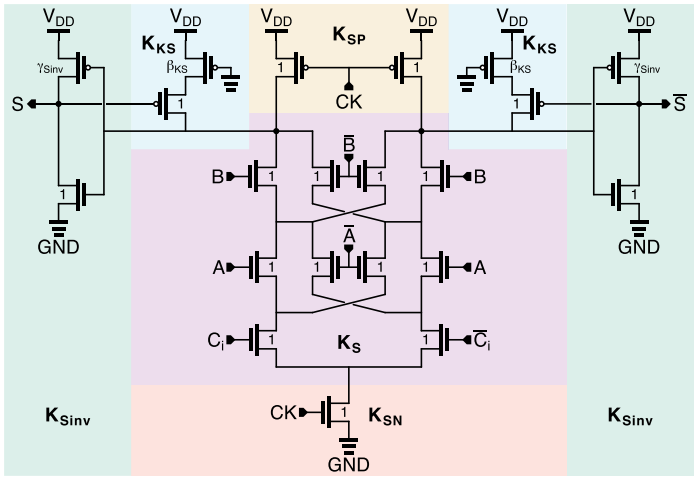

(b)

FIGURE 9. Dual-rail domino (DRD) full adder. The carry and the sum signals are generated independently. The cell uses a differential logic for which the output signals are available during the evaluation phase (CK = 1). (a) Circuit for the generation of the Carry signal. (b) Circuit for the generation of the Sum signal.

B. ENERGY

The energy consumption per single transition, E, is evaluated with the following simulation setup. We perform a transient simulation in the time interval $[0, T_f]$ driving the OBFA with a proper input pattern with N_t meaningful transitions. The interval between two consecutive transitions defines the switching frequency, $f_s = (N_t + 1)/T_f$, that is set small enough to allow each full adder output to reach the steady state for any input transition.

For any input and power supply terminal, q, we register the net power that flows into the cell as $p_q(t) = v_q(t)i_q(t)$ and integrate this value over the simulation interval, so to obtain the energy dissipated in the simulation interval for any terminal, q. Then we divide this value by the number of transitions, N_t and sum all the terminal contributions together, that is

$$E = \sum_q \frac{1}{N_t} \int_0^{T_f} i_q(t) v_q(t)\, \mathrm{d}t = \frac{T_f}{N_t} \sum_q \langle p_q(t) \rangle \qquad (6)$$

where $\langle p_q(t) \rangle = \langle v_q(t) i_q(t) \rangle$ is the average power that flows from terminal q into the cell in the time interval $[0, T_f]$.

This latter consideration allows us to relate the average power consumption per single transition, $\langle P \rangle$, to energy, E. In fact, since static dissipation is negligible with respect to dynamic one, the above-mentioned power consumption can be expressed as $\langle P \rangle = \sum_q \langle p_q(t) \rangle / N_t$, that easily leads to

$$\langle P \rangle = \frac{E}{T_f} = \frac{f_s}{N_t + 1} E \qquad (7)$$

This means that, for the same switching frequency, f_s, and input transitions, N_t, we can compare the OBFAs by indifferently using the Energy-Delay Space or the Power-Delay one, since the comparison results (and the corresponding plots) will differ by a scale factor, only. The fact that the energy consumption is completely independent of the switching frequency makes the Energy-Delay Space more convenient (and fair) for the comparison with respect to the Power-Delay one.

As established in [35] and proficiently exploited in [5], the energy consumption is evaluated using the whole input patterns reported in Fig. 10 where the portions in the light area were specifically designed to alternate low-, medium- and high-frequency sub-patterns at the three different input

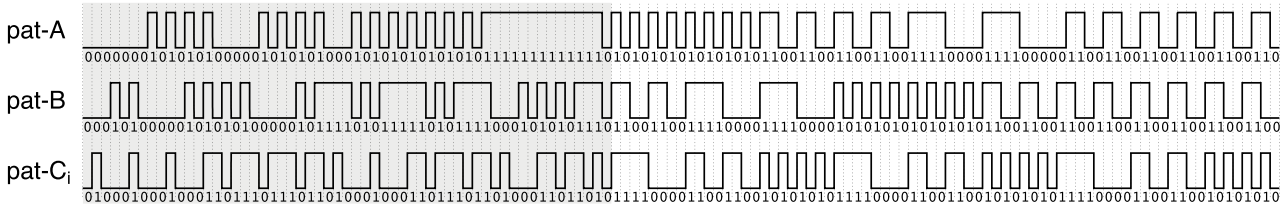

FIGURE 10. Input patterns proposed in [35]. The patterns allows to 1) check the correct functionality of the full adder cell; 2) evaluate the propagation delay considering all possible input transitions; 3) estimate the power dissipation of the full adder cell.

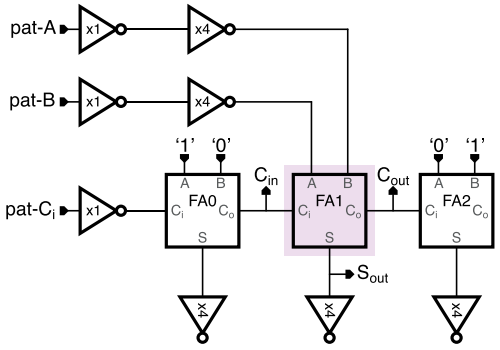

FIGURE 11. Simulation schematic for testing one-bit full adder cell.

nodes. Each stream of the pattern has a full length of 129 bits and $N_t = 128$ transitions. Assuming a negligible static dissipation, we set a 2-GHz switching frequency for our transient simulations.

Since the input waveform can appreciably alter the delay and the short-circuit power consumption, the one-bit cell of the full adder under test must be driven with realistic waveforms. The simulation schematic is shown in Fig. 11 where the full adder under test, FA1, is displayed in a shaded box. Its input terminals, A and B, are driven by the cascade of two symmetrical inverters (FO1 and FO4) that process the ideal input patterns A and B. The Carry input terminal is driven by an equal full adder in propagate mode,[2] the Carry output terminal is loaded by the Carry input of an equal full adder and the Sum terminal is reasonably loaded by a symmetrical inverter (FO4).

C. AREA

Even if it is not used as a design constraint, a comparison in terms of area occupation is also reported. The area of a OBFA circuit, A, is estimated by summing the areas $W_i \times L_i$ of each i-th transistor of the cell, that is

$$A = \sum_i W_i \times L_i \tag{8}$$

Since (8) does not include the drain and the source regions nor the extra space occupied by other layers (metallization, contacts, vias, etc.), the area estimation, A, can strongly differ from the actual area occupation. However, at a first approximation, if we assume that the area contribution of the other layers is proportional to A, we can still use this result to compare the different OBFA topologies in terms of relative area occupation.

[2]If the full adder FA0, that drives the full adder under test, does not invert the Carry signal, the input pattern of C_i is complemented.

D. NORMALIZATION

To compare the different OBFA topologies in a manner that is independent of the adopted technology, the energy, the delay and the area estimation are normalized with respect to proper reference values. The energy reference value, E_0, is defined as the energy dissipated by a symmetrical minimum-size unloaded inverter (i.e., $W_p = 2W_n = 2W_{\min}$, $L = L_{\min}$ and $C_L = 0$ F) in one clock cycle. The delay reference value, D_0, is defined as the average propagation delay[3] of a symmetrical FO4 inverter driven by a minimum-size inverter and loaded by a symmetrical FO16 one. This represents the delay of one element in a tapered chain buffer with FO4. The area reference value, A_0, is defined as the gate area of a minimum size transistor ($W_{\min} \times L_{\min}$).

In our FD-SOI 28-nm process we obtain the following normalization values

$$E_0 = 183.4 \cdot 10^{-18} \text{ J} \tag{9a}$$
$$D_0 = 13.5 \cdot 10^{-12} \text{ s} \tag{9b}$$
$$A_0 = 2400 \text{ nm}^2 \tag{9c}$$

V. DERIVATION OF THE ENERGY-EFFICIENT CURVES

To extract the EEC of the OBFA topologies we design each cell in the Cadence environment. All the OBFA cells, reported in Figs. 3 and 5–9, are partitioned into different sections, each identified by a different background color and a specific parameter (i.e., $K_{C1}, K_{C2}, \ldots$) that represents the relative size of the transistors in the section with respect to the minimum size, $W_{\min}/L_{\min}$. In addition, each transistor is marked with a number that represents its relative size in the section. So, for example, referring to Fig. 3, the size of NMOS transistors in section K_{C1} is $K_{C1} \times W_{\min}/L_{\min}$, while the size of PMOS transistors in the same section is $2 \times K_{C1} \times W_{\min}/L_{\min}$. In this manner we use a single parameter for the section but we specify, also, that the ratio between the PMOS and the NMOS transistors is 2 (to compensate the reduced mobility of holes). Observe that, if we set $L = L_{\min}$, these relative sizes affect only transistor widths.

Once the circuit is arranged, we find the EEC by seeking the parameters that minimize some specific FOMs in a reasonable space of values. Such FOMs are the delay, the energy and five significant energy-delay combinations in the form E^iD^j. The minimization process results in seven design points that are referred to as $D_{\min}$, ED^3, ED^2, ED, E^2D, E^3D

[3]It is the average of the propagation delay measured at the rising and at the falling edge of the gate.

TABLE 2. CMC full adder at different EEC design points. Normalized delay ($\mu \pm \sigma$), Energy ($\mu \pm \sigma$), Area estimation and design parameters.

Index	D/D_0	E/E_0	A/A_0	K_{C1}	K_{C2}
$D_{\min}$	1.82 ± 0.12	10.7 ± 0.17	111.0	5.50	6.00
ED^3	1.89 ± 0.12	8.98 ± 0.16	85.5	4.00	4.00
ED^2	1.94 ± 0.13	8.49 ± 0.16	78.0	3.50	3.50
ED	2.03 ± 0.13	8.01 ± 0.16	70.5	3.00	3.00
E^2D	2.37 ± 0.16	7.08 ± 0.15	55.5	2.00	2.00
E^3D	2.72 ± 0.18	6.66 ± 0.15	48.0	1.50	1.50
$E_{\min}$	3.46 ± 0.24	6.30 ± 0.13	40.5	1.00	1.00

and $E_{\min}$. The exploration of the EDS for the minimization of the FOMs is carried out by using the "Global Optimization" tool of the Cadence Virtuoso simulation environment and by varying some specific parameters of the cell (i.e., K_{C1}, K_{C2},...) in proper design ranges. As a final step, for each E^iD^j design point, Monte Carlo simulations are carried out to check the robustness of the OBFA against inter-die (global) process variations.

A. CMC FULL ADDER

The CMC full adder, shown in Fig. 3, is partitioned into four sections corresponding to four parameters that should be explored by the minimization process. However, some practical design considerations allow us to reduce the space of the parameters values (and the simulation time) drastically. In particular, as we mentioned in Section IV, the overall propagation delay of an n-bit adder is not affected by the delay of the Sum signal. Hence, the two parameters that refer to the Sum generation section (i.e., K_{S1} and K_{S2}) can be set to 1, since this minimizes the energy dissipation without affecting the propagation delay of the cell. Therefore, the minimization process concerns K_{C1} and K_{C2}, only, that ranges in the interval [1, 10] with a step of 0.5.

Tab. 2 shows the results of the minimization process. The first column identifies the design point specifying the index minimized by the tool. The subsequent three columns report the normalized delay, the normalized energy (both in terms of average and standard deviation, $\mu \pm \sigma$) and the normalized area estimation. The remaining two columns report the parameters that refer to the Carry generation section.

The standard deviations of delay and energy are not derived from the minimization process and are evaluated, for each of the seven optimal design points, by subsequent 100-run Monte Carlo simulations that account for inter-die (global) variations. Considering all the optimal design points, the relative standard deviation (σ/μ) of the normalized delay ranges from 6.3% to 6.9% while, for the normalized energy, it ranges from 1.6% to 2.3%.

The plot of the EEC in the normalized EDS is shown in Fig. 12. Gray dots represent the simulation points explored by the minimization process. Black circles are the simulation points found by the optimization tool during the minimization of a specific FOM. In the EEC the ratio between the maximum and the minimum delay is 1.9, a value quite close to the ratio between the maximum and the minimum energy that is 1.7. Therefore, we can say that the curve is well balanced since it equally spans over the energy and the delay. This makes the CMC topology suitable for general purpose full adders and, in fact, is frequently implemented in many libraries of digital standard cells.

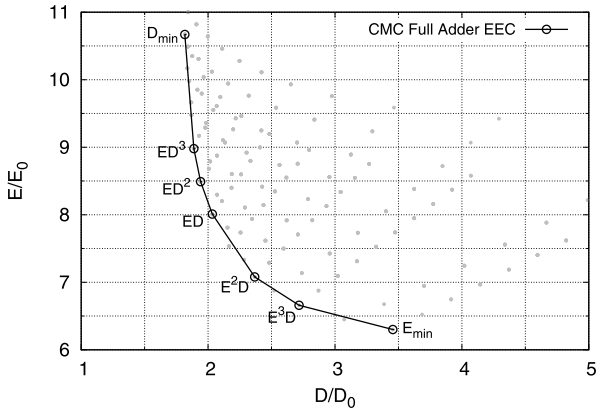

FIGURE 12. Energy-efficient curve of the CMC full adder. Gray dots: simulation points explored by the minimization process. Black circles: simulation points found by the minimization process.

B. CPL FULL ADDER

The CPL Full Adder topology has two separate subcircuits for the Carry and the Sum generation, depicted in Figs. 5a and 5b, respectively. Each subcircuit is partitioned into four different sections. Parameters $K_{C1,2,3}$ with $K_{C\text{inv}}$ affect the Carry subcircuit while $K_{S1,2,3}$ with $K_{S\text{inv}}$ act on the Sum subcircuit. To reduce the exploration space, all the parameters of the Sum subcircuit are set to 1, since this minimizes the energy consumption without affecting the propagation delay. The minimization tool is set with parameters K_{C1}, K_{C2} and $K_{C\text{inv}}$ that can range in the interval [1, 10] with a 0.5-step while K_{C3} can range in the interval [1, 2] with the same step size. The different range for K_{C3} is due to the fact that the cross-coupled PMOS transistors are introduced just to restore the logic levels and, generally, their size is very small. Note that, since the CPL full adder is a differential circuit, the test circuit in Fig. 11 is modified consistently and each single-ended signal is replaced with its differential counterpart. The propagation delay is evaluated considering the worst value among the outputs and its complemented value.

The results of the minimization process are shown in Tab. 3 where the last four columns report the parameters that refer to the Carry generation section. After the minimization process, to confirm the robustness of the design, a series of Monte Carlo simulations (100 runs each) are performed considering inter-die (global) variations. As a result, considering all the optimal design points, the relative standard deviation (σ/μ) of the normalized delay ranges from 5.4% to 6.3% while, for the normalized energy, it ranges from 2.5% to 2.8%.

The plot of the EEC in the normalized EDS is shown in Fig. 13. In the EEC the ratios between the extreme values of delay and energy are 1.21 and 1.24, respectively. Although the curve is balanced, the two smaller ratios make the CPL topology less flexible with respect to the CMC case.

TABLE 3. CPL full adder at different EEC design points. Normalized delay ($\mu \pm \sigma$), Energy ($\mu \pm \sigma$), Area estimation and design parameters.

Index	D/D_0	E/E_0	A/A_0	K_{C1}	K_{C2}	K_{C3}	$K_{C\text{inv}}$
$D_{\min}$	1.70 ± 0.10	13.4 ± 0.34	96.0	7.00	2.50	1.00	2.00
ED^3	1.73 ± 0.10	12.3 ± 0.33	83.0	6.00	2.00	1.00	1.50
ED^2	1.73 ± 0.10	12.2 ± 0.33	79.0	5.50	2.00	1.00	1.50
ED	1.84 ± 0.10	11.3 ± 0.31	66.0	4.50	1.50	1.00	1.00
E^2D	1.86 ± 0.10	11.1 ± 0.31	58.0	3.50	1.50	1.00	1.00
E^3D	1.97 ± 0.12	10.9 ± 0.30	52.0	3.00	1.00	1.00	1.00
$E_{\min}$	2.05 ± 0.13	10.8 ± 0.29	44.0	2.00	1.00	1.00	1.00

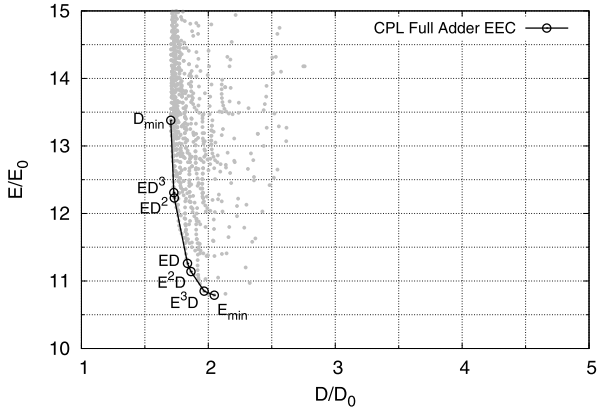

FIGURE 13. Energy-efficient curve of the CPL full adder. Gray dots: simulation points explored by the minimization process. Black circles: simulation points found by the minimization process.

TABLE 4. LP full adder at different EEC design points. Normalized delay ($\mu \pm \sigma$), Energy ($\mu \pm \sigma$), Area estimation and design parameters.

Index	D/D_0	E/E_0	A/A_0	K_X	K_C
$D_{\min}$	2.47 ± 0.15	8.59 ± 0.16	84.0	8.00	4.00
ED^3	2.49 ± 0.15	7.66 ± 0.15	68.0	6.50	3.00
ED^2	2.56 ± 0.15	7.10 ± 0.14	58.0	5.50	2.50
ED	2.69 ± 0.17	6.52 ± 0.14	48.0	4.50	2.00
E^2D	3.65 ± 0.26	5.27 ± 0.13	28.0	2.50	1.00
E^3D	3.88 ± 0.26	5.14 ± 0.13	24.0	2.00	1.00
$E_{\min}$	4.61 ± 0.33	5.05 ± 0.13	20.0	1.50	1.00

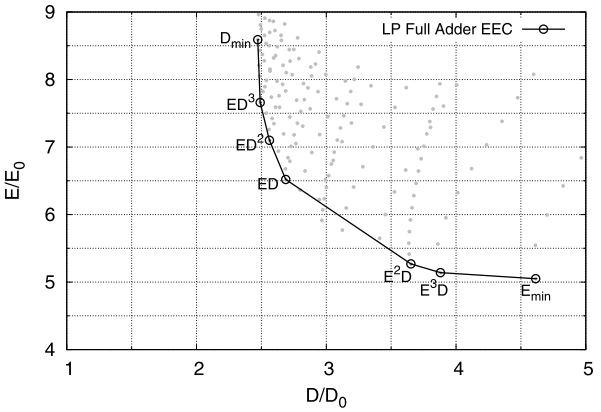

FIGURE 14. Energy-efficient curve of the LP full adder. Gray dots: simulation points explored by the minimization process. Black circles: simulation points found by the minimization process.

C. LP FULL ADDER

The LP Full Adder topology in Fig. 6 is partitioned into three sections each identified by a different background color and a specific parameter. Parameter K_X refers to the section that performs the xor/xnor of the two inputs, A and B. Parameter K_C affects the Carry section while K_S defines the transistors of the Sum section.

Since the propagation delay is independent of K_S, we set it to 1, to minimize the energy dissipation, and find the EEC by exploring the EDS in a reasonable range of values for K_X and K_C. With these latter parameters ranging in the interval $[1, 10]$ with a 0.5-step, the minimization process leads to the results shown in Tab. 4. Subsequent Monte Carlo simulations shows that the relative standard deviation (σ/μ) of the normalized delay ranges from 5.9% to 7.2% while, for the normalized energy, it ranges from 1.9% to 2.6%. The corresponding EEC plot is shown in Fig. 14 in the normalized EDS. In the EEC the ratios between the extreme values of delay and energy are 1.87 and 1.7, respectively, that make the LP topology suitable for general purpose full adders as for the CMC one.

D. TGDC FULL ADDER

The TGDC Full Adder topology in Fig. 7 is partitioned into five sections. Parameter K_{inv} refers to the section that inverts the input signals. Parameter K_X refers to the section that performs the xor/xnor of the two inputs, A and B. Parameters $K_{C1,2}$ affect the Carry section while K_S defines the transistors of the Sum section. Since the propagation delay is independent of K_S, we set this parameter to 1, to minimize the energy dissipation, and find the EEC by exploring the EDS in a reasonable range of values for the remaining parameters. Ranging them in the interval $[1, 5]$ with a 0.25-step, the minimization process yields the results shown in Tab. 5. It is worth noting that the minimizations of the three low-energy indices (i.e., E^2D, E^3D and $E_{\min}$) lead to the same solution with minimum size transistors. Monte Carlo simulations confirm the robustness of the design and reveal that the relative standard deviation (σ/μ) of the normalized delay ranges from 5.7% to 6.6% while, for the normalized energy, it ranges from 1.6% to 2.2%.

The corresponding EEC plot is shown in Fig. 15 in the normalized EDS. In the EEC, the ratios between the extreme values of delay and energy are 1.19 and 1.6, respectively. This means that the TGDC topology is not well balanced because the energy variation of the EEC is higher than the delay one. In other words, any improvement in the delay is not paid at the expense of a similar amount of energy.

E. NHPSC FULL ADDER

The NHPSC Full Adder topology in Fig. 8 is partitioned into seven sections each identified by a different background color and a specific parameter. Parameter K_{inv} refers to the section that inverts the input signals. Parameters K_{X1} and K_{X2} refer to the section that performs the xor/xnor of the two inputs, A and B. Parameters K_{C1}, K_{C2} and $K_{C\text{inv}}$ affect the Carry section while K_S defines the transistors of the Sum section. Since the propagation delay is independent of K_S, we set this parameter to 1 and find the EEC by exploring the EDS in a reasonable range of values for the remaining parameters.

TABLE 5. TGDC full adder at different EEC design points. Normalized delay ($\mu \pm \sigma$), Energy ($\mu \pm \sigma$), Area estimation and design parameters.

Index	D/D_0	E/E_0	A/A_0	K_{inv}	K_X	K_{C1}	K_{C2}
D_{min}	2.70 ± 0.17	13.0 ± 0.21	75.8	3.00	3.25	2.25	2.25
ED^3	2.82 ± 0.16	9.80 ± 0.19	46.5	1.75	1.75	1.25	1.50
ED^2	2.92 ± 0.17	9.10 ± 0.18	40.5	1.50	1.50	1.00	1.25
ED	3.09 ± 0.19	8.34 ± 0.18	33.3	1.25	1.00	1.00	1.00
E^2D	3.20 ± 0.21	8.12 ± 0.18	31.0	1.00	1.00	1.00	1.00
E^3D	3.20 ± 0.21	8.12 ± 0.18	31.0	1.00	1.00	1.00	1.00
E_{min}	3.20 ± 0.21	8.12 ± 0.18	31.0	1.00	1.00	1.00	1.00

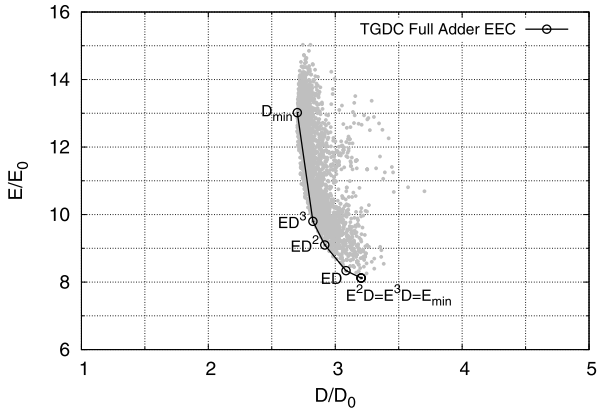

FIGURE 15. Energy-efficient curve of the TGDC full adder. Gray dots: simulation points explored by the minimization process. Black circles: simulation points found by the minimization process.

TABLE 6. NHPSC full adder at different EEC design points. Normalized delay ($\mu \pm \sigma$), Energy ($\mu \pm \sigma$), Area estimation and design parameters.

Index	D/D_0	E/E_0	A/A_0	K_{inv}	K_{X1}	K_{X2}	K_{C1}	K_{C2}	K_{Cinv}
D_{min}	3.12 ± 0.19	16.0 ± 0.32	79.0	2.00	6.50	2.50	4.00	2.00	3.00
ED^3	3.15 ± 0.18	13.3 ± 0.28	60.0	1.50	5.00	2.00	2.50	1.50	2.00
ED^2	3.25 ± 0.20	11.3 ± 0.25	44.5	1.00	3.50	1.50	2.00	1.00	1.50
ED	3.44 ± 0.21	10.2 ± 0.24	38.5	1.00	2.50	1.00	1.50	1.00	1.50
E^2D	3.72 ± 0.24	9.57 ± 0.23	34.0	1.00	2.00	1.00	1.00	1.00	1.00
E^3D	3.72 ± 0.24	9.57 ± 0.23	34.0	1.00	2.00	1.00	1.00	1.00	1.00
E_{min}	3.96 ± 0.27	9.52 ± 0.24	32.0	1.00	1.50	1.00	1.00	1.00	1.00

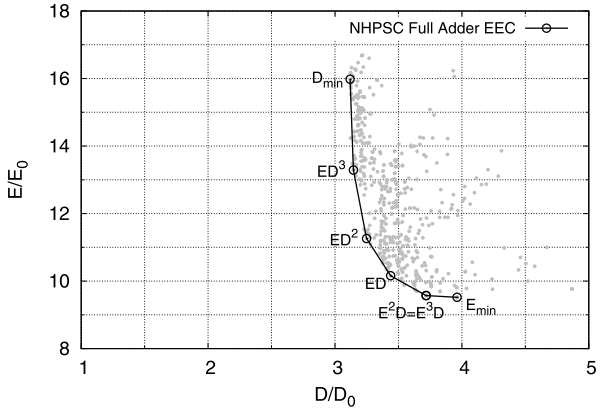

FIGURE 16. Energy-efficient curve of the NHPSC full adder. Gray dots: simulation points explored by the minimization process. Black circles: simulation points found by the minimization process.

Parameters K_{X1} and K_{C1} range in the interval [1, 10] while the remaining parameters range in the interval [1, 5], all with a 0.5-step.

The minimization process yields the results shown in Tab. 6. It is worth noting that the minimizations of two low-energy indices (i.e., E^2D, E^3D) lead to the same solution. Monte Carlo simulations report that the relative standard deviation (σ/μ) of the normalized delay ranges from 5.7% to 6.8% while, for the normalized energy, it ranges from 2.0% to 2.5%. The corresponding EEC plot is shown in Fig. 16 in the normalized EDS. In the EEC, the ratios between the extreme values of delay and energy are 1.27 and 1.68, respectively. As for the TGDC case, also the NHPSC topology is not well balanced since any improvement in the delay requires a higher amount of energy with respect to other balanced solutions.

F. DRD FULL ADDER

The DRD Full Adder topology in shown in Fig. 9. As for the CPL, the cell uses fully differential logic and is made up of two separate subcircuits for the Carry and the Sum generation. The two subcircuits are partitioned into five different sections. Referring to the Carry subcircuit in Fig. 9, parameter K_C sets the sizes of transistors of the pull-down network. K_{CN} and K_{CP} set the sizes of NMOS and PMOS clock-driven transistors, respectively. K_{KC} and β_{KC} define the sizes of the keeper devices, implemented with degenerated PMOS transistors. Finally, K_{Cinv} and γ_{Cinv} determine the size of the two output inverters. This latter parameter allows one to make the PMOS transistor wider than the NMOS one since, as known, DRD logic requires high-skewed output stages [36], [37]. Similar considerations hold for the Sum generation subcircuit, in Fig. 9b.

The space of parameter values can be drastically reduced by some practical design considerations. Referring to the Carry subcircuit, the trade-off between noise immunity and speed depends on the ratio (R_K) between the saturation current of the keeper and the saturation current of the pull-down network, that is [34], [38]

$$R_K = \frac{I_K}{I_{PDN}} \approx \frac{\mu_p \frac{K_{KC} W_{min}}{\left(1+\frac{1}{\beta_{KC}}\right) L_{min}}}{\mu_n \frac{K_C W_{min}}{2L_{min}}} \tag{10}$$

A good compromise is setting $R_K \sim 0.1$ and, as suggested in [34], it is done by setting the lower transistor at the minimum size (i.e., $K_{KC} = 1$) and by adjusting the upper one according to (10), that is

$$\beta_{KC} = \frac{1}{2\frac{\mu_p}{\mu_n}\left(\frac{1}{R_K K_C} - 1\right)} \tag{11}$$

In practice, we set the width of the upper transistor at the minimum width, W_{min}, and set its length as stated by

$$L_{upper} = \left(\frac{1}{R_K K_C} - 1\right) L_{min} \tag{12}$$

where $\mu_n/\mu_p \sim 2$ is assumed.

As a second design consideration, the speed of the Carry subcircuit is not affected by the size of the clock-driven PMOS transistors nor by the size of the NMOS transistors of the output inverters. Therefore, we set $K_{CP} = K_{Cinv} = 1$ and use γ_{Cinv}, K_C and K_{CN} as free design parameters.

TABLE 7. DRD full adder at different EEC design points. Normalized delay ($\mu \pm \sigma$), Energy ($\mu \pm \sigma$), Area estimation and design parameters.

Index	D/D_0	E/E_0	A/A_0	K_C	K_{CN}	$\gamma_{P\text{inv}}$
$D_{\min}$	1.28 ± 0.09	31.48 ± 0.97	86.5	3.00	15.0	5.00
ED^3	1.30 ± 0.10	29.93 ± 1.03	81.0	3.00	13.5	4.00
ED^2	1.34 ± 0.10	27.75 ± 0.85	71.5	2.50	11.0	3.50
ED	1.45 ± 0.10	25.01 ± 0.76	61.0	2.00	9.00	2.50
E^2D	1.70 ± 0.13	22.46 ± 0.60	49.5	1.50	4.50	2.00
E^3D	2.16 ± 0.16	20.60 ± 0.62	42.0	1.00	3.00	1.50
$E_{\min}$	2.82 ± 0.22	19.71 ± 0.58	38.0	1.00	1.00	1.00

As far as the Sum subcircuit is concerned, this is not critical for speed. Therefore, we use minimum size transistors for the pull-down network section and all the clock-driven devices (i.e., $K_S = K_{SN} = K_{SP} = 1$). Parameter β_{KS} is set from (11), using $K_S = 1$ instead of the free parameter K_C. Finally, parameter $\gamma_{S\text{inv}}$ is set equal to the free parameter $\gamma_{C\text{inv}}$.

With respect to the other full adder structures, the simulation of the DRD cell requires some modifications. To obtain a realistic waveform, the clock terminal of the cell (not shown in the simulation schematic in Fig. 11) is driven by the cascade of two symmetrical inverters (FO1 and FO4), that process an ideal squared clock signal. A second difference is that the carry propagation delay does not depend on the rising/falling edges of A and B since these signals are already stable when the clock signal goes high. This implies that the propagation delay of C_{out} must be evaluated with respect to changes on C_{in} and the clock, only. In addition, transitions that produce a commutation in C_{out} are different from those established in Tab. 1. Finally, the clock terminal is included in the evaluation of the energy defined in (6).

The minimization tool is set up with K_C ranging in the interval $[1, 5]$, K_{CN} ranging in the interval $[1, 20]$ and $\gamma_{C\text{inv}}$ ranging in the interval $[1, 6]$, all with the same step size of 0.5. The minimization process leads to the results shown in Tab. 7. Monte Carlo simulations turn up that the relative standard deviation (σ/μ) of the normalized delay ranges from 6.9% to 7.8% while, for the normalized energy, it ranges from 2.7% to 3.4%. The corresponding EEC plot is shown in Fig. 17 in the normalized EDS. In the EEC, the ratios between the extreme values of delay and energy are 2.24 and 1.72, respectively. In this case, since the ratio of the delay is higher than the ratio of the energy, the delay can be improved at the expense of a lower increment of energy, contrarily to the cases of the TGDC and NHPSC topologies.

VI. COMPARISON

To compare all the full adder topologies that were analyzed in section V, we plot their EECs in Fig. 18. The figure is very effective since, on the basis of delay requirements and energy budget, it allows one to choose the best topology at a glance. The figure also illustrates which topologies should be avoided when the main design metric concerns energy-delay trade-offs.

If the energy budget is low and the delay is not a concern, the best solution seems to be the LP topology, which, as discussed in section V-C, is suitable for general purpose

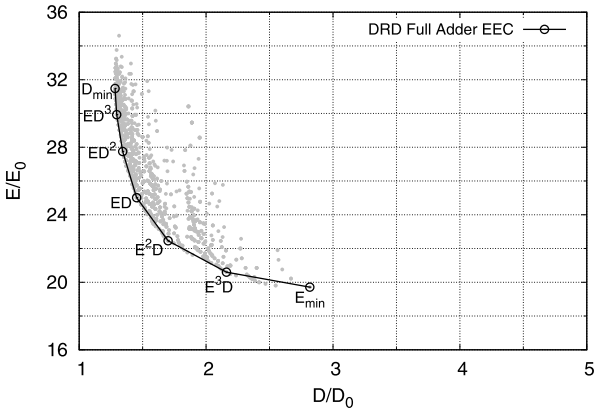

FIGURE 17. Energy-efficient curve of the DRD full adder. Gray dots: simulation points explored by the minimization process. Black circles: simulation points found by the minimization process.

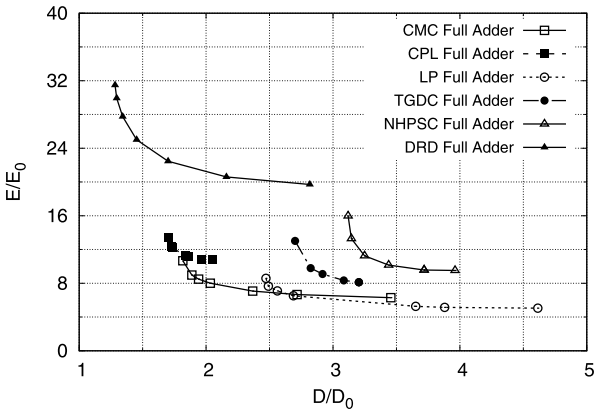

FIGURE 18. Full adder comparison in terms of energy-efficient curve.

full-adders. In this case, the LP design space that ranges from ED to $E_{\min}$ has certainly the lowest energy dissipation but this energy advantage is easily lost for practical n-bit adders because, due to the lack of drive capability, the propagation delay increases with the square of the number of cells. This latter consideration makes the CMC topology the preferred choice over the LP one for the design of n-bit adder architectures. Of course, using a LP topology for high-speed applications is unreasonable.

In the medium range of the EDS, the CMC full adder is an excellent compromise also because its well-balanced EEC makes it suitable for general purpose full adders (in fact, the CMC topology is regularly included in many digital standard cell libraries). For it, the design space that ranges from $D_{\min}$ to E^2D has the best performance over the other topologies.

In the field of high-speed topologies, the CPL full adder exhibits a delay lower than the CMC topology and becomes competitive in the design space that ranges from $D_{\min}$ to ED^2. Conversely, the CPL topology should not be used in low-power contexts since its performance are poor in the space that ranges from ED to $E_{\min}$. The ECC extends on a small portion of the EDS and, as discussed in section V-B, although well-balanced, the CPL topology is less flexible with respect to others so its energy/delay advantage can be proficiently exploited in few specific cases, only.

TABLE 8. Full adder comparison in terms of relative standard deviation for normalized delay and energy.

Full adder topology	D/D_0		E/E_0	
	$[\sigma/\mu]_{min}$	$[\sigma/\mu]_{max}$	$[\sigma/\mu]_{min}$	$[\sigma/\mu]_{max}$
CMC	6.3%	6.9%	1.6%	2.3%
CPL	5.4%	6.3%	2.5%	2.8%
LP	5.9%	7.2%	1.9%	2.6%
TGDC	5.7%	6.6%	1.6%	2.2%
NHPSC	5.7%	6.8%	2.0%	2.5%
DRD	6.9%	7.8%	2.7%	3.4%

If speed is the primary requirement and the power dissipation is unimportant, the DRD full adder has the absolute lowest delay performance, obviously paid in terms of the highest power dissipation. Since its dissipation is from 2 to 3 times higher than that of a CPL cell, the DRD full adder should be used prudently and only in the design space that ranges from D_{min} to ED, where the speed is worth the price paid in terms of dissipation. As highlighted in section V-F, since the ratio between the maximum and the minimum delay is higher than the ratio between the maximum and the minimum energy, the DRD topology allows one to improve the delay at the expense of a moderate increase of energy and, therefore, it is more convenient to design it for maximum speed.

The plot in Fig. 18 also illustrates which topologies are disadvantageous in terms of energy-delay trade-offs. Specifically, based on the discussion reported in section II, it is apparent that the TGDC and the NHPSC full adders do not offer any advantage over other topologies. Indeed, any design point of their EECs can always be replaced by a more efficient design point of a different topology that exhibits either the same propagation delay at the cost of a lower energy dissipation or the same energy dissipation with a lower propagation delay. Furthermore, as reported in sections V-D and V-E, since the ratio between the maximum and the minimum delay is lower than the ratio between the maximum and the minimum energy, any improvement in the delay is not paid at the expense of a similar amount of energy.

Finally, for the different OBFA topologies, Tab. 8 shows a summary of the relative standard deviation (σ/μ) that concern delay and energy. By comparing the minimum and maximum values of the relative standard deviations, we can conclude that all the topologies analyzed have a similar robustness with respect to process variations.

VII. CONCLUSION

In this paper we compared six significant topologies of one-bit full adders in terms of their Energy-Efficient Curves in the Energy-Delay Space. After a brief description of each full adder cell, we defined the simulation strategies that were adopted to make a fair comparison even among cells with very different characteristics (i.e., single-ended versus differential structure, with versus without drive capability, etc.).

In the paper we introduced a design methodology to optimize a full adder cell in terms of some significant FOMs in the form E^iD^j. In the specific, each topology was partitioned into different sections, each identified by a specific parameter that represents the relative size of the transistors in the section with respect to the minimum size, W_{min}/L_{min}. These specific parameters were fed to a circuit optimizer to find the design points that minimized the FOMs and allowed us to carry out the EEC of the cell.

All the EECs were plot in a single graph thus making a very effective comparison that allows the designer to choose the best topology or to reject the worst ones, at a glance. On the basis of the comparison, the CMC full adder is an excellent choice over other low-power solutions based on transmission gates or hybrid topologies (i.e., LP, TGDC, NHPSC). Furthermore despite the DRD full adder exhibits the lowest delay (less than 25% and 30% of CPL and CMC cells, respectively), it has two to three times more power consumption than CPL and CMC topologies, when designed for maximum speed.

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