UNIVERSITY OF CATANIA | STMicroelectronics

DEPARTMENT OF CHEMICAL SCIENCES

INTERNATIONAL Ph.D. IN CHEMICAL SCIENCES

Matteo Barcellona

4H-SiC Deep Trench Etch: Investigation of Chemical and Physical Approaches to Surface Damage Recovery

Ph.D. Dissertation

Ph.D. Coordinator:
Prof. Salvatore Sortino

Supervisor:
Prof. Maria Elena Fragalà

XXXVI CYCLE
2020-2023

I am become death,
the destroyer of worlds.

J. Robert Oppenheimer

Dedicated to those
who work tirelessly to
achieve scientific advancements
for good and ethical purposes.

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Philosophy Doctoral Dissertation

International Ph.D. in Chemical Sciences, XXXVI cycle, 2020-2023

4H-SiC Deep Trench Etch: Investigation of Chemical and Physical Approaches to Recovery Surface Damage

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UNIVERSITY OF CATANIA, 2023

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Abbreviations

AC	Alternated Current
AFM	Atomic Force Microscopy
AR	Aspect Ratio
BCD	Bottom Critical Dimensions
BE	Binding Energy
BET	Brunauer-Emmett-Teller
BEV	Battery Electric Vehicles
BJT	Bipolar Junction Transistor
BSE	BackScattering Electrons
CCD	Charge Coupled Device
CD	Critical Dimension
CMOS	Complementary Metal–Oxide–Semiconductor
CMP	Chemical Mechanical Polishing
CVD	Chemical Vapor Deposition
CW	Clockwise
DC	Direct Current
DI	Deionized
DLS	Dynamic Light Scattering
DOE	Design Of Experiments
DRIE	Deep Reactive Ion Etching
ECE	Electrochemical Etching
ECR	Electron Cyclotron Resonance
EDX	Energy Dispersive X-Ray
EV	Electric Vehicles
FAB	Fabrication plant
FE	Field Emitting
FET	Field Emitting Transistor
FIB	Focused Ion Beam
GBS	Giant Bunching Steps
HMO	Hard Mask Oxide
IC	Integrated Circuit
ICE	Internal Combustion Engine
IGBT	Insulated Gate Bipolar Transistor
IGFET	Insulated Gate Field Emitting Transistor
INF	Inferior
IV	Intensity-Voltage
JFET	Junction Field Emitting Transistor
KE	Kinetic Energy
MACE	Metal Assisted Chemical Etching
MAPCE	Metal-Assisted PhotoChemical Etching
MEMS	Micro Electro-Mechanical Systems
MESFET	Metal-Semiconductor Field-Effect Transistor
MID	Middle

MOS	Metal Oxide Semiconductor
MOSFET	Metal Oxide Semiconductor Field Emitting Transistor
NPs	Nanoparticles
NRs	Nanorods
OX	Oxidation
PdI	Polydispersity Index
PSI	Paul Scherrer Institute
PtP	Peak-to-Peak
QDR	Quick Dump Rinsing
RA	Roughness Average
RDS	Drain-Source on Resistance
RED	Reduction
RIE	Reactive Ion Etching
RMS	Root Mean Square
RR	Relative Roughness
RSM	Responsive Surface Method
RTA	Rapid Thermal Annealing
SD	Standard Deviation
SE	Secondary Electrons
SEM	Scanning Electron Microscopy
SPM	Scanning Probe Microscopy
SUP	Superior
TCD	Top Critical Dimension
TOC	Total Organic Carbon
UMOSFET	U-shaped Metal Oxide Field Emitting Transistor
USA	United States of America
UV	Ultraviolet
VDMOS	Vertical Double-Diffused Metal-Oxide Semiconductor
VMOSFET	V-shaped Metal Oxide Field Emitting Transistor
WBG	Wide Band Gap
WCE	Wet Chemical Etching
XPS	X-Ray Photoelectron Spectroscopy

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Abstract

Quick and new actions are needed to fight climate change. European legislators are trying to solve the problem in the short or medium term. One of the European actions is to promote the electrification of vehicles. This leads to an increasing demand for the production of electronic devices and the expansion of the fabrication plant (FAB) in European countries.

STMicroelectronics, the largest microelectronic company in Europe, is actively pushing the advancement of high-performance and energy-efficient devices. In particular, this thesis focuses on the evolution of a trench MOSFET device and its initial stages of development. The novelty of the work lies in the adoption of 4H-SiC as a material to obtain better performance and withstand higher voltages.

The adoption of 4H-SiC material, instead of the well-established silicon, poses many challenges due to its chemical inertia, high hardness, and poor state of the art. 4H-SiC has only recently been used in microelectronics and is still a material to be fully discovered. The problems encountered in the early stages of trench MOSFET development were specifically investigated and resolved by morphological and surface chemical analysis. The main characterization techniques used were Scanning Electron Microscopy (SEM) and Atomic Force Microscopy (AFM) for morphological evaluation, and X-ray Photoelectron Spectroscopy (XPS) for qualitative and quantitative evaluation of the surface chemical composition. In particular, micrographs were used to perform image analysis and to obtain important pieces of evidence.

Although 4H-SiC is chemically inert and the microelectronic industry primarily focuses on physical dry etching techniques, investigations of wet chemical etching approaches have been conducted on 4H-SiC. For this purpose, Electrochemical Etching (ECE) and Metal Assisted Chemical Etching (MACE) were effective for various applications on 4H-SiC. These methods of etching might be useful in the future for batch processing and speeding up the production of the devices. In addition, the ECE application provides an opportunity to study the top-down production of particles of 4H-SiC with potential applications in biomedical, mechanical, and sensor technology.

The doctoral thesis is categorized into physical and chemical approaches for 4H-SiC etching, and these approaches will be comprehensively discussed in this text. In virtue of its physicochemical characteristics, silicon carbide has launched numerous challenges and offers prospects for future academic and industrial research opportunities.

Preface

Nowadays, climate change must be fought with decisive changes. The competent institutions adopt decisive laws in order to reduce the carbon emissions derived from the industry to the automotive fields (i.e. the Euro emission standards). Occasionally, the Internal Combustion Engine (ICE) vehicles of the last generation help reduce pollution, but hybrid and fully electric vehicles are playing a major role, indeed e-bikes, e-cars, e-train, and even e-trucks are more common today than before. Replacing a ten-year-old gasoline car with a new hybrid car of the same class would reduce lifecycle CO_2 emissions by 40%. In particular, emissions from Battery Electric Vehicles (BEVs) would be 80% lower than ICE vehicles in Europe, 40% lower in China, and 60% lower in the U.S., while BEVs completely eliminate dangerous NOx [1]. For this reason, in the last few years, the interest in EVs has risen exponentially.

The growing EVs market is having an exponential rise since there is an increasing vehicle electrification level, as reported in Fig. 1.1. It is expected an increase of 60% in China, and a lower 45% in the United States by 2030. It is predicted that there will be a significant increase in sales share percentage in Europe, from 19% in 2022 to 71% in 2030. The main reasons lie in the new environmental laws, the tightening of the ICs vehicles, and the recognized convenience behind the use of EVs.

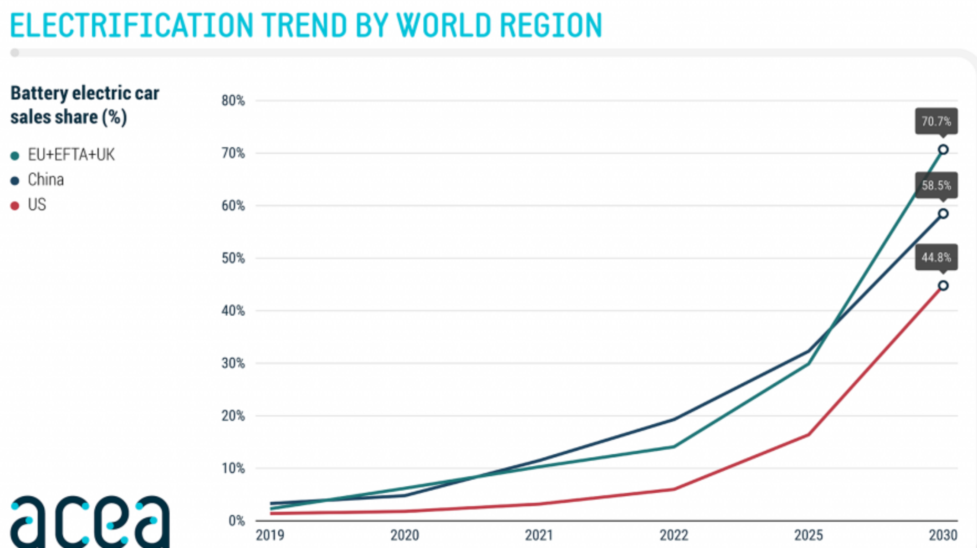


Fig. 1.1 Electrification level of vehicles growing with time [2]**. All rights reserved to ACEA, S&P Global Mobility.**

EVs are mainly composed of three components: batteries, the electric traction motor, and the power electronics system. In particular, a significant portion of the electronics compartment is

allocated to the primary inverter, which converts the battery's DC power into AC power for the electric traction motor. The power switching technologies, which devices are called transistors, are going through a period of huge developments. In particular, the 4H-SiC Metal Oxide Semiconductor Field-Effect Transistor (MOSFET) technologies offer many advantages over the consolidated Si-based Insulated Gate Bipolar Transistors (IGBTs).

The leader in the EV market sector is Tesla, which first implemented the 4H-SiC MOSFET transistor in the Model 3 in 2018, buying the components from *STMicroelectronics* [3]. The 97% energy efficiency achieved in the 1-in-1 power module guarantees lower weight and consequently less consumption [4]. The EV industry also requires more sophisticated electronic devices that can withstand high voltages, high frequencies, and high temperatures. To this end, Silicon Carbide (SiC) is emerging as a Wide Band Gap (WBG) semiconductor that guarantees the ability to maintain high performance. In fact, SiC is involved in many applications: from power supplies, motor control, photovoltaic converters, and telecommunications to robotics, electric/hybrid vehicles, traction, and grid control [5]. Although its excellent properties, the state of the art of SiC is still immature, despite many years of research and improvements that are emerging day by day.

Aims of the Work and Experiences

Initial stages of a trench MOSFET based on 4H-SiC material were followed. The device development sees the processes, techniques, and methodologies that were originally developed for silicon. Processing 4H-SiC presents novel challenges that require rapid actions while aiming for optimal and conclusive outcomes.

The present Ph.D. project involves the study of the very first stages of a trench MOSFET device, ranging from annealing surface protection to trench quality recovery. The present thesis will shed light on the use and optimization of the microelectronic industry's typical techniques while trying to explain the observed phenomena on the basis of the acquired pieces of evidence, and furthermore trying to place suggestions for other applications of 4H-SiC and its manipulation. Basically, two fundamental stages of the trench MOSFET fabrication were part of this study:

- The carbon capping protection layer is applied to the 4H-SiC after doping for high-temperature annealing. The atom mobility of 4H-SiC below 1600 °C is low and high-temperature are required. However, this results in the occurrence of physical surface phenomena that lead to the quality degradation of the material and the device. For this reason, a carbon cap layer is put on the surface to repress the phenomena and obtain a high-quality surface even after the high-temperature annealing treatments.
- The wall recovery after manufacturing of high-aspect-ratio trenches, formed using the DRIE technique. Along the walls of the trenches, the 4H-SiC experiences striation formation alongside typical silicon scallops. To perform high-quality surfaces, methods of dry gas etching and sacrificial oxidation were employed and optimized. For this purpose, an internally developed method of image analysis permitted us to evaluate the walls' roughness and speed up the optimization process.

The Ph.D. project results from the *STMicroelectronics Catania* and the *University of Catania* joint collaboration with the aim to address the above-mentioned issues, making use of their facilities and equipment. The above-mentioned treatment studies have been mainly focused on the morphological and chemical features of the surface.

It is also possible to discern the present thesis work into two further parts:

- Physical methodologies of 4H-SiC manipulation performed at *STMicroelectronics Catania* and at the Department of Chemical Sciences of the *University of Catania*. To some extent, the microelectronics industry prefers the dry physical approaches because they produce no chemical waste. The activities involved the recovery of trenches by H_2 gas etching and dry sacrificial oxidation. Our objective was to obtain flattened trench walls with reduced defectivity and lattice

inhomogeneity. At the same time, the optimization of the physical etching approaches had an eye on the resultant modification of the geometric sizes of the system according to the desired device layout.

- Wet chemical approaches of 4H-SiC etch followed at the Department of Chemical Sciences of the *University of Catania*, at the *Paul Scherrer Institute* in Switzerland, and at the *GREMAN* laboratories in France as part of a 4-month visiting research period during the third year of the doctoral research experience. Traditional chemical wet etching experiments were performed on 4H-SiC despite the characteristic chemical inertia of the material. The inertia issues have been exceeded by electrochemical etching and electrodeless methods of 4H-SiC attack. The thesis sheds light on the basic principles and issues of the techniques since there is no extensive scientific literature behind them. Lastly, the electrochemical etching executed on 4H-SiC was useful to produce nanoparticles on a top-down approach. This line of research was more academic and less oriented to the microelectronic industry, highlighting the multi-applicability of silicon carbide.

During the third year of my Ph.D., I gained valuable knowledge about the electrochemical etching approach at the *Paul Scherrer Institute* in Switzerland. The collaboration with the *GREMAN* Laboratories in France, specifically with the research group of *Prof. Gaël Gautier*, *Prof. Thomas Defforge*, *Prof. Brice Le Borgne*, and colleagues was particularly fruitful due to their expertise in silicon electrochemical and electrodeless etching. The experiments on Electrochemical Etching (ECE) and Metal-Assisted Chemical Etching (MACE) on 4H-SiC were conducted at the *GREMAN* Laboratories facilities.

1. Introduction

1.1. Integrated Circuit and MOSFETs

In the past, electric device components were connected by wires from one to another. The novelty arrived in 1985 after *Jack Kilby* of *Texas Instruments* demonstrated the first integrated circuit (IC) [6,7]. Each component of the chip was built into a single Germanium (Ge) block, eliminating the need for interconnecting wires and resulting in a more compact design. Continuous development of more complex ICs followed since the first. The IC technology opened the door to more suitable electronic device mass-production thanks to the benefits in terms of lower costs and production ease [8]. According to the famous *Moore's la*w (of *Dr. Gordon E. Moore*), in a single chip, the number of transistors doubles every two years. This prediction has been surprisingly accurate, the reason why electric devices achieve better performances year after year. In fact, as reported in Fig. 1.1, the number of transistors per IC chip grew from a few thousand in 1975 to almost 50 milliards in 2020.

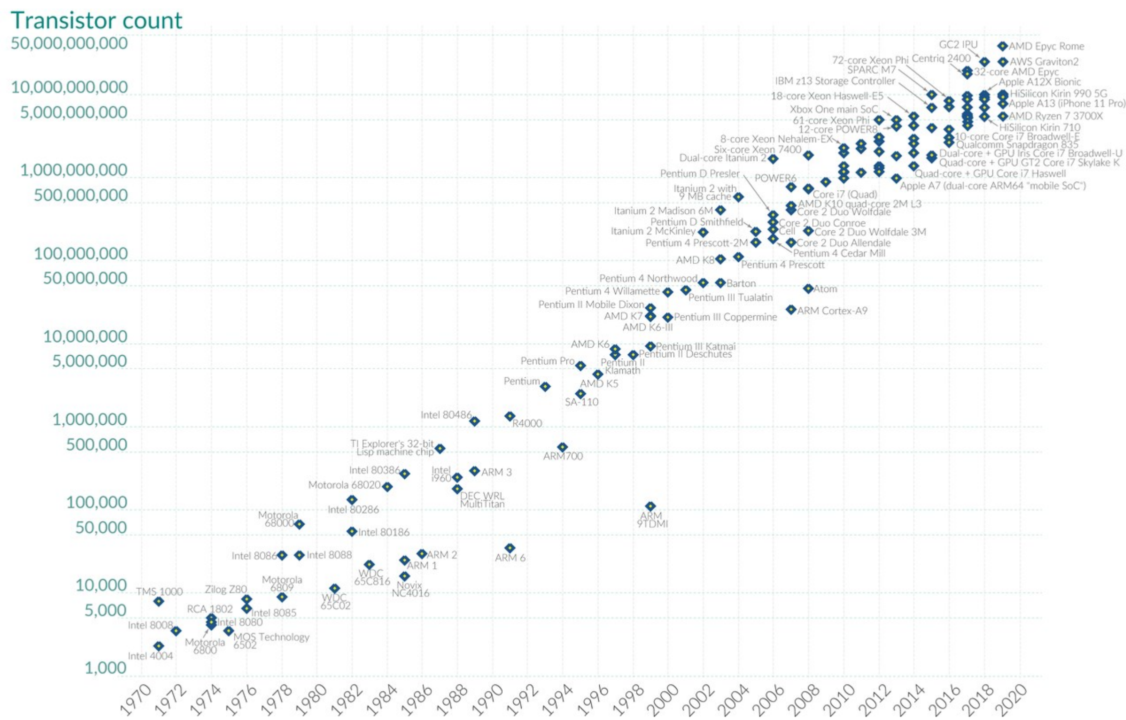


Fig. 1.1 The number of transistors on integrated circuits increment from 1975 to 2020 according to Moore's law [9]**. Under CC BY 4.0, all rights are reserved to Max Roser and Hannah Ritchie.**

The increase in transistor density is attributable to the decrease in transistor size. In 1971, the typical size was 10 μm [10]. However, nowadays, the size has impressively decreased to 3 nm [11],

and we are awaiting the emergence of the 2 nm technology expected by 2024 or 2025 [12,13]. ICs realization is made step-by-step following different fabrication processes [6] but, not all of these will be examined in this doctoral dissertation:

- Thermal oxidation
- Photomasks and photolithography
- Etching
- Diffusion
- Ion Implantation
- Metallization, bonding, and packaging

To note how the listed processes are commonly employed in every device fabrication of the microelectronics industry.

For example, the listed processes are used to manufacture transistors, electrical devices that allow for modulation of both electrical signal and power. At least, three terminals are connected to the external circuit, namely source, drain, and gate. The device architecture can vary but two major transistor types can be recognized: the Bipolar Junction Transistor (BJT) and the Junction-Field Effect Transistor (JFET). The modulation of the electrical signal is achieved by varying the gate current intensity (BJT) or the voltage (JFET). Besides the transistor type, in the philosophy of IC devices, layers of different materials, doping, and concentrations follow each other to obtain a specific architecture. One major distinction between the Junction Field-Effect Transistor (JFET) and the Bipolar Junction Transistor (BJT) is the type of carriers utilized in regulating the output. The BJT makes use of both electrons and holes (majority and minority carriers), whereas the JFET works only with the majority or minority carriers at once depending on the doping type [14]. The author invites the readers to consult the suggested books to deepen the main features of semiconductor materials [15,16]. Among the JFET type, stricter discrimination follows corresponding to the device architecture. The Complementary Metal–Oxide–Semiconductor (CMOS), the Metal-Semiconductor Field-Effect Transistor (MESFET), and the Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET) are some of the possible architectures [7]. The research of the present doctoral project is focused on MOSFET. The variety of possible device architecture can be seen as a funnel-shaped set, where among the MOSFET type, a lot of variants exist. Among them, a closer look at trench MOSFET will follow.

The Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET) is one of the most used among all the possible transistor architectures. Because of the presence of an insulating layer, another less common name is adopted: Insulated-Gate Field-Effect Transistor (IGFET). Among the MOSFET types, two sub-categories can be recognized: depletion and enhancement MOSFETs. In

the depletion-type (see Fig. 1.2), the substrate is a slab of p-type semiconductor in which two n-type regions are connected via metallic contacts (source and drain). The gate is made of an insulator (originally SiO_2 but high dielectric insulators are constantly under research) between the metal contact and the n-channel region of the substrate. The insulator-metal oxide thickness is about 500 nm in the source and drain region, whereas it is thinner, with 5-200 nm, in the gate region [14]. The higher thickness helps prevent breakdowns and allows for the application of higher voltages. The insulator ensures no electrical contact between the gate terminal and the channel.

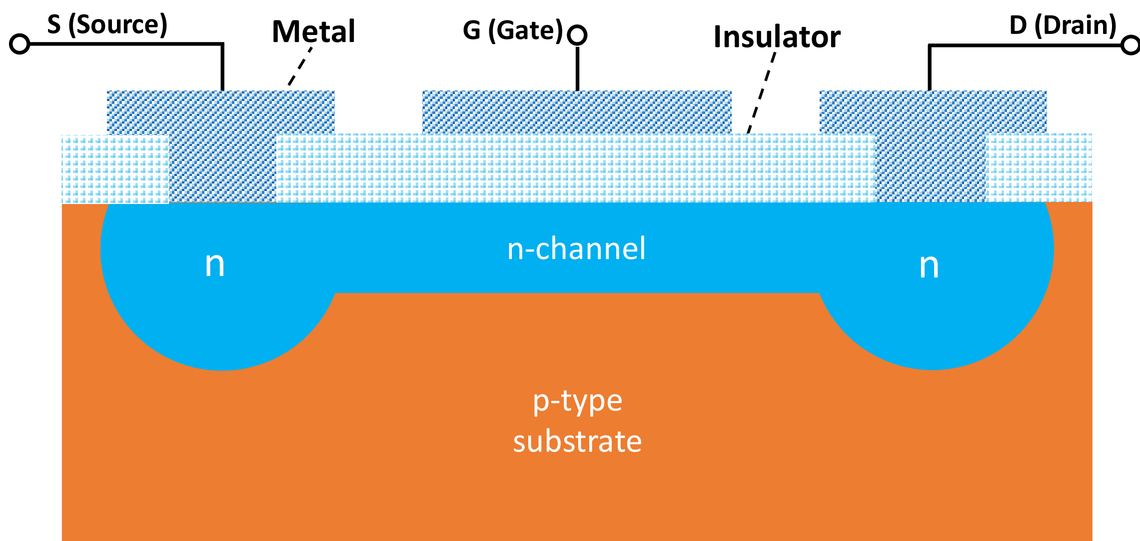


Fig. 1.2 n-channel depletion-type MOSFET illustration.

When no potential is applied to the gate and a voltage is applied between the drain and the source, electrons move from the source to the drain, resulting in the flow of an electrical current in the opposite direction of the electrons' movement. The modulation of the electrical current is achieved when a potential is applied to the gate. In the case of a negative voltage to the gate, a depletion of electrons in the n-channel leads to the migration of the holes from the p-type portion of the substrate. The depletion is the result of the electric field of 1-5 MV/cm [14]. Fewer electrons can reach the drain from the source, due to the depleted channel, and a decrease in current intensity is observed. Conversely, a positive potential to the gate leads to the migration of electrons from the p-type region to the n-channel and an increase of current intensity takes place. Another configuration of MOSFET provides the absence of the n-channel doped region between the n-doped region under the source and drain (see Fig. 1.3). This configuration is named enhancement-type MOSFET.

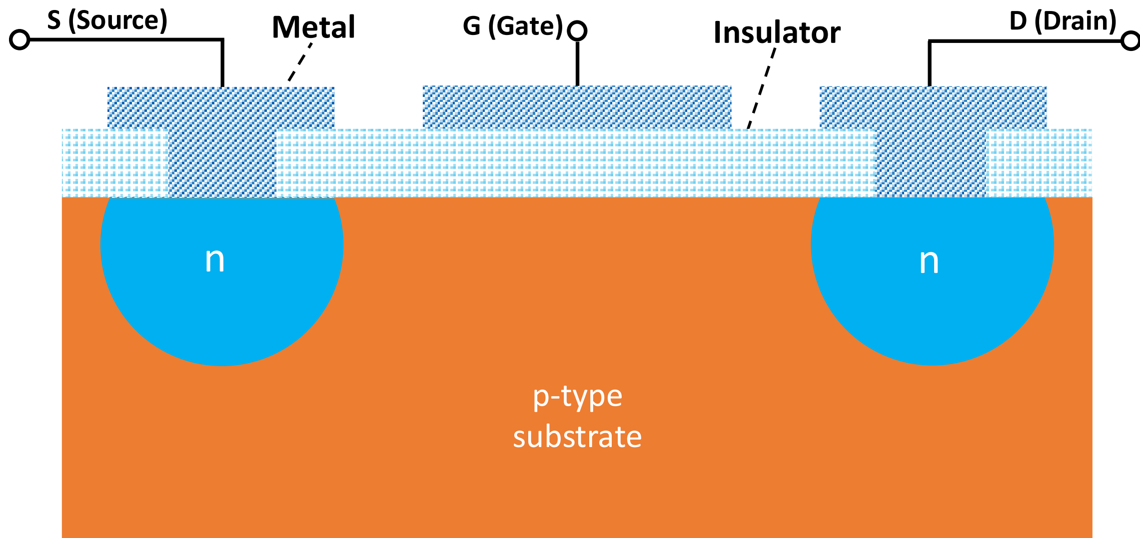


Fig. 1.3 Enhancement-type MOSFET illustration.

After applying a potential between the source and the drain, no current intensity is detectable unless a potential is applied to the gate. This is due because of the absence of the n-channel, in other words, there is no path for the electrons to flow from the source to the drain, as the opposite of the depletion-type MOSFET. Instead, when a positive voltage is applied to the gate, the majority carriers of the p-type portion under the insulator are repelled (positively charged holes), while the minority carriers (the electrons) are attracted up to the insulator portion of the gate. Obviously, the electrons are unable to pass through the gate because of the low electrical conductivity of the insulator. Finally, an n-channel is established by the increasing flow of minority carriers of the substrate with the increasing voltage to the gate, therefore the prefix enhancement-type of the MOSFET. The potential that guarantees a significant increase in the drain current is named threshold voltage.

1.2. Trench MOSFETs

After the 70s, BJT-based devices for power switch applications were outdone by MOSFET as a result of some limitations encountered through the years. BJTs suffered from low switch speed [17–19], thermal runaway [20], second breakdown [21,22], and demanded high base drive currents [23]. However, MOSFET guarantees high-speed switching [24], high input impedance, and the possibility to scale down the device without electrical conduction issues or thermal runaway. To enhance the performances, different MOSFET architectures were developed, and the trench MOSFET was among the emerged structures that accomplished the purpose. They found large applications in electronic devices, automobiles, motor drives, and lithium-ion battery control devices [25].

Initially, the planar MOSFET architecture was developed to provide extensive blocking voltage and fast switching speed, making it suitable for most applications. However, the architecture soon encountered problems as on-resistance ($RD_{S(on)}$) increased asymptotically with the density of cells, as shown in Fig. 1.4. The demand for greater performance along with the need for miniaturization has led to an increase in cell density. The automotive industry requires smaller and lighter devices to be produced. The possibility of building the device vertically enabled a remarkable reduction of the cell pitch, which consequently increased the cell density [26,27]. The breakthrough arrived with the development of the V-shaped MOSFET and the trench MOSFET. Herein, the RD_S(on) decreases with the cell density (Fig. 1.4) leading to good future prospects of performance increment.

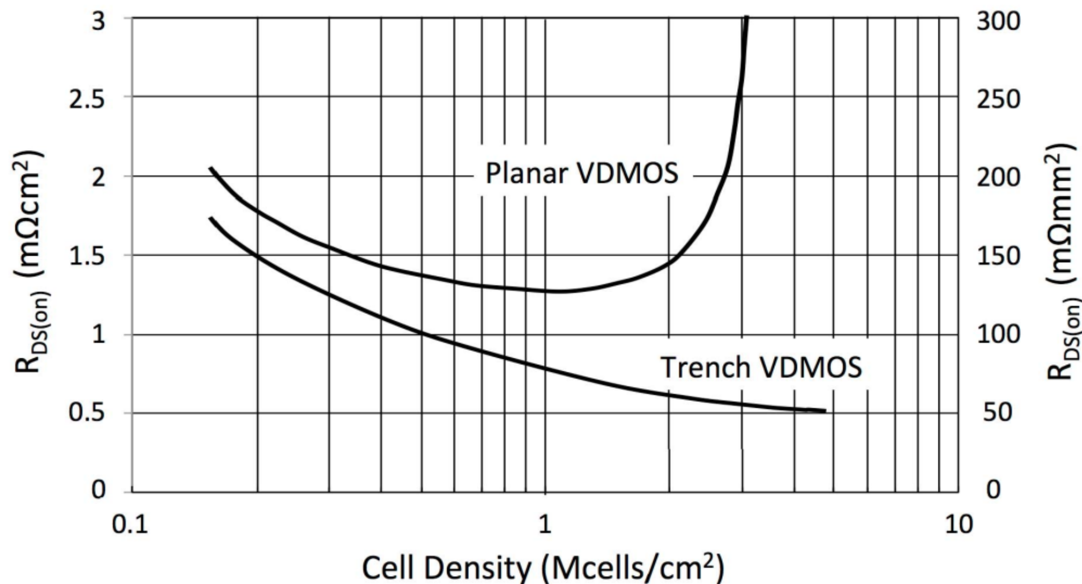


Fig. 1.4 $R_{DS(on)}$ comparison of planar VDMOS and trench VDMOS as a function of the cell density. The denomination VDMOS stands for Vertical Double-Diffused Metal-Oxide Semiconductor since a double diffusion of n and p regions occurs. Figure produced from [28]**, under CC BY 4.0.**

The device fabrication starts from the deposition of the epi-layer. After the steps of ion doping, diffusion, and activation; the realization of the gate takes place. In both the VMOSFET and trench MOSFET, the gate is realized through the epi-layer via Deep Reactive Ion Etching (DRIE) (see paragraph 1.3.3). The difference lies in the shape of the gate, which is V-shaped or trench-shaped respectively for the VMOSFET and the trench MOSFET (example of trenches plane view in Fig. 1.5). Hence, the trenches are a crucial structure and their fabrication quality is of utmost importance.

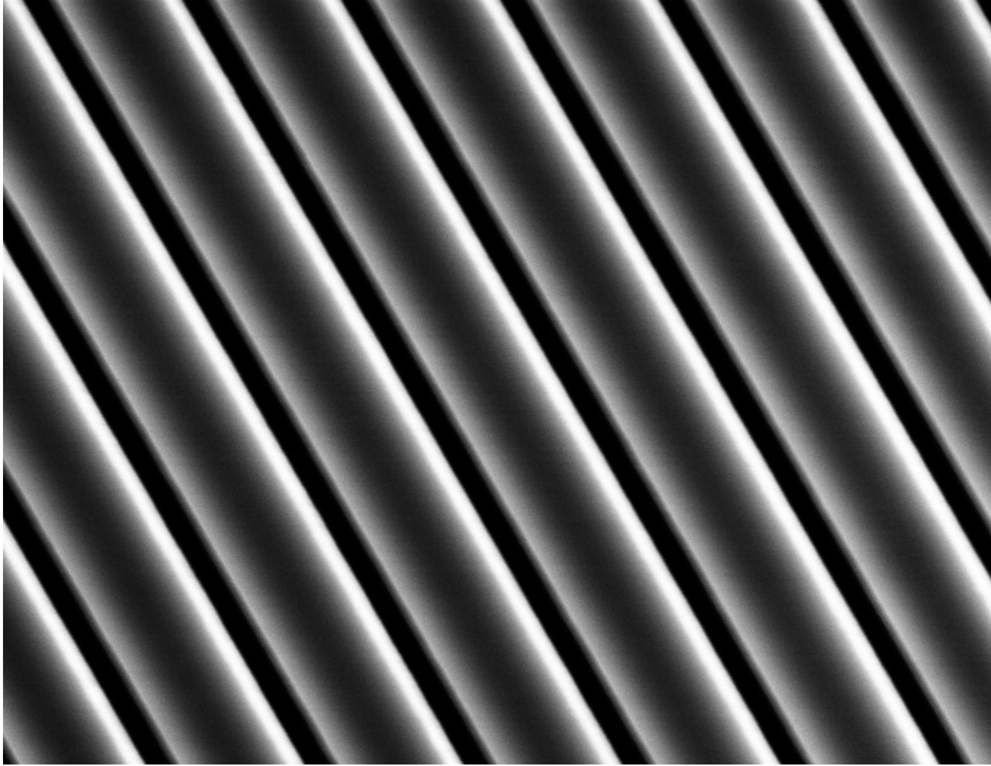


Fig. 1.5 SEM micrograph of trenches of 4H-SiC on plane view.

The expansion of trench MOSFET started with silicon [28,29] and it was transferred to SiC due to the guaranteed higher performance. In a vertical MOSFET, the higher bandgap of SiC (≈ 3.26 eV) compared to Si (1.11 eV) results in a lower conduction and valence band offset with SiO_2 (8.9 eV), which is generally employed as dielectric part of the MOSFET [30]. Moreover, SiC MOSFET ensures a higher on-state gate oxide field and blocking voltages above 1000 V (1997 data) increasing, as a consequence, the device life. SiC vertical MOSFET investigation went through the 3C-polytype [31,32], 6H-polytype [33], and finally the development of 4H-SiC-based MOSFETs [34–36] which guarantees better performances in power converter applications.

1.3. Early Stages of Trench MOSFETs Development

The next-gen MOSFET devices are vertically built following the previous research and development of vertical MOSFET made of silicon. The novelty lies in the ability to significantly increase cell density by reducing the cell pitch, also known as cell size. Although SiC and Si have different properties, the semiconductor industry utilized the same manufacturing processes for Si devices and adapted them for SiC. Especially on SiC, the device engineering is achieved by dry physical methods according to the main following steps, approximately listed in sequence:

- Homoepitaxial growth on the 4H-SiC substrate
- Ion implantation

- Rapid thermal annealing
- Photomasking and photolithography
- Oxide deposition (CVD)
- Dry etching (DRIE)
- Gas etching
- Thermal oxidation
- Metallization, bonding, and packaging

After the ion doping, the activation step demands a temperature above 1700 °C. Because of the phenomena of silicon sublimation, the carbon-cap methodology was employed during the first year of research. Morphological and surface chemical analyses were made to verify the method's efficacy (chapter 3). The abovementioned SiC vertical MOSFET has fundamental microstructures of trench shape.

1.3.1. Homoepitaxial Layer Deposition

The first treatment of all is the Chemical Mechanical Polishing (CMP) of the 4H-SiC substrate. It has the role of reducing surface roughness (polishing) by means of slurry (with abrasive colloidal silica), reactants, and pads that apply a mechanical force. The CMP technique makes use of $KMnO_4$ and HNO_3 [37], with some experimental variants also with MnO_2 [38] or TiO_2 [39]. The typical removal rate is of the order of nanometers per hour [40].

After the polishing, the deposition of homoepitaxial layers occurs with thicknesses in the range of micrometers. The deposition is performed by Chemical Vapor Deposition (CVD) on the 4H-SiC substrate. The homoepitaxial growth by definition should recreate the same polytype without inclusions of other lattice types. The homoepitaxial growth could be performed on both the C-face [41] and Si-face [42], albeit the last one is preferred in power application device manufacturing. During the deposition, it is possible to introduce dopants and achieve different doping types and concentrations as schematized in Fig. 1.6.

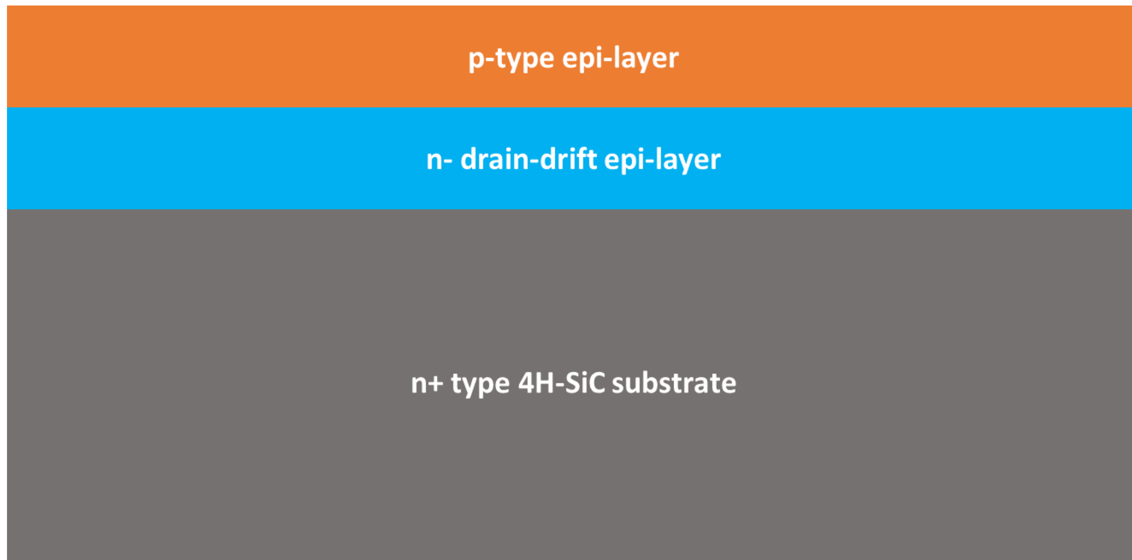


Fig. 1.6 MOSFET development illustration: deposition of homoepitaxial layers of different doping types.

The difficulties in homoepitaxial deposition are related to achieving high-quality films with low defect concentrations. It is a well-known fact that numerous defects, such as etch pits [42], micropipes [43], and triangles [44]. In this doctoral dissertation, no CMP steps were taken under investigation.

1.3.2. Doping and Activation

Although it is possible to deposit epilayers that are doped directly, region-selective doping should be performed using ion bombardment techniques under a masking approach. As displayed in the scheme of Fig. 1.7, selective regions are reproduced on the surface. Bombardment of Al and P or N ions is required respectively for p- and n-type doping, reaching depths of the micrometer order of magnitude. Especially for high-performance power devices, the 4H-SiC is highly doped with a dopant concentration of the order of 10^{18} – 10^{20} cm^{-3}. In order to activate the dopants in the lattice and release the accumulated damage [45], high-temperature annealing is performed. It requires a temperature above 1600 °C in an Ar environment [46], at the point where atoms' mobility activates and surface reactions occur. A study revealed that surface roughening starts at a temperature of 1300 °C [47].

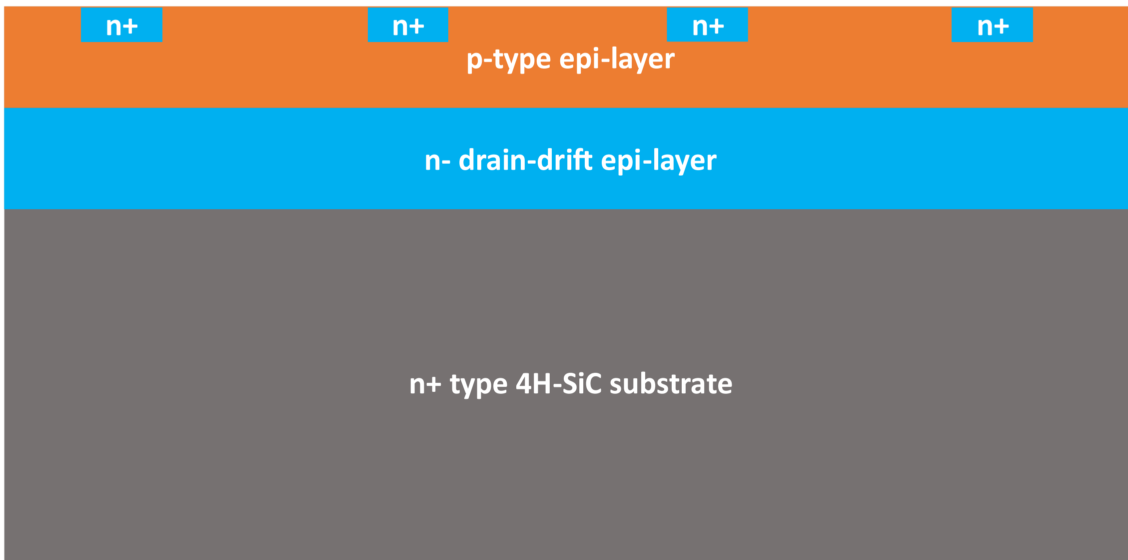


Fig. 1.7 MOSFET development illustration: ion bombardment and annealing activation of highly doped regions of the material.

For instance, it is possible to note the formation of stacking faults defects after the annealing [48]. For this reason, carbon cap layer methodology is used to prevent such manifestations. The technique will be introduced in chapter 3 with morphological and chemical analysis of C-cap-protected samples after annealing at 1700 °C.

1.3.3. Trench Fabrication

The step of doping and the following activation is roughly followed by the realization of the trenches. The trenches are fabricated on certain spots of the epi-layer, hence it is required a previous photolithography patterning as shown in Fig. 1.8. It starts with the deposition of a thick oxide layer, namely Hard Mask Oxide (HMO) as displayed in Fig. 1.8a. It is typically a thick layer of SiO_2 selected for its susceptibility to both dry and wet etching methods. The deposition of the HMO layer is followed by the deposition of photoresist (Fig. 1.8a), typically achieved through spin coating. A vast research background in photoresist science and technology application is consultable in relevant scientific contributions [49,50]. The photoresist is developed by a complex system of mask and UV irradiation, followed by etching in a dedicated solvent mix. The voids formed following the photoresist development reveal the HMO layer beneath, making it susceptible to etching (Fig. 1.8c). Once the HMO mask is finalized, the photoresist is removed (Fig. 1.8d), and the 4H-SiC trench fabrication follows.

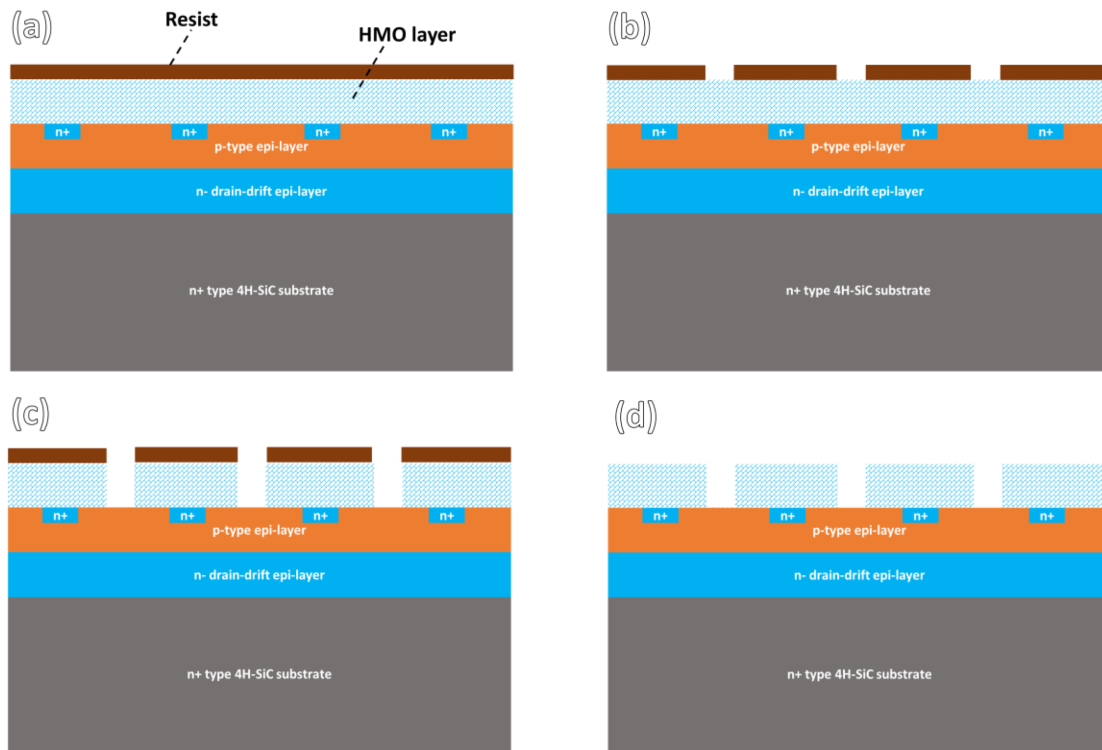


Fig. 1.8 Schematization of the patterning process: a) HMO and photoresist deposition, b) photoresist development, c) HMO etch, and d) photoresist removal.

The trenches should meet the correct desired sizes in terms of width and height. For instance, the trench MOSFET technology requires high-aspect-ratio structures [51–53]. Moreover, the shape should meet also specific requirements, for example, round corners, as displayed in Fig. 1.9. Hence, trench fabrication should be achieved through the use of a technique that allows for the production of the desired structures with the highest possible quality.

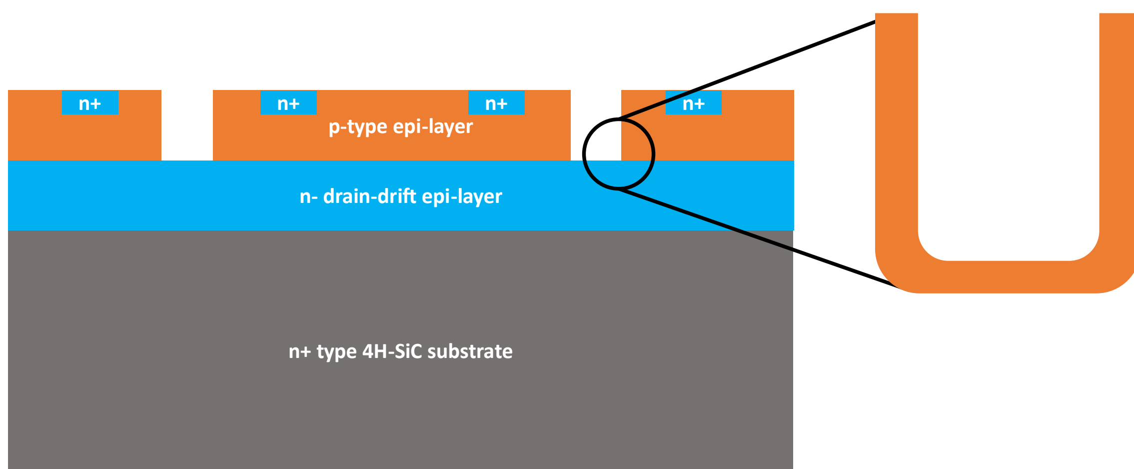


Fig. 1.9 Trench MOSFET development: trench fabrication.

The trenches are notoriously fabricated by the DRIE technique, which was employed back to application on Si. The DRIE technique is the result of the combination of physical and chemical approaches where the chemistry of the gases in the plasma is of the most importance. Via the DRIE technique, high etching rate, directionality, and selectivity can be achieved as a result of the system's variables such as radio frequency power, pressure, gas etchant flow rates, and temperature [54]. The selectivity is achieved by virtue of the chemical feature of the method since not every gas etchant is suitable to etch all the materials. The high versatility leads to the attribution of the put-before term "Deep" thanks to the opportunity to etch high aspect ratio structures. The reactions involved in the chamber are schematized as in Eq. 1.1.

$$\textbf{Substrate}_{(s)} + \textbf{Reactants}_{(g)} \rightarrow \textbf{Etched Substrate}_{(s)} + \textbf{Byproducts}_{(g)} \qquad \textbf{Eq. 1.1}$$

The substrate material is eroded by the reactants (gas etchants) under a plasma environment. The quality of the etching attack strongly depends on the formation of gaseous byproducts, their volatility, and the absence of immovable solid byproducts that certainly constitute a source of contamination. Generally, gases such as SF_6, CF_4, Cl_2, and BCl_3; are commonly employed as gas etchants with the successive release of SiF_4 or $SiCl_4$ byproducts. At the same time, the technique should meet some requirements such as high anisotropy and a high selectivity towards the 4H-SiC. The choice of the material mask is of the most importance. Studies revealed that metal (Al) mask contaminates the trench walls instead of SiO_2 mask. Such contaminations lead to device performance reduction such as the degradation of channel mobility. For this reason, the DRIE method and its modification were optimized in high etch selectivity of SiC (and Si) over SiO_2.

To understand the DRIE benefits over etch rates and mask selectivity, a particular remark on the *Bosch* process is crucial [55–58]. It was developed for shallow Si nanostructure fabrication and afterward transferred to some extent to SiC [59,60]. High selectivity is strongly demanded since only the material below the mask material should be etched. On the other hand, the chemistry involved does not guarantee anisotropy to the etching process without which the trenches cannot be attained. To prevail over the aforementioned issue, the *Bosch* method operates on a time-domain multiplexed process by which different gas compositions are sent to the reaction chamber at different times. The process consists of two main steps:

- Etching step with sulfur hexafluoride (SF_6) which is a source of the etchant agents F• radicals (Fig. 1.10a).
- Passivation step with the formation of Teflon-like $(CF_2)_n$ polymers at the sidewall (Fig. 1.10b).

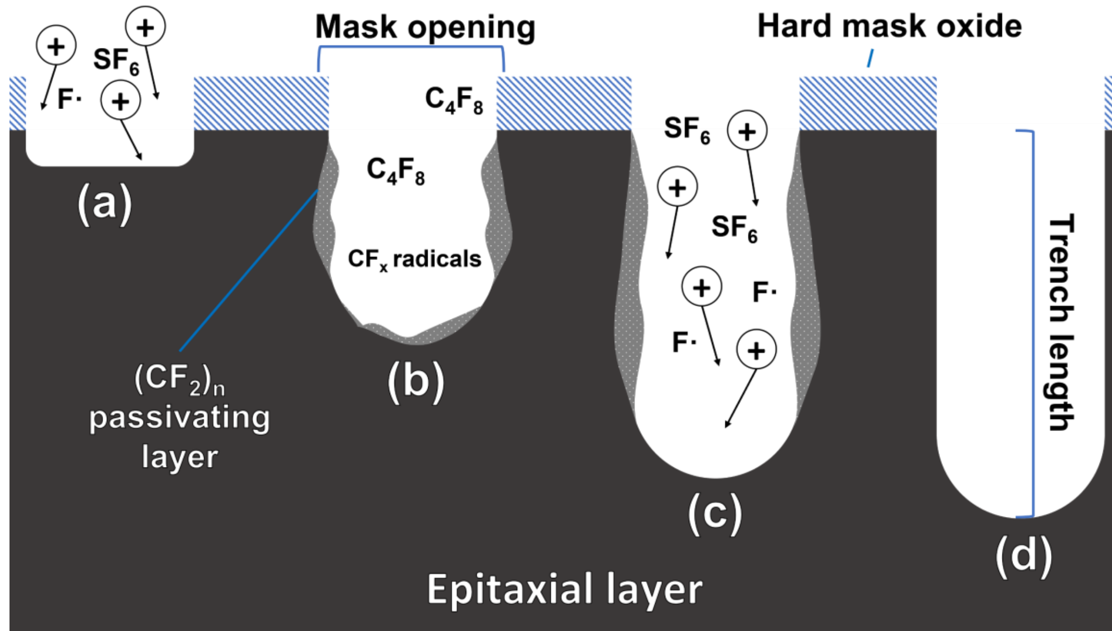


Fig. 1.10 Illustration of the Bosch DRIE process: a) Initial etching step, b) passivation step, c) second etching step, and d) final trench at the desired length.

During the etching step, the polymeric film is brought below, and simultaneously the bottom is etched and cleared as illustrated in Fig. 1.10c. Each step can be long from a hundredth fraction of a second up to minutes. The *Bosch* process makes use of the fluorinated gas passivating agents octafluorocyclobutane (C_4F_8) which guarantees high etch rates and high selectivity to the mask oxide. The method permits obtaining a high selectivity to the SiO_2 hard mask up to 300:1. The time-domain multiplexed process is advantageous in shallow and deep structures fabrication of SiC with an aspect ratio (AR) higher than 13 and deepness higher than 100 µm [61]. The quality of the trenches depends on the hard mask opening since small values (about 2 µm) are not suitable to properly etch SiC via DRIE [62].

One of the most important issues regards the formation of scallops or after striations with the consequent increase of the roughness of the walls which causes a decrement in channel mobility [63] and other device performances. The experiments that will be shown in chapter 4 aimed to recover the wall roughening after the appearance of the striation phenomena as shown in Fig. 1.11a. The striations have been formed perpendicularly to the surface. In Fig. 1.11b, the striations appear along all the analyzed sections with a high density.

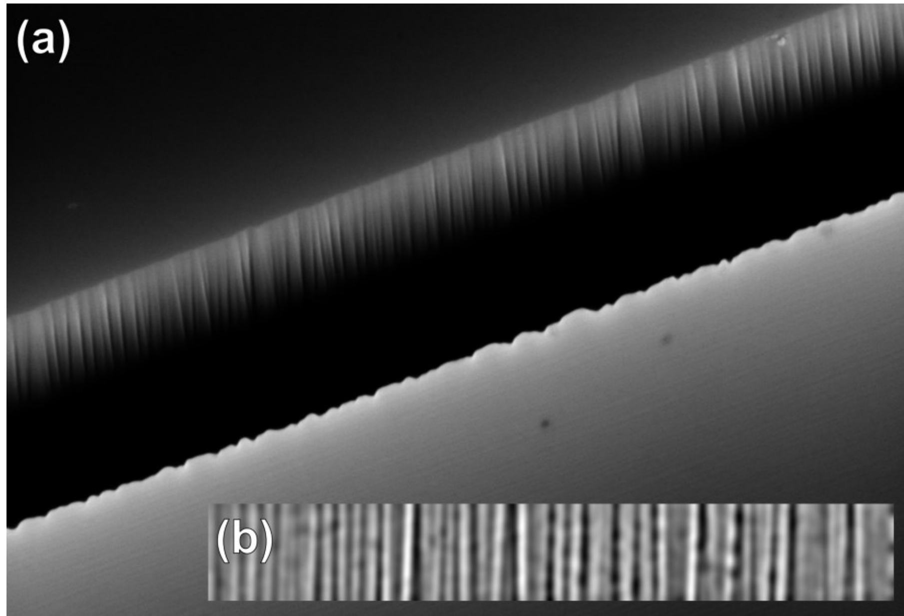


Fig. 1.11 SEM image of a) trench in the 4H-SiC substrate after DRIE process, and b) a closer look at the trench wall with image enhancement to highlight the striations.

Parallelly at the efforts made to recover the trenches wall roughening, optimization of the system parameters was set. The optimization, with the aim to reduce the wall roughening, can be accomplished by varying the fundamental parameters such as: etch cycle time, bias power, etch pressure, SF_6 flow rate, C_4F_8 flow rate, Ar flow rate, and the steps time [64–67]. In the present doctoral dissertation, the study behind the trench fabrication and optimization is not discussed.

It is mandatory to properly tune the instrument set-up in order to achieve the best results in terms of trench quality and design reproduction. Although *STMicroelectronics Catania* performed a precise tuning of all system parameters, striations formed on the walls of the trenches. The introduction of the issue is covered in chapter 4. For this reason, a conspicuous part of this doctoral dissertation covers physical and chemical methods to flatten the walls by reducing the roughness. A combination of gas etching and sacrificial oxidation was employed as a mixed physical and chemical technique in the gas phase covered in chapter 4. Pure chemical approaches were also employed to reduce the striation or to achieve flat surfaces by means of etching in a wet environment. A pure wet chemical etching attempt is covered in chapter 5, with results far from desirable. Herein, metal-assisted chemical etching and electrochemical etching were chosen as techniques to achieve surface flattening, with discussions and results covered in chapter 6 and chapter 7, respectively.

1.3.4. Insulator and Metallic Deposition

The trench fabrication and recovery are then followed by insulator and metal contacts. The insulator is generally SiO_2 but high-dielectric constant materials are under research [68–70]. The use of SiO_2 is mainly focused on the fabrication of the gate of the MOSFET which is deposited all along the trenches [71], as displayed in Fig. 1.12. The use of SiO_2 or other insulators could enhance the devices' performances [72]. Finally, the core of the device fabrication is completed with the metal deposition on top and at the bottom.

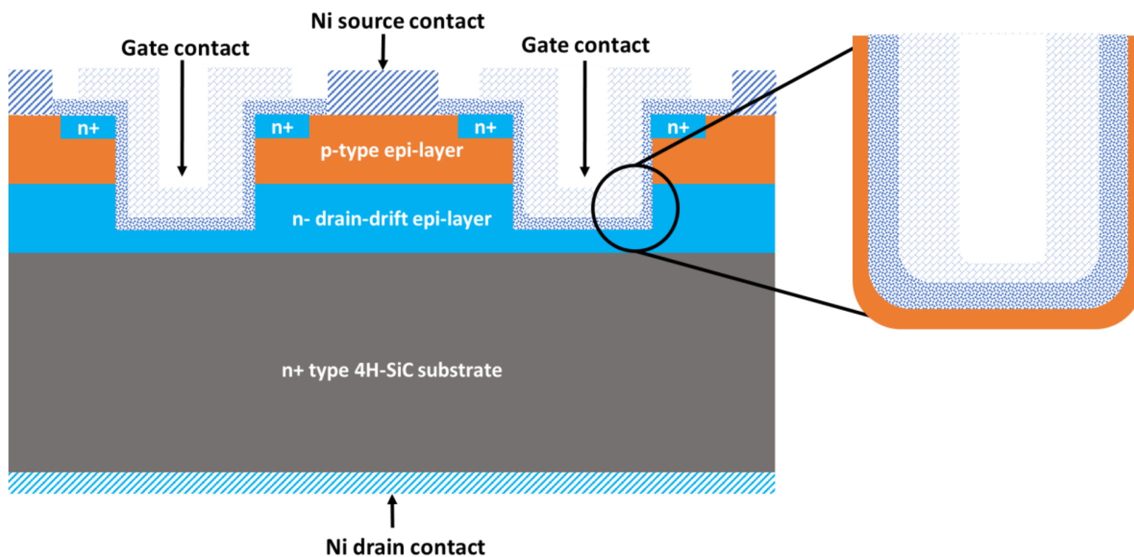


Fig. 1.12 Trench MOSFET development: insulator and metal deposition.

1.4. 4H-SiC Physical and Chemical Properties

Silicon carbide is a solid comprised of silicon and carbon elements that are mostly covalently bonded (with 12% ionic bond). In this structure, each carbon atom is tetrahedrally complexed with four silicon atoms, while each silicon atom is surrounded by four carbon atoms in the same way. The average distance between silicon and carbon is 1.89 Å. The double layer of silicon and carbon is the brick that constitutes the over 200 SiC polytypes. Each double layer can stack with the others in three ways, namely A, B, and C. Consequently, the stacking order leads to a particular polytype in which crystallographic structure can be hexagonal (H), rhombohedral (R), or cubic (C). The three common polytypes of SiC are the 3C, 6H, and 4H, according to the *Ramsdell* notation, in which the number represents the quantity of double layers involved in the stacking sequence, and the letter the crystallographic structure. The 3C-SiC is commonly defined as α-SiC whose structure resembles the cubic form of ZnS (Zinc Blende in Fig. 1.13b) while the 4H and 6H polytypes have a structure like the Wurtzite form of ZnS which indeed is hexagonal (Structure in Fig. 1.13a) [73].

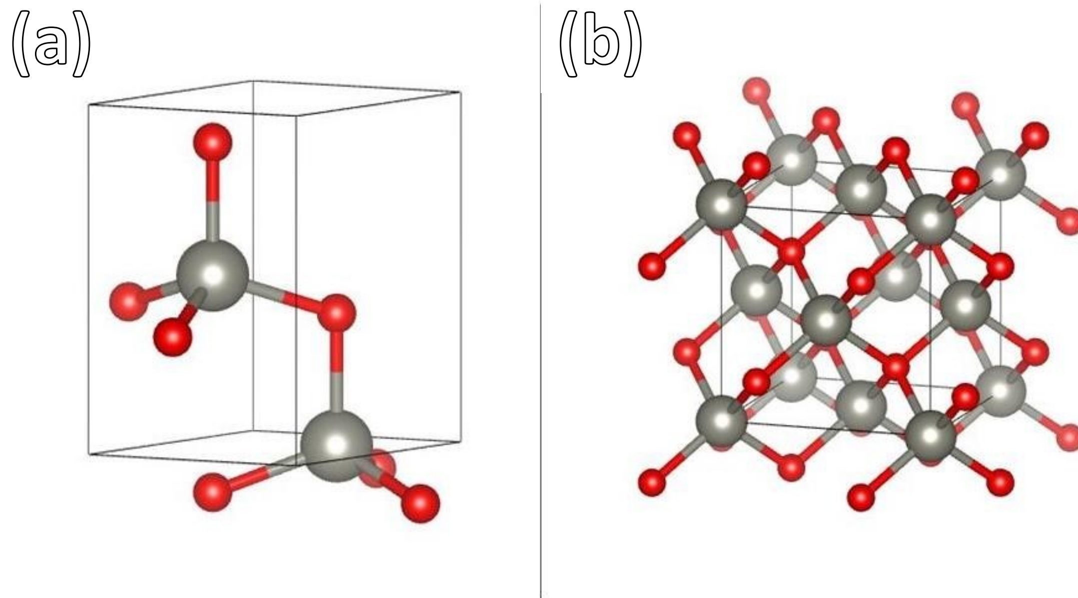


Fig. 1.13 Lattice cell of a) Wurtzite and b) Zinc Blende.

As follows, only the physical and chemical properties of 4H-SiC are discussed in this paragraph. The 4H-SiC has a hexagonal-like structure with two lattice parameters a=3.07 and b=10.05 [74,75] and 50% of hexagonality [76] (only 2H-SiC has 100% of hexagonality due to ABABAB stacking order). Among all the polytypes of silicon carbide, 4H-SiC exhibits great thermal properties that allow its use in high-performance devices. The 4H-SiC polytype has a melting point of 3103 ± 40 K [77] and a sensational thermal conductivity of 4.56 W/cm^2 °C [78,79] which permits the dissipation of heat when used in high-voltage and high-frequency devices.

Although the good performances of the material, it has chemical inertia due to the strong C-Si bond and the formation of a passivation layer. Thermally growth of SiO_2 can be obtained in either Si or SiC. No major differences are noted when hydrofluoric acid (HF) is employed to etch the SiO_2 bulk until the last layer is exposed [80]. In particular, the Si-C-OH bond acts as a passivation layer blocking the reaction of HF with the SiC surface which indeed 2 eV of energy is required to overcome the activation state of the reaction [81]. This is why the chemical etching of SiC, and in particular 4H-SiC, is hard to achieve unless the treatment in harsh conditions such as gas reactions at high temperatures [82–85], molten salts [86–88] (problems of impurity involved), and (photo)-electrochemical methods [87,89]. Beyond the wet chemical etching, nowadays only dry etching is a proper viable and scalable approach to realize complex structures on SiC [62,90–92].

Electrical properties will be further discussed in paragraph 1.5 where the comparison between silicon and 4H-SiC is highlighted so that one may demonstrate the better performances offered by the last one.

1.5. Comparison of Si and 4H-SiC Electric Properties

The most extensively researched semiconductor is silicon, which has established a state-of-the-art status thanks to decades of technological research and application. The market, the automotive in particular, demands powerful and cheaper devices, so the semiconductor industry is always looking forward to low-cost and better-performance devices. Silicon has certain physical limitations, necessitating new materials that can achieve improved electrical and thermal efficiency while also reducing costs. There are many reasons to operate with WBG semiconductors. In this paragraph the major differences between the silicon and the silicon carbide as 4H-polytype. In the semiconductors industry, some principal electrical and thermal characteristics are considered.

WBG-based devices compared with silicon exhibit higher breakdown electric field, lower specific on-resistance, faster-switching speed, and high-temperature capability because of a common higher thermal conductivity of WBGs. These characteristics help against the power loss problems that are present in silicon-based devices. Commonly, the electrical power is interested in several steps of conversion which makes the process highly inefficient. In fact, only 20% of the energy generated is being used by the end-user [78,93]. Additionally, WBGs go beyond the limits of silicon in high-frequency and high-voltage devices [94–96]. In Tab. 1.1 the most important electrical properties are resumed, furthermore, for better visualization of the improvements involved, a diagram is shown in Fig. 1.14.

	E_g (eV)	E_c (V/cm)	μ_e (V/cm^2 s)	μ_p (V/cm^2 s)	v_{sat} (cm/s)	ε_r	λ (W/cm °C)	T_{melt} (°C)
Si	1.12	$3 \cdot 10^5$	1450	450	$1.0 \cdot 10^7$	11.7	1.45	1412
4H-SiC	3.2	$1.9 \cdot 10^6$	950	115	$2.2 \cdot 10^7$	9.66	4.56	3103

Tab. 1.1 Comparison of electrical properties of Si and 4H-SiC [78,79]**.**

The higher breakdown field of SiC in comparison to Si permits to use a thinner drift layer and a higher doping concentration. A thinner blocking layer and higher doping concentration lead to a lower specific on-resistance than Si-based devices [93]. For high-frequency devices, the fast switching-speed capability (5-10 times higher in MOSFET devices than Si) [97] is of most fundamental importance. This is due to the high breakdown field and the higher electron velocity [93]. Additionally, the saturation drift velocity (v_{sat}) of silicon at room temperature is $1 \cdot 10^7$ cm/s whereas for 4H-SiC is attested to be $2.2 \cdot 10^7$ cm/s [98,99]. Finally, the peculiar thermal conductivity

allows SiC and in general WBGs to dissipate heat more efficiently. This results in the possibility of operating with high power, high frequency, and high-temperature environments [93].

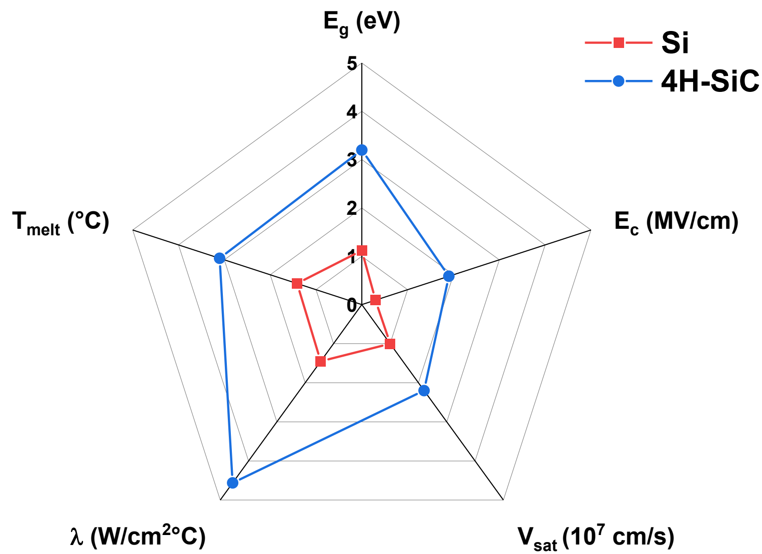


Fig. 1.14 Diagram of comparison of Si (red line) versus 4H-SiC (blue line). The electrical properties are referred at a temperature of 300 K.

As previously discussed, silicon has been researched for many years. The wafer diameter production ranges from 20 mm up to 450 mm with a low concentration of defects. For SiC, the availability of high-quality wafers permits them to be used in many areas of the electronic industry. Nowadays, 150 mm (6-inch) SiC wafers are commercially available with low defect concentrations [97]. Recently, 200 mm (8-inch) wafers of 4H-SiC have been produced for the first time which is a great step of an important milestone of the electronic industry where the automotive industry is pressing for low-dimension and high-power devices [100]. However, there is still a long way to go in the direction of achieving mass production of wafers with higher diameters and lower defect densities.

1.6. Physical Etching Methods

4H-SiC is a hard material that is characterized by chemical inertia. Its features make difficult the manipulation and carving. As discussed previously, the covalent nature and the strong bonds of SiC require drastic conditions to operate at the bulk and surface levels. In particular, the etch approaches well consolidated in the semiconductor industry are based on plasma treatments or gas etching techniques which activate reactions at the surface level. In fact, it is not possible to discuss exclusively about physical techniques since some reactions occur during the treatment. The

selective etch on certain zones is achieved thanks to the nature of the unidirectional flow of the plasma or by the patterning, generally adopting thick SiO_2 layers.

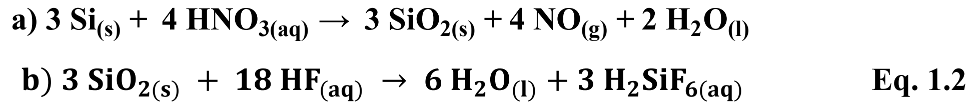
The most frequently used plasma technique is Reactive Ion Etching (RIE). The RIE uses plasma of Ar^+ ions and variable chemistry of SF_6/O_2 [101] or CHF_3/O_2 [102] or other halogen-based/O_2 combinations [103,104]. In paragraph 1.3.3 it was discussed the fabrication of trenches using the DRIE which is indeed a typology of RIE. The RIE-based approaches are commonly used to achieve massive etch with high rates of the order of 1 μm/min [105] with the possibility of carving hundreds of μm in a relatively short amount of time.

In this doctoral dissertation, physical/chemical methods were also employed. The plasma-free gas etch approaches use high temperatures to activate the surface and let the gases react with it. A variety of gases were employed on 4H-SiC ranging from Cl_2/O_2 [106] to H_2/O_2 [107]. Herein, low etch rates of the order of 1 μm/h are reached. In fact, the gas etching technique is often employed as a precise etching method to refine corners or eliminate defects resulting from high-impact etch techniques like DRIE. In this doctoral dissertation, trenches were fabricated using DRIE. Striations appeared on the walls as a result of the employed etching approach. Therefore, the H_2 gas etch technique was adopted to remove the striations and obtain smooth walls. The excellent results obtained by H_2 gas etch in striation reductions are discussed in chapter 4.

1.7. Chemical Etching Methods

The physical etching methods have many advantages, but one issue with equipment usage is the inability to work generally on a high number of wafers at once. The semiconductor industry needs to produce more in less time, for this reason, chemical baths surpass such problems since it is generally possible to work in batch. The practice of silicon wet chemical etching is well consolidated, thanks to the many years of research. Both the SiC and the Si have a thermic oxide layer up to the surface that must be cut out before every etching process. A study reveals that a 0.1 nm/s rate is achieved for silicon dioxide (SiO_2) etch in HF(50%):H_2O 1:50 solution [108]. The oxide layer is not affected by the underlying substrate material, hence, there is no etching rate variation for the SiO_2 growth on a 4H-SiC, 6H-SiC, or Si wafer [80]. The Si has a good chemical activity which makes it easy to attack in an acidic or basic solution environment. Its etching can be achieved through tetramethylammonium hydroxide (TMAH) reactants (viable for industrial manufacturing) [109,110], via hot KOH solution [109,111], or by use of an HNO_3 and HF mixture [112,113]. The last two methods are more feasible for laboratory experiments than the first one since TMAH is highly toxic. For instance, the reaction involving the HNO_3 and HF solution proceeds in two main steps. The first reaction step (Eq. 1.2a) involves the oxidation of Si into the

oxide form. The HF is not able to directly etch Si and the formation of SiO_2 should take place. After oxide formation, the HF in the mixture is free to dissolve SiO_2, according to the reaction in Eq. 1.2b, revealing the underneath Si layer. The steps repeat one by one till the total dissolution of Si or the consumption of the reactants.



$$\text{a) } 3\,Si_{(s)} + 4\,HNO_{3(aq)} \rightarrow 3\,SiO_{2(s)} + 4\,NO_{(g)} + 2\,H_2O_{(l)}$$

$$\text{b) } 3\,SiO_{2(s)} + 18\,HF_{(aq)} \rightarrow 6\,H_2O_{(l)} + 3\,H_2SiF_{6(aq)} \qquad \text{Eq. 1.2}$$

At this stage, etching silicon chemically is a simple process that employs commonly available reagents. However, the relatively strong chemical resistance of 4H-SiC creates a remarkably different situation. A detailed explanation, incorporating thermodynamic and kinetic studies, of the 4H-SiC etch problem is reported in the current literature [81]. On Si, when all the SiO_2 layer is consumed, the last residue functional group is the Si-OH, which is eliminated in place of a Si-F group. The last reaction occurs with the replacement of the fluorine with a Si-H bond and the elimination of a molecule of $SiF_{4(g)}$ as in Fig. 1.15a. The wet chemical etching of 4H-SiC in HF aqueous solution proceeds in the same way, up to the formation of the Si-C-OH termination that acts as a passivation functional group as schematized in Fig. 1.15a. The elimination of the hydroxyl group, bonded with the C-terminal atom, requires an activation energy between 1.5 and 2 eV (see the diagram in Fig. 1.15b). Moreover, the oxygen insertion to the Si-C bond is unfavorable because endothermic and highly energetic (4 eV) [81].

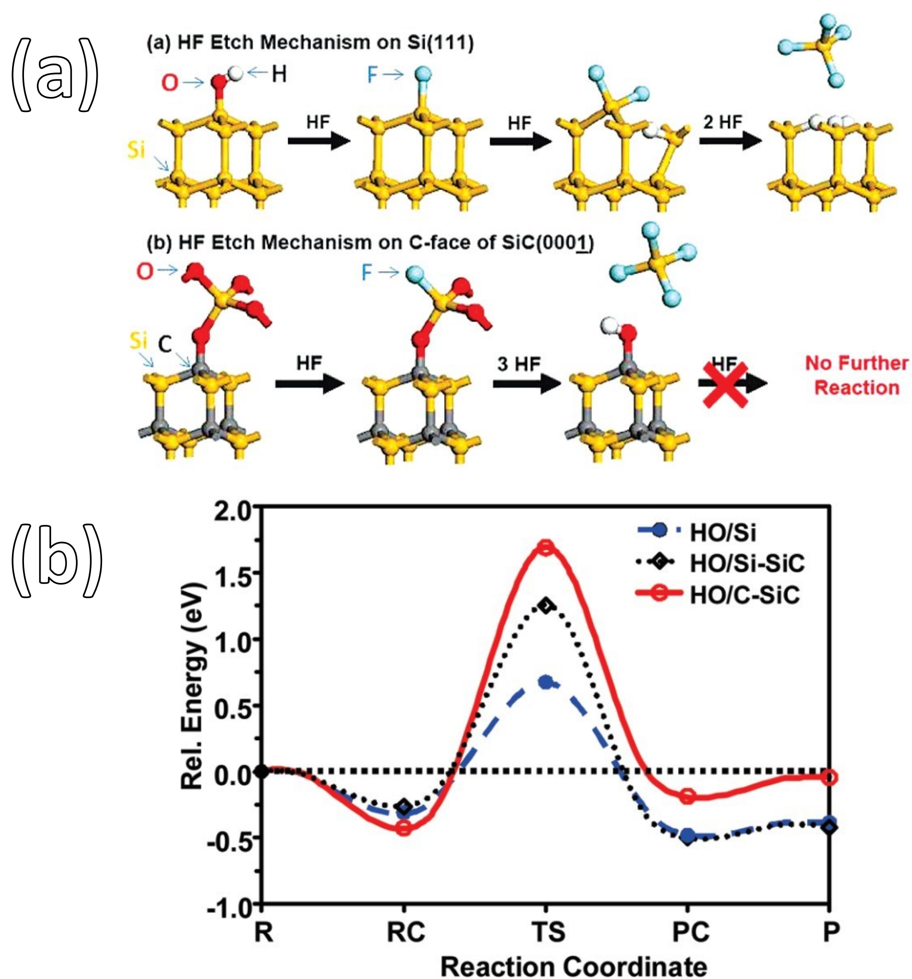


Fig. 1.15 a) Reaction mechanism of HF etching on (a) Si (111) and (b) on C-face of SiC ($000\overline{1}$) and b) reaction diagram of OH group elimination on Si, Si-SiC, and C-SiC. Adapted with permission from [81]**. Copyright 2009 American Chemical Society.**

Therefore, it has been shown that wet chemical etching of 4H-SiC is a difficult challenge. In short, it is not possible to overcome the energy barrier using standard wet chemical etching approaches. During the writing of this dissertation, no etchant or chemical solution was able to overcome the problem of the -OH passivation group. At this point, two major chemical etching approaches work on 4H-SiC: ElectroChemical Etching (ECE) and Metal Assisted Chemical Etching (MACE). In both cases, it is supplied with an external energy source that is able to exceed the barrier energy and the oxidation of 4H-SiC is free to happen. Once the 4H-SiC surface is oxidized, the HF is free to dissolve the oxide layer.

Such as any technique, wet chemical etching approaches suffer from many drawbacks. The most important is the treatment efficiency along a wafer. The differences in etch rate could be consistent and the final results could be very different from one point to another of the wafer. In addition, the

use of chemical baths increases the need to install a huge recovery system of harmful reactants and to treat a huge amount of water. The cleaning processes also require a large amount of water as no traces of reactants should be left on the wafers. In conclusion, the adoption of a wet chemical etch method should be economically convenient, hence, the technique should guarantee high throughput and low costs.

2. Experimental

2.1. Outline

The following section encloses all the experimental results of adopted physical and chemical etching methodologies to apply to 4H-SiC. The development of the device encountered different challenges since the 4H-polytype is harsh to deal with, compared to silicon. For instance, the activation of dopants necessitates high-temperature annealing (> 1500°C) which results in silicon sublimation. As a solution, carbon cap layers are utilized in SiC technologies. In chapter 3 the state of the art and the outcomes of the carbon capping methodology are discussed.

The dry etching process found applications in the development of the first stages of a trench MOSFET device based on 4H-SiC material. Although the trench MOSFET on 4H-SiC enhances the well-established technology on Si, several challenges have arisen due to the different physical and chemical properties of SiC. In this context recovery of trenches walls via dry (chapter 4) and wet (chapter 5) approaches are presented and discussed.

Complex and innovative wet etching methodologies of 4H-SiC have been also discussed in the present thesis as strategies to recovery DRIE damage or to obtain porous silicon for other applications. Metal Assisted Chemical Etching (MACE) has been investigated as a wet chemical etching technique with the aim of flattening the striations on the walls of the trenches. The introduction of the technique and its performance on 4H-SiC are discussed in chapter 6. Furthermore, the study of electropolishing (chapter 7) on 4H-SiC was also conducted as a wet etch method to identify the optimum etch condition while achieving the lowest final surface roughness. Furthermore, the electrochemical etching technique has been used to explore the applicability of the method for the 4H-SiC etch in wet environments. In fact, the last experimental part sheds light on the potential of electrochemical etching techniques to produce SiC micro- and nanoparticles by a top-down approach (chapter 8).

2.2. Analysis Instrumentations

General characterization techniques are resumed and described in this section. During the different work discussions, the analysis instrumentation will be recalled. Specific instrumentation and methods will be further described at every work contribution.

A dual-beam SEM (*FEI DA300*) performed the trenches' topographical analysis. The micrographs were acquired setting the energy of the e-beam at 15 keV. The samples were tilted at a

40° angle to observe the striations of the trenches. All the micrographs were acquired under a magnification level of 150 kX. The samples were not diced prior to SEM analysis.

A Field Emission-Scanning Electron Microscopy (FE-SEM) image acquisition was performed with a *Zeiss SUPRA-55 VP*. The images were acquired with an electron probe energy of 15 kV. The sample chamber had a pressure of 10^{-7} Torr during analysis and the column chamber had an average pressure of $3 \cdot 10^{-10}$ Torr. Tilting of 40° was set by occurrence.

Elemental analysis was performed by Energy Dispersive X-Ray (EDX) instrument (*Oxford solid state detector*) built-in in the FE-SEM instrument. The windowless detector allowed the detection of the O Kα peak at 0.560 KeV.

A third FE-SEM instrument (*Jeol JSM-7900F*) was used. A typical probe energy of 10 kV was set for the image acquisition. An in-lens detector (UED) and a working distance of 4 mm were standard settings to acquire high-magnification images. A minimum chamber pressure of $3 \cdot 10^{-3}$ Pa was employed during the analysis.

The surface roughness was characterized by Atomic Force Microscopy (AFM) technique. An *NT-MDT modular AFM NTEGRA* instrument equipped with a PX Ultra controller system was used to perform the measurements. The instrument was equipped with a high-resolution silicon tip (ETALON HA_NC type, resonant frequency 140 kHz ± 10% kHz, force constant 3.5 N/m ± 20% N/m, cantilever length 124 µm ± 2 µm, cantilever width 34 µm ± 3 µm, cantilever thickness 1.85 µm ± 0.15 µm). The images were acquired in semi-contact mode at room temperature. The RMS (Root Mean Square) and RA (Roughness Arithmetic Average) were chosen as rugosity parameters. The Peak-to-Peak (PtP) expresses the maximum height of the acquisition. Additionally, the Developed Surface Area Ratio (Sdr, defined as the ratio between the real sample area and the nominal area) has been chosen as a parameter to investigate the flatness of the samples. The Sm parameter expresses the average lateral distance between peaks in a section expressed in nm or µm.

The surface chemical composition was examined by X-Ray Photoelectrons Spectroscopy (XPS) with a *PHI 5600 Multi Technique system*. The samples were analyzed with a take-off angle of 45° in the $1 \cdot 10^{-8}$ Pa depressurized sample chamber. The X-Rays source was an Al Kα 1486.7 eV. The signal calibration was done by fixing the C-C signal of C1s orbital at 285.0 eV. Deconvolutions of the experimental spectra were made to evaluate the surface chemical composition with *XPSPeak 4.1* [114]. Atomic concentrations were assessed by considering the atomic sensitivity factors after *Shirley* background correction.

The final metallic thickness was measured by a spectroscopic ellipsometer (*SEMILAB SE-2000*) working in the wavelength range of 250-1650. The angle between the source and the detector was set at 75 °.

DLS analysis was operated by *Malvern Zetasizer Nano-ZS Zen 3600*. The cuvettes used for particle size were in polystyrene. The cuvettes were washed with isopropyl alcohol and dried with pure N_2 before DLS measurements.

Specific methods of analysis and materials used during experiments will be introduced in each work-dedicated paragraph.

3. Carbon Cap Protection Layer

3.1. Introduction

Semiconductor doping in microelectronic devices is one of the first and fundamental stages to be performed. A high concentration of dopants is required because of the necessity to reduce the ohmic contact resistivities and the drain regions in FETs. Selective n- or p-regions in SiC can be achieved by doping with the Group V elements N or P and Group III elements B or Al, respectively. Diffusion problems arise after ion implantation in both doping types, due to the small diffusion coefficients which result in a lack of impurity diffusion [115].

In the case of p-doping, Al is preferred over the B element because the last one has a higher ionization energy of 285 meV [116] over the 190 meV [117] of the Al in 4H-SiC. Although the n-doping N and P are commonly used, the nitrogen is less favorable because of the relatively low solubility of 10^{19} atoms/cm^{-3} in 4H-SiC [118]. Moreover, the high dose n-doping with P ions is preferred because of the lower sheet resistance achieved.

The high-temperature annealing enables the dopants' activation in the host lattice [119]. As shown in Fig. 3.1 the ion activation ratio is low when the annealing temperature is below 1500 °C whereas at temperatures higher than 1600 °C more than 95% of the activation ratio is reached [120].

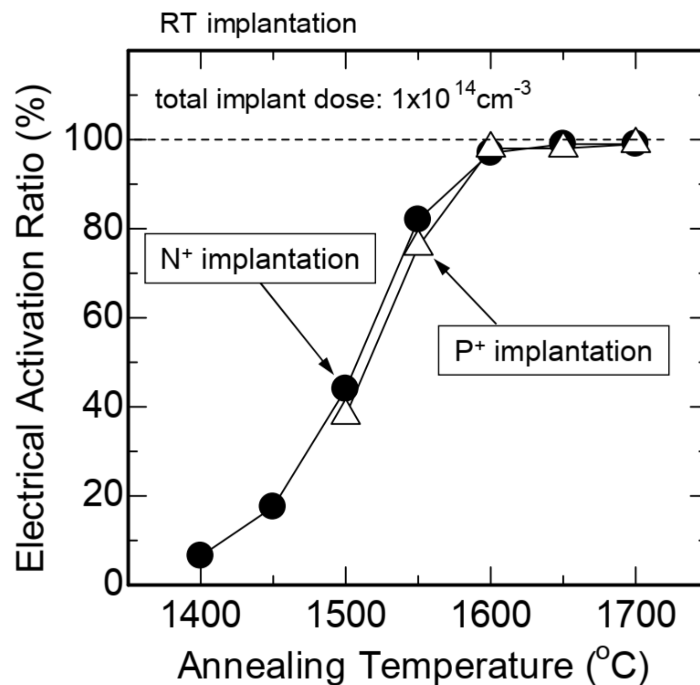


Fig. 3.1 Electrical activation ratio (%) as a function of annealing temperature (°C). Reprinted with permission from [121]**. Copyright 2014 John Wiley and Sons.**

Although annealing resolves internal defects and diffusional and ion activation issues, it also leads to surface roughening phenomena. It has been demonstrated that annealing above 1600 °C produces a high increase in roughness and a high concentration of defects. For instance, Fig. 3.2a shows the pristine 4H-SiC surface which is characterized by an atomical flatness with an average roughness value of 0.2 nm. After annealing at 1700 °C, the aforementioned phenomena cause an increase of average roughness of 44 nm (Fig. 3.2b), hence associated with a strong increment compared with the bare 4H-SiC [122]. Moreover, the high temperatures lead to silicon sublimation and surface atom migration and consequently the change in surface chemical composition [121].

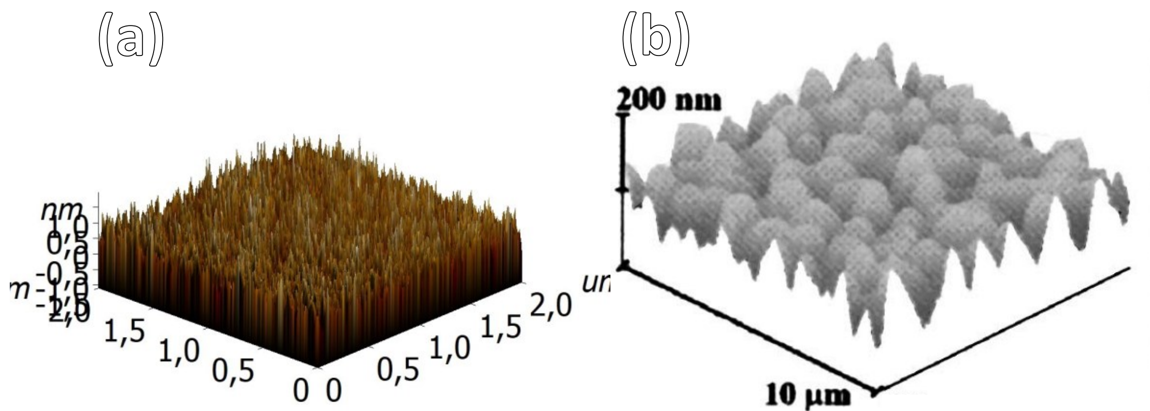


Fig. 3.2 AFM 3D images of a) 4H-SiC Si-face in 4 µm^2 acquisition area and b) 4H-SiC Si-face after doping 6·10^{16} cm^{-2} and post-annealing at 1700 °C for 30 min. Adapted with permission from [122]**. Copyright 2004 American Institute of Physics.**

In order to repress the silicon sublimation and the surface roughness increment, the carbon-cap (C-cap) methodology is a viable good choice [123,124]. Before the post-doping annealing, the deposition of a carbonaceous material layer is made. It can be done following different more or less viable techniques: the deposition of a photoresist [122,123] or Electron Cyclotron Resonance (ECR) sputtering [124]. The adoption of a C-cap has no influence on ion activations, and the same resistivity values are reported with or without the C-cap layer [125]. The C-cap layer has a role only at the surface while during the annealing, the ion activation involves the bulk portion of the substrate or epitaxial layer.

The present study sheds light on different doping types and concentrations by activating the dopants with annealing performed at a temperature of 1700 °C. Different thicknesses of the C-cap layer were used to investigate any possible variations in 4H-SiC surface roughness.

3.2. Materials and Methods

The substrate employed for the study was a 6-inch 4H-SiC (0001) with an 8° off-axis. The dopings were done by singular or mixed Al/P ion implantation at different concentrations as shown in Tab. 3.1. Thicknesses from 100 to 400 nm were realized. The activation process was conducted at a temperature of 1700 °C, and a pressure of 20 mTorr, under an Ar environment for 30 minutes. The ions implantation sequence was similar to the one adopted for production wafers. After the annealing, the carbon layer was removed by dry oxidation at 850-900°C for 15 min. A 4H-SiC wafer was left undoped as a reference sample. A total of five samples were doped following different patterns of concentration and doping type. The five samples were labeled from letters A to E. The carbon thickness was varied as well between the investigated samples, as shown in Tab. 3.1. The thickness of the carbon layer deposited on samples A and B is unknown due to company confidentiality.

	Implant		**C-cap thickness (nm)**
	Dopants	**Type**	
4H-SiC reference	NA	NA	NA
Sample A	P	N+	Unknown
Sample B	Al + P	(P-) + (N+)	Unknown
Sample C	Al + P	(P-) + (N+)	200
Sample D	P	N+	400
Sample E	Al	P+	100

Tab. 3.1 Experimental doping type, concentration, and C-cap layer thickness conditions. The samples were coded from letter A to letter E.

All wafers were vertically cut along the red dashed line as shown in Fig. 3.3. Three pieces per sample were obtained of about 4 cm^2 large area, namely SUP, MID, and INF.

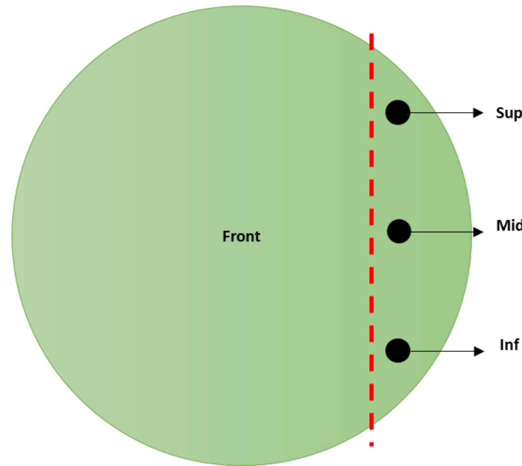


Fig. 3.3 Scheme of wafer cut along the red dashed line. Three different samples were obtained on the superior (SUP), middle (MID), and inferior (INF) parts of the wafer.

Surface roughness was measured by AFM (*NT-MDT* modular *AFM NTEGRA*) technique. The average values of RMS and RA were obtained from 18 measurements (6 in each region of the acquired samples from each wafer) on a 4 µm^2 scan area. Standard deviation is correlated with the average values.

3.3. Results and Discussions

The 4H-SiC is characterized by an atomic flatness as evidenced by Fig. 3.4a image, with a typical RMS value of 0.2 nm. The events that occur during the high-temperature annealing cause a conspicuous and detectable increase in surface roughness, as previously reported in the scientific literature [122,126]. On the contrary, the protection with the C-cap layer represses the mentioned phenomena and the flatness remained the same as displayed in Fig. 3.4b.

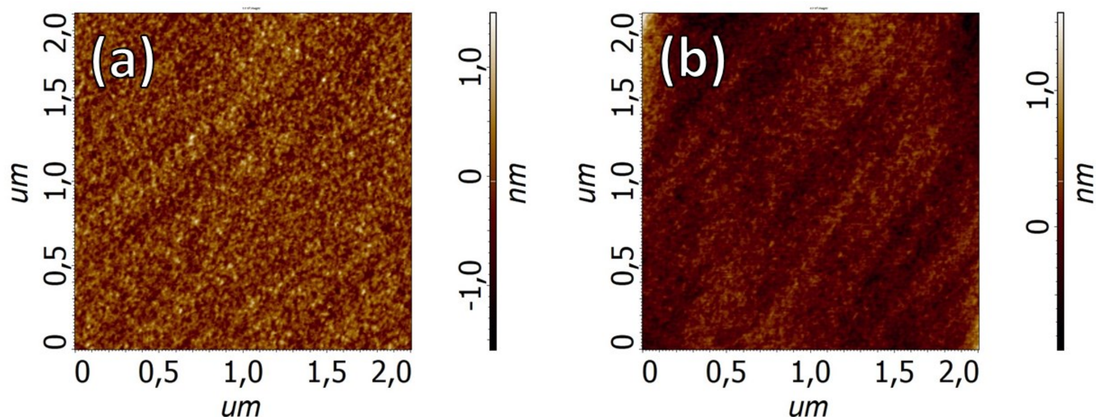


Fig. 3.4 AFM 2D images of a) 4H-SiC pristine and b) C-cap protected and annealed sample.

The average values of RMS and RA are reported for each investigated sample in Tab. 3.2. The average values are correlated with the standard deviation obtained out of 18 measurements for each sample. As noticeable from Tab. 3.2, the detected surface roughness for the carbon-protected and annealed samples is equal to or even lower than the reference 4H-SiC surface.

	RMS (nm)	**RA (nm)**
4H-SiC reference	0.35 ± 0.02	0.28 ± 0.02
Sample A	0.27 ± 0.06	0.22 ± 0.04
Sample B	0.35 ± 0.16	0.28 ± 0.14
Sample C	0.33 ± 0.10	0.25 ± 0.08
Sample D	0.12 ± 0.04	0.16 ± 0.03
Sample E	0.17 ± 0.02	0.13 ± 0.03

Tab. 3.2 Average roughness of reference and C-capped samples. The average data and the standard deviation are the results of 18 acquisitions.

For the sake of better data visualization, Fig. 3.5 displays the average roughness values contoured with the associated error bars. Comparable roughness was measured from samples A to C, by considering the overlapping errors associated with them. A decrease in the average roughness is observed for sample D and sample E.

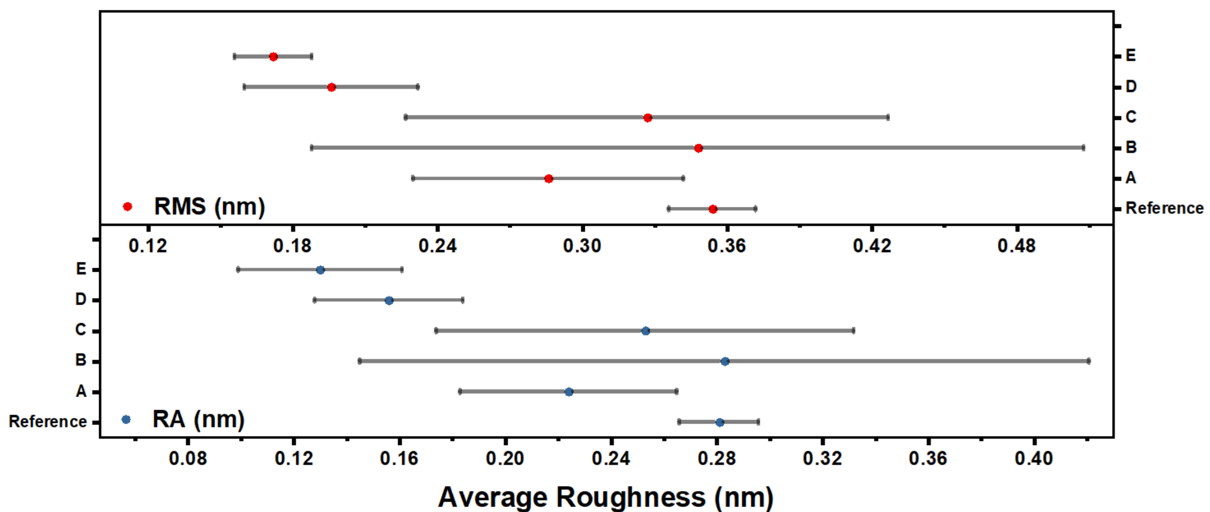


Fig. 3.5 Graphs of a) RMS and b) RA values of 4H-SiC reference and C-cap protected and annealed samples. The data are contoured with error bars.

Their reduced roughness is probably due to the high temperature during the activation process which indicates that some physicochemical phenomenon takes place. For this reason, it was worth studying by XPS the elemental and chemical surface composition, summarised in Tab. 3.3. Increased content of C and Si is detected for the C-cap samples, and on the other hand, a lower percentage of oxygen has been detected. The samples provided by *STMicroelectronics*, which were examined in a controlled environment, have lower thermal silicon dioxide than the reference sample which was stored for a longer time. Samples A and C have a similar C/Si ratio to the reference sample whereas the others have a higher ratio possibly due to silicon diffusion or even sublimation.

	C%	**F%**	**O%**	**Si%**	**O/Si**	**C/Si**
4H-SiC reference	35.81	1.11	25.63	37.45	0.68	0.96
Sample A	43.51	0.25	14.34	41.91	0.34	1.04
Sample B	46.07	1.03	11.87	41.03	0.29	1.12
Sample C	48.99	0.29	9.43	41.29	0.23	0.84
Sample D	46.99	0.26	11.05	41.70	0.26	1.13
Sample E	44.98	0.33	14.41	40.29	0.36	1.12

Tab. 3.3 XPS elemental quantitative analysis of 4H-SiC reference and C-capped and annealed samples.

A qualitative study of the chemical moieties present at the surface is obtained by proceeding with a photoelectron peak deconvolution: XPS deconvoluted spectra of the 4H-SiC reference and sample D are compared in an attempt to highlight the major differences. For the 4H-SiC reference sample, the C1s spectrum (Fig. 3.6a) is deconvoluted in four components at 283.0 eV, 285.0 eV, 286.5 eV, and 289 eV, attributed to Si-C, C-C, C-O and C=O bonds, respectively [127]. The Si2p peak reported in Fig. 3.6b has three main components at 100.1 eV, 102 eV, and 102.9 eV attributed to Si-C, Si-O, and stoichiometric SiO_2 groups [128]. The presence of the oxide layer is confirmed by the O1s signal in Fig. 3.6c which is mostly attributed to the Si-O groups at 532.5 eV and some other components attributable to adventitious carbon at 531.3 eV and 534 eV [129]. Finally, the fluorine (detected as F1s Fig. 3.6d) is present in traces, and a signal, near the limit of detection, is randomly visible in some samples and associated with C-F moieties due to the wet cleaning process of the wafers.

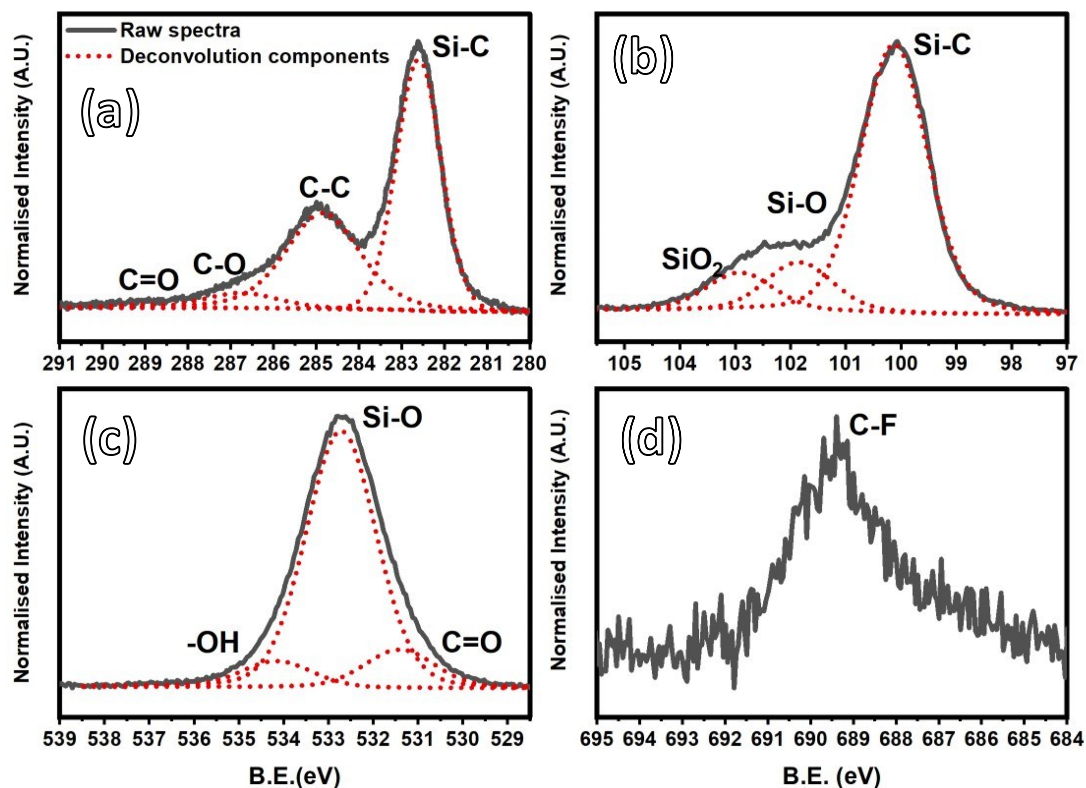


Fig. 3.6 XPS spectra of 4H-SiC reference sample: a) C1s, b) Si2p, c) O1s, and d) F1s signals.

XPS analysis of sample D revealed a surface composition almost identical to that of the reference sample except for a sub-stoichiometric oxide layer at 102 eV (Fig. 3.7b) attributed to some diffusion phenomena of oxygen or silicon during the activation process.

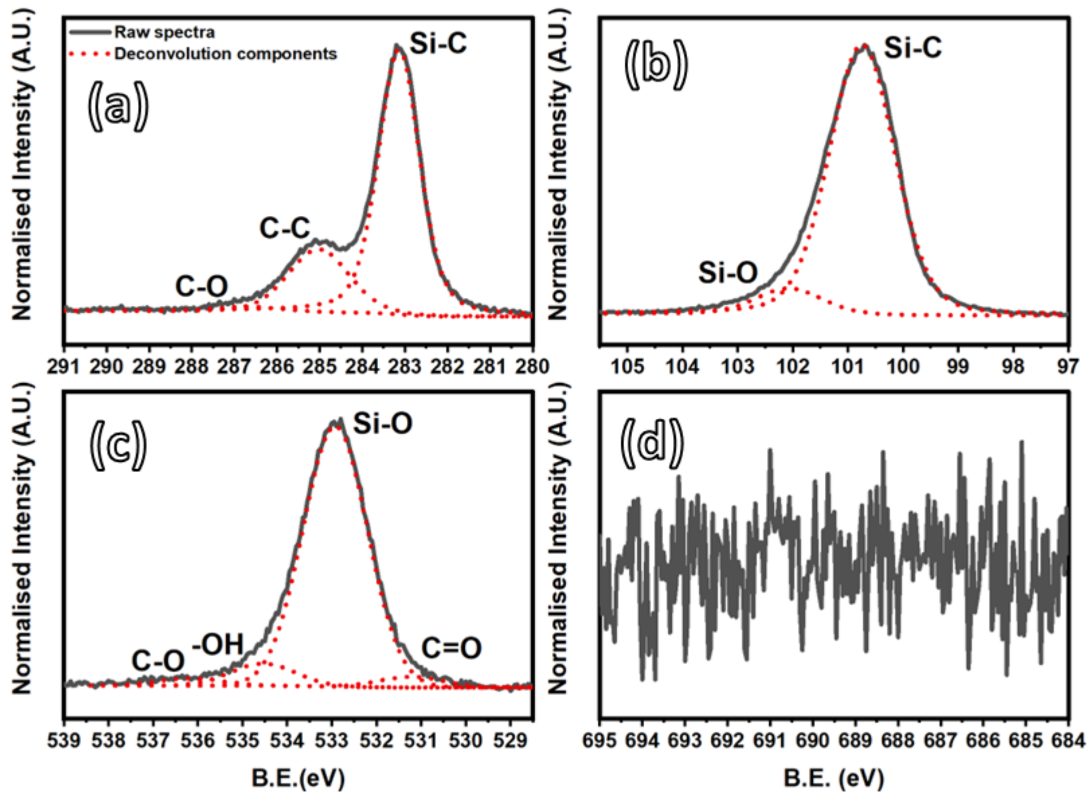


Fig. 3.7 XPS multi spectra of sample D: a) C1s, b) Si2p, c) O1s, and d) F1s.

There were no significant differences between sample D and other C-capped samples analyzed. As a result, the data for those samples are not displayed.

3.4. Conclusions

The effects of C-cap protection on 4H-SiC doped samples have been investigated. Morphological and surface chemical analyses were performed by AFM and XPS analysis techniques. Slightly, but not relevant, roughness variation from one sample to another has been detected. It was demonstrated that the C-cap protection method is effective over different combinations of doping types and levels. The surface roughness of C-capped samples was equal to or even below the reference 4H-SiC sample.

The surface chemical composition of the C-capped samples was different in chemical composition and elemental percentage. In particular, in terms of O/Si and C/Si ratios: one might speculate a possible silicon diffusion after annealing and eventually explain the minor ratio variations. It is noted that at a temperature above 1400 °C the silicon sublimes from the SiC surface which compromises the surface stoichiometry [130]. Indeed the carbon cap is a viable method to repress the silicon sublimation but the hypothesis of a small percentage of diffusion extent cannot

be excluded. The decrease in roughness is likely attributed to the elevated temperature during the activation process, indicating the occurrence of certain physicochemical phenomena.

4. Trench Walls Recovery by Gas Phase Methods

4.1. Introduction

Mechanical polishing, Reactive Ion Etch (RIE), or other energetic fabrication techniques are indispensable in the manufacturing of microelectronic devices, but often these techniques bring to the surface some issues related to the formation of lattice damage, high energy surface states, and morphological inhomogeneity. In paragraph 1.3.3, the formation of striations on the walls of the trenches fabricated by DRIE was introduced. It is commonly noted that the presence of damaged areas in the material degrades the devices' performances such as the decrease of the charge mobility [131]. In addition, morphological discontinuities could cause further issues for subsequent treatments. Trench MOSFET technology entails the coating of trench walls with a layer of SiO_2 or other dielectrics. The existence of striations may result in poor deposition quality. The striations start up to the surface and go down till the end of the walls as shown in Fig. 4.1. The striations are densely distributed, with some spreading in depth and width.

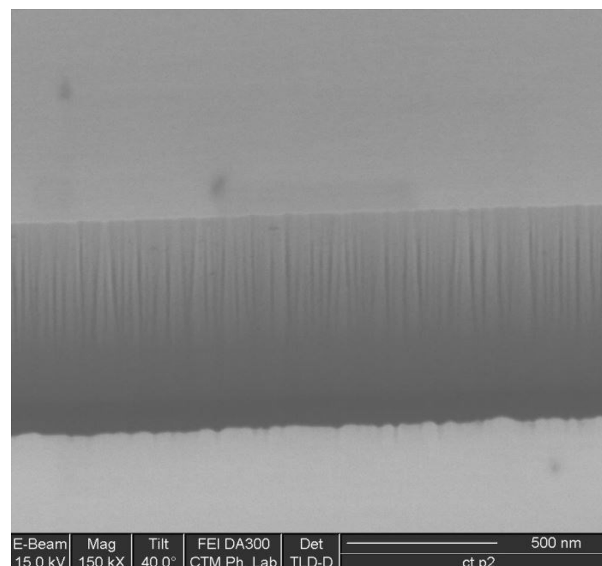


Fig. 4.1 SEM micrograph of trenches with striations on the walls.

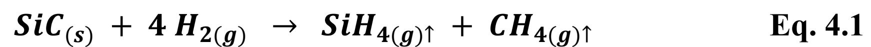
Many approaches could be employed as an attempt to reduce the striations. In this doctoral dissertation, a physicochemical route was chosen. The gas etching in the reducent H_2 gas environment and the sacrificial oxidation techniques were combined. The gas etching technique is commonly employed in obtaining a flat surface after manufacturing steps that involve superficial

lattice damage. In principle, the gas etching technique should favor damage recovery. Gas etching alone does not fit as a stand-alone technique to recover the 4H-SiC trenches wall. Rather than only H_2 etching, dry thermal oxide growth serves as a complementary technique to oxidize the surface and completely get rid of the striations by successive oxide etching in diluted hydrofluoric acid (HF). The combination of gas etching and thermal oxidation could provide the elimination of the lattice damage after the DRIE attack [132] employed in the fabrication of the trenches. Gas etching and dry oxidation of SiC fundamentals will be covered in the following paragraphs.

Another important aspect after oxide growth concerns the variation of trench distance: in particular, after the dry oxidation process, a thin but still impactful oxide layer reduces the width of the trenches and so the distance between them. The oxide removal in HF solution is, unfortunately not effective in overcoming this problem because it might cause the reduction of edge sharpness and consequently the lessening of the electric field tip effect [133,134].

4.1.1. H_2 Gas Phase Etching

Gas etching of 4H-SiC is typically performed using H_2 gas, which acts as a reducing agent. Thermodynamics and kinetics theoretical evaluations were done by researchers with chemical density functional theory. H_2 gas attacks SiC from the surface eliminating C as CH_4 and Si as SiH_4 both evoluting as gas molecules following the reaction in Eq. 4.1. The SiC etching passes through intermediate steps with the formation of surface chemical groups such as Si-CH_3, SiH_3CH_2, SiH_2 and so on [135].



$$SiC_{(s)} + 4\,H_{2(g)} \rightarrow SiH_{4(g)\uparrow} + CH_{4(g)\uparrow} \qquad \textbf{Eq. 4.1}$$

On SiC, the gas etching technique is broadly adopted since it is suitable for 4H-, 6H-, and 3C-SiC polytypes and in both on- and off-axis sides [136–138]. Gas etching occurs in a relatively short time ranging from 5 to 30 minutes. Generally, 3C-SiC requires a lower temperature of about 1250 °C than hexagonal polytypes which require a higher temperature from 1400 °C to 1550 °C [136].

The gas etching phenomena, as a matter of industrial value, was studied and a theoretical model was also developed. With the aim of decreasing the etching time, physical variables of most importance are temperature, pressure, H_2 concentration, and flow. The H_2 concentration is adjusted by Ar gas injection in the chamber. The etching rate linearly increases with H_2 flow and temperature, whereas it linearly decreases with pressure. Theoretical equations are in good accordance with the experimental data [107].

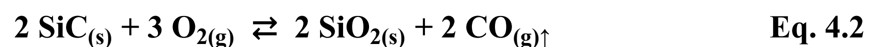
If on the one hand gas etching has beneficial effects on device manufacturing, on the other some collateral issues can occur. Since the H_2 gas etching requires high temperature, Si sublimation, and C migration takes place on the surface, with the consequent formation of the so-called Giant Bunching Steps (GBS). Due to the formation of regularly spaced structures, GBS were used in nanostructure fabrication [139–141]. Moreover, the gas etching could lead to the formation of graphene from the SiC surface. If graphene growth is useful for graphene CMOS-based devices fabrication [142,143], for *STMicroelectronics* SiC-based devices this phenomenon is unwanted.

By evidence, GBS mostly form inside the mass transfer limit region after the formation of the C cluster after Si sublimation [144]. The phenomenon is governed by temperature and pressure conditions. In particular, high pressure does not let a proper diffusion of byproducts, and C clusters easily form. A high H_2 percentage represses the formation of C clusters formation and the issue is overwhelmed.

4.1.2. Sacrificial Oxidation

Gas etching alone does not fit as a stand-alone technique to fully recover the 4H-SiC trenches wall. Rather than only etching, dry thermal oxide growth serves as a complementary technique to oxidize the surface and get rid of the striations by successive etching in diluted HF. The combination of gas etching and thermal oxidation provides the elimination of lattice damage after the DRIE attack [132]. Moreover, it is well known that DRIE is not sufficient to remove dangling bonds and sacrificial oxide is required [145].

SiC oxidation has been largely studied [146–149] because of its importance in electronic device fabrication [150,151]. An exhaustive model for SiC thermal oxidation is nowadays accepted and the equation that occurs is shown in Eq. **4.2**.



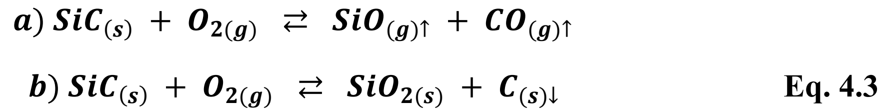
$$\mathbf{2\ SiC_{(s)} + 3\ O_{2(g)} \rightleftarrows 2\ SiO_{2(s)} + 2\ CO_{(g)\uparrow}} \qquad \textbf{Eq. 4.2}$$

Observing the reaction at equilibrium, during this process, two major problems occur:

- During the oxide growth, less oxygen will be available at the SiC/SiO_2 interface (where the reaction takes place).
- The SiO_2 layer limits the CO molecules' diffusion, thus hindering the reaction to proceed, according to the *Le Châtelier* principle.

The model was released for silicon with the name *Deal Grove* model [152] and next updated for SiC [153] where other peculiarities take place due to the more complex nature.

Dry oxidation on SiC strongly depends on the temperature and the face orientation. In particular, the oxidation rate increases with the temperature, and higher rates were found in $(000\overline{1})$ C-face than (0001) Si-face termination. Intermediate rate values were determined for amorphous SiC (a-SiC) which is probable to be found after DRIE processes [153]. Temperature and O_2 pressure must be accurately tailored because of the eventuality of side reactions such as the evolution of SiO gas (high temperature and O_2 low pressure, reaction in Eq. 4.3a and the precipitation of C (low temperature and O_2 high pressure, reaction in Eq. 4.3b [150,154,155].



$$\boldsymbol{a})\ \boldsymbol{SiC}_{(s)} + \boldsymbol{O}_{2(g)} \rightleftarrows \boldsymbol{SiO}_{(g)\uparrow} + \boldsymbol{CO}_{(g)\uparrow}$$
$$\boldsymbol{b})\ \boldsymbol{SiC}_{(s)} + \boldsymbol{O}_{2(g)} \rightleftarrows \boldsymbol{SiO}_{2(s)} + \boldsymbol{C}_{(s)\downarrow} \qquad \textbf{Eq. 4.3}$$

Taking into account the thermodynamics and kinetics at the SiC/SiO_2 interface, an ideal temperature range can be deduced. Firstly, an oxide thickness of about 15 nm is enough to limit CO diffusion during dry oxidation in the range of 1100-1300 °C on 4H-SiC (0001). Secondly, the O_2 solubility in SiO_2 ($2.5\cdot10^{16}$ cm^{-2} [156]) leads to a pO_2 (at the reaction interface) of $5\cdot10^{2}$ Pa in 1 atm pO_2 ambient at 1300 °C. After the aforementioned considerations, an ideal range of temperature for a clean dry oxidation process is estimated to range from 1100 to 1400 °C [150].

4.2. Materials and Methods

Gas etching experiments were performed on trench-patterned 150 mm 4H-SiC wafers with a dedicated tool supplied by a sector leader company. Relevant parameters were optimized following a Design of Experiment (DOE) chart and by varying the time, pressure, temperature, H_2, and Ar flow rate according to values variations in two or three levels. The desired temperature was reached with a heating ramp of 323 °C/min. Sacrificial oxide growth was realized by using a dedicated instrument of the same company. Oxidation occurred at a temperature of 1200 °C, at a fixed O_2 flow rate and pressure for a time length of 30 min. The thin oxide layer was removed by dipping in diluted HF solution, following washing in DI water and drying in N_2 flow. Trench micrographs were acquired by *SEM* (*FEI DA300*).

The DOE input values were the roughness data measured by a developed method to analyze SEM micrograph images. The developed method will be explained in paragraph 4.2.1. Curvature analysis was also performed by ImageJ free software [157] by first fixing the scale factor. A curvature analysis plugin named Kappa was installed for this purpose. The observable obtained from the analysis was the curvature value expressed in μm^{-1}. A set of 8 measurements were made

making a distinction between 4 measurements on the top side of the trenches and 4 measurements on the bottom side. Mean and standard deviation values are reported in the discussion section.

4.2.1. Description of Image Analysis Method

The conventional techniques for morphological characterization, such as Focused Ion Beam (FIB) and Scanning Electron Microscopy (SEM), produce images that result from converting the instrumental signal into grayscale. As a consequence, they do not provide information about the surface roughness in a three-dimensional system. On the other hand, direct roughness measurements by Atomic Force Microscopy (AFM) would be fundamental in trenches wall recovery evaluation. However, the AFM should be the best technique to evaluate the wall roughness variation after the recovery methods, unless the use of industrial-adapted instruments, is a destructive technique due to the necessity to dice the wafer in smaller samples. Even if the sample is diced, a section should be made to orient the surface to be analyzed orthogonal to the AFM tip.

In virtue of the SEM technique, adapted for wafer analysis, images were analyzed by a colorimetric approach that overcomes the aforementioned issue by grayscale evaluation and consecutive relative roughness (RR) values measurement. The RR value is the denomination adopted in the present project to indicate the roughness value estimated by the developed image analysis approach. The method facilitated the assessment of the recovery effectiveness after the dedicated treatments of gas etching and sacrificial oxidation.

The image analysis has been useful in the roughness evaluation of SEM micrograph images where only the grayscale values can be used as a data source. The grayscale values were measured by ImageJ free software [157]. AFM analyses were done through the dedicated software. The acquired roughness sections were performed, on both methods, along a diagonal line drawn with the appropriate software tool. The profile obtained from the two approaches has been adopted as a source of data for statistical calculation and hence for the roughness evaluation. Taking into account the basic statistical parameters, the mean and median are not suitable, since the AFM and grayscale lay on different ranges of values. The dispersion around the mean value is a better parameter for roughness evaluation, and consequently, Standard Deviation (SD) was chosen as the measurement variable.

Early measurements provided validation trials for the method. Grayscale was compared to AFM section analysis by graphical and statistical approaches. At first, the 4H-SiC Si-face (0001) surface was analyzed and the 2D AFM image was reported in Fig. 4.2a. Directly from the image, the AFM section profile and grayscale section values were compared in Fig. 4.2b. The 4H-SiC Si-face is characterized by atomic flatness with a roughness RMS value of around 0.2/0.3 nm. The AFM

section height has a profile comparable to the grayscale section. The second trial involved the 4H-SiC C-face ($000\bar{1}$) which is characterized by higher roughness due to the typical face off-axis. AFM analysis (see the image in Fig. 4.2c) permits to do the height profile measurements again by using both AFM and image analysis whose roughness section is shown in Fig. 4.2d. The abovementioned trials underwent F-test statistical analysis which aims to validate the image analysis method. The F-test result elucidated the absence of major differences between the two profiles with a significance level of $\alpha = 0.1$.

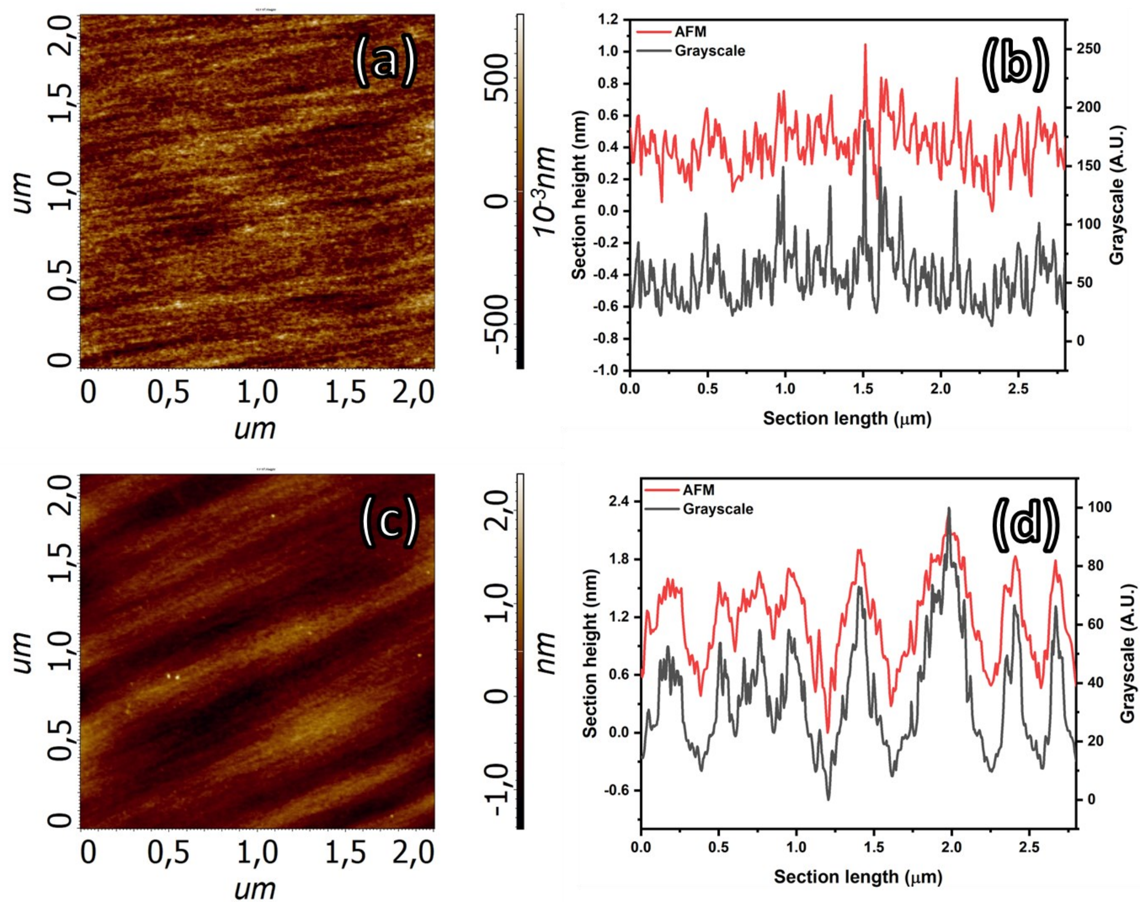


Fig. 4.2 AFM 2D images on 4 μm² scan of (a) 4H-SiC Si-face and (c) 4H-SiC C-face. Comparison of roughness measured by AFM (red curve) and grayscale (gray curve) of (b) 4H-SiC Si-face and (d) 4H-SiC C-face.

To further validate the method, the AFM and grayscale profiles were achieved starting from trench structures of 4H-SiC as shown in the AFM image Fig. 4.3a. Higher and cleaner profiles permit obtaining a high degree of superimposability between the AFM and grayscale sections as demonstrated in Fig. 4.3b.

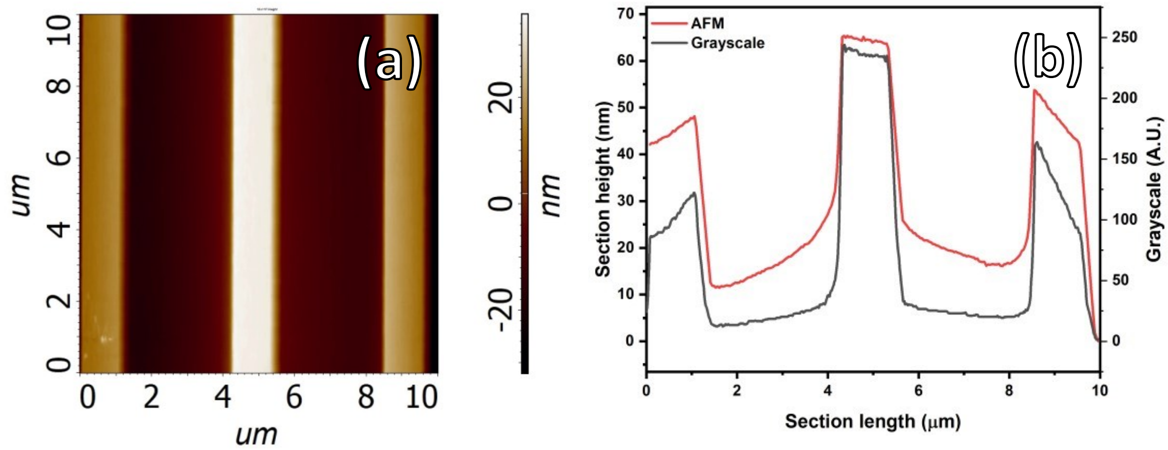


Fig. 4.3 AFM image of the 4H-SiC trench and (b) comparison of trenches height profile from AFM (red curve) and grayscale (gray curve) methods.

The first trial revealed a difference in SD value between the two methods equal to 5.37% whereas the second regarding the C-face analysis revealed a difference of 8.82%. Finally, the last trial revealed a difference of only 3.22% between the SD values obtained by AFM and the grayscale dataset. All the data are resumed in Tab. 4.1.

Sample	Method	Standard Deviation	Difference percentage (%)
4H-SiC Si-face	AFM (nm)	14.35	5.37
	Grayscale (A.U.)	13.58	
4H-SiC C-face	AFM (nm)	19.21	8.82
	Grayscale (A.U.)	18.59	
4H-SiC trench	AFM (nm)	26.47	3.22
	Grayscale (A.U.)	29.03	

Tab. 4.1 Standard deviation values calculated from AFM and grayscale of 4H-SiC Si-face, C-face, and trench sections.

After the validation of the method, the Relative Roughness (RR) terminology will refer to the grayscale standard deviation as the fundamental roughness value of the walls. We analyzed the mean value of RR and its standard deviation to assess the effectiveness and consistency of the recovery treatments.

Although RR data are crucial for optimizing the recovery treatments, they only allow for relative comparisons between samples. To obtain an absolute roughness value (RA) expressed in

nanometers, we established a phenomenological calibration curve (Fig. 4.4) using 4 AFM measurements. The fitting equation is shown in Fig. 4.4.

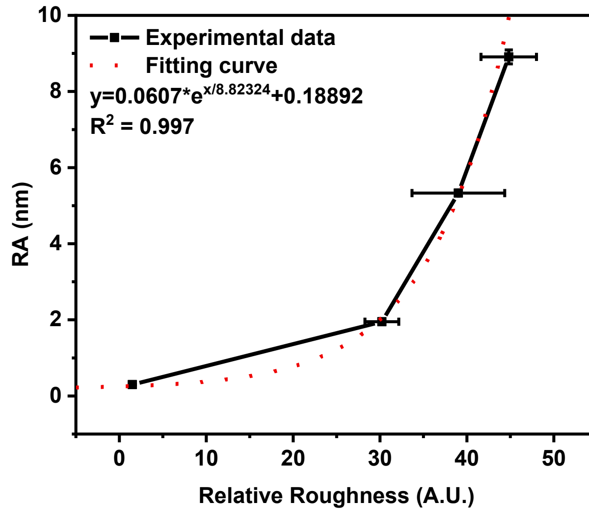


Fig. 4.4 Fitting graph of Relative Roughness (RR) in Roughness Average (RA) values. The fitting equation is reported in the graph.

The developed method of roughness image analysis was adopted in the roughness evaluation of trench walls before and after the recovery treatments. The numerical data generated by the image analysis method were used in the Design of Experiment (DOE) approach for combining gas etching and sacrificial oxidation techniques. The aim was to optimize these techniques to obtain flat trench walls.

4.3. Results and Discussions

The DRIE attack causes the formation of striations along the direction of the etching path. The striations appear in random repetition in terms of width and shape. This effect is visible as early as in the Hard Mask Oxide (HMO) layer after the DRIE attack in Fig. 4.5a, although the underneath 4H-SiC (Fig. 4.5c) finds a higher striation density and aspect randomness than the HMO. The striations difference is furthermore evident in Fig. 4.5e where a comparison of striation frequency between HMO and 4H-SiC is displayed. SiC substrate (red curve) develops more numerous and more pronounced (higher intensity) striations than HMO (black curve). Noteworthy, AFM analysis (in Fig. 5.3 of chapter 5) on the top part of the trench evidenced a similar striation transfer issue from the HMO layer to the 4H-SiC substrate. Sideview image acquisition revealed that in both HMO (Fig. 4.5b) and 4H-SiC substrate (Fig. 4.5d), the striation pattern is not affected by the trench depth.

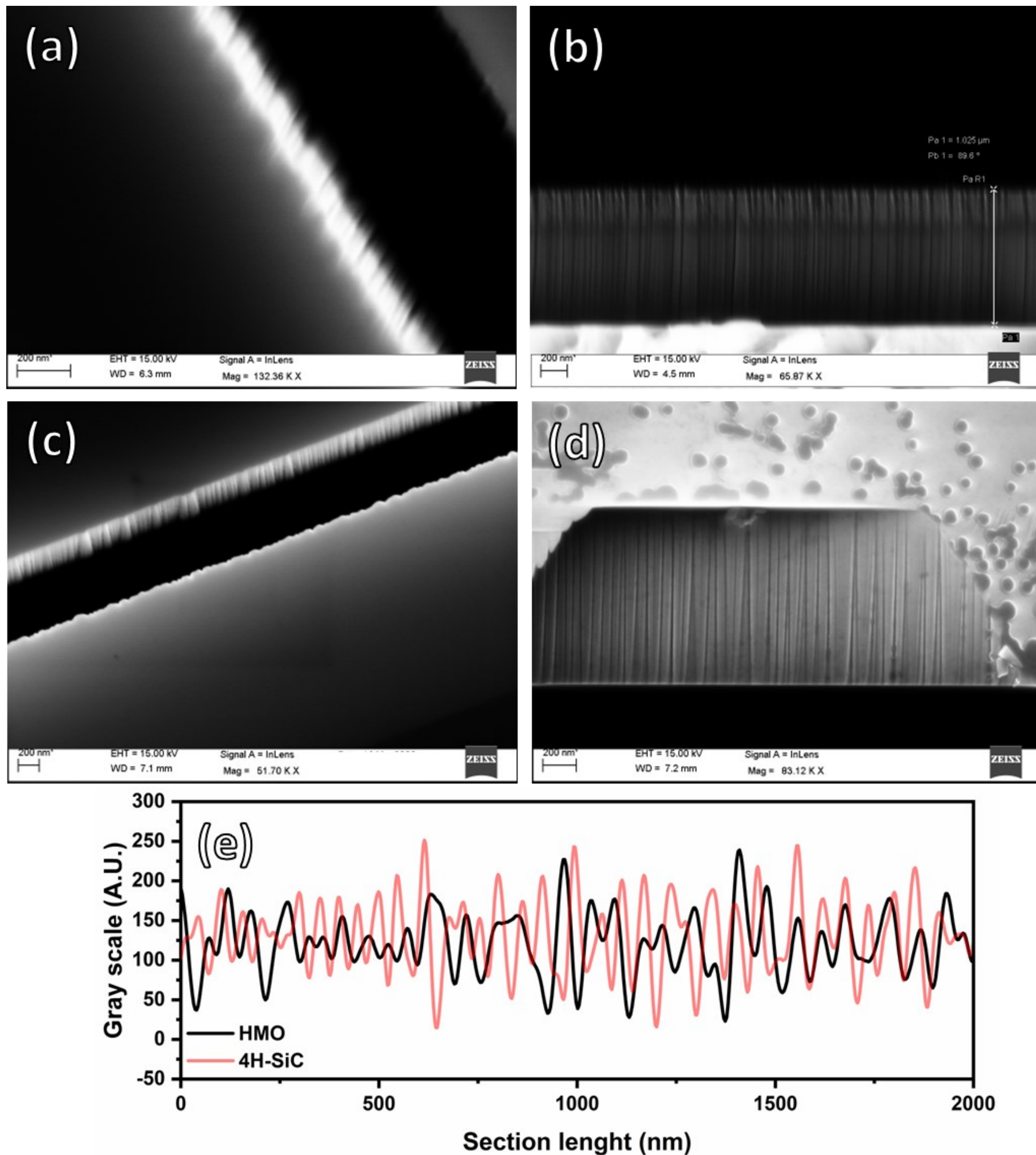


Fig. 4.5 SEM micrographs of HMO layer a, b) and 4H-SiC c, d) after the DRIE process. e) Grayscale values from SEM images of HMO (black curve) and 4H-SiC (red curve) after trench formation.

The image analysis estimated a roughness difference between the HMO and the underlying 4H-SiC of 10%. The striation formation is ascribable to C sublimation and/or migration from the surface since it was detected the presence of Si at zero-state (Si^0 at BE 99.9 eV) signal bond in XPS analysis of 4H-SiC after DRIE and HMO removal (spectra in Fig. 4.6) together with the expected SiC and non-stochiometric silicon oxide signals detected at BE of 101.4 and 102.2 eV respectively.

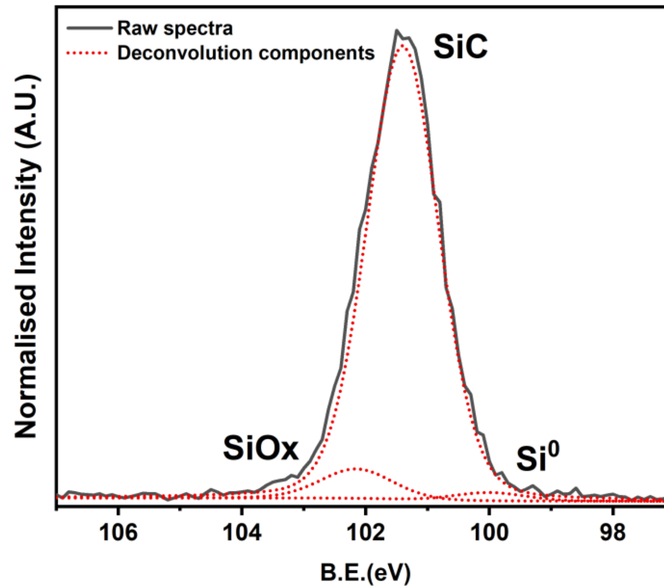


Fig. 4.6 XPS Si2p signal of 4H-SiC after DRIE and HMO removal.

Preliminary results lead to the hypothesis that 4H-SiC striations develop according to a molding-like mechanism in accordance formation of striations at the top of the process on the resist polymer during the HMO patterning (data not shown). Since polymer chemistry, in the DRIE environment, is difficult to understand, the 4H-SiC recovery remains the most viable method to overcome the issue.

Gas etching and sacrificial oxide growth parameters optimizations were performed following the DOE chart in Tab. 4.2 where temperature, time, pressure, H_2, and Ar gas flows were varied. For a matter of company confidentiality, the values of the factors involved in the studied where coded in -1 (low), 0 (medium), and +1 (high) levels. Anyway, it is possible to understand the behavior of the gas etching and sacrificial oxidation techniques combination on 4H-SiC. A total of 9 tests were performed where ID 1.8 and ID 1.9 experienced sacrificial oxide growth after the gas etching treatment. In particular, ID 1.8 and ID 1.9 samples went through the same gas etch treatments as ID 1.2 and ID 1.3 samples.

Sample	Run	T (°C)	t (min)	H_2 flow rate (sccm)	Ar flow rate (sccm)	Pressure (mbar)	Sacrificial Oxide	RA (nm)
Reference	NA	NA	NA	NA	NA	NA	NA	5.36 ± 0.20
ID 1.1	1	-1	-1	-1	-1	0	no	2.23 ± 0.18
ID 1.2	2	0	-1	-1	-1	0	no	1.83 ± 0.19
ID 1.3	3	+1	-1	-1	-1	0	no	2.08 ± 0.19
ID 1.4	4	0	-1	-1	-1	-1	no	0.61 ± 0.20
ID 1.5	5	0	-1	-1	-1	+1	no	1.83 ± 0.18
ID 1.6	6	0	-1	+1	+1	0	no	1.24 ± 0.20
ID 1.7	7	0	+1	-1	-1	0	no	0.48 ± 0.19
ID 1.8	2	0	-1	-1	-1	0	yes	1.38 ± 0.25
ID 1.9	3	+1	-1	-1	-1	0	yes	1.12 ± 0.17

Tab. 4.2 First DOE chart to optimize relevant parameters. The factors' values were coded in +1 (high), 0 (medium), and -1 (lower) levels. RA values were measured by the image analysis method.

In every treatment, it was obtained a consistent reduction of RA compared with the reference sample that was not involved in any treatment after the DRIE process. Generally, the roughness detected is over 1 nm, hence far from the characteristic flatness of the 4H-SiC surface. The best recovery results were obtained for ID 1.4 and ID 1.7 with an average RA value of 0.61 and 0.48 nm respectively. Despite the reduction degree of striations, most of the samples do not find relevant enhancements in terms of striations drop as evidenced by SEM micrographs in Fig. 4.7. Additionally, the results were not promising since it is possible to glimpse the presence of the Giant Bunching Steps (GBS) on the top part of the samples from ID 1.3 to ID 1.9 in Fig. 4.7. Their formation constitutes a major drawback of the gas etching technique.

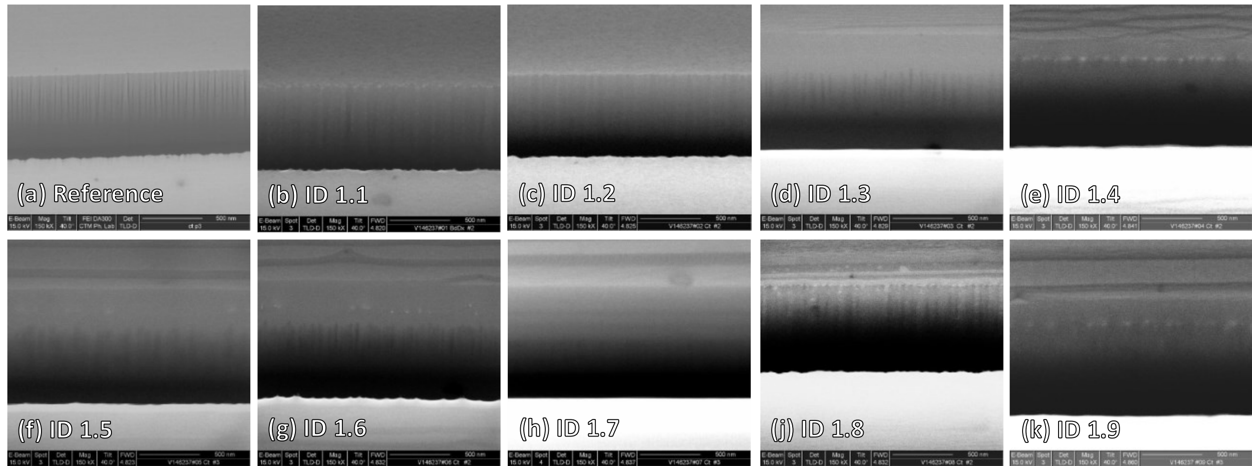


Fig. 4.7 SEM micrographs of 4H-SiC shallow trenches of a) reference, b) ID 1.1, c) ID 1.2, d) ID 1.3, e) ID 1.4, f) ID 1.5, g) ID 1.6, h) ID 1.7, j) ID 1.8, and k) ID 1.9 samples.

In the first experimental set, the sacrificial oxide step does not seem to have beneficial effects on striations recovery. The roughness values mentioned earlier were estimated using the developed image analysis method, described in paragraph 4.2.1. This method makes it possible to introduce numerical data to the DOE.

Contour plots in Fig. 4.8 and fitting variable factors in Tab. 4.3 are shown. The study was particularly interesting and fruitful thanks to the possibility of optimizing the relevant variables of the recovery approaches. All of the contour plots in Fig. 4.8 have temperature as a fixed parameter on the x-axis. In fact, all of the plots are vertically symmetrical. Hence, an average level of temperature seems to be advantageous in obtaining a reduction in roughness. Anyway, the temperature factor value in Tab. 4.3 suggests a minor role in the overall process. As the time increases, the roughness decreases as expected and is further confirmed by the RSM in Fig. 4.8a. The time variable is the most influential. The pressure is the second most significant variable of the study and the most important parameter of the instrument. From Fig. 4.8b, it is possible to note a strong negative influence of the pressure on the roughness reduction. Finally, the H_2 flow rate plays a minor role in the roughness reduction (Fig. 4.8c and Tab. 4.3). The results could be attributed to a saturation level of the surface already achieved at the lowest set factor value. Finally, it should be noted how the factors are consistent with the results of the scientific literature as discussed in paragraph 4.1.1.

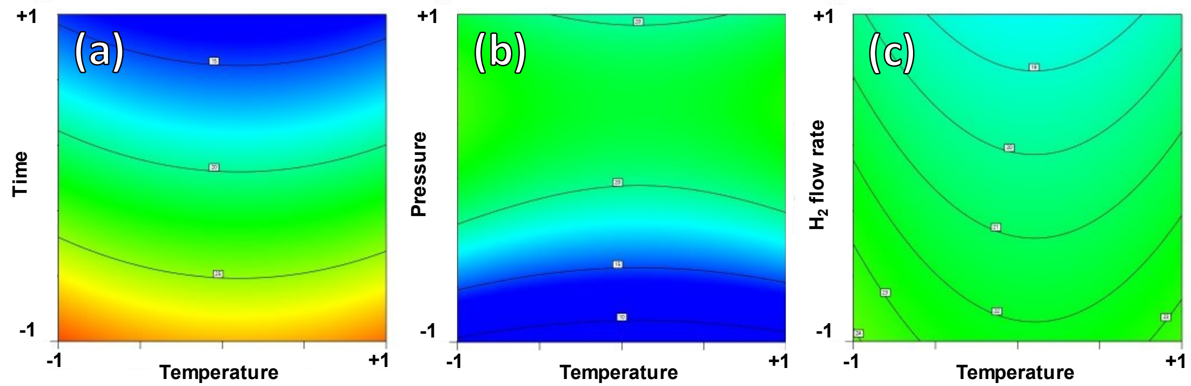


Fig. 4.8 Contour plot of gas etching factors: a) time vs. temperature, b) pressure vs. temperature, and c) H_2 flow rate vs. temperature. Reduction of roughness lower going from red to blue color.

Response	Temperature (°C)	Time (min)	H_2 flow rate (sccm)	Ar flow rate (slm)	Pressure (mbar)	Sacrificial oxide
RR	-2.03	-7.68	-1.95	NA	+5.99	-1.42

Tab. 4.3 DOE variables factors affect on roughness response. Positive and negative factor values were respectively colored in red and blue.

The overlap between our results and those of the scientific literature reinforces and further confirms the effectiveness of the image analysis method. The early findings allowed the planning of a new DOE chart to further optimize the gas etching and sacrificial oxide growth combination with the aim of promoting a more efficient striations decrement. For this reason, it was established a second experimental set taking into account the previous results. In the present DOE chart (Tab. 4.4), the temperature was fixed at a middle value according to the previous experimental set, whereas other parameters were varied according to the results of the precedent DOE. Only ID 2.1 and ID 2.2 samples were submitted to sacrificial oxide growth treatment. Specifically, ID 2.3 and ID 2.4 were treated in the same way of respectively ID 2.1 and ID 2.2 but with additional growth of the sacrificial oxide layer. The samples ID 2.2 and ID 2.4 were treated according to the optimized variables settings corresponding to the results of the previous DOE.

	t (min)	H_2 flow rate (sccm)	Ar flow rate (sccm)	Pressure (mbar)	Sacrificial Oxide	RA (nm)
Reference	NA	NA	NA	NA	NA	5.36 ± 0.20
ID 2.1	+1	-1	-1	+1	No	3.21 ± 0.20
ID 2.2	+1	+1	-1	-1	No	1.04 ± 0.23
ID 2.3	+1	-1	-1	+1	Yes	0.60 ± 0.22
ID 2.4	+1	+1	-1	-1	Yes	0.41 ± 0.21
ID 2.5	+1	-1	-1	-1	Yes	0.47 ± 0.19
ID 2.6	+1	+1	+1	-1	Yes	0.40 ± 0.27
ID 2.7	-1	-1	-1	-1	Yes	0.39 ± 0.21

Tab. 4.4 Second DOE chart with the aim to optimize relevant parameters. The factors' values were coded in +1 (high), 0 (medium), and -1 (lower) levels. RA values were measured by the image analysis method.

The SEM images in Fig. 4.9 definitely exhibit better results than the ones of the previous experiment by only comparing with the SEM micrographs of the first set of experiments in Fig. 4.7. The gas etching instrument was opportunely set in order to avoid the formation of the GBS which were visible in the previous samples in Fig. 4.7. The additional phenomenon is not discussed for a matter of briefness.

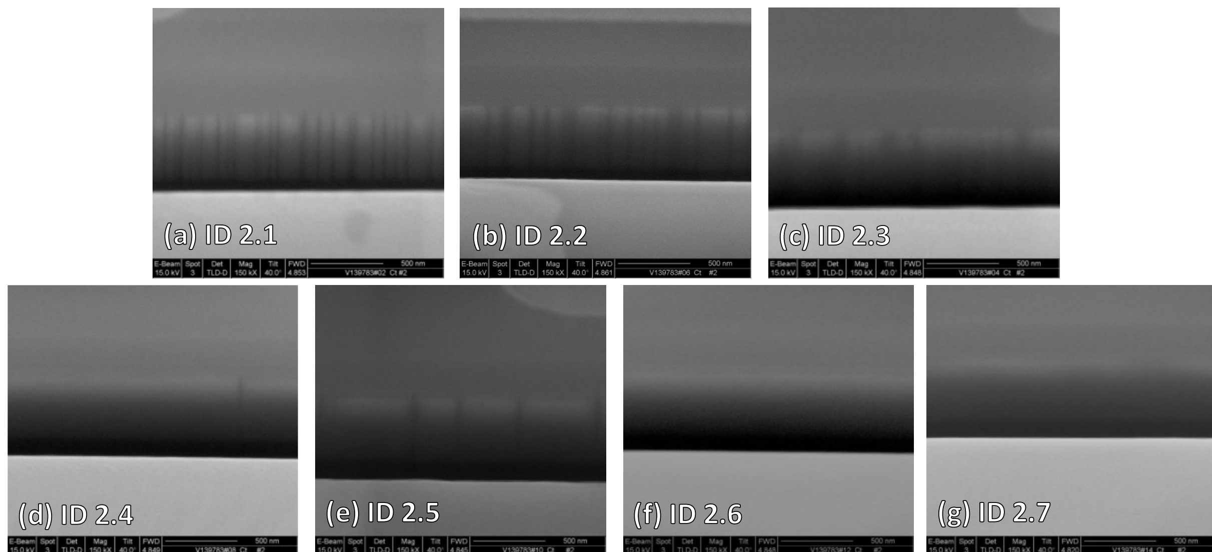


Fig. 4.9 SEM micrographs of 4H-SiC shallow trenches of a) ID 2.1, b) ID 2.2, c) ID 2.3, d) ID 2.4, e) ID 2.5, f) ID 2.6, and g) ID 2.7.

The second run of experiments allowed us to obtain better results. Firstly, an essential decrease of RA passing from ID 2.1 to ID 2.2 (samples without sacrificial oxide step) was revealed, underlining the importance of the previous DOE and the effects of the optimized variables settings. Secondly, further RA value decrement was registered after sacrificial oxide treatments, highlighting the beneficial effects of the sacrificial oxidation technique. The most favorable outcomes were achieved for ID 2.4 (optimized settings), ID 2.6, and ID 2.7. The last three mentioned samples have comparable RA values. In particular, the samples ID 2.4, ID 2.6, and ID 2.7 were distinguished by 75% RA decrement in comparison with the reference sample.

Once the trenches have been restored, the size of the layout should match that of the desired design. Unfortunately, the etch recovery processes slightly modify the geometry of the system. One of the parameters taken into account is the distance between two adjacent trenches, namely the Critical Dimension (CD) parameter. As evidenced in Tab. 4.5, the Top Critical Dimension (TCD) changes with only gas etch or even with the combination with the sacrificial oxide growth.

The results shed light on the major role of gas etch in the trenches geometry modification: size reduction is observed on the Bottom Critical Dimension (BCD) after the recovery treatments. In the same way, the trenches' height increases by 10-40 nm due to the etch in the gas phase and the sacrificial oxidation. The variation of the height seems to be more subjected to modification than the CDs.

Samples	Oxide growth	CD_{up} (nm)	CD_{down} (nm)	Height (nm)
Reference	NA	923	725	1026
ID 2.1	No	750	687	1034
ID 2.2	No	713	664	1069
ID 2.3	Yes	764	691	1070
ID 2.4	Yes	762	750	1385
ID 2.5	Yes	774	746	1083
ID 2.6	Yes	770	717	1070
ID 2.7	Yes	762	716	1075

Tab. 4.5 CD and height values of second DOE samples.

In trench MOSFET technology, it should be avoided to have sharp corners because of the accumulation of charges and the creation of a high electric field that will be detrimental to device performance. Experimental data gave interesting results concerning the curvature values of both the

top and bottom corners of the trenches. The curvature of the trenches was assessed by Kappa plugin of ImageJ software. The curvature value expresses the deviation from the linearity of an object boundary. Hence, a higher curvature value indicates sharper borders than a lower curvature value which indeed implies smoother edges. From these assumptions, gas etching alone contributes to reducing the corners' sharpness as evidenced by ID 2.1 and ID 2.2 curvature values in comparison to the reference (Fig. 4.10). Dry oxidation and successive SiO_2 etch do not lead to further reduction of curvature. The only main effect stands in an evident inversion of corners' smoothness from the bottom (reference sample) to the top side (oxide-treated samples).

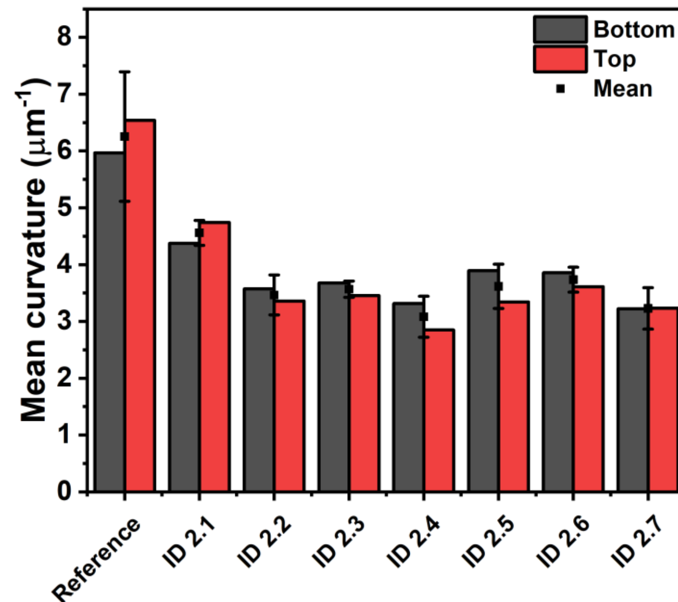


Fig. 4.10 Curvature analysis of second DOE samples. Trench top side (red bars), bottom side (dark gray bars), and total mean value (black dot).

The multi-approach technique of gas phase H_2 etching and sacrificial oxide growth consistently reduced the striations on the walls of shallow trenches fabricated using the DRIE technique and led to the corner smoothness increment of about 50%.

4.4. Conclusions

The present work involved the recovery of shallow trenches in next-generation trench MOSFET. The development of vertical MOSFETs aims to increase the device's performance and reduce its size and weight. The efforts are well-demanded since such improvements lead to a decrement in energy consumption due to the enhancement of energy conversion yield.

The implementation of trench MOSFET requires numerous steps starting from HMO deposition, going through photolithography, and ending with the complex DRIE process. The fabrication of

shallow SiC trenches by DRIE does not directly return flat trenches walls. Recovery methods should be taken into account to retrieve the atomic flatness that characterizes the 4H-SiC.

The physical methods involved a gas etching in an H_2-rich environment and successive sacrificial oxidation. After two sets of Design of Experiments (DOE), the combination of H_2 gas phase etching and sacrificial oxide growth was optimized. The multi-approach treatment had a dual beneficial effect: reduction of striations and corner smoothing.

The evaluation of the wall roughness, for non-disposable samples, was accomplished by developing an image analysis out of SEM micrographs. The data relevant to the DOE were collected by evaluating the variations in the intensity of the grayscale among the samples analyzed by following the conversion in average roughness, expressed in nanometers, using an experimental calibration curve. Consistent improvements in terms of trench wall quality were revealed after the second DOE. The ImageJ software was used to analyze further morphological characteristics of the trenches, such as the distance between the trenches and the smoothness of the edges. The image analysis method facilitated the overall optimization of the trench recovery and acceleration of the device development.

Further characterizations were carried out by performing elemental and chemical analyses using EDX and XPS techniques, respectively. The surface chemical analysis has indicated the presence of elemental silicon, which has led to speculation about the phenomena involved in gas etching. Moreover, the presence of elemental silicon has opened up the possibility of etching the detected Si-Si bond moieties using standard etch solutions. This will be discussed in the following chapter, starting the section dedicated to the chemical approaches of etch.

5. Standard Wet Chemical Etching

5.1. Introduction

The striations on the trenches wall were revealed as early as the HMO layer. The patterned HMO layer is defined by photolithography involving the deposition of a photoresist layer. The adoption of HMO is related to the fact that the photoresist is not suitable to directly undergo the DRIE process because it would degrade after fluorine radicals attack and, accordingly, it has been hypothesized (see paragraph 4.3) a transfer of striations from the HMO to the rest of the stack as displayed in the illustration of Fig. 5.1. The striations begin to form up to the HMO layer during the DRIE process, as shown in Fig. 5.1a. As the DRIE progresses, the striations transfer to the underlying 4H-SiC, as seen in Fig. 5.1b. Eventually, the thick HMO layer is eliminated using an HF solution, leaving the striations on the 4H-SiC.

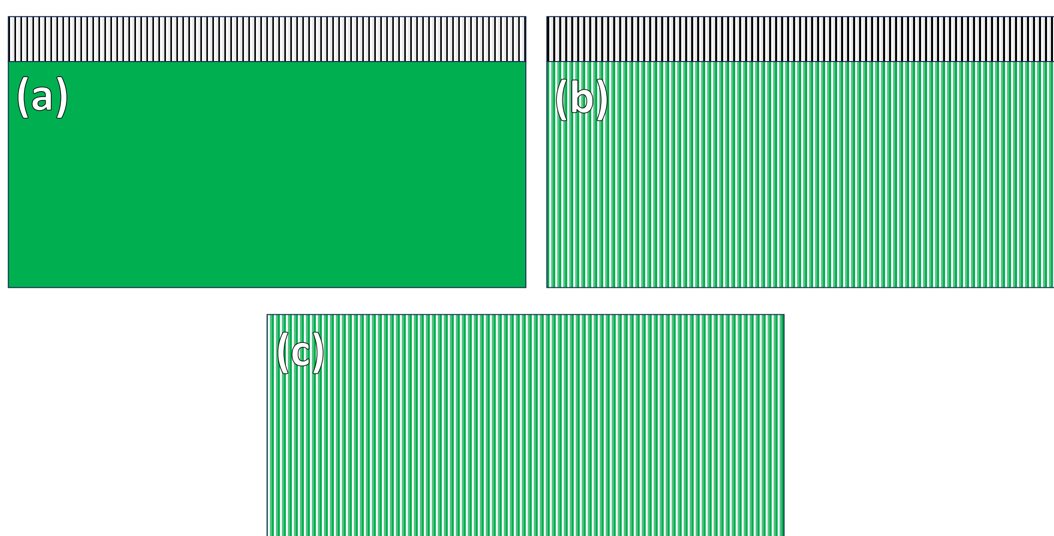


Fig. 5.1 Illustration of trench wall striations transfer from HMO to 4H-SiC.

As discussed in the previous chapter, physical methods, in specific thermal H_2 gas etching and sacrificial thermal oxide growth, were effective in shallow trench roughness recovery. Elemental and morphological characterization (performed by XPS) of etched SiC, following HMO deposition and the DRIE process, evidenced the presence of silicon-rich areas in the material. This finding has driven us toward the possibility of chemically recovering the trenches wall after the DRIE process. The Si etchability in a standard acidic solution is discussed in paragraph 1.7.

5.2. Materials and Methods

Etching experiments were conducted with high-grade reagents by *Sigma-Aldrich*. HNO_3:HF solution was prepared from nitric acid (HNO_3) ≥90 wt% (density = 1.48 g/mL at 20 °C; M_w = 63.01 g/mol, *Sigma-Aldrich*) and hydrofluoric acid (HF) 48-51 wt% (density = 1.16 g/mL at 20 °C; Mw = 20.01 g/mol, *Sigma-Aldrich*) stock solutions. Potassium hydroxide (KOH, M_w = 56.11 g/mol, *Sigma-Aldrich*) solution was made from pellets at a concentration of 3 mol/L by weighing the adequate mass of the reagent. The solution dilution and the sample washing were made with ultrapure water (18.2 MΩ cm, TOC 1 pbm, PURELAB Flex 3 by *Elga Veolia company*). Etching procedures were performed in a Teflon beaker where HF was involved. KOH etching was accomplished in a *Pyrex* glass beaker. Solution heating at 45 °C and 60 °C was achieved by putting the beakers in bain-Maire during the period of the experiment. Samples after etching were washed in DI water and dried under N_2 flow. Sample analyses were run without further preparations.

5.3. Results and Discussions

Etching techniques based on hard or soft sputtering have effects to some extent on material quality. Although the DRIE system can be optimized, it is hardly possible to completely eliminate the damages. The optimized DRIE process results in the formation of striations on the trench walls of the HMO layer (Fig. 5.2a) and on the underlying 4H-SiC (Fig. 5.2b), which are visible after dissolution of the oxide in a 5% HF solution. The striations transfer from the HMO to the underneath SiC substrate as a result of a molding-like phenomenon. The appearance of the striations comes all around the wafer on both the wall sides of the trench.

In the present work, the roughness of the trench's wall surface was evaluated by AFM (*NT-MDT modular AFM NTEGRA*). The striations can be seen on both the HMO (Fig. 5.2c) and the SiC (Fig. 5.2d) trenches by which interesting information follows in the text.

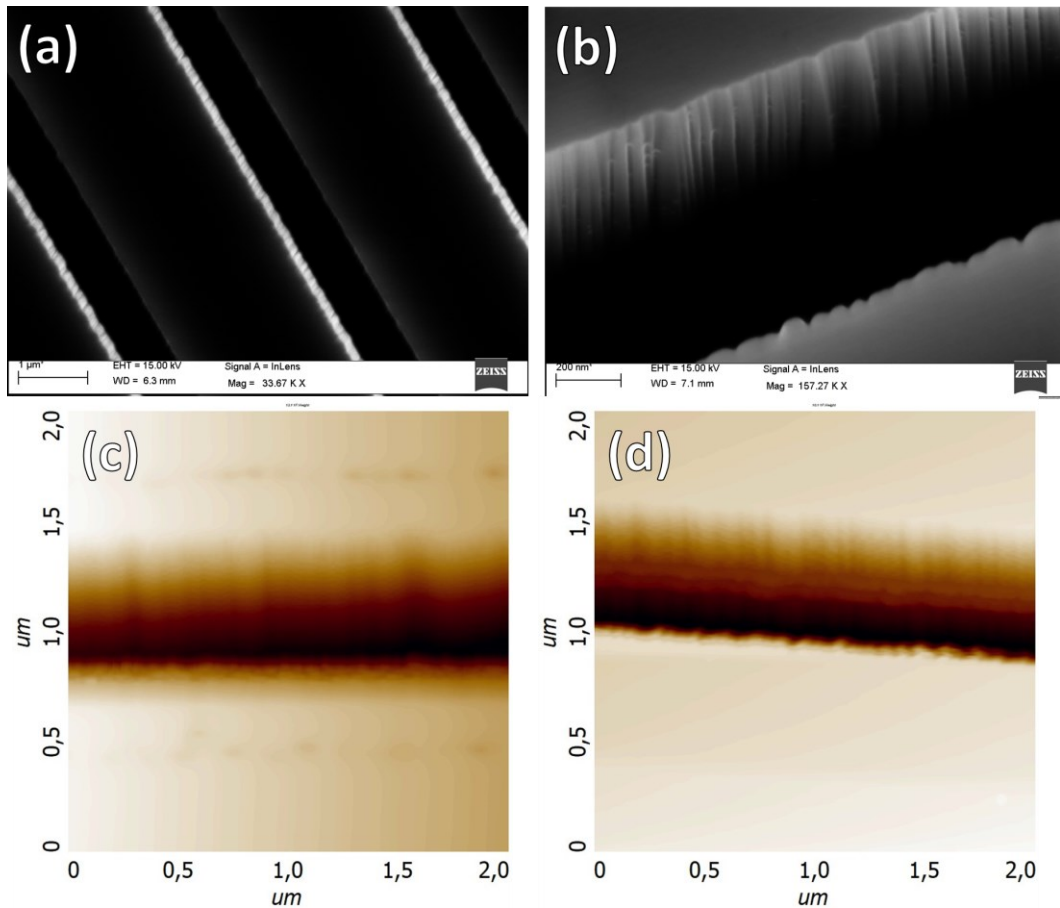


Fig. 5.2 SEM micrographs of a) HMO trench and b) 4H-SiC trench. AFM 2D images of 4 µm^2 acquisition area of a) HMO trench and b) 4H-SiC trench.

As already shown via image analysis in paragraph 4.3, the HMO walls have a 10% lower relative roughness than SiC substrate trenches. The increase of striations density, going from HMO to SiC, has been also uncovered by AFM analysis (Fig. 5.3) and confirms what has been revealed by the image analysis method (see the description of the method in paragraph 4.2.1). The AFM analysis revealed comparable roughness RMS between HMO and SiC trenches walls with 9.52 ± 1.91 nm and 8.91 ± 1.50 nm, respectively. The difference in percentage between HMO and SiC is equal to -6.4% in comparison with the 10% according to the image analysis method (the differences should be considered inside the margin of error).

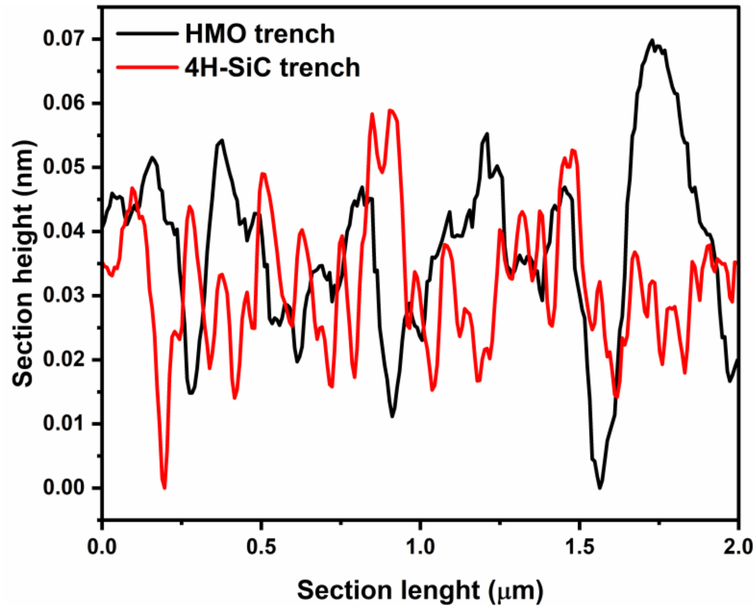


Fig. 5.3 AFM section analysis of HMO (black curve) and 4H-SiC (red curve) trench surface.

Elemental analysis performed by EDX (Tab. 5.1) technique has shown important properties of both HMO and 4H-SiC after the DRIE attack. The percentage of Si and O on both the HMO top and wall surface does not describe the typical stoichiometry of silicon dioxide (SiO_2). Oxygen on 4H-SiC was detected neither on the plane nor on the trench wall surface. On the top side, the mutual percentage of Si and C elements does not respect the stoichiometry 1:1 of SiC, whereas on the trench wall surface a remarkable 100% of Si was detected.

Layer analyzed	Zone analyzed	Si%	C%	O%
HMO	**Trench wall**	63	0	37
	Plane	45.4	0	54.6
4H-SiC	**Trench wall**	100	0	0
	Plane	39.1	60.9	0

Tab. 5.1 Elemental EDX analysis of trench wall and plane on HMO and 4H-SiC after DRIE treatment.

The interesting result can be ascribable to amorphization phenomena during the etching step in DRIE. Amorphous SiC, commonly denoted as “a-SiC”, is more thermodynamically unstable in comparison to its crystalline form, and accordingly, wet chemical etching might be more effective and used as a possible approach to remove striations [158,159]. The presence of silicon moieties on

the trenches wall was furthermore corroborated by XPS analysis: deconvolution of Si 2p photoelectron peaks suggests the presence of a small component at 99.9 eV, as shown in Fig. 5.4a. The Si etch mechanisms and reactions are discussed in paragraph 1.7.

Hence, the etched samples were first dipped in a 5% HF solution for 30 min to remove the thick HMO layer without impacting the Si^0 moieties which are not etched by HF. After this step, the patterned 4H-SiC underwent five etching experiments for a total etching time of 30 min: the experiments were coded by numbers as follows:

1. HNO_3:HF 1:1 V/V at 25 °C
2. HNO_3:HF 1:1 V/V at 45 °C
3. HNO_3:HF:H_2O 1:1:1 V/V at 25 °C
4. HNO_3:HF:H_2O 1:1:1 V/V at 45 °C
5. KOH 3 mol/L at 60 °C

AFM analysis was conducted both before and after each trial and the trenches' roughness values are reported in Tab. 5.2. As previously discussed, the comparison of sidewall roughness moving from HMO to 4H-SiC trenches does not change significantly, with an RMS variation from 9.52 nm to 8.91 nm. This result reinforces the hypothesis of the molding-like transfer from the HMO to 4H-SiC.

Moreover, it was previously demonstrated that the transfer from HMO to 4H-SiC results in an increase in striation density. Thus, it should be noted that the lower roughness of the 4H-SiC relative to HMO implies a reduction in striation heights despite the higher striation degree.

	RMS (nm) ± SD (nm)	**RA (nm) ± SD (nm)**	**Peak-to-Peak (nm) ± SD (nm)**
HMO trench	9.52 ± 1.91	8.28 ± 2.44	41.30 ± 9.55
4H-SiC trench	8.91 ± 1.50	6.92 ± 1.21	51.20 ± 7.64
1	11.75 ± 1.27	9.59 ± 0.83	54.81 ± 7.18
2	10.42 ± 2.76	8.30 ± 2.34	50.72 ± 8.92
3	4.26 ± 0.67	3.62 ± 0.63	18.54 ± 1.75
4	6.70 ± 0.57	5.15 ± 0.52	33.10 ± 1.32
5	12.72 ± 1.57	10.13 ± 1.59	60.60 ± 7.24

Tab. 5.2 AFM analysis of reference samples and wet chemically etched samples.

The etching experiments 1 and 2 were not successful since the average roughness values (RMS and RA) remained almost the same as the 4H-SiC wall trench roughness. Although the study of

silicon etching in the HNO_3/HF solution has been widely investigated, the mechanism is still not fully understood due to the complex chemistry involved. The negative results of wet etch trials 1 and 2 can be imputable for the following reasons:

- The high concentration of both HNO_3 (70 wt%) and HF (48% wt) does not favor the diffusion of byproducts, establishing a rate-limiting step of the process [160].
- The etch rate is independent of HF concentration whereas HNO_3 concentration has a maximum etch rate at 48% V/V because of the aforementioned diffusion limiting step [161].

Experiments number 3 and 4 were set by adding water to the HNO_3:HF mixture with a 33% fraction in volume for each component. Optimization of the solution conditions has significantly improved the recovery of trench walls resulting in a significant reduction of wall roughness, which is equal to 52.2% and 24.8% respectively for experiments 3 and 4. Finally, experiment number 5 with KOH 3 mol/L solution was not effective since no decrement of roughness was detected.

Surface chemical analysis was performed by XPS. The experimental spectra of the Si2p signal have tails and broadening effects which indicate the presence of more than one component inside (Fig. 5.4). Deconvolution of the spectra revealed the presence of the main component, attributed to SiC, in the BE range of 101.2-101.4 eV. To clarify, SiC is detected due to the low lateral resolution of the XPS technique. The X-ray beam spot is not small enough to select only the trenches. The elemental Si component at B.E. 99.9 eV was detected only for pristine and sample etched by using the experimental conditions n.3. To note, etching at a temperature of 25 °C with the HNO_3:HF 1:1 V/V solution is not sufficient to completely remove the Si layer from the trenches (Fig. 5.4b). By increasing the temperature to 45 °C, the Si^0 component disappears (Fig. 5.4c) thus indicating the complete removal of the elemental silicon layer. The presence of HNO_3 leads to the formation of stoichiometric SiO_2 on both the samples of experiments 3 and 4 with a component at B.E. 103.2 eV. The SiO_x component at 102 eV is common in all the analyzed samples.

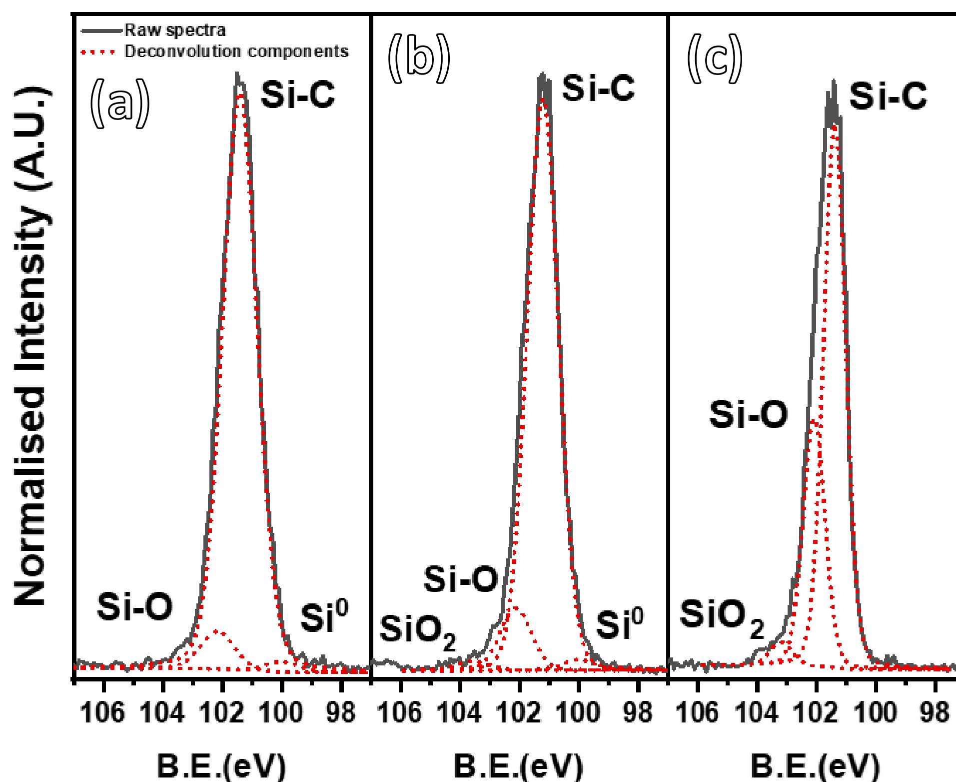


Fig. 5.4 XPS Si2p deconvoluted spectra of a) 4H-SiC reference, b) 4H-SiC experiment 3 (25 °C), and c) 4H-SiC experiment 4 (45 °C) samples.

The amorphization phenomena after DRIE and the following recovery in the HNO_3 and HF solution had some effects on wall roughness reduction. Despite the high percentage of roughness decrement, it would be preferable to obtain a perfectly flat wall surface with roughness RMS values of the order of the angstrom. The 4H-SiC on the Si-face (0001) roughness is attested to be around 0.1/0.2 nm. The presence of striations even after the disappearing of the Si^0 signal implies that only a superficial portion of them is made of Si at the zero-state. The remaining part is made of SiC which is impossible to etch by traditional wet chemical etching approaches. The reasons behind the chemical inertia of SiC are discussed in paragraph 1.7.

5.4. Conclusions

The Wet Chemical Etching (WCE) approach was effective in trench wall roughness lessening. The optimization of the HNO_3/HF solution diluted with H_2O allows to etch the elemental Si fraction detected on the walls by EDX and XPS analysis. In particular, the WCE in HNO_3:HF:H_2O 1:1:1 solution at 25 °C led to a roughness reduction of 52.2%. The roughness was measured by AFM. Despite the interesting result, the measured wall roughness after etching (3-6 nm) by comparison

with the typical surface roughness of 4H-SiC (few angstroms) is not sufficient to avoid device electrical issues.

The silicon sublimation/amorphization of the supposed thin layer detected by EDX and XPS analysis could be a springboard for physical and chemical approaches combination of SiC etching. The findings could interest applicability where a thin layer of material should be finely etched. The present work served also to demonstrate the impossibility of 4H-SiC etch using standard etch solution as nitric/fluoric acid which by counterpart is effective for Si. It has been demonstrated the elimination of the Si moieties by XPS analysis while the 4H-SiC was not affected by the traditional wet chemical etching as demonstrated by AFM analysis.

6. MACE Mediated Trench Recovery

6.1. Introduction

The high chemical stability of 4H-SiC indicates that it may not be possible to etch it using standard wet chemical etching solutions. Herein, it was employed a novel method of etching with the aim of reducing the striations on trench walls and examining the behavior over 4H-SiC. The proposed etching technique is called Metal Assisted Chemical Etching (MACE). It can also be referred to as Metal Assisted Photo-Chemical Etching (MAPCE). This study aims to investigate the fundamentals of MACE on 4H-SiC. The amount of scientific research on the MACE technique on SiC is currently limited and many behavior clarifications occur. Moreover, the MACE method was utilized for 4H-SiC trench samples with the objective of minimizing the number of striations on the walls. Various system parameters were manipulated to attain increasingly improved outcomes.

The classic wet chemical etching approach suffers from isotropic etching, making it unsuitable for semiconductor microstructure fabrications. The MACE approach enables the selective etching of specific areas of a surface and even produces high-aspect-ratio structures [162,163]. The etching mechanism will be explained below.

The MACE process could be split into 4 principal components:

- Noble metal (Au, Pt, Pd)
- Light source (UV lamp or solar lamps)
- Oxidant agent (H_2O_2, $K_2S_2O_8$)
- Etching agent (HF)

This etching technique is highly versatile since it is possible to change or modulate one or more components to obtain different results. It was also employed in patterned systems as reported in the scientific literature [164,165]. In fact, the method could find applications in the fabrication of Micro-Electro-Mechanical Systems (MEMS), in microelectronics, in solar cells [166,167], and in the realization of nanostructures [168,169].

The scheme in Fig. 6.1 displays the different stages of a MACE process. Stage 1 of Fig. 6.1 involves material irradiation in order to promote the electrons to a higher energy level state. The electrons migrate through the noble metal (Fig. 6.1 stage 2) to reach the boundary with the solution. The oxidant is reduced and the electrons are taken away from the sample (Fig. 6.1 stage 3). The holes remaining in the sample induce a process of surface oxidation. The formed oxide is finally etched with the HF (Fig. 6.1 stage 4).

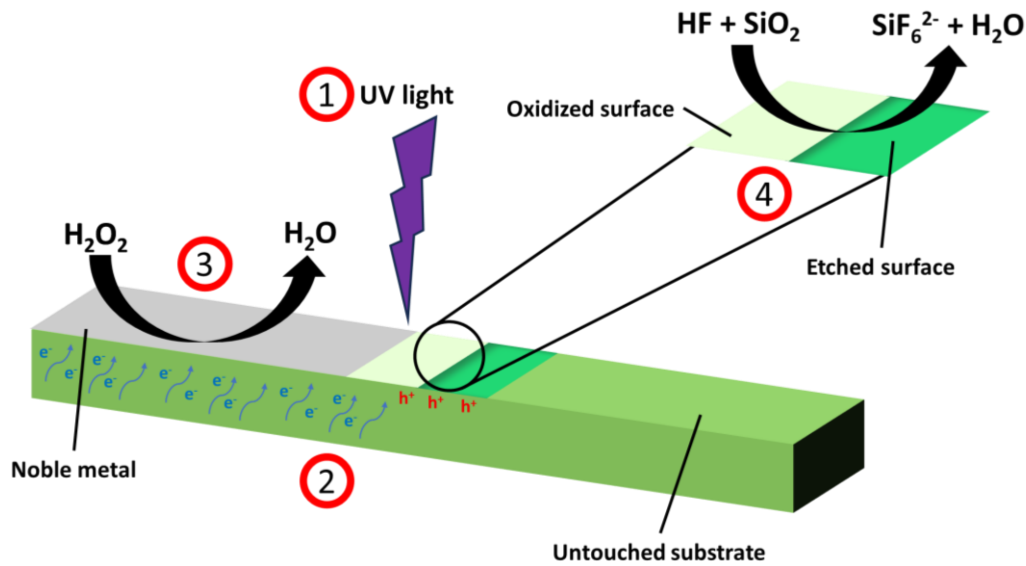
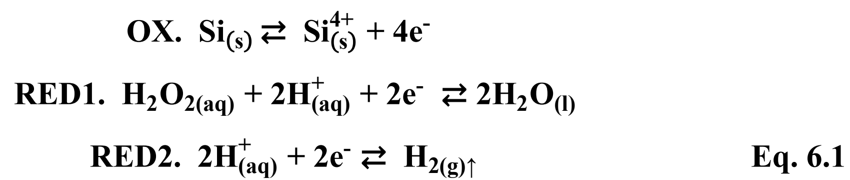


Fig. 6.1 Schematization of a MACE process.

The light source must have as high an intensity as possible, but most importantly, its energy must match the semiconductor band gap, commonly indicated as Eg. Note that the energy required is strongly affected by the presence or the type of dopants in the semiconductor. The electrons in the semiconductor promoted in the conduction band participate in the redox reactions between the semiconductor and the oxidant agents as in Eq. 6.1. The electrons should travel through the noble metal to reach the oxidant. For this reason, it is of the utmost importance to have good Schottky contact. It is the contact between a metal (conductor) and a semiconductor. By keeping fixed the metal, the Schottky contact could be enhanced by annealing treatments.

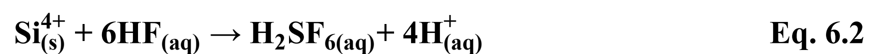


$$\textbf{OX.}\;\; Si_{(s)} \rightleftarrows Si^{4+}_{(s)} + 4e^-$$

$$\textbf{RED1.}\;\; H_2O_{2(aq)} + 2H^+_{(aq)} + 2e^- \rightleftarrows 2H_2O_{(l)}$$

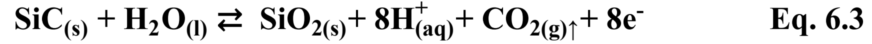
$$\textbf{RED2.}\;\; 2H^+_{(aq)} + 2e^- \rightleftarrows H_{2(g)\uparrow} \qquad \textbf{Eq. 6.1}$$

The H_2O_2 (or other oxidants) molecules and protons (H^+) take part in the reduction semireactions at the metal/semiconductor interface, whereas the Si passes in the oxidated state. The main role of the metal is to reduce the reduction energy required. The Si^{4+} on the surface (which is why is indicated in the solid-state) is readily dissolved after the HF attack in the form of H_2SiF_6 as displayed in Eq. 6.2.



$$Si^{4+}_{(s)} + 6HF_{(aq)} \rightarrow H_2SF_{6(aq)} + 4H^+_{(aq)} \qquad \textbf{Eq. 6.2}$$

The MACE is a suitable method to etch most of the semiconductors. The method works well on etchable materials such as Si [163,170,171], Ge [172], and GaAs [173]. The following redox reaction (Eq. 6.3) shows the way the SiC is oxidized during the MACE process:



$$\mathbf{SiC_{(s)} + H_2O_{(l)} \rightleftarrows SiO_{2(s)} + 8H^+_{(aq)} + CO_{2(g)\uparrow} + 8e^-} \qquad \textbf{Eq. 6.3}$$

The MACE method guarantees an anisotropic etching process because the redox reactions occur only at the metal/semiconductor interface. In the field of catalytical chemistry is well established that noble metals such as palladium (Pd) and (Pt) are more active than others such as Au and Ag. This is the reason why the goodness of the metal catalytical activity is one of the most important features of the MACE method. On the other hand, cheaper metals make the MACE a more viable electroless wet chemical etching method. At first, the semiconductor is etched, the noble metal sinks and the process continues until all the oxidant agent is consumed. Therefore, nanostructures can be produced on porous etched materials, for example, nanowires [174,175] or nanocolumn [176]. In the present work, some experimental attempts over 4H-SiC samples have been conducted adopting gold (Au) as a catalyst metal, despite the lower catalytical activity than Pd and Pt. The experiments in this study utilized also Pt metals, as suggested by the scientific literature [177,178].

6.2. Materials and Methods

The diced samples adopted in this study come from a 4H-SiC 8° off-axis 6-inch wafer. The face that has been taken under investigation is the Si-face. A 4H-SiC wafer comprehending the trenches was cut and employed in the study. Si samples were used with the aim of having a reference and evaluating the effect of the etching process. Pieces of about 4 cm^2 large area were obtained by diamond cut or sawing.

Aliquots of HF (48 wt%, M_w=20.1 g/mol, d=0.97 g/cm^3) stock solution were drawn toward a final concentration of 1.5 M in the reaction solution. H_2O_2 (30 wt%, M_w=34.01 g/mol, d=1.11 g/cm^3) stock solution stored in the fridge was drawn to reach solution concentrations between 0.15 and 0.30 M. After every treatment, the samples were rinsed and dried under N_2 flux. All work and washing solutions were prepared by using ultrapure water (18.2 MΩ cm, TOC 1 pbm) from *Elga Veolia PURELAB Flex 3* system.

The Au deposition was achieved by plasma deposition instrument (*EMITECH K450X*) adjusting the voltage according to a 40 mA current for 3 min. The deposition chamber was held under vacuum at $1\cdot10^{-3}$ atm and filled with Ar gas reaching a final pressure of $6\cdot10^{-2}$ atm. The Ag

nanoparticles were dispersed in water, and successively they were deposited by drop-casting. The drop was let to evaporate in atmospheric conditions.

The MACE process was conducted by mixing HF and H_2O_2 in a Teflon beaker in the fume hood. The processing time went from 15 min to 30 min. The system irradiation was achieved under a solar lamp (*Osram Ultra Vitalux 300 W E27*). The solar lamp offers different wavelengths in the visible and in the UV region. The distance between the lamp and the sample was kept at a fixed distance of about 15 cm. The solutions were not maintained under stirring. Following experiments with Pt metal deposition were performed with a UV lamp (*Loctite UVALOC 97039*) maintaining the distance between the UV source and the sample of about 5 cm, with a nominal power density of 115 mW/cm^2.

The metallic deposition on 4H-SiC of Ti and Pt metals was achieved by an e-Gun Physical Vapor Deposition (*Plassys MEB 550 S*) instrument. The loadlock and the chamber pressure were respectively kept at $1 \cdot 10^{-6}$ and $1 \cdot 10^{-7}$ mbar. An Ar sputtering for 1 min at mid-energy was added in the deposition process flow to remove eventual atmospheric contamination from the surface. The deposition of metals was done under an electron emission gun at 240 mA modulating the deposition rate 0.05 nm/s. The final thickness was set depending on the experiment. The metal deposition was done after an HF 5 wt% etch for 2 min.

Annealing of Pt metallic layers was performed via RTA instrumentation (*AS-One, Annealsys*). The annealing was done in an inert Ar flow atmosphere with a flow of 40 L/h. The heating ramp was set at 10 °C/s up to 600 °C and increased to 20 °C/s up to a final temperature of 1050 °C that was kept for 2 min.

6.3. Results and Discussions

6.3.1. Au Metallization

The first attempt of the MACE approach has been conducted by employing Au as a catalyst metal. This noble metal is effective for the Si material whilst results on 4H-SiC are not reported. The MACE process, firstly tested on Si by preparing a solution of HF 1.5 M and H_2O_2 0.15 M, was activated by irradiating with the solar lamp (*Osram Ultra Vitalux 300 W E27*) for 30 min. A certain degree of etching is visible even outside the mask region (SEM in Fig. 6.2a) which is due to the reactivity of Si towards H_2O_2/HF solution. The well-defined interface shown in the SEM micrograph of Fig. 6.2b displays two regions characterized by different surface morphologies due to different etching mechanisms. A microporous surface is observable after the etching below the Au mask region, as shown in Fig. 6.2c: the micrometric features up to the surface, highlighted in the red solid circle of Fig. 6.2c, are attributed to wrapped Au foils formed during the process. On the

surface of the micrometric voids, understructures can be seen in the SEM micrograph as well as in the AFM image of Fig. 6.2d. The AFM analysis (*NT-MDT* modular *AFM NTEGRA*) revealed an average roughness of 83.4 nm, which is largely higher than the roughness values of the sample out of the Au mask region of 6.1 nm.

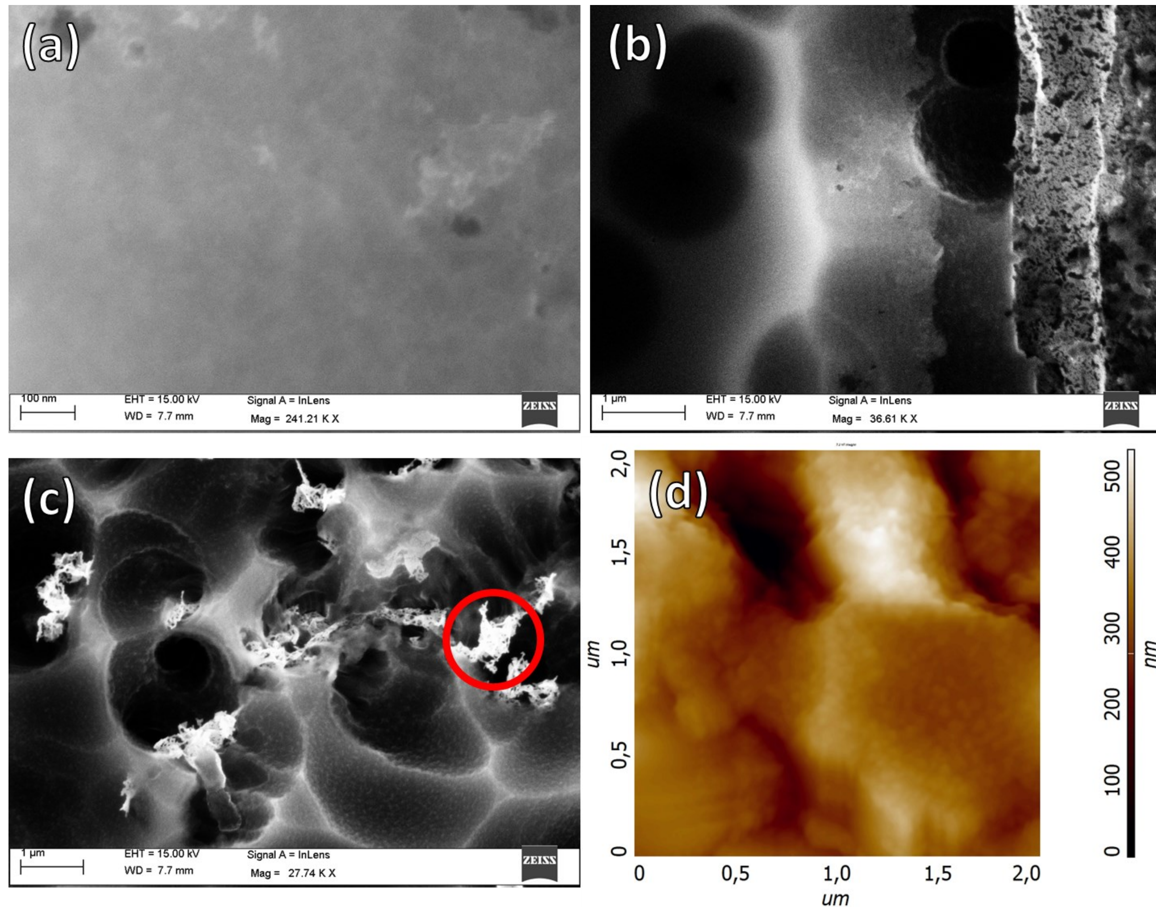


Fig. 6.2 MACE on undoped Si substrate, HF 1.5 M + H_2O_2 0.15 M under solar lamp 30 min. SEM micrographs of a) uncovered region, b) interface region, c) Au-covered region with a red circle highlighting Au foils, and d) AFM 2D height image of the Au-covered region.

This first experiment confirms that Si material is promptly etched in an H_2O_2/HF mixture using Au as a noble metal. The result falls in the high reactivity of the Si surface and the easiness of manipulation by wet chemical methods.

The same behavior is not remarked by 4H-SiC which results will be presented as follows. The 4H-SiC underwent a MACE treatment in a solution of HF 1.5 M and H_2O_2 0.30 M under a solar lamp (*Osram Ultra Vitalux 300 W E27*) for 1 h. The Au layer remained attached to the surface as displayed in Fig. 6.3a. The typical Au-deposited morphology was reported in [179]. The Au layer was eliminated by dipping the sample in aqua regia. The underneath SiC surface appears flat as shown in Fig. 6.3b. More closely AFM analysis returned a RMS value of 0.76 nm (AFM 2D height

image in Fig. 6.3c) slightly higher than the surface roughness of the pristine 4H-SiC sample that has a RMS of 0.35 nm.

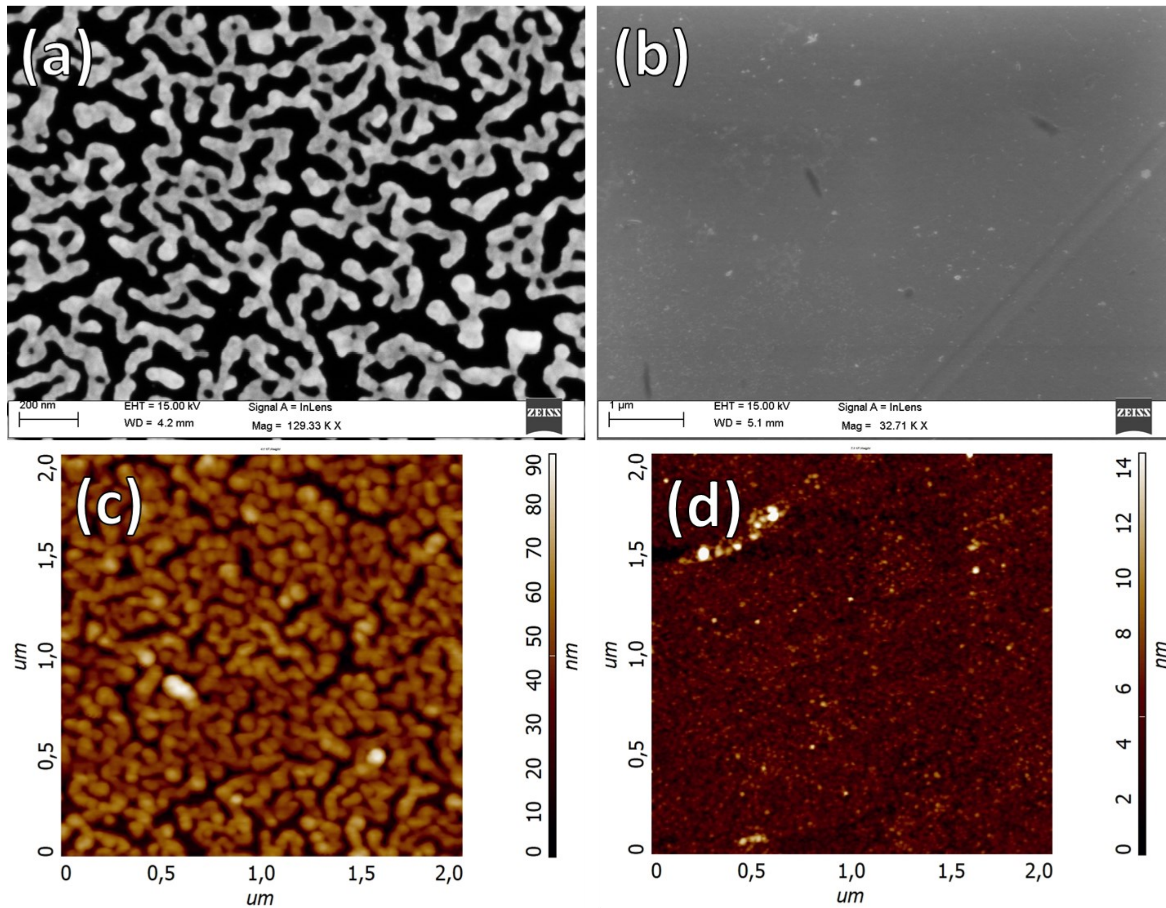


Fig. 6.3 Effects of 4H-SiC after Au-assisted chemical etching (HF 1.5 M + H_2O_2 0.30 M under solar lamp 1 h): SEM micrographs of a) Au mask area, b) after aqua regia cleaning, and AFM 2D height images of c) Au mask area, d) after aqua regia cleaning.

The slight increase in roughness might be due to surface contamination. This result confirms that the Au noble metal is not suitable for MACE on 4H-SiC. The Au film is not a sufficiently powerful catalyst to promote the oxidation of SiC and the reduction of the H_2O_2. The Pt metal is, thus, the best candidate to perform a successful MACE on SiC as shown in the next paragraph.

6.3.2. Pt Metallization Without Annealing

The Au metallization is unhelpful for MACE application on SiC. The scientific community reports that Pt is the only “viable” metal able to properly work on SiC. A first set of experiments was done by depositing a thin layer of 10 nm of Pt by evaporation (*Plassys MEB 550 S*). No annealing was deliberately performed after the metal deposition in this first experimental set: note the absence of annealing does not ensure good electric contact between the substrate and the

metallic layer. A two-level DOE was set by varying the concentration of H_2O_2 as oxidant and HF as etchant as shown in Tab. 6.1.

	C_{H2O2} (mol/L)	C_{HF} (mol/L)	H_2O_2/HF	Time (min)	Surface RMS (nm)	Surface RA (nm)	Trench RA (nm)
SiC MACE 1.1	1	0.5	2.0	30	2.0 ± 0.1	1.5 ± 0.1	1.8 ± 0.5
SiC MACE 1.2	5	0.5	10.0	30	2.1 ± 0.3	1.6 ± 0.2	2.7 ± 0.7
SiC MACE 1.3	1	1.5	0.7	30	2.2 ± 0.4	1.7 ± 0.3	2.1 ± 0.4
SiC MACE 1.4	5	1.5	3.3	30	2.2 ± 0.1	1.8 ± 0.1	0.7 ± 0.2
SiC MACE 1.5	5	1.5	3.3	90	2.5 ± 0.1	2.0 ± 0.1	2.1 ± 0.3

Tab. 6.1 Experimental table of MACE on Pt covered 4H-SiC samples without annealing treatments. AFM surface and image analysis trench roughness are attached to the table.

The UV irradiation was performed with a *Loctite UVALOC 97039* UV polymer curing lamp, heating it 15 min prior to starting the first experiment. The molar concentrations of H_2O_2 are 1 and 5 mol/L whereas the HF concentration was set at 0.5 or 1.5 mol/L values. Since the oxidation/etchant ratio is a key parameter of MACE, the value is reported in the table. The time is fixed at 30 min at the exception of the fifth experiment where the time was extended to 90 min remarking the same solution of the fourth experiment. The RMS and RA values are reported in the right part of Tab. 6.1. The roughness parameters were measured by AFM (*NT-MDT modular AFM NTEGRA*), whereas the trench RA was measured by image analysis method (see paragraph 4.2.1) out of SEM micrographs (*Jeol JSM-7900F* and *Zeiss SUPRA-55 VP*) presented in Fig. 6.4.

The early experiments revealed that the surface roughness does not depend on the adopted concentrations within the tested range. The roughness increase was expected due to the rise in sample opacity visible to the naked eye. The effect occurred in the zone not covered by Pt. The metal acts as a barrier to protect the underneath 4H-SiC from eventual etch. The metal protection potentiality in MACE was exploited in the realization of complex structures mediated by nano soft lithography [180]. The increase in opacity may have potential applications in wafer handling, as

detailed in paragraph 6.3.4. Although the metallic film was not annealed, micrographs in Fig. 6.4b and Fig. 6.4e reveal a slight etch on the top.

The modification of the trench followed a different route. The striations along the wall of the trench are visible in the reference sample from tilting view SEM micrographs (Fig. 6.4a). Following the MACE procedures, roughening of the wall surface is evident in all the treated samples. A high magnification inset has been added to Fig. 6.4b with the aim of appreciating the roughening effects. Through the image analysis method, previously described in paragraph 4.2.1, it was possible to estimate an average roughness of about 2 - 2.7 nm as reported in Tab. 6.1.

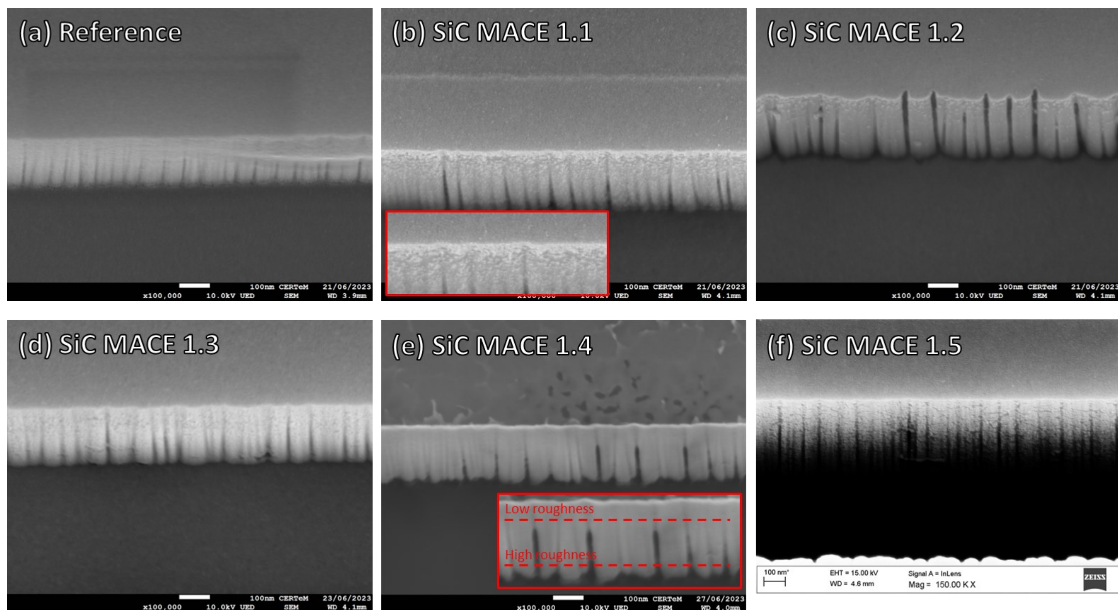


Fig. 6.4 SiC MACE 1 SEM micrographs of a) reference, b) SiC MACE 1.1, c) SiC MACE 1.2, d) SiC MACE 1.3, e) SiC MACE 1.4, and f) SiC MACE 1.5 samples. In b) and e) the inset displays the trench wall at higher magnification. The inset in e) highlights the low and high roughness areas of the trench.

Among the treated samples, SiC MACE 1.4 (Fig. 6.4e) shows the most evident trench striation lessening. The trenches appear less rounded and more flattened after the treatment with an assessed roughness of 0.7 nm: this value takes into consideration the roughness all along the trenches. An analysis performed only at the top of the trench revealed an average roughness of 0.3 ± 0.2 nm which is close to the target (see the inset of Fig. 6.4e), but unfortunately, some voids are still visible on the lower part of the wall. The SiC MACE 1.5 experiment replicated the previous experiment by increasing the etching time to 90 min, but these experimental conditions did not result in any significant improvement in the trench quality.

Adding up some important information regarding the behavior of MACE, the same experiments were conducted adopting a 365 nm *Black-RayB-100 A* lamp without any success. The unsuccessful results could be attributed to the doping of the samples adopted in these experiments. The photon energy associated with a wavelength of 365 nm is equal to 3.40 eV, which is slightly higher than the 4H-SiC energy band gap of 3.23 eV. Hence, in principle one may assume the perfect suitability of the 365 nm lamp for the purpose. The doping of a semiconductor results in a decrease in electron transition energy, allowing photons with higher wavelengths (lower energy) to resonate with them. In this scenario, it is more advantageous to utilize UV lamps with a wider emission spectrum.

In conclusion of this first section, despite the lack of annealing after the metal deposition, a faint 4H-SiC etching is observable. However, the subsequent section will cover the outcomes of annealed samples.

6.3.3. Pt Metallization With Annealing

The annealing is mandatory to reduce the Schottky contact between the 4H-SiC and the metal [181–183]. In particular, a high temperature should be reached in the case of Pt metal by virtue of the high melting temperature. In the present section, samples of 4H-SiC with 10 nm of Pt coverage were annealed at 1050 °C for a short time by RTA (*AS-One, Annealsys*) technique. The H_2O_2 and HF concentrations and the etching time (Tab. 6.2) had not changed since the first set of experiments (Tab. 6.1).

The surface RMS and RA values are respectively around 3 and 2 nm respectively. Accordingly, the SiC MACE 2 experiments show the same behavior as the SiC MACE 1 experiments in terms of surface roughness. The main difference is the slightly higher roughness compared to the SiC MACE 1 samples. These results support the notion that the annealing improves the etching performance in MACE, as previously discussed. This suggests the potential to further adjust the etching efficiency of MACE through the modulation of metal/semiconductor electric contacts.

	C_{H2O2} (mol/L)	C_{HF} (mol/L)	H_2O_2/HF	Time (min)	Surface RMS (nm)	Surface RA (nm)	Trench RA (nm)
SiC MACE 2.1	1	0.5	2.0	30	3.2 ± 0.3	2.6 ± 0.2	NA
SiC MACE 2.2	5	0.5	10.0	30	2.6 ± 0.6	2.0 ± 0.5	4.3 ± 1.3
SiC MACE 2.3	1	1.5	0.7	30	2.6 ± 0.4	2.0 ± 0.3	NA
SiC MACE 2.4	5	1.5	3.3	30	2.8 ± 0.2	2.0 ± 0.1	1.1 ± 0.3

Tab. 6.2 Experimental table of MACE on Pt covered 4H-SiC samples with annealing treatments. AFM roughness data and trench RA by image analysis method are attached to the table.

To corroborate the findings, the RA of the trench, determined by analyzing the images, was quantifiable for solely SiC MACE 2.2 and 2.4 samples. This is due to the fact that the trenches in samples SiC MACE 2.1 and 2.3 were nearly entirely etched, which is visible in Fig. 6.5a and Fig. 6.5c, respectively. The SEM micrograph in Fig. 6.5d visually confirms the decrement of the trench roughness of the SiC MACE 2.4 sample as reported in Tab. 6.2. The AFM images of SiC MACE 2.4 sample in Fig. 6.5e and Fig. 6.5f reveals the step at the upper edge of the trenches as visible also in the SEM micrograph in Fig. 6.5d.

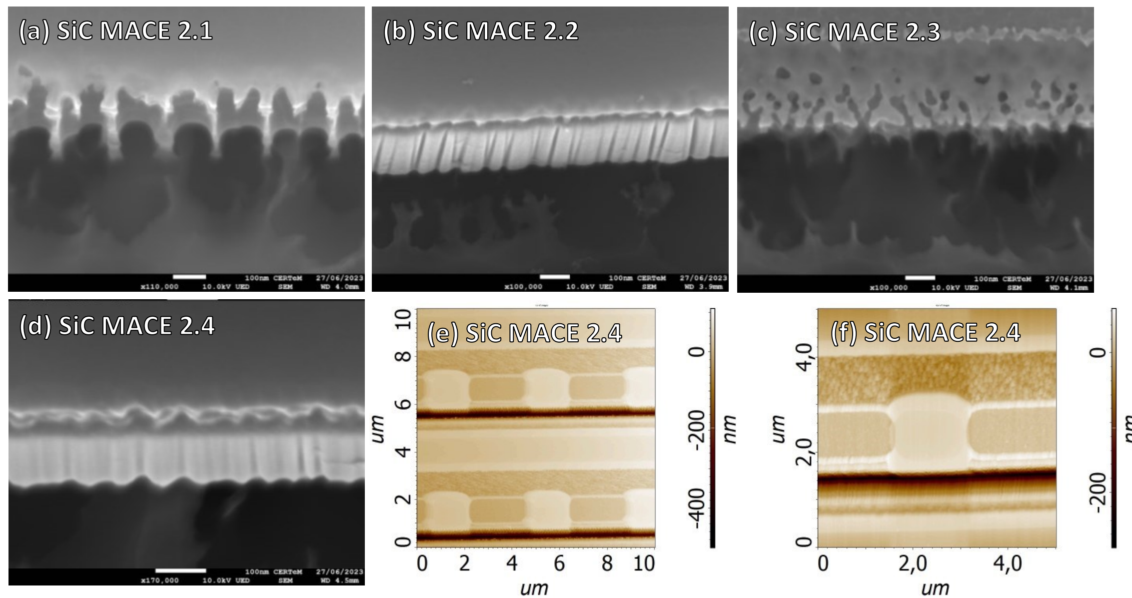


Fig. 6.5 SiC MACE 2 SEM micrographs of a) SiC MACE 2.1, b) SiC MACE 2.2, c) SiC MACE 2.3, and d) SiC MACE 2.4 samples. AFM images of SiC MACE 2.4 samples from e) 100 μm^2 and f) 25 μm^2 acquisition areas.

Herein, the H_2O_2 concentrations seem to play a major role in the trench etching efficiency and selectivity. The lower oxidant concentration seems to enhance the etch selectivity towards the trenches whereas higher oxidant concentration drastically reduces it. The higher oxidation power at higher concentration could quickly detach the trenches from the bottom causing the elimination of the electric contact. The MACE mechanism involves the electron recruitment to the top and their transfer to the oxidant. If the electrons find some constraints (high resistivity, electrical interruption, material interruption) can not reach the surface and the MACE process stops. The findings demonstrate that the parameter control in MACE is of utmost importance. Despite the good roughness value obtained for the SiC MACE 1.4 sample of the previous experimental set, the striations are still visible and it is also possible to observe the etching of the material on the bottom (Fig. 3.1a-d) and on the top part (Fig. 3.1e-f) of the trenches. The direct application of MACE as a method to recover the quality of the trenches should require some protective layer that could ensure the absence of etch in the undesired zones.

6.3.4. Applications of Substrate Roughening and Opacification

It was previously stated that the MACE process attacked along the uncovered spots. The MACE is an isotropic etching approach. However, patterning can assist in protecting sensitive zones of the material. The surface roughening obtained under UV irradiation in H_2O_2 5 M and HF 1.5 M for 30 min (SiC MACE 2.4) is clearly visible in the SEM micrograph of Fig. 6.6a which is a well-known

morphology aspect on 4H-SiC [184]. It was detected a RMS value of 13 nm with a maximum height of 54 nm, hence a conspicuous surface roughening occurred. Despite eventual system divergences, the measured roughness value of 13 nm is close to the 9 nm detected by Liu and coworkers after the same time of etch [185]. The AFM image shows that the roughening occurs homogeneously onto the doped area as displayed in Fig. 6.6b. The correlated section discovered the presence of nanometric length valleys (one located around 2.5 μm in Fig. 6.6c), which contribute to the 54 nm Peak-to-Peak measurement.

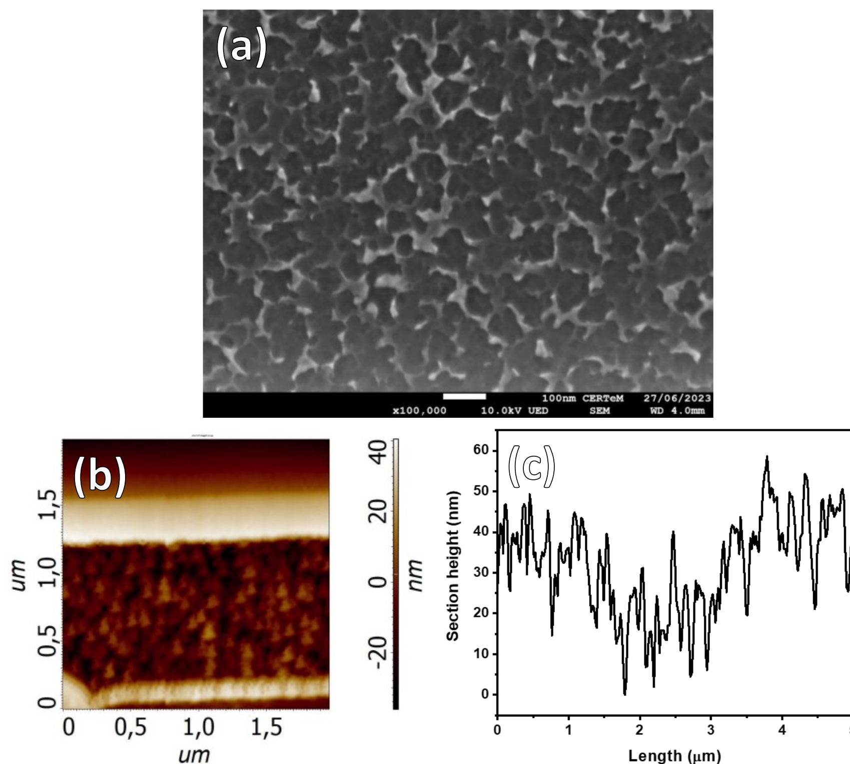


Fig. 6.6 Surface morphological analysis of SiC MACE 2.4 sample: a) SEM micrograph, b) AFM 2D height image, and c) correlated height section.

Research into the use of porous and rough SiC has led to potential applications in liquid and gas separation [186], catalysis [187], and other fields. For instance, in the microelectronic manufacturing industry, the instruments operate by clamping and moving the wafers, and these operations, which are performed hundreds of times each day, require perfect wafer pre-alignment. In fact, a faulty alignment could cause the stop of the machine in the best scenario or even worse the destruction of the wafer. The wafer position and recognition are accomplished by the Charge Coupled Device (CCD) transmission sensor, which generally works with low-intensity light in the green portion of the visible spectra (500-570 nm). The wafer alignment is specifically achieved by the optical recognition of the notch [188,189], a flat zone in the corner of the wafer. The alignment

problems occur especially in the first steps of the devices' manufacturing or when thin wafers are employed [190].

The MACE treatment on 4H-SiC leads to the increase of roughness with the subsequent increase of opacity, as evidenced in Fig. 6.7a, where the MACE-treated area has a characteristic white/gray color. Surprisingly, the MACE had effects inside the 1 mm wide zone not covered by the Pt. The finding suggests that the electrons' recruitment and the Pt catalysis effects occur even at relatively high distances from the noble metal. To note how the catalysis phenomena generally have short extinction time and low mean free paths. Outside, the Pt-covered zone does not present any increased opacity due to the absence of etch. The patterning of large areas has a different behavior compared with small ones. When employing nanoparticles, the etch occurs solely at the interface metal/semiconductor [191,192]. The result is that the nanoparticles settle, allowing for a subsequent cycle of catalysis/etching to occur at a greater depth, producing a mesoporous material. The findings indicate that utilizing the metal itself as a protective layer for patterning may be a viable alternative to the resource-demanding and time-consuming deposition of hard mask oxides.

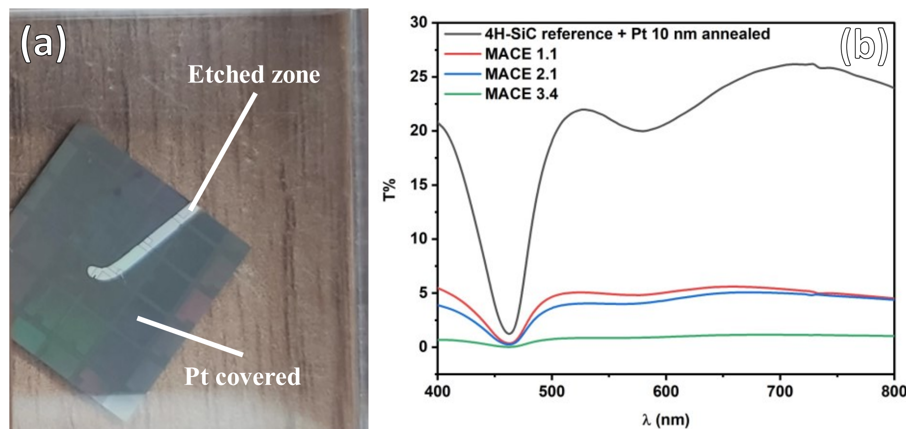


Fig. 6.7 a) Photograph of 4H-SiC sample with trenches after MACE treatment and b) UV-Vis transmittance spectra of 4H-SiC trench pristine (gray curve), SiC MACE 1.1 (red curve), SiC MACE 2.1 (blue curve), and SiC MACE 3.4 (green curve) samples.

To further confirm the increase of opacity, a spectroscopic evaluation of the transparency was made by the UV-Vis spectroscopy technique. The spectrum in Fig. 6.7b shows the transmittance (T%) values in the wavelength range between 400 and 800 nm. The 4H-SiC reference sample is distinguished by the higher transmittance values in all the analysis ranges. A decrease in transmittance is the result of an increase in opacity due to reflection or scattering phenomena. Taking into account the transmittance value at 550 nm, the metalized 4H-SiC trench reference sample has a T% value of 21%. The MACE process in SiC MACE 1.1 and SiC MACE 2.1 samples

results in the decrease of T% at 5% value. Further decrease of transmittance is observed for the sample SiC MACE 3.4 with a detected value of 1%.

The surface and optical modification of a few nanometers could be performed on the C-face (generally the back of the wafer). The slight, but optically effective modification gives a strong response in terms of transmission reduction and possibly the overcoming of the misalignment problems that occur during device manufacturing.

6.4. Conclusions

MACE experiments were conducted on both Si and SiC samples revealing the effectiveness of adopting Au and Pt metals for the two semiconductors, respectively. For Silicon MACE Au is effective in activating the process, but, conversely, it has been demonstrated the absolute necessity of adopting Pt metal to perform MACE on 4H-SiC.

The MACE approach could be finely tuned by varying the metal thickness, the light exposure, the solution composition, and many other parameters. For the current investigation, a 10 nm thick layer of Pt was deposited onto 4H-SiC. Two series of experiments were done without and with annealing. Annealing primarily reduces the Schottky barrier and enables the electron flow from the semiconductor to the metal.

The morphological variations of SiC samples (flat and patterned) were investigated: in particular, the roughness on the top of the samples was measured by the AFM technique whilst the roughness of the trench walls was estimated by SEM micrographs (tilted analysis) coupled with the image analysis method. The best result in terms of the trench wall's flattening was achieved using the experimental conditions of SiC MACE 1.4. The lateral roughness of 0.7 nm was obtained in a solution of H_2O_2 and HF respectively 5 and 1.5 mol/L for 30 min. However, the presence of residual striations at the bottom of the walls is still detected.

The second experimental set was outdone by annealing the Pt metal film at 1050 °C after deposition: this thermal treatment had the effect of enhancing the MACE process, but in some cases, it completely disrupted the DRIE fabricated trenches. The solution concentration used for SiC MACE 1.4 leads to the best results in terms of lateral roughness flattening, nevertheless, the value of 1.1 nm is slightly higher than that obtained for the SiC MACE 1.4 sample (0.7 nm). In both cases, the atomical flatness of 4H-SiC (RMS 0.2 nm) was not reached.

The MACE on 4H-SiC could be employed for polishing and fine etch purposes under metallization without annealing. Additional potential applications of MACE were investigated. The increase in surface roughness was demonstrated and it could be a possible application in many fields, from catalysis to photovoltaics. The increase in sample opacity could be useful for the wafer

handling issues of 4H-SiC which is managed by optical sensors built in the instrumentations. Defined structures and morphologies of 4H-SiC can also be achieved by combining the MACE technique with other methods, as previously studied [185,193,194].

In conclusion, the MACE technique could be easily scalable regardless of its intended use due to easy setup. The only necessary equipment to perform MACE is a chemical bath and an illumination system. The combination of promising preliminary research findings and the potential for upscaling etching systems could result in the MACE technique becoming a widely adopted method in the semiconductor industry.

7. Electropolishing

7.1. Introduction

Electrochemical etching (ECE) is the final wet chemical approach investigated in this doctoral dissertation. This chapter will focus on the use of the technique to perform electropolishing. It can be described as the ECE practice with the aim of achieving the flattest possible surface. This approach has been previously studied on silicon [195,196] and to a lesser extent on other SiC polytypes [197], although the underlying mechanism of 4H-SiC remains partially unknown due to a lack of scientific contributions. Following, this section provides a concise overview of the ECE technique.

The ECE is fundamentally an electrolytic process. It starts with an electric stimulus applied to the material. In other words, a voltage is applied with the consecutive extraction of electrons from the material. The sample constitutes the anode of the electrolytic cell since it is interested in the oxidative process. In fact, the ECE is applicable only to conductive materials. The electrons are stripped from the material causing surface oxidation (anodic oxidation). The oxide is then removed thanks to the presence of an opportune etchant. For Si and SiC the SiO_2 or substoichiometric oxides are easily etched in concentrated or diluted HF solution.

It is possible to conduct ECE experiments through potentiostatic or galvanostatic modes, by fixing the potential or the current respectively. In this doctoral thesis, the galvanostatic mode was employed for the experiments. In this mode, the voltage variation over time is observed to keep the current at a fixed value. The ECE experiments are affected by the material to be etched, the composition of the solution, the electrical parameters, and in some cases by the irradiation light employed. Even by fixing the material, the face exposed to the etching solution plays a major role.

Talking about the 4H-SiC, the material is characterized by two different faces, namely Si-face and C-face. In chapter 8, different morphologies of the etched material were obtained starting from the two different faces. Other sample characteristics that influence the ECE results are the doping type [198–200] and the doping level [198,200]. Therefore, by fixing the material features, the other parameters of the system can be adjusted to obtain different results. For this reason, the ECE approach is highly adaptable and applicable in numerous fields requiring the fabrication of porous membranes and microstructures.

In this doctoral thesis, the ECE technique was employed for microelectronics and other possible applications. This section will cover the use of ECE to perform electropolishing with the aim of providing a hint for possible microelectronic purposes. This experimental chapter focuses on the investigation of the main ECE parameters on highly n-doped 4H-SiC samples, considering only the

Si-face. Both high and low currents were used in the experiments. The solution composition was modified with the aim of obtaining interesting results. Chapter 8 will exclusively showcase the use of the electrochemical technique to produce porous particles that have potential applications in various fields.

7.2. Materials and Methods

ECE experiments were performed in a hand-crafted cuve whose layout is shown in Fig. 7.1. The sample of 4 cm^2 was faced toward the hole, in contact with the etching solution. At the bottom of the sample, a copper metal plate is put to create electrical contact with the source power system through alligator contacts. The system was capped and tightly secured with screws. The solution was filled from the top with a volume of 20 mL. All the elements of the cuve in contact with the HF solution were in Teflon. A spiral Pt electrode was placed fully immersed in the solution at the same distance from the sample for every experiment. The power source was a *Keithley Sourcemeter Serie 2400* with a compliance voltage of 20 V. The electrical parameters were adjusted by software associated with the source power instrument. The ECE experiments were conducted in galvanostatic mode.

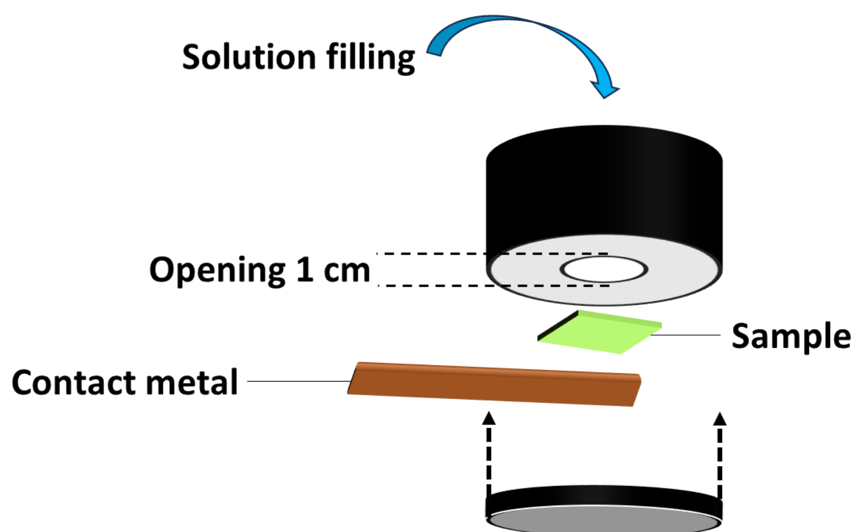


Fig. 7.1 Scheme of ECE cuve adopted in this work.

The reactants employed for the experiments were microelectronic purity grade. The HF (M_w=20.1 g/mol, d=0.97 g/cm^3) and the HCl (M_w=36.5 g/mol, d= 1.19 g/cm^3) mother solutions were respectively at 50 and 37 wt%. The glacial acetic acid (M_w= 60.1 g/mol, d=1.05 g/cm^3) was employed in the experiments as well. The dilutions were done with DI water. After the etching

experiments, the samples were washed by Quick Dump Rinsing (QDR) system for five runs. After the cleaning, the samples were dried with filtered compressed air and dried on a hot plate.

7.3. Results and Discussions

7.3.1. 4H-SiC ECE: High Current

The first set of experiments, labeled as SiC ECE 1, was performed employing high current in the range of the milli-ampere. According to the used samples, it was not possible to convert the current in current densities. The doped and consequently etched spots are very small and one can assume that high current densities are involved. As reported in Tab. 7.1, the current was set at 50 or 100 mA. Two HF concentrations of 0.5 and 15 wt% were used in 15-minute long experiments.

	Current (mA)	HF concentration (wt %)	Time (min)
SiC ECE 1.1	100	0.5	15
SiC ECE 1.2	50	0.5	15
SiC ECE 1.3	100	15	15

Tab. 7.1 Experimental set of electrochemical etching (SiC ECE 1).

The electrochemical etching performed under high current densities on 4H-SiC notoriously produces highly porous surfaces [201]. The behavior is in contrast with the ECE process on Si, where higher current densities contribute to lowering the porous entity (explanation in paragraph 7.3.2). The prediction is confirmed by the SEM micrographs (*Jeol JSM-7900F*) in Fig. 7.2a and Fig. 7.2b respectively of SiC ECE 1.1 and SiC ECE 1.2 samples. In both cases, the low HF concentration does not guarantee a fast oxide etching. The SiC ECE 1.1 treatment has a higher porosity and surface roughness along with a higher current than the SiC ECE 1.2 treatment. The higher surface roughness is confirmed by the AFM (*NT-MDT modular AFM NTEGRA*) roughness reported in Tab. 7.2 with RA values of 6.8 and 4.6 nm respectively for SiC ECE 1.1 and SiC ECE 1.2. The relative AFM images are reported in Fig. 7.2d and Fig. 7.2e.

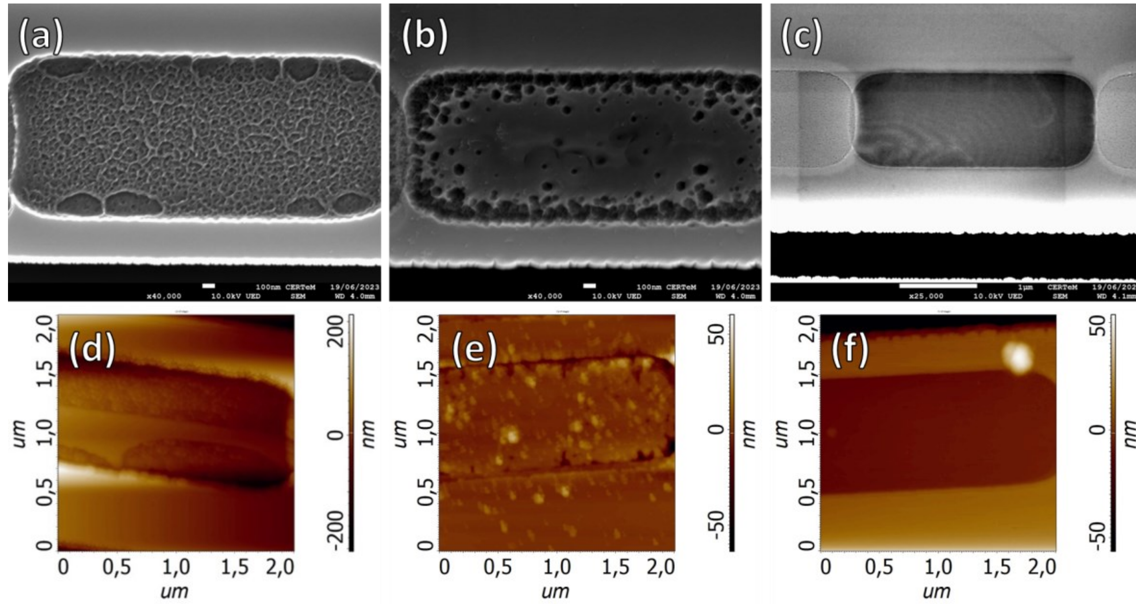


Fig. 7.2 SEM micrographs of 4H-SiC highly doped region of a) SiC ECE 1.1, b) SiC ECE 1.2, and c) SiC ECE 1.3. AFM 4 μm² acquisition 2D height images of d) SiC ECE 1.1, e) SiC ECE 1.2, and f) SiC ECE 1.3 samples.

Preliminary experiments (data not shown) imply that higher etch rates result in increased surface roughness. According to the etch process, as a rate-limiting step, the uncontrolled growth of the oxide layer increases the roughness of the surface. The measured rates by AFM analysis were 9.2 and 2.2 nm/min respectively for SiC ECE 1.1 and SiC ECE 1.2.

	RMS (nm)	RA (nm)	Rate (nm/min)
SiC ECE 1.1	8.0 ± 0.7	6.8 ± 0.8	9.2 ± 0.9
SiC ECE 1.2	6.3 ± 0.8	4.6 ± 0.7	2.2 ± 0.2
SiC ECE 1.3	1.5 ± 1.1	1.3 ± 0.9	1.3 ± 0.01

Tab. 7.2 AFM analysis of 4H-SiC ECE 1 experiments.

The last experiment of the series (SiC ECE 1.3) with the combination of high current and high HF concentration seems to be helpful in reducing the roughness. As a drawback, a lower rate of 1.3 nm/min was measured.

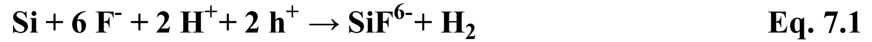
7.3.2. 4H-SiC ECE: Low Current

The system parameters were tuned to obtain lower surface roughness as possible and finally achieve the desired electropolishing. To some extent, the SiC behavior is different than Si. As

reported in *Sailor*'s "*Porous Silicon in Practice*" [202], Si electropolishing occurs at high voltages and current densities whereas the porous form at low values. The Si behavior has to be attributed at:

- Various reactions are involved, transitioning from a 2-electron to a 4-electron mechanism.
- Higher oxidation rate with better oxide uniformity reached in less time.

More in deep, the 2-electron mechanism involves the net reaction displayed in Eq. 7.1. Hence, it involves the formation of H_2 gas which forms bubbles and consequently reactants diffusion issues.

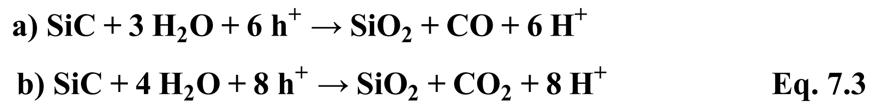


$$\mathbf{Si + 6\,F^- + 2\,H^+ + 2\,h^+ \rightarrow SiF^{6-} + H_2} \qquad \textbf{Eq. 7.1}$$

The electropolishing regime is otherwise favored by a 4-electron mechanism with the reaction reported in Eq. 7.2. Here no gas production should occur.

$$\mathbf{Si + 6\,F^- + 4\,h^+ \rightarrow SiF^{6-}} \qquad \textbf{Eq. 7.2}$$

The SiC electrochemical etching process involves the removal of C as CO or CO_2 gases according to a 6-electron (Eq. 7.3a) or 8-electron (Eq. 7.3b) mechanism, respectively [203]. The anodization causes the oxidation of silicon in SiO_2.



$$\mathbf{a)\ SiC + 3\,H_2O + 6\,h^+ \rightarrow SiO_2 + CO + 6\,H^+}$$
$$\mathbf{b)\ SiC + 4\,H_2O + 8\,h^+ \rightarrow SiO_2 + CO_2 + 8\,H^+} \qquad \textbf{Eq. 7.3}$$

In contrast with Si, the ECE on SiC always involves the production of gases. Hence, the conditions for electropolishing follow different rules. The effects of current density on the surface porosity of SiC have already been investigated. *Cao* et al. [201] found that employing low current densities of around 100 μA/cm^2 leads to a less porous surface. In addition, *Tan* et al. [204] obtained a highly porous surface by using current densities within the 1-100 mA/cm^2 range. The results indicate a reversed trend when compared to Si as previously introduced.

For these assumptions, the second experimental (label SiC ECE 2) set was set with lower currents. The currents ranged between 1 and 10 μA. The HF concentrations were varied according to two levels of 3 and 30 wt%. Finally, the time was fixed at 10 min. The parameters combination is reported in Tab. 7.3 for a total of 4 runs.

	Current (μA)	HF concentration (wt %)	Time (min)
SiC ECE 2.1	10	3	10
SiC ECE 2.2	1	3	10
SiC ECE 2.3	10	30	10
SiC ECE 2.4	1	30	10

Tab. 7.3 Experimental set of electrochemical etching (SiC ECE 2).

The morphological SEM analysis revealed a flattened etched surface for all the samples in Fig. 7.3. The etched areas are recognizable from the corner at high grayscale intensity. The SEM micrographs are not suitable for qualitatively determining the variations of roughness from one sample to another.

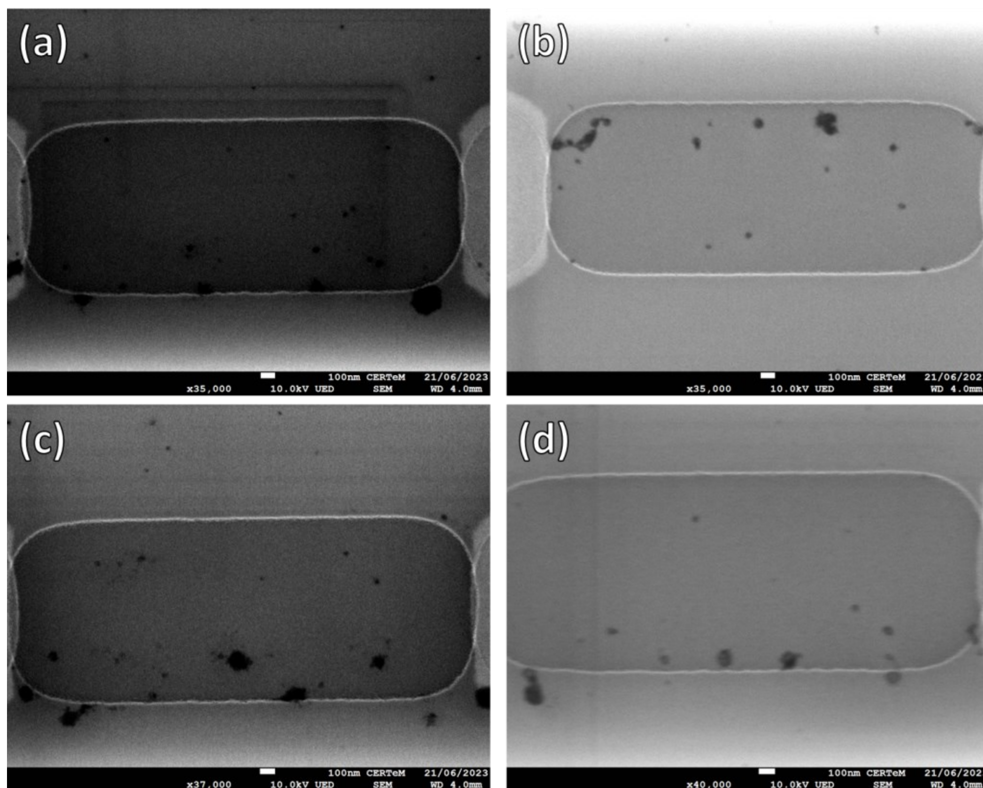


Fig. 7.3 SEM micrographs of 4H-SiC highly doped region of a) SiC ECE 2.1, b) SiC ECE 2.2, c) SiC ECE 2.3, and d) SiC ECE 2.4.

The AFM analysis revealed low roughness values for all the samples with RA values ranging from 1.6 to 4.2 nm along with etch rate with an average value of 2.5 nm/min as shown in Tab. 7.4. A comparison with the SiC ECE 1 experiments showed that using a lower current does not lead to a

decrease in etch rate, as shown by the comparison between Tab. 7.2 and Tab. 7.4. The effects could be attributed to the rate-limiting step associated with etching instead of the oxidation step.

	RMS (nm)	RA (nm)	Rate (nm/min)
SiC ECE 2.1	1.9 ± 0.6	1.6 ± 0.6	2.4 ± 0.1
SiC ECE 2.2	2.8 ± 0.3	2.1 ± 0.6	2.5 ± 0.1
SiC ECE 2.3	4.8 ± 0.3	4.2 ± 0.3	2.5 ± 0.03
SiC ECE 2.4	2.0 ± 0.4	1.6 ± 0.2	2.2 ± 0.2

Tab. 7.4 AFM analysis of 4H-SiC ECE 2 experiments.

The reduction in current employed during the ECE contributed to lowering the surface roughness with a minimum RA value of 1.6 nm for SiC ECE 2.1 and SiC ECE 2.4 samples. According to the typical 4H-SiC atomically flat surface, the electropolishing performed by ECE could be further improved to achieve lower average roughness. The experimental set will introduce two new reagents with focused roles oriented toward modifying and improving the ECE process.

7.3.3. 4H-SiC ECE: Solution Formulation

The third experimental set introduces two new chemical agents in the solution: HCl and acetic acid. The HCl has a double role in enhancing the oxidation of the surface and reducing the concentration of the F^- nucleophile. Acetic acid has the role of maintaining at a constant value the current density with the consequential reduction of the size of the pores [205].

The following set of experiments sees currents between 10 and 100 μA. The HF concentration varies around 1 and 5 wt% values. The HCl and acetic acid concentrations were fixed at 5 and 3 wt%, respectively. The experimental time was fixed at 10 minutes. All the conditions combinations are reported in Tab. 7.5.

	Current (μA)	HF concentration (wt %)	HCl (wt %)	Acetic acid (wt %)	Time (min)
SiC ECE 3.1	100	1	5	3	10
SiC ECE 3.2	10	1	5	3	10
SiC ECE 3.3	100	5	5	3	10
SiC ECE 3.4	10	5	5	3	10

Tab. 7.5 Experimental set of electrochemical etching (SiC ECE 3).

The SEM micrographs in Fig. 7.4 reveal a similar flattish surface as previously seen for the SiC ECE 2 samples. The contribution of the new reactants allowed us to lower the actual average roughness as it will be introduced soon.

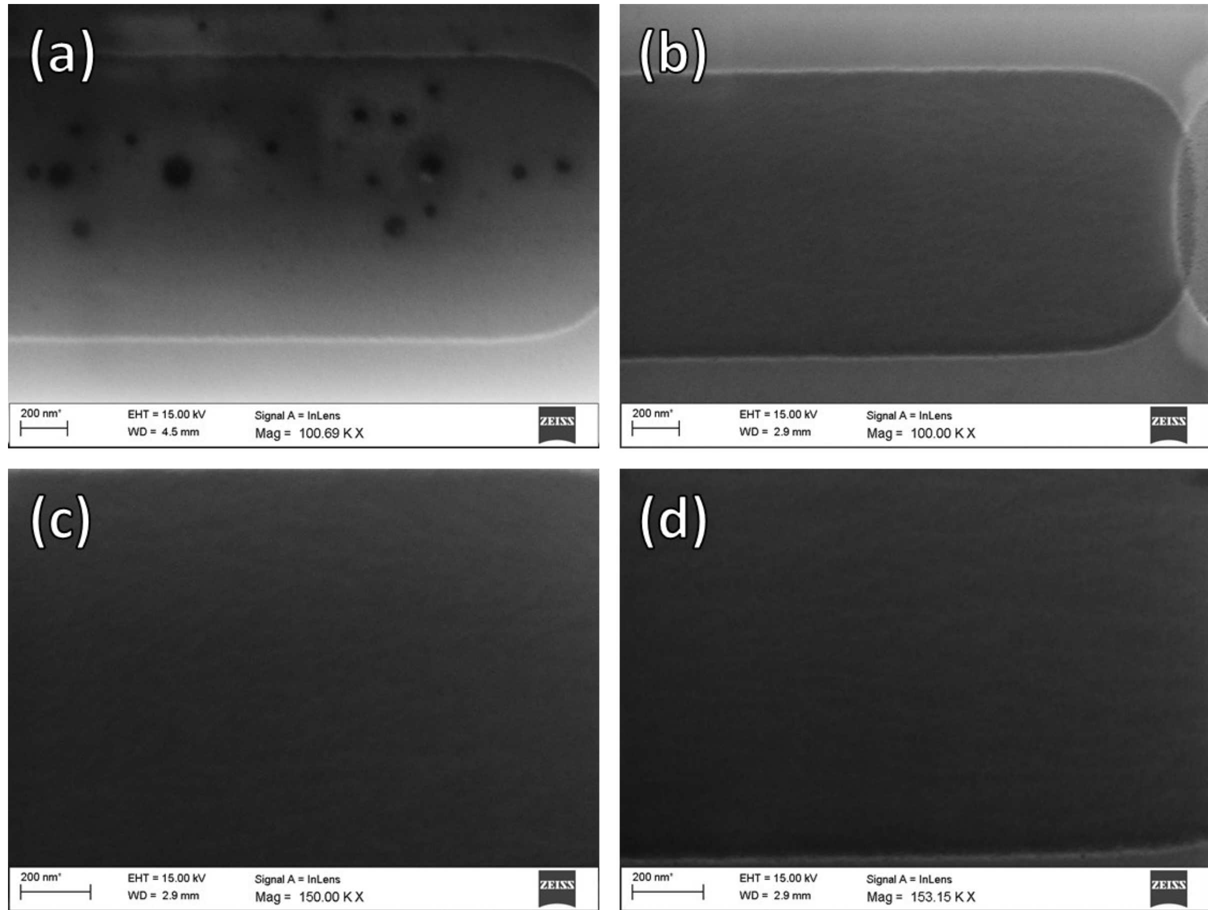


Fig. 7.4 SEM micrographs of 4H-SiC highly doped region of a) SiC ECE 3.1, b) SiC ECE 3.2, c) SiC ECE 3.3, and d) SiC ECE 3.4.

The AFM analysis revealed impressive low roughness for SiC ECE 3.1 and SiC ECE 3.3 samples as shown in Tab. 7.6. The RMS and RA values range between 0.5 and 0.3 nm, close to the 0.1-0.2 nm of the standard flat 4H-SiC surface roughness. Herein, the rate is preserved at the previously reported value of 2.5 nm/min. The unchanged rate reinforces the previously hypothesized rate-limiting step of the etching process. The HCl chemical has the main role in lowering the pH and lowering the F^- nucleophile concentration. The HF is a weak acid ($Ka=6.7\cdot10^{-4}$) and its dissociation is governed by a reversible reaction as shown in Eq. 7.4. As the pH lowers and the H_3O^+ concentration increases, the equilibrium shifts to the reagents (the left).

$$\mathbf{HF + H_2O \rightleftarrows F^- + H_3O^+} \qquad \textbf{Eq. 7.4}$$

The F^- anions are the main ones responsible for SiO_2 etch although the HF solution equilibria are more complex involving polymeric forms such as HF_2^-, $H_2F_3^-$, and, $H_3F_4^-$ chemical species, whose concentration depends on pH and HF concentration [206,207]. The combination of low pH and low HF concentration leads to the equilibrium shift to the HF form.

	RMS (nm)	**RA (nm)**	**Rate (nm/min)**
SiC ECE 3.1	0.5 ± 0.1	0.4 ± 0.1	2.4 ± 0.1
SiC ECE 3.2	4.0 ± 1.3	3.4 ± 1.1	3.6 ± 0.1
SiC ECE 3.3	0.4 ± 0.1	0.3 ± 0.1	2.3 ± 0.03
SiC ECE 3.4	1.7 ± 0.5	1.4 ± 0.6	1.9 ± 0.04

Tab. 7.6 AFM analysis of 4H-SiC ECE 3 experiments.

The results show that the main goal is achieved in the present work. The ECE process is governed by both physical and chemical parameters. This feature makes the ECE technique of utmost complexity. The low etch rates of electropolishing are necessary to perform fine etching of surface flattening.

7.3.4. Flat 4H-SiC at High Current Densities

The ECE technique could be useful in a variety of applications. It was previously investigated for the electropolishing application working with low current densities. Besides, the ECE technique offers many advantages in many fields. In this section, the topic of ECE on n-doped 4H-SiC flat polished samples is covered. The samples were highly doped (n-doped with resistivity 0.037 Ω·cm) and no light irradiation was necessary to properly perform the ECE attack, as previously reported by *Gautier* et al. [208].

A total of three experiments were conducted by varying the current, and the HF concentration, and by fixing the time at 10 min as reported in Tab. 7.7. The current densities were varied according to two values 100 mA and 1 mA flowing through a 1 cm^2 aperture. The concentrations varied between 0.5 and 15 wt%. The variables' combinations were reported in Tab. 7.7.

	Current density (mA/cm^2)	**HF concentration (wt %)**	**Time (min)**
SiC flat 1.1	100	15	10
SiC flat 1.2	1	15	10

SiC flat 1.3	1	0.5	10

Tab. 7.7 Experimental set of electrochemical etching on 4H-SiC n-doped ρ=0.037 Ω·cm Si-face.

The higher current employed in the first experiment caused the production of a highly porous surface. The detachment of some flakes even in a small 4 cm^2 sample occurred as displayed in the SEM micrograph in Fig. 7.5a. The flakes are portions of material that usually detach from the surface. The production and further manipulation of flakes were the object of study in this doctoral work and the discussion is available in chapter 8. The bottom level on the left is not focused because distant from the point of focus. On the right side of Fig. 7.5a and in Fig. 7.5b, the porosified surface is attributed to a portion of material not separated from the surface. The delamination effects of high current density were already reported in [209] and replicated in the flakes production investigation in chapter 8.

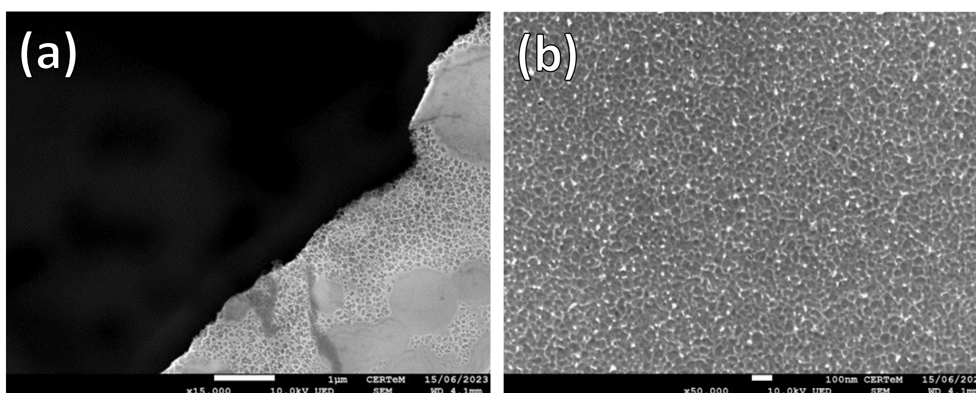


Fig. 7.5 SEM micrographs of SiC flat 1.1 on a) interface zone and b) porous zone.

The SiC flat 1.2 sample whose surface is shown in Fig. 7.6a, exhibits prominent stripes. The sample was kept under 1 mA/cm^2 current density and HF acid solution at 15 wt%. The noticeable stripes were the results of the typical marks due to the polishing processes made on 4H-SiC substrates [210,211]. Generally, the stripes are barely detectable from SEM acquisitions as highlighted in the red circle of Fig. 7.6a. The ECE selectively attacked some stripes by making them more visible and clear. The selective etching can be attributed to the higher surface energy along the stripes compared to the rest of the substrate. The ECE mechanism enables the surface oxidation process and it is particularly efficient on high-energy surfaces, especially at low current densities [209]. The lower current density used in the second experiment prevented the complete surface etch and selectively etched the defects. The high HF concentration allows the immediate etching of the generated oxide and the refreshing of the surface for further oxidation. Regardless,

for unknown reasons, some stripes were more etched than others as highlighted in the red circle of Fig. 7.6a. The ECE approach enabled to highlighting the surface defects cleanly and effectively, with the possibility of spotting them in an easy way the defects.

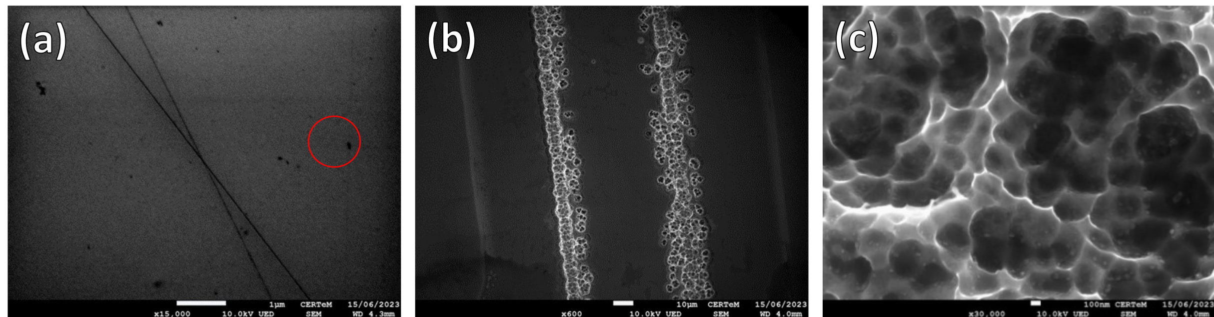


Fig. 7.6 SEM micrographs of a) SiC flat 1.2, b) SiC flat 1.3, and c) higher magnification of SiC flat 1.3 focusing on the porous stripes.

Maintaining the lower current density of 1 mA/cm^2 and lowering the HF concentration, the SiC flat 1.3 samples have evidenced high porous production along the stripes as noticeable in Fig. 7.6b. The different mechanisms of attack are due to the lower HF concentration. Herein, the oxidation rate is prominent compared with the oxide etching rate. The predominant oxide growth creates highly porous zones as shown in the high magnification micrograph in Fig. 7.6c. The porous lines along the polishing stripes constitute an interesting discovery. The production of localized porous structures could find applications in the development of devices in the field of sensing [212–214]. The results are furthermore interesting in observing the complexity behind the ECE mechanism and how all the fundamental parameters of the system play a major role.

7.4. Conclusions

The ECE technique on 4H-SiC was investigated. The research involved the fine-tuning of the critical parameters (current and solution composition) to enter into the electropolishing regime. Since the well-investigated Si ECE conditions differ from 4H-SiC, the mechanisms of ECE on SiC have been taken under study. Various attempts were made employing different ECE conditions, and the lower measured roughness was as low as 0.4 nm by maintaining an etch rate of 2.3 nm/min. It was discussed how the electropolishing regime is promoted by low current densities and, hence, low etch rates. The measured low etch rates may not be suitable for extensive etching, but they could be useful in surface refining applications.

The ECE technique was useful in evidencing the polishing stripes of traditional 4H-SiC wafers. Opportune conditions have evidenced the possibility of creating porous lanes along the polishing stripes. The discovery could be useful in the development of sensors or detectors based on 4H-SiC.

Finally, ECE at high current densities on 4H-SiC produced a highly porous surface with delimitation phenomena of the material's portion. The detachment mechanism has been used in the production of highly porous 4H-SiC powders which will be discussed in the following chapter.

8. 4H-SiC Particles Production by ECE

8.1. Introduction

The last experimental part is dedicated to research activities that do not have a direct and strict correlation with microelectronics applications. The electrochemical etching (ECE) technique has the potential to create porous material by removing small portions of the material through delamination, as illustrated in Fig. 8.1a. Each step of material removal could be investigated closely in the voltage plot in Fig. 8.1b. The plot displays peaks and valleys that follow over time. Each variation is assumed to be associated with the detachment of material. The sudden fall of voltage indicates a new cycle of ECE attack on a freshly exposed surface. The etching process leads to the delamination of a portion of material with the production of the so-called “flakes”, as shown in Fig. 8.1c. To let the formation of porous flakes, high current densities come into play. For 4H-SiC, the appearance of pores causes a change in color from the greenish of the starting wafer to the gold of the flakes. The porous flakes are characterized by a low density and high volatility.

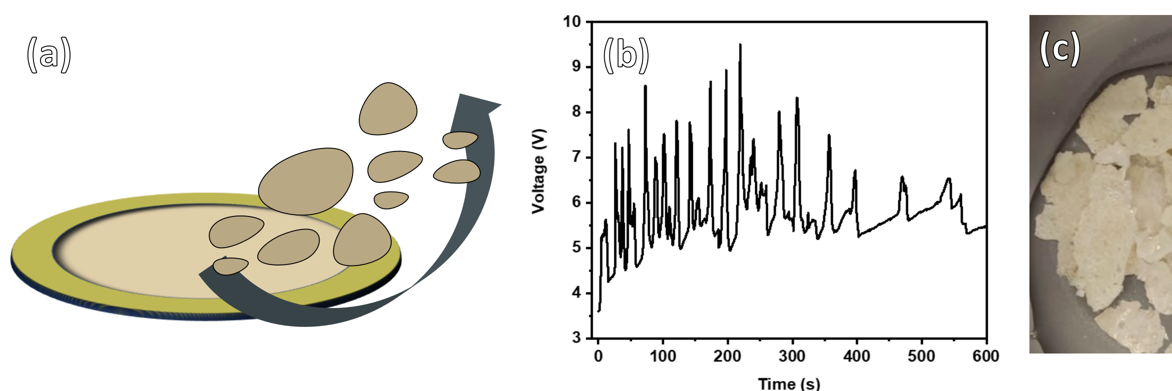


Fig. 8.1 a) Schematization of flakes production from high current density electrochemical etching, b) voltage variations with time of 4H-SiC Si-face ECE at 100 mA/cm^{2}, and, c) photo of 4H-SiC flakes.

In this experimental section, the flakes analysis will be presented. It will shed light on the differences in morphology and chemical composition of the flakes obtained from the C-face and Si-face of 4H-SiC wafers. The flakes are an interesting material due to their high porosity, which will be discussed in more detail shortly. Nevertheless, they can be exploited to produce micro- or nano-particles on a top-down approach. The two methods adopted are the sonication and the ball milling techniques. The sonication of the flakes in a water dispersion leads to the production of nanoparticles (NPs) with the same gold color as displayed in Fig. 8.2a. Instead, the ball milling

produced particles that change in color from gold to brownish as shown in Fig. 8.2b. The color change indicates a modification in the structure, size, and porosity of the starting material.

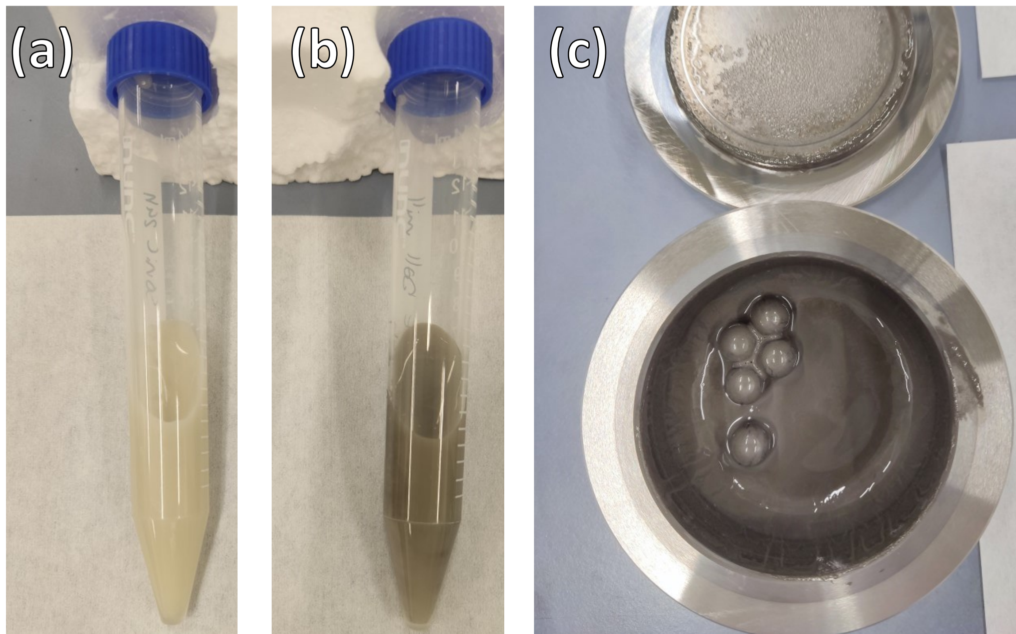


Fig. 8.2 Photos of a) sonicated 4H-SiC flakes dispersion, b) ball milled 4H-SiC flakes dispersion, and c) ball milling bowl after 2 hours of treatment of 4H-SiC flakes.

The ball milling approach involves mechanically crushing and grinding a material feed inside a bowl filled with balls, usually both made of the same material, as shown in Fig. 8.2c. The bowl is kept under rotation at adjustable speed in the range of hundreds of rounds per minute. At the end of the treatment, the final product can be recovered as a dispersion in water or organic solvent. The flakes production, the sonication, and the ball milling procedures will be discussed as follows.

The 4H-SiC particles have various applications apart from microelectronics, such as photoluminescence [215], light detection [216], and as components of the feed in polishing [217]. SiC-based particles with sizes ranging from micro to nano could possibly enhance most of these applications.

8.2. Materials and Methods

4H-SiC flakes production was performed by the ECE technique with a PS electrochemical cell from *AMMT Advanced Micromachining Tools* company. The electrochemical attack was performed under galvanostatic mode etching for 300 cycles under pulsed current at 510 mA/cm^2. The pulsed current was kept in the on-state for 2 s and 5 s in the off-state. The electrolyte solution was a mixture of HF 30 wt% + CH_3COOH (Acetic acid) 10 wt% + H_2O. A 4H-SiC n-type (resistivity

equal to 0.037 Ω·cm) material was employed for the top-down approach. Flakes fabrication was carried out on both C- and Si-faces. The flakes were collected and washed several times in DI water to eliminate all the absorbed HF. The washing procedure was repeated till the neutral pH of the water was detected by indicator paper. The dispersed flakes were filtered and dried in the oven at 80 °C for 4 h. According to the described method, the mass of flakes produced from a 4-inch 4H-SiC is around 1 g.

The first adopted method of particle-making was sonication. An average mass of 10 mg was put in a Falcon test tube with 10 mL of DI water. The sonication was performed in an ultrasonicator bath at room temperature for 2 h or 24 h. The sonicated dispersion was then centrifugated twice at 4500 rpm for 15 min and one time at 9000 rpm for 15 min.

The ball milling experiments were performed with a *PULVERISETTE 6 classic line* instrument of *Fritsch*. Each session of ball milling was performed with 100 mg of flakes (feed material) and a few drops of water. The water serves as a lubricant and heat dissipator. A WC + Co bowl and a total of 5 balls were used for the experiments. The complete ball milling recipe for both the C and Si surfaces is given in Tab. 8.1. A total of 4 runs were set with a total milling time of 2 h. Each run lasted 30 min with a pause of 15 min to dissipate the heat generated. A maximum speed of 400 ± 10 rpm was set as standard for all runs. The first run started with clockwise rotation, followed by alternating with counterclockwise rotation until the end of the process.

Runs	**Speed (rpm)**	**Time (min)**	**Rotation sense**	**Time break (min)**
1st	400	30	Clockwise	15
2nd	400	30	Counterclockwise	15
3rd	400	30	Clockwise	15
4th	400	30	Counterclockwise	End

Tab. 8.1 Ball milling recipe of 4H-SiC flakes treatment.

The ball-milled flakes were recovered with DI water to create a mother dispersion collected in a *Falcon* test tube. The produced particle dispersions were sonicated for 2 h or 24 h followed by centrifugation twice time at 4500 rpm for 15 min and one time at 9000 rpm for 15 min. The separated particles were collected and stored. The balls were sonicated in water to recover the attached SiC particles. The bowl and the balls were cleaned with acetone and paper.

The porosity of the flakes was assessed using Brunauer-Emmett-Teller (BET) adsorption-desorption of N_2 at −196 °C via a *Micromeritics Tristar II Plus 3020*. Prior to analysis, the materials were subjected to out-gassing at 100 °C overnight.

8.3. Results and Discussions

8.3.1. 4H-SiC C-face and Si-face Flakes Analysis

The electrochemical etching of 4H-SiC produces flakes with dimensions in the order of centimeters. The morphology of flakes produced from the Si or the C-face was characterized by SEM (*Zeiss SUPRA-55 VP*). The plane view of the C-face flakes (Fig. 8.3a) shows a morphology structured in tips and voids densely distributed. The columnar-like sidewall view morphology of the C-face flakes shown in Fig. 8.3b is well-known as reported in [218]. The columnar shape is a result of the [0001] direction of the C-face being easily etched [203].

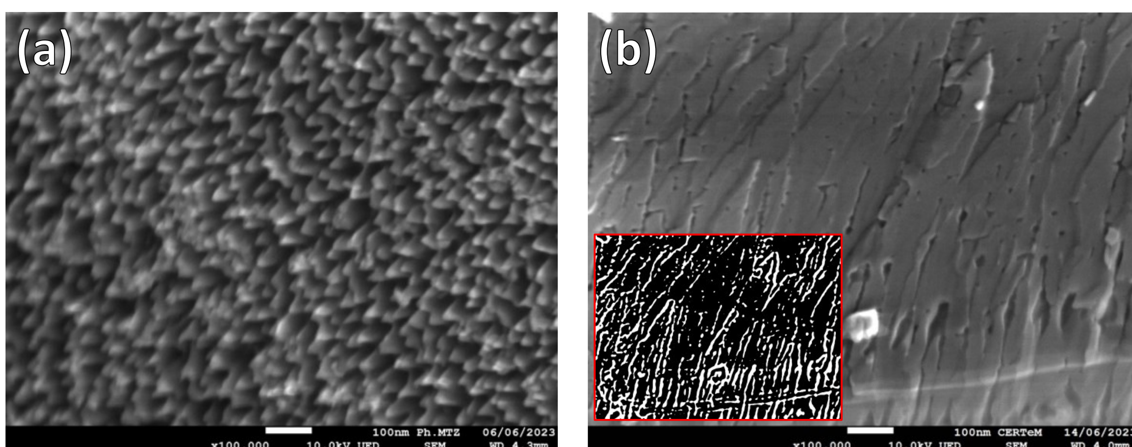


Fig. 8.3 SEM micrographs of ECE derived flakes from 4H-SiC C-face of a) plane and b) sidewall view. The inset of b) were the results of threshold image analysis respectively for c) C-face and d) Si-face flakes walls.

When transitioning to the Si-face, the plane view in Fig. 8.4a shows a cauliflower-like structure with less uniform understructures compared to those on the C-face. Finally, the sidewall view of the Si-face flakes (Fig. 8.4b) shows the well-known "dendritic" structure as reported in [219]. The morphology is due to the pores propagation along the $(11\bar{0}4)$ and $(1\bar{1}04)$ planes and their symmetrical equivalents [220] with angles between 90 and 120°. The high versatility of the ECE approach may be a result of the possibility of obtaining various morphologies for the Si-face, as elucidated by *Shishkin* and coworkers [219].

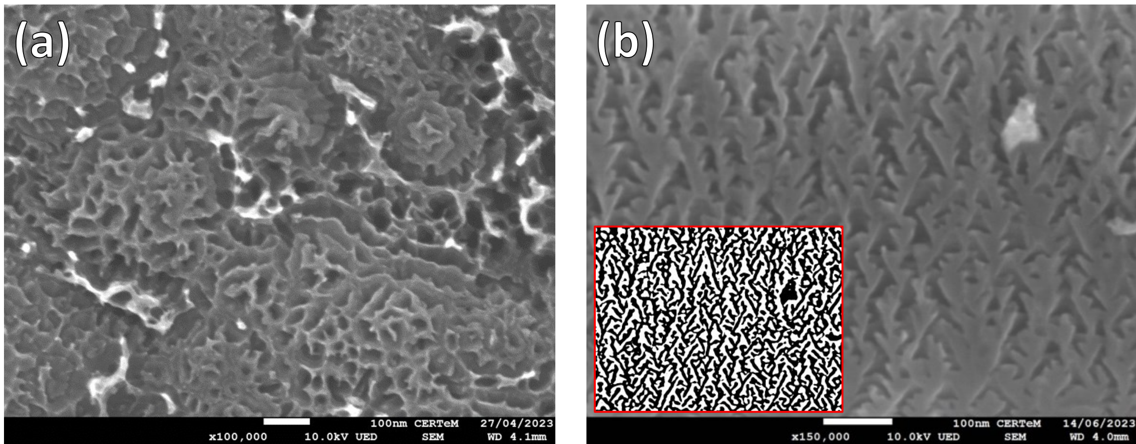


Fig. 8.4 SEM micrographs of ECE derived flakes from 4H-SiC Si-face of a) plane and b) sidewall view. The inset of b) were the results of threshold image analysis respectively for c) C-face and d) Si-face flakes walls.

The image analysis by *ImageJ* software permitted us to estimate the porosity on both the surface and the walls of the flakes. The porosity was estimated by measuring the ratio between the thresholded and the total area. Examples of threshold images are displayed as inset in Fig. 8.3c and Fig. 8.3d. On both the flakes surface and the walls it was measured a lower porosity for the C-face was compared with the Si-face as reported in Tab. 8.2.

	Acquisition zone	Porosity (%)
C-face	**Plane view**	30 ± 6
	Side view	21 ± 5
Si-face	**Plane view**	45 ± 12
	Side view	44 ± 5

Tab. 8.2 Porosity calculated from SEM acquisition and image analysis of 4H-SiC C-face and Si-face derived flakes plane and side view.

The columnar morphology of the C-face flakes was also characterized by AFM (*NT-MDT modular AFM NTEGRA*) as shown in Fig. 8.5a. The roughness in terms of RMS, RA, and PtP values decreases with the acquisition area as shown in Tab. 8.3. This effect is due to the presence of large valleys and hills on the surface, as confirmed by the SEM micrograph in Fig. 8.5c. On the contrary, the AFM analysis of the Si-faced flakes (Fig. 8.5b) showed a lower and more constant

roughness than the C-faced flakes. No wavy surface in the micrometer range was observed for the Si-face flakes.

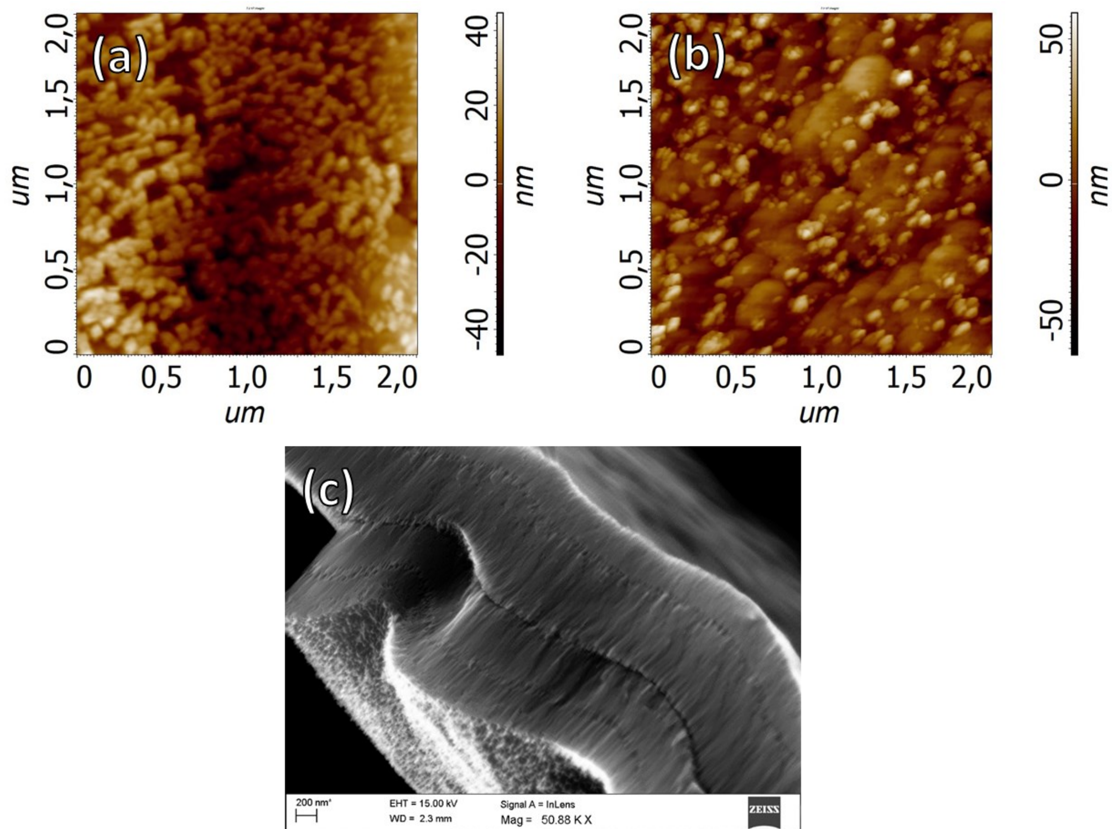


Fig. 8.5 AFM 4 μm² images of 4H-SiC flakes from a) C-face and b) Si-face, and c) SEM side view micrograph of C-face derived flakes.

		RMS (nm)	RA (nm)	PtP (nm)	Sm (nm)
4H-SiC C-face	**10x**	126.8	98.1	951.8	1278
	5x	50.5	40.7	416.9	1148
	2x	14.6	11.8	91.2	147
4H-SiC Si-face	**10x**	16.0	12.5	170.7	498
	5x	16.0	12.6	123.8	274
	2x	14.3	11.2	120.9	190

Tab. 8.3 AFM analysis of flakes from 4H-SiC C-face and Si-face. The RMS and RA refer to average roughness, PtP refers to the maximum height, and Sm refers to the average lateral dimensions.

The comparison of the lateral dimension parameter (Sm) in Tab. 8.3 suggests a lower pore dimension for the Si-face than the C-face flakes. The higher porosity of the Si-face was further corroborated by BET analysis (*Micromeritics Tristar II Plus 3020*) for a direct determination of the pores' dimension and the surface area. The BET analysis confirmed a lower pore dimension of 4.4 and 48.1 nm on the Si-face flakes compared to an unimodal distribution of 59.4 nm for the C-face as shown in Fig. 8.6.

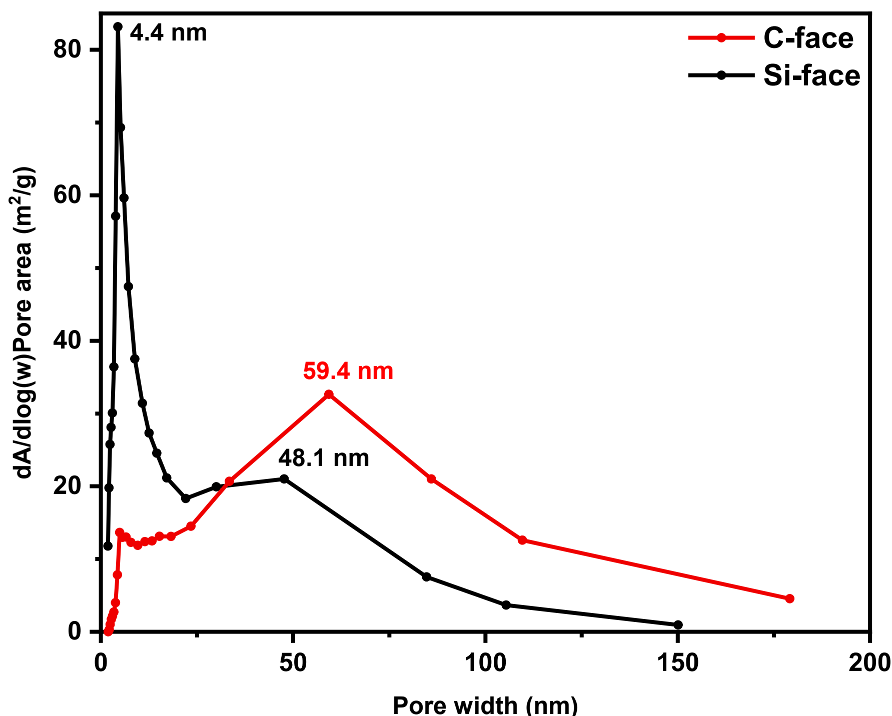


Fig. 8.6 BET of 4H-SiC flakes from C-face (red curve) and Si-face (black curve).

The BET analysis revealed also a great increase in the surface area of both the C-face (36.4 m^2/g) and Si-face (46.5 m^2/g) flakes compared to the standard SiC particle systems with surface area comprised between 5-15 m^2/g [221–224]. The scientific community has realized many contributions to porous micro and nano-SiC systems with a surface area equal to or greater than 50 m^2/g [225–229]. Some of these approaches involved the use of energy-demanding techniques or uncommon reagents, making them less viable for applications at large scale. The discovery confirms the high porosity of the electrochemically produced flakes. The BET analysis also highlighted a porosity increase of 22% of the Si-face compared to the C-face flakes. The increment is more in line with the porosity difference estimated by the image analysis fulfilled from the plane view micrographs.

	Surface area (m^2/g)
Standard SiC particles	5-15
4H-SiC C-face flakes	36.4
4H-SiC Si-face flakes	46.5

Tab. 8.4 BET surface area values of standard SiC NPs, 4H-SiC C-face, and Si-face flakes.

In the present work, the elemental and chemical composition of the flakes was also investigated. The XPS (*PHI 5600 Multi Technique system*) elemental compositions of both C-face and Si-face flakes were compared to the pristine 4H-SiC wafer with their respective faces (Tab. 8.5). Unexpectedly, the surface elemental composition does not change drastically before and after the ECE for both faces. The pristine 4H-SiC carbon face sample had an overoxidized surface with a higher O/Si ratio than the other samples. After the ECE, the O/Si ratio normalizes to a value of 0.4 and an oxygen percentage of 14-15%. Since the ECE is performed under a moderately concentrated HF solution, the final oxygen percentage is due to the thermal oxide layer and the adventitious carbon contamination from exposure to air.

	C%	Si%	O%	F%	C/Si	O/Si
4H-SiC C-face reference	36.21	37.87	25.92	NA	0.96	0.68
4H-SiC Si-face reference	46.99	41.70	11.05	NA	1.13	0.26
4H-SiC C-face flakes	44.08	39.59	15.01	1.32	1.11	0.38
4H-SiC Si-face flakes	47.65	36.49	14.14	1.71	1.31	0.39

Tab. 8.5 XPS elemental composition of 4H-SiC C-face and Si-face references and their respective flakes.

The surface chemical composition was either studied by XPS analysis. A comparison between the C-face (left) and the Si-face (left) flakes is shown in Fig. 8.7. The C1s signal is displayed in Fig. 8.7a. The deconvoluted components of Si-C at 283.4 eV and C-C at 284.8 eV were attributed to both samples. The major differences lie in the presence of a specific Si-O-C component at 286.4 eV for the C-face in contrast with the C-O group at 286.1 eV for the Si-face. The presence of a Si-O-C is corroborated by the presence of a component in the Si2p signal for the C-face flakes in Fig. 8.7b. It was not possible to detect the same component in the relative Si-face signal. Instead, a

stoichiometric SiO_2 component, with a binding energy (BE) of 103.5 eV, was observed due to a slight tail termination at higher BE. The O1s is not reported since no particular groups and differences were detected between the two faces.

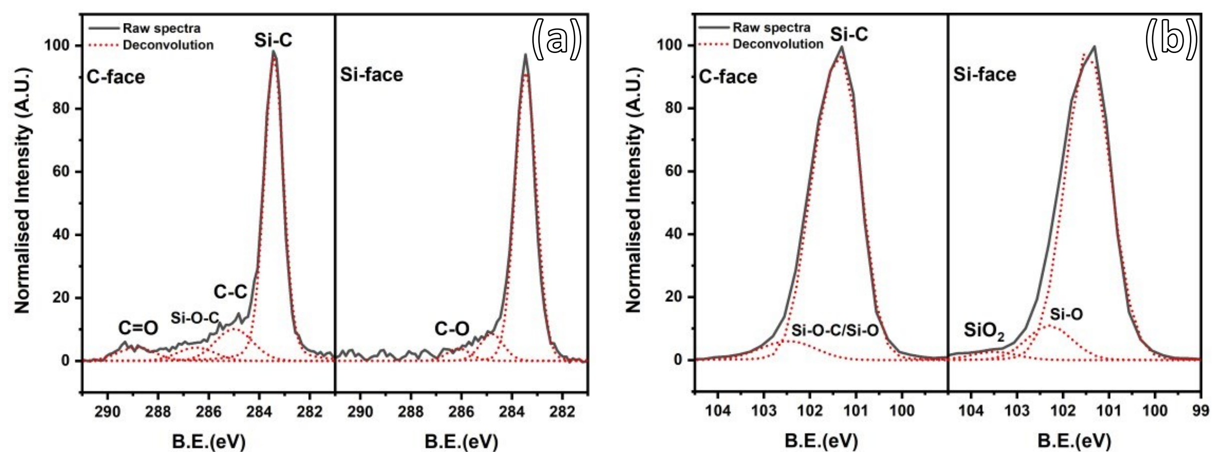


Fig. 8.7 XPS spectra of 4H-SiC derived flakes from C-face (left) and Si-face (right) of a) C1s and b) Si2p. The solid gray and the dotted red curves respectively represent the XPS raw spectra and the deconvolution. The same components were not labeled on the right.

The presented results highlight that the major differences concerning the two faces lie in the different morphology of the flakes at the micro and nano-dimension. The chemical composition between the two faces returned similar characteristics. The findings are due to the mechanisms of production of the flakes. The portion of SiC materials detaches from the wafer maintaining almost the same nature but with different structures and morphological appearances.

8.3.2. Sonication of 4H-SiC C-face and Si-face Flakes

This section discusses the production of SiC nanoparticles (NPs) using a top-down method of flakes sonication. As displayed in Fig. 8.8a, after the sonication of the C-face flakes, it is possible to collect nanoparticles in the form of nanorods (NRs). Under the same conditions, the Si-face-derived nanoparticles look smaller in size and less uniform in shape as shown in Fig. 8.8b.

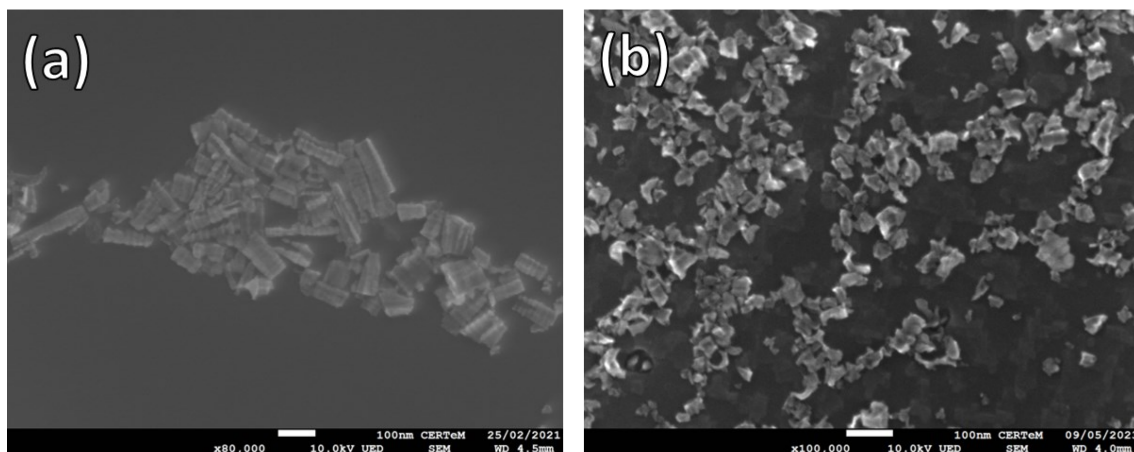


Fig. 8.8 SEM micrographs of 4H-SiC a) C-face NRs and b) Si-face NPs produced under sonication for 24 h and centrifugation procedures.

The NPs sizes were indeed characterized by the SEM micrographs as presented in Tab. 8.6. Firstly, it was possible to quantify the reduced sizes of the Si-face-derived NPs compared with the relative C-face-derived NRs. Secondly, it was possible to verify the stability of the NPs in water dispersion. After two years the length and the width of the C-face flakes derived NRs remained unvaried. The result is of most importance since the mentioned feature is mandatory for some Si and SiC-based particle applications such as drug delivery [230] and phototherapy [231,232]. For instance, porous silicon nanoparticles are not stable in water and biological fluids, and their dissolution can be observed over time, although it may occur slowly [231,233,234].

		Size (nm)
C-face (2 years dispersion)	**Length**	112 ± 50
	Width	41 ± 18
C-face	**Length**	127 ± 43
	Width	38 ± 13
Si-face	**Length**	48 ± 16
	Width	26 ± 8

Tab. 8.6 4H-SiC NPs size measured by SEM micrograph analysis.

The C-face and Si-face derived NPs sizes were put in comparison also by DLS (*Malvern Zetasizer Nano-ZS Zen 3600*) analysis. The C-face derived NPs are bigger than the relative Si-face NPs as confirmed by the DLS analysis results in Tab. 8.7. The C-face polydispersion appears higher than the Si-face one as evidenced by the Polydispersity Index (PdI) value. While the Si-face NPs

results are all below 100 nm, the C-face dispersion presents some particles above 100 nm, so by definition, there is the presence of microparticles.

	Z-Ave (d.nm)	PdI	Number Mean (d.nm)	Volume Mean (d.nm)
C-face sonication 24h	209.60 ± 43.89	0.79 ± 0.08	37.72 ± 4.75	342.90 ± 84.45
Si-face sonication 24h	64.47 ± 0.36	0.19 ± 0.01	37.94 ± 1.59	56.54 ± 11.15

Tab. 8.7 DLS analysis of 4H-SiC NPs of C-face and Si-face from flakes sonication 24h.

The reason for the different shapes and sizes of the nanoparticles needs to be investigated with respect to the morphology of the flakes. The Si-face is characterized by a cauliflower-like surface with irregular shape structures as exposed in Fig. 8.9a. The sonication has detachment effects and the illustration of the NPs production is shown in Fig. 8.9c. At first sight, the NPs production from C-face flakes seems to be of simple interpretation. The top surface is featured by columnar-like structures as evidenced in Fig. 8.9d. The sonication could have for sure the effect of detaching the columns on the top as depicted in Fig. 8.9b.

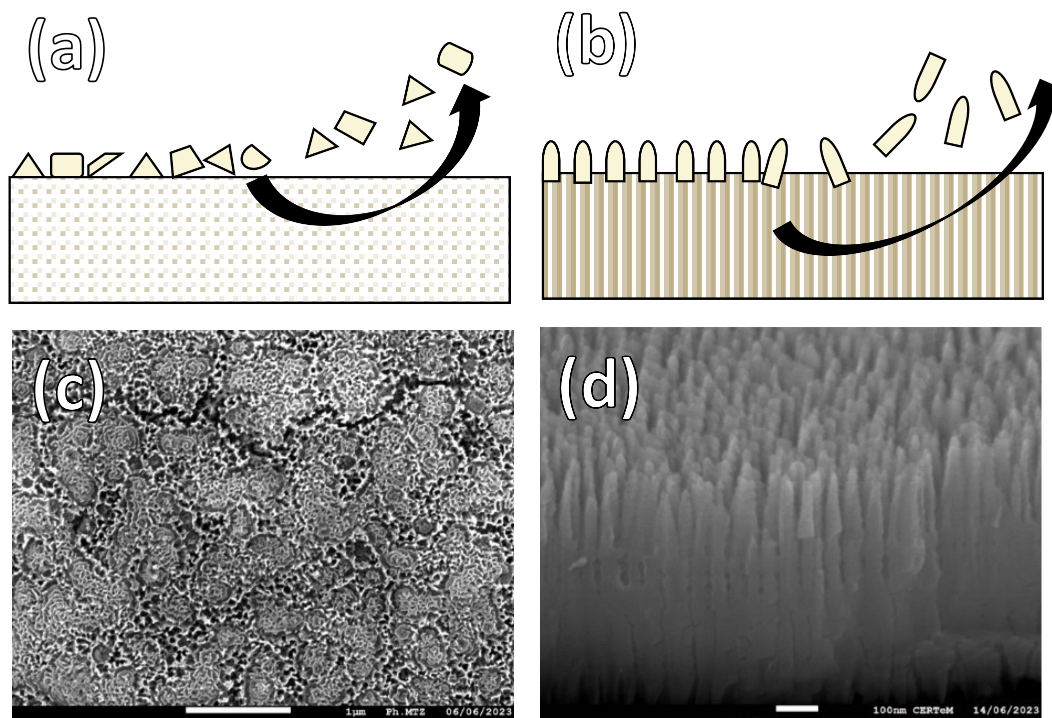


Fig. 8.9 Illustration of the sonication effects on 4H-SiC a) Si-face and b) C-face flakes. SEM micrographs of c) Si-face and d) C-face flakes.

A second possible mechanism of NRs production from C-face flakes sonication is illustrated in Fig. 8.10a. Some SEM micrograph sideviews revealed a possible lateral detachment as highlighted in the red box of Fig. 8.10b. The hypothesis is reinforced by the presence of steps on the top corner of the flakes as emphasized in the red box in Fig. 8.10c.

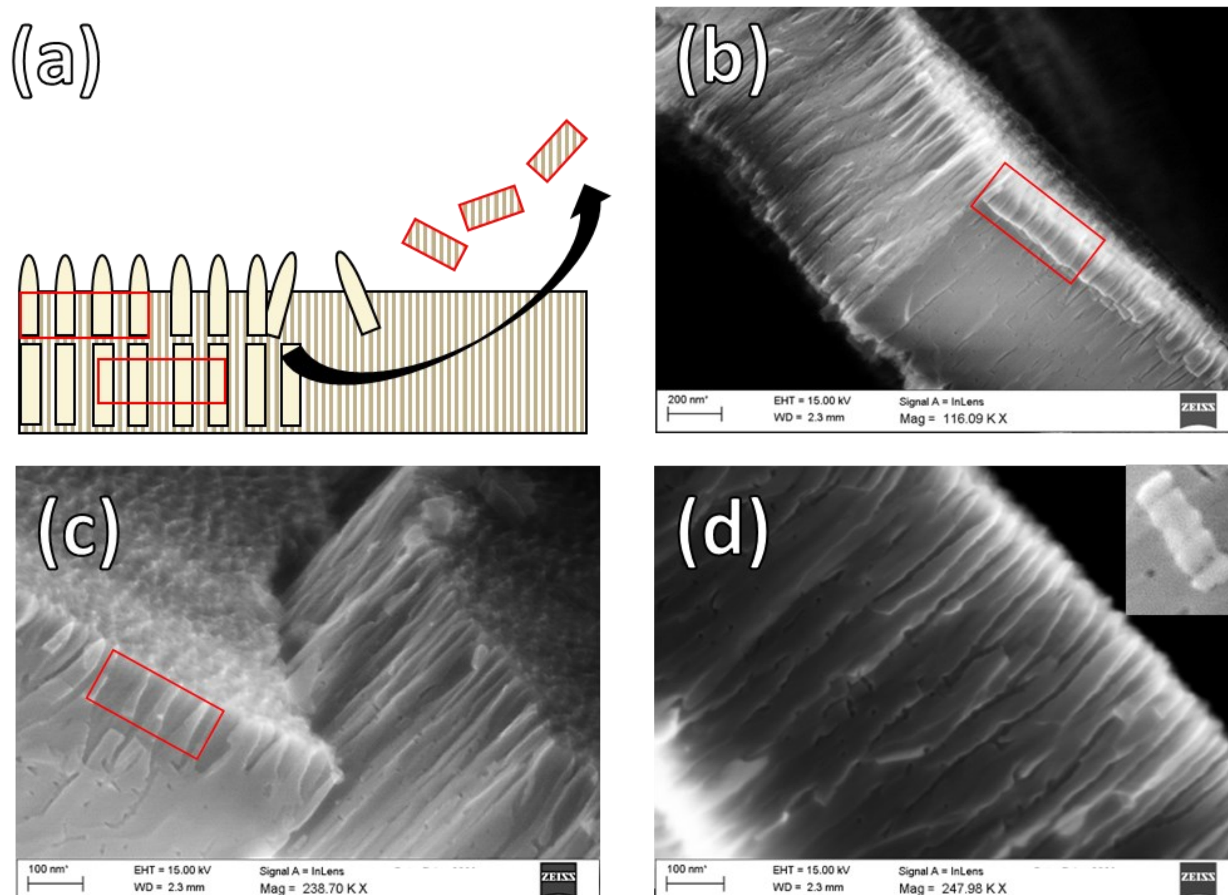


Fig. 8.10 Illustration of the second mechanism of C-face flake NPs. SEM micrographs of C-face flakes side view at low b) and high c,d) magnification. The inset in d) represents a C-face flake-derived NRs.

The previously seen SEM micrographs of the C-face derived NRs in Fig. 8.8a were characterized by striations perpendicular to the length of the particles. The structure of the striations is similar to the lateral part of the flakes, which further supports the hypothesis of the second mechanism. Finally, an image analysis of the striation width in Fig. 8.10d, showed a good superposition of the values with 17 ± 4 nm of the flakes versus the 11 ± 3 nm of the NRs.

In the following paragraph, the surface chemistry of the nanoparticles obtained by sonication will be presented alongside the ball-milling particles.

8.3.3. Ball Milling of 4H-SiC C-face and Si-face Flakes

Another top-down approach to produce 4H-SiC-based particles from the electrochemically etched flakes is the ball milling technique. The features of the technique are discussed in paragraph 7.1. As previously studied for the sonication, it will be discussed the comparison between the C-face and Si-face flakes derived particles. Ball milling is not a suitable technique to produce nanoparticles especially when starting from a macrometric material as the flakes with an average dimension in the order of the centimeter. For this reason, it is possible to view the formation of microstructures formed by the agglomeration of portions of the loading material as displayed in the SEM micrographs of the C-face derived particles in Fig. 8.11a after further sonication for 2 h. The high porosity with nanometric pores seen on the flakes seems to be completely lost with only the presence of micropores as visible in Fig. 8.11b in contrast with the nanopores of the flakes. The ball-milled particles out of C-face flakes were also sonicated for 24 h. The expressed effects are the reduction in particle dimension (Fig. 8.11c) and the release of filaments or wrapped sheets as highlighted in the red circle of Fig. 8.11c and focused in Fig. 8.11d.

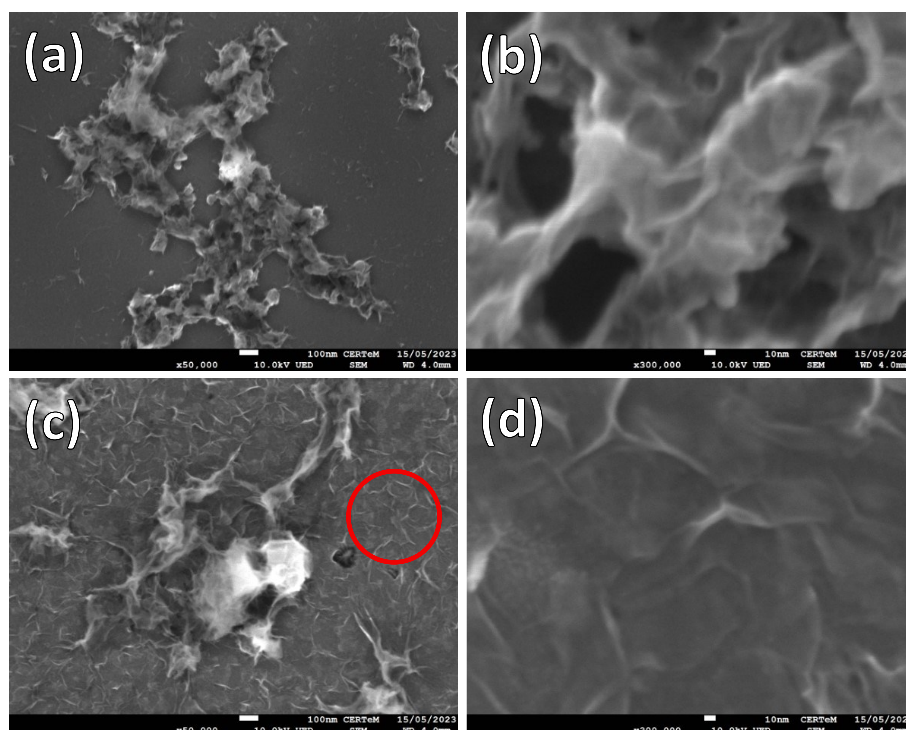


Fig. 8.11 SEM micrographs of ball milled flakes of 4H-SiC C-face after a,b) sonication at 2 h and c,d) after sonication at 24 h.

As a replication of the NPs produced by sonication, it is possible to see a difference in particle structures by switching to the Si-face. More compact particles were produced after ball milling and sonication for 2 h as shown in Fig. 8.12a. The compact particles result even less porous as

noticeable from the high-magnification SEM micrographs in Fig. 8.11b. Further sonication for 24 h produces still agglomerated micrometric particles (Fig. 8.11c and Fig. 8.11d) with lower dimensions than the relative C-face derived particles.

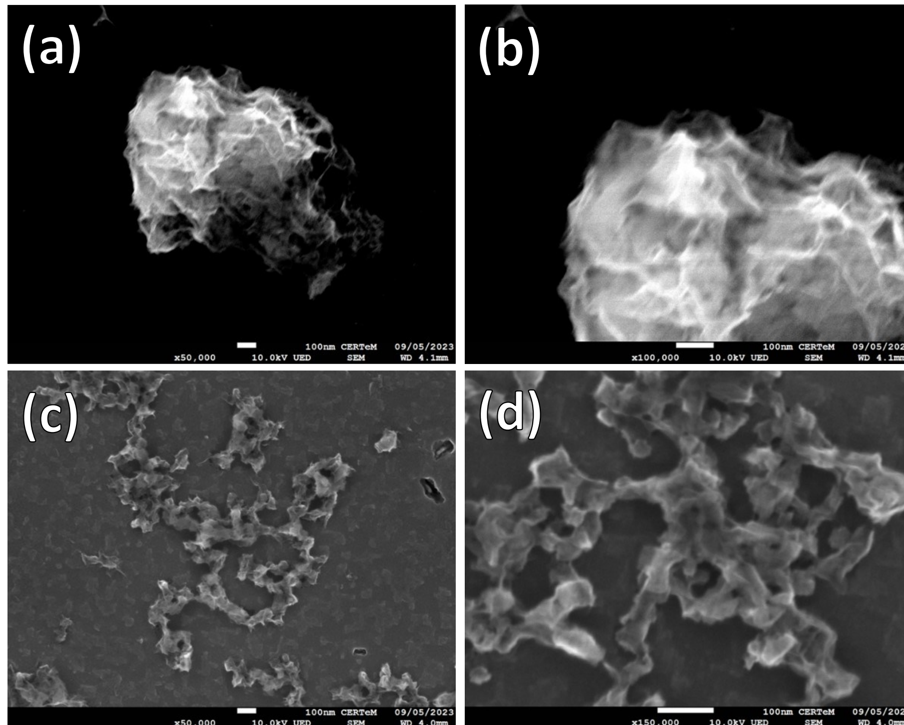


Fig. 8.12 SEM micrographs of ball milled flakes of 4H-SiC Si-face after a, b) sonication at 2 h and c, d) after sonication at 24 h.

The AFM analysis also revealed a bigger size for the ball-milled C-face flake particles (Fig. 8.13a) compared with the Si-face in Fig. 8.13b. The height of the particles decreases slightly from the C-face (147 nm) to the Si-face (50 nm). However, the lateral mean spacing of the particles is similar when comparing the C-face and the Si-face, as shown in Tab. 8.8. The result suggests that the agglomeration process is more governed by the ball milling process instead of the loading material.

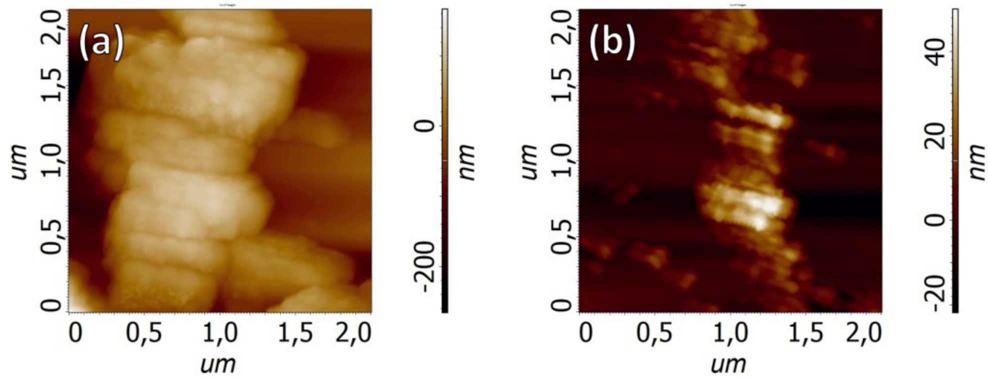


Fig. 8.13 AFM images of 4H-SiC of a) C-face and b) Si-face ball milled flakes after sonication for 24 h.

	PtP (nm)	Mean spacing (nm)
4H-SiC C-face	147	119
4H-SiC Si-face	50	93

Tab. 8.8 AFM section analysis of 4H-SiC C-face and Si-face ball milled flakes after sonication for 24 h.

Finally, the surface elemental analysis by XPS technique revealed some differences between the two top-down methods investigated: sonication and ball milling, taking into account the C-face flakes. The elemental percentages are reported in Tab. 8.9 shows a very low carbon content for the sonicated flakes compared to the higher percentage of silicon and oxygen. A more normalized distribution of elemental percentages was observed for the ball-milled C-face flakes. In particular, the ball milling method is able to transfer some elements from the bowl and the balls to the final products [235,236]. In the present work, the bowl and balls made of WC + Co were adopted to overcome the hardness of 4H-SiC. As shown in Tab. 8.9, W and Co elements were detected with percentages of 1.42 and 2.09%, respectively. Moreover, the higher percentage of carbon than the sonicated NPs could be attributed to the transfer effect from the ball milling environment to the final product. The ball-milled particles have a high concentration of carbon and oxygen compared to the sonicated ones. The evidence comes from the higher C/Si and O/Si ratios as shown in Tab. 8.9.

	C%	Si%	O%	W%	Co%	C/Si	O/Si
C-face sonication	10.64	44.69	44.67	NA	NA	0.24	1
C-face ball milled	30.26	23.63	42.60	1.42	2.09	1.28	1.8

Tab. 8.9 XPS elemental composition of 4H-SiC C-face sonicated and ball-milled flakes.

The ball milling approach is not suitable for producing nanosized particles. However, certain applications require micrometric particles with particular shapes and mechanical features. Particles of 4H-SiC are employed in alloy surface modification [237], grain refinement [237], and as additives in alloys [238,239].

8.4. Conclusions

In the present work, electrochemical etching was effective in producing porous material called flakes in this work. The etching was performed on both silicon and carbon surfaces. The flakes were analyzed on the morphological side by SEM and AFM techniques along with surface chemical analysis by XPS analysis. The exceptional porosity was also confirmed by BET analysis.

The flakes were additionally treated by sonication or ball milling to produce micro and nano-sized particles following a top-down approach. Herein, different morphologies and dimensions were obtained according to the faces by which were derived the flakes and the methodology of particle production. The produced particles were analyzed by SEM, AFM techniques, as well as XPS and DLS methods.

The flakes sonication gave nanosized particles with diverse morphologies according to the different faces of 4H-SiC subjected to ECE attack. Different mechanisms of particle production were hypothesized. The ball milling approach on SiC flakes led to the production of microsized particles. Some filaments or nanosheets were visible from SEM micrographs, providing future prospects for investigations.

9. Summary

The study of some of the 4H-SiC trench MOSFET device development has been central to this doctoral thesis. The investigations of some of the early stages of the device's fabrication were conducted by adopting different characterization techniques. The morphological part was studied via SEM and AFM techniques. An internally developed method of image analysis has been used to investigate some morphological variations on the trenches' walls. The elemental and chemical surface analysis was performed via EDX and XPS.

The first early stage of the device development involved the annealing of the 4H-SiC epi-layer with the aim of activating the dopants in the lattice after ion bombardment. The required high-temperature annealing at 1700 °C has made necessary the deposition of the C-cap layer. It has been revealed that the use of this surface protection approach is highly effective and convenient due to the necessity of common resources and facilities within the semiconductor industry. The C-cap method has been proven to be effective since no increase of roughness has been detected, as instead revealed in the absence of the carbonaceous layer.

The epi-layer doping is followed by the realization of the trenches via DRIE. Despite the dry etching technique optimization, the formation of striations on the walls of the trenches was observed. A first dry approach was chosen to lessen the striations and try to recover the walls' atomical flatness which is typical of 4H-SiC. The combination of H_2 gas etching and sacrificial oxidation was revealed to be effective for the purpose. The optimization of fundamental physical variables via DOE and RSM was supported by the image analysis method by which it has been possible to estimate the trenches' walls' roughness. The image analysis method produced precious numerical data to implement in the optimization study. An astonishing final RA value of 0.4 nm was determined, confirming the actual flattening of the walls.

Another study involved the use of wet chemical approaches. EDX and XPS analysis performed on the trenches suggested the presence of elemental Si, which is easily etched in a mixture of HNO_3 and HF. The traditional wet chemical attack was effective in removing the Si-Si moieties but the striations remained, and only a little decrement in trench walls roughness was detected.

The etching process was subsequently carried out in a wet environment with the introduction of the MACE technique. It is a relatively new approach used on 4H-SiC. Different chemical and fundamental variables were manipulated to minimize the walls' striations and analyze the response of 4H-SiC to this etching technique. The lowest roughness value obtained was 0.7 nm demonstrating the feasibility of the MACE technique to lessen surfaces.

The ECE was the last approach to be adopted for surface smoothing. It was utilized to operate within an electropolishing regime that achieves low etch rates and low surface roughness. Physical and chemical parameters were varied to achieve the lowest surface roughness possible. Due to sample features, the trenches walls' electropolishing was impracticable since the trenches were not doped in the employed samples. Various attempts were made employing different ECE conditions, and the lower measured surface roughness was as low as 0.4 nm by maintaining an etch rate of 2.3 nm/min.

The ECE technique was adopted also to investigate the feasibility of 4H-SiC Si- and C-faces to produce porous materials at a high current density regime. The results were the production of porous flakes, with high porosity corroborated by BET analysis. Furthermore, the flakes were sonicated or ball milled obtaining micro- and nano-particles valuable in many applications such as medicinal and catalysis.

This doctoral thesis exhibits some 4H-SiC issues that arise during its manipulation for microelectronics applications. The 4H-SiC is commonly etched via dry technique although this dissertation offers insights into many methodologies of massive and fine etches in both dry and wet environments.

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Appendix: Characterization Techniques

Atomic Force Microscopy (AFM)

The AFM technique is one of the Scanning Probe Microscopies (SPM). It uses the intermolecular forces, mostly of Van der Waals, between the probing tip and the sample surface. The tip is below the so-called cantilever as shown in Fig. 0.1. The probing tip can be of different shapes and materials according to the purpose of the measurements. For morphological investigation, the most common and cheap tip is made of polySi. The tip interacts with the surface causing the bending and twisting of the cantilever. Its movement is detected by a laser that is reflected by a gold plate on top. Finally, the laser deflection due to the cantilever bending and twisting is detected by a photodiode.

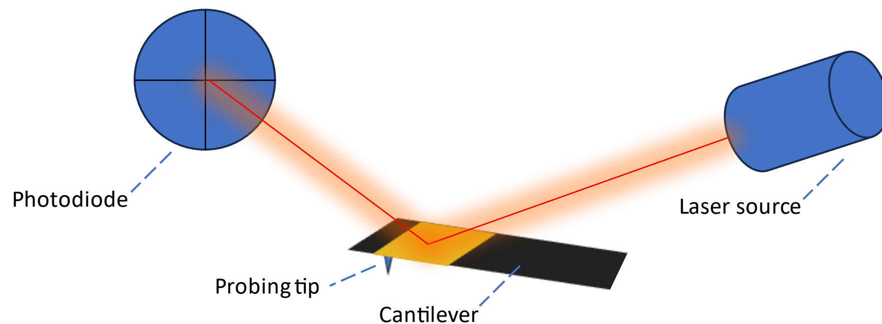

Fig. 0.1 Schematization of AFM instrument.

Small areas of the samples of a few μm^2 are scanned with a high resolution. This was made possible thanks to the implementation of piezoelectric. The typical working modes are noncontact, semicontact, and contact. Each mode has its own features and it is more suitable for specific sample typology. The most suitable mode is the semicontact.

Scanning Electron Microscopy (SEM)

SEM technique permits to study the structure, morphology, phase, and compositional distribution of the material's surface. Thanks to complex instrumentation, it is possible to magnify an object up to the nanometer order of magnitude. The classic laboratory microscope uses the light in the visible region to observe objects, but according to Abbe's equation (Eq. 0.1) the wavelength (λ) limits the resolution (d) due to the direct proportion. The resolution of laboratory microscopes stops at the micrometer order of magnitude.

$$\mathbf{d = 0.612 \frac{\lambda}{n} sen\alpha} \qquad \textbf{Eq. 0.1}$$

The SEM uses an electron beam with energy between ten and thousands of keV. The primary ray hits the sample's surface starting a multiple interactions phenomenon:

- Emission of Secondary Electrons (SE)
- Emission of BackScattering Electrons (BSE)
- Emission of characteristic X-Ray

The secondary electrons originate from the inelastic interaction between the primary beam electrons and the sample electrons. This collision facilitates the transfer of energy, causing the sample electron to depart from the atom and surface, becoming visible. The SE are useful to investigate the sample surface morphology since they guarantee information from the top part of the material.

Further interaction is the result of elastic collisions between the primary electrons and the atoms of the material. The resultant BSE are the results of a change in the trajectory of the primary electrons. The elastic interaction and BSE energy are strongly dependent on the atomic number. The pieces of information acquired by BSE permit the investigation of eventual phase heterogeneity.

The micrograph generation is the result of the conversion of the detected electrons (SE or BSE) energy in grayscale. The SEM images are bidimensional and offer a prospect of the third dimension thanks to the differences in grayscale intensity point by point. The electron brush coming from the source scans a small portion of the sample according to the desired magnification.

The SEM technique is primarily applicable to conductive specimens, as extracting electrons from a specimen generates a positively charged surface. This phenomenon results in distorted images with the presence of stripes and artifacts.

Energy Dispersive X-Ray (EDX)

EDX instrument is generally implemented in SEM machines. The X-Rays emitted after the interaction of the SEM primary electrons are characteristics of the element that constitutes the material. Each element has characteristics of X-Ray energies according to the most probable transitions between the shells. The mechanism starts with the extraction of an electron from an atom caused by one of the primary electrons. The phenomenon left a vacancy in the orbital which is promptly filled with an electron of the same atom at higher energy. The transition has the result of the characteristic X-Ray emission since the differences in energy between two orbitals if fixed. The typical X-Rays for each element are well known and available.

X-Ray Photoelectron Spectroscopy (XPS)

The XPS technique is based on Einstein's photoelectric observation. Electrons can be emitted from a material only if stimulated with an appropriate energy. This energy is characteristic of the elements which constitute the sample. The XPS instrumentation is able to detect the kinetic energy (KE) of the emitted electrons after stimulation with X-Rays of energy (hν). The Binding Energy (BE) is the real parameter that is taken into account in element recognition and it is obtained starting from Eq. 0.2, while the working function (Φ) is dependent on the investigated material.

$$\mathbf{KE = h\upsilon - BE - \phi} \qquad \textbf{Eq. 0.2}$$

The electrons that come out from the surface have a really low mean free path, making the XPS technique a surface investigation analysis with a sampling depth of a maximum of 10 nm. Each element is characterized by different BEs associated with different external orbitals. Electrons in the external orbitals are less energetic and more easily removable than the electrons in the core. XPS is useful in elemental qualitatively and quantitatively elemental analysis but also in surface chemical investigations. The detection of slight energy shifts of BE is associated with specific chemical groups. The BE shifts are due to the shift of electronic clouds due to the bonding of different electronegative elements.

Dynamic Light Scattering (DLS)

The DLS is a powerful technique extensively used in the fields of materials science, biophysics, and chemistry. It is used in size, shape, and molecular weight analysis. The sample is solubilized or dispersed in a liquid medium. The technique is suitable for detecting molecules or particles within nanometers and micrometers. The sample is irradiated with a laser beam while a detector measures the variation of the scattered light intensity over time. The scattering is due to the Brownian motion of the specimens. A theory and equations permit the conversion of scattering light intensity variations in specimens' mean size and distribution.

UV-Vis Spectroscopy

UV-Vis spectroscopy is a highly versatile technique based on the extinction of light as it passes through a medium. The decrease of light intensity expressed in percentage is called transmittance (Eq. 0.3) with I_0 the incident intensity and I the residual intensity after the extinction.

$$\boldsymbol{T}(\%) = \frac{\boldsymbol{I}}{\boldsymbol{I_0}}\ \mathbf{100} \qquad \textbf{Eq. 0.3}$$

The UV-Vis instruments generally scan in the range of wavelength between 190 and 800 nm. The full scan includes all the visible and the near ultraviolet regions. UV-Vis spectroscopy could analyze liquids, solutions, and solids. In this doctoral thesis, the technique has been adopted for solid light extinction investigations. The technique is useful to estimate the entity of the increase of roughness due to the higher scattering. Moreover, the technique is suitable to detect the doping of the semiconductor.

Acknowledgments

The third and last degree has been full of great experiences. It allowed me to acquire valuable skills thanks to the unique approach of a doctoral course in Chemical Sciences of the Department of Chemical Sciences at the University of Catania. Congresses, schools, and seminars have contributed to enriching my background in Chemistry and Material Sciences with the possibility to view at large sight the unique world of Science. I take the opportunity to thank the coordinator of the doctoral course in Chemical Sciences Prof. Salvatore Sortino. Many thanks to Ms. Sabrina Tosto for her immense support during the three years of the doctoral experience, thanks to which every question was clarified and every problem was solved promptly.

A Ph.D. path could be more or less harder, but for sure it has been leaner thanks to my friends before than colleagues Alessia Distefano, Gabriele Travagliante, Claudia Sciacca, Dr. Massimiliano Gaeta, and last but not least Orazio Samperi. I thank also the rest of my colleagues of the XXXVI cycle of the Ph.D. course in Chemical Sciences.

I cannot express enough gratitude to my tutor and mentor, Prof. Maria Elena Fragalà, for her solid support and availability during my three years of Ph.D., as well as during my Bachelor's and Master's thesis experiences. Under her guidance, I had the privilege of exploring various subjects and materials in my research activities, thus enhancing my proficiency as a researcher.

The introduction to the research and development of microelectronic devices started with this precious opportunity of doctoral thesis with STMicroelectronics. Many thanks to all the colleagues of STMicroelectronics Catania for the great collaboration together which led to fantastic results. Thank you very much for the trust and the support received during the three years. Thank you again for the opportunity to work with such a challenging and fascinating material as 4H-SiC.

I thank all the colleagues from the PSI for their support and introduction to the ECE technique.

I'd like to thank the entire Porous Silicon Team at GREMAN Labs and all the people who work there for the immense support they've given. In particular, many thanks to Prof. Gaël Gautier for the trust in accepting me as a visiting researcher, to Prof. Thomas Defforge for the precious pieces of advice given to me, and to Prof. Brice Le Borgne for the great support. I also thank my colleagues Lisa Monnier and Bashar Al Chimali for letting me feel great at the workplace. A special thanks go to Dr. Irene Carrasco Ruiz, the experience would have not been the same. Thank you for the incommensurable support, making me settle immediately at the workplace, I would never thank you enough.

I conclude to thank my parents, for their presence and support in these years.