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# Power Switching Converters with very low power consumption and high efficiency for energy savings

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# Chapter 1

Defining the objectives of the research

# 1. Introduction

The objective of this research is the analysis of power switching converters with targets of very low power consumption and high efficiency for being used in new system for energy savings.

Typically, they are implemented as Switching Mode Power Supply (SMPS) modules in different type of applications in both consumer and energy businesses.

In particular have been considered power supply systems with output power in the class of low and medium power, in the range from few watts up to hundreds watts.

Referring to consumer business, the main fields of application are lighting and home appliances where in the last years the international Agencies and Governments have been focused their attention to ask for reducing the continuous energy waste.

Therefore, more restricted and challenging constraints have been fixed in order to reduce the energy waste and to improve the level of performances of new products, that pushed the introduction of new technologies and new design solutions.

In particular in the lighting applications the improvement in LED technologies is leading to the development of LED lamps with higher light efficiency and lower power consumption.

Appropriate electronics circuits are used in order to make the LED supply compatible with energy that is provided by the electrical main, 230 VAC @ 50 Hz. Thus a low DC voltage drives a small number of LED diodes in series connection. The most important requirements of the power converters for LEDs is a low ripple current, because it may cause changes in the light emitted from the diode (flickering). Also important are low power losses, high power factor and dimming capability.

The analysis will start making an overview of the principal topologies of switching converters used to drive the LED bulbs. Advantages and disadvantages will be shown for each topology. Then the flyback topology will be analyzed and discussed in more details, since it is considered the most promising one. Finally, an alternative schematic will be proposed in order to increase the electrical performance of the whole power conversion system.

On the other side in the home appliance applications there are conditions where the energy is consumed by the device when this does not work or does not perform its main functions and that happens without the final user realizing it. One condition is when the device is put in standby status.

For this case the analysis of the commonly used techniques for reducing power consumption in the switching converter is discussed and a new technique for reducing power during the inactivity state of the appliance system is proposed.

The proposed solution works on the feedback network, introducing a perturbation on the feedback signal: in this way the main power transistor, in the converter, is switched off and the output voltage of the converter is settled to zero. This solution allows an important reduction of the effective power consumption of the system.

In order to confirm this solution an auxiliary SMPS with output power of 5 W to supply the user interface of a washing machine has been designed, and the converter topology used is a Flyback converter, compliant with the current regulations of the home appliance applications.

In addition a prototype is realized and then simulations in PSpice, thermal and electrical measurements are performed in order to verify the operations of the converter in different environmental and electrical conditions.

Looking at the business of energy conversion, in the design of applications of high power systems an important issue is to provide low voltages, in the range of tens of Volt, tapping from high voltage input line, which is usually in the range between hundreds of Volt to kilovolt, by means of switching power supplies. Low voltages are needed to supply the logic control circuits and the power semiconductors driving the applications. The supply system has to deal, consequently, with both wide input voltage range and electrical insulation. The evaluation of the operative conditions of a driving system for IGCT devices, used in a transmission system application with wide input voltage range, is described. The design of a 100 W supply converter is shown considering all the issues related with the series connection of power devices and the needs of insulation.

Converter design, modelling and experimental results are shown together with the evaluation of the efficiency of the proposed solution.

# Chapter 2

Sustainable development

## 2. Introduction

The earth is suffering more and more from the damage due to the pollution resulting from the use of fossil fuels for energy production.

The most important portion of consumption of the natural resource and energy in the Community is due to the products energy consumption. Also these products provide a number of other important environmental impacts and for these reasons as well as to make more widespread use of renewable energy sources, is important to learn how to save energy.

In particular, the electricity demand is characterized by a fast growth and it is forecasted to growing over the next 20-30 year, in absence of a policy to counteract this trend. Developed countries are the most responsible ones both for the pollution and the depletion of energy resources because, with 25% of the world population, they consume each year over 75% of the available energy. For this reason it is very important to sensitize not only the industry, but also consumers in industrialized countries.

The energy that is used for civil use (non-industrial) is approximately 20% of that consumed in total; exists therefore a large amount of energy that can be spared. However, without making strong sacrifices, and simply changing the daily behaviour, it has been estimated that a family could save:

- 15% of heating costs
- More than 10% of cost for household appliances
- 20% of cost for gasoline

For the majority of product categories available in the Community market can be observed very different levels of environmental impact, although their functional performances are similar.

In order to promote the sustainable development a continuous improvement in the overall environmental impact of those products should be encouraged, in particular identifying the major sources of negative environmental impacts and avoiding the transfer of pollution, when this improvement does not involve excessive costs.

The eco-design of products is a crucial factor in the community strategy that is finalized to the improvement of the environment performance of products and in the same time to keep the quality for the manufacturer, consumer and the society on together.

The improvement of the energy efficiency, which includes the most efficient use of the electricity, is considered a very important contribution in order to achieve the goals of emission reduction of the greenhouse gases in the Community.

It is needed acting as soon as possible in the design phase of a product that consumes energy (EuP), in order to define and control the level of pollution caused during the life cycle of the product and to find solutions to reduce that during this stage when most of the costs are taken up.

For this purpose, the Directive 2005/32/CE seeks to achieve a high level of prevention by reducing the potential environmental impact of the energy-using product, this results a benefit for the final consumers [1].

Furthermore, the Directive provides the setting of requirements which the energy using products, covered by implementing measures, must fulfil in order to be placed on the market and / or putting them in service.

It contributes to the sustainable development by increasing the energy efficiency and the level of environmental protection, and in the same time improving the security of energy supply.

## 2.1. Energy waste and power consumptions.

There are situations in which the energy is used even if the user doesn't realize it. One of these is just leave the device in stand-by mode.

Energy is the average power multiplied by the time. Electrical energy is generally expressed in watt-hours or kilowatt-hours. Energy can also be expressed in joules.

One watt is the rate of energy consumption of 1 J/s and 1 kWh is equivalent to 3.6 MJ. To convert power to energy (an annual energy consumption), the number of hours of operation in each mode must be assumed for a given period and the average power for each mode must also be known. As most appliances can operate in a number of modes and the usage patterns and profiles may considerably vary between countries, converting power values determined under this standard to energy is potentially fraught with difficulty.

In the simplest case, an appliance that has only a single mode of operation can be converted to annual energy value by assuming a constant power for a whole year.

A year has 8760 h (this ignores leap years), so an appliance that has say a constant standby power of 5 W (assuming that there is no use in other modes) would consume 43800 Wh per year or 43.8 kWh per year.

Annual energy consumption can be determined for more complex user patterns by the sum of power per hours of use for each mode during one year (hours 1 to 8760).

When the total energy consumption for a large appliance is being considered, it is necessary to know as a minimum the "on" mode time and energy consumption per cycle, an assumed number of uses (cycles) per year and the "standby" (usually off mode) power.

For example, a TV set in stand-by consumes typically about 8 W, in order to want to avoid unnecessary waste, it is always necessary to turn off the device with the on / off button. This behaviour, as mentioned above, leads to a significant reduction in fuel consumption and thus save energy for electricity generation.

Considering a daily usage of the appliance (TV) for 5 h/day, and then a state of stand-by time for 19 h/day, it is possible to estimate the consumption and consequently the wasted energy. For one year the uses hours of the appliance for each mode are respectively 1825 h for the usage and 6935 h for stand-by.

By considering a typical power consumption of 80 W, the power consumption in a year will be 146 kWh, which means that on average in the remaining hours the appliance is in stand-by mode, its power consumption will be equal to 55.48 kWh.

This simple analysis let us understand how the energy consumption for an unnecessary TV waiting is exactly more than 1/3 of the energy spent for the activity of interest.

Typically, the situations of waste of energy are closely tied to the low efficiency of the device, as in the case of incandescent lamps. The following Table 2.1 shows a comparison of the energy savings between light bulb fluorescent, traditional incandescent, and LED lamp.

Therefore, the table results shows that actually the best technology in the market is the LED lighting because it has about 6 times lesser power consumption than traditional incandescent light bulb. Also from an economic point of view, if it is considered an analysis in the short time the cost of the lamp is very high, about 27 time than traditional incandescent lamp, but if it is considered the life time of the LED lamp and the energy consumption, the total cost of the LED technologies is about 1/3 than the traditional light bulb.

Table 2.1

| Lamps |  Incandescent |  Fluorescent |  LED |
|---|---|---|---|
| Consumption (W) | 40 | 8 | 7 |
| Luminous Flux (lumen) | 410 | 420 | 400 |
| Life (hour) | 1000 | 8000 | 25000 |
| Cost Lamp(€) | 1,3 | 18 | 35 |
| Buying Cost per 25000 h of use (€) | 32,5 | 56,25 | 35 |
| Energy Cost per 25000h of use (€) | 120,00 | 24,00 | 21,00 |
| **Cost per 25000h (€)** | **152,50** | **80,25** | **56,00** |

Other typically example is a washing machine, that has a program time of 85 min and an energy consumption of 0.95 kWh per cycle and a standby power consumption (off mode) of 1.30 W. The annual energy consumption for 300 uses per year would be (assuming no use of delay start and assuming end of program power is equal to the standby power consumption):

Time in use = 85 x 300 ÷ 60 = 425 h per year;

Time in standby = 8760 - 425 = 8335 h per year;

Energy consumption in use = 300 x 0.95 = 285 kWh per year;

Energy consumption in standby = 8335 x 1.30 ÷ 1000 = 10.83 kWh per year;

Energy consumption total = 285.00 + 10.83 = 295.83 kWh per year

= 296 kWh per year (rounded to the near whole kWh).

# Chapter 3

Energy saving regulations

## 3. Introduction

Sustainable development requires careful consideration about the economic, social and health impacts of the measures envisaged. Improving the energy efficiency of products contributes to guarantee the assurance of energy supply, that is a requirements for a healthy economic activity and therefore of sustainable development, which aims is to reduce the environmental impact of products throughout of their entire life cycle.

In order to maximize the environmental benefits from improved design it may be necessary to inform consumers about the environmental characteristics and performance of energy-using products and to advise them how to use environmentally friendly product. Taking into account, in the design stage, the environmental impact of a product throughout its whole lifetime can facilitate environmental improvements and costs. May be necessary and justified to establish specific quantified requirements for the eco-design for some products or environmental aspects in order to ensure the minimum environmental impact.

Such measures can also contribute to promote a sustainable use of resources and constitute a major contribution to the ten-year framework of programs on sustainable consumption and production, agreed at the World Summit on Sustainable Development in Johannesburg in September 2002.

As a general principle, the energy consumption of energy-using products in stand-by or off-mode should be reduced to the minimum necessary for their proper functioning. For this purpose, will be taken as reference the best-performing products or technologies available on the market, and the level of specific eco-design requirements should be established on the basis of technical, economic and environmental analysis.

## 3.1. Reference to the regulation on the Appliance field

In the recent past, the consumption of appliances in stand-by in Europe just in 2005 alone reached some 47 TWh equivalent to more than 19 MT of $CO_2$ emissions [2].

In order to reduce the waste of energy and ensure a sustainable development, the European Union issued a regulation in late December 2008, the Commission established clear limits to the consumption of household appliances in standby or off mode.

Since 2010, one year after the entry into force of the regulation, which implements Directive 2005/32/EC applicable to equipment sold in Europe in off mode or standby may

not exceed 1 W of input power, 2 W in case in which in the stand-by mode provides information about the status of the machine via a display. These limits of consumption, in 2013 will be further reduced by halving the threshold.

In particular the extent permitted by law, provide for the following energy consumption in Watts (rounded to two decimal places)

- From January 7, 2010: Off Mode consumption should not be more than 1,00W

- From January 7, 2010: In Standby Mode must not be greater than 1,00W, and 2,00W if in the display are shown data or status information.

- From January 7, 2013: Off Mode consumption should not be more than 0,50W

- From January 7, 2013: In Standby Mode must not be greater than 0,50W, and 1,00W if in the display is shown data or state information

The Stand-by/off mode is applied across a wide range of products which fall within the EuP (Energy-using Product), as shown in Tables 3.1, 3.2, and 3.3.

Table 3.1

| Appliances | |
|---|---|
| Washers | Dryers |
| Dishwasher | Cooking appliances |
| Electric ovens | Electric hot plates |
| Microwave ovens | Toaster |
| Fryers | Grinders |
| coffee machines and electrical equipment for opening or sealing containers or packages | Electric knives |

Table 3.2

| Information technology equipment intended primarily for use in the home and consumer equipment: | |
|---|---|
| IT equipment | Radio equipment |
| Television sets | Camcorders |
| VCRs | Hi-fi |
| Audio Amplifiers | Systems "home theatre" |
| Musical Instruments | Other equipment for recording or reproducing sound or images, including signals or other technologies for the distribution of sound and image than by telecommunications |

Table 3.3

| Toys and equipment for the leisure and sports | |
|---|---|
| Electric trains or tracks for electric toy cars racing | Portable game console |
| Sports equipment with electric or electronic components | Other toys and equipment for the leisure and sports |

### 3.1.1. Measurement's method of power consumption – EN62301

The International Standard EN 62301 specifies methods of measurement of electrical power consumption in standby mode. It is applicable to mains powered electrical household appliances and to mains powered parts of appliances that use other fuels such as gas or oil [3].

The objective of this standard is to provide a method of test to determine the power consumption of a range of appliance and equipment in standby mode (generally where the product is not performing its main function), this standard define "standby" mode as the lowest power consumption when connected to the mains. The test method is also applicable to other low power modes where the mode is steady state or providing a background or secondary function (e.g. monitoring or display). This standard does not

specify safety requirements. It does not specify minimum performance requirements nor does it set maximum limits on power or energy consumption.

### 3.1.1.1. Subject of the regulation

The Standby mode is the lowest power consumption mode which cannot be switched off (influenced) by the user and that may persist for an indefinite time when an appliance is connected to the main electricity supply and used in accordance whit the manufacture's instructions.

The standby mode is usually a non-operational mode when compared to intended use of the appliance's primary function. The definition of standby mode in this standard is only applicable to the determination of standby power or standby energy consumption under this standard.

Tolerances and control procedures

The tolerance and control procedures shall be according to the following two cases:

- power consumption greater than 1 W.

- power consumption less or equal to 1 W.

In the first case, the standby power determined according to this standard on the first appliance shall not be greater than the value declared by the manufacturer plus 15%.

If the result of the test carried out on the first appliances is greater than the value declared plus 15% the test for standby power shall be carried out on a further three appliance, which shall be randomly selected from the market.

The arithmetic mean of the values of these three appliances for the standby power shall not be greater than the declared value plus 10 %.

In the second case, the standby power shall not be greater than the value declared by the manufacturer plus 0.15 W.

If the result of the test carried out on the first appliance is greater than the declared value plus 0.15 W, the test shall be carried out on a further three appliances, which shall be randomly selected from the market. The arithmetic mean of the values of these three appliances shall not be greater than the declared value plus 0.1 W.

Regarding the power measurement accuracy, the measurements of the power of 0.5 W or greater shall be made with an uncertainty of less than or equal to 2 % at the 95 % confidence level. Measurement of power of less than 0.5 W shall be made with an uncertainty of less than or equal to 0.01 W at 95 % confidence level. The power measurement instrument shall have a resolution of:

- 0.01 W or better for power measurement of 10 W or less;

- 0.1 W or better for power measurements of greater than 10 W up to 100 W;

- 1 W or better for power measurements of greater than 100W.

For appliance connected to more than one phase, the power measurement instrument shall be equipped to measure total power of all phase connected.

Where the current waveform is a smooth sine wave in phase with the voltage waveform (e.g. in a resistive heating load), there is no harmonic content in the current waveform. However, some current waveforms associated with low power modes are highly distorted and the current may appear ad a series of short spikes or a series of pulse over a typical a.c. cycle.

This effectively means that the current waveform is made up of a number of higher order harmonics which are multiple of the fundamental frequency (50 Hz or 60 Hz). Most digital power analysis will have no problem with the accurate measurement of recommended current harmonics presented by low power modes. However, it is recommended that a power instrument should have the ability to measure harmonic components up to at least 2.5 kHz. Note that harmonic components greater than the 49th harmonic (2459 Hz) generally have little power associated with them. As a rule, the scanning frequency of a power measurement instrument should be at least twice the frequency of the highest order harmonic that has significant power associated with it.

About the supply voltage waveform, where the test voltage and frequency are not defined by an external standard, the test voltage and test frequency shall be in agreement to the data of Table 3.4:

Table 3.4

| Source | Voltage | Frequency |
|--------|---------|-----------|
| SINGLEPHASE | 230 V ± 1% | 50 Hz ± 1% |
| THREE-PHASE | 400 V ±1% | 50 Hz ±1% |

The total harmonic content of the supply voltage when supplying the appliance under test in the specified mode shall not exceed 2 % (up to and including the $13^{th}$ harmonic); harmonic content is defined as the root-mean-square (r.m.s.) summation of the individual components using the fundamental as 100 %.

The ratio of peak value to r.m.s. value of the test voltage is to define as crest factor (i.e. crest factor) shall be between 1.34 and 1.49. For a sinusoidal waveform the crest factor is 1,414, while for a dc voltage it is 1.0.

Under normal conditions it is assumed that the waveform of the input voltage will remain generally sinusoidal, when supplying small loads in stand-by, so the parameter of particular interest from the side of measurement is the current and its waveform.

### 3.1.1.2. Procedures of measurements

The Standards define the criteria of measurement of the power consumption in different operation modes. Power consumption may be determined:

- Where the power value is stable, by recording the instrument power reading; or

- Where the power value is not stable, by averaging the instrument power readings over a specified period and dividing by the time.

Tests in this standard are to be performed on a single appliance. The appliance shall be prepared and set up in accordance with the manufacture's instruction, except where these conflict with the requirements of this standard. Where the selected mode is stable.

This methodology may only be used where the mode and measured power are stable. A variation of less than 5 % in the measured power over 5 min is considered stable for the purpose of this standard. Instrument power readings may be used in this case.

Connect the product to be tested to the metering equipment, and select the mode to be the measurement. After the product has been allowed to stabilize for at least 5 min, monitor the power consumption for not less than an additional 5 min. if the power level does not drift by more than 5 % (from the maximum value observed) during the latter 5 min, the load can be considered stable and power can be recorded directly from the instrument at the end of the 5 min.

All other measurements methodology shall be used where either the mode or measured power is not stable. However, it may also be used for all stable modes and is the recommended approach if there is any doubt regarding the behaviour of the appliance or stability of the mode. Average power readings or accumulated energy over a user-selected period are in this case.

Connect the appliance (equipment) to the metering equipment. Select the mode to be measured (this may require a sequence of operations and it may be necessary to wait for the equipment to automatically enter the desired mode) and monitor the power. Average power is determined using either the average power or accumulated energy approach outlined below.

a)    Average power approach: where the instrument can record a true average power over a user selected period, the period selected shall not be less than 5 min (except if there is an operating cycle – see below).

b)    Accumulated energy approach: where the instrument can accumulate energy over a use selected period, the period selected shall not be less than 5 min (except if there is an operating cycle – see below). The integrating period shall be such that the total recorded value for energy and time is more than 200 times the resolution of the meter for energy and time. Determine the average power by dividing the accumulated energy by the time for the monitoring period.

If the power varies over a cycle (i.e. a regular sequence of power states that occur over several minutes or hours), the period selected to average power or accumulate energy shall be one more complete cycles in order to get a representative average value.

In case of accumulated energy the integrating period shall be as described above.

### 3.1.1.3. Low power measurement

There are a number of problems associated whit power measurement of very small loads that are typically found in standby and other low power modes (typically less than 10 W). These mostly relate to the ability of the measurement instrument to respond correctly to current waveform that is presented. Key points for consideration are discussed briefly below.

In many low power modes, the current waveform is unlikely to be sinusoidal, so it is necessary to ensure that the meter has a scanning frequency that is sufficiently fast to capture the unusual current waveforms that are common (such as pulses or spikes). To determine the power, the meter has to multiply the instantaneous current and voltage values several hundred times per cycle. Most digital instruments accumulate these values and display an average power once or twice a second. It is important to note that the power of many products in low power modes will be less than 10 W (some will be very small). This is partly due to low current levels, but also, in some case, due to the current waveform being largely unrelated to the voltage waveform.

Other critical parameter of the measurement instrument is the crest factor, that is defined as the ratio of peak current to r.m.s. current (or peak voltage to r.m.s. voltage). In normal circumstances it is assumed that the voltage supply impedance will be such that the voltage waveform will remain generally sinusoidal in shape when supplying small standby loads, so the parameter of particular concern from a metering perspective is usually current and its waveform. During the measurement, it is critical that the crest factor capability of the meter is greater than the actual crest factor of the load, otherwise the peak value of the current will be "lopped off" and the integration for power will be incorrect. Most meters will have a rated crest factor stated for the rated input within each "range". Usually, the available crest factor will increase as the actual load becomes smaller relative to the rated input range selected. However, if the range selected is too large, the accuracy resolution of the measurement will became poor. Good meters will give an "out of range" reading if the available crest factor is exceeded. Note that crest factors for standby loads are typically 3 and can, in some circumstances, be as high as 10. Good instruments will provide guidance on how to deal with high crest factor loads while retaining measurement accuracy.

Depending on the power supply configuration and design, some small loads (such as those associated with standby) can draw asymmetric current, i.e. drawing current only

on either the positive or negative part of the a.c. voltage cycle. This is effectively a d.c. power load component supplied by an a.c. voltage supply. Most digital power analysers can adequately handle low frequency and d.c. components during a power measurement. However, it is not possible to undertake accurate measurements of this type of current waveform using any type of transformer input such as a current transformer – d.c. components are not visible through a transformer input. It is therefore critical that any power instrument use a direct shunt input to measure current. Rotating disk meter is unsuitable for any size load of this type because d.c. loads also exert a braking torque on the meter which creates further inaccuracies.

## 3.2.    Reference to the regulation on the Lighting field

The paragraph 2, article 16 of the Directive 2005/32/CE establish an executive measure on the lighting products. The mandatory requirements, regarding the argument of the eco-design, are applied at the product introduced in the Communitarian market everywhere these are installed or used, as in case of domestic lighting [4].

The European commission has performed a preliminary analysis of technical, environmental and economic aspects of the lighting product used in domestic ambient, and the result are shown in the web site EUROPA of the European Commission.

The subject products of this regulation are principally designed to total o partial lighting of a domestic ambient and replacement o complete the natural light with artificial light in order to improve the visibility of the environment.

The lamps for special uses, that are designed for other type of application as shown from the information attached on the product, for example for road signs or semaphore lights, are not regulated from this regulation.

The most important environmental aspects, of products covered in the regulation, are the energy during the operation phase, the content and emission of mercury over the different phases on its life cycle.

In this way, the use of the requirements in energy efficiency of the lamps subject of the regulation, will allow to reduce the global mercury emission.

Also, the target of the electricity consumption will be obtained using technologies that are no actual proprietary, efficient cost and to allow reducing the cost of buying and use.

In order to improve the environmental performance of products covered by this Regulation, should be established requirements for eco-design contributing to the functioning of the internal market and to the Community objective to reducing energy consumption by 20% within 2020 compared to estimated consumption for that year in the absence of measures.

Therefore, the regulation scope is also to increase the penetration in the market of the consumer energy product in this regulation, in order to reach the estimates saving of 39 TWh of energy in 2020 compared estimated consumption for that year in the absence of measures to promote eco-design.

The requirements of the eco-design from the point of view of user shouldn't influence the operation and to be negative for the health, safety or environment. In particular the advantage obtained from the use of the products, should compensate the possible environmental impact of the manufacturing phase.

Regarding the requirements of the eco-design, the lamps not directional for domestic use must fulfil the requirements on the following phases.

Phase 1: 1$^{th}$ September 2009

Phase 2: 1$^{st}$ September 2010

Phase 3: 1$^{st}$ September 2011

Phase 4: 1$^{st}$ September 2012

Phase 5: 1$^{st}$ September 2013

Phase 6: 1$^{st}$ September 2016

A requirement unless is replaced or unless otherwise stated, it continues to be applied jointly to those introduced in next stages.

Beginning from 1 September 2009: for the lamps with special use, the information should be shown in clear way and highlight in the box and in attached documents together the product the planned use and the indication that the lamps are not suitable for household room illumination.

The maximum power, $P_{max}$, for a specific luminous flux, $\Phi$, is shown in Table 3.5.

Instead, in Table 3.6 are resumed the exception for the maximum power.

Table 3.5

| Data application | Maximum characteristic power ($P_{max}$) for a characteristic luminous flux ($\Phi$) (W) | |
|---|---|---|
| | Clear Lamps | Not Clear Lamps |
| Phase 1 to 5 | $0.8 \cdot \left(0.88\sqrt{\Phi} + 0.049\Phi\right)$ | $0.24 \cdot \sqrt{\Phi} + 0.0103\Phi$ |
| Phase 6 | $0.6 \cdot \left(0.88\sqrt{\Phi} + 0.049\Phi\right)$ | $0.24 \cdot \sqrt{\Phi} + 0.0103\Phi$ |

Table 3.6

| Exception | |
|---|---|
| Range exception | Maximum power (W) |
| Clear Lamps 60 lm $\leq \Phi \leq$ 950 lm     in phase 1 | $P_{max} = 1.1 \cdot \left(0.88\sqrt{\Phi} + 0.049\Phi\right)$ |
| Clear Lamps 60 lm $\leq \Phi \leq$ 725 lm     in phase 2 | $P_{max} = 1.1 \cdot \left(0.88\sqrt{\Phi} + 0.049\Phi\right)$ |
| Clear Lamps 60 lm $\leq \Phi \leq$ 450 lm     in phase 3 | $P_{max} = 1.1 \cdot \left(0.88\sqrt{\Phi} + 0.049\Phi\right)$ |
| Clear Lamps with connector G9 or R7, phase 6 | $P_{max} = 0.8 \cdot \left(0.88\sqrt{\Phi} + 0.049\Phi\right)$ |

In other way, the power limit of the incandescent bulb manufactured from the phase 1 can't be exceed a maximum power of 80W (all lamps with greater power are banned), in the next phase the limit will goes down and the maximum power of lamps produced can't be exceed 65 W, up to phase 4 where the maximum power is 7 W. Beginning the first September 2013 all the incandescent lamps will be banned in the market

# Chapter 4

## Analysis of Power Converters for LED Lamps

# 4. Introduction

Today themes such as ecology, global warming, melting of ice, due to the increase of global temperatures and huge energy consumption worldwide, are a lot discussed [5]. In this context the application of LEDs for lighting use seems to meet the needs of the environmental respect, thus leading to even more massive use of these ones in various fields, especially in public and private lighting in order to obtain energy savings and long lifetime. Nowadays, the lighting designers search more and more for energy saving, and the luminous efficiency is a key parameter to get it, but this parameter should be aligned with other important parameters. The high luminous efficiency, exceeding 100 lm/W, makes the LEDs more competitive than traditional light sources. A light source has to be with even a suitable lifetime. In order to achieve a system with high performance in terms of efficiency, it is necessary to focus on the energy conversion aspect, which includes the switching converters used to drive the power LEDs. These circuits must meet several electrical features such as power factor, harmonic distortion, efficiency, dimming capability, reduced flicker, and specific field of temperature [6]. Often the input of the converters, which feds the LEDs, is an unregulated dc voltage obtained by rectifying the mains voltage. A dc-dc switching converter is then used to convert this input to a dc output controlled voltage having the desired level. A power conversion system having low power losses allows obtaining both high efficiency and small heat to be wasted.

In this chapter the main topologies of switching converters, which may drive the LED bulbs, will be discussed. Insulated and non-insulated topologies will be compared showing their advantages and disadvantages. In particular the flyback topology, which is actually used in many LED lamps on the market, will be taken into account. The flyback topology belongs to the category of dc-dc converters with insulation between the input and output. The insulation is achieved by means of a transformer, which works at the switching frequency. An analysis of the power quality, such as power factor (PF) and total harmonic distortion (THD) will be discussed with reference to their sensitivity on the change of the converter parameters. Finally, an alternative topology will be discussed, with the aim of improving the electrical performance of the conversion system.

## 4.1. Improvement of LED technologies

The light-emitting diodes (LEDs) are *pn* junctions, which may emit radiations in the ultraviolet, visible, and infrared range if they undergo an appropriate bias. In particular, the LED emitting radiation in the visible spectrum will be considered [7]. They have multiple applications to transmit information to the human users from electronic instruments and other equipment. The light effectiveness in stimulating the vision depends on the sensitivity of the human eye, which is a function of wavelength (Figure 4.1). The maximum sensitivity, $V(\lambda)$, of the human eye to light is at a wavelength $\lambda = 0.555$ μm.

If we consider the relative sensitivity of the eye equal to 1 at $\lambda=0.555$ μm, which means $V(0.555$ μm$)=1$, then we can say that $V(\lambda)$ decreases approximately to zero at the extremes of the visible spectrum $\lambda=0.77$ μm and $\lambda=0.39$ μm. The human eye is able of absorbing radiation having energy (*hv*) approximately equal to 1.7eV. In the choice of semiconductor for the LED realization, only those with bandgap energy higher than 1.7 eV will be considered.

The semiconductors may be divided into types, direct and indirect ones. In a direct semiconductor a minimum of the conduction band is directly upon the maximum point of the valence band, as show in Figure 4.2 in the energy/moment plane. Differently, in indirect semiconductors, the minimum of the conduction band is not direct upon the maximum of the valence band (Figure 4.3).
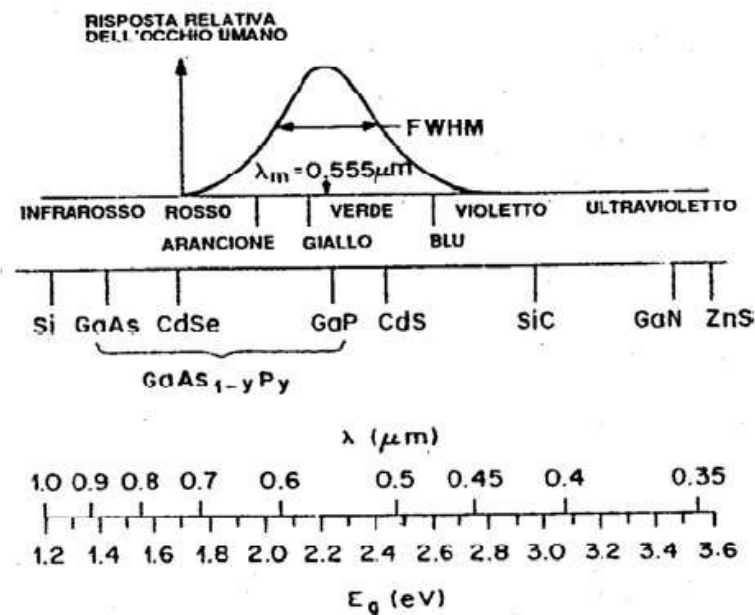


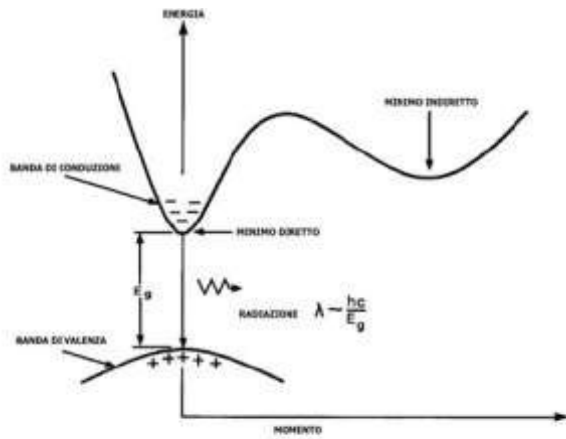Figure 4.1: Sensitivity of the human eye.

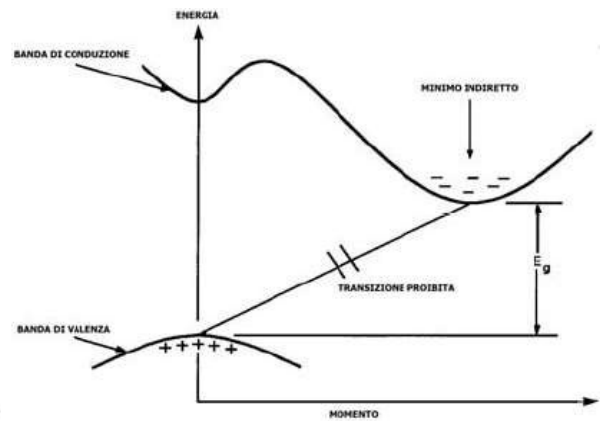Figure 4.2: Energy band structure of a semiconductor with emit radiations.



Figure 4.3. Energy band structure of a semiconductor without emit radiations.

Due to this differences physical structures, the direct semiconductors emit radiation than the other one. In the indirect semiconductors the recombination process between electrons and holes occurs without radiation emission and for this reason, the semiconductors used on the LEDs manufacture are of direct type [7][8].

Therefore, when the electron goes from $E_2$ level to $E_1$ level, the energy produced in form of radiation is equal to the product between $h$ and $v$, where $h$ is the Plank constant $(6,62 \cdot 10^{-34}$ Js$)$ and $v$ is the frequency of the emit radiation:

$$v = \frac{E_2 - E_1}{h} \rightarrow \lambda = \frac{ch}{E_2 - E_1}$$

Eq. 4.1

The difference between two levels comes from the doping of the semiconductor material. The exact choice of the semiconductor determines the peak of the photons wavelength and thus the colour of the light. Unlike the incandescent lamps that emit a continuous spectrum, an LED emits almost monochromatic light of a particular colour.

## 4.2. Survey of the power converter topologies

Actually, many applications of LEDs exist on the outdoor and indoor lighting market. Traffic lights, street lighting, braking markers in cars, billboards with variable messages, backlighting for display are non exhaustive examples of LED use. However, all these solutions have as a disadvantage the high cost, thus preventing large scale diffusion for lighting applications. The power converter used as driving circuit is an important aspect too, since it contributes to the final cost of the system. An important feature of a power converter driving LED strings is a low current ripple looking to avoid variations of the light level emitted from the diode (flickering). Also important are low power losses, high power factor, dimming capability.

### 4.2.1. Insulated topology

The insulation from the electrical main may be realized by transformers. They allow to change the ratio between the input voltage and the output voltage and furthermore, two or more independent outputs.

### 4.2.1.1. Flyback converter

The input of a flyback converter is an unregulated DC voltage, obtained by rectifying the mains voltage, and the output is a DC voltage controlled at the desired level. In general, in a power conversion system it is important to achieve low power losses in order to have both high efficiency and to contain the heat to be wasted. The circuit model of the converter is shown in Figure 4.4.

The flyback converter may work in discontinuous conduction mode (DCM) that means the current at the secondary winding vanishes before the next closure of the switch (complete demagnetization of the transformer). This implies that the primary current will start from zero in the next cycle. If instead, the current in the secondary has a non-zero value at the end of the period (partial demagnetization), also the primary current will start from a non-zero value, and in this case the converter works in continuous conduction mode (CCM).
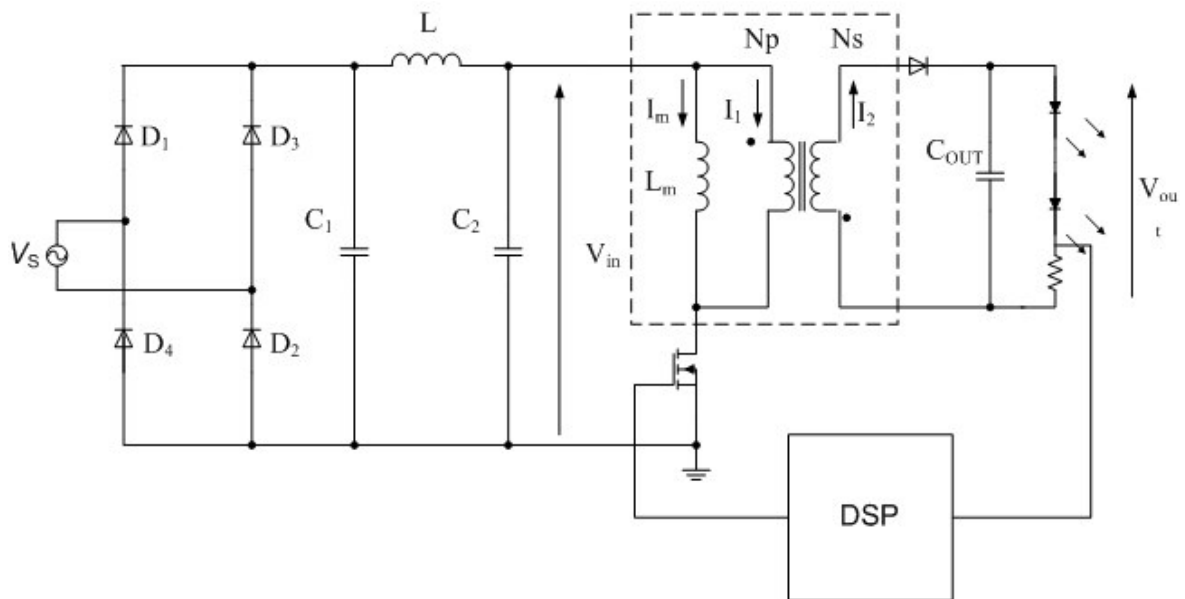
Figure 4.4: Schematic of a flyback converter.

In DCM the waveform of the secondary current is a triangular wave, while in CCM is a trapezoidal one. When the converter works in the boundary condition between CCM and DCM, or rather when the current in the secondary vanishes at the end of the switching cycle, then this mode is said transition mode (TM). In the subsequent analysis of the converter the operation mode taken into account is the TM [9]. Some advantages of such a mode of operation are related to the energy stored in the magnetic field, and to the reduced effects of the parasitic inductances. In fact, at operations with equal power, DCM leads to a higher peak current on the primary than CCM, thus causing more losses due to the parasitic elements. Also the need to use a transformer with a higher value of saturation current arises. In order to improve the efficiency, in case of applications with low output voltages where it is necessary to minimize the voltage drops in the devices, a Schottky diode is used. In the following it is shown the sizing of the flyback converter that is used to supply LED lamps. Emphasis is given to the quantities such as the power factor, the input power into the lamp, and the efficiency of the circuit. The aim is to obtain a suitable sizing of the circuit in order to improve the power factor. Also, a required performance is to have a low lamp flickering.

The features of a light source such as the Index Rendering Color (IRC), the colour temperature, and lifetime are related to the type of LED diode that is used. In our case study, ten LED diodes were used as light source and the voltage drop on the diode is 3V at 350 mA, as it is shown in Figure 4.5.
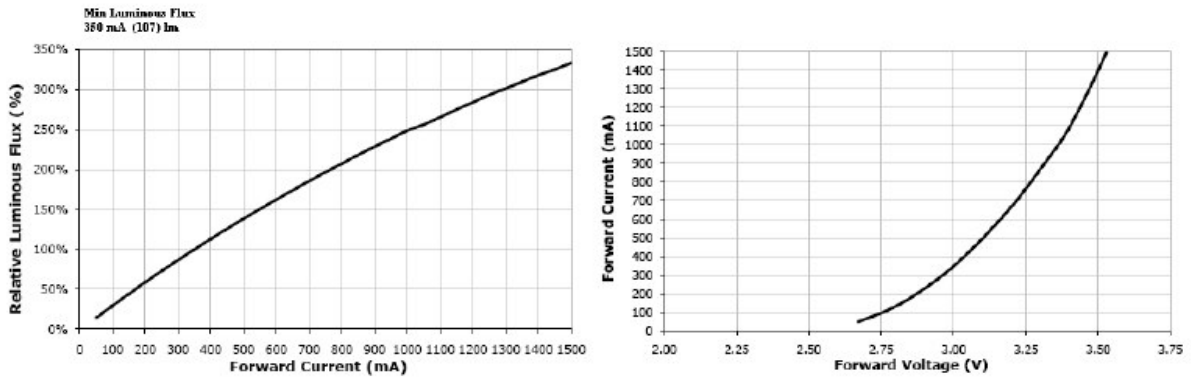
Figure 4.5: LED characteristics: on the left the relative luminous flux as function of the forward current; on the right the forward current as function of the forward voltage.

Ten LEDs in series connection emit in total about 1070 lm, and the voltage drop on the series is about 30 V. The first step on the design of the DC/DC flyback converter is the choice of the switching frequency of the power MOSFET. This is chosen suitably in the range of 80-150 kHz as a trade-off to avoid disturbances due to electromagnetic emission, and also to reduce the burden of their filtering. The second aspect is the choice of the breakdown voltage of the power MOSFET, this quantity is obtained by the following relationship:

$$BV_{DSS} = V_{IN} + V_{fl} + V_{spike} + V_{safe} \approx 600V$$

Eq. 4.2

where $V_{fl}$ is the flyback voltage (it will be fixed at a value of 100 V), which is the reflected voltage to the primary during the off state of the power MOSFET; $V_{spike}$ is the overvoltage that occurs during the turn off on the drain of the device, and it is due to the parasitic inductances; $V_{safe}$ is taken as an additional safety margin voltage (to be considered in about 20% of the supply voltage). The choice of the device in the case study is one with a breakdown voltage of 600 V. The calculation of the turn ratio is done by:

$$V_{fl} = \left(V_{out} + V_D\right)\frac{n_p}{n_s} \qquad \frac{n_p}{n_s} \approx 3.22$$

Eq. 4.3

where $V_D$ is the forward voltage drop in the output diode D.

The value of the primary and secondary inductance and the input current of the converter are to be calculated. Based on the voltage area equivalence across the inductance in steady-state, we have:

$$V_{in,min}T_{on,max} = V_{fl}T_{off}; \quad T_s = T_{on,max} + T_{off}$$

Eq. 4.4

By combining relations Eq. 4.4, and also accounting for the output power (10.5 W), the $T_{on,max}$ value is calculated, and subsequently the value of the primary inductance $L_p$ and the maximum current value at the primary, $I_{pk}$, by:

$$I_{pk} = \frac{V_{in,min}T_{on,max}}{L_p}; \quad P_{out} = \frac{1}{2}L_p I_{pk}^2 \eta f_{sw}$$

Eq. 4.5

The obtained values are: $L_p$=1.46 mH and $I_{pk}$=370 mA. The value of the secondary inductance may be determined by:

$$\frac{L_p}{L_s} = \left(\frac{N_p}{N_s}\right)^2 = 10.37$$

Eq. 4.6

that means $L_s$=140 µH.

With reference to the design of the output stage, the output capacitor is connected in parallel to a non-resistive load (LED) whose voltage-current characteristic is non-linear. The action of the capacitor is to filter the voltage ripple across the load. By the design equations Eq. 4.5 [10] and Eq. 4.6 [11], and also taking into account the contribution on voltage ripple that is caused by the parasitic ESR (equivalent series resistance), a capacitance value of 220 µF has been calculated. Finally, the features of the л input filter are defined, whose cut-off frequency is:

$$f_{cutoff} = \left(2\pi\sqrt{L\frac{C_1 C_2}{C_1 + C_2}}\right)^{-1}$$

Eq. 4.7

The values of the capacitance and inductance are settled so that the cut-off frequency is a decade below the switching frequency of the flyback converter ($f_{sw}$=132 kHz). Once the value of the inductance $L$ is fixed, by increasing the value of the buffer capacitances ($C_1+C_2$) we obtain a decrease of the output voltage ripple of the buffer. Also the peak current through the primary of the transformer and through the switch is reduced,

and the power losses decrease. As a consequence, we obtain a smaller sized transformer with the disadvantage of a lower power factor. On the contrary, by reducing the value of the buffer capacitance, the output voltage ripple increases on the buffer, this implies a greater peak current through both the primary of the transformer and the power switch, and the efficiency is reduced. The advantage is to have a higher power factor. As it is shown in Figure 4.6, the line current is heavily distorted. The non-sinusoidal waveform $i_S(t)$ that is repeated with frequency $f_s$, may be developed in Fourier series and may be expressed as the sum of its harmonic components. The line current has a dominant fundamental frequency, and contains infinite components with multiple frequencies of the fundamental, which are the distortion components of the current:

$$i_S(t) = i_{S1}(t) + \sum_{h \neq 1} i_{Sh}(t) = \sqrt{2} I_{S1} \sin(2\pi f_S t - \phi_l)$$
$$+ \sum_{h \neq 1} \sqrt{2} I_{Sh} \sin(2\pi f_h t - \phi_h)$$

Eq. 4.8
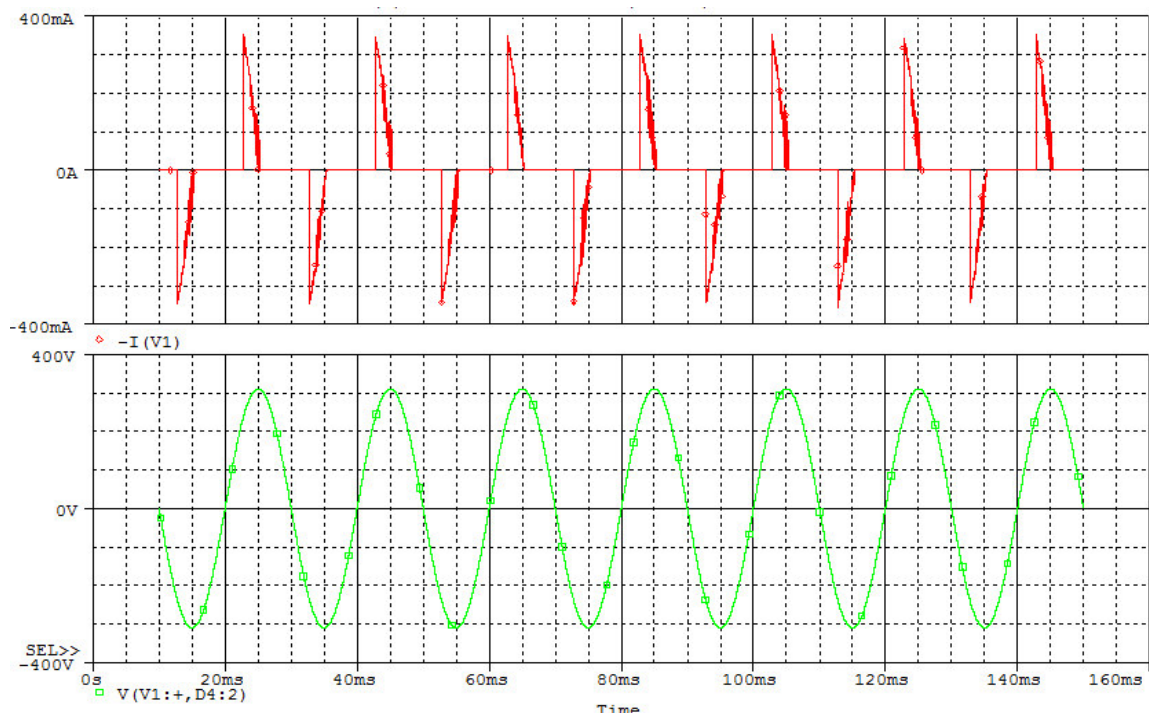


Figure 4.6: Line current on the top: voltage main on the bottom ($f_{cutoff} = 1/10\, f_{sw}$).

The harmonic components of the current with frequencies above the fundamental do not contribute to the average power (active power) that is supplied from the source with sinusoidal voltage. The power factor (PF) is defined as the ratio between the active power and the apparent power:

$$PF = \frac{P}{S} = \frac{V_S I_{S1} \cos(\phi_l)}{V_S I_S} = \frac{I_{S1}}{I_S} \cos(\phi_l) \qquad \text{Eq. 4.9}$$

The peak amplitudes of the most significant harmonics that are contained in the line current are shown in Figure 4.7. The *rms* value of the current line ($I_S$) in Eq. 4.9 has been calculated by taking into account the distortion content till the twentieth harmonic. The line current $i_s(t)$ is far from a sinusoidal waveform, and the amount of the distortion of the current waveform is given by the total harmonic distortion (THD) index.



Figure 4.7: Fourier analysis of the line current ($f_{cutoff} = 1/10\, f_{sw}$).

$$THD\% = \frac{I_{dis,rms}}{I_{S1,rms}} 100 = \frac{\sqrt{I_{S,rms}^2 - I_{S1,rms}^2}}{I_{S1,rms}} 100 \qquad \text{Eq. 4.10}$$

Analyses at different values of the cut-off frequency of the $\pi$ filter have been performed, and the performance of the converter was evaluated. The most significant figures are written in Table 4.1. In order to obtain better PF values and lower THD values, a change in the input stage of the flyback converter has been made, as it is shown in Figure 4.8.

Table 4.1

| Freq.($f_{sw}$) [Hz] | $\Delta V_{out}$ [%] | $P_{out}$ [W] | $P_a$ [W] | S [VA] | PF | $\eta$ | THD % |
|---|---|---|---|---|---|---|---|
| 1/10 | 1.2 | 10.48 | 13.53 | 22.92 | 0.59 | 0.78 | 126 |
| 1/50 | 0.2 | 10.50 | 13.78 | 31.54 | 0.44 | 0.76 | 194 |
| 1/100 | 0.1 | 10.50 | 14.05 | 36.32 | 0.39 | 0.75 | 227 |
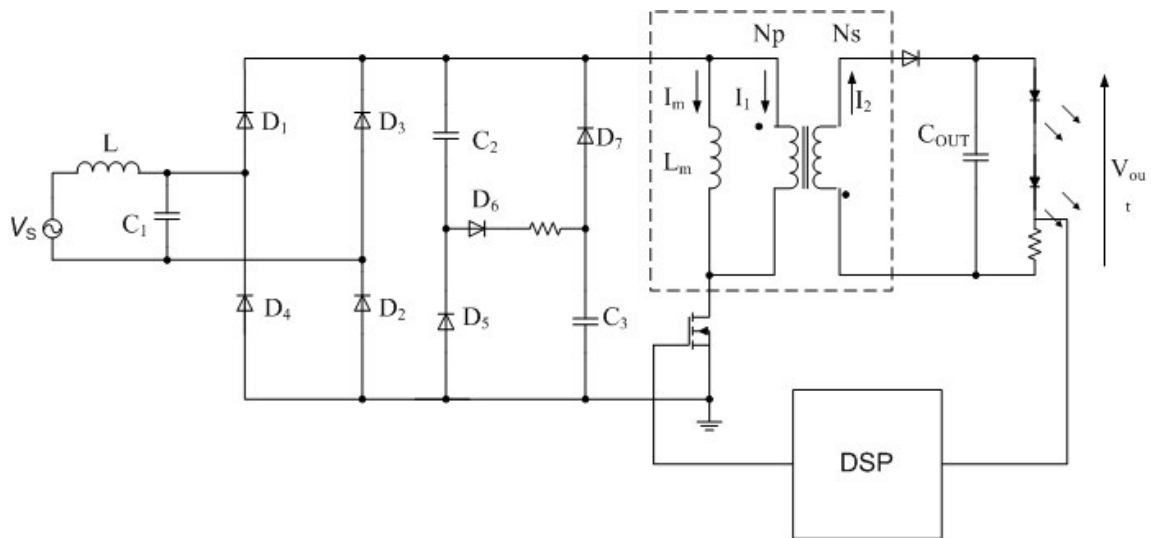
Figure 4.8: Schematic of flyback converter with a valley PFC.

The π input filter was changed with a passive power factor corrector circuit (PFC, or valley circuit), and before the rectifier bridge was introduced a LC filter with a cut-off frequency fixed at about 1/10 of the switching frequency. Subsequently a sensitivity analysis was made in order to evaluate the parameter influence on the input quantities (PF, THD, and efficiency) of the converter. In particular, attention was focused on the output capacitor. The main results are detailed in Table 4.2. The current and voltage waveforms on the main line are shown in Figure 4.9, while the harmonic components of the current are shown in Figure 4.10.

Table 4.2

| Cout [μF] | fcutoff [kHz] | Pout [W] | Pa [W] | S [VA] | PF | η | THD % | ΔVout % |
|---|---|---|---|---|---|---|---|---|
| 220 | 11.3 | 11.7 | 14.6 | 16.0 | 0.91 | 0.80 | 32.3 | 14.7 |
| 470 | 11.3 | 10.9 | 13.6 | 16.5 | 0.82 | 0.80 | 58.3 | 6.9 |
| 680 | 11.3 | 10.8 | 13.6 | 16.5 | 0.82 | 0.79 | 70.2 | 4.9 |
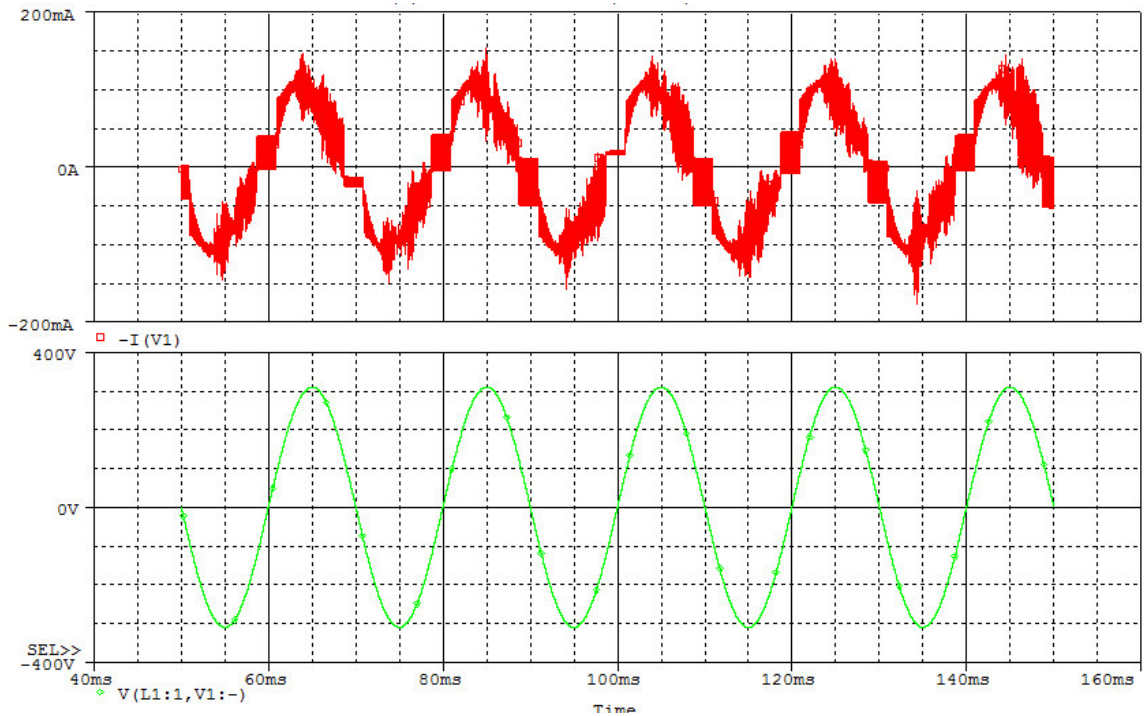
Figure 4.9: Line current on the top and voltage main on the bottom (C_out=220 µF).
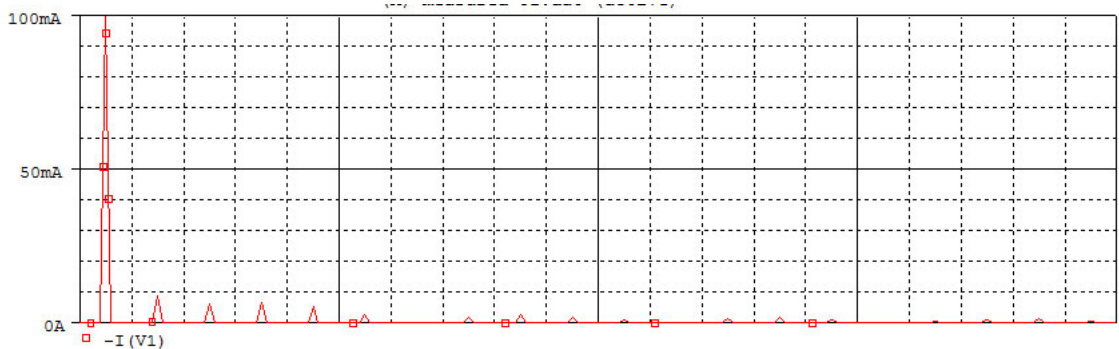


Figure 4.10: Fourier analysis of the line current (C_out=220 µF).

There are different types of dimming strategies well-known and reported in literature. Such strategies may be summarized into two main categories: analogue dimming and PWM dimming [12] and [13]. The former case requires that the current of the LEDs is regulated in a continuous way; this technique takes the advantage of the linearity between the output luminous flux of the LED and the forward current. The latter case is a bit more complicated, and may be split into different types of PWM dimming. They are based on the principle of driving the diode with a constant peak current, and modulating the duty cycle of the current, by implementing a PWM control current. In this way the current in the diode will be modulated above the critical frequency which causes the flicker effect (>120 Hz), typically the frequency ranges between 200 Hz and 400 Hz.

The technique used to control the brightness in the flyback topology is the PWM series dimming, where a switch (power MOSFET) is connected in series with the LEDs. Another technique is the high frequency PWM series dimming, that has similar features of the above technique, but by means of an appropriate control loop the control of the LED is with equal switching frequency of the converter.

### 4.2.1.2. Resonant converter

The high-frequency resonant converters allow using capacitor and inductor, respectively used to filter the voltage and current ripple, with small size and small weight [14]. In fact, if compared with converter working in PWM mode, resonant converter technology has a high switching frequency, small switching losses, a wide range of input voltage, high efficiency, light weight, small size, small EMI noise, small switch stress. The schematic for a LED driving circuit is shown in Figure 4.11, where the two switches at the same arm bridge are an integrated module [14] – [17].
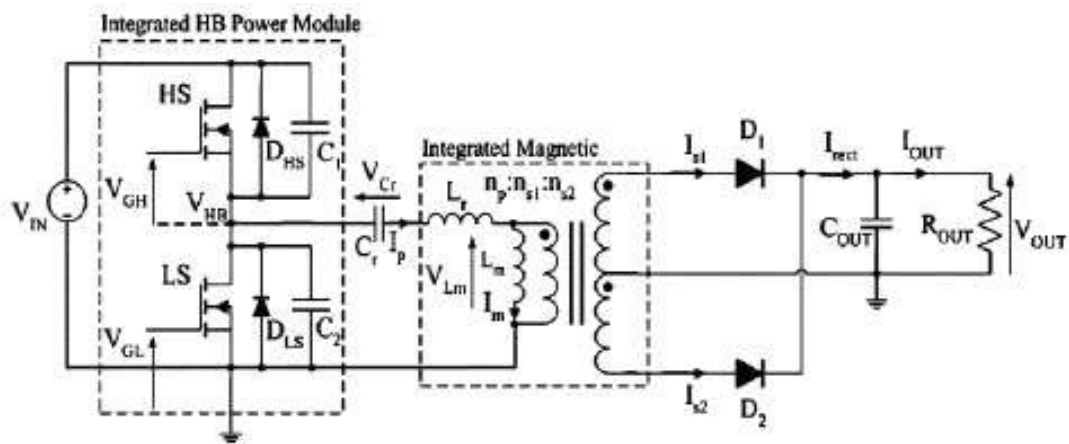


Figure 4.11: Resonant circuit schematic for LED.

### 4.2.2. Non-isolated topology

Three main dc-dc switching converters topologies, without isolation, may be used as LED driving circuits: the buck, the boost, and the Z converter (Figure 4.12 to Figure 4.14). These converters are used in order to convert a DC input voltage in to a regulated DC output voltage at a required level.
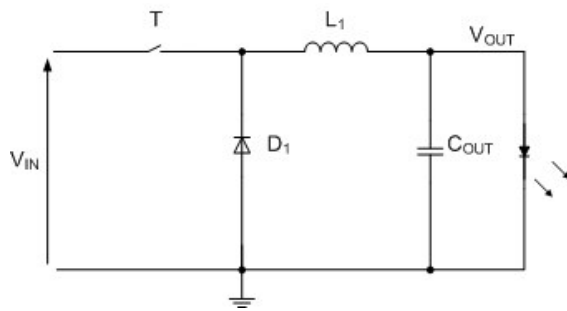
Figure 4.12: Schematic of the buck converter.
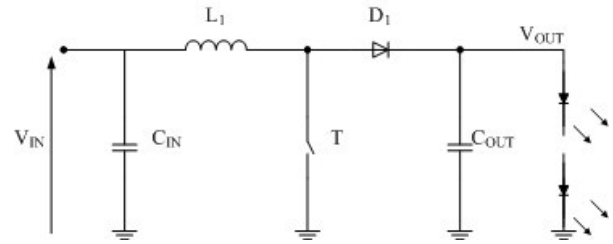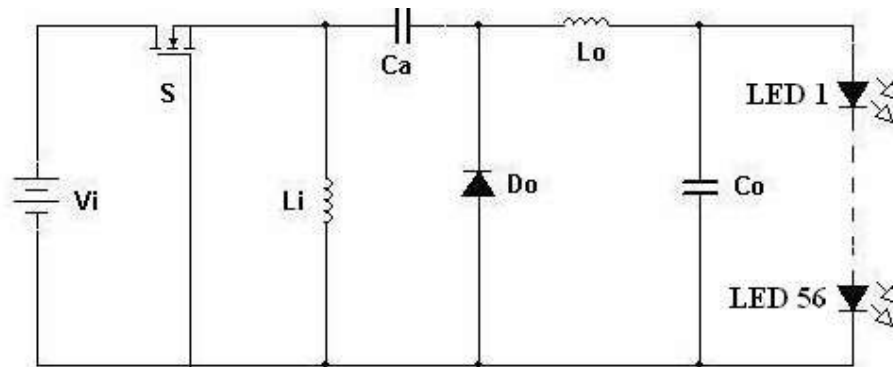
Figure 4.13: Boost converter LED driver.



Figure 4.14: Schematic of a Z converter.

### 4.2.2.1. Buck converter

Solid-state lighting bulbs may be driven in an existing lighting fixture and require a high-voltage step-down ratio in order to produce an output voltage of about 10–20 V. A buck converter provides a low average output voltage lower than the input voltage. The most important advantage is the low number of passive component of the topology and the high efficiency. The structure of a buck circuit is simple, and its design is easy. By changing the duty cycle we can get different output voltages. But in case of small duty cycle, traditional non-isolated step-down pulse width modulation buck converters may suffer of poor efficiency due to the long diode freewheeling time. One other disadvantage is the not easy drive of the power switch, because its reference terminal is floating.

### 4.2.2.2. Boost converter

A boost converter provides an average output voltage greater than the input voltage. Therefore, boost converters are ideal for LED driver applications where the LED string voltage is greater than the input voltage. The converter can easily be designed to operate at efficiencies greater than 90%. Both the source of the MOSFET and LED string are

connected to a common ground. This simplifies the sensing of the LED current (unlike the buck converter where we have to choose between either a high side MOSFET driver and a high side current sensor). The input current is continuous which makes easy to filter the input ripple current (and easier to meet any required conducted EMI standards). However, boost converters have some disadvantages. The output current of the boost converter is a pulsed waveform. Thus, a large output capacitor is required to reduce the current ripple in the LED.

### 4.2.2.3. Zeta converter

A new alternative topology has been proposed to drive LED lamps. The proposed circuit shows a very high efficiency beyond keeping constant current through the LED. According to [14], when applying white LEDs for display backlighting or other illumination applications, there are two reasons to drive them with constant current:

1. To avoid violating the absolute maximum current rating, thus compromising the reliability.

2. To obtain predictable and matched luminous intensity and chromaticity from each LED.

It is important to note that a white LED luminous intensity and chromaticity (colour) are tested and best controlled by driving it with constant current. The topology shown in Figure 4.14 is a ZETA converter. According to [12], the circuit has the following properties:

1) The transformerless version of the converter has a positive dc voltage transfer function M, *i.e.*, the circuit is a non-inverting converter.

2) The dc voltage transfer function M can be either less or greater than 1, depending on the value of the switch duty cycle D:

*M < 1 for D ≤ 0.5 and M > 1 for D > 0.5*                                Eq. 4.11

3) The transfer function M is independent of the load resistance $R_L$ in the continuous mode of operation by neglecting the power losses, while it is proportional to the square root of $R_L$ in the discontinuous mode of operation.

4) In both the transformerless and with transformer versions of the converter, the entire dc input energy is first converted into ac energy and then the ac energy is converted into the dc output energy.

## 4.2.3. Analysis of the results

The LED lighting market is an area that is rapidly expanding, and the manufacturers adopt for indoor or outdoor lighting the "retrofit" concept looking to substitute the incandescent bulbs. A power converter able to drive a string of ten diodes is required for a LED lamp having an equivalent luminous flux of a 60 W incandescent lamp. The analysis has been devoted to a flyback converter, and to its sensitivity analysis to the electrical parameter change. In particular, when a $\pi$ filter is the input of the converter, it was noted that by reducing the value of the buffer capacity an increase of the ripple of output voltage appears. This implies an increased peak of the current through the primary of the transformer and the power switch. The advantage is a higher power factor. In order to improve the PF and THD values a valley PFC circuit is used, but the output voltage ripple increases till 15% of the nominal voltage (30V). The analogue dimming is the simplest one to control the brightness of the LED lamp. although it has disadvantages, because high injection currents may lead to a lack of linearity between injected current and luminous flux output, and a noticeable shift in chromaticity coordinates, which are considered the most important drawback of this technique [18]. Alternatively, PWM techniques may be used and in particular the PWM series dimming. This technique maintains all the advantage and has not the disadvantage of the previous technique; however, this technique can lead to fluctuations of the feedback signal due to the absence of load for long transient. Series high frequency PWM dimming is an appropriate control technique that allows turning the switch in series to the LEDs at the same switching frequency of the power converter, in this way the previous problem of fluctuations is cancelled at the cost of a slight efficiency reduction.

# Chapter 5

Analysis of the conventional
techniques to reduce the power
consumption of appliances

## 5. Introduction

There are many different type of techniques that allow reducing the waste of energy in a power converter [19] [20].

## 5.1. Start up circuit

The start up resistor can be replaced by an internal high voltage current source consisting of a J-FET [21]. At start up, the internal high voltage current source supplies the internal bias and charges the external capacitor that is connected to the Vcc pin as it is shown in Figure 5.1. After Vcc is reached, the PWM controller begins switching and the internal high voltage current source is disabled. Thus, the power dissipation in the start-up resistor can be removed.
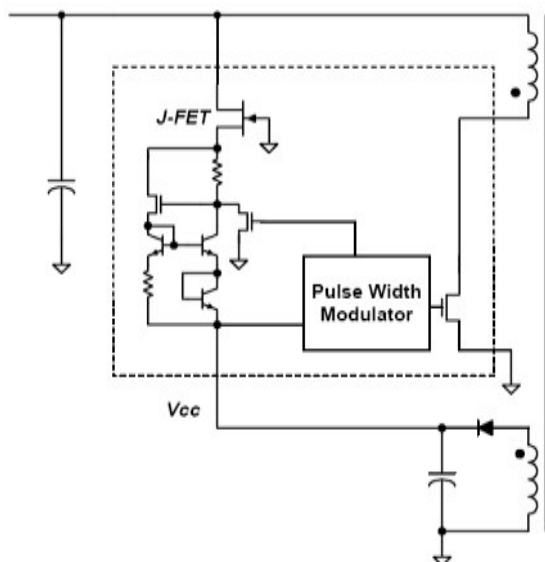


Figure 5.1: Start-up circuit.

## 5.2. Switching frequency reduction

A common technique widely used to reduce the power consumption is reducing the switching frequency. The power consumption in a power MOSFET is proportional to the switching frequency and the hysteresis losses in the transformer too. By a frequency reduction switching losses may be reduced, but entering into the human range of hearing may cause a problem. In order to reduce the audible noise, it is required to limit the peak of the drain current when passing through several kHz range. The optimum value of peak drain current is determined by trade-off between efficiency and audible noise.

## 5.2.1. Effective switching frequency reduction

In general, human ears are most sensitive to frequencies around 2 kHz and less sensitive to frequencies which are higher or lower as shown in Figure 5.2. The Figure is a graphical representation of the sensitivity of the ear to frequencies over the human range of hearing at various loudness levels.
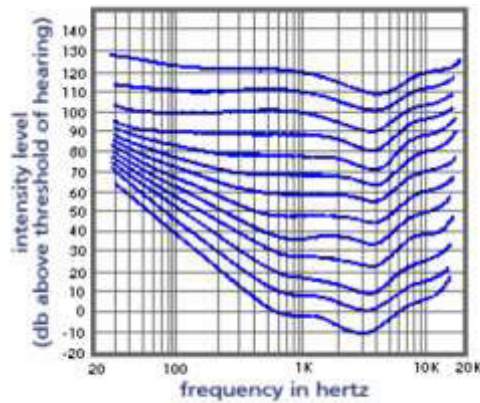


Figure 5.2: Equal Loudness curves.

Each line shows the intensity level for the range of frequency that gives a subjective impression of similar loudness with reference to a starting level of 1 kHz.

In order to limit the current level, the burst operation mode is employed to reduce the fundamental frequency. The fundamental frequency is reduced to several hundred Hz, as shown in Figure 5.3. In standby mode, the functional blocks in PWM controller for normal operation are disabled and therefore the operating current can be reduced minimizing power consumption in the PWM IC.
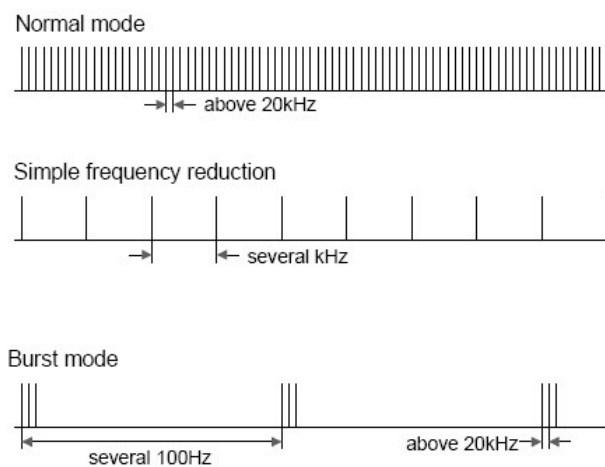


Figure 5.3: Effective frequency reduction with burst operation.

## 5.3. Output voltage disconnection

When the output load is disabled in the standby mode, some amount of leakage current always flows in the output side.

Reducing this leakage current requires a whole new design circuit in the secondary side. . In some special cases, output disconnection method is used as shown in Figure 5.4. However, this approach increases the total cost and deteriorates the efficiency.
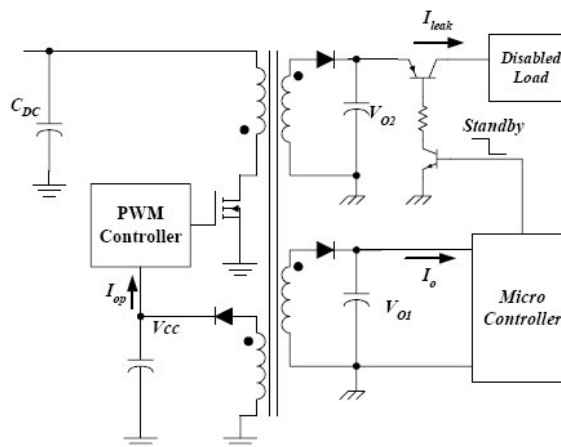


Figure 5.4: Output voltage disconnection.

## 5.4. Output voltage drop

Another approach to reducing losses caused by leakage current in the high voltage output is lowering the output voltage in the standby mode [22]. This approach is widely used when the supply for the micro-controller is provided through a linear regulator as shown in Figure 5.5. The range of the output drop is limited by the linear regulator. In order to drop the output voltage much in standby mode, the input voltage of the linear regulator in normal operation should be set as high as possible. However, this results in severe loss in the linear regulator in normal operation.
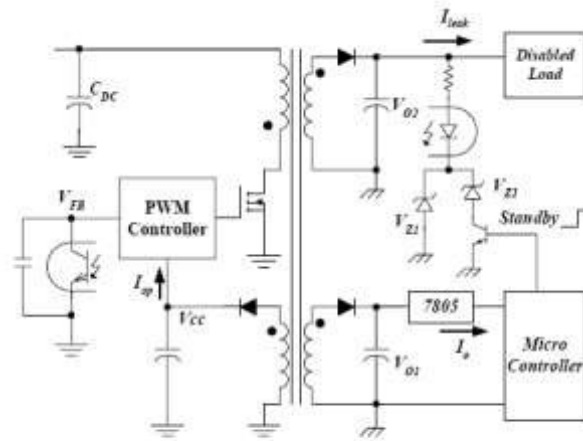
Figure 5.5: Output voltage drop.

## 5.5. Output voltage drop with auxiliary winding

As discussed in the previous session, the range of the output drop is limited by the linear regulator input voltage. By using voltage drop approach with auxiliary winding, the output can drop without limitation by the linear regulator supply voltage; Figure 5.6 shows the auxiliary winding circuit for the output voltage drop. $V_{o1}$ provides the supply voltage for the linear regulator in normal operation while $V_{o2}$ supplies the linear regulator in standby mode. Therefore, the linear regulator input voltage is selectively provided by $V_{o1}$ and $V_{o2}$, minimizing the power dissipation in the linear regulator.
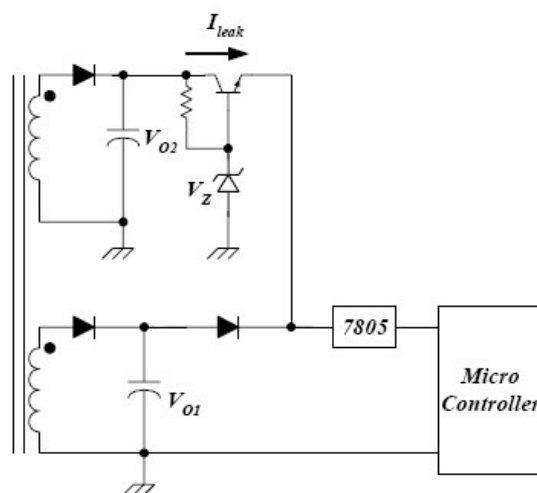


Figure 5.6: Output voltage drop with auxiliary winding.

## 5.6. Auxiliary Power supply

For auxiliary converters in high power applications above 200 W, reducing the switching frequency has limitation in lowering switching losses since MOSFET with a relatively large output capacitance is used. In that case, the use of another auxiliary power supply that is optimized for the standby power level is preferred. In the standby mode, the main power supply is shut down completely.

# Chapter 6

Design of a 5W SMPS for appliance field

## 6. Introduction

In this chapter the steps to design a power supply stage as SMPS (Switching Mode Power Supply) of 5W are exposed. Such a converter is used to supply the power board and user interface board of a washing machine.

The environment in which the SMPS is working is particularly stressful for the electronic components, because high environment temperature is reached with high humidity.

These critical conditions deteriorate components (pcb, diodes, transistors, capacitors, etc. ..), causing damages. For this purpose a suitable choice of some critical components allows to achieve a good reliability of the product.

## 6.1. Project requirements

As already mentioned the power supply is an SMPS with a maximum output power of 5 W.

Before proceeding to the sizing of the circuit in the Table 6.1 below are given the specific data that the power supply has to fulfil. It will be used throughout the project and commented on at the appropriate time.

Table 6.1

| $P_{out}$ | Output Power | 5 | [W] |
|---|---|---|---|
| Pout (-5 V) | Output Power | 1.5 | [W] |
| Pout (-15 V) | Output Power | 3.5 | [W] |
| η | Efficiency | 70 | [%] |
| $V_{IN}$ | Typically input voltage | 230 ± 10% | [V] |
| | Minimum input voltage | 170 | [V] |
| $V_{out\,1}$ | Output voltage | -5 | [V] |
| $V_{out\,2}$ | Output voltage | -15 | [V] |
| $f_{sw}$ | Switching frequency | 132 | [kHz] |
| T | Maximum ambient temperature | 70 | [°C] |

## 6.2. Selection of the operation mode in Flyback converter

The choice of the working condition depends on several parameters: one must take account of the switching frequency, the inductance value of the primary, the turns ratio of the transformer, of the input voltage and the output load.

Typically, the flyback works in the CCM with the scope of maximizing the operating power of the converter or minimize the RMS current in the primary. However, when working in CCM mode the behaviour from the dynamic point of view appears to be the worst.

In this project, the power request is 5 W, and the operation mode chosen is discontinuous (DCM) for reasons relating to the performance of the components, as will be shown in the following.

Advantage of discontinuous mode (DCM):

1   Can be used a transformer with low size, because the average energy stored is low, the uses of low turns is translated into reduced losses for Joule effect ($I^2R$).

2   Stability is easier to achieve because at frequencies less than one half the switching frequency there is no net inductance reflected to the transformer secondary, and hence no second pole in the input-to-output transfer function. Also, no right half-plane (RHP) zero appears since energy delivered to the output each cycle is directly proportional to the power transistor on-time ($T_{on}$) for the discontinuous case.

3   Output rectifiers are operating at zero current just prior to becoming reverse biased. Therefore, reverse recovery requirements are not critical for these rectifiers.

4   Similarly, the power transistor turns on to a current level which is initially zero, so its turn-on time is not critical. This results in a low emission level of noise at high frequency.

Unfortunately, some disadvantages also accrue from the use of a discontinuous current (DCM)

1   Transistor and diode peak current requirements are approximately twice what they would be in a continuous mode design. Average current requirements remain unchanged.

2    In the transformer the change of flux dΦ/dt and leakage inductance are both high under discontinuous operation, resulting in some loss of cross-regulation.

3    High values of ripple current make output capacitor ESR requirements quite stringent. In most practical discontinuous flyback circuits, capacitance values must be increased in order to achieve adequate ESR. Transient response is correspondingly slower.

In the present design, these few disadvantages were not deemed sufficient to warrant a choice of continuous mode operation. In particular, low output current requirements reduce the impact of the capacitor ESR problem.

## 6.3.  Control driver

It is a driver that incorporates a 700 V power MOSFET, oscillator, simple ON/OFF control scheme, a high voltage switched current source, frequency jittering, cycle-by-cycle current limit and thermal shutdown circuitry onto a monolithic IC (Integrated Circuit). The start-up and operating power are derived directly from the DRAIN pin, eliminating the need for a bias winding and associated circuitry.
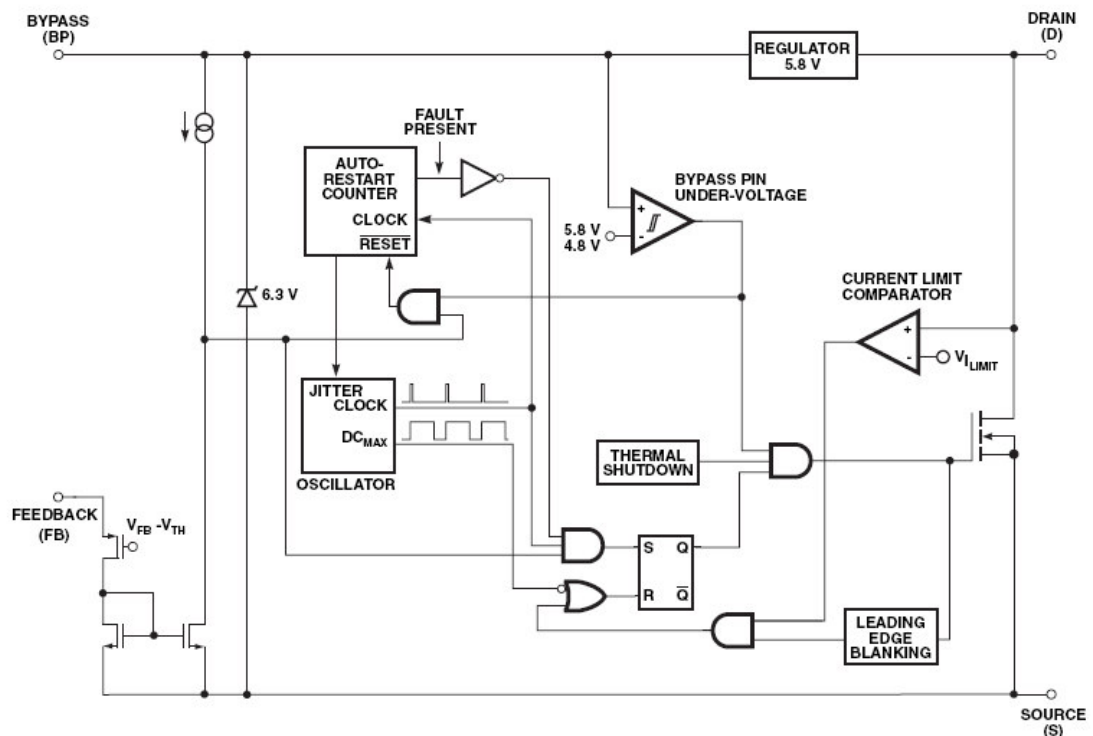


Figure 6.1: Functional block diagram.

Pin functional description

*DRAIN (D) Pin:*

Power MOSFET drain connection. Provides internal operating current for both start-up and steady-state operation.

*BYPASS (BP) Pin:*

Connection point for a 0.1μF external bypass capacitor for the internally generated 5,8 V supply. If an external bias winding is used, the current into the BP pin must not exceed 1mA.

*FEEDBACK (FB) Pin:*

During normal operation, switching of the power MOSFET is controlled by this pin. MOSFET switching is disabled when a current greater than 49 μA is delivered into this pin.

SOURCE (S) Pin:

This pin is the power MOSFET source connection. It is also the ground reference for the BYPASS and FEEDBACK pins.
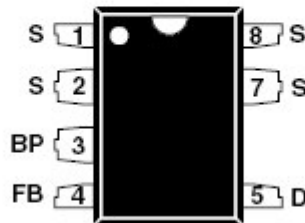


Figure 6.2: Pin configuration, P Package DIP-8B, G Package SMD-8B

Functional description:

The driver combines a high voltage power MOSFET switch with a power supply controller in one device. Unlike conventional PWM (pulse width modulator) controllers, a simple ON/OFF control regulates the output voltage. The controller consists of an oscillator, feedback (sense and logic) circuit, 5.8 V regulator, BYPASS pin under-voltage circuit, over-temperature protection, frequency jittering, current limit circuit, and leading edge blanking integrated with a 700 V power MOSFET. The *driver* incorporates additional circuitry for auto-restart.

*Oscillator*

The typical oscillator frequency is internally set to an average of 132 kHz. Two signals are generated from the oscillator: the maximum duty cycle signal (DCMAX) and the clock signal that indicates the beginning of each cycle.

The oscillator incorporates circuitry that introduces a small amount of frequency jitter, typically 9 kHz peak-to-peak, to minimize EMI emission. The modulation rate of the frequency jitter is set to 1.5 kHz to optimize EMI reduction for both average and quasi-peak emissions. The frequency jitter should be measured with the oscilloscope triggered at the falling edge of the DRAIN waveform. The waveform in Figure 6.3 illustrates the frequency jitter.

*Feedback Input Circuit*

The feedback input circuit at the FB pin consists of a low impedance source follower output set at 1.63 V for LNK363. When the current delivered into this pin exceeds 49 μA, a low logic level (disable) is generated at the output of the feedback circuit. This output is sampled at the beginning of each cycle on the rising edge of the clock signal. If high, the power MOSFET is turned on for that cycle (enabled), otherwise the power MOSFET remains off (disabled).

Since the sampling is done only at the beginning of each cycle, subsequent changes in the FB pin voltage or current during the remainder of the cycle are ignored.

*5.8 V Regulator and 6.3 V Shunt Voltage Clamp*

The 5.8 V regulator charges the bypass capacitor connected to the BYPASS pin to 5.8 V by drawing a current from the voltage on the DRAIN, whenever the MOSFET is off. The BYPASS pin is the internal supply voltage node. When the MOSFET is on, the *driver LNK363* runs off of the energy stored in the bypass capacitor.

Extremely low power consumption of the internal circuitry allows the device to operate continuously from the current drawn from the DRAIN pin. A bypass capacitor value of 0.1 μF is sufficient for both high frequency decoupling and energy storage.

In addition, there is a 6.3 V shunt regulator clamping the BYPASS pin at 6.3 V when current is provided to the BYPASS pin through an external resistor. This facilitates

powering of the device externally through a bias winding to decrease the no-load consumption to less than 50 mW.

*BYPASS Pin Under-Voltage*

The BYPASS pin under-voltage circuitry disables the power MOSFET when the BYPASS pin voltage drops below 4.8 V. Once the BYPASS pin voltage drops below 4.8 V, it must rise back to 5.8 V to enable (turn-on) the power MOSFET.

*Over-Temperature Protection*

The thermal shutdown circuitry senses the die temperature. The threshold is set at 142 °C typical with a 75 °C hysteresis. When the die temperature rises above this threshold (142 °C) the power MOSFET is disabled and remains disabled until the die temperature falls by 75 °C, at which point it is re-enabled.

*Current Limit*

The current limit circuit senses the current in the power MOSFET. When this current exceeds the internal threshold ($I_{LIMIT}$), the power MOSFET is turned off for the remainder of that cycle. The leading edge blanking circuit inhibits the current limit comparator for a short time ($t_{LEB}$) after the power MOSFET is turned on. This leading edge blanking time has been set so that current spikes caused by capacitance and rectifier reverse recovery time will not cause premature termination of the switching pulse. In particular for LNK363 the current limit value is 210 mA.

*Auto-Restart*

In the event of a fault condition such as output overload, output short circuit, or an open loop condition, *the driver* enters into auto-restart operation. An internal counter clocked by the oscillator gets reset every time the FB pin is pulled high. If the FB pin is not pulled high for approximately 40 ms, the power MOSFET switching is disabled for 800 ms. The auto-restart alternately enables and disables the switching of the power MOSFET until the fault condition is removed.
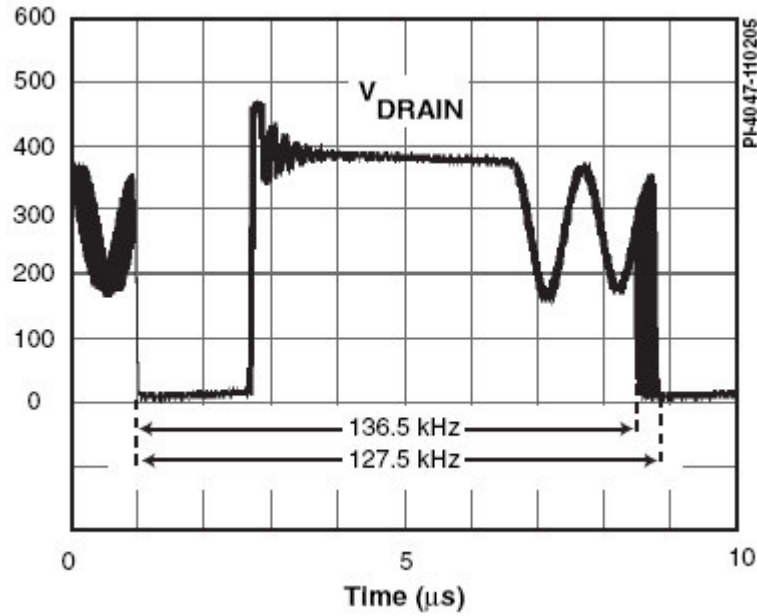
Figure 6.3: Frequency jitter.

## 6.4. Design of passive components

Following the following section is exposed an analysis of the design of the most critical passive component in the flyback converter.

### 6.4.1. Transformer

Now it possible proceeding to define two parameters of the transformer, the turns ratio ($n$) and the primary inductance ($L_1$). The turns ratio is established so that the value of $V_{fl}$ is equal to the desired value, while the primary inductance is chose so that the converter works in mode DCM (Discontinuous Mode) or in a limit condition, Transition Mode.

By recalling that:

$$V_{fl} = \left(V_{OUT(-15)} + V_{DIODO}\right) \cdot \frac{N_1}{N_{2-15V}}$$ 
Eq. 6.1

$$V_{fl} = \left(V_{OUT(-5)} + V_{DIODO}\right) \cdot \frac{N_1}{N_{2-5V}}$$ 
Eq. 6.2

we obtain:

$$\frac{N_1}{N_{2-15}} = \frac{V_{fl}}{\left(\left|V_{OUT(-15)}\right| + V_{DIODO}\right)} = \frac{120}{\left(\left|-15\right| + 1\right)} = 7.5$$ 
Eq. 6.3

$$\frac{N_1}{N_{2-5}} = \frac{V_{fl}}{\left(\left|V_{OUT(-5)}\right| + V_{DIODO}\right)} = \frac{120}{\left(\left|-5\right| + 1\right)} = 20 \qquad \text{Eq. 6.4}$$

After to define the transformation rapports between primary and secondary windings, the value of the primary winding will be calculated by means of the specifications of the driver LNK363.

The characteristic of this driver is to work at constant $T_{on}$ and variable frequency with the output power, in this way the primary current peak is always at maximum value and the $T_{off}$ change.

The datasheet of the driver define the value of the maximum current in the drain ($I_{LIM}$), the switching frequency ($f_{sw}$) and from Figure 6.1 the value of the output power, the inductor $L_1$ is obtained as:

$$L_1 = \frac{2 \cdot P_{OUT}}{I_{1\max} f_{sw} \eta} = \frac{2 \cdot 5}{2 \cdot 10^{-3} \cdot 130 \cdot 10^3 \cdot 0.7} = 2.5mH \qquad \text{Eq. 6.5}$$

By using the ratio of transformation previously calculated, $N_1/N_{2-15V}$ and $N_1/N_{2-5V}$, and the following equation, the value of $L_{2-15V}$ and $L_{2-5V}$ can be calculated.

$$\left(\frac{N_1}{N_2}\right)^2 = \sqrt{\frac{L_1}{L_2}} \qquad \text{Eq. 6.6}$$

The value of $L_{2-5V}$ is 6.2 µH and the value of $L_{2-15V}$ is 44.3 µH.

As said before the driver works with a constant $T_{on,\,max}$ value and in this time the drain current reach its maximum value, also $T_{on,max}$ is due to $L_1$ and the $V_{IN}$ values. In particular the input voltage can change in the range 170 to 250 V, and in order to evaluate the maximum value of $T_{on}$ the minimum input voltage value is taken into account.

$$T_{onMAX} = \frac{I_{1\max}}{\dfrac{V_{IN\min}}{L_1}} = \frac{210 \cdot 10^{-3}}{\dfrac{170}{2.5 \cdot 10^{-3}}} = 2.15 \mu \sec \qquad \text{Eq. 6.7}$$

By taking into account as voltage drop on the primary winding the flyback voltage, $V_{fl}$, it is possible to evaluate the $T_{reset}$ or rather the time needed for the secondary current to reach zero.

$$T_{reset} = \frac{I_{1\max}}{\dfrac{V_{fl}}{L_1}} = \frac{210 \cdot 10^{-3}}{\dfrac{120}{2.5 \cdot 10^{-3}}} = 4.36 \mu \sec$$

<div align="right">Eq. 6.8</div>

Once all the specifications of the transformer are known, it is possible to start with the design of the geometry, the size of the magnetic core and material.

The geometry of the core selected is E one, that has proper the shape of E and in particular has been selected an E10. Other configurations are not recommended because have higher losses, and considering that the reduction of the leakage inductance is one of the primary goals in the design of the transformer, the selection of other geometry make it more difficult to achieve the purpose.

Regarding the material, typically the chosen is between the shape and style provided from the manufacturers, and has been taken into account consideration both technical and economic. The choice for this application is the N87 because it is suitable to work at high frequency and a gap on the central leg is used.
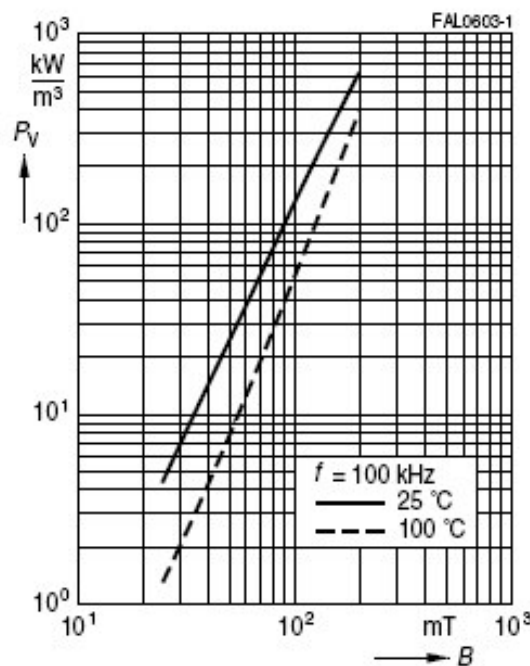


Figure 6.4: Power losses per volume in the ferrite N87.

Below it is shown, step by step, the procedure in order to design the transformer.

1) **Choice of the core size**: the core of the transformer must be able to process the input power $P_{IN}$ without saturating and with acceptable power losses, but with the minimum size possible.

The selection of the optimal size is based on a process for attempts, up to reaches the right choice. The most common parameter to describe the size of the core of the transformer is the "*Area product (AP)*", which is the product between the effective area of the core to the area of the windows available for the winding of the wire. The $AP_{min}$ can be calculated by the following relationship:

$$AP_{min} = 10^3 \cdot \left( \frac{L_p \cdot I_{pRMS}}{\Delta T^{1/2} \cdot K_u \cdot B_{max}} \right)^{1,316} [cm^4] \qquad \text{Eq. 6.9}$$

2) **Evaluation of the total power losses in the transformer.** Provided all the specifications, the total power losses are calculated. Established the maximum current in the primary winding:

$$I_1 = 210mA$$

Has been considered a margin on the current of the 20%, in this way:

$$I_1 = 210mA + 0.2 \ 210mA = 252mA.$$

Looking the graph in Figure 6.4, the saturation value of the core is near 400 mT at 100 °C.

In order to work in a safety region, the maximum value possible that can be reached is 200 mT at 100° C. About the double of the current is considered in order to guarantee of working in the linear region of the characteristics:

$$I_{DC}@100°C = 504mA$$
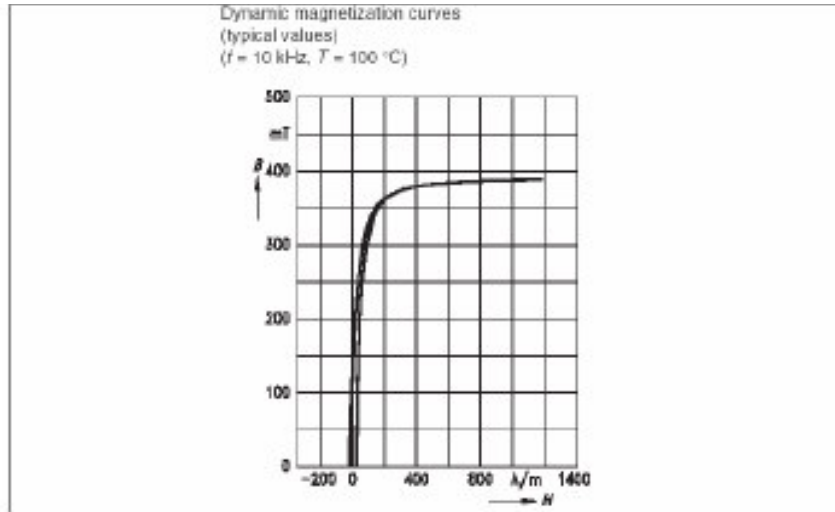
Figure 6.5: Magnetization curve.

The power dissipated into the core is:

$$P_{core} = P_{core\_per\_volume} \cdot V_e \qquad \text{Eq. 6.10}$$

where:

- $V_e$ is a value taken from the datasheet and it is:

$$V_e = 0.287 \ [\text{cm}^3]$$

- $P_{unit\,per\,volume}$ is the power dissipated per unit of volume at 200 mT and frequency of 132 $kHz$, that is the frequency of the converter taken into account, as shown from the Figure 6.6:

$$P_V = 1000 \frac{kW}{m^3}$$
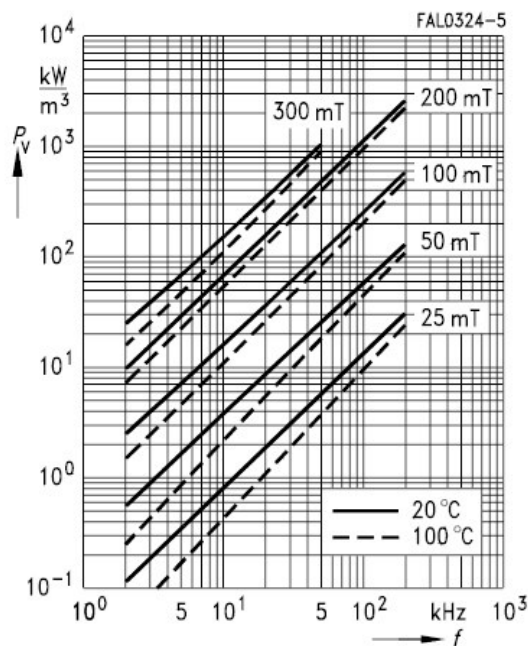


Figure 6.6: Power losses vs. frequency.

The power dissipates from the magnetic core will be:

$$P_{core} = 1 \; 0.287 = 0.287 \; W$$

By considering that the efficiency of the power converter is near 70%, the power losses in the transformer should be lower 0.6 W, because the total power wasted is near 2.1 W.

Since the power losses in the core is 0.278 W, about the same amount of losses is dissipated into the windings: 0.250 W.

**3) Design of number of turns, the gap size and the diameter of the wire.** In order to evaluate the number of turns of the windings, the follows relationship has been considered:

$$I_{DC} @100°C = \left( \frac{0,9 \cdot A_L}{K_3} \right)^{1/K_4} \qquad \text{Eq. 6.11}$$

Where the $A_L$ is the inductance of one coil and the unit is *nH*. The calculation of this value is performed by the reverse of the previous equation:

$$A_L = \frac{K_3}{0.9} \cdot \left( I_{DC} @100°C \right)^{K4} \qquad \text{Eq. 6.12}$$

Regarding the core E10 the datasheet provides the following constants $K_3$ e $K_4$, and the values are shown in Table 6.2.

Table 6.2: Value of constants to design the size of the wire and gap

**Calculation factors (for formulas, see "E cores: general information")**

| Material | Relationship between air gap – $A_L$ value | | Calculation of saturation current | | | |
|---|---|---|---|---|---|---|
| | K1 (25 °C) | K2 (25 °C) | K3 (25 °C) | K4 (25 °C) | K3 (100 °C) | K4 (100 °C) |
| N27 | 61.6 | -0.737 | 88.1 | -0.847 | 80.9 | -0.865 |
| N87 | 61.6 | -0.737 | 88.5 | -0.796 | 78.4 | -0.873 |

Validity range: K1, K2: 0.05 mm < s < 1.50 mm

K3, K4:  50 nH < $A_L$ < 430 nH

From the Table is obtained:

$$K_3 = 78.4; \; K_4 = -0.873;$$

By substituting this values in **Eq. 6.12**, we obtain:

$$A_L = 158.43 \text{nH/sp}^2$$

For the ferrite taken into account there is an operative range. As shown in Table 6.2 the range is:

$$(50 \leq A_L \leq 430)nH$$

The value obtained before is within the range and so the constraint is fulfilled. If the value obtained was not within the range then a greater core will be needed.

In order to design the gap it is used the following equation:

$$Ig = \left(\frac{A_L}{K_1}\right)^{1/K_2}$$  Eq. 6.13

Where the constant $K_1$ and $K_2$ are taken from the datasheet as the constant $K_3$ and $K_4$, see Table 6.2.

From the table, the constant values are:

$$K_1 = 61.6; K_2 = -0.737$$

and

$$Ig = \left(\frac{A_L}{K_1}\right)^{1/K_2} = 0.277 \text{ mm}$$

From equation Eq. 6.12, with one coil an inductance value of $A_L$ is obtained. Thus the total inductance is provide by relationship Eq. 6.14.

$$L_p = N_p^2 \cdot A_L$$  Eq. 6.14

hence  $N_1 = \sqrt{\dfrac{L_1}{A_L}} \approx 126 spire$

Where W1 = $N_1$ = 126 turns (see Figure 6.7b)

From the number of turns of the primary winding and by means the transformer ratio we obtain the number of turns of two secondary:

$$\frac{N_1}{N_{2-15}} = 7,5; -> N_{2-15} = \frac{N_1}{7,5} \approx 17$$

$$\frac{N_1}{N_{2-5}} = 20; -> N_{2-5} = \frac{N_2}{20} \approx 6$$

In particular the secondary windings are connected in series, therefore the number of turns of W2 and W3 (Figure 6.7) will be respectively:

$$W2 = N_{2-5} = 6$$

$$W3 = N_{2-15} - N_{2-5} = 11$$

In order to design the size of the wires, the rms value of the currents is needed. For the primary winding is taken into account the following relationship:

$$I_{RMS\_primary} = \frac{I_{peack\_primary}}{\sqrt{3}} \sqrt{\frac{T_{on\_MAX}}{T_S}} = 64.8mA \qquad \text{Eq. 6.15}$$

The calculation of the secondary rms currents has been performed by considering the maximum power, $P_{out-5V}$ and $P_{out-15V}$ respectively 1.5W and 3.5 W.

$$I_{RMS\_secondary-5V} = \frac{P_{out\_-5V}}{V_{out-5V}} = 300mA \qquad \text{Eq. 6.16}$$

$$I_{RMS\_secondary\_15V} = \frac{P_{out\_-15V}}{V_{out-15V}} = \frac{3,5}{15} = 233mA \qquad \text{Eq. 6.17}$$

As said before the total power losses are near 0.5 W, and are composed by 287mW from the core and about 100 mW from the copper wire. In particular the power losses in the primary winding, W1, will be 25 mW as it is shown by the following equation:

$$P_{Cu\_primary} = 30mW = Rp \left( I_{RMS\_primary} \right)^2$$
$$Rp < 7\Omega$$
\qquad Eq. 6.18

It is known that the resistance is:

$$R = \frac{\rho \cdot l}{A}$$

Eq. 6.19

And :

$$A = \frac{\rho \cdot l}{R}$$

Eq. 6.20

Hence:

$$A_{pcu} = \frac{\rho \cdot l_t \cdot N_P}{R_P}$$

Eq. 6.21

Where $l_t$ is the length averaged per one coil and $\rho$ is resistivity of the copper that is equal 2.3 μΩ/cm.



(a)                                                    (b)
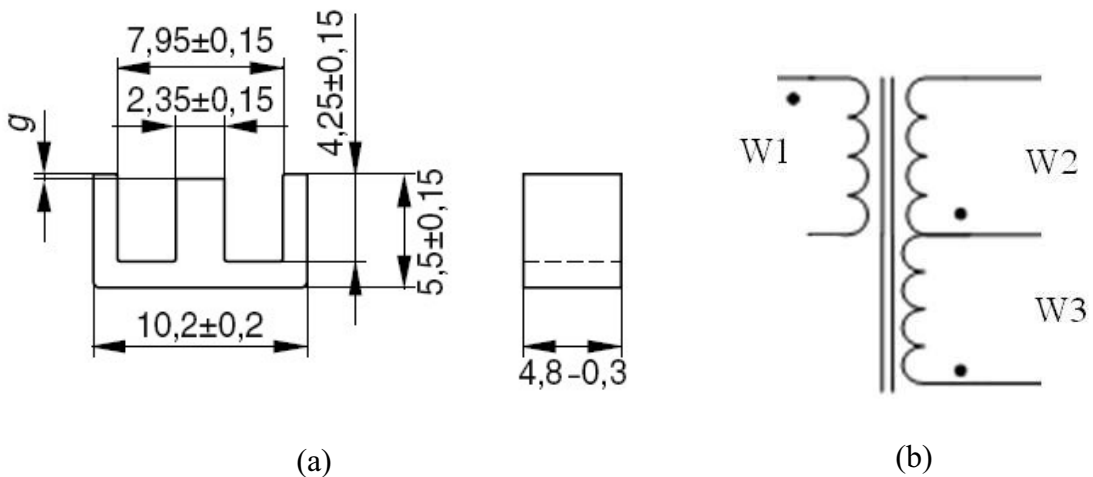
Figure 6.7: (a) Magnetic core E10 size;(b) electronic schematic of the transformer.

In Figure 6.7 is shown the sizing of the core. Now it is possible to evaluate the section and so the diameter:

$$A_{pcu} = \pi \cdot r^2 = 133,8 \cdot 10^{-6} cm^2$$

Eq. 6.22

$$d = 2\sqrt{\frac{A_{pcu}}{\pi}} = 0,13mm \qquad \text{Eq. 6.23}$$

The diameter of the wire used in the transformer is 0,130 mm that is equal to 5,1 Mils.

For the design of the wire's diameter of the secondary windings, the same operation will be used as before. In particular the two secondary winding are connected in series between them, in this way the current that flows through the winding W2 (see Figure 6.7b) is the sum of $I_{RMS\_secondary\text{-}5V}$ and the $I_{RMS\_secondary\text{ -}15V}$.

By taking into account the power losses of 200mW for the W2 winding, we obtain:

$$P_{CU\_\sec ondary(-5)} = 40mW = R_{S(-5)} \cdot \left(I_{RMS\_\sec ondary\text{-}5V} + I_{RMS\_\sec ondary\text{-}5V}\right)^2$$
$$R_S < 140m\Omega \qquad \text{Eq. 6.24}$$

$$d_{-5} = 0.250 \text{ mm}$$

that is equal to 10Mils.

Regarding $W3$ winding, it is in series with $W2$ and this provide -15V in the output.

$$P_{CU\_\sec ondary(-15)} = 40mW = R_{S(-15)} \cdot \left(I_{RMS\_\sec ondary\text{-}15V}\right)^2$$
$$R_S < 730m\Omega \qquad \text{Eq. 6.25}$$

$$d_{-15} = 0.250 \text{ mm}$$

## 6.4.2. Output capacitors

For the target of this application the transformer has been designed with two outputs with power of 1.5 W and 3.5 W, respectively.

In a first analysis the peak current in the secondary is evaluated as follows, from equation, Eq. 6.15 to Eq. 6.17. In the  following it is shown the relationship between the rms current and the peak current:

$$I_{peack\_secondary\_-5V} = \frac{I_{RMS\_secondary\text{-}5V}\sqrt{3}}{\sqrt{\dfrac{T_{reset}}{T_S}}} = 690mA \qquad \text{Eq. 6.26}$$

$$I_{peack\_secondary\_-15V} = \frac{I_{RMS\_secondary\text{-}15V}\sqrt{3}}{\sqrt{\dfrac{T_{reset}}{T_S}}} = 536mA \qquad \text{Eq. 6.27}$$

After that the voltage ripple value on the output voltages are fixed to $V_{ripple}$ = 150mV, these values correspond respectively to 3% of $V_{out\text{ -}5V}$ and 1% of $V_{out\text{ -}15V}$.

The voltage ripple is to due to two contributions, the first due to the Equivalent Series Resistor (ESR) of the electrolytic capacitor and second to of the charge variation in the capacitor.

The most important contribution is provided by the ESR one, that may be evaluated by the following equation:

$$ESR \cdot C = 65 \cdot 10^{-6}\,s \qquad \text{Eq. 6.28}$$

In particular, for each output capacitor:

$$ESR_1 = \frac{V_{ripple}}{I_{ripple}} = \frac{250 \cdot 10^{-3}}{0{,}69} = 217m\Omega \qquad \text{Eq. 6.29}$$

$$ESR_2 = \frac{V_{ripple}}{I_{ripple}} = \frac{250 \cdot 10^{-3}}{0{,}69} = 279m\Omega \qquad \text{Eq. 6.30}$$

By substituting the values in the following equations we obtain the capacitor values:

$$C'_1 \geq \frac{65 \cdot 10^{-6}}{ESR} > 300\mu F \qquad \text{Eq. 6.31}$$

$$C'_2 \geq \frac{65 \cdot 10^{-6}}{ESR} > 230\,\mu F \qquad\qquad \text{Eq. 6.32}$$

Other contributions are due to the changing charge, ΔQ, in the capacitor:
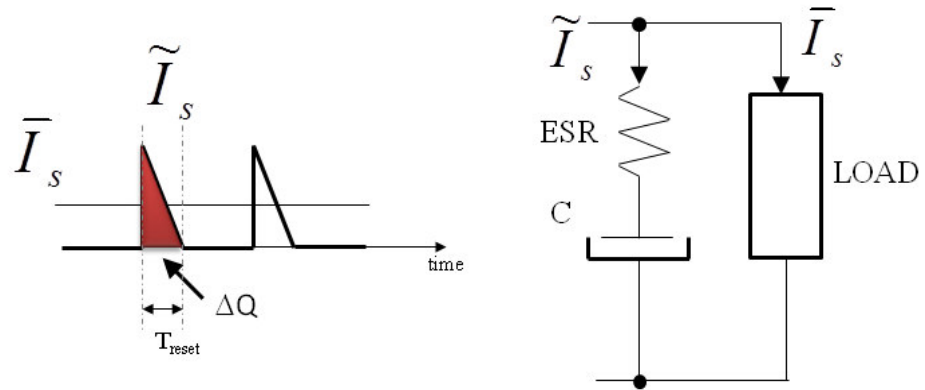


Figure 6.8: waveform of the output current in the secondary and equivalent model of capacitor.

$$C = \frac{\Delta Q}{\Delta V}$$
$$\Delta Q = \frac{I_{2\max} T_{reset}}{2} \qquad\qquad \text{Eq. 6.33}$$

Where $\Delta V = V_{\text{ripple}} = 150$ mV, $I_{2\max}$ is the peak current in secondary.

For the two secondary outputs a capacitor value has been calculated:

$$C''_1 \geq \frac{0{,}91\,\mu C}{150 mV} = 3.65\,\mu F$$

$$C''_2 \geq \frac{0{,}71\,\mu C}{150 mV} = 3.20\,\mu F$$

The total capacitor $C_{\text{out}}$ is provided by the sum of two capacitive contributes C' and C'', respectively for the two capacitors ($C_1$ and $C_2$).

$$C_{out1} = C'_1 + C''_1$$
$$C_{out2} = C'_2 + C''_2 \qquad\qquad \text{Eq. 6.34}$$

The capacitor value selected is 330 µF, this one fulfilled the specifications of output voltage ripple according to the relationship Eq. 6.34.

The ESR is an important parameter of the electrolytic capacitor because it causes power dissipation by Joule effect and so modifies its electrical performance.

## 6.4.3. Snubber network

The snubber network is used in order to limit the over voltage on the power MOSFET that can be damaged due to the leakage inductor in the primary winding. The network is composed by a resistor, a capacitor and a diode as shown in Figure 6.9:
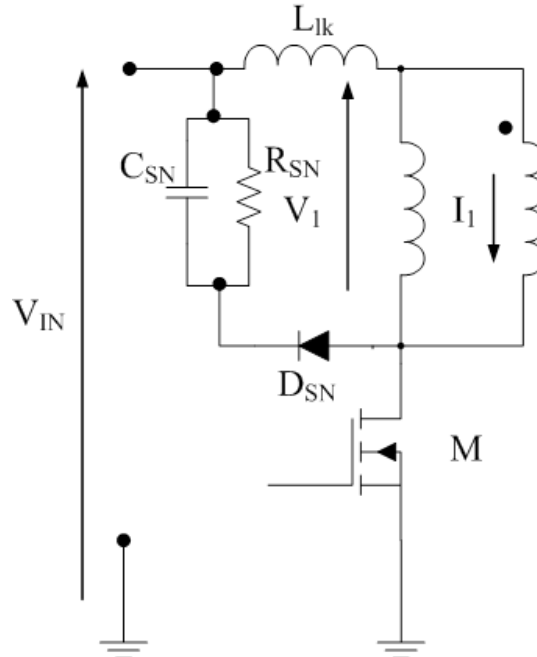


Figure 6.9: Snubber network

During the $T_{on}$ time of the power MOSFET, the leakage inductor stores energy and during the $T_{reset}$ time transfers such an energy into the snubber capacitor. In this way from the energy stored in the leakage inductor, $L_{lk}$, can be calculated the snubber capacitor value and then the resistor value.

$$E_{lk} = \frac{1}{2} L_{lk} I_{1max}^2$$

Eq. 6.35

$$E_{Cap} = \frac{1}{2} C_{SN} \left( V_{Cmax}^2 - V_{Cmim}^2 \right)$$

Eq. 6.36

The value of the leakage inductor is 35 µH and the maximum value in the inductor $I_{1max}$ is 210mA. From Eq. 6.35 follows the energy value $E_{lk}$ = 772 nJ, and by fixing the energy capacitor equal to the energy inductor, then the equation Eq. 6.37 can be solved as follow:

$$E_{Cap} = E_{lk}$$

$$C_{SN} = \frac{2 \cdot E_{Cap}}{\left(V_{C\max}^2 - V_{Cmim}^2\right)}$$

Eq. 6.37

Where the average voltage value on the capacitor is $V_{fl}$ and in particular the maximum value is fixed at $V_{fl}$ + 5% of $V_{fl}$ and the minimum value at $V_{fl}$ - 5% of $V_{fl}$.

From Eq. 6.37 $C_{SN}$ is near 535 pF and a capacitor of 560 pF with a maximum voltage rating of 270V is taken into account in the project.

After the reset time, of the primary inductor of the transformer, the capacitor $C_{SN}$ needs to be discharged in a $R_{SN}$ resistor for a time equal to:

$$T_{discharge} = T_{SW} - T_{reset}$$

Eq. 6.38

The waveform of the discharge of capacitor is:

$$V_{cap}(t) = V_{C\max} e^{-\frac{t}{\tau}}$$

Eq. 6.39

Where the parameter $\tau$ is the constant time of the snubber circuit: $\tau = R_{SN} C_{SN}$.

$$R_{SN} = \frac{T_{discharge}/C_{SN}}{\ln\left(\frac{V_{Cmac}}{V_{C\min}}\right)}$$

Eq. 6.40

By substituting the parameter values in Eq. 6.40, a resistor value of 143 kΩ is obtained. The power dissipated from the resistor for Joule effect is:

$$V_{R\max} = V_{C\max}$$

$$P_{\max} = \frac{V_{C\max}^2}{R_{SN}} = \frac{126^2}{143 \cdot 10^3} = 111mW$$

Eq. 6.41

A resistor of 150 kΩ and ¼ W is selected in the project.

## 6.4.4. Input filter

The input flyback voltage, $V_{IN}$, is a DC voltage that is obtained from the main voltage AC at 230 V ± 10% and 50 Hz of frequency.

In order to rectify the main voltage into a DC voltage, a rectifire circuit at half waveform has been used. The input voltage of the flyback converter, $V_{IN}$, may have a change of 20% of the rated value, in particular the worst case was considered when the main voltage is at minimum value from specifications, see Table 6.1. The capacitor will provide the energy to the circuit for a period $T_{dis}$ as it is shown in Figure 6.10 and this time is near 15 msec. The capacitor value is calculated starting from energy considerations:

$$P_{in} = \frac{P_{out}}{\eta} = \frac{E_{cap}}{T_{dis}} = \frac{1}{T_{dis}} \frac{1}{2} C_{IN} \left( V_{max}^2 - V_{min}^2 \right)$$

$$C_{IN} = \frac{2 \cdot P_{out} \cdot T_{dis}}{\eta \cdot \left( V_{IN\,max}^2 - V_{IN\,min}^2 \right)} = \frac{2 \cdot 5 \cdot 15 \cdot 10^{-3}}{0,7 \cdot \left( 240^2 - 192^2 \right)} \cong 10 \mu F$$

Eq. 6.42
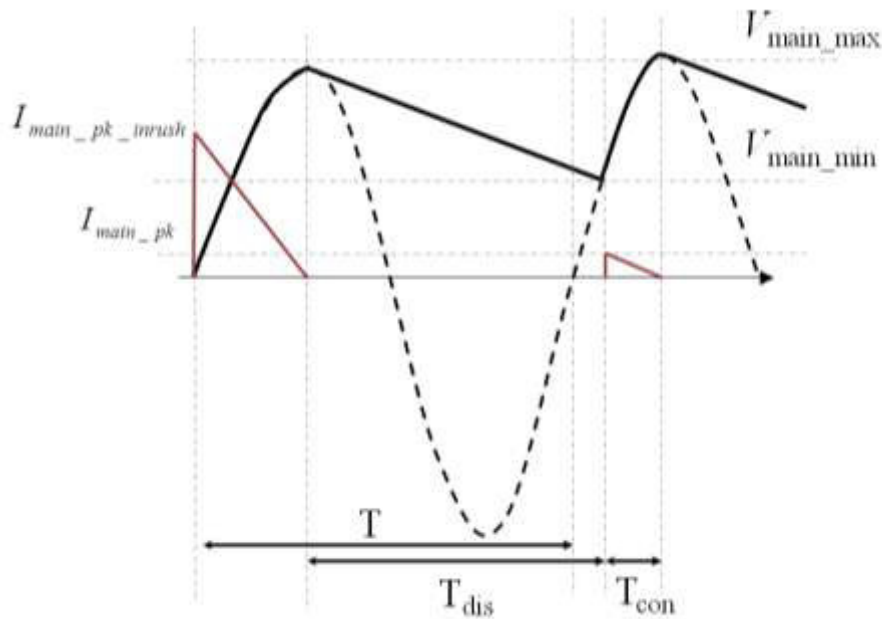


Figure 6.10: Waveform main voltage and current.

Also an inrush resistor has been calculated in order to reduce the current during the start up time of the SMPS in the rectifier diode, because the input capacitor is discharged with a great current through the diode. The value is calculated by taking into account an $I_{main\_pk\_inrush} = 16A$.

$$R_{IN} = \frac{V_{mainMAX}}{I_{main\_pk\_inrush}} = \frac{360}{16} = 22.45\Omega$$

<div align="right">Eq. 6.43</div>

In order to calculate the power consumption of the resistor the rms current on the input has been evaluated. During the conduction time of the diode, $T_{con}$, a current flows through the input resistor, as it is shown in Figure 6.11
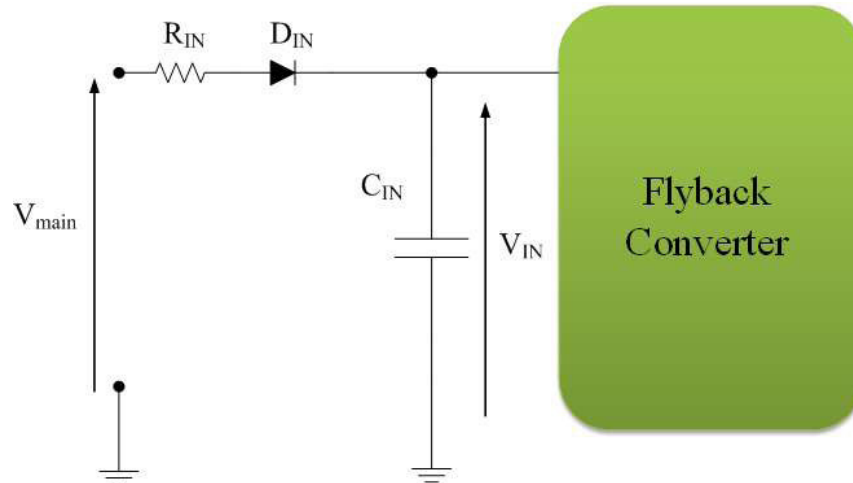


Figure 6.11: Input filter at half waveform.

The total energy provided from the main source at $f = 50Hz$ (T = 20msec) to the load is the sum between the energy of the capacitor and the energy feeding the power supply.

$$E_{tot} = E_{cap} + P_{in} \cdot T_{con} = \frac{V_{main\_min} \cdot I_{main\_pk} \cdot T_{con}}{2}$$

$$I_{main\_pk} = \frac{2 \cdot E_{tot}}{V_{IN\,min} \cdot T_{con}} = 696mA$$

$$I_{main\_rms} = I_{main\_pk} \cdot \sqrt{\frac{T_{con}}{2T}} = 220mA$$

$$P_R = R_{IN} \cdot I_{main\_rms}^2 = 1.1W$$

<div align="right">Eq. 6.44</div>

The resistor selected is a 22 Ω, 3W.

## 6.5. Design of active components

In the  following is proposed an analysis of the active critical component of the flyback converter, and the selection of appropriate part numbers of components. In particular are taken into account the diode in the input stage and output stage of the converter.

### 6.5.1. Design of the output rectifier diode and snubber's diode

In order to select the correct type of diodes in the output circuit of the flyback converter, it needs to evaluate the reverse voltage on the diodes. From equation (see Appendix I, Eq. I.31) the voltage in output on the W2 winding is 16 V and in the series of W2 and W3 windings is 43 V.

By remembering that the maximum peak current in the secondary are shown in (Eq. 6.26 and Eq. 6.27), the diodes taken into account for the project are: SB240 and UF4002. The features of the components are shown in the following Table 6.3:

Table 6.3

| Specification | D1 = SB240 | D2 = UF4002 | $D_{IN}$ = 1N4007 |
|---|---|---|---|
| $V_F$ | 0,7 V | 1 V | 1 V |
| $I_F$ | 2 A | 1 A | 1 A |
| $V_{RRM}$ | 40 V | 400 V | 1000 |
| $R_{thj\text{-}a}$ | 45 °C/W | 50 °C/W | 100 °C/W |

By considering the feature in the Table 6.3 and the values calculated before, the maximum junction temperature of the components taken into account can be estimated. The power dissipated from the diode at maximum load, and, and the diode temperature are:.

$$P_{DIODE} = \frac{1}{T}\int_T v \cdot i\, dt = \frac{1}{2}V_F I_{pk}\frac{T_{con}}{T}$$
<div align="right">Eq. 6.45</div>

$$Tj = Ta + P_{DIODE}R_{thj-a}$$
<div align="right">Eq. 6.46</div>

The temperature has been evaluated in different ambient condition, in normal condition and hard condition. In the first case the junction temperature reach Tj(Ta=23°C) = 31°C for D1 and Tj(Ta=23°C) = 34°C for D2, while in the second condition the value estimated are Tj(Ta=70°C) = 76°C and Tj(Ta=23°C) = 79°C.

Regarding the input rectifier diode of the main voltage has been used a 1N4007, that has a reverse voltage $V_{RRM}$ = 1000 V and a forward current of 1 A and non repetitive peak current of 30 A. These features match the work condition. Also the thermal resistance $R_{thj-a}$ =100 C/W, and considering a forward voltage of $V_F$ = 1V the power consumption is near 70mW (see the specification relationship Eq. 6.44 and Eq. 6.45) and the junction temperature at Ta =25°C and Ta = 70 is 32 °C and 77 °C respectively according to equation Eq. 6.46.

# Chapter 7

Analysis and design of a circuit for control state of the SMPS

## 7. Introduction

The model of the circuital technique proposed in order to reduce the power consumption in non operation mode is shown in Figure 7.1, and in Figure 7.2 details of the topology proposed are shown.

The operation of the circuit allows to control the state of SMPS both from a mechanical switch and from a microcontroller inside to the user interface circuit.

When the microcontroller detects an inactivity state of the washing machine, after two minute, send a low digital signal to SMPS and this one goes in off state. Therefore, the output voltage is reduced to zero and all system is shouted down [23].

## 7.1. Electrical circuit analysis

The turn off of the SMPS is obtained by forcing, in a feedback pin of the driver controller, a current greater than $I_{LIM}$ that is equal to 49µA and over this value the power MOSFET, inside the driver, is disabled (in off state).

This current is provided by means of the network composed by D and $R_1$ (Figure 7.2), and supplied to the driver controller from Bypass pin that provides a voltage reference of 5,8V. In steady state a current flows through the series of resistor ($R_1$) and diode (D). The resistor will be designed in order to provide a current greater than $I_{LIM}$.

The turn on of the SMPS can be realized by means of a mechanical operation by pushing the button T (on/off button) until the output goes high. The switch turn on the bipolar transistor $Q_1$ and the diode D will be reverse polarized. The current of $R_1$ flows through to the collector of $Q_1$, and the feedback path is enabled. After few milliseconds the output voltages reach the value of -5 V and -15 V.

After that, the microcontroller inside the user interface put high a digital signal (STATE signal) to keep on the transistor $Q_1$ and in this way when the switch is released the diode D keep the reverse polarization and the SMPS stay on.

On the contrary, by pushing the button T for a long time, the capacitor $C_1$ is charged and after some second the transistor $Q_2$ goes on and disables $Q_1$, because the base current of $Q_1$ goes in the collector of $Q_2$, so the SMPS is turned off.

The capacitor $C_1$ is designed in order to delay the turn off by means of the mechanical button T.

As said before, if the machine doesn't work for two minute, the microcontroller put low the output signal (STATE) that drives $Q_1$ to turning off it.
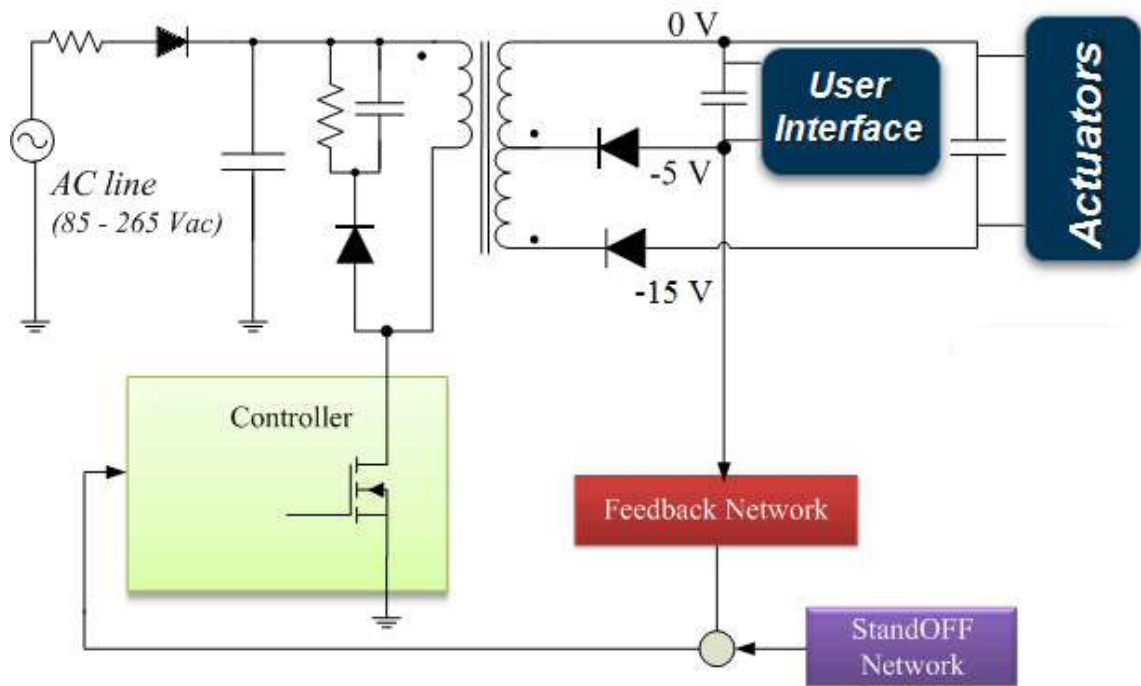


Figure 7.1: SMPS model.
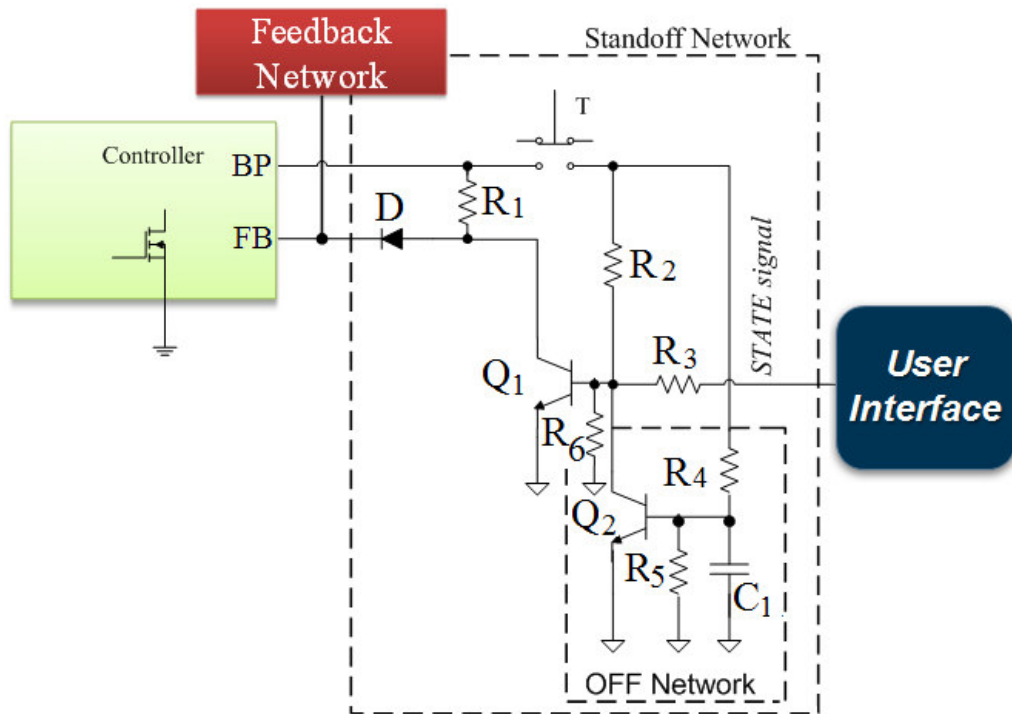


Figure 7.2: Detail of the proposed scheme.

## 7.2. Circuit design

In order to keep off the MOSFET of the driver controller a current greater than $I_{LIM}$ will be provided into the feedback pin, and in this condition the voltage in the feedback pin (as shown in the datasheet) is 2 V. From this consideration:

$$V_{BP} - R_1 \cdot I_F - V_{DIODE} - V_F = 0 \qquad \text{Eq. 7.1}$$

By manipulating Eq. 7.1 and substituting the critical values of the voltage and current, we obtain:

$$I_F = 90 \mu A > I_{LIM\_max} = 68 \mu A$$

$$R_1 \cdot = \frac{V_{BP} - V_{DIODE} - V_F}{I_F} = \frac{V_{BP} - V_{DIODE} - V_F}{I_F} = \frac{5,5 - 0,62 - 2}{90 \cdot 10^{-6}} = 32 k\Omega \qquad \text{Eq. 7.2}$$

$$P_{R_1} \cdot = R_1 \cdot I_F^2 = 259 \mu W$$

After that, the value of the driver resistor of the bipolar transistor $Q_1$ are designed.

When the bipolar transistor $Q_1$ is turned on the voltage collector goes low, and in order to guarantee the correct function the transistor works in the saturation region ($V_{CE} = V_{CEsat}$). In this way the current collector is provided by the equation:

$$I_{C1} = \frac{V_{BP} - V_{CEsat}}{R_1} = \frac{V_{BP} - V_{CEsat}}{R_1} = \frac{5,8 - 0,1}{33 \cdot 10^3} = 172,6 \mu A \qquad \text{Eq. 7.3}$$

The gain $I_C/I_B$ of the transistor $Q_1$ in order to work in saturation region is fixed to 5, in this way the base current is $I_B = 34,5 \mu A$.

The base current is given by the equation:

$$I_{B1} = I_{R_2} - I_{R_6} \qquad \text{Eq. 7.4}$$

The current $I_{R6}$ is fixed to 1/3 of $I_B$ and the value is $I_{R6} = 11,5 \ 10^{-6}$ A, in this way it is possible evaluate the resistors $R_6$ and $R_2$ as follows:

$$I_{R_2} = I_{B1} + I_{R_6} = 45{,}3\,\mu A$$

$$R_2 = \frac{V_{BP} - V_{BE}}{I_{R_2}} = \frac{V_{BP} - V_{BE}}{I_{B1} + I_{R_6}} = \frac{5{,}8 - 0{,}6}{45.3 \cdot 10^{-6}} = 115k\Omega \qquad \text{Eq. 7.5}$$

$$R_3 = \frac{V_{BE}}{I_{R_6}} = \frac{0{,}6}{11{,}5 \cdot 10^{-6}} = 52k\Omega$$

In order to turn off the transistor $Q_1$ and as well as the SMPS, the transistor $Q_2$ is turned on. The collector current of $Q_2$ is the same to the base current of $Q_1$:

$$I_{C2} = I_{B2} = 34{,}5\,\mu A \qquad \text{Eq. 7.6}$$

As done for $Q_1$, the transistor $Q_2$ works in the saturation region and the gain current is fixed to 5 in this way the base current is $I_{R2} = 7\mu A$.

The value of $I_{R5}$ is fixed to the double of $I_B$, therefore it is near $I_{R5} = 14\mu A$.

The value of the resistor $R_5$ is given by the following relationship:

$$I_{R_4} = I_{B2} + I_{R_5} = 20{,}7\,\mu A$$

$$R_4 = \frac{V_{BP} - V_{BE2}}{I_{R_4}} = \frac{5{,}8 - 0{,}6}{20{,}7 \cdot 10^{-6}} = 250k\Omega \qquad \text{Eq. 7.7}$$

$$R_3 = \frac{V_{BE2}}{I_{R_5}} = \frac{0{,}6}{14 \cdot 10^{-6}} = 43k\Omega$$

The values of resistors taken into account are show in Table 7.1.

Table 7.1

| | |
|---|---|
| $R_1$ | 33kΩ |
| $R_2$ | 100kΩ |
| $R_3$ | 100kΩ |
| $R_4$ | 270kΩ |
| $R_5$ | 47kΩ |
| $R_6$ | 56kΩ |
| Tolerance: 5% Power: ¼ W | |

Regarding the capacitor $C_1$, this value is fixed in order to turn on the transistor after a pressure of the button of 3 second.

If the transistor is in off state, the maximum voltage value on $R_5$ is:

$$V_{C1\max} = (V_{BP} - V_{out}) \cdot \frac{R_5}{R_5 + R_4} = (5.8 - (-5)) \cdot \frac{47k}{47k + 270k} = 1,6V \qquad \text{Eq. 7.8}$$

This one is the maximum value that could be reached by $C_1$, but the real maximum value is lower because the base-emitter junction clamps the voltage to $V_{BE2}$. Remember that the voltage on the capacitor change according to the equation Eq. 7.9.

$$V_{C1}(t) = V_{C1\max} (1 - e^{-\frac{t}{\tau}}) \qquad \text{Eq. 7.9}$$

Where $\tau$ is the constant time given by :

$$\tau = R_{eq} \cdot C_1$$
$$R_{eq} = R_4 \,//\, R_5 = 40k\Omega \qquad \text{Eq. 7.10}$$

The value of the capacitor is:

$$V_{C1}(t) = 0,6V$$
$$t = 3\sec. \qquad \text{Eq. 7.11}$$

$$C = \frac{t/R_{eq}}{\ln\left(\frac{V_{C1\max}}{V_{C1\max} - V_{C1}(t)}\right)} = 216\mu F$$

$$r_\pi = \frac{\beta V_T}{I_{C2}} = 113k\Omega \qquad \text{Eq. 7.12}$$

$$R_p = \frac{1}{\frac{1}{R_5} + \frac{1}{R_4} + \frac{1}{r_\pi}} = 29,6k\Omega$$

The capacitor used in the project is a 220μF with a rated voltage of 25V.

## 7.3. Simulation and experimental measurements

Figure 7.3 shows what happen when the machine is in OFF state and the on/off button T is pushed, $V(T) = 1$. Therefore, the npn transistor $Q_1$ turn on and the driver controller regulates the output voltage of the power supply to -5 V, V(SMPS). In the same time the microcontroller goes on and led high the control signal STATE, that keeps on $Q_1$ for indefinite time. In this way, when the on/off button is released the SMPS continues to power all the system.
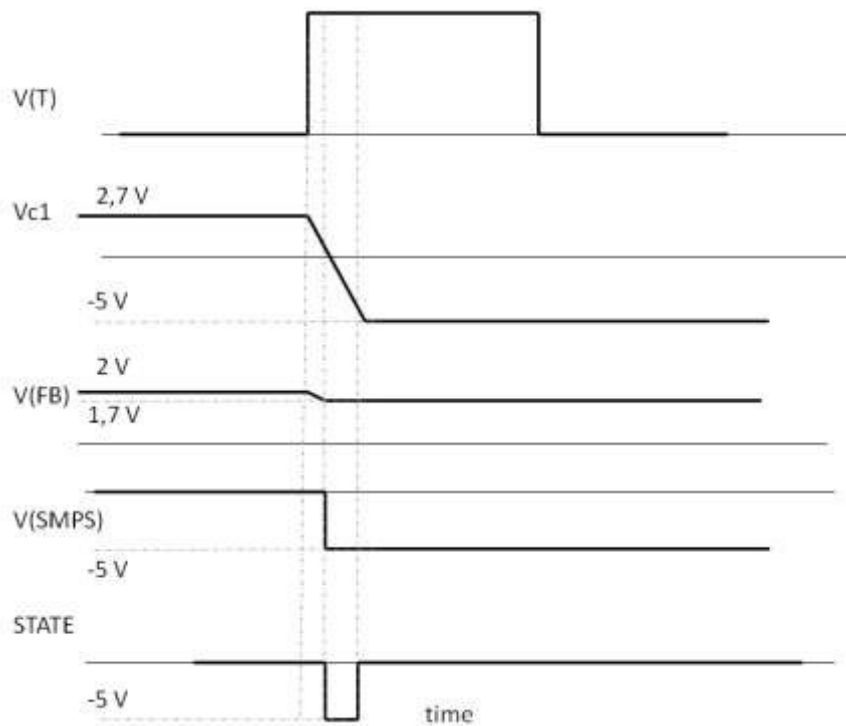
Figure 7.3: Detail of turn on.
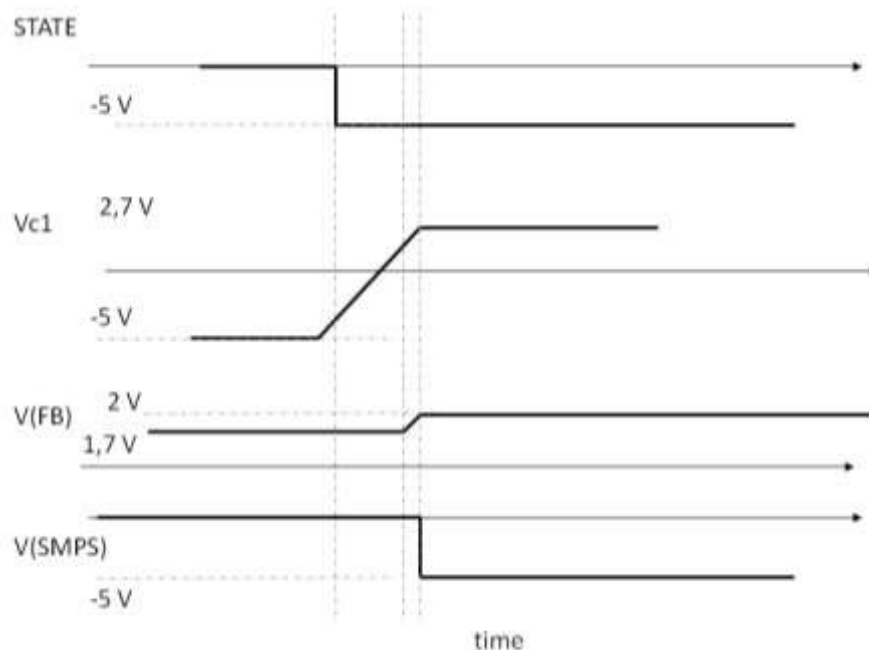


Figure 7.4: Auto turn off.

An other phase is when the washing cycle is finished, the SMPS goes in low power consumption mode and after two minute of inactivity, the status of control signal STATE by the microcontroller goes low and the npn transistor $Q_1$ turns off. The diode D turns on, so the feedback signal of the driver controller is modified.

In this way, a great current is forced in the feedback input pin and the power MOSFET and the SMPS goes in off state, see Figure 7.4.

After that, a model of the circuit proposed has been implemented in a PSpice simulator, also control driver and the flyback converter has been implemented by means of the ABM library block, and the same has been done for passive components that described the behaviour of the system.
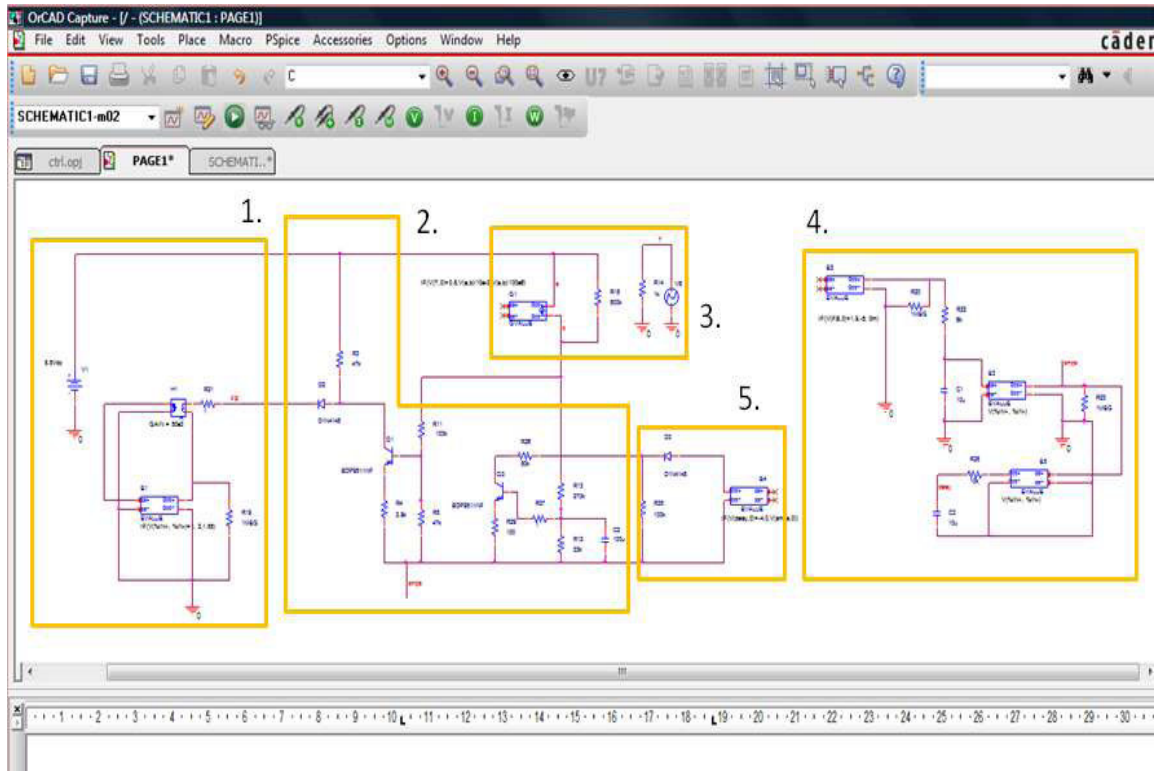


Figure 7.5: Electrical circuit in a PSpice simulator.

In Figure 7.5 is shown the circuit used for the simulation in PSpice and the yellow blocks highlight the most important part of the system:

1. Control driver of the converter (LNK363)

2. Proposed circuit to control the state of the SMPS

3. Start button ( T )

4. The output stage of Flyback converter.

5. Microcontroller.

In  Figure 7.6 and Figure 7.7 are shown the results according, respectively, to Figure 7.3 and Figure 7.4.
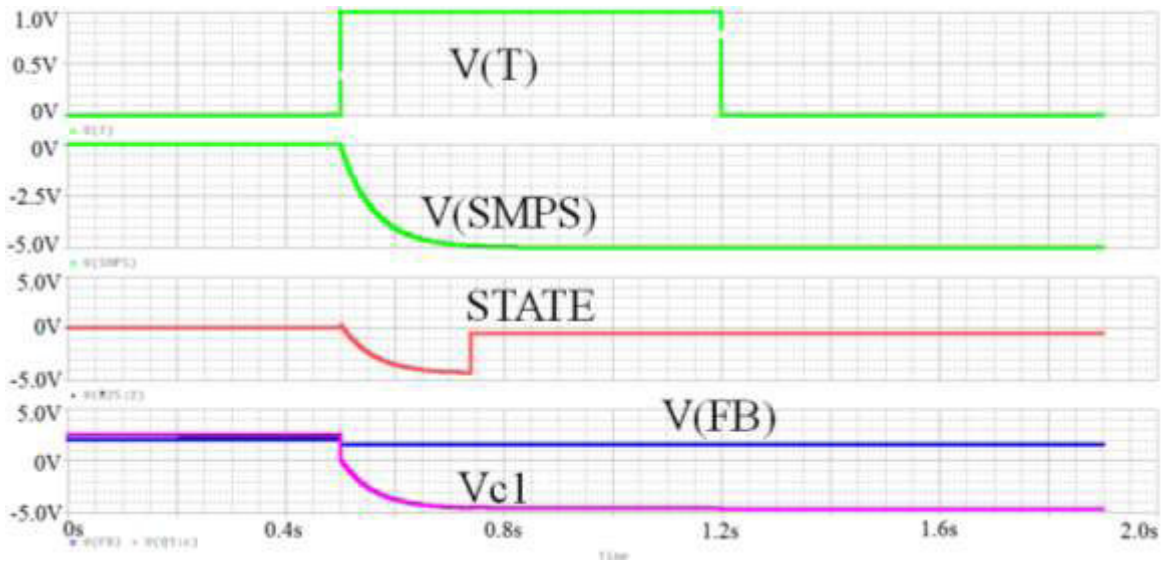
Figure 7.6: Simulation of the turn on.
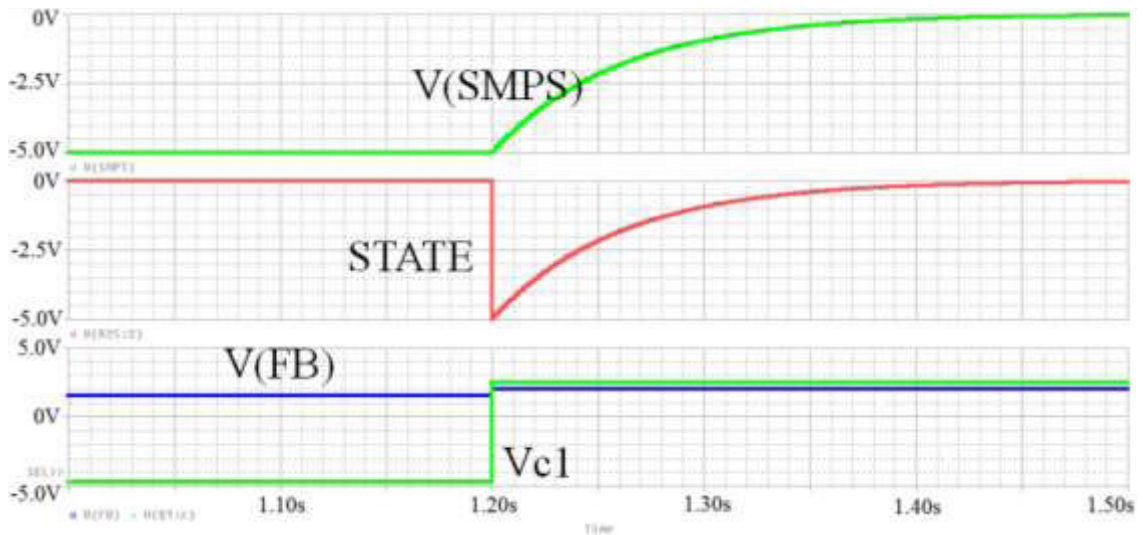


Figure 7.7: Simulation detail of the turn off from microcontroller.
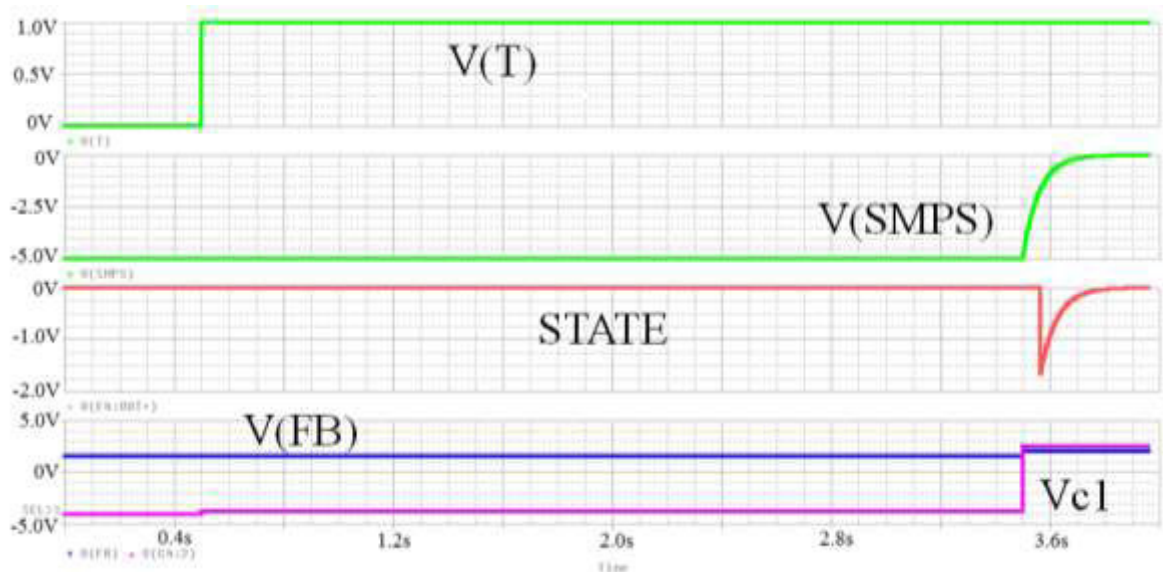


Figure 7.8: Simulation of a turn on and turn off by push button (mechanical operation).

In the last picture is simulated the turn off of the SMPS by means of a mechanical operation, or rather pushing the start button of the machine for a long time, about 3 second. The SMPS goes in off state, because the transistor Q2 turn on with a delay time due to the charge of the capacitor $C_1$, then the transistor Q1 turn off and so the output of the SMPS goes low.

A prototype of the system has been realized, in Chapter 8 will be discussed in more details. Experimental measurements of the signals that drive the state of the SMPS were stored by means an oscilloscope. In the following pictures are shown the measurements regarding the turn on of the SMPS by means of mechanical operations (by pushing the start button) Figure 7.9. As said before the collector voltage of the transistor $Q_1$ goes in the saturation region with a $V_{CEsat}$, the SMPS feedback is enabled and the output voltages growth.
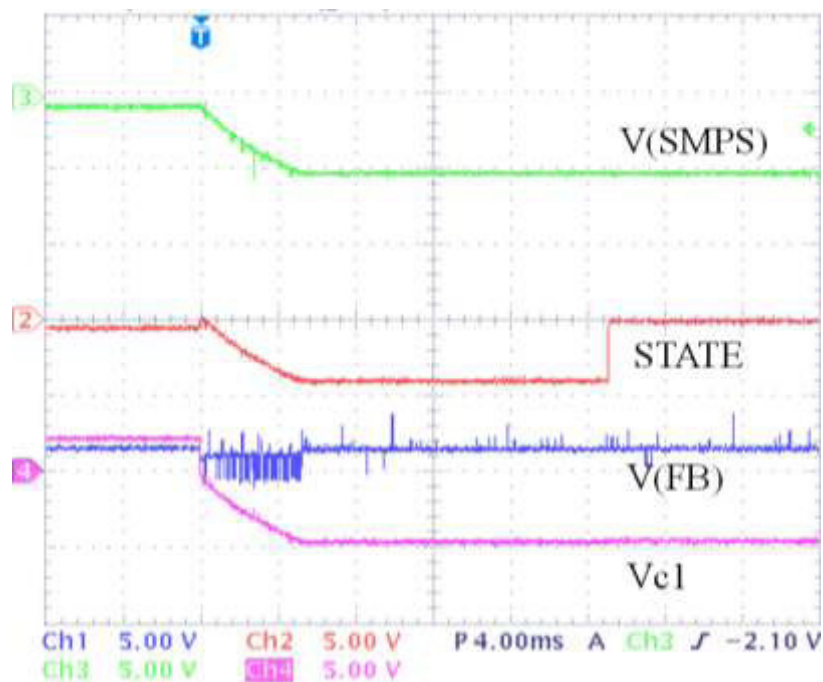


Figure 7.9: Detail of turn on measurement.

In Figure 7.8, the microcontroller puts in a low level the output PIN that drive $Q_1$, after two minute of inactivity of the washing machine, in this way the SMPS is turned off.
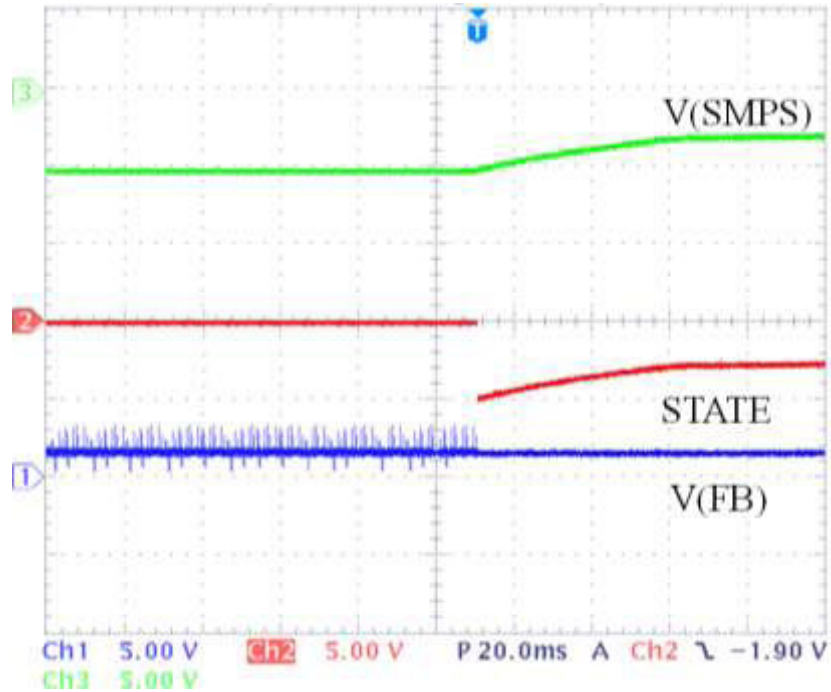
Figure 7.10: Measurement of the turn off from microcontroller.

In Figure 7.11 instead is shown the turn off by a mechanical operation and so pushing the start button.
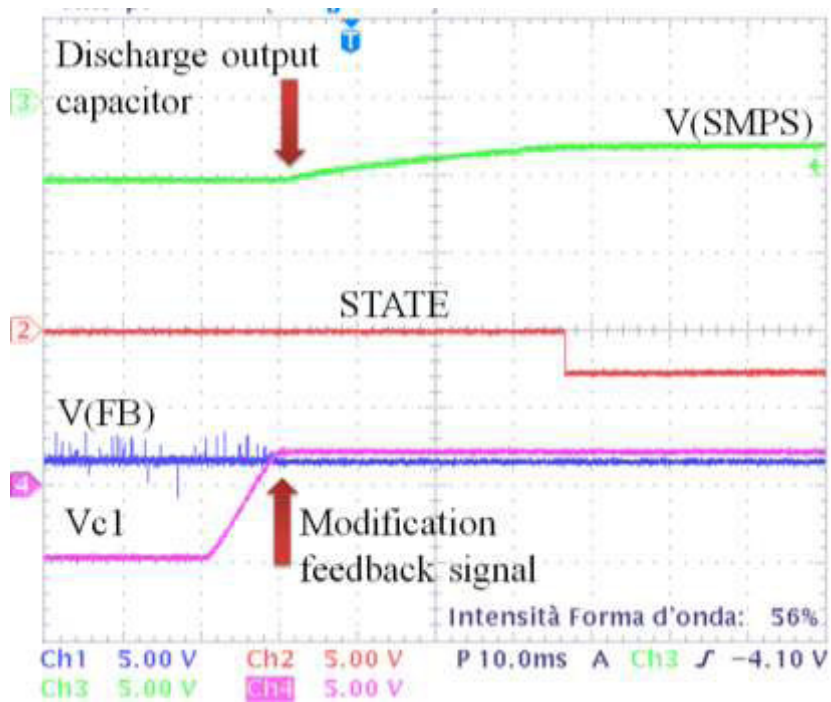


Figure 7.11: Measurement of turn off from mechanical operation.

# Chapter 8

Development of a prototype and experimental measurements

## 8. Introduction

A washing machine is a system composed by 4 most important parts, as it is shown in Figure 8.1.These are the SMPS, the user interface, the actuator and the input sensor circuits. The core of the system is the **user interface** where a microcontroller control the whole system; the **actuator** circuits are composed by relays and triacs driving the heater resistor, the door lock, the drain pump and electro valves.

The **input sensor** circuit allows to control the status of the machine as the motor speed, the open door, the heater temperature and other.

The focus of the research is on the auxiliary SMPS part, that supplies all logical parts and driver circuits.
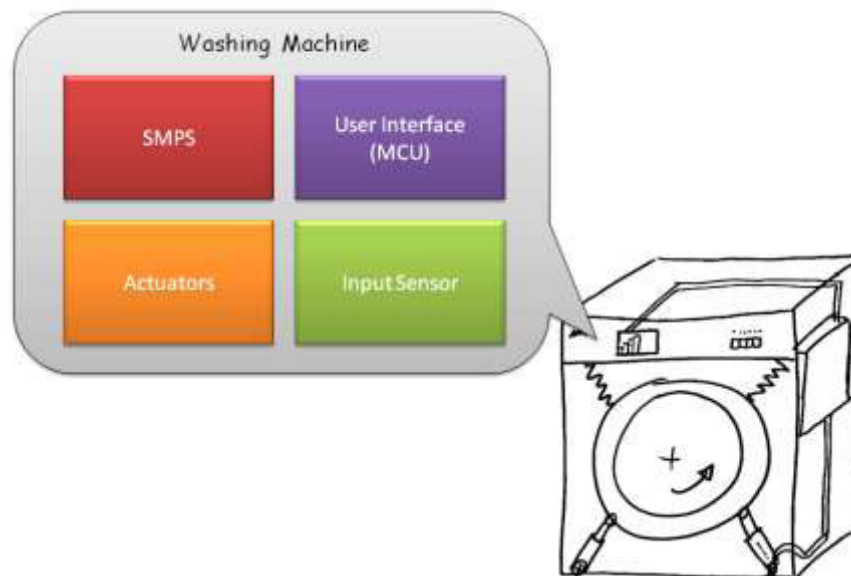


Figure 8.1: Most important parts of a washing machine.

A prototype of the auxiliary SMPS, and also the user interface and power control for washing machine has been developed, see Figure 8.17, in particular only the SMPS part of the system is discussed because the other parts are not involved in the topics of the research.

## 8.1. Electrical schematics

In order to develop schematics and the pcb, the program used is PADS logic and PADS layout, respectively. In the pictures from Figure 8.2 to Figure 8.4 are shown the electrical circuit of the SMPS and other parts regarding the external control actuator and the user interface of a washing machine.
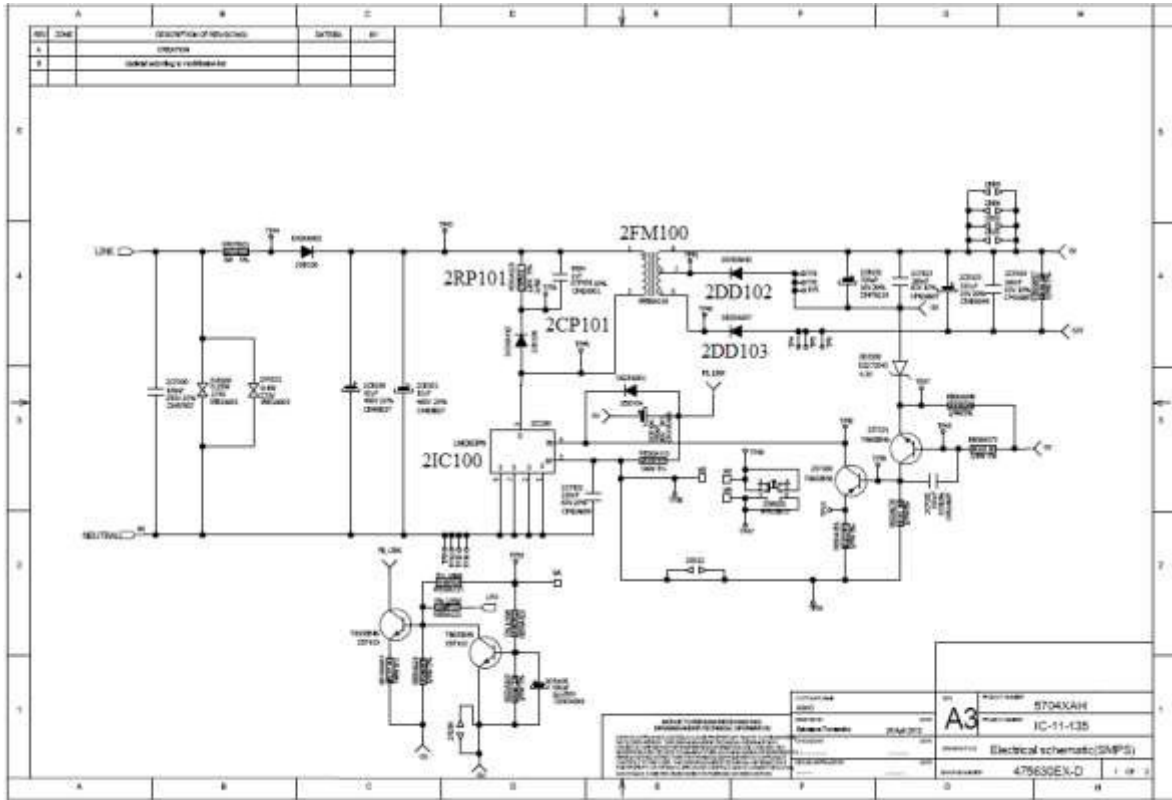
Figure 8.2: electrical schematic of the SMPS.
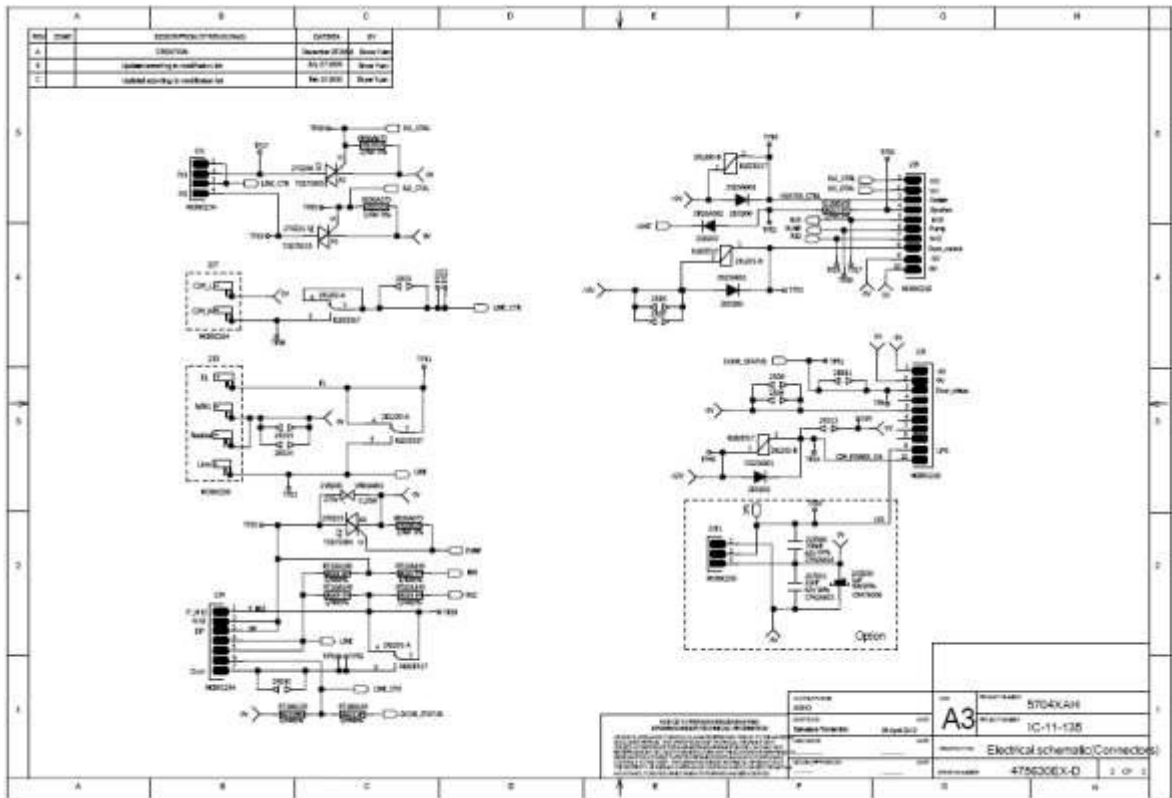
Figure 8.3: electrical schematic of the actuators.
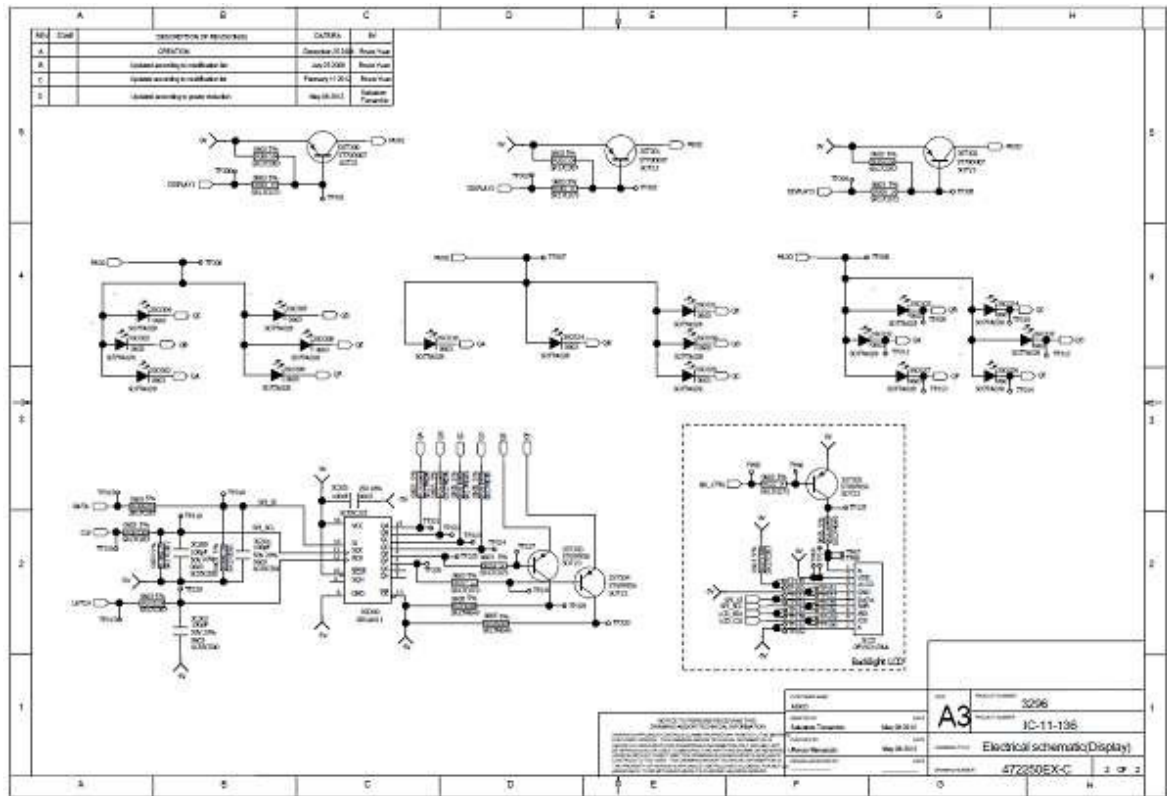
Figure 8.4: electrical schematic of the display interface.

## 8.2. Test for project validation

In order to verify the operation of the SMPS in every environmental and electric condition some tests have been performed, from environmental point of view in a climatic chamber in hard environmental conditions, while from the electrical point of view the SMPS has been stressed in different load condition up to the limit value of the power.

### 8.2.1.    Measurements of the electrical specifications

The power consumption of some parts of the washing machine have been measured by means a power meter, and in Table 8.1 are depicted the results.

Table 8.1

|  | OFF mode [W] | ON mode [W] | Stand by mode [W] |
|---|---|---|---|
| **SMPS** | 70.0E-3 | 400.0E-3 | 300.0E-3 |
| **Actuator** | 0 | 80.0E-3 | 0 |
| **User interface** | 0 | 560.0E-3 | 100.0E-3 |
| **Sensing** | 160.0E-3 | 350.0E-3 | 350.0E-3 |
| **EMI filter** | 78.0E-3 | 78.0E-3 | 78.0E-3 |
| **Washing Machine** | 308.0E-3 | 1.46 | 828.0E-3 |

Subsequently, the power supply has been tested in different loaded conditions, and both the power consumption and the efficiency of the converter were evaluated. Hence, the voltage and the current in the converter have been measured at maximum output load conditions.

Table 8.2

| $P_{IN}$ [W] | Efficiency [%] | $P_{OUT}$ [W] | LOAD [%] |
|---|---|---|---|
| 6.68 | 75.90% | 5.07 | 100% |
| 5.29 | 75.80% | 4.01 | 79% |
| 4.25 | 75.36% | 3.20 | 63% |
| 3.20 | 74.06% | 2.37 | 47% |
| 2.47 | 71.26% | 1.76 | 35% |
| 1.33 | 64.29% | 0.86 | 17% |
| 0.85 | 52.41% | 0.45 | 9% |

Table 8.3

| LOAD 1 [%] | LOAD 2 [%] | Pout 1 [W] | Pout 2 [W] |
|---|---|---|---|
| 100% | 100% | 1.55 | 3.52 |
| 78% | 80% | 1.21 | 2.80 |
| 71% | 60% | 1.10 | 2.10 |
| 52% | 44% | 0.81 | 1.56 |
| 36% | 34% | 0.56 | 1.20 |
| 20% | 16% | 0.31 | 0.55 |
| 9% | 9% | 0.15 | 0.30 |

The electrical performance of the converter has been measured, and the main results are given in Table 8.2, and Table 8.3, in  Figure 8.5 to Figure 8.7. In particular, Figure 8.5 shows the efficiency of the auxiliary SMPS prototype, that is greater than 70% with an output power load of 2.20 W (about 30% of the maximum output load).

The Figure 8.6 shows the relationship between the input power and the output power, and Figure 8.7 shows the power distribution in the two outputs.
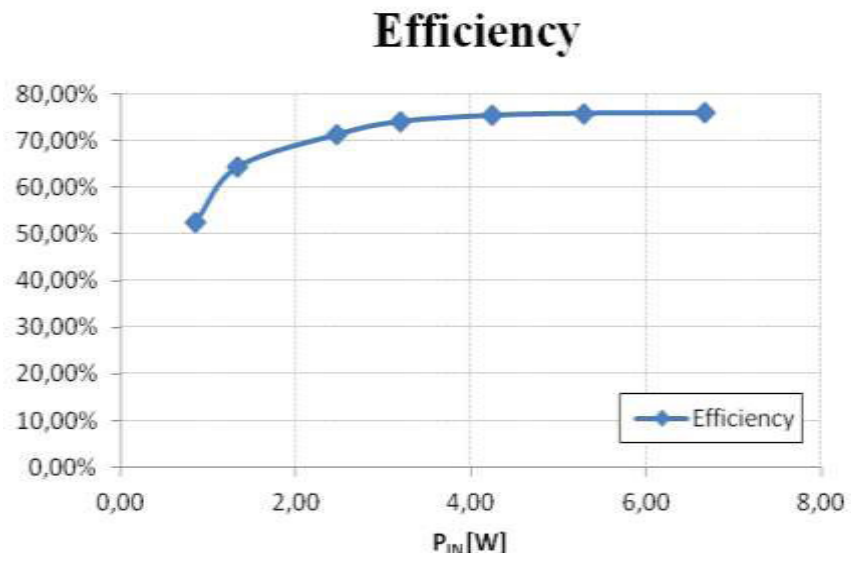
## Efficiency



Figure 8.5: Efficiency of the Flyback converter.

## $P_{IN}$
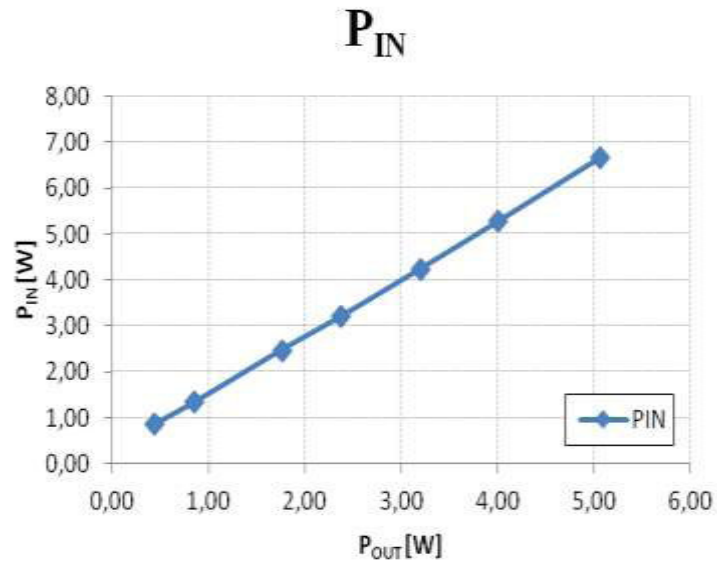


Figure 8.6: Relation between input power and output power.

## $P_{OUT}$ vs. OUT 1 and OUT 2
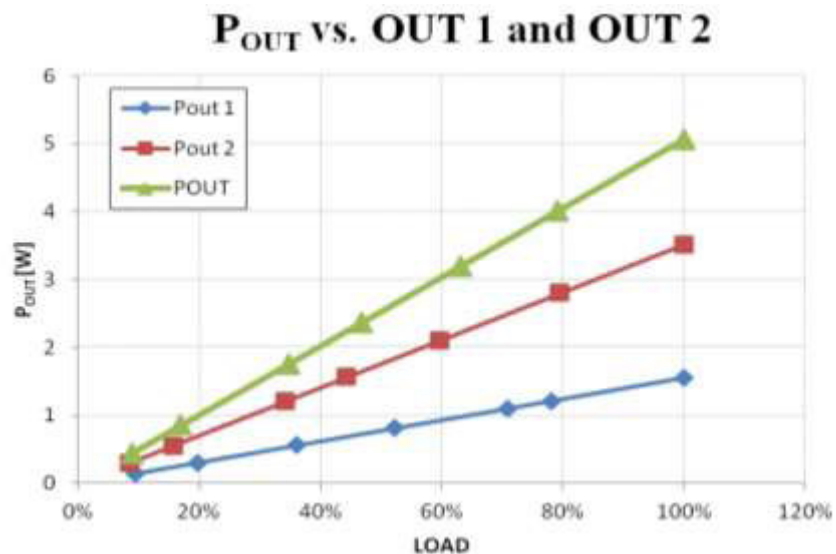


Figure 8.7: Power distribution in the outputs.

The two output voltages, -5 V and -15 V, and the respective ripple voltages are shown from  Figure 8.8 to Figure 8.10.
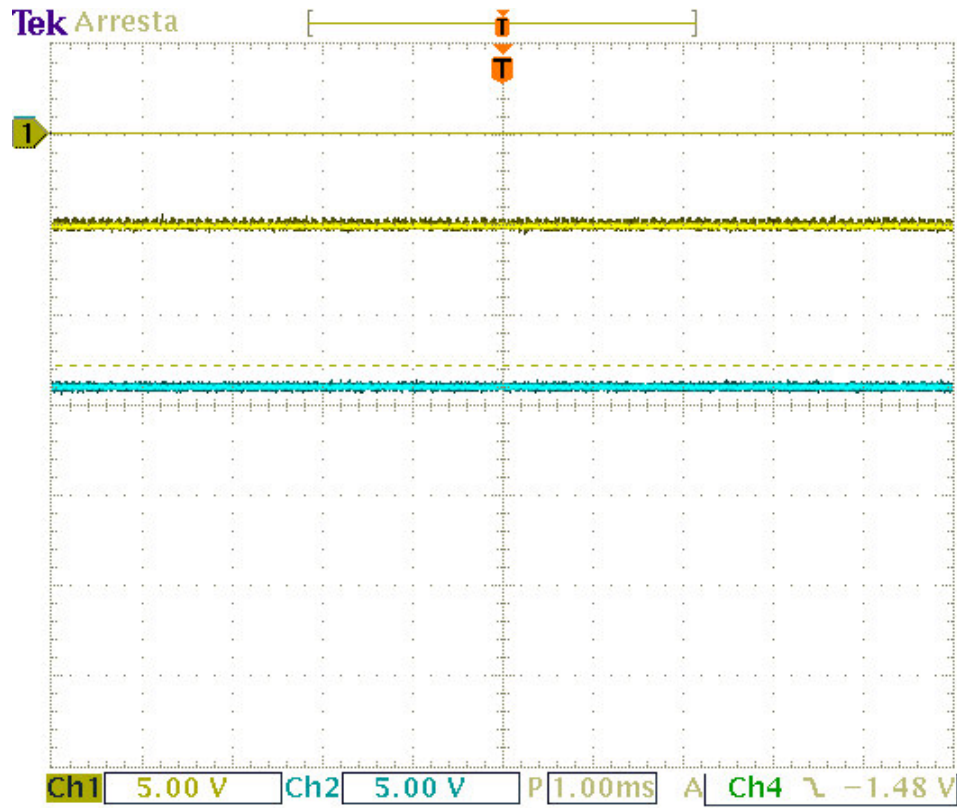


Figure 8.8: Ch 1: 5 V/div, output Flyback voltage -5 V; Ch 2: 5 V/div, output Flyback voltage -15 V; Time 1,0 ms/div;
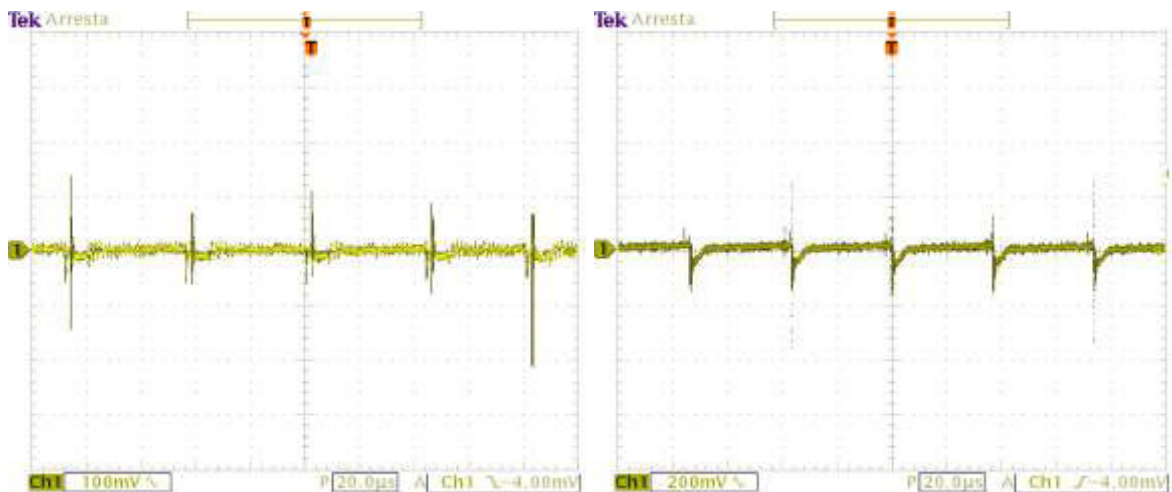


Figure 8.9: Ch1: 100mV/div, output voltage ripple -5 V; Time: 20 μs

Figure 8.10: Ch1: 200mV/div, output voltage ripple -15 V; Time: 20 μs

The input voltage, input current and the output voltage -5 V has been measured in two different case: the first in off mode (Figure 8.11) , and second in on mode with the maximum load in the output, see pictures from Figure 8.12 to Figure 8.16.
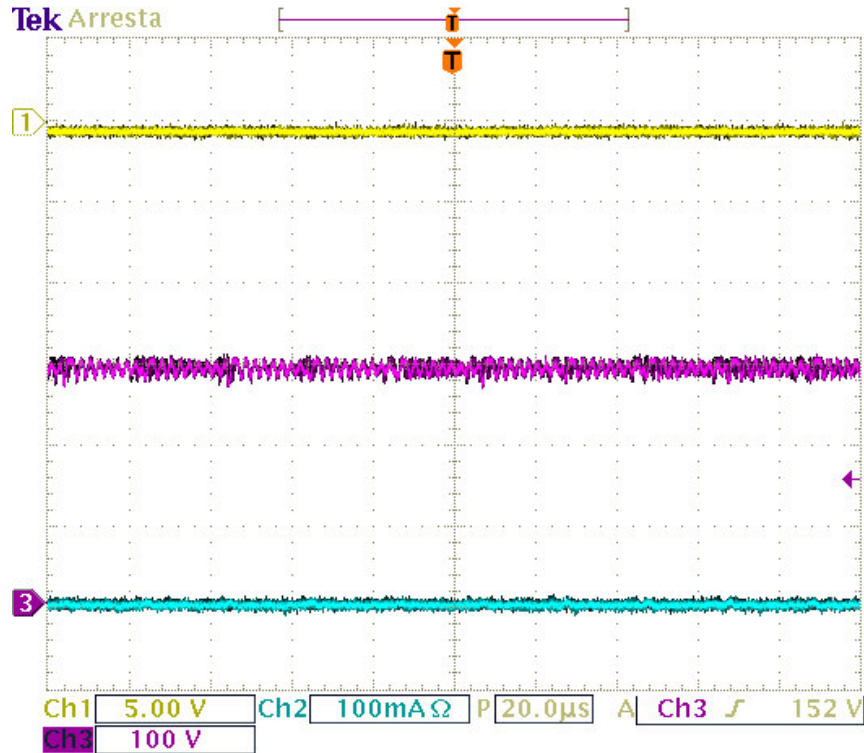


Figure 8.11: Ch1:5 V/div output voltage -5V; Ch2: 100 mA/div drain current;
Ch3: 100 V/div drain-source voltage ;Time 20μsec.
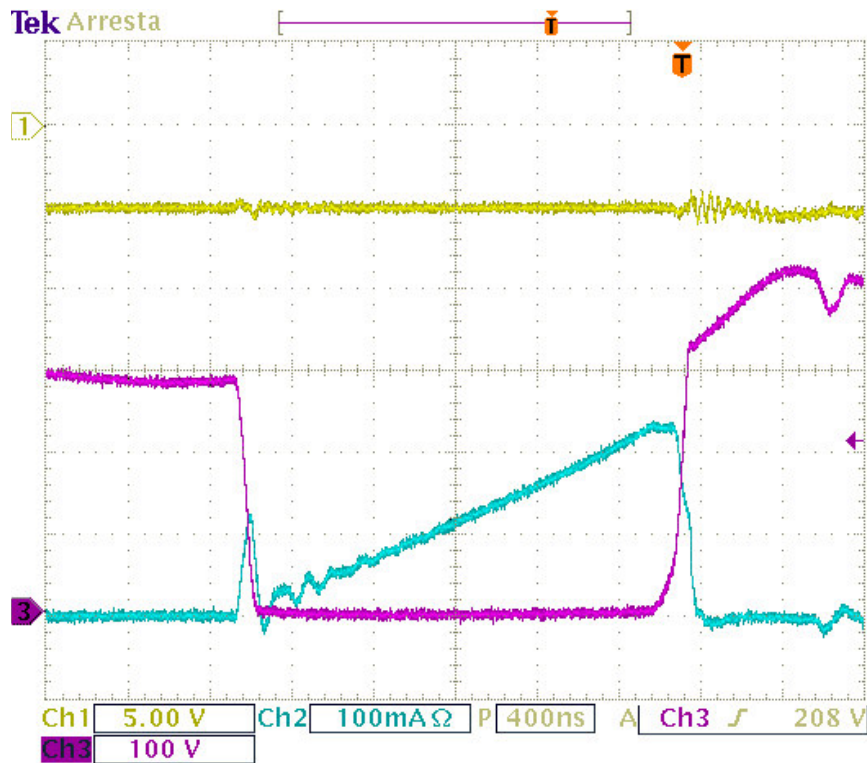


Figure 8.12: Ch1:5 V/div output voltage -5V; Ch2: 100 mA/div drain current;
Ch3: 100 V/div drain-source voltage ;Time 400nsec.
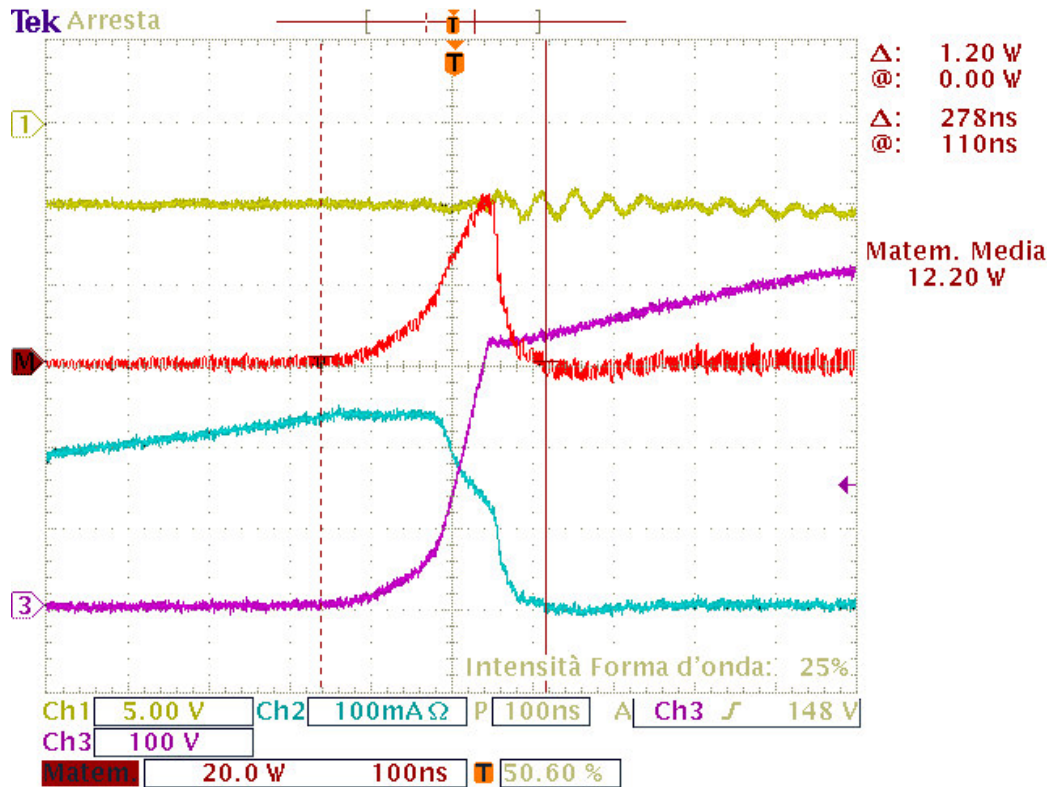
Figure 8.13: Turn off; Ch1:5 V/div output voltage -5V; Ch2: 100 mA/div drain current;

Ch3: 100 V/div drain-source voltage ;Mat: 20 W/div; Time 100nsec.
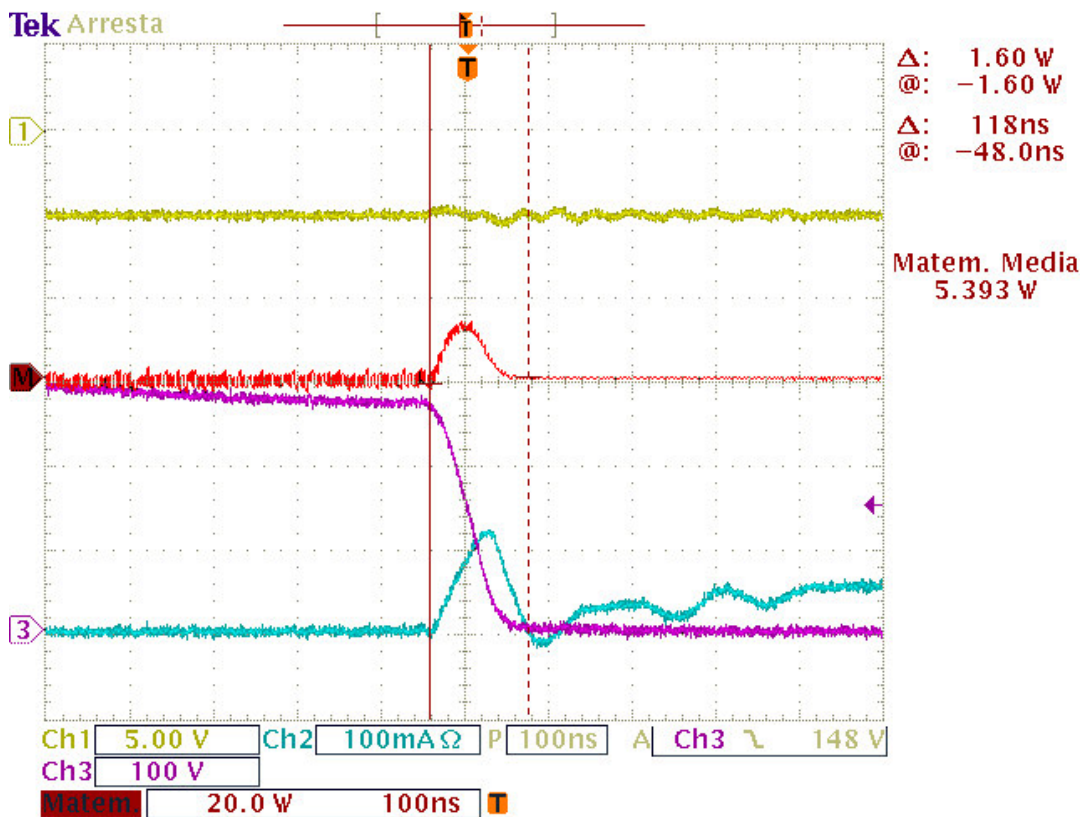


Figure 8.14: Turn on;  Ch1:5 V/div output voltage -5V; Ch2: 100 mA/div drain current;

Ch3: 100 V/div drain-source voltage ;Mat: 20 W/div; Time 100nsec.
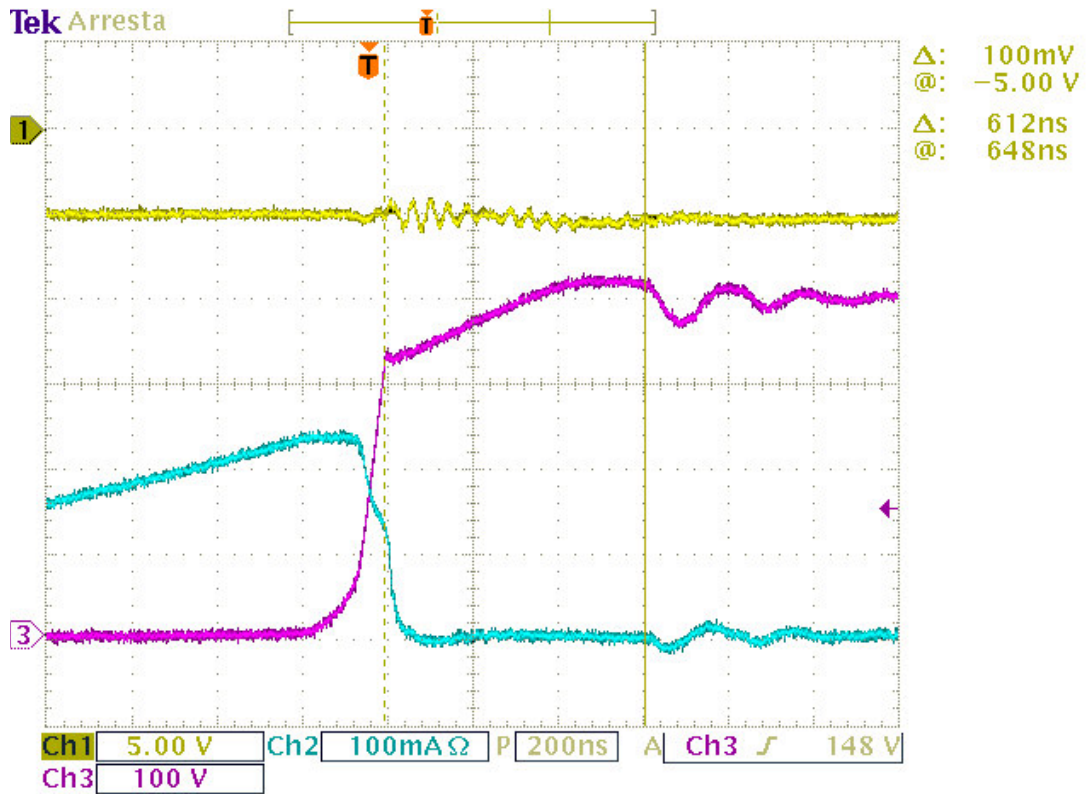
Figure 8.15: Detail drain voltage clamp; Ch1:5 V/div output voltage -5V; Ch2: 100 mA/div drain current;Ch3: 100 V/div drain-source voltage ; Time 200nsec.
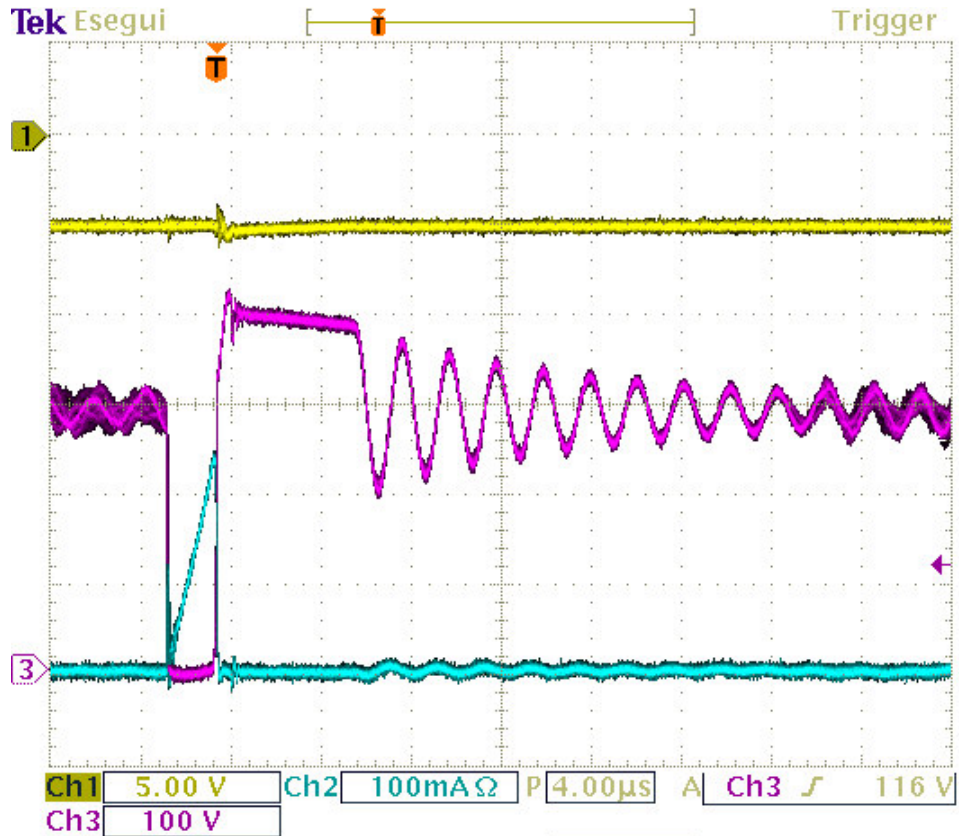


Figure 8.16: Detail of the off time; Ch1:5 V/div output voltage -5V; Ch2: 100 mA/div drain current; Ch3: 100 V/div drain-source voltage ; Time 4µsec.

### 8.2.2. Thermal analysis in climatic chamber at hard condition

The thermal analysis in a climatic chamber has been performed in the following environment conditions: temperature 70°C, and 50% of humidity for a time lasting 2 hours per cycle.

The electrical schematic of the circuit is depicted from Figure 8.2 to Figure 8.4, and the components under test, that are the most critically for the operation of the SMPS, and are listed in Table 8.4.

Table 8.4: Components

| Component | Description |
|-----------|-------------|
| 2DD102 | DD SB140 DO41 40V 1° (output -5V) |
| 2DD103 | DIODE SCHOTTKY BYV (output -15V) |
| 2IC100 | PWM CONTROLLER DIP8 LNK363PN |
| 2FM100 | TRANSFORMER EE10 2.52mH |
| 2RP101 | RSA 1/4 5% 220K H.T 24153224 (snubber resisto) |
| 2CP101 | CD.PLR 1NF 400V 10% P=5 (snubber capacitor ) |

Also, the test is performed in different electrical conditions of maximum and minimum load and different main voltages, minimum: 170V and maximum: 254V, Table 8.5.

Table 8.5: Test conditions

| 2 h (Time cycle) | | 2 h (Time cycle) | |
|------------------|---|------------------|---|
| Env. Conditions | Electrical Condition | Env. Conditions | Electrical Condition |
| 70°C / 50% | 170 V | 70°C / 50% | 254V |

The thermal test has been performed on four boards, and configured as in Table 8.6. Two different cases were taken into account at maximum and minimum load, and the boards are configured with all relays on and backlight always turning on for the maximum power, and all relays off and backlight off for minimum power.

These configurations have been implemented by shorting the transistor that drives the relay and the backlight in the first case, while in the second case by opening (removed from the pcb) these ones. The pictures from Figure 8.17 to Figure 8.19 show the hardware modification of the boards in order to configure the minimum and maximum power consumption.

Table 8.6: Board Configurations

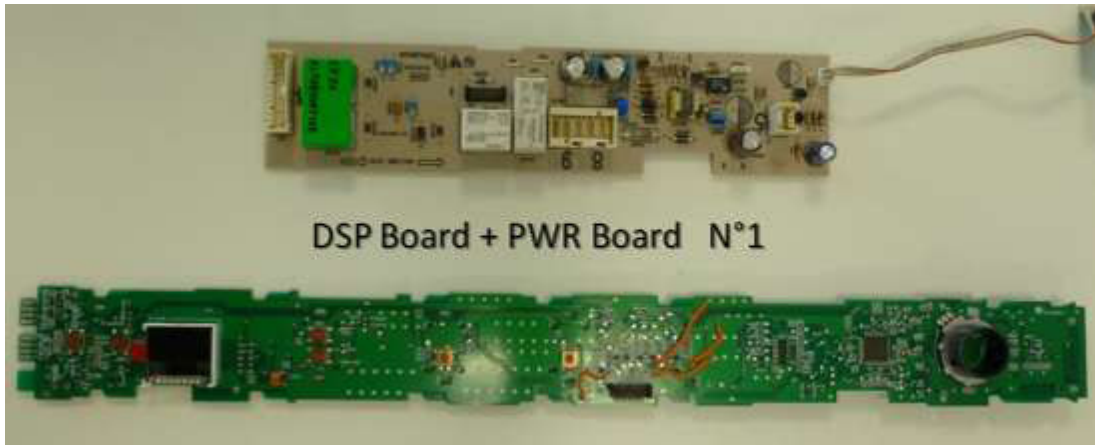| Sample | Backlight | Relay | Power |
|--------|-----------|-------|-------|
| Board 1 | ON | ON | MAX |
| Board 2 | OFF | OFF | MIN |
| Board 3 | OFF | OFF | MIN |
| Board 4 | ON | ON | MAX |



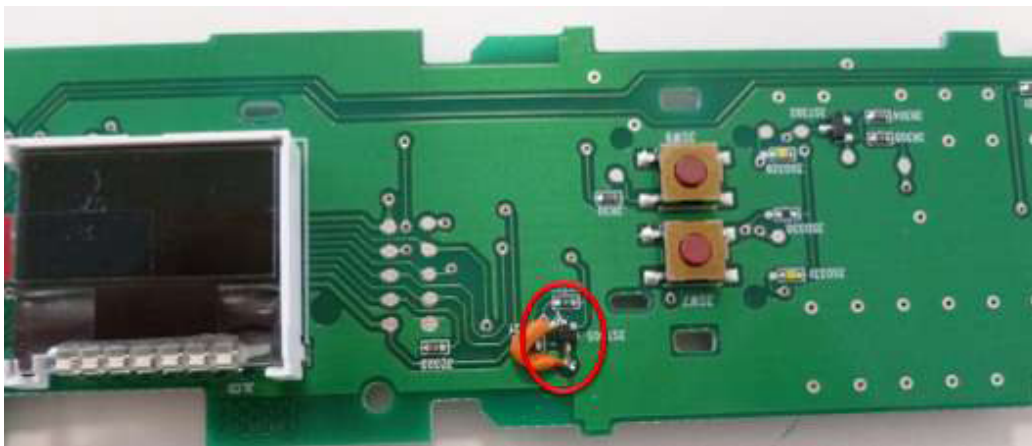Figure 8.17: Display board and Power board.
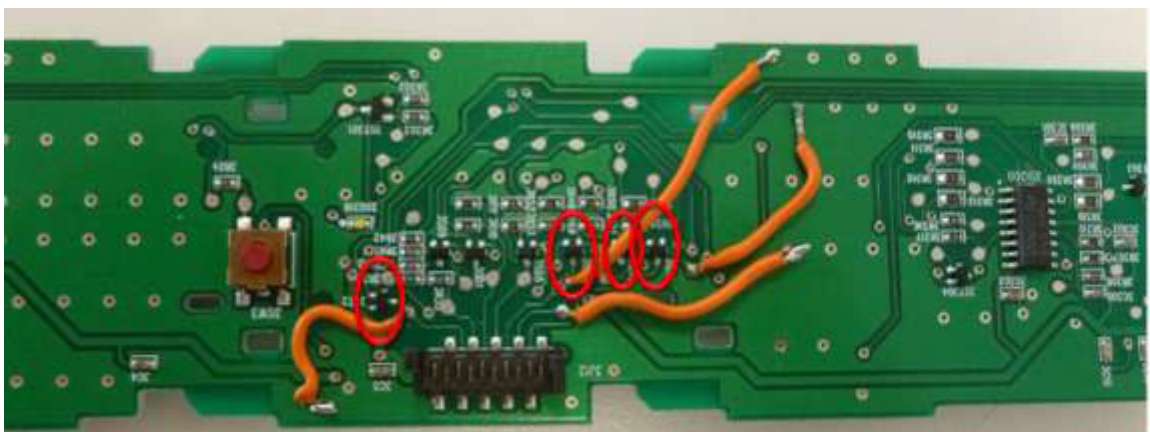


Figure 8.18: Modifications on the backlight.



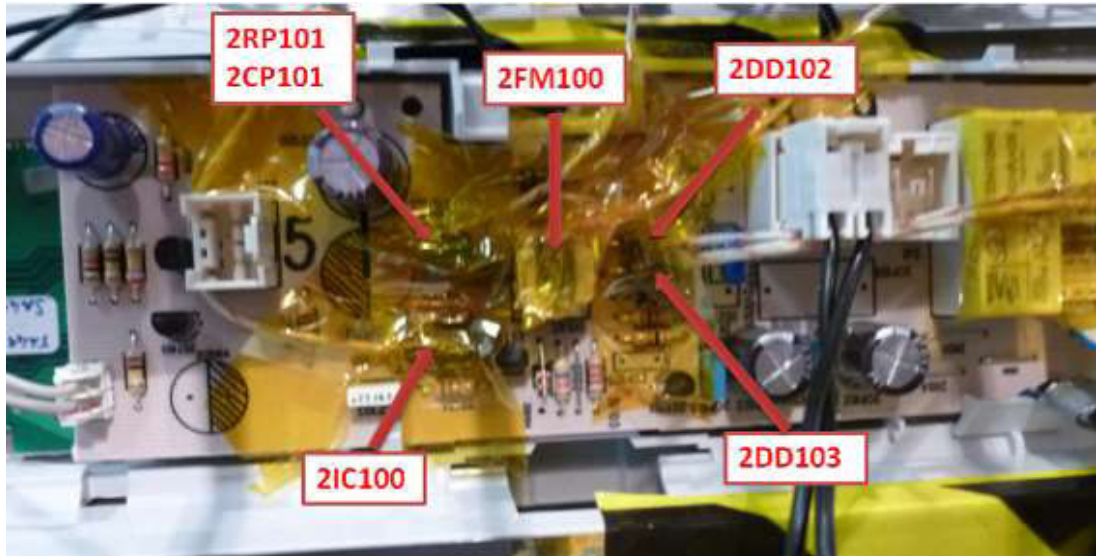Figure 8.19: Modification on transistor to drive the relay.

Figure 8.20: Details of the thermocouple's setup in the PWR board.

In Figure 8.21 and Figure 8.22 is shown the setup used for the thermal measurements, in the first picture two boards with a maximum power are positioned on the top side of the climatic chamber and two boards with a minimum power are positioned on down side.

In the second picture, Figure 8.22, the boards have been supplied by AC source in the electrical condition as reported in Table 8.5.
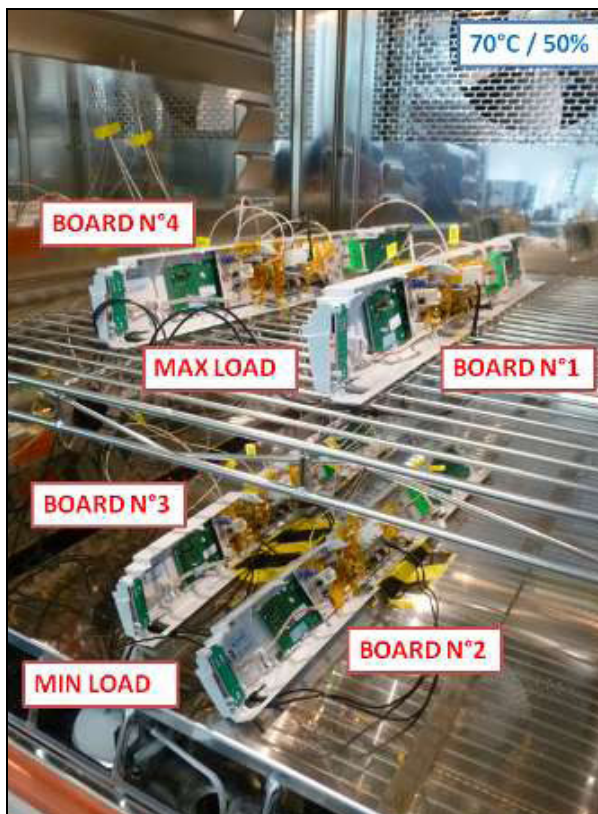


| Figure 8.21: Setup in climatic chamber. | Figure 8.22: Setup out climatic chamber. |

The results of the analysis are summarized in Table 8.7, where for each board and electrical condition has been detected the temperature of the critical components by means a thermocoupler type K, that has an accuracy of ±2.2 °C.

Table 8.7: Average temperature [read °C ±2.2°C]

| Component | Climatic Chamber T [°C] | | MAX LOAD | | | | MIN LOAD | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | Board N1 | | Board N4 | | Board N2 | | Board N3 | |
| Main voltage [V] | 170 | 254 | 170 | 254 | 170 | 254 | 170 | 254 | 170 | 254 |
| 2DD102 | 72.21 | 73.27 | 78.87 | 79.29 | 79.98 | 80.46 | 75.49 | 75.68 | 74.96 | 75.13 |
| 2DD103 | 72.21 | 73.27 | 79.86 | 80.34 | 80.71 | 81.19 | 74.91 | 75.06 | 75.17 | 75.39 |
| 2IC100 | 72.21 | 73.27 | 80.93 | 84.19 | 80.95 | 84.48 | 79.64 | 82.61 | 79.14 | 81.85 |
| 2FM100 | 72.21 | 73.27 | 78.18 | 79.05 | 77.78 | 78.42 | 74.94 | 75.33 | 74.80 | 75.13 |
| 2RP101 2CP101 | 72.21 | 73.27 | 77.01 | 77.64 | 79.65 | 80.89 | 75.53 | 76.12 | 74.41 | 74.65 |

Also, the waveform of the components temperatures are shown in the following graphs (Temperature vs. time), .
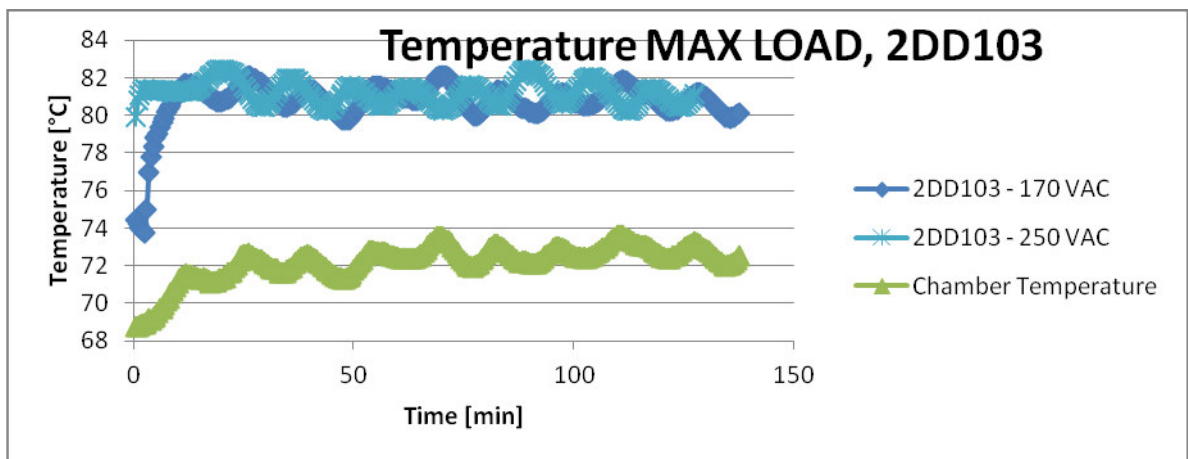


Figure 8.23: 2DD103 temperature at maximum load.
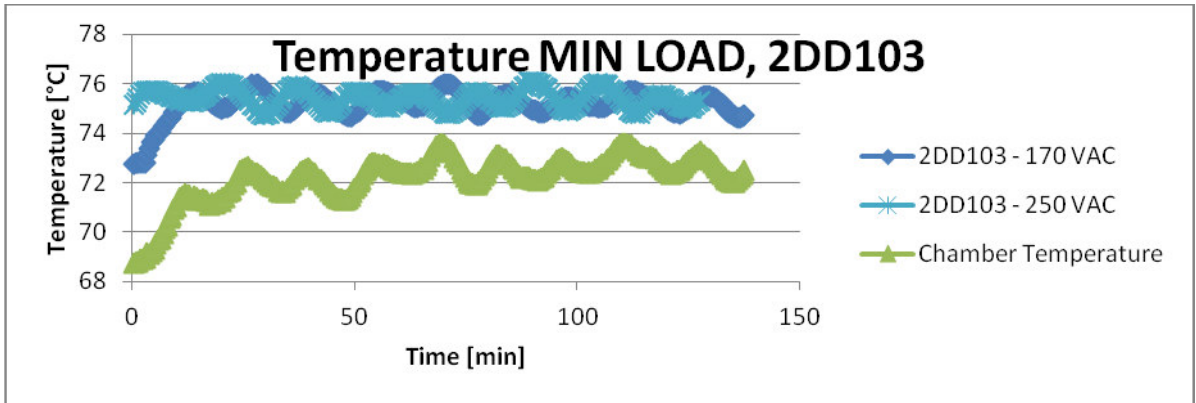
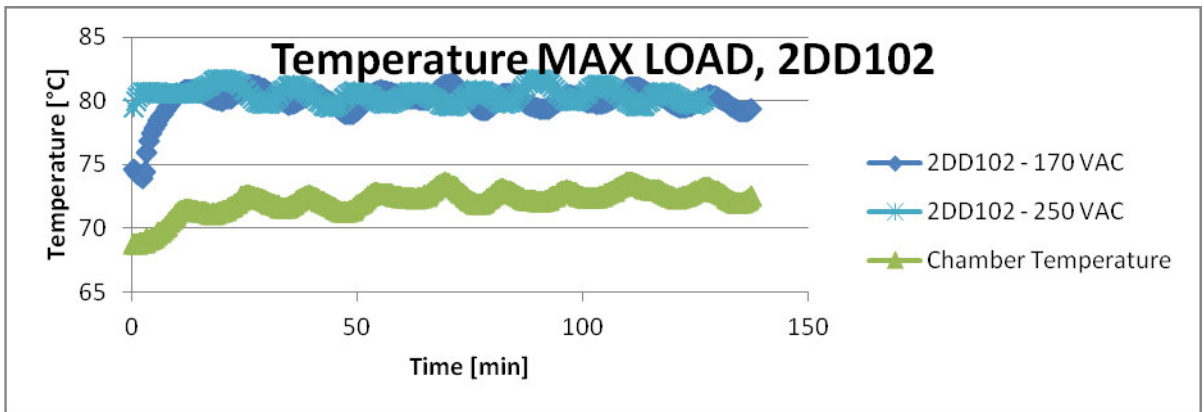Figure 8.24: 2DD103 temperature at minimum load.



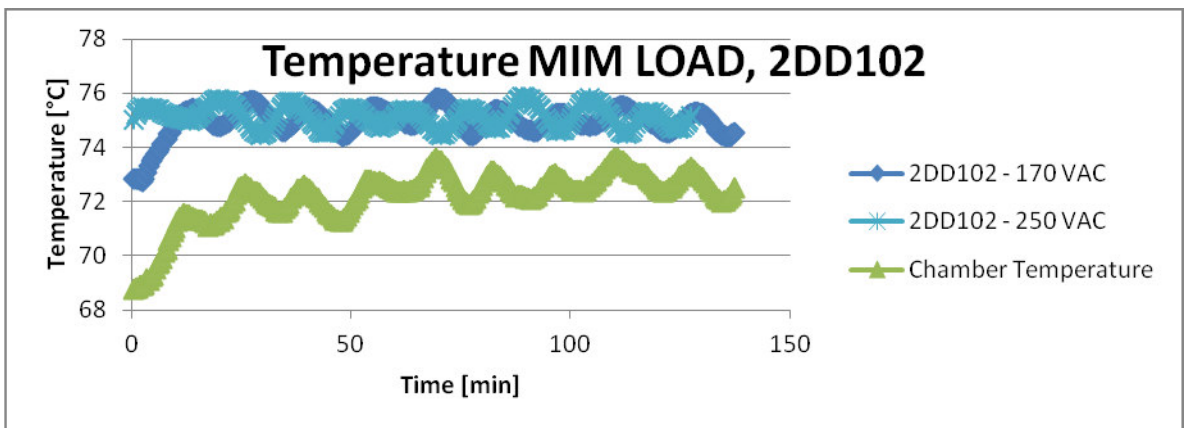Figure 8.25: 2DD102 temperature at maximum load.



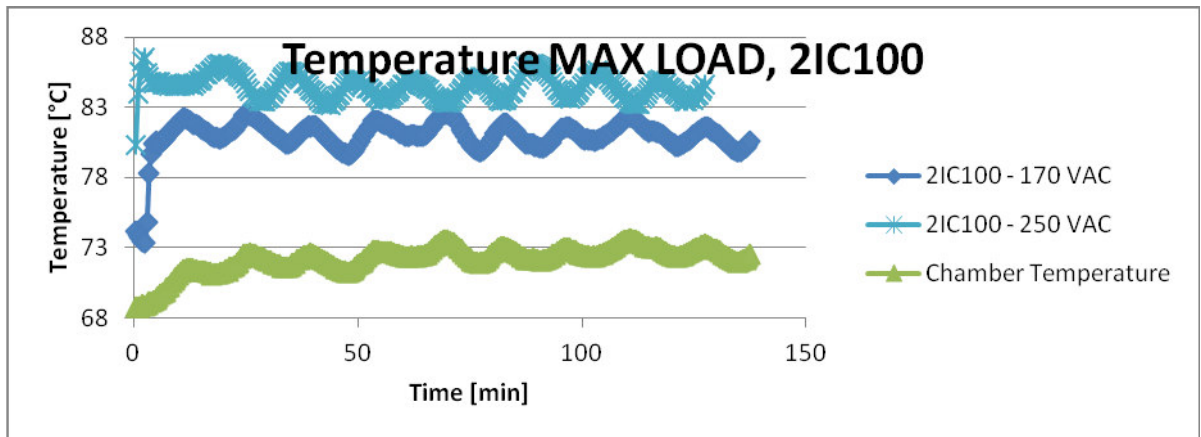Figure 8.26: 2DD103 temperature at minimum load.

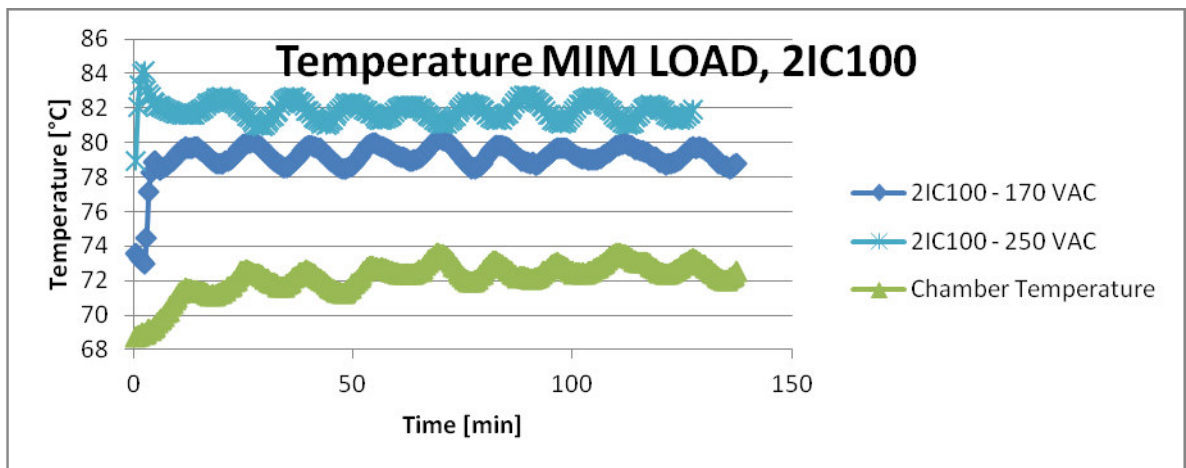Figure 8.27: 2IC100 temperature at maximum load.



Figure 8.28: 2IC100 temperature at minimum load.
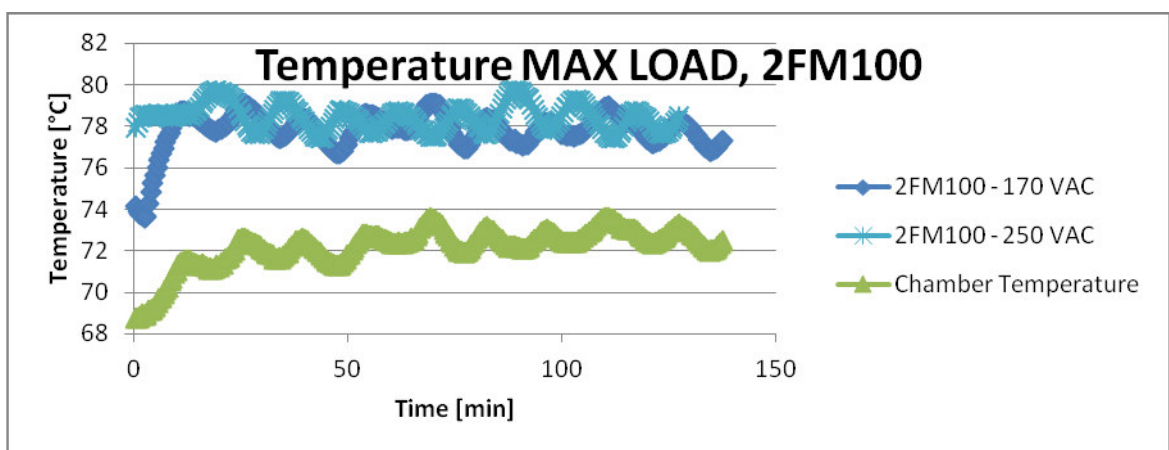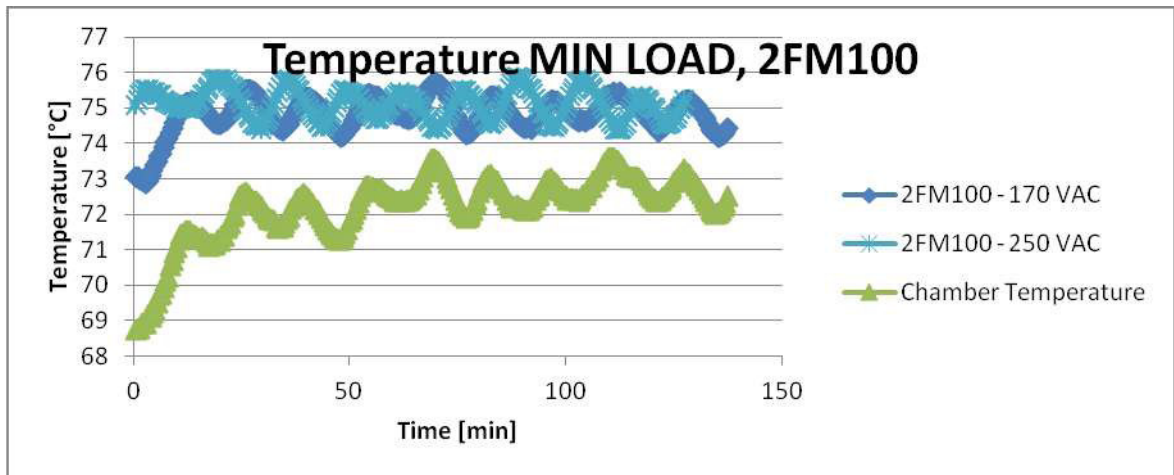


Figure 8.29: 2FM100 temperature at maximum load.

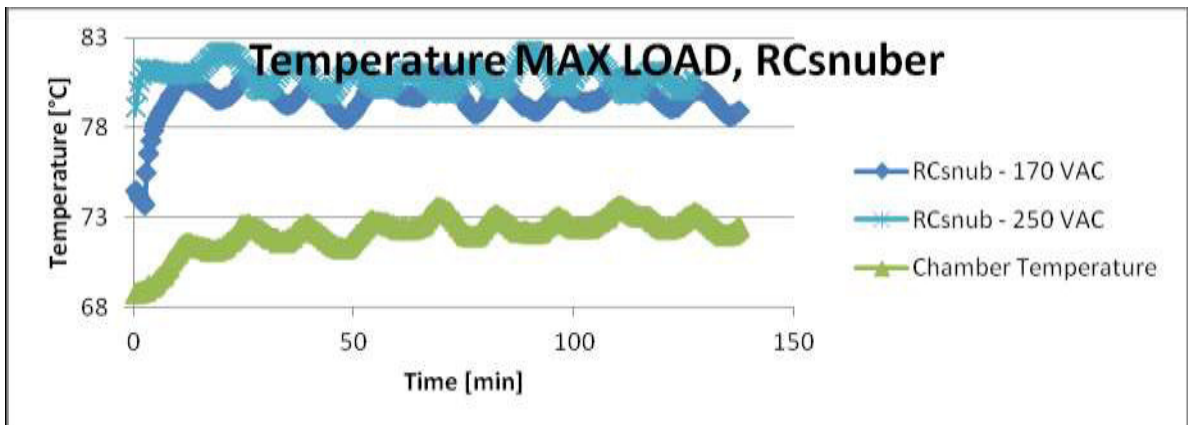Figure 8.30: 2FM100 temperature at minimum load.


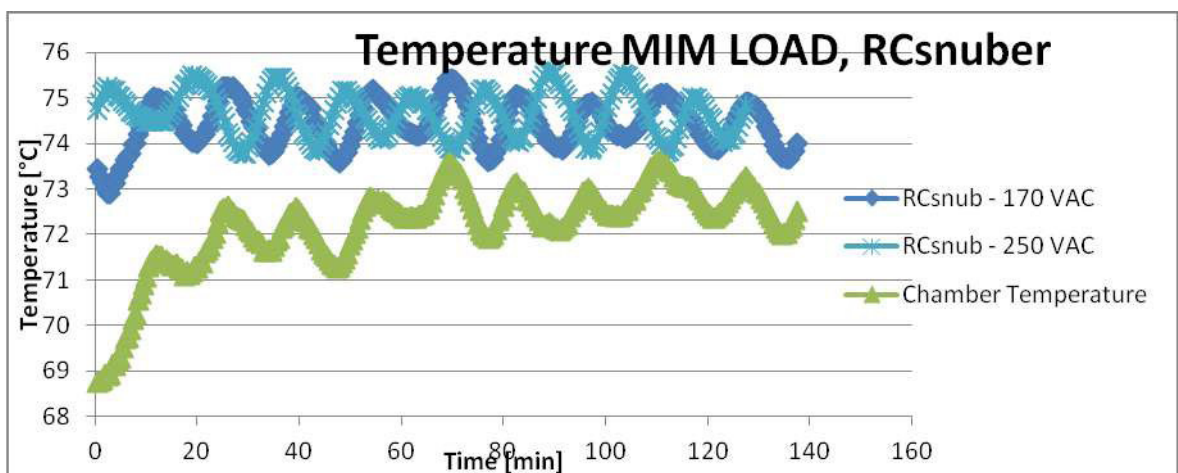
Figure 8.31: RC temperature at maximum load.



Figure 8.32: RC temperature at minimum load.

Moreover , the temperature measurements of the critical components in ambient conditions of 25°C temperature and 50% of humidity and with electrical condition of maximum output load, has been detected by means of an infra red camera.

Table 8.8

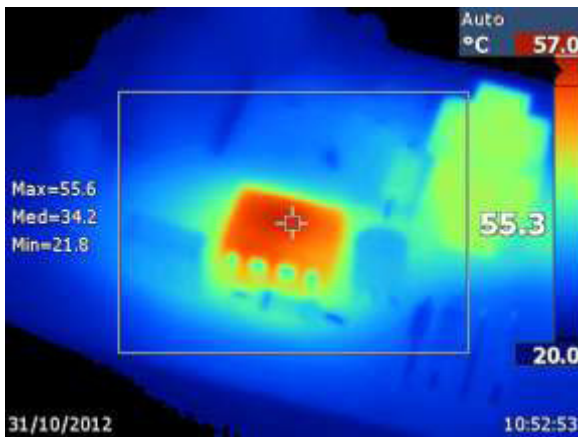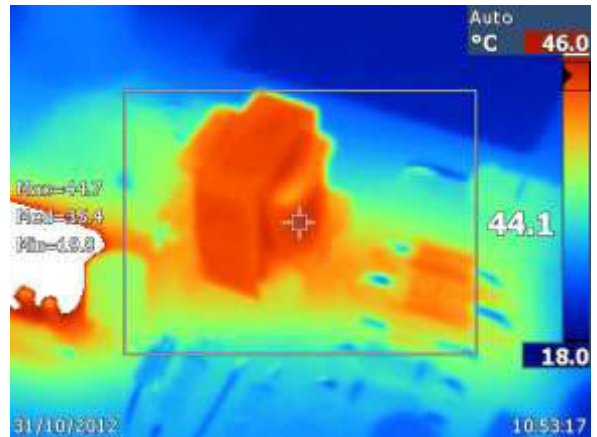| Board N°1 | MAX LOAD | |
|---|---|---|
| Component | Temperature [°C] | Main Voltage [V] |
| 2DD102 | 39.8 | 230 |
| 2DD103 | 40.6 | 230 |
| 2IC100 | 55.3 | 230 |
| 2FM100 | 44.1 | 230 |
| 2RP101 | 38.3 | 230 |
| 2CP101 | 32.3 | 230 |



Figure 8.33: 2IC100 temperature.



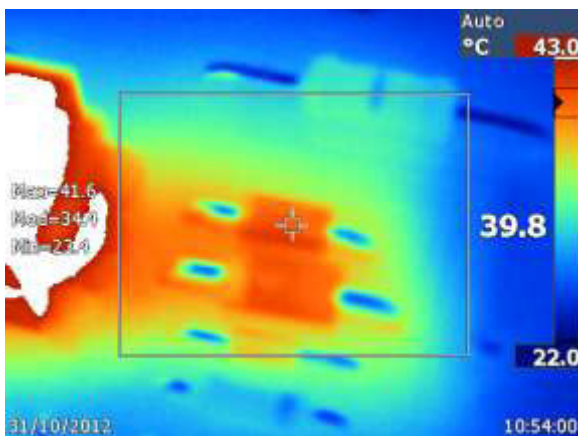Figure 8.34: 2FM100 temperature.



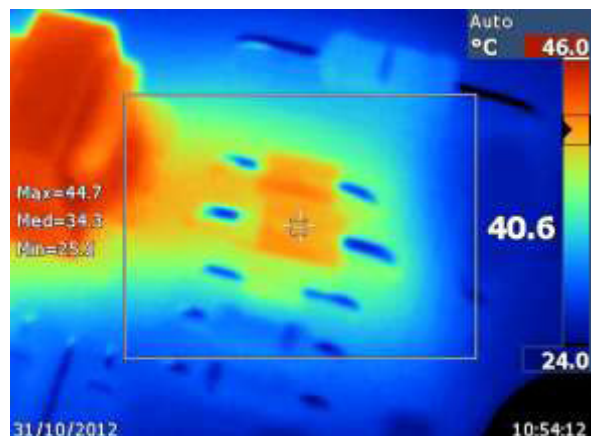Figure 8.35: 2DD102 temperature.
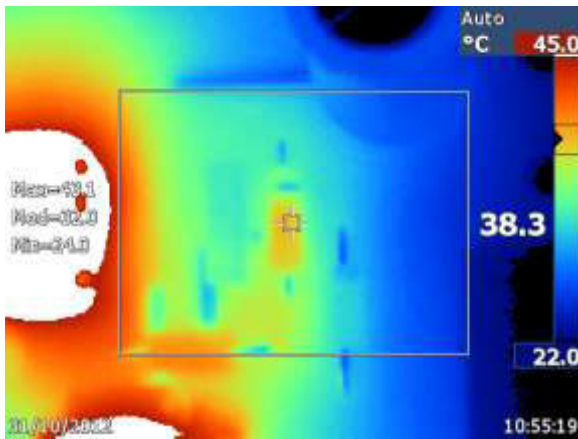


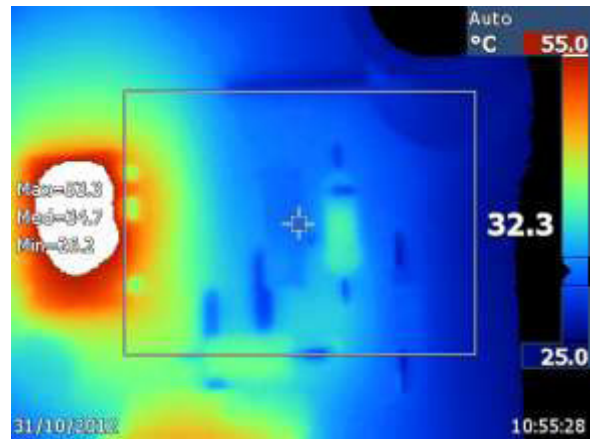Figure 8.36: 2DD103 temperature.

Figure 8.37: 2RP101 temperature.



Figure 8.38: 2CP101 temperature.
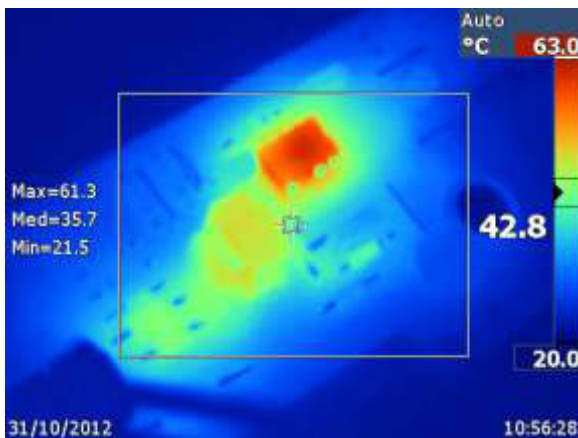


Figure 8.39: overall temperature in the board.

## 8.3. Analysis of the results

By electrical analysis of the behaviour, it has been verified that the power consumption in off mode of the washing machine is composed by the consumption of its parts and the total value is 0.3 W.

In particular the power consumed by the SMPS is 70 mW due the leakage current of the LNK363. The other power consumption is caused by EMI input filter used in the input stage of the washing machine and the sensing resistor.

The power consumption measured in stand-by is 828 mW that is lower of 1 W (see the regulation on energy saving), while using the proposed circuit for turning off the SMPS, the power consumption is reduced below 0.5 W.

# Chapter 9

Series Connection of Power Switches in High Input Voltage with Wide Range Power Supply for Gate Driving Application

## 9. Introduction

One of the main problems besetting the power supply designers today is to design a switching power supply that is able to operate in the power systems within their international marketplaces according to the available voltage supply in the specific setup. When the DC input voltage to a buck converter has a wide range, it becomes important to select a suitable switching regulator integrated circuit (IC) for the application, and to select the power components able to handle the worst-case input voltage. For a given component, the worst-case may be the maximum input voltage or the minimum input voltage, but in fact may also be somewhere in between. The study which will be described in this chapter concerns the development of a high voltage buck converter for gate drive applications [25]-[27]. Usually, these converters are used to feed the gate driving unit (GU) of IGBTs or IGCTs. In particular this study will focus on IGCTs gate driver which needs a greater power then an IGBT gate driver because of the higher current necessary to operate the switching of the device. The IGBT or IGCT are used in HVDC or FACTS applications and the gate drive unit takes energy from the high DC voltage input.

In the field of high voltage power conversion and low current, series connected MOSFETs have reached a wide diffusion mostly due to the fact that other types of high voltage devices often do not match the designer needs in terms of the switching frequency. Therefore in applications requiring a high switching frequency such as high voltage power supplies for color television, medical equipments or railway motor drives, a series connection of MOSFETs is the most advantageous solution and may sometimes be considered the only viable [28] [29]. In fact by connecting MOSFETs in series allows obtaining the equivalent of a fast high voltage switch but with only a fraction of the voltage applied to each single device. In spite of this, however some additional problems arise since small differences in the switching times of the series connected devices may cause an unequal voltage sharing during the commutations. This is a problem since voltage imbalances may lead some devices to exceed their maximum forward blocking voltage causing failures. Since voltage imbalances cannot be avoided, since depend on the usual parameter spread of MOSFETs, in order to avoid any device failure a reliable voltage balancing strategy is required, during switching transients and also in steady state [30].

A power supply for power devices driver has been studied and designed. A series connection of power devices, with an insulated power stage, allows high voltage switching

and operation at high frequency in order to obtain a low voltage ripple in the regulated output. A design procedure for a converter providing the power needed by four driving circuits is detailed to follows. In particular, the analysis focuses on both the insulation issues and the control. Finally, the experimental results on a full scale prototype are discussed.

## 9.1. The Buck Converter Design

The main purpose of the analysis in this chapter is the design of the first power stage, not isolated DC/DC converter shown in Figure 9.1. The gate drive units are fed by the DC voltage and so the energy is taken from a high voltage DC link that in this case may have a voltage up to 3000 V. The DC supply is composed of two stages. The input voltage is first stepped down by a not isolated DC/DC converter from the DC link high voltage to a regulated 300 V DC. Two independent DC/DC converters are used in parallel, for redundancy. This voltage is then fed to insulated DC/DC converters which feed the gate drive units with the required 24 V DC.

The first not isolated stage represents the most critical part of the design for the isolation implications and the necessity to deal with wide input voltage range operation. The topology used is a buck converter. In this one, the reference of the gate drive signal of the power MOSFET is floating. Therefore, the gate drive circuit needs isolation from the ground of the system, which is obtained by means of suitable optocouplers. The use of these electronic devices allows transmitting signals keeping a galvanic isolation between the two parts of the circuit. The main schematic of the circuit used for IGCTs GUs supply is depicted in **Errore. L'origine riferimento non è stata trovata.**. In particular, a function generator is used to drive the power MOSFETs, $V_{\text{pulse}}$. In the following sub-sections a description of the specifications and the design of the several parts composing the DC-DC converter are carried out in detail.
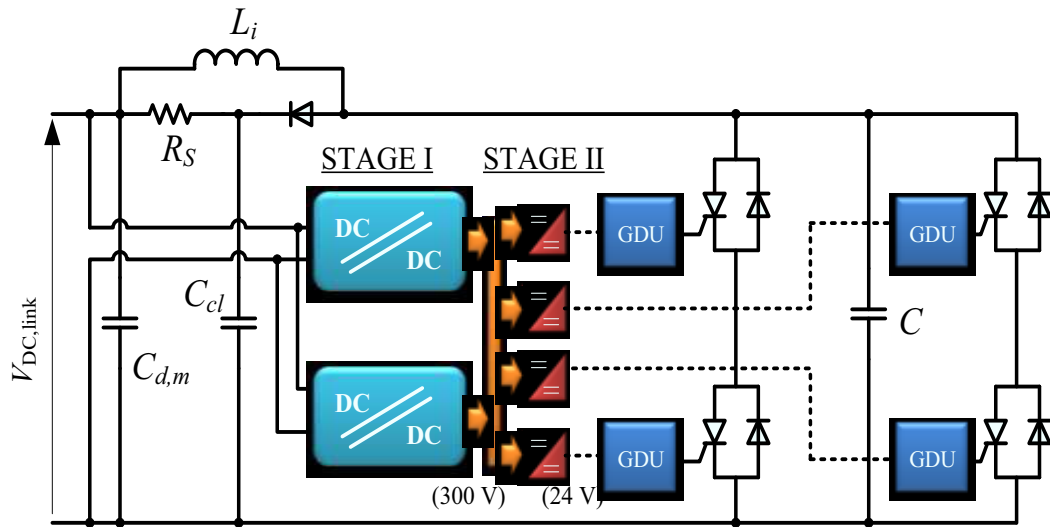
Figure 9.1: Overall solution for providing gate drive power from the DC link, composed by a not isolated first stage and isolated second stage switching converter.

### 9.1.1. Main circuit requirements for IGCT GU supply

The power supply for the IGCTs gate driver (STAGE I) is fed from the DC link which has an input voltage varying within a wide interval. The main design quantities for the converter are given in Table 9.1.

Table 9.1: Main design quantities for the converter.

| Input voltage | 400 – 3000 V |
|---|---|
| Output voltage | 300 V |
| Output rated power | 100 W |
| Output voltage ripple (%) | 20% (output voltage) |
| Switching frequency | 30 kHz |
| Efficiency (@ 2.4 kV$_{DC}$) | ≈80% |

### 9.1.2. Design of power switches and passive components

The first step on the converter design is the choice of the switches. The maximum input voltage, as previously shown, is 3000 V$_{DC}$, so that three MOSFETs should support the high voltage and the breakdown voltage of each power MOSFET has to be at least 1000 V. In order to guarantee the safe operation of the system, the device of choice has been power MOSFET of the series SuperMESH3, that have a 1200 V breakdown voltage and 3 A rated current. The mentioned rating has been chosen in order to minimize the on state losses.

In a buck converter, when the switch is in on state, the total DC input voltage is applied across the cathode and anode of the diode and, as previously shown, the maximum voltage in this application is 3000 V. In order to guarantee a safe switching, three diodes in series connection have been used and each diode can withstand a maximum voltage of 1000 V. In order to avoid voltage imbalance, capacitors in parallel connection with the diodes are used. The main features of the used diodes are $V_{RRM}$ = 1200 V and $I_F$ = 1 A.
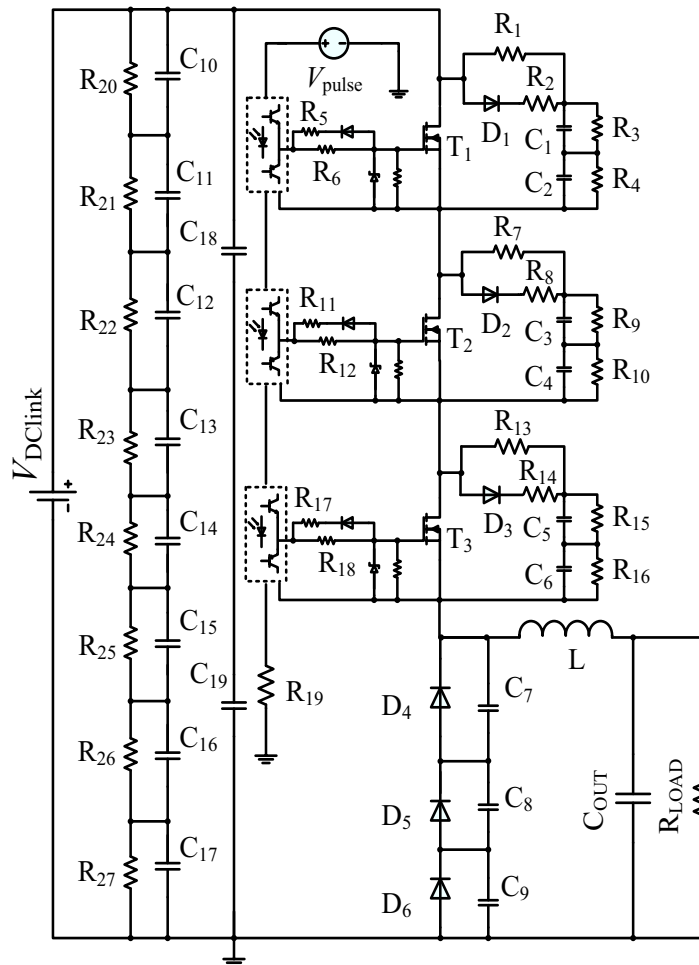


Figure 9.2: Schematic of the low power solution adopted for IGCT driver supply as not isolated first stage switching converter.

The converter has been designed to operate in continuous current mode (CCM). In order to guarantee the converter to work in CCM in all the possible input voltage states there has been the need to evaluate the minimum duty cycle value. According to the buck converter equations [10]:

$$\delta_{min} = \frac{V_{out}}{V_{in,max}} \Rightarrow t_{on,min} = \delta_{min} T_s \qquad \text{Eq. 9.1}$$

In equation Eq. 9.1 the input voltage Vin = VDClink; Ts = 1/fs, where fs is the switching frequency and $t_{on,min}$ is the minimum conduction time value of the power MOSFETs, that is equal to 3µs. The equation Eq. 9.2 provides the values needed to design the minimum inductor value, $L_{min}$ that allows the continuous mode.

$$L > L_{min} = \frac{V_{in,max} - V_{out}}{I_{peak}} t_{on,min} \cong 10mH \qquad \text{Eq. 9.2}$$

where $I_{peak}$ is the peak value of the inductor current when the duty cycle is minimum, $\delta_{min}$; $I_{in,rms}$ is the *rms* input current. In the buck converter, the minimum inductor value that guarantees the continuous current mode operation is 10mH, and the value taken into account in the design is 15mH. With reference to the output stage, the output capacitor value depends on the design constraints on the voltage ripple, and this value is fixed at 20%.

From the characteristic equations of the buck converter is then possible to calculate the value of the capacitor to be considered to obtain the desired voltage ripple. The main values to take into account are then the capacitance and the parasitic Equivalent Series Resistance (ESR),[10] [11].

$$C_{out} = C'_{out} + C''_{out}$$

$$C'_{out} = \frac{65 \cdot 10^{-6}}{ESR} \qquad C''_{out} = \frac{T_s^2}{8L} \frac{V_0}{\Delta V_0} (1 - \delta) \qquad \text{Eq. 9.3}$$

Where $C'_{out}$ is the output capacitance contribute due to the ESR and $C''_{out}$ is the one to consider in order minimizing the output voltage ripple $\Delta V_0$.

### 9.1.3. Series connection

As described in the previous sections, the input voltage may change in the range between 400 V to 3000 V, so that more power devices connected in series are needed. In order to do not have failures in the system all of these devices must behave like one device thus being triggered at the same time with an optimized synchronization between their driving stages. Therefore, every power MOSFET used as switch must have the same dynamic characteristics in order to avoid issues of imbalance [31]. Since, as known, possible parameters spread among power devices is unavoidable, the series connection driving has to be realized as effective through the use of proper snubber circuits [32], or rather a passive network that guarantees the correct balance of the bus voltage on every device when this ones are on off state (static balance) and during the switching (dynamic balance). If the voltage is not equal on every switch failures may happen. The problem may arise from the following issues:

- spread on the leakage current;

- different delay time among the gate signals;

- different input impedance.

Thus, if the system operates in a correct way, the same dv/dt on the series connected devices will appear, and such a condition may be ensured by an appropriate design of the snubber circuit [33]. The circuit used on every device is a RCD one, as shown in Figure 9.3. Two paths, having different resistance, are used to control the dynamic voltage during the turn-on time and the turn-off time. A diode is used to separate the two paths of charge and discharge of the capacitors, but can be omitted in some cases.

When the power device is in off state the diode $D_1$ is in forward state and (neglecting the two resistors $R_3$ and $R_4$) the series connection of the capacitors $C_1$ and $C_2$ is charged with a time constant $\tau_1$.

$$\tau_1 = R_1 \mathbin{/\mkern-5mu/} R_2 \cdot \left(C_{OSS} + C_{SN}\right) \qquad \text{Eq. 9.4}$$

where $C_{OSS}$ is the intrinsic equivalent output capacitance of the MOSFET device and $C_{SN}$ is the equivalent capacitor given by the series of $C_1$ and $C_2$. The resistors $R_3$ and $R_4$ are balancing ones and they have high value (about 3 M$\Omega$). Their main function is to

allow the static voltage balance on the device. When the device is in on state, the diode is reverse biased and the capacitor will discharge with a constant time $\tau_2$.

$$\tau_2 = R_1 \cdot (C_{OSS} + C_{SN})$$
Eq. 9.5

The value of the equivalent capacitor $C_{SN}$ was designed greater than $C_{OSS}$. In particular, the value taken into account is the equivalent $C_{OSS}$ capacitance. This latter is defined as a constant equivalent capacitance giving the same charging time as $C_{OSS}$ when $V_{DS}$ increases from 0 to 80% of $V_{DSS}$. The value shown in the datasheet is 40 pF ($V_{GS} = 0$, $V_{DS}$=0 to 960 V).
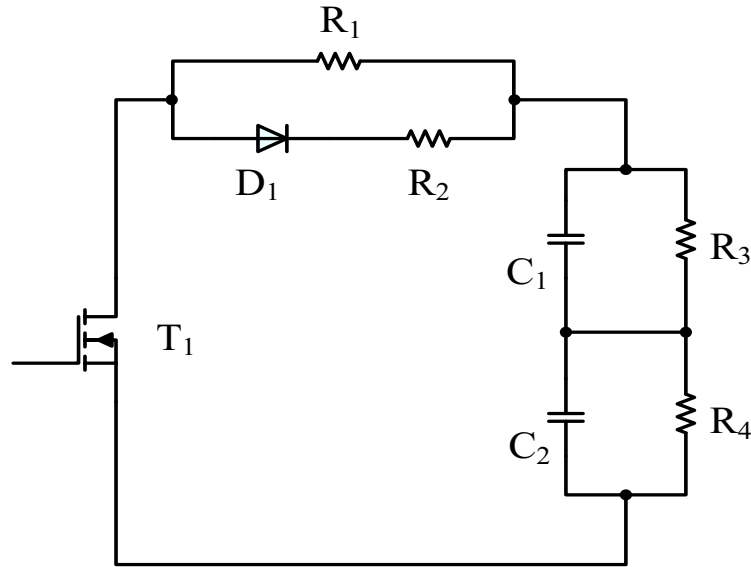


Figure 9.3: Snubber RCD circuit used for each power switch in the series connection.

If the value of $C_{SN}$ is too big, the turn off switching is very slow. In order to have a good switching the time to charge and discharge the capacitor has to be less then $t_{on}$ and $t_{off}$. The design of this circuit was done considering the extreme case when the input voltage is 3000 V and the duty cycle is the minimum, as shown by Eq. 9.6. This condition provides the minimum $t_{on}$ that allows fixing the constant time of the capacitor's discharge. The value of the time constant $\tau_2$ is calculated according to the following expressions:

$$T_{disch} < t_{on,\min}$$
Eq. 9.6

According to Eq. 9.6 , it is possible to obtain the discharge time constant value $T_{\text{disch}}<$ 3µs and because the discharge time is about 4 – 5 times the time constant $\tau_2$, this is fixed as follows:

$$\tau_2 = \frac{T_{disch}}{5}$$

<div align="right">Eq. 9.7</div>

The value of the capacitor ($C_{\text{SN}}$) is fixed at 410pF by means of two capacitors in series connection ($C_1$ and $C_2$) having 820pF, while $R_1$ value is 5kΩ.

The time constant $\tau_2$ sets the discharge time of the capacitor during on time, while during turn off state the slope is fixed by the time constant $\tau_1$. Choosing $R_1 \gg R_2$ and $C_{\text{SN}} \gg C_{\text{OSS}}$, the constant time relation can be simplified as follows:

$$\tau_1 \cong R_2 C_{SN}$$

<div align="right">Eq. 9.8</div>

Experimental measurements have shown that a good matching between voltage imbalance and turn off time (of the voltage $V_{\text{DS}}$ of each device) is obtained by fixing the time constant $\tau_1$=7ns, so the value of resistor $R_2$ is 45Ω.

In order to evaluate the power losses in the snubber circuit, the energy stored in the snubber capacitor is considered. During the turn off and turn on switching, the energy of the capacitor ($E_{C_{SN}}$) is dissipated by the resistors $R_1$ and $R_2$. The power losses in the resistors, $P_{\text{loss,R1}}$ and $P_{\text{loss,R2}}$ are given by the following relations, where $I_{\text{ch,rms}}$ and $I_{\text{disch,rms}}$ are respectively the *rms* current of charge and discharge of the equivalent capacitor $C_{\text{SN}}$, and V is the voltage drop on it.

$$P_{loss,R_1} = R_1 I^2_{ch,rms} = \frac{1}{2} C_{SN} V^2 f_s$$
$$P_{loss,R_2} = R_2 I^2_{disch,rms} = \frac{1}{2} C_{SN} V^2 f_s$$
$$E_{C_{SN}} = \frac{1}{2} C_{SN} V^2$$

<div align="right">Eq. 9.9</div>

In this way the power losses in the snubber circuit, $P_{\text{loss,tot}}$, are obtained by the product between the switching frequency $f_s$ and the double of the energy stored in the equivalent capacitor $C_{\text{SN}}$.

$$P_{loss,tot} = P_{loss,R_1} + P_{loss,R_2} = f_s C_{SN} V^2$$

<div align="right">Eq. 9.10</div>

As shown by equation Eq. 9.10, the losses increase with the square of the voltage drop on the capacitor, being constant the switching frequency and the snubber capacitor. In Figure 9.4 the power losses in each snubber circuit and the total power losses at different input voltages are shown.
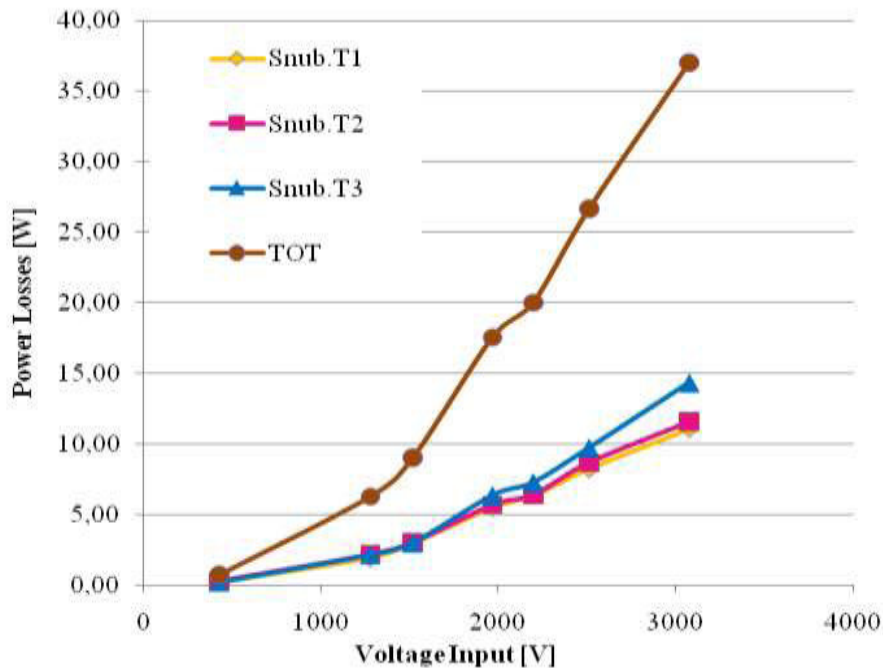


Figure 9.4: Power losses of the snubber circuits vs. voltage input.

## 9.2. Experimental validation

Experimental tests have been done in different conditions of input voltage (from 400 V to 3000 V) and constant output power of 100 W.  The outline of the experimental evaluated scenarios is the following:

1.      Evaluation of synchronous operation among the series connected switches;

2.      System efficiency and device temperature.

The performance of the system has been evaluated for different values of the input voltage.  The evaluation is focused on the power losses during the switching transients, during the conduction and on the snubber circuit.  In particular $R_{DS,on}$ has, for power MOSFETs, a positive thermal coefficient as shown in Figure 9.5.  The effects on the system temperature and the efficiency have consequently been evaluated.
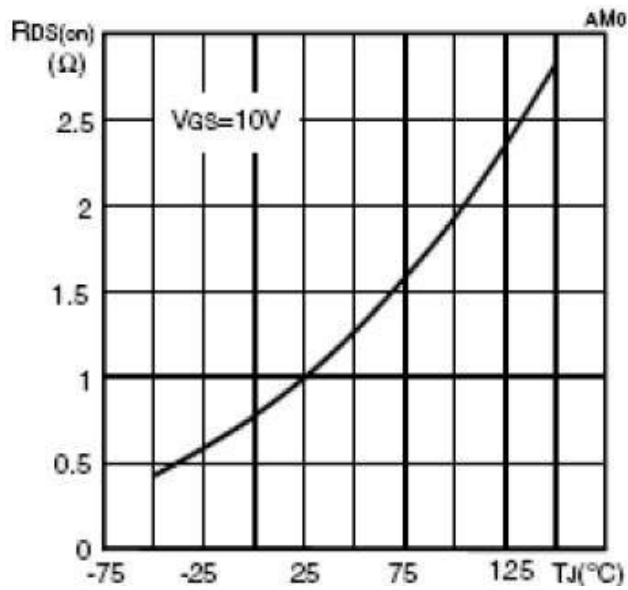
Figure 9.5: Normalized $R_{DS,on}$ value @25°C vs. temperature (from device datasheet).

The selection of the components is important in order to fulfill the system requirements. The spread of the parameters in the device may cause a different start time at turn on and turn off, and causes a voltage imbalance between the devices. Other important feature is the isolation between the input and output obtained by means of the optocouplers, which will guarantee isolation up to 3000 V.
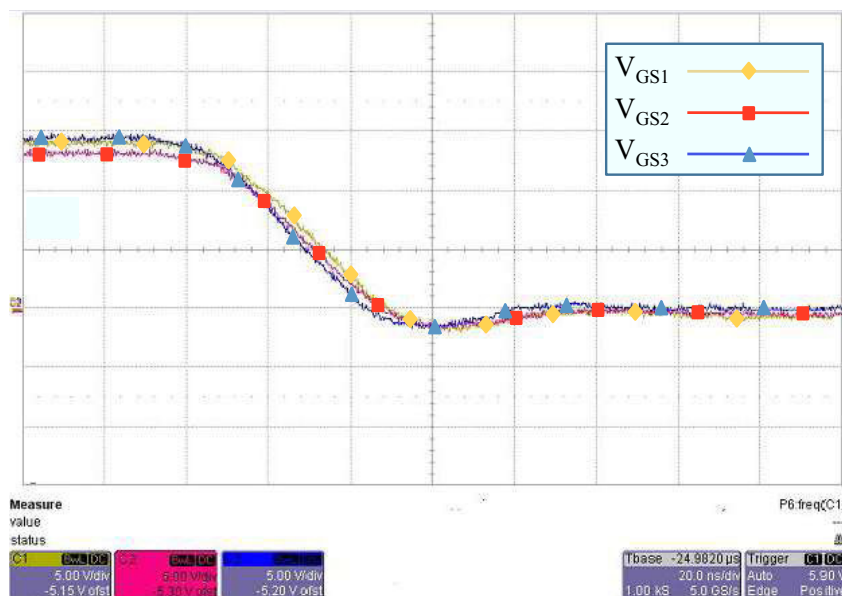


Figure 9.6: Gate voltages during turn off switching; $V_{GS1}$, $V_{GS2}$, $V_{GS3}$ 5 V/div; time 20 ns/div.

In Figure 9.6 and Figure 9.7 the waveforms of the gate signal in the three devices are shown, during the turn off and turn on switching transients. In particular, in Figure 9.6, it is possible to see the turn off sequence of the devices, T3, T2 and T1 respectively. This

one causes a greater voltage drop on the device T3 and lower in T1 and T2, (see Figure 9.8).
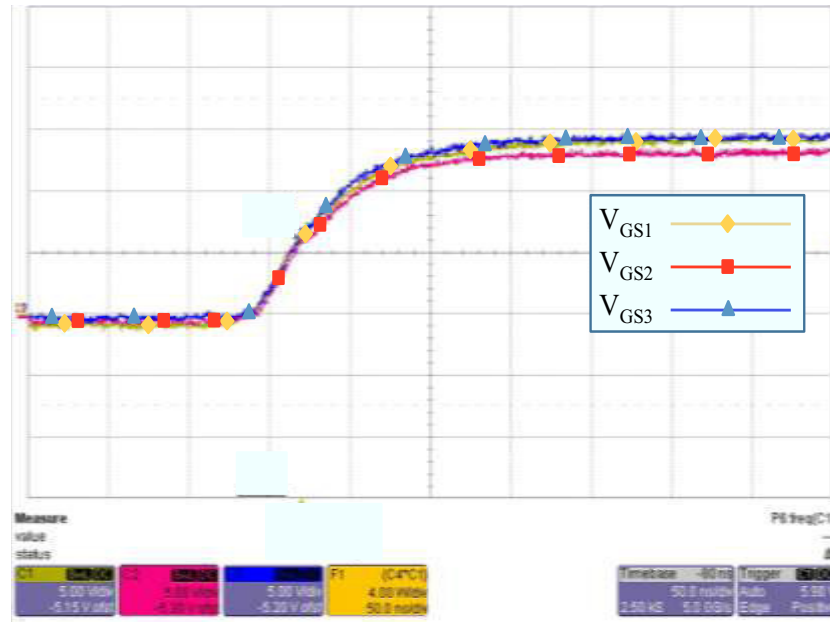


Figure 9.7: Gate voltages during turn on switching; $V_{GS1}$, $V_{GS2}$, $V_{GS3}$ 5 V/div; time 50 ns/div.

In Figure 9.7, instead, the turn on sequence of the device, is T3, T1 and T2 respectively. The unbalances are due to the parameters spread of the optocouplers and of the passive components.
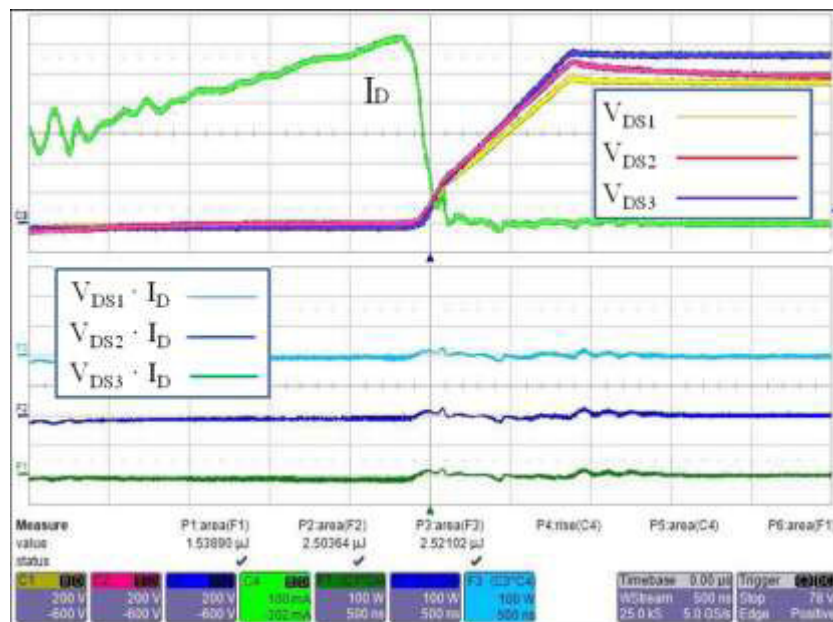


Figure 9.8: Turn off switching; $V_{DS1}$, $V_{DS2}$, $V_{DS3}$ 200 V/div, $I_D$ 100 mA/div; $P_1$ ($V_{DS1} \cdot I_D$), $P_2$ ($V_{DS2} \cdot I_D$), $P_3$ ($V_{DS3} \cdot I_D$) 100W/div; time 500 ns/div.
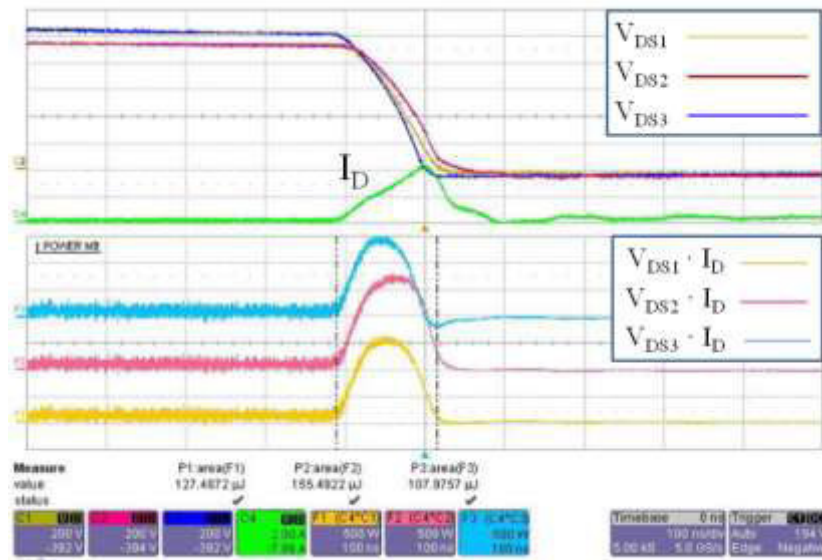
Figure 9.9: Turn on switching; $V_{DS1}$, $V_{DS2}$, $V_{DS3}$ 200 V/div, $I_D$ 2 A/div; $P_1$ ($V_{DS1} \cdot I_D$), $P_2$ ($V_{DS2} \cdot I_D$), $P_3$ ($V_{DS3} \cdot I_D$) 500W/div; time 100ns/div.

In Figure 9.8 and Figure 9.9 the switching transients and the power losses for the three devices are shown at $V_{in}$=3000 V. Higher losses at turn on than at turn off are clearly shown. This is caused by the snubber circuit because during the turn off, the $V_{DS}$ slope is reduced on each device and the cross between voltage and current is lower.

In a similar way in Figure 9.10 and Figure 9.11, the switching transient and the power losses are shown at $V_{in}$ =400 V. In this case the power losses in the devices are lower than in the first case, because the cross between voltage and current is lower. Thus by reducing the voltage drop on the devices the power losses get reduced.
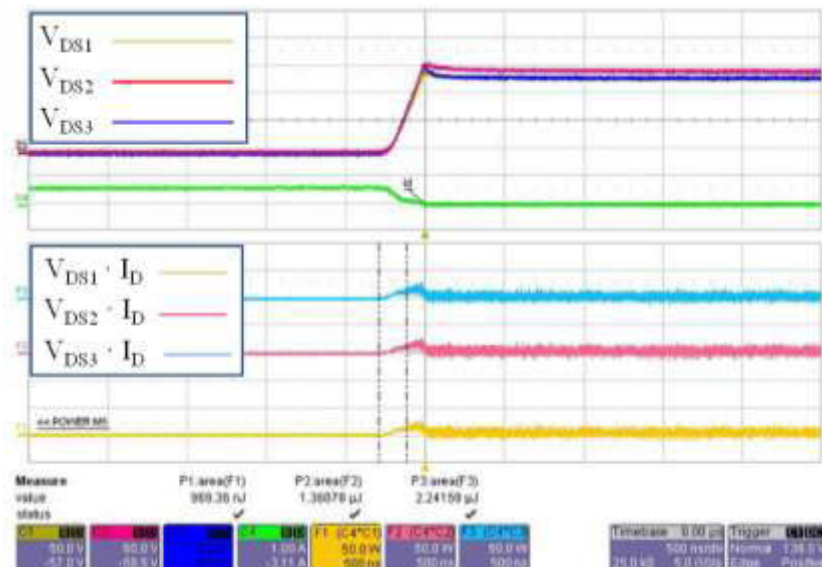


Figure 9.10: Turn off switching; $V_{DS1}$, $V_{DS2}$, $V_{DS3}$ 50 V/div, $I_D$ 1 A/div; $P_1$ ($V_{DS1} \cdot I_D$), $P_2$ ($V_{DS2} \cdot I_D$), $P_3$ ($V_{DS3} \cdot I_D$) 50 W/div; time 500 ns/div.
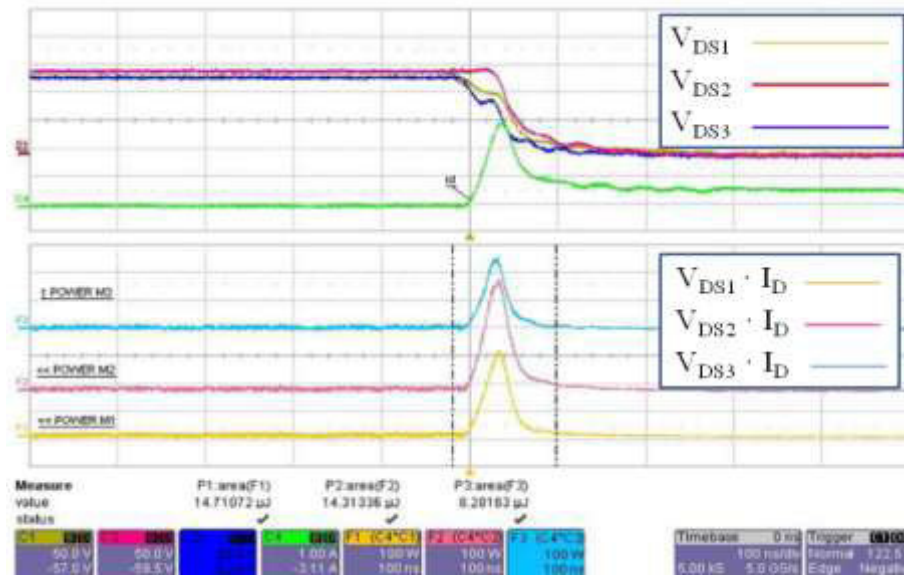
Figure 9.11: Turn on switching; $V_{DS1}$, $V_{DS2}$, $V_{DS3}$ 50 V/div, $I_D$ 1 A/div; $P_1$ ($V_{DS1} \cdot I_D$), $P_2$ ($V_{DS2} \cdot I_D$), $P_3$ ($V_{DS3} \cdot I_D$) 100 W/div; time 200 ns/div.

In Table 9.2 a summary of the main results coming from the experimental tests at different input voltages are shown.

In Figure 9.12 and Figure 9.13 the evaluation of the distribution of the temperatures among devices is shown in an infrared camera capture for two different cases of input voltage (Vin=400 V and Vin=3000 V). In agreement with Table 9.2 the devices temperature is higher on the device with greater losses than device with lower losses.

In Figure 9.14 and Figure 9.15 the temperatures and the power losses on the devices are shown at different input voltage, and in Figure 9.16 and Figure 9.17 are shown respectively the voltage drop on each devices and the relative voltage unbalance (ΔV%) at different input voltage. This latter has been evaluated in the following way:

$$\Delta V\% = \frac{\left|V_N - V_{avg}\right|}{V_{avg}} 100$$

Eq. 9.11

Where $V_N$ is the voltage drop on the N device (N = 1, 2 or 3), and $V_{avg}$ is $V_{in}/3$.

Table 9.2: Summary of the power losses in the three series connected switches.

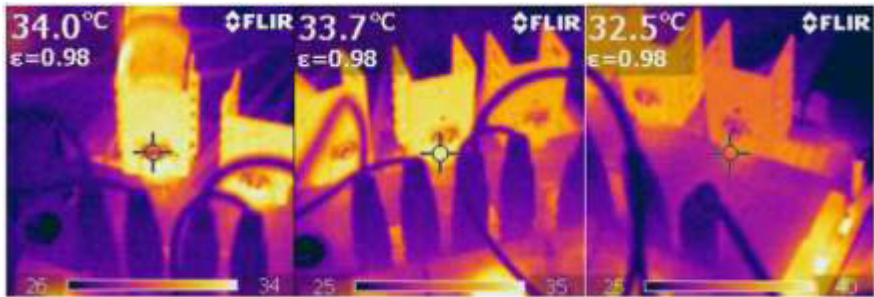| $V_{IN}$ [V] | Device | $P_{ON}$ [W] | $P_{OFF}$ [$10^{-3}$W] | $P_{COND}$ [$10^{-3}$ W] | $P_{TOT}$ [W] |
|---|---|---|---|---|---|
| 400 | $T_1/T_2/T_3$ | 0.44/0.43/0.25 | 29/40/67 | 146/146/146 | 0.61/0.61/0.46 |
| 1200 | $T_1/T_2/T_3$ | 0.74/0.98/0.38 | 19/18/26 | 20/20/20 | 0.77/0.99/0.42 |
| 1500 | $T_1/T_2/T_3$ | 0.73/0.98/0.38 | 19/18/26 | 20/20/20 | 1.12/1.51/0.68 |
| 2000 | $T_1/T_2/T_3$ | 1.82/2.25/1.18 | 78/62/117 | 8/8/8 | 1.91/2.32/1.31 |
| 2500 | $T_1/T_2/T_3$ | 2.67/3.35/1.89 | 48/71/59 | 6/7/6 | 2.62/3.40/1.94 |
| 3000 | $T_1/T_2/T_3$ | 3.82/4.66/3.24 | 114/32/40 | 6/7/4 | 3.90/4.70/3.28 |

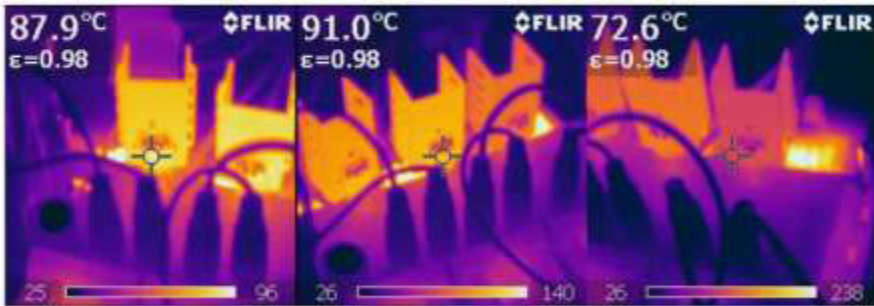Figure 9.12: Thermal image by T1, T2 and T3 with $V_{in}$=400V.



Figure 9.13: Thermal image by T1, T2 and T3 with $V_{in}$=3000V.
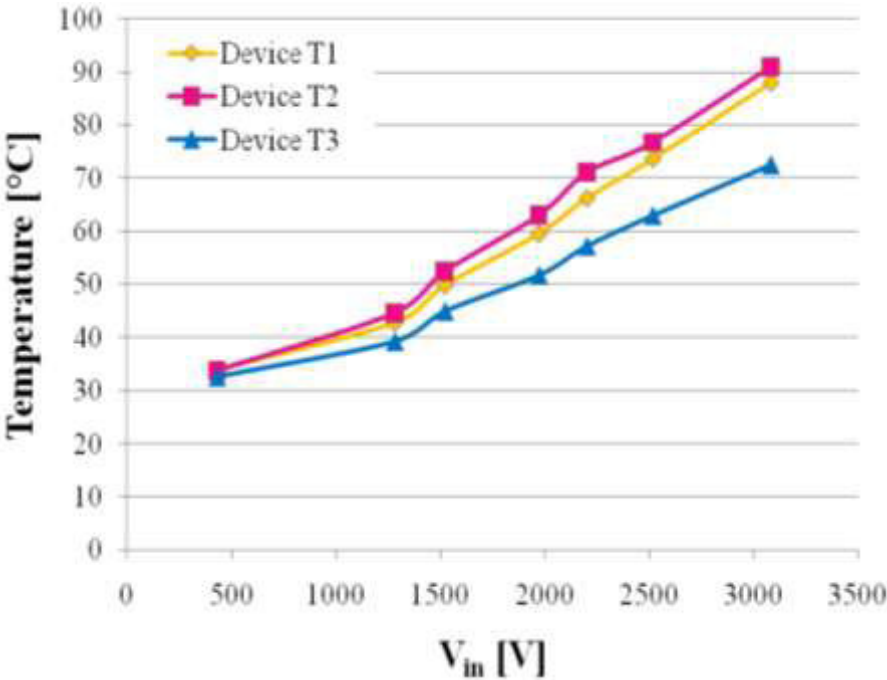


Figure 9.14: Temperature on the devices (T1, T2, T3) vs. input voltage ($V_{in}$).
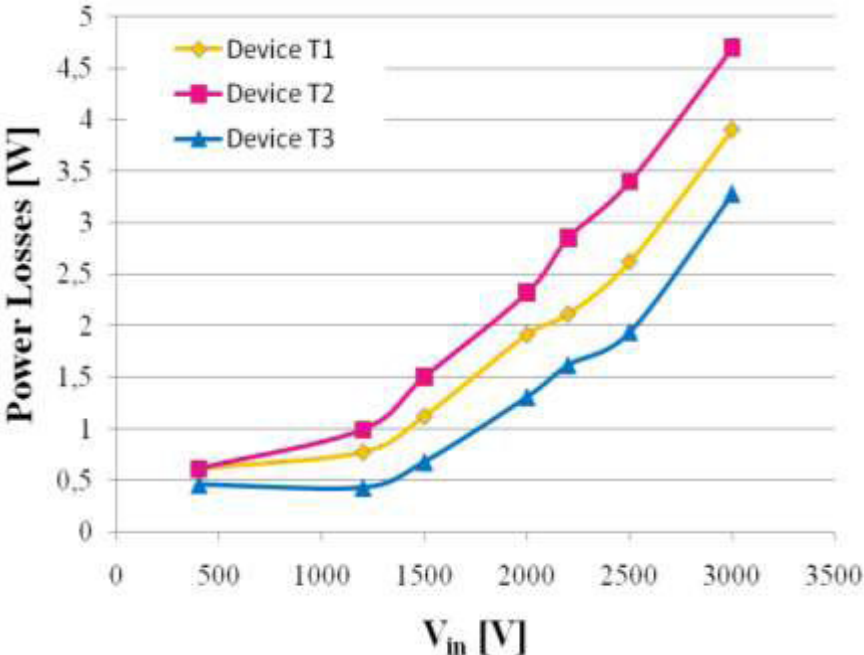
Figure 9.15: Power losses on the devices (T1, T2, T3) vs. input voltage ($V_{in}$).
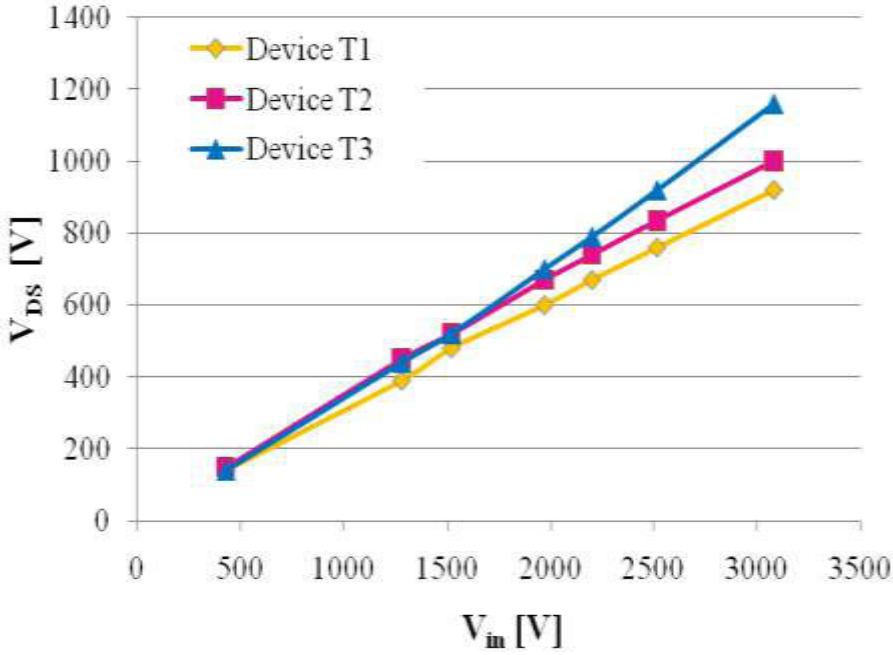


Figure 9.16: Drain- source voltage vs. input voltage.
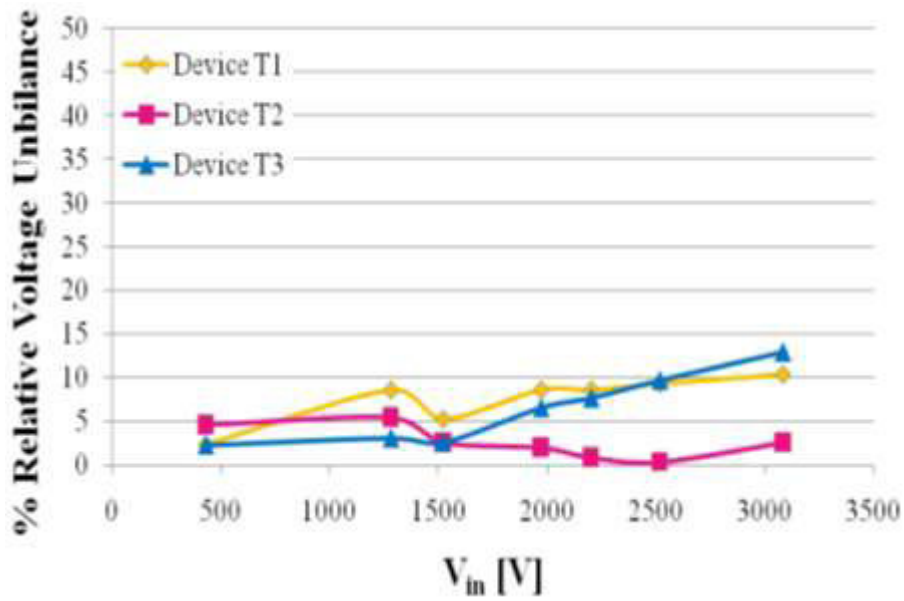
Figure 9.17: Percentage relative voltage imbalance vs. input voltage.

After the measurements of the switching and the conduction losses on all three devices, and the evaluation of the power losses on the snubber circuits, the efficiency was estimated. **Errore. L'origine riferimento non è stata trovata.** shows as the efficiency changes at different input voltage.
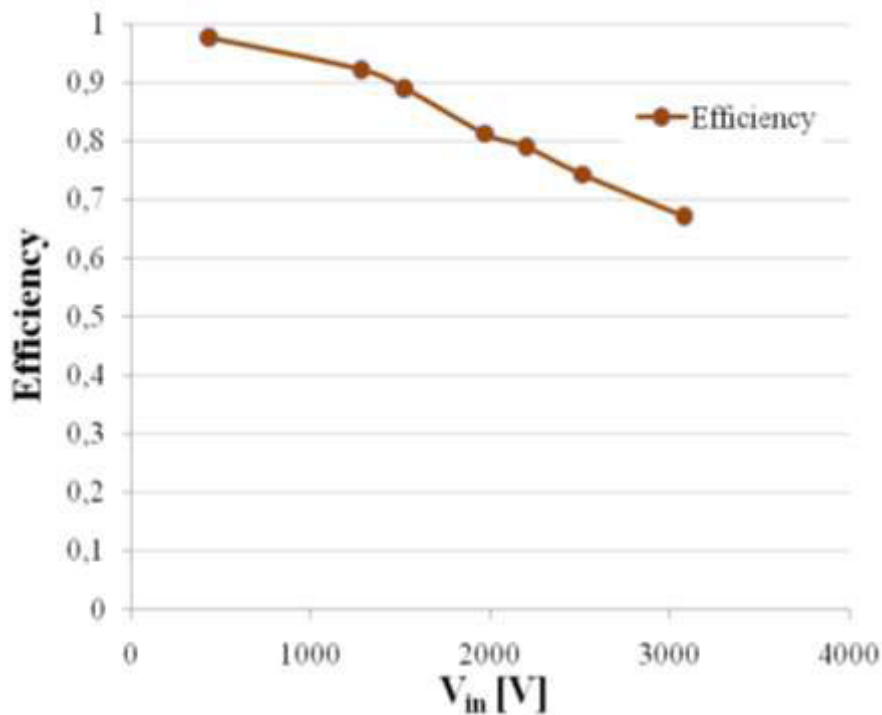


Figure 9.18: Efficiency (output power /input power) vs. input voltage.

The efficiency of the system goes under 80% up to 2200 V because the power losses on the snubber increase with the square of the input voltage.

The system without snubber has been tested and the voltages drop, $V_{DS}$, for each device is shown from Figure 9.19 to Figure 9.21 and compared with the voltage drop with snubber circuit.
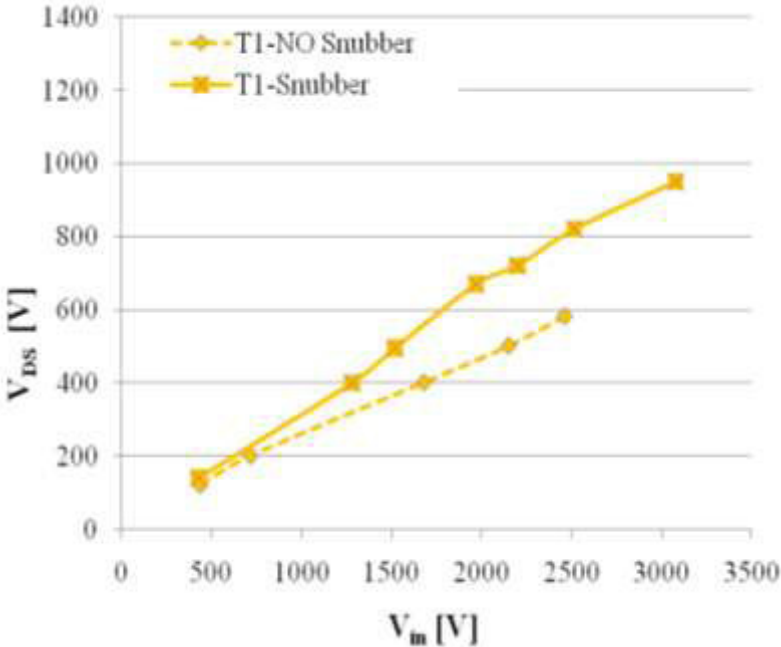


Figure 9.19: Drain- source voltage (T1) vs. input voltage.
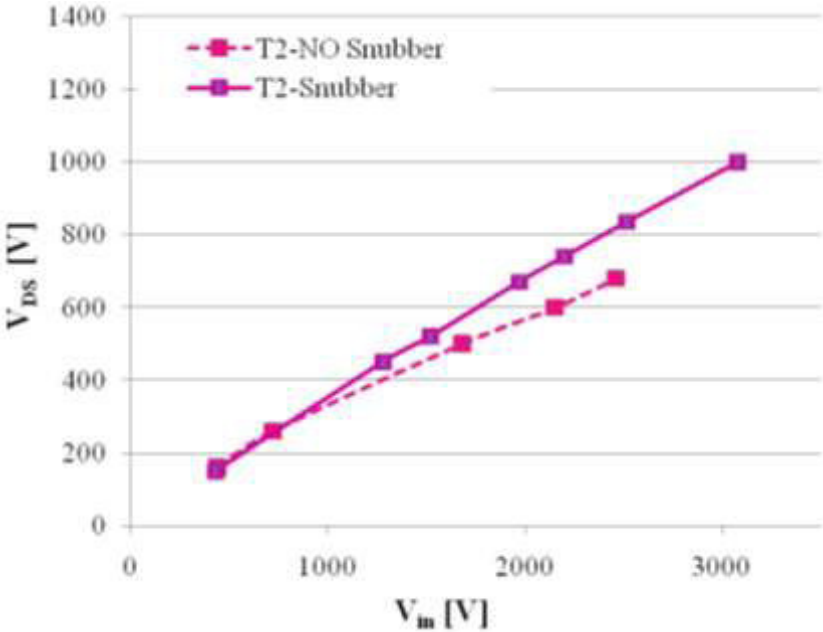


Figure 9.20: Drain- source voltage (T2) vs. input voltage.
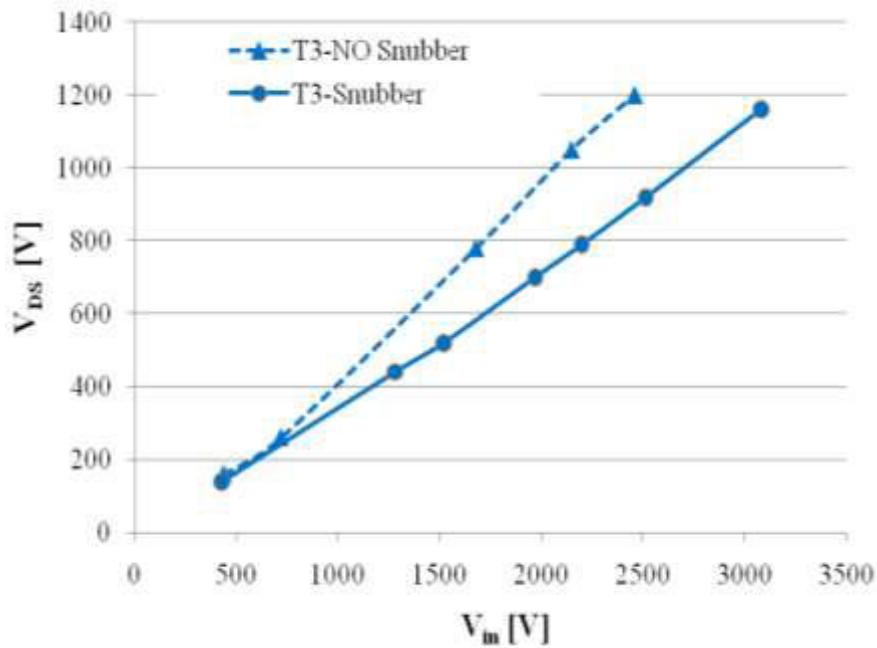
Figure 9.21: Drain- source voltage (T3) vs. input voltage.
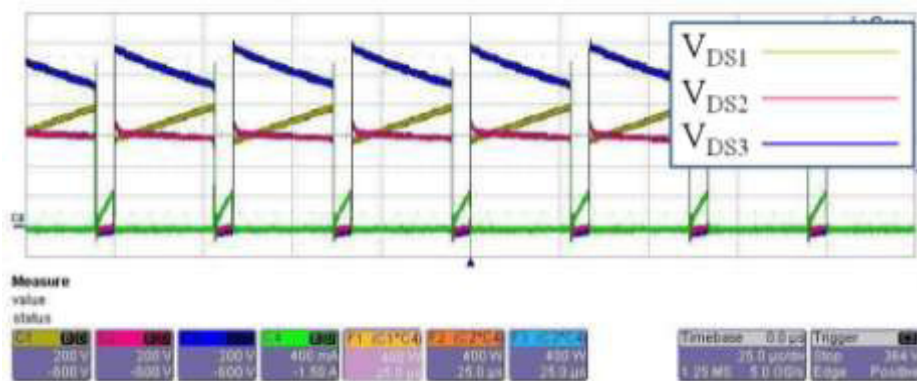


Figure 9.22: Switching overall without snubber circuit; $V_{DS1}$, $V_{DS2}$, $V_{DS3}$ 200 V/div, $I_D$ 500 mA/div; time 25 µs/div.

In Figure 9.22 the drain–source voltage on each power MOSFET of the series and the drain current, $I_D$ are shown. The maximum input voltage reached without snubber circuit is 2460V, because the voltage drop on the device T3 reaches a value near the $V_{DSS}$.

In Figure 9.23 the relative voltage imbalance on the power MOSFETs in the series connection is shown. In order to test the strength of the snubber circuit, simulations were done considering a modification of the delay time of gate-source driving signal of the power MOSFET at 3000V input voltage. In particular the gate source signal of T2 and T3 was delayed form 50ns to 1µs, the voltage on each device was taken into account and the relative imbalance was evaluated, as shown in Figure 9.24 and Table 9.3.
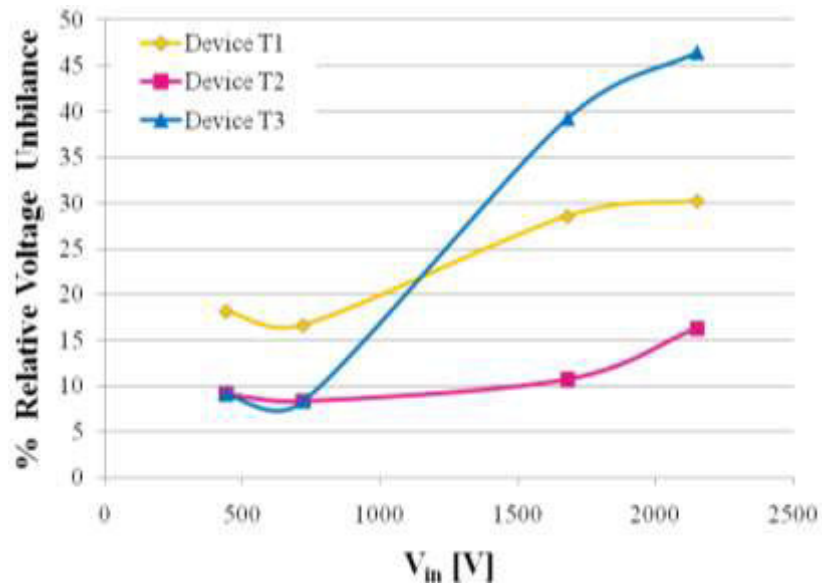
Figure 9.23: Percentage relative voltage imbalance without snubber circuit vs. input voltage.

By this comparison it can be observed that the snubber circuit allows a safer operation especially at higher input voltage levels making it possible to have a lower relative voltage imbalance than in the case when it is not used (see Figure 9.17 and Figure 9.23).
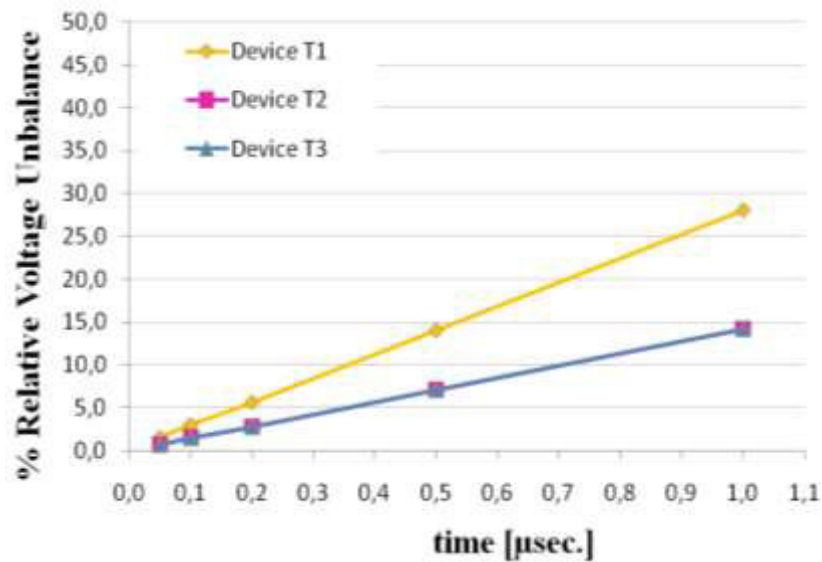


Figure 9.24: Percentage relative voltage vs. delay gate – emitter voltage.

Table 9.3: Simulation at 3 kV of $V_{in}$ and T2, T3 delayed.

| Delay [µs] | T1 [V] | T2 [V] | T3 [V] | $\Delta V_{T1}\%$ | $\Delta V_{T2}\%$ | $\Delta V_{T3}\%$ |
|---|---|---|---|---|---|---|
| 1 | 1280 | 858 | 858 | 28.0 | 14.2 | 14.2 |
| 0,5 | 1140 | 929 | 929 | 14.0 | 7.1 | 7.1 |
| 0,2 | 1056 | 972 | 972 | 5.6 | 2.8 | 2.8 |
| 0,1 | 1030 | 985 | 985 | 3.0 | 1.5 | 1.5 |
| 0,05 | 1015 | 993 | 993 | 1.5 | 0.7 | 0.7 |

## 9.3. Discussion

IGCTs can be considered as the device of choice in several power systems applications. In these applications the gate units used to drive IGCTs need a power supply that takes energy from the high voltage line. The wide input voltage range due to the operation of the power circuit makes the need to design a system that is able to provide a stable output voltage (usually 24 V) with a high input voltage range.

The system described in this chapter is realized by the cascade of a first not isolated stage that provides 300 V output with an input voltage in the range between 300 V and 3000 V. The chosen topology has been a buck converter. MOSFET devices in series connection have been used in order to obtain a better $R_{DS,on}$ than a single device and a breakdown voltage up to 3000 V. In general, the series connection is able to work at higher frequency than a single device with same breakdown voltage and nominal current.

In order to avoid voltage imbalance a suitable snubber circuit has been used in parallel connection with the devices and optocouplers have been used to drive the gate of each device and to ensure galvanic isolation between power side and the driver (signal side). Design procedures and experimental results have been shown and the efficiency of the realized prototype has been evaluated.

# Chapter 10

## Conclusions

The research carried out was aimed to determine both techniques and circuits that allow to obtain energy savings, while are maintaining the performances and functionalities of systems, components, and appliances.

A well known and widely used power converter, the flyback, has been investigate in several applications. By means of a sensitivity analysis has been clarified how the electrical parameters of the power converter act into the power quality of the main line-Improvements on the performances have been obtained by using a new input stage topology. In particular, when a $\pi$ filter is used in the input of the converter, it was noted that by reducing the value of the buffer capacity an increase of the ripple of output voltage appears. This implies an increased peak of the current through the primary of the transformer and the power switch. The advantage is a higher power factor. In order to improve the PF and THD values, a valley PFC circuit may be the choice , but the output voltage ripple increases till 15% of the nominal voltage (30V). The analogue dimming is the simplest one to control the brightness of the LED lamp. Although it has disadvantages, because high injection currents may lead to a lack of linearity between injected current and luminous flux output, and a noticeable shift in chromaticity coordinates, which are considered the most important drawback of this technique. Alternatively, PWM techniques may be used and in particular the PWM series dimming. This technique maintains all the advantage and not has the disadvantage of the previous technique. The case study was a LED lamp having the luminous flux equivalent to a 60 W incandescent lamp.

From a different field of applications, in case of appliances the reduction of the power consumption of the converter in non operation mode of an appliance has been faced. The model of the circuital technique proposed in order to reduce the power consumption, in particular for a washing machine, has been realized. The operation of the circuit allows to control the state of SMPS both from a mechanical switch and from a microcontroller inside to the user interface circuit.

When the microcontroller detect the inactivity state of the washing machine, after two minute, send low a digital signal to SMPS and this one is setting in off state. From an electrical analysis, the power consumption in off mode of the washing machine is composed by the consumption of its parts and the total value is 0,3 W. Instead, the power consumption measured in stand-by mode is 828 mW that is lower of 1 W (see the regulation on energy saving).This means that the consumption in non operation mode is 60% lesser.

Regarding the field of the energy conversion, and in particular power converter to supply the unit control driver of IGCT devices. A study has been performed in order to improve the performance of the converter. In this field the most critical issue is tied to a wide input voltage line that supplies the system. The system described and realized provide a stable output voltage and it is composed by the cascade of a first not isolated stage that provides 300 V output with an input voltage in the range between 300 and 3000 V. The chosen topology has been a buck converter and MOSFET devices in series connection have been used in order to obtain a better $R_{DS,on}$ than a single device and a breakdown voltage up to 3000 V. In general, the series connection is able to work at higher frequency than a single device with the same breakdown voltage and nominal current and allows to improve the performance of the converter. In order to avoid voltage imbalance a suitable snubber circuit has been used in parallel connection with the devices and optocouplers have been used to drive the gate of each device and to ensure galvanic isolation between power side and the driver (signal side). Design procedures and experimental results have been shown and the efficiency of the realized prototype has been evaluated.

# I. Appendix

## The Flyback Converter

## A.    Introduction

In Figure I.1 is shows the model of the flyback converter [34]. The operation can be quickly understand to look the position of the dot in the primary and secondary winding of the transformer. When the switch is on (turn on of power MOSFET), the edge of the windings with the dot are positive than the edge without the dot. Therefore, the output rectified diodes are reverse polarized and all current is provides to the load by means the output capacitor, $C_{out}$.
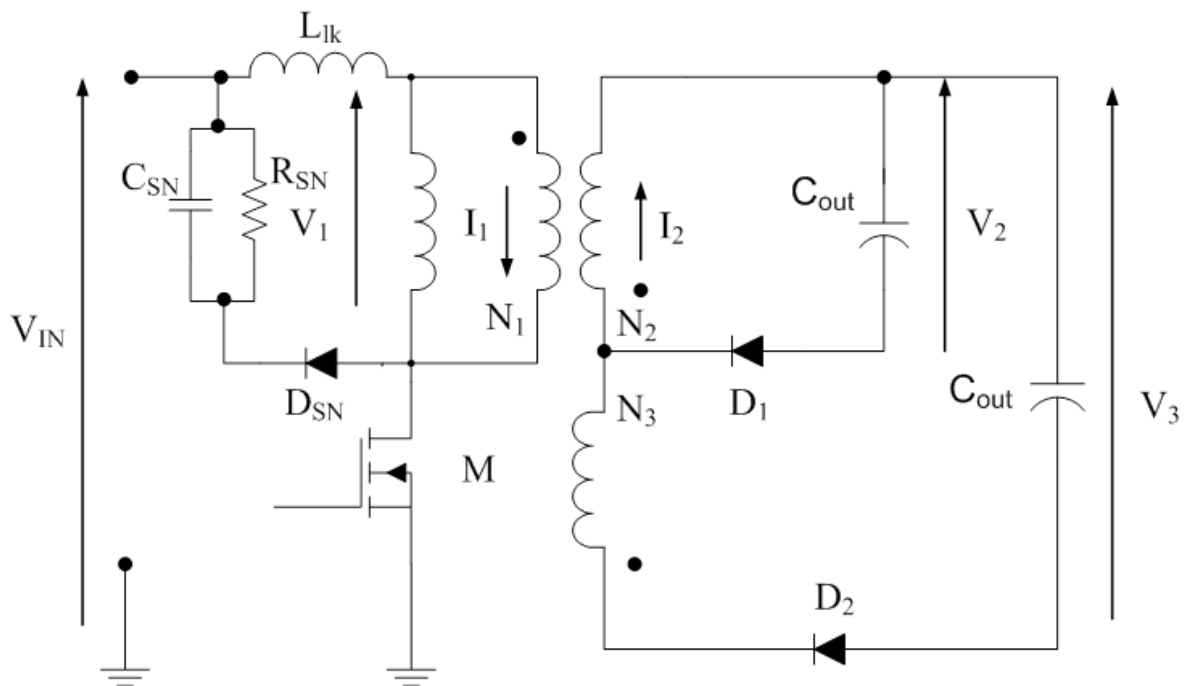


Figure I.1: Configurazione del convertitore Flyback

Also, during the turn on time of the power MOSFET a constant voltage is provided at the primary winding $N_1$ and the current on it increase linearly Figure I.2a with a slope of:

$$\frac{dI}{dT} = \frac{V_{IN}}{L_1}.$$

Eq. I.1

Where $L_1$ is the magnetic inductance of the primary and $V_{IN}$ is the input voltage, furthermore, the voltage drop on the device when this one is on and the leakage inductor has been neglected. At the end of the turn on time the current has reached the peak value, that is equal to $I_{1max}$.

$$I_{1max} = \frac{V_{IN}T_{on}}{L_1}.$$

Eq. I.2

The energy stored by primary inductor is E and provide by equation Eq. I.3.

$$E = \frac{1}{2} L_1 I_{1\,max}^2 \qquad \text{Eq. I.3}$$

Where $E$ is the energy in Joule and $L_1$ is the inductor in Henry, $I_{1max}$ the peak current in Ampere.

Because the current in an inductor can't be changed instantly, when the power MOSFET is off the current of the magnetization inductor forces a polarity change on all windings. On the turn off, the current on the primary is transfer to secondary with a value of $I_{2max}$.

$$I_{2\,max} = I_{1\,max} \frac{N_1}{N_2} \qquad \text{Eq. I.4}$$

In this way the edge with the dot of the winding $N_2$ is negative than other edge and the current can flows in de diode and decrease (Figure I.2) with a slope as in the relationship Eq. I.5.

$$\frac{dI_2}{dt} = \frac{V_2}{L_2} \qquad \text{Eq. I.5}$$

dove L2 è l'induttanza del secondario.
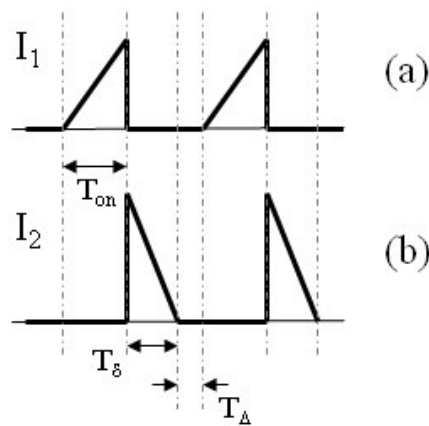


Figure I.2: Waveform of input and output current in the transformer

## B. Operations modes

The flyback converter can be used in different mode of operation. It said that one work in DCM ("Discontinuous Conduction Mode", Figure I.3a) when the current on the secondary goes to zero before the next cycle (next turn on of the MOSFET). This occurred because the secondary of the transformer has discharged all energy stored to transfer it in the load.

Instead, if the energy doesn't be transfer all to the load before the next cycle, the current in the secondary doesn't reach zero and the primary current star from a value greater zero in the next cycle. In this way, the converter work in CCM ( "Continuous Conduction Mode", Figure I.3c). In DCM the waveform of the current is a triangular, instead in CCM the current waveform is trapezoidal.

When the device work on the edge between DCM and CCM, the flyback operation is said "transition mode", Figure I.3b.



Figure I.3 Operation Modes.

In particular, in continuous mode the flux in the transformer doesn't reach zero, in this way during the turn on, of the power MOSFET, the current in the primary winding is shown in Eq. I.6.

$$I_1 = I_{1\min} + \frac{V_1}{L_1} t \qquad 0 < t < T_{on} \qquad \text{Eq. I.6}$$

Where $I_{1min}$ is the minimum value of the current $I_1$ at the start of the cycle, the value of it will be evaluated on follow. At the end of the turn on the $I_1$ reach its maximum value $I_{1max}$.

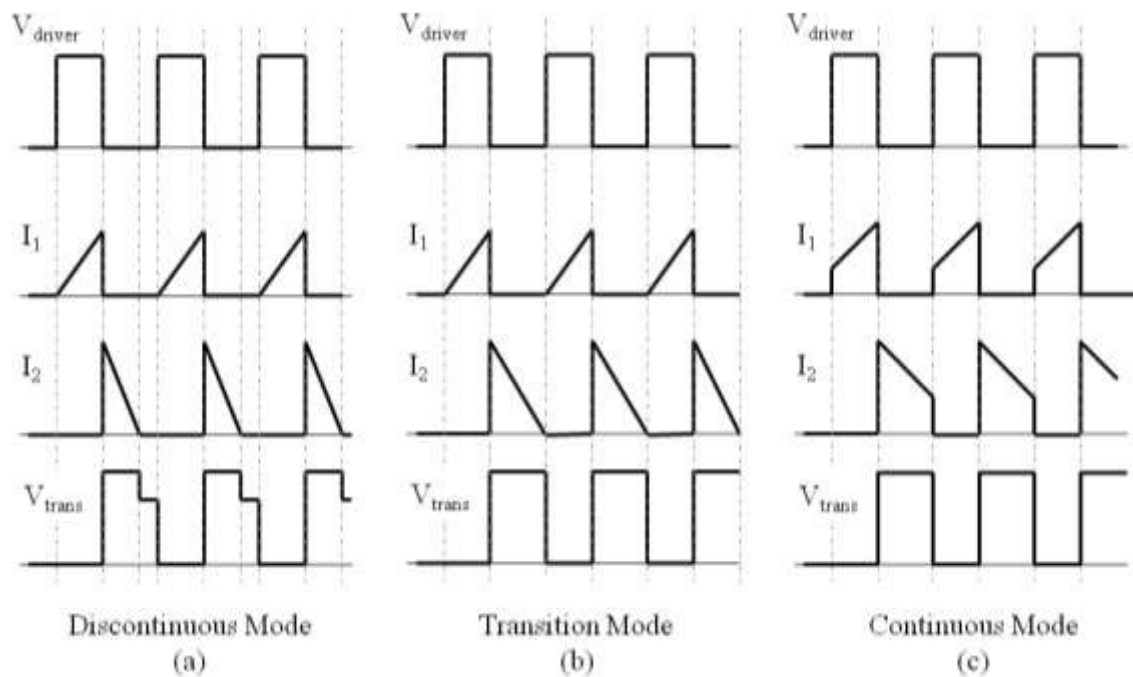$$I_{1max} = I_{1min} + \frac{V_1 T_{on}}{L_1} = I_{1min} + \frac{V_1 DT}{L_1} \qquad 0 < t < T_{on} \qquad \text{Eq. I.7}$$

Where D is the duty cycle and shows the part of switching cycle T when the power \\MOSFET is on. The value of D can change from 0 (the power MOSFET is always off) and 1 (the power MOSFET is always on). At the end of the conduction phase the energy stored is:

$$E = \frac{1}{2} L_1 \cdot I_{1max}^2 \qquad \text{Eq. I.8}$$

At the end of the conduction time, the power MOSFET goes off and blocks the current $I_1$. The conservation of the energy stored in the transformer causes the current $I_2$ in the secondary of the transformer, whose start value $I_{2max}$ can be calculated by using the conservation of the energy stored in the transformer in its transfer from the primary to the secondary.

$$E = \frac{1}{2} L_1 \cdot I_{1max}^2 = \frac{1}{2} L_2 \cdot I_{2max}^2 \qquad \text{Eq. I.9}$$

By substituting $L1$ and $L2$ with its expression in terms of reluctance $\Re$ of the magnetic circuit and the number of turns of the windings of the transformer, is obtained:

$$E = \frac{1}{2} \frac{N_1^2}{\Re} \cdot I_{1max}^2 = \frac{1}{2} \frac{N_2^2}{\Re} \cdot I_{2max}^2 \qquad \text{Eq. I.10}$$

Hence:

$$I_{2max} = \frac{N_1}{N_2} \cdot I_{1max} \cdot \qquad \text{Eq. I.11}$$

The voltage $V_2$ can be calculated from flux/voltage relationship.

$$V_1 = N_1 \frac{d\varphi}{dt} \cdot$$

$$\qquad \text{Eq. I.12}$$

$$V_2 = -N_2 \frac{d\varphi}{dt} \cdot$$

Hence:

$$V_2 = -\frac{N_2}{N_1} \cdot V_1 \qquad\qquad 0 < t < T_{on} \qquad\qquad \text{Eq. I.13}$$

During the off state, the energy stored within the magnetic circuit during the on state, is transfer to the capacitor $C_{out}$.

$$V_2 = -L_2 \frac{dI_2}{dt} \qquad\qquad\qquad \text{Eq. I.14}$$

$$I_2 = I_{2\,max} - \frac{V_2}{L_2}(t - DT) \qquad\qquad T_{on} < t < T \qquad\qquad \text{Eq. I.15}$$

At the end of the off state, $I_2$ decrease to minimum value $I_{2min}$.

$$I_{2\,min} = I_{2\,max} - \frac{V_2}{L_2}(T - DT) \qquad\qquad T_{on} < t < T \qquad\qquad \text{Eq. I.16}$$

Also at the and of the off state can be applied, similarly as at the end of the on state, the conservation of the energy stored in the transformer.

In order to evaluate $V_1$ the relationships in Eq. I.12 are used.

$$V_1 = -\frac{N_1}{N_2} \cdot V_2 \qquad\qquad T_{on} < t < T \qquad\qquad \text{Eq. I.17}$$

The voltage drop on the power MOSFET, $V_t$, is equal to Eq. I.18

$$V_t = V_{IN} - V_1 = V_{IN} + \frac{N_1}{N_2} \cdot V_2 \qquad\qquad T_{on} < t < T \qquad\qquad \text{Eq. I.18}$$

In order to obtain the relationship between input and output, the operation of the converter has been considered in steady state. The average voltage drop in the winding must be null. In particular, in the secondary winding, the average voltage drop $\overline{V_2}$ is considered.

$$\overline{V_2} = \frac{1}{T}\left(-\frac{N_2}{N_1} V_1 DT + V_2(T - DT)\right) = 0 \qquad\qquad \text{Eq. I.19}$$

It follows:

$$V_2 = \frac{N_2}{N_1}\frac{D}{1-D}V_1 \qquad\qquad \text{Eq. I.20}$$

The relationship obtained is the same of the boost converter with the addition of the ratio $N_1/N_2$, this is due to similar principle diagram between a flyback converter and a boost converter in which the inductor is replaced by a transformer with turns ratio $N_2/N_1$. The output voltage does not depend on the current output, but only by duty cycle and from the input voltage. If one considers the converter will be ideal that the input power and the output power will be the same, and then:

$$\bar{I}_1 = \frac{\overline{V_2}}{\overline{V_1}}\cdot \bar{I}_2$$

$$\bar{I}1 = \frac{N_2}{N_1}\frac{D}{1-D}\cdot \bar{I}_2 \qquad\qquad \text{Eq. I.21}$$

The value of $I_{1min}$ e $I_{1max}$, can be calculated from the average value of $I_1$.

$$\bar{I}_1 = \frac{N_2}{N_1}\frac{D}{1-D}\cdot \bar{I}_2 \qquad\qquad \text{Eq. I.22}$$

$$\bar{I}_1 = \frac{1}{T}\int_T I_1(t)dt = \frac{1}{T}\left( I_{1min}DT + \frac{DT(I_{1max}-I_{1min})}{2} \right)$$
$$= D\left( I_{1min} + \frac{I_{1max}-I_{1min}}{2} \right) \qquad\qquad \text{Eq. I.23}$$

By substituting $I_{1max} - I_{1min}$ with the relationship in terms of $V_1$, $D$, $T$, and $L_1$(see Eq. I.7), is obtained:

$$\bar{I}_1 = D\left( I_{1min} + \frac{V_1DT}{2L_1} \right) \qquad\qquad \text{Eq. I.24}$$

And by substituting $\bar{I}_1$ with the expression in terms of secondary current:

$$I_{1min} = \frac{N_2}{N_1}\frac{1}{1-D}\bar{I}_2 - \frac{V_1D}{2L_1f} \qquad\qquad \text{Eq. I.25}$$

$$I_{1max} = \frac{N_2}{N_1}\frac{1}{1-D}\bar{I}_2 + \frac{V_1D}{2L_1f} \qquad\qquad \text{Eq. I.26}$$

Using the transformation rapport, the $I_{2min}$ e $I_{2max}$ expression is calculated.

$$I_{2\,min} = \frac{1}{1-D}\bar{I}_2 - \frac{N_1}{N_2}\frac{V_1 D}{2L_1 f}$$

$$I_{2\,max} = \frac{1}{1-D}\bar{I}_2 + \frac{N_1}{N_2}\frac{V_1 D}{2L_1 f}$$

Eq. I.27

In discontinuous mode of operation, the energy required by the load is sufficiently low and can be transferred in a time lesser than the switching period. In this case, the magnetic flux in the transformer is zero for part of the period. The only difference with the principle described above is that the energy stored in the magnetic circuit is zero at the beginning of the cycle. Although small, the difference between the two modes has a strong impact on the relationship of the output voltage. In discontinuous mode, the difference than the previous relationship is that $I_{1min}$ is null in conduction phase of the transistor:

$$I_1 = \frac{V_1}{L_1}t$$

Eq. I.28

$$I_{1\,max} = \frac{V_1 DT}{L_1}$$

Eq. I.29

$$I_{2\,max} = \frac{N_1}{N_2}I_{1\,max} = \frac{N_1}{N_2}\frac{V_1 DT}{L_1}$$

Eq. I.30

It follows:

$$V_2 = -\frac{N_2}{N_1}V_1$$

Eq. I.31

In the off state, the energy stored in the last cycle is transfer to the output capacitor.

$$I_2 = I_{2\,max} - \frac{V_2}{L_2}(t - DT) \qquad\qquad T_{on} < t < T$$

Eq. I.32

In off state, the $I_2$ vanishes after a time $\delta T$, that is the reset time.

$$I_{2\,max} - \frac{V_2}{L_2}\delta T = 0$$

Eq. I.33

by substituting the $I_{2max}$ with Eq. I.30, it follows:

$$\delta = \frac{V_1}{V_2} \frac{L_2}{L_1} \frac{N_1}{N_2} D \qquad\qquad \text{Eq. I.34}$$

By substituting $L_1$ and $L_2$ with their respective relationships in terms of reluctance $\Re$ of the magnetic circuit and the number of turns of the windings of the transformer, is obtained:

$$\delta = \frac{V_1}{V_2} \frac{N_2}{N_1} D \qquad\qquad \text{Eq. I.35}$$

The load current Io is equal to the average current through the diode, $I_2$. The current through the diode is equal to that of the secondary in off state. Therefore the current through the diode can be written as follows:

$$I_{DIODE} = \bar{I}_2 = \frac{I_{2\max}}{2} \delta \qquad\qquad \text{Eq. I.36}$$

By substituting $I_{2\max}$ and $\delta$ with the respectively relationship, is obtained:

$$I_{DIODE} = \frac{N_1}{N_2} \frac{V_1 DT}{2L_1} \frac{V_1}{V_2} \frac{N_2}{N_1} D = \frac{V_1^2 D^2 T}{2L_1 V_2} \qquad\qquad \text{Eq. I.37}$$

The voltage gain of the output can be write as:

$$\frac{V_2}{V_1} = \frac{V_1 D^2 T}{2L_1 I_{DIODE}} \qquad\qquad \text{Eq. I.38}$$

Regarding the operation mode at the border between continuous and discontinuous (transition mode), the border is reached when the current in the inductor became zero as soon before the switching of the transistor.

$$DT + \delta T = T$$
$$D + \delta = 1 \qquad\qquad \text{Eq. I.39}$$

In this case the output current limit, $I_{2\lim}$, is provided by equation:

$$I_{2\lim} = \bar{I}_2 = \frac{I_{2\max}}{2}(1 - D) \qquad\qquad \text{Eq. I.40}$$

By substituting the $I_{2\max}$ with the relationship in discontinuous mode:

$$I_{2\,\text{lim}} = \frac{N_1}{N_2}\frac{V_1 DT}{2L_1}(1-D)$$

Eq. I.41

At the border between the two conduction mode, the output voltage follows the expressions of the two modes. The relationship of the continuous mode has been used.

$$\frac{V_2}{V_1} = \frac{N_2}{N_1}\frac{D}{1-D}$$

Eq. I.42

The output current can be written as follow.

$$I_{2\,\text{lim}} = \frac{N_1}{N_2}\frac{V_1 DT}{2L_1}\frac{N_2}{N_1}\frac{V_1}{V_2}D = \frac{V_1 DT}{2L_1}\frac{V_1}{V_2}D$$

Eq. I.43

The following annotations are used: $\left|V_2\right| = \dfrac{V_2}{V_1}$ that is the voltage gain of the converter, and:

$\left|I_2\right| = \dfrac{I_2}{\dfrac{N_1}{N_2}\dfrac{TV_1}{L_1}}$, where the term: $\dfrac{N_1}{N_2}\dfrac{TV_1}{L_1}$ is the maximum current that can be reach

theoretically over a cycle (D = 1). In steady state $\left|I_2\right| = 0$ when the output current is zero, and $\left|I_2\right| = 1$ when the output current is maximum.

Using these notations is obtained:

1. In continuous mode:

$$\left|V_2\right| = \frac{N_2}{N_1}\frac{D}{1-D}$$

Eq. I.44

2. In discontinuous mode:

$$\left|V_2\right| = \frac{N_2}{N_1}\frac{D^2}{2\left|I_2\right|}$$

Eq. I.45

3. The current limit in transition mode, between continuous and discontinuous mode:

$$I_{2\,\text{lim}} = \frac{N_1}{N_2}\frac{V_1 T}{2L_1}D(1-D) = \frac{I_{2\,\text{lim}}}{2\left|I_2\right|}D(1-D)$$

Eq. I.46

The border between two regions is described by the following relationship:

$$\frac{1}{2|I_2|} D(1-D) = 1$$

Eq. I.47

The curve has been drawn for $\frac{N_2}{N_1} = 1$.
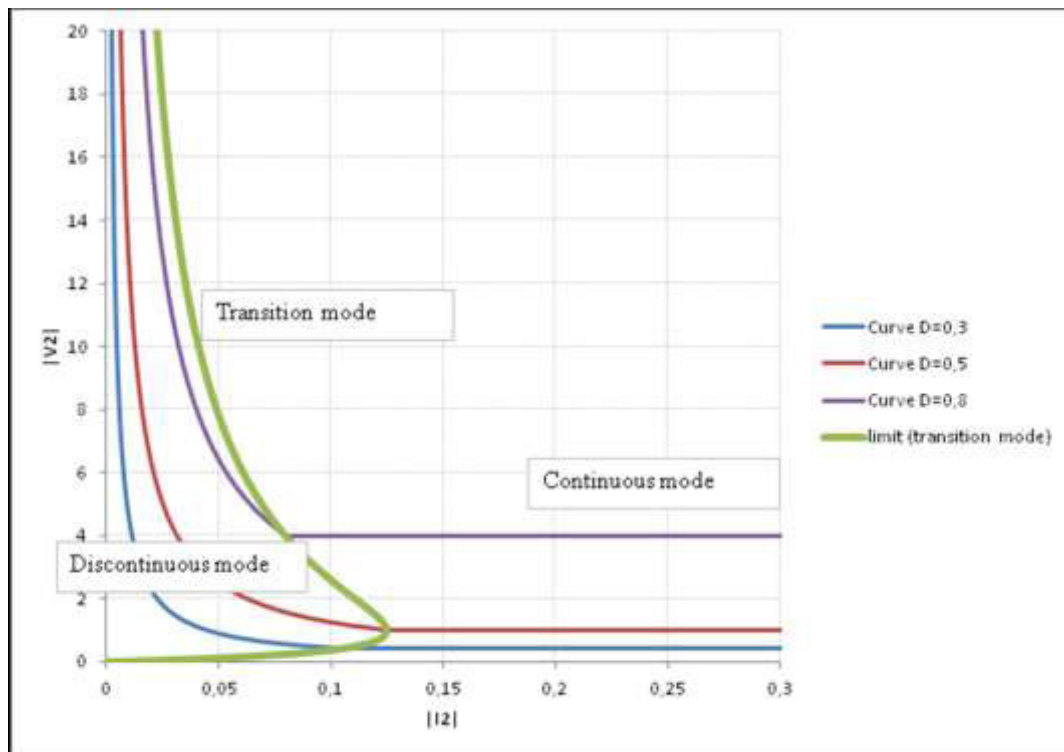


Figure I.4: output voltage normalized $|V_2|$ vs. output current normalized $|I_2|$

## C.    Waveform of the voltage drop on the power switching device

The flyback schematic and the clamp network that are shown in **Figure I.5** have been analyzed [34]. Also in the figure, is shown the qualitative waveform of the voltage that must be blocked from the power switch during the turn off.

At the end of on time, the current on the switch has reached the maximum value, and both the magnetization inductance and the leakage inductance have accumulated energy. As soon as the switch is switched off by the control signal, the magnetization inductance reverses the voltage, and this value is blocked to $V_{fl}$ that is the output voltage mirrored in the primary. The leakage inductance instead generates an extra voltage that without the presence of the clamp network would reach a very high value, limited only by the parasitic resistance of the circuit. As a result of these consider the waveform in **Figure**

**I.5** can be described as follows: at the beginning of the off time, the voltage applied on the device is $V_{IN} + V_{fl} + V_{spike}$ plus a small overvoltage due to the clamp diode.

After the phase to turn on of the clamp diode, the voltage is blocked at the value: $V_{IN} + V_{fl} + V_{spike}$.
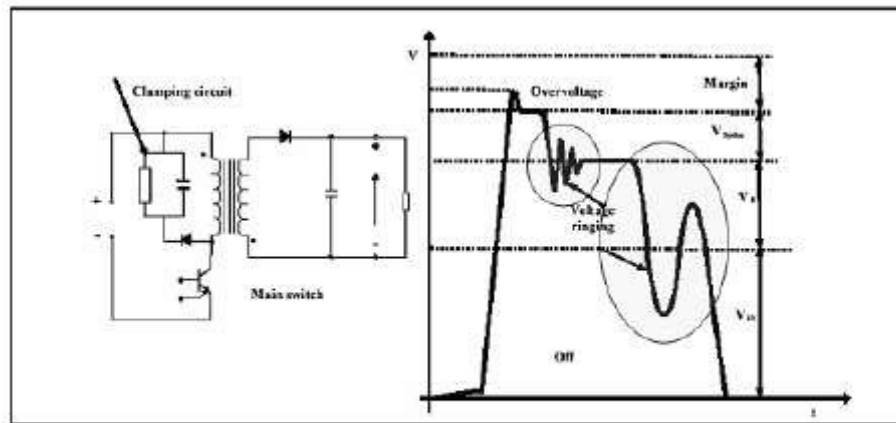


Figure I.5 Voltage drop in the power transistor

The voltage on the device, after to be blocked by the clamp network, begin to oscillate about the value $V_{fl}$. These oscillations are caused by the leakage inductance that resonates with the equivalent capacitance of the drain node, due to the parasitic capacitance of the transformer and the device, and have an amplitude value of $V_{spike}$. As soon as the magnetization inductance is fully demagnetized, begin the second oscillations around $V_{IN}$, with amplitude $V_{fl}$, which this time is due to the equivalent capacitance that resonates with the inductance of magnetization. As can see in the figure, this one has frequency smaller do to greater value of the magnetization inductor than leakage inductor.

# BIBLIOGRAPHY

[1] "Direttiva 2005/32/CE del dipartimento europeoe del consiglio", 6 July 2005.

[2] "REGOLAMENTO (CE) N. 1275/2008 DELLA COMMISSIONE", 17 December 2008

[3] CEI EN 62301, "household electrical appliances – Measurement of stand-by power" April 2006, First edition.

[4] "REGOLAMENTO (CE) N. 244/2009 DELLA COMMISSIONE", 18 March 2009

[5] C. Lazzarotti, A. Raciti, S. Tomarchio, "Analysis of Power Converters for LED Lamps", Convegno Nazionale AEIT 2011, Milano (Italy), 27 – 29 June 2011.

[6] L. Ribellino, S. Pioppo, K. Blaha, J. Milsimer, "Circuiti di Pilotaggio ad Alto Rendimento per Lampade a LED", AEIT 2009, Catania, September 27-29, 2009, pp. 1-6.

[7] M. Di Guardo, S. A. Russo, F. Chimento, G. Laudani, S. Musumeci, A. Raciti, "Alimentazione di LED per Retroilluminazione di Schermi LCD", AEIT 2009, Catania, September 27-29, 2009, pp. 1-6.

[8] S. M. Sze, "Physics of semiconductor devices", 2th edition, 1981.

[9] K.I. Hwu, Y.T. Yau, Li-Ling Lee, "Powering LED Using High-Efficiency SR Flyback converter", IEEE Transactions on Industry Applications, Vol. 47, NO. 1, Jan – Feb. 2011, pp. 376 – 386.

[10] N. Mohan, T. M. Undeland, W. P. Robbins, "Power Electronics", Second edition, 1995, John Wiley & Sons, Inc.

[11] A. I. Pressman, "Switching power supply design", Mc Graw-Hill, Inc. New York, 1991.

[12] Jacek J. Jozwik, M. K. Kazimierczuky, "Dual Sepic PWM Switching-Mode DC/DC Power Converter", IEEE Transactions on Industrial Electronics, Vol. 36, No. I, Febr. 1989, pp 64-70.

[13] D. Gacio; J. M. Alonso; J. Garcia; L. Campa, M. Crespo, M. Rico-Secades, "PWM Series Dimming for Slow-Dynamics HPF LED Drivers: the High Frequency Approach", IEEE Transactions on Industrial Electronics, March 22, 2011.

[14] L. Yu, J. Yang, "The Topologies of White LED Lamps' Power Drivers", Power Electronics Systems and Applications, 2009. PESA 2009, 3rd International Conference, May 20–22, 2009, pp.1-6.

[15] Y. Gu, Z. Lu, L. Hang, Z. Qian, and G. Huang. "Three-level LLC series resonant dc/dc converter". IEEE Trans. Power Electron., vol. 20, issue. 4, Jul. 5, 2005, pp. 781–789.

[16] M. Z. Youssef, P. K. Jain. "A front end self-sustained LLC resonant converter". IEEE 35th Annual Power Electronics Specialists Conference, PESC 04, Aachen, Germany, Jun. 20–26, 2004, Vol. 4, pp. 2651–2656.

[17] C. Q. Lee, K. Siri. "Constant switching frequency LLC type series resonant converter", in Proc. 32nd Midwest Symp. Circuits Syst., Urbana,IL, Vol. 1, Aug. 14–16, 1989, pp. 513–516.

[18] J. Garcia, M. A. Dalla-Costa, J. Cardesin, J. M. Alonso, M. Rico-Secades, "Dimming of High-Brightness LEDs by Means of Luminous Flux Thermal Estimation", IEEE Transactions on Power Electronics, Vol. 24, Issue 4, April 2009, pp. 1107-114.

[19] J.P. Ross, Alan Meier, "Whole-House Measurements of Standby power Consumption", International Conference on Energy Efficiency in Appliances, September, 2000.

[20] A. Meier, W. Huber, K. Rosen, "Reducing Leaking Electricity to 1 Watt", The 1998 ACEEE Summer Study on Energy Efficiency in Buildings, August 1998.

[21] Hang-Seok Choi, D.Y Huh, "Techniques to minimize Power Consumption of SMPS in Standby Mode", PESC'05, Recife, Brazil, June 16, 2005, pp. 2817-2822.

[22] Jee-Hoon Jung, Jong-Moon Choi, Joong-Gi Kwon, "Novel techniques of the reduction of standby power consumption for multiple output converters", IEEE Applied Power Electronics Conference and Exposition, APEC 2008, February 24-28, 2008, Austin, Texas.

[23] Joon Heo, Choong Seon Hong, Seok Bong Kang, Sang Soo Jeon, "Design and Implementation of Control Mechanism for Standby Power Reduction" IEEE Transactions on Consumer Electronics, Feb. 2008, Vol 54, Issue: 1, pp.179 - 185.

[24] S.Buonomo, F. Distefano, A. Gaito, R. Scollo, F. Chimento, A. Raciti, S. Tomarchio, D. Armenia,"Series Connection of Power Switches in High Input Voltage with Wide Range Power Supply for Gate Driving Application", third IEEE Energy Conversion Congress, ECCE 2011, Phoenix (Arizona), 17- 22 September 2011.

[25] S. Eicher, S. Bernet, P. Steimer, A. Weber, "The 10 kV IGCT. A new Device for Medium Voltage Drivers", Proceedings of IAS Industry Applications Conference 2000, October 2000, pp. 2859-2865 vol. 5.

[26] S. Klaka, M. Frecker, H. Gruening, "The Integrated Gate-Commutated Thyristor: A New High Efficiency, High-Power Switch for Series or Snubberless Operation", PCIM'97 Europe.

[27] E. I. Carroll, "Power Electronics for very High Power Applications", Power Engineering Journal, Apr. 1999 Vol. 13, no. 2. pp. 81.

[28] G. Belvedere, A. Galluzzo, M. Melito, S. Musumeci, A Raciti, "Snubberless Voltage Sharing of Series Connected Insulated-Gate Device by a Novel Gate Control Strategy", IEEE Transactions on Powe Electronics, January 2001, Vol. 16, No. 1, pp.132-141.

[29] G. Belvedere, A. Galluzzo, G. Greco, M. Melito, S. Musumeci, A Raciti, "Control of the switching Transients of IGBT Series Strings by High-Performance Drive Units", IEEE Transaction on Industrial Electronics, June 2001, Vol. 48, No 3, pp. 482-490.

[30] K. Sasagawa, Y. Abe, K. Matsuse, "Voltage-Balancing Method for IGBTs Connected in Series", IEEE Transactions on Industry Application, July-August 2004, pp. 1025-1030 vol. 40.

[31] Herbert L. Hess, R. Jacob Baker, "Transformerless Capacitive Coupling of Gate Signals for Series Operation of Power MOS Devices", IEEE Transactions on Power Electronics, Sept. 2000, Vol. 15, pp. 923-930.

[32] F. V. Robinson, V. Hamidi, "Series Connecting Devices for High Voltage Power Conversion", Proceedings of UPEC 2007, 4-6 Sept. 2007, pp. 1134-1139.

[33]J.W. Baek, D.W. Yoo, H.G. Kim, ,"High Voltage Switch Using Series-Connected IGBTs With Simple Auxiliary Circuit", IEEE Transactions on Industry Application, Nov. – Dec. 2001, Vol. 37, pp. 1832 - 1839.

[34] Application Note AN 1262, C. Adragna "Offline Flyback converters design methodology with the L6590 family"