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Innovative Power Devices in Si, SiC, and GaN: Modeling, Characterization, and Applicative Aspects

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Ph.D. Thesis

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Abstract

Power semiconductor devices are being more and more spreading, because of new applications in renewable energy and electrical vehicles. The need of studying topics related to power devices is even reinforced thanks to new wide band-gap materials, such as Silicon Carbide (SiC) and Gallium Nitride (GaN), which have superior features in comparison to Silicon (Si), but also to innovative package solutions. For these reasons, the aims of this Thesis regard modeling, characterization, and applicative aspects of innovate Si, SiC, and GaN devices, taking the advantage of a strong cooperation with industrial experience. Firstly, a review of the various power loss estimation methods, regarding all relevant device types, is accomplished, considering the most important electric and thermal experimental methods, analytical and numerical models. Then, a comprehensive and industry-related collection of the most important issues, encountered during the design phase of SiC power modules for tractions inverters, is given. Electric simulations have performed to evaluate the losses and junction temperature, parallel connection of dice inside a switch is studied by circuit simulations, Finite Element Method (FEM) models have developed to determine the thermal behaviour. Moreover, gate-source overvoltages problem, short circuit, and avalanche topics are treated. GaN power devices are then focused with a work that studies the dependences of dynamic drain-source resistance (dynamic $R_{DS(ON)}$) on frequency, off time and voltage, temperature, and current, resulting in a novel applicative parametric study based on available literature data. A new FEM flow is proposed to study a GaN-surface-mounted device (SMD), to evaluate the thermal behavior of copper traces inside the package. This is achieved by an electromagnetic simulation to get the power losses, followed by a

thermal study having the previously computed loss as input: package reliability is not reduced, because of the copper layer's elastic regime deformation. The last part deals with SMD packages based on Si MOSFETs. Various high voltage MOSFET-based packages have studied experimentally. Furthermore, an analytical thermal model is proposed, which accounts for the heat transfer in the package and board system, resulting in a good trade-off between accuracy and low computation burden. The last chapter presents an innovative simulated-based design flow especially focused on low-voltage MOSFET-based packages, which comprises thermo-mechanical models to evaluate lifetime of solder joints (useful to compare structurally different options), electro-magnetic simulations to compute $R_{DS(ON)}$ and parasitic elements, and a thermal evaluation to ensure that the package's temperature is below the maximum rating.

Introduction

Both traditional and innovative applications in power electronics framework require the use of semiconductor-based power devices, which are fundamental pillars to process electric power. New application contexts encompass environments such those related to renewable energies, with, as an example, wind and photovoltaic-related converters, and distributed generation. On the other hand, automotive market is rapidly spreading: electric vehicles, both hybrid and full plug-in, need to be carefully designed. Hence, innovative power devices must be modeled, simulated, and tested in application-like conditions, to properly characterize and predict its behavior.

This Thesis will consider both "traditional" silicon (Si)-based low-voltage and high-voltage power MOSFETs, and wide band-gap-based power devices, such as silicon carbide (SiC) metal–oxide–semiconductor field-effect transistors (MOSFETs) and gallium nitride (GaN) high electron mobility transistors (HEMTs). Among the applications related to SiC power modules, there are traction inverters, while those related to GaN HEMTs and Si low-voltage MOSFETs are used, as an example, in auxiliary DC-DC converters. High voltage Si MOSFETs are, instead, employed in industrial field, such as server or telecom applications, but their use will become more and more present also in automotive framework, such as in on-board chargers.

The final requirement in this kind of devices is to have a high efficiency, thereby ensuring a flawless power conversion. However, power losses are unavoidable, due to conduction and switching processes. These phenomena are strictly related to the heat generation in power devices. More in general, thermal management of the entire converter must be

assessed. For these problems, power losses estimation in semiconductor devices is of paramount importance and it is carefully considered in the introduction part of this Thesis. More in detail, in the first Part of the work a review on power losses estimation methods is addressed, considering both experimental methods and model-based ones, analyzing both Si- and WBG-based devices. Electrical methods, including double pulse test, and thermal ones, with calorimetric techniques, are dealt with.

In Part II, SiC based power modules are focused, pointing out the main applicative issues present in the design phase of innovative traction inverters, such as electro-thermal modeling, paralleling, reliability and layout issues. Moreover, a comparison between simulation and experimental techniques to compute the thermal impedance of the module is addressed.

GaN-based devices are studied in Part III, firstly by a review of the main application-like consequences of dynamic on-state resistance on off voltage and time, load current, temperature, and switching frequency. Then, a new integrated electromagnetic-thermal finite-element flow is proposed for an integrated GaN HEMT, which can give insight into the copper traces design phase. This model considers firstly an electromagnetic simulation, which permits power losses computation in copper traces. Then, this power becomes the input of the thermal simulation, aimed at the temperature computation inside the package.

An analytical model, as well as an experimental analysis of different cooling solutions, are developed in the first chapter of Part IV, which considers high-voltage Si MOSFETs as analyzed technology, taking into account various surface-mounted package solutions. This kind of packages poses new problems in cooling system's design, as they are attached to printed circuit board. Surface mounted packages are analyzed also in low-

voltage power devices, in Part IV, where a new comprehensive finite-element based design flow is proposed. The test vehicle is a novel system-in-package. The methodology comprises both electromagnetic and thermal simulation. But, at the same time, package’s structural integrity is of crucial importance: hence, a thermo-mechanical simulation is performed to assess the package’s robustness.

Indeed, the main global aim of this Thesis is to study, from different points of view and considering both design and applicative aspects, innovative power devices and packages in Si, SiC, and GaN, giving steps for future developments.

PART I: INTRODUCTION ON LOSSES IN POWER DEVICES

1. POWER LOSSES ESTIMATION METHODS IN SILICON AND WBG SEMICONDUCTOR DEVICES – A REVIEW

The calculation of power losses, especially today, is one of the principal issues in power semiconductor devices, due to the even more stringent requirements for efficiency and power density. Closely related to these requirements, the thermal management of power converters is of paramount importance. Therefore, in recent years, several electrical and thermal methods have been developed to calculate power losses, which have also opposite features, usually different from each other. To date, however, the multiple approaches have not been classified and compared comprehensively. For this reason, a survey of all classes of methods is presented in this chapter, including silicon and wide band-gap power devices technologies. More specifically, in the chapter traditional electrical experimental setups and models are outlined, highlighting their criticalities. In addition, an overview of the best performing thermal methods is described. Finally, a brief comparison among all the methods is presented, highlighting the main advantages and criticalities of the different estimation techniques.

1.1 Introduction

Advanced modern power devices are more and more necessary for a wide class of power electronic applications. The application fields range from high voltage direct current systems to storage systems, from renewable energies, such as photovoltaic and wind systems, to industry applications. There are also home appliances and automotive industry, with the development of electric vehicles on a larger scale, in which power

semiconductors are acquiring even more importance [1], [2]. These needs have paved the way for an ever-increasing demand of power devices that require low power losses. A compromise among reliability, power density, and efficiency must be achieved. Obviously, a high value of devices power losses entails a lower value of converter efficiency [3].

An extensive introduction in the market of silicon-based power semiconductor devices dates back to ‘80s. Insulated gate bipolar transistors (IGBTs) and metal-oxide-semiconductor field-effect transistors (MOSFETs) are today used in power electronics applications [4]. Among the second group of devices, nowadays the Super Junction (SJ) is the technology mostly diffused, for high voltage applications, while trench technology is used for low voltage MOSFETs. Today, wide bandgap (WBG) materials-based devices in Silicon carbide (SiC) and Gallium Nitride (GaN) are used in many applications because of their better thermal and electrical properties in comparison to those based on silicon [5]-[7]. In fact, SiC MOSFETs can reach 200 °C junction temperature, also requiring smaller size in power converter. Higher operating temperature can be reached in converters operation, however there are still reliability issues in SiC devices. SiC devices are present in the today market either for medium or high voltage range applications [8], [9]. GaN switches have even better performance in terms of switching and conduction losses in low-medium power applications with higher switching frequency because of the low internal capacitances [10]-[13]. In GaN high-electron-mobility-transistors (HEMTs), one of the most investigated phenomena is the dynamic on state resistance, as a consequence of trapped charges in devices [14]. In fact, in this case the data provided in datasheet regarding the drain-source resistance usually may not be accurate, despite those regarding Si and SiC devices, resulting in an adjunctive factor to be considered, which in turn

worsens the power losses [15]. SiC, and GaN even more, have favoured the spreading of WBG-based devices on the semiconductor market, especially in automotive field [16]. In the future, also ultrawide-band gap (UWBG) materials, such as gallium oxide (Ga_2O_3), aluminum nitride, and diamond may have a role in power conversion applications [17]-[19]. However, also new silicon based MOSFETs products are still currently under development. These technologies allow a higher power density capability, also thanks to the availability of new packages on the market. The reasons are related to physical devices characteristics, that ensure a more compact design and smaller die size consequently. Another important feature of WBG devices is the possibility to operate at higher switching frequency, high voltage, and current slew rates. But these benefits can be also an issue for the thermal management of power semiconductor devices and, in a more general sense, of the converter. In fact, overheating can compromise both the reliability and efficiency of power converters. Hence, the estimation of power losses plays a key role in order to design the cooling system and to evaluate the junction temperature at the surface of the die. In Figure 1, a scheme of the various types of power devices is reported.

Dependence of losses on operating temperature, especially the conduction ones, is due to the increasing of the drain to source resistance, related to self-heating effect. Moreover, switching losses dependence on load current is well known in literature. Thermal management is strictly related to the conduction period and switching transients at turn on and turn-off, impacting on the system reliability [20]. Instead, the off-state losses, involving the leakage current coupled with the blocking voltage, usually can be neglected [21].

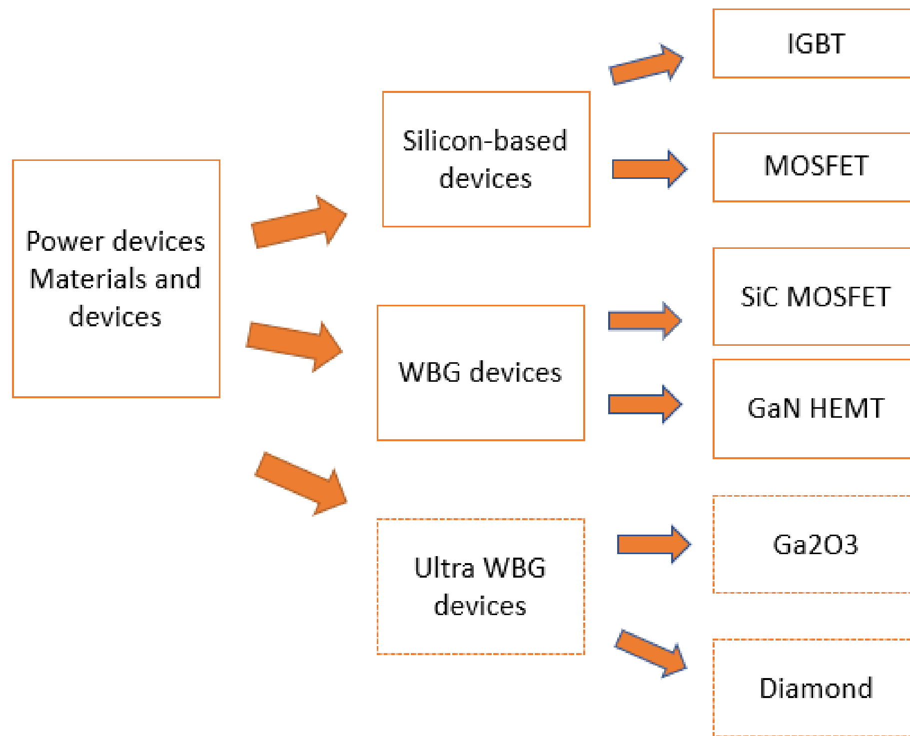


Figure 1. Classification of the main Si and WBG-based power semiconductor devices.

In fact, at higher temperatures, there can be single-event and aging effect problems, due for example to mechanical stress on bonding wires. For example, regarding thermal management, in [22] a model and algorithm are proposed in order to size properly the thermal vias and the thermal pads. In that case, the power loss profile is an input data, and the model considers all heat transfer modes. Power losses are important also for lifetime predictions of discrete devices and power modules [23], based on certain mission profiles, as it can be seen in Figure 2 [24]. The mission profile is the starting point, then the model is obtained considering converter data, thermal and electrical domains, including power losses. With new SiC and GaN power switches, as they permit smaller die size, and therefore higher power density, but also higher thermal resistance, thermal management (i.e., new cooling system concepts) and power losses

reduction have become more and more critical [6]. Basically, in a first phase the device's losses are computed, then these quantities are the input of thermal models, which determine the thermal behaviour of the system. The thermal resistance (or the thermal transient impedance, including also the thermal capacitances) can be determined by means of equivalent thermal networks, e.g Foster or Cauer poles [24].

There exist some method classes to measure or evaluate the losses: electrical methods, analytical methods, and calorimetric or thermal methods.

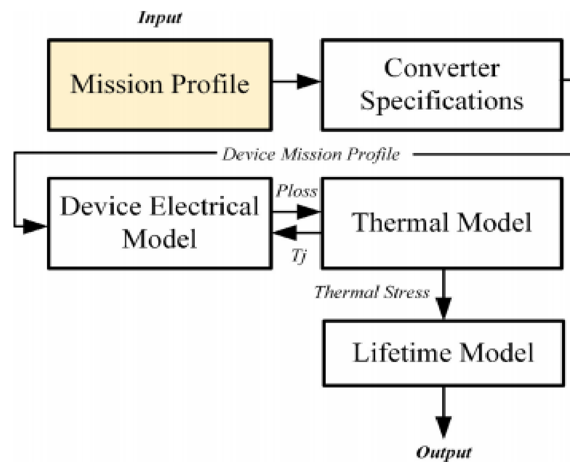


Figure 2. Lifetime model estimation scheme. From [24]

1.1.1 Electrical methods outline

Electrical methods are those traditionally used in power electronics field. Classic double pulse test (DPT) is universally the most used in industry and academy, for both Si- and WBG-based devices. The basic circuit comprises the device under test (DUT), an inductor for inductive load switching, and a freewheeling diode. However, there are issues with WBG devices, due to parasitic inductances and internal capacitances, coupled with high di/dt and dv/dt [25]-[28]. The internal capacitances are

due to the following paths: gate-drain C_{GD} (also referred to as "Miller capacitance"), gate-source C_{GS}, drain-source C_{DS}. The parasitic inductances are due to source, gate, and drain paths. Gate resistance also plays a key role: in fact, the higher this parameter, the higher the switching losses, although this action can alleviate overshoots on the drain-source voltage. The coupling between parasitic elements and high slew rates can bring to switching oscillations in converters [29] and devices [30]. There can be distinguished internal and external parasitic elements, the first are a consequence of the package, the seconds are due to the printed circuit board [31], [32]. For this reason, switching losses caused by charging or discharging of parasitic capacitances inside the device and other physical mechanisms must be accurately considered and modeled. Moreover, devices overshoot and ringing events are possible due to crosstalk phenomenon when power devices are arranged to realize a half-bridge topology. For instance, in case of half bridge topologies the switching transient of the active device can induce the passive device to turn on, or to have voltage overshoot in turn-off. In that case, multi-pulses are almost mandatory if dynamic $R_{ds(on)}$ estimation is required, as they would be capable to take into account more realistic converter operating conditions.

Measured efficiency, especially for WBG devices, and possibly even more for UWBG, may be also over 100%, due to measure errors [18]. Among the measurement issues, especially for advanced applications using WBG switches and high switching frequencies, there are current and voltage probes grounding and bandwidth, and V-I alignment [14]. Regarding the V-I alignment, there exist various techniques in literature allowing the alignment between the two quantities in a proper way. DPT allows the measurement of current and voltage across the power device. To evaluate the dynamic resistance contribution, it is necessary to use a

clamping circuit, because only few nanoseconds is the turn-on period in which usually the voltage value falls from hundreds of volts to very little values. Therefore, even for modern oscilloscopes, it is difficult to catch the voltage difference. Various circuits have been proposed in the last years, a summary of the techniques proposed can be found in [14]. One of the circuits reviewed herein is reported in this review and shown in Figure 3: it is a self-feeding minor current, and it does not introduce external source voltage.

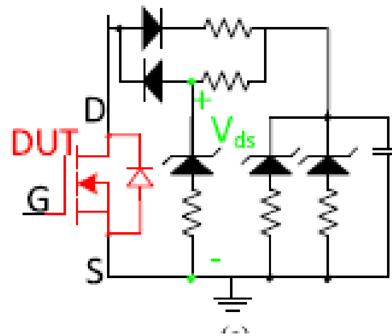


Figure 3. Clamping circuit to measure the on-state voltage, to determine the dynamic resistance. From [14]

Usually, experimental tests are performed to validate analytical models or numerical simulations. Circuit simulators, based on software such as SPICE, are usually employed. They are based on device's behavioural models [34], usually obtained from experimental results. Basic models are available on semiconductor supplier web sites. The main goal is to carry out a method that should be easy, with a simple setup, able to distinguish the loss types for WBG in a wide power range.

The opposition method belongs to another class, developed in the framework of electrical engineering [35], [14]. It was devised for high power converters and employs two identical converters to be used which

can operate in both direct and reverse conditions. This is also the major drawback of the method. In Figure 4, an explanative scheme is shown.

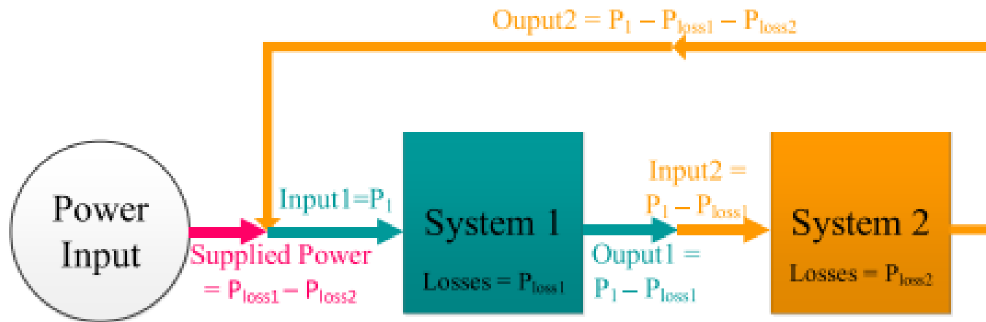


Figure 4. Opposition method schematic. From [14]

There exist several models in literature of semiconductor-based devices, developed in many papers. Several electric equivalent lumped-element circuits, each for a particular transition, are developed and solved [14]. In some cases, it is possible to compute power losses only knowing the datasheet parameters. However, usually these models do not exhibit high accuracy. The traditional models are based on piecewise linear approximations, but they have problems with parasitic and high voltage and current rates. Also, the high frequency can have a negative impact in those types of models [36]. Behavioural models are also used [37], because they can fit well the electrical behaviour based on experimental measures, for example DPT executed at different values of bus voltage, load current, gate voltage, gate resistance, and so on. Usually, to verify new models, or also to characterize new products, DPT is used. But this approach can be not very accurate, because, especially for WBG devices, this technique may bring incorrect results. Classic efficiency measurements can give incorrect results. Physics-based models, also based on technology computer aided design (TCAD) simulations, have been also developed [38]. These models

are based on the resolution of equations related to device physics, such as the doping concentration, or the oxide structure. This technique requires very demanding computing resources and time, although they can be very accurate. In addition, a TCAD simulation requires several device data, which usually are owned by manufactures. They can be also coupled with circuit elements, thereby permitting more complete simulations, but slowing further the simulation time. In another work [34], instead, TCAD-based methods are classified as “numerical methods”.

1.1.2 Thermal or Calorimetric Methods Overview

The other class of methods can be referred to as the thermal or calorimetric ones [39], [40], [41]. Calorimetric methods rely on novel modulations and/or topologies modifications (hardware modification) aimed at power losses identification and separation. Insulating chambers can be or not be included, to measure heat exchange, directly or indirectly. In recent years, several methods have been developed, with different experimental setups [42].

Another class of methods relies on the so-called temperature sensor measures, usually also with the help of modelling strategies [43]. In the last case, several methods comprise mainly circuit models, using only resistors if steady-state operation is considered. But also thermal capacitances can be added, if also the thermal dynamics is taken into account. In any case, a calibration is firstly executed, to determine the thermal resistance characteristics. In temperature sensor methods, the measures of temperature are performed with a thermal camera, in different points of the experimental converter. Then, in the second phase there is the measure of the heatsink or case temperature. The last method is implemented in the most recent literature [15]. In this case, it is important to determine the

model parameters, for example by using least means squares fitting method. These methods are more accurate in general. However, problems with time consuming measures, measurements setups with high complexity, and fitting procedure methods do exist today for thermal methods.

1.1.3 Chapter overview

The objective of this chapter is to give, in the next sections, an outline of the power losses types, to highlight the critical issues of electrical methods of measurement [26]-[52], [152], [154] to give an insight of models for IGBTs [53]-[56], [144], [145], [150] silicon [57]-[69], [134]-[136], [153] [146] SiC devices [70]-[89], [130], [132], [138], [142], [143], [148][129] and GaN devices [90]-[100], [129], [131] [133], [137], [139], [140], [147], [151], [155], and to introduce advanced calorimetric methods [101]-[128], [141], [149]. For each methods class, brief sketches about the various issues will be given: the scope of this section is not to give a detailed description of all the estimation methods for all device types (e.g., Si- and WBG-based ones), rather to define all the main topics in this framework, in broad terms. Moreover, a comparison will be carried out. In particular, accuracy comparison among various electrical and thermal methods has been done. The main merit of this chapter is to give a comprehensive overview of the various measurement methods and models to establish the power losses in both silicon and WBG devices.

Basically, in literature based on the power losses topic, there are two main research lines: one is focused on power devices losses, regardless the final application, while the other one mainly regards applicative conditions, considering also parameters such as the modulations and the possible converter’s topologies. This review regards mainly the first research line.

Nevertheless, sometimes in the sections, in order to explain the power losses mechanisms and computation, certain topologies and control techniques will be outlined, the simplest ones like buck and boost converters, or the half bridge on inductive load, commonly used to characterize the devices. The rest of the chapter is organized as following: in paragraph 1.2 an outline of the various loss types is given, in paragraph 1.3.1 the issues related to electrical measures are briefly recalled, while in Sections 1.3.2, 1.3.3 and 1.4, respectively, analytical (for silicon and WBG, i.e. SiC and GaN materials) and calorimetric methods are described. Finally, in Section 1.5 a comparison is made, and in Section 1.6 the conclusions are drawn.

1.2 Power loss types

A graphical representation of the power loss separation is given in Figure 5 for a SiC MOSFET case [103]. As it can be seen, the conduction losses do not depend on the modulation strategy. Instead, regarding the switching losses, it must be assured if the converter operates in hard or soft switching. In hard switching, there are both turn on and turn off losses. In this framework, several different topologies do exist, such as power factor correctors (PFCs) and motor drive applications. If the zero-voltage switching (ZVS) or zero-current switching (ZCS) conditions are reached, lower switching losses are achieved, because the commutation is operated when current or voltage are near to zero value. However, it is important to avoid, for example in LLC converters, capacitive or other modes, that could bring the power switches to operate in hard switching. If turn off losses are considered, both in hard and soft switching, there is a part of charge that is stored in the output capacitance, and in soft switching case it

is not lost [103]. The use of Kelvin pin, in order to decouple the power and the control signal paths, can lower switching losses contribution.

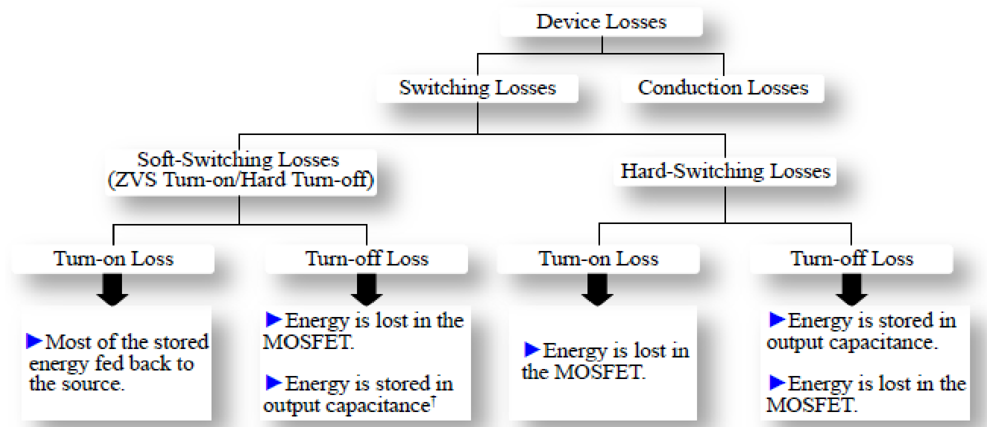


Figure 5. Power loss types in switching devices, divided by switching (turn-on and turn-off) and conduction phases. Both hard and soft switching transitions are considered. From [103]

Conduction losses are a consequence of drain-source on resistance ($R_{ds(on)}$), when the device is in on state. These losses are strongly dependent on the temperature. E_{oss}, that is the energy which is exchanged between power device and the load within the switching cycle [109], is due to C_{oss}, output capacitance hysteresis phenomenon, especially at high frequency investigated in many papers in recent years, because of the resonant applications, should be also considered in efficiency computations and, therefore, in converter's design stage. This phenomenon, for soft switching applications, many times is not focused on datasheets, and it is related to pillar structure in SJ structures [148]. It has been studied in recent literature, above all for GaN devices [146], [148], [151], but also for SiC Shottky diodes [143]. The efforts rely on measurement equipment and methods (such as, for example Sawyer–Tower circuit), in order to better

understand the loss contribution, as well as modelling [140]. In addition, also gate driver losses and losses related to the dead time in converters control should be taken into account. Furthermore, freewheeling diode, which is external to the device in IGBTs and body diode or third quadrant in SiC MOSFETs are included in several models, while in GaN based switches there is not diode, but the device can conduct in both the directions.

If switching transitions are considered, it can be possible to distinguish between hard switching and soft switching. The first mode relies on the intersection, during the switching phase, of current and voltage, which give power losses. Instead, in soft switching operation, the converter can operate in ZVS or ZCS [47], [53], [86], [107], [113], [123]-[125]. In this regard, there exist power converters such as resonant ones, e.g. LLC, or phase shift modulated converters or dual active bridge [103]. In soft switching topologies, the loss calculation is even also more complicated, because the amount of losses is less than the hard switching case [69], [111], [112]. As the converter's switching frequencies are continuously increasing, especially in WBG devices, the switching frequency, which are dependent on such a parameter, are becoming prevalent, while, in high power applications, conduction losses represent the major contribution. Regarding the parallel connection, in both discrete and modular solutions, negative thermal coefficient of $R_{ds(on)}$ is potentially dangerous for thermal runaway, that is a positive feedback mechanism, for example in IGBTs. Instead, MOSFETs have positive thermal coefficient, thereby permitting the parallel connection of more devices, especially in modular packages. But, in this case, mismatches on devices or layout can bring to switching losses increment, and more in general, of uneven loses distribution among the paralleled devices [130].

One important quantity, which can assess a specific power device has been proposed by Baliga: it is the figure of merit $R_{ds(on)}*Q_G$, used in many contexts to compare different devices.

A model of MOSFETs losses in an LLC converter is given in [111], [112], where a time interval analysis is proposed, which goes beyond the traditional first harmonic approximation giving more accurate results. Moreover, an extended device characterization is performed, also with thermal methods, as it will be explained in the paragraph 4. In [37], a new behavioral model is presented for the turn off energy of WBG devices channel computation in ZVS condition. In this case, as showed in Figure 6, there are two current components, one related to channel, and the other one that flows in the output capacitor. That paper extends the Clemente's model, which relates off energy and current, to model E_{off} with curve fitting at a single value

$$E_{off} = \alpha I^{\beta} \quad (1)$$

where α and β, with further equations, are given by (2) and (3):

$$\beta = \frac{\log\left(\frac{E_{off_{ch1}}}{E_{off_{ch2}}}\right)}{\log\left(\frac{I_1}{I_2}\right)} \quad (2)$$

$$\alpha = \frac{E_{off_{ch1}}}{I_1^{\beta}} \quad (3)$$

To extend the model to full current and voltage ranges there exist several methods, such as the use of E_{oss} - V_{ds} curve if it is present in datasheet, or the integration of the product of V_{ds} and E_{oss}, by knowing the C_{oss} - V_{ds} curve (available in datasheets). The full method is explained in detail in the paper cited above.

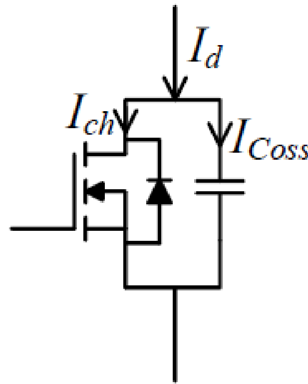


Figure 6. Turn off soft-switching transition current components, related to channel and output capacitance. From [37]

1.3 Equivalent Electric Circuit approaches: Analytical and Simulation Methods

In this section, analytical models, experimental setups, and connected topics are briefly presented. Moreover, the distinction between silicon and WBG based devices is dealt with.

1.3.1 Experimental methods issues

In Figure 7, the hardware components to implement DPT are showed [25], with the control and power parts. In Figure 8, the equivalent electrical circuit, that can be used to make experimental measure or to do analytical calculations, is depicted. In recent years, various papers have evidenced problems related with convectional experimental tests to determine the conduction and switching losses, developing by novel works to present

issues related to DPT and to develop analytical models that cope with this problem.

In [25], [14], issues to be considered are extensively treated for WBG devices, and for GaN in particular, respectively. Here they are briefly recalled.

- Accuracy, bandwidth, and dynamic range of the probes are required to measure fast waveforms during switching transients.
- De-skew of voltage and current oscilloscope channels, as a consequence of V–I timing misalignment.
- Layout of the DPT board must be carefully designed, for parasitic elements.
- Grounding of voltage and current probes should be avoided for the measurement of switching waveforms during transients.
- Cross-talk phenomenon, specifically shoot-through current in half bridge topologies.

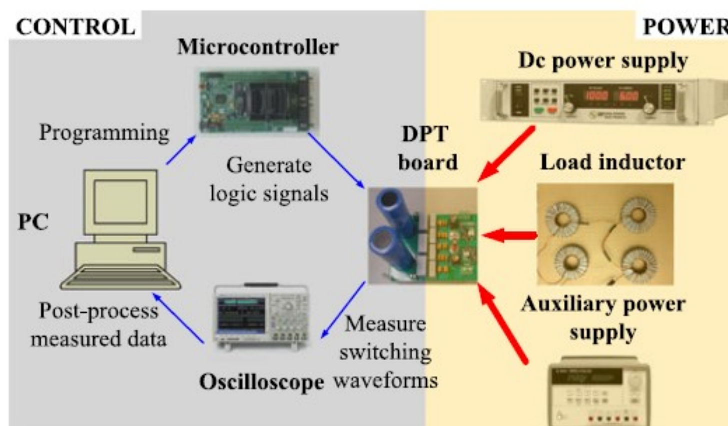


Figure 7. DPT experimental setup scheme, including the power and the control parts. From [25]

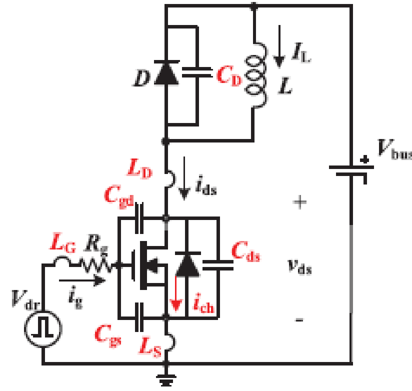


Figure 8. Equivalent electric circuit of DPT, including internal device capacitances, parasitic inductances, body diode with parasitic capacitance, and load inductor. From [74]

1.3.2. Si MOSFET models

Power loss models can be very simple, in comparison to costly experimental setups, to rapidly evaluate the losses contribution in the Si IGBTs and MOSFETs. A review of power losses computation methods in low-voltage MOSFETs is presented in [134]. In this section, some sketches on Si devices models will be given. One of the new ideas in several studies, according to the recent literature [38], is that it is necessary to consider the non-linearity of the internal capacitances, in order to obtain more accurate results. In addition, also transfer characteristic must be taken into account for an accurate loss estimation. There exist also various physics-based [28], [44] and behavioral models [29], [30]: they are both simulation-based approaches.

It is important, in general, to compute the conduction losses for the body diode, integrated in Si MOSFETs case. Moreover, losses related to the reverse recovery at the turn off of the diode, due to the discharging phase, should be considered. More specifically, charge, peak current, and

reverse recovery time are important parameters to be accounted for, in this framework, as it will be explained in the following. Usually, in analytical models, switching stages are divided into a number of sub-stages, where analytical formulas are used [58]. A model which considers parasitic inductances due to both the device package and to the PCB layout in presented in [59]. In all these cases, when equivalent circuits are developed, differential equations are solved, in order to get the switching loss quantities.

Models to compute losses in IGBTs are already developed in the past twenty years [54], [56], [144]. In IGBTs, current tail, due to the bipolar nature of the device, results in higher turn-off losses, related to charges recombination. IGBTs may, in the future, be replaced, for some high-power high voltage applications, by SiC MOSFETs, for its higher switching slew rates, that can reduce switching losses; however, these high dv/dt may cause problems for motor reliability and EMI [145]. Therefore, IGBT would still have its market share in this field in next years. A behavioral loss model of an IGBT-based power module used in [149], in order to insert this value in finite-element simulation which, with the aid of a genetic algorithm, can get the optimal thermal placement of the various components. The switching energy is obtained by using a fitting procedure, the following polynomial function:

$$E_{SW} = f(I) = a_1 I^3 + a_2 I^2 + a_3 I + a_4 \tag{4}$$

where I is the load current and a_1, …, a_4 are the fitting coefficients. The switching energies as a function of current can be commonly found in manufacturer's datasheets, as it is showed in Figure 9, for an IGBT from STMicroelectronics [150].

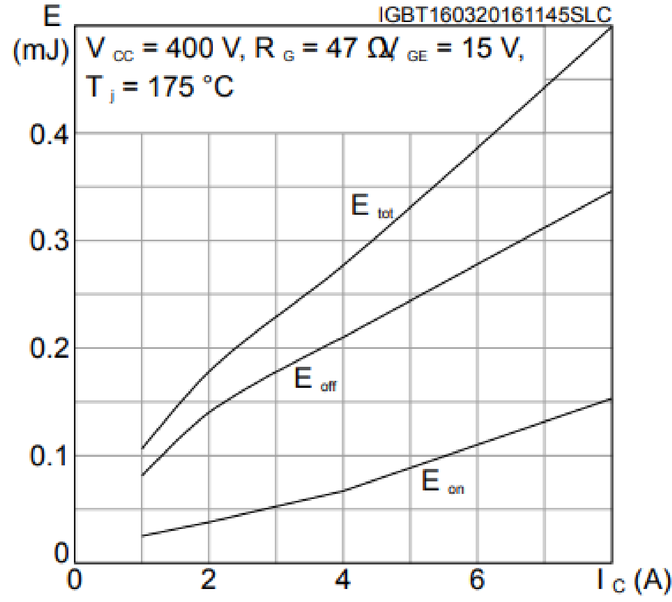


Figure 9. Dependence of on- and off-switching energies in an IGBT by STMicroelectronics manufacturer. From [150]

The switching energy E_{SW} at varying bus voltage, which usually is not present in datasheets, would be obtained by using an appropriate scaling, such as the following [149]:

$$E_{SW} = E_{SE,dc} \frac{V_{dc}}{V_{base}} \tag{5}$$

where E_{dc} is the datasheet energy, obtained at V_{base}, while V_{dc} is the new voltage point to be considered.

An innovative model, which comprises capacitive nonlinearities and displacement current for high voltage SJ MOSFETs to calculate the losses, is proposed in [64], showing that gate resistance should not be too large to not have too switching losses. [64] takes into account also the channel current behaviour, which is also modelled for WBG devices. The capacitive non-linear characteristics for a Si MOSFETs, by

STMicroelectronics datasheet for this product [153], are reported in Figure 10.

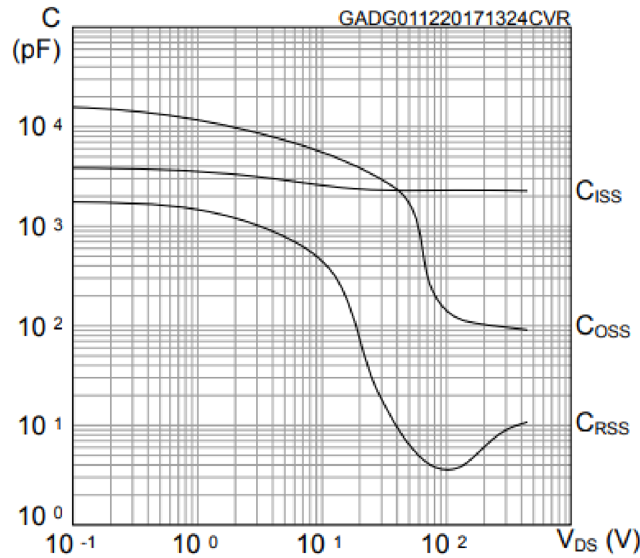


Figure 10. Internal capacitance variations (Ciss, Coss, and Crss), as a function of VDS, of a SJ MOSFET (by STMicroelectronis). From [153]

Another quantity that can be found in datasheet from manufacturers is the normalized on-state resistance as a function of temperature, showed in Figure 11.

C_{iss} stands for input capacitance, while C_{oss} and C_{rss} are, respectively, the output and the reverse transfer capacitances. These characteristics would be obtained by a fitting procedure [36], to be then used in modelling phase. In Figure 12, a flowchart is proposed for the extraction of parasitic elements, from [64].

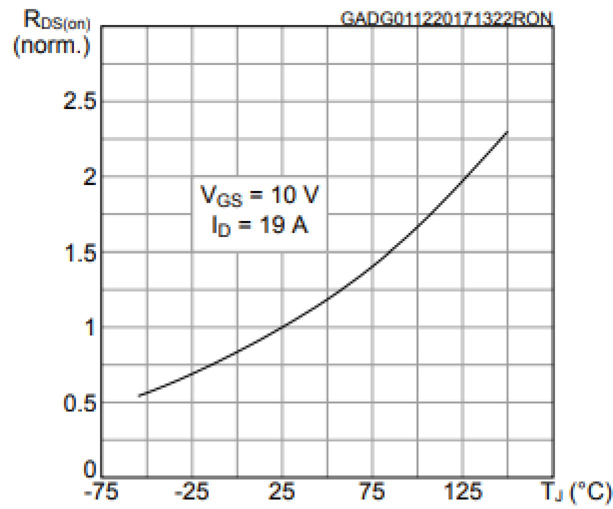


Figure 11. Normalized on-state resistance as a function of temperature, in a SJ MOSFET by STMicroelectronics. From [153]

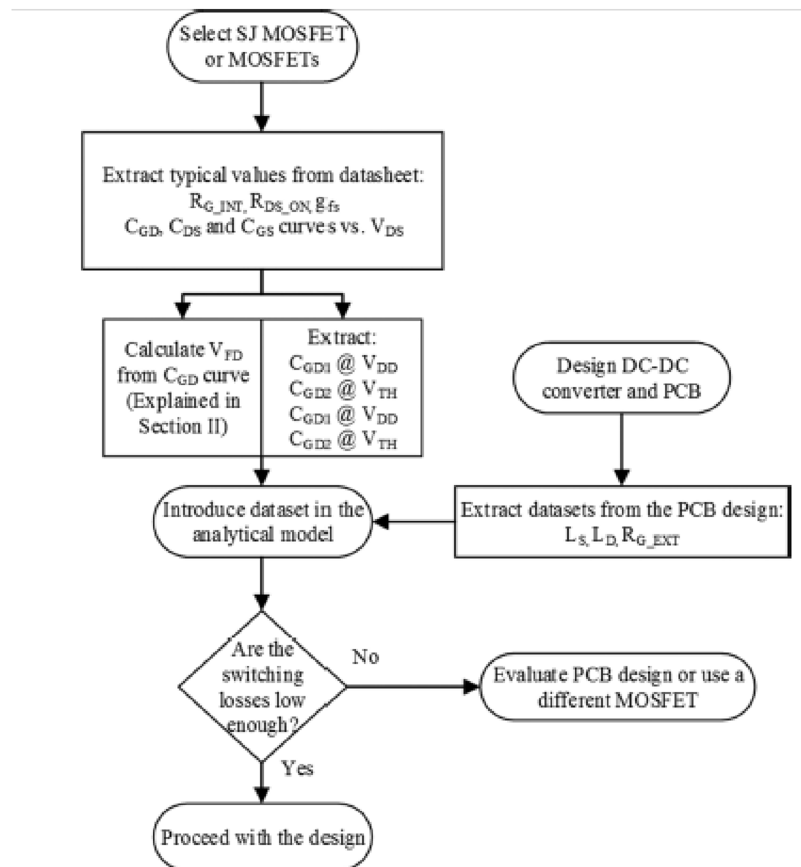


Figure 12. Flowchart regarding the extraction of device quantities, from device datasheet and from PCB, to be inserted in analytical model. From [64]

A more recent MOSFETs switching losses is based on the model developed in [63]. In this way, switching energy can be computed with the datasheet parameters. This is possible by considering the charging and discharging of parasitic MOSFET capacitances: in fact, the charge is related to the energy and, therefore, to the power losses. In general, for all the models outlined in this section, in Si- and WBG-based power devices models, in equivalent-circuit approximations, the electric circuits obtained in the models are solved by means of using the Kirchhoff's voltage and current laws, and the characteristic equations of the capacitor the inductor, in order to obtain the quantities for the power losses calculation. An example of the equivalent circuit approach is depicted in Figure 13.

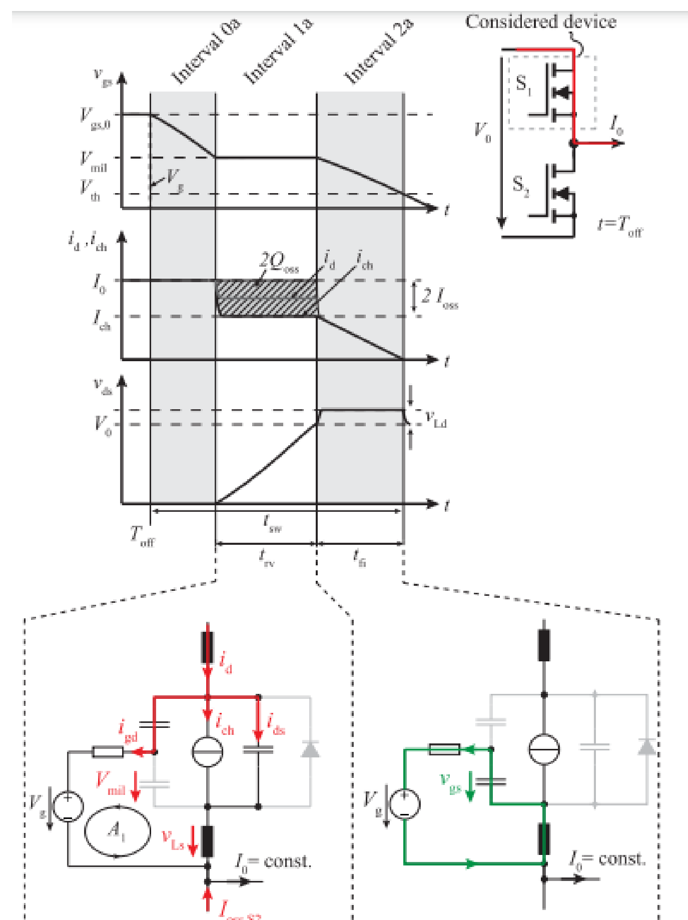


Figure 13. Turn-off phase of the switch S1: linearized characteristics of i_{ch}, v_{gs}, and v_{ds}. From [63]

Turn on, turn off and conduction losses are due to different mechanics. For this reason, in many papers, and also in the following in this chapter, the three stages are treated separately. They are related to different mechanisms involved during the switching phase.

1.3.3. Simplified formulas overview

Some basic formulas for a MOSFET are reported in the following: there are not the only formulas developed in literature, rather can represent a quick comprehensive overview of the different sources of losses [14], [21], [81], [101], [104]. Conduction losses can be expressed by:

$$P_{cond} = R_{DS(on)} \cdot I_D^2(RMS) \tag{6}$$

where $R_{DS(on)}$ is the drain-to-source resistance in on-state and $I_D(RMS)$ is the drain current, root mean square value. Regarding switching losses, there are turn-on losses, related to gate charge:

$$P_{sw,on} = E_{on} \cdot f_{sw} \tag{7}$$

where E_{on} is the switching energy due to on transition, while f_{sw} is the switching frequency.

The turn off losses are given by:

$$P_{sw,off} = E_{off} \cdot f_{sw} \tag{8}$$

where E_{off} is the switching energy in off transition.

Loss formulas, related to diode conduction and reverse recovery are

$$P_{diode,off} = V_f \cdot I_{SD} \cdot f_{sw} \cdot t_{dead\ time} \quad (9)$$

$$P_{diode,cond} = Q_{rr} \cdot V_{in} \cdot f_{sw} \quad (10)$$

where V_F is the diode forward voltage, I_{SD} is the current that flows in the diode, V_{in} is the voltage, $t_{dead\ time}$ is the period in which the diode sustains the current, and Q_{rr} is the reverse recovery charge of the diode.

At the end, also gate driving losses are present, even though they are usually neglected; they are given, in a simplified way, by

$$P_{gate} = Q_g \cdot V_g \cdot f_{sw} \quad (11)$$

where Q_g and V_g the gate charge and voltage of the gate, respectively.

1.3.4. SiC-based models

In this section, a brief outline of the models in WBG devices will be given [132], [135], [138], [142]. For same aspects, the features explained in the previous section, remain valid, as the fundamental switching mechanisms are the same of that of the Si MOSFETs. Regarding the SiC MOSFETs, a loss model for turn on transition considering dynamic behavior for SiC MOSFETs, by accounting for the transfer characteristic and the gate drain charge Q_{gd}, is developed in [74]. In that paper, short-channel effect is also considered. More specifically, the period considered is during turn on, and going beyond the datasheet data.

Among the analytical models developed for SiC devices, one relies on finite state machine in [71], considering both C-V and I-V characteristics. In [84], an analytical methodology based on the conservation of energy, taking into account the displacement currents, is presented for MOSFETs and Schottky barrier diode pairs made by SiC. As can be noted from the below data and graphs (Figures 14 and 15), the model is developed both for turn-on and turn-off transients. It has been assumed that the variations of V_{ds} and I_d quantities are both linear in each stage, thereby excluding the use of state equations or numerical simulations but preserving good accuracy. Also, the parameters extraction is faced out in the paper, together with some operational conditions.

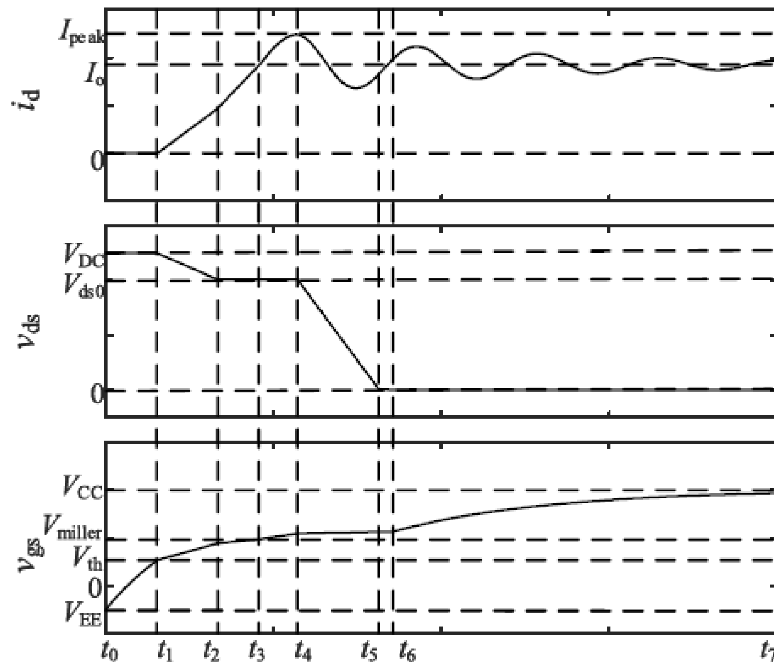


Figure 14. Turn-on transition of a SiC MOSFET: from top to down, drain current, drain-to-source voltage, gate-source voltage. From [84]

In [73], it is proposed an analytical model for SiC module which is semi-physical and semi-behavioral. The second model "part" is introduced because of the most critical transient sub-intervals. More recently, the

authors in [75], [76] have been firstly reviewed the methods to model analytically the turn off and turn-on processed. Then, the authors proposed a new technique considering the transient phase between ohmic and saturation regions, by accounting also the transverse electric field contribution. In Figure 16, a scheme that accounts for device-level and system-level simulations, coupled by power losses estimation, is showed [81].

Stage		Time duration	$E_{loss1(on)}$
Stage 1 (t_0—t_1)		$t_{don} = R_g(C_{gs} + C_{gdL})\ln\left[(V_{CC} - V_{EE})/(V_{CC} - V_{th})\right]$	$I_o\left(V_{D(on)} + I_o R_{D(on)}\right)t_{don}$
Stage 2 (t_1—t_3)	Substage 2.1	$t_2 - t_1 = \left(-B_0 + \sqrt{B_0^2 - 4A_0C_0}\right)/(2A_0)$	$I_o\left(V_{DC}/4 + V_{FD} - V_{drop}/2\right)(t_2 - t_1)$
	Substage 2.2	$t_3 - t_2 = \frac{R_g\left(C_{gs} + C_{gdL}\right)\left(V_{miller} - V_{gs1}\right) + L_s I_o/2}{V_{CC} - V_{gs1}/2 - V_{miller}/2}$	$\left(V_{ds0} - \frac{V_{DC}}{4}\right)I_o(t_3 - t_2)$
Stage 3 (t_3—t_4)		$t_4 - t_3 = \left(-B_1 + \sqrt{B_1^2 - 4A_1C_1}\right)/(2A_1)$	$V_{DC}dQ + I_o V_{ds0}(t_4 - t_3)$
Stage 4 (t_4—t_5)		$t_5 - t_4 = \left(-B_2 + \sqrt{B_2^2 - 4A_2C_2}\right)/(2A_2)$	$V_{DC}I_{os}\frac{\alpha_{on}}{\omega_{on}^2 + \alpha_{on}^2} + I_o\frac{V_{ds0}}{2}(t_5 - t_4) + I_o\frac{V_{miller} - V_{th}}{2}(t_6 - t_4) + I_o V_{ds(on)}\left(\frac{t_6 - t_5}{2} + t_7 - t_6\right)$
Stage 5 (t_5—t_6)		$t_6 - t_5 = R_g C_{gdH}\left(V_{miller} - V_{th} - I_o R_{ds(on)}\right)/\left(V_{CC} - V_{gs2}\right)$	
Stage 6 (t_6—t_7)		$t_7 - t_6 \approx 2R_g\left(C_{gs} + C_{gdH}\right)$	

Figure 15. Example of temporal stages related to Figure 13, with the analytical formulation of time duration and energy loss. From [84]

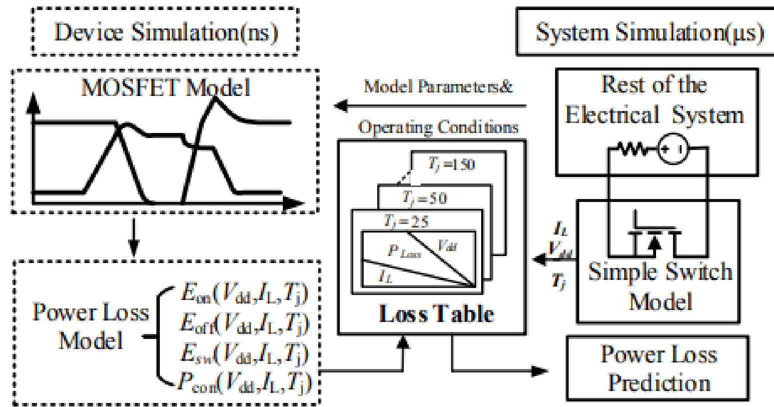


Figure 16. Block scheme of the power loss estimation method proposed in [81]. From [81]

1.3.5. GaN-based models

Now, some sketches on analytical models for GaN-based power devices have given. A comprehensive model of the GaN losses in an inverter is presented in [90], including thermal considerations such as the case temperature estimation and junction temperature with varying losses in a cycle (that have a major impact at high load), capacitor contribution, inclusion of filter, while the inductor is an important factor at light load. Moreover, the parasitic capacitances have included in the inverter model. Loss breakdown il GaN HEMTs is deeply explained in [14], pointing out the differences from the loss types in silicon devices. In that paper, E_{qoss} is distinguished from the E_{oss}, because in this case the charging current is needed to charge C_{oss} capacitor of the opposite switch in the leg of the half bridge [147], in which the voltage is close to zero at the begin. Moreover, GaN HEMTs can conduct currents, even if they do not have body diode, as opposed to Si and SiC MOSFETs: for this reason, there are not reverse recovery losses. GaN-based HEMTs are usually employed for synchronous rectification purposes for this reason. Instead, they do not have a negligible forward voltage in reverse conduction [139].

As GaN devices turn-on switching loss is much higher than turn-off loss, due to the capacitance charging of the freewheeling switch, the zero-voltage turn-on circuit is also favorable for GaN-based converter with high switching frequency, for what already expressed above. There is also an impact of gate resistance and packaging (parasitic inductances) on switching losses [129]. In Figure 17, turn-on and turn-off transitions of a GaN HEMT are showed, highlighting the Q_{COSS} due to freewheeling switching; however, the total amount of switching losses is less than that of Si-based devices.

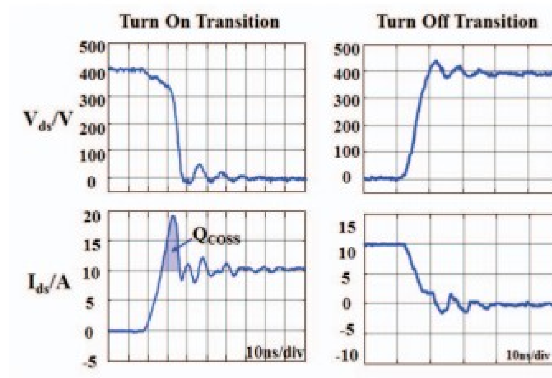


Figure 17. Turn-on and Turn-off voltage and current transients, highlighting the Q_{COSS}, of a GaN HEMT. From [129]

In [36], a model for low-voltage GaN HEMTs switching process is developed for synchronous buck topology, including nonlinear quantities such as junction capacitances and transconductances, and parasitic inductances. Then, a loss method, considering also the reverse conduction loss, is developed. In Figure 18, firstly the circuit topology of buck converter and the associated waveforms are shown, then a circuit model including capacitive (for example, the internal device's capacitances) and inductive (for example, package-related inductances) elements is proposed.

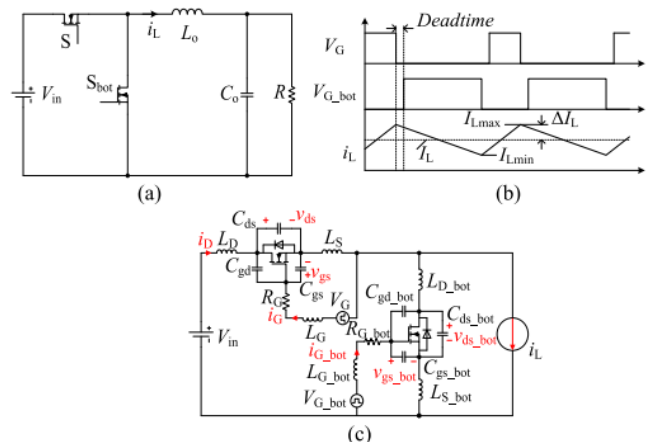


Figure 18. Equivalent circuit of a buck converter employing GaN devices. (a) Topology considered. (b) Waveforms of buck converter. (c) Circuit scheme with lumped elements. From [36]

A comprehensive explanation for GaN HEMTs is presented in [14], resuming the concepts already outlined in this section. In this framework, one of the quantities to be accurately measured and modelled specifically in GaN devices is the dynamic $R_{ds(on)}$ [95], [96], [98], [99]. This quantity depends on various parameters such as blocking voltage (during turn off), current, frequency, off time, and temperature: in [155], an analysis regarding the impact of these parameters, based on literature data, is made. This phenomenon can also bring to power losses increment in conduction phase. In Figure 19, a comparison between dynamic resistance and the static ones, both at case temperature and at room temperature, in soft and hard switching, is depicted.

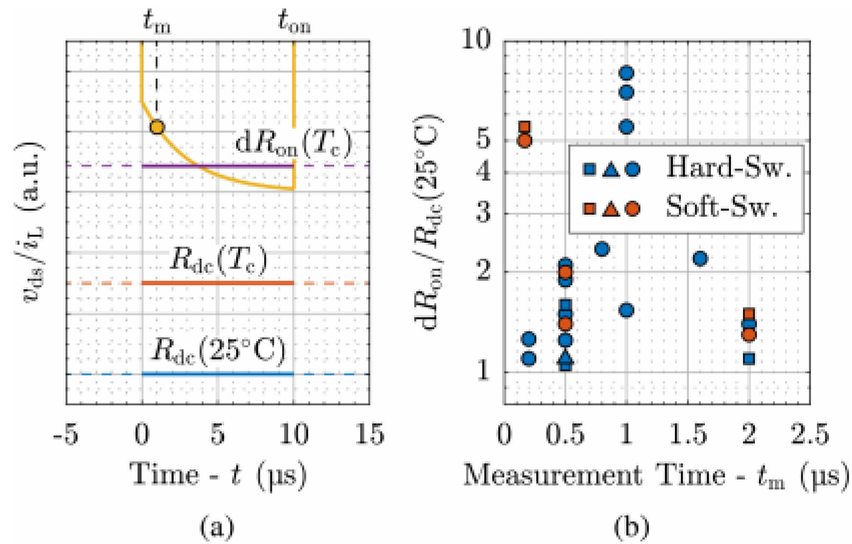


Figure 19. (a) Dynamic Resistance: comparison between dynamic on state resistance and dc resistance. t_m indicates the measurement time after the turn-on process, while t_{on} is the conduction time. (b) Dynamic resistance, normalized to the static one, for commercial GaN HEMTs, in hard and soft switching conditions at 400 V turn-off voltage. The device's manufactures are related with the various marker shapes. From [96]

1.4 Thermal methods: calorimetry and temperature sensor

Calorimetric methods have been already used in various fields, such as electric machines, motors, and drives [40], [126]. Various methods have considered, but several ones require complex measurements devices and environmental conditions. In addition, usually they are more time-consuming in comparison to the electric ones.

In this thesis, those regarding the power devices have considered. Many papers make use of the well-known relationship between temperature and power through the thermal impedance, or the thermal resistance in steady-state conditions. In the latter case, a generic formula of the thermal resistance is given by:

$$\Delta T = R_{th} \cdot P \tag{12}$$

where R_{th} is the steady state thermal resistance, P is the dissipated power, and ΔT is the temperature difference between two points. For example, if thermal resistance between junction to ambient is considered, the temperature difference is between the junction to the ambient, and the power is that of the path between these two system's parts.

In various cases of calorimetric measures, there are two steps: in the first, a system characterization is performed. In the second, the main experiment is executed [112]. The measurements are based on the observation of thermal quantities; thus, they are typically independent from the electric characteristics of the analyzed devices. Calorimetric measurement methods can be divided into two subcategories, i.e., steady-state methods and transient methods. In steady-state methods, the setup is continuously operated until the thermal steady-state is reached and, only then, the occurring losses are determined from the observation of specific

temperature values. Transient methods analyze the thermal dynamics of the system and, at the expense of slightly increased complexity, offer reduced measurement times and comparable accuracies [15]. A straightforward idea may be to measure the air temperature, in order to know firstly the heat exchange in the system and then the total power losses [14].

A common problem in calorimetric methods is that by these techniques it can be possible to estimate, in a good way, the loss of the power device, however it is difficult to separate the switching loss components, i.e. to distinguish between E_{on} and E_{off} [101]. In [108], three methods are developed: method 1, by using heatsink thermal resistance, method 2, by considering heatsink air flow temperature difference, and method 3, with the air enthalpy increase. These methods can be applied by using a full bridge scheme, as the one showed in the Figure 20. Switching power ratio, defined as following,

$$SW_{ratio} = \frac{P_{sw}}{P_{sw} + P_{cond}} \tag{13}$$

can be improved by employing a full bridge topology (in particular, and using an appropriate duty ratio, with lower devices in both legs carrying the freewheeling currents), thereby reducing the conduction losses in the DUT, i.e. one switch of the bridge. DUT is represented in Figure 20, which reports the full bridge topology.

In this way, a pretty accurate measure of the switching losses can be made, but, as outlined above, some factors must be taken into account [109]: calorimetric setup must be carefully design, switching ratio must have an high value, and of course, as a necessary condition, it must be present a system that can measure accurately the switch conduction losses.

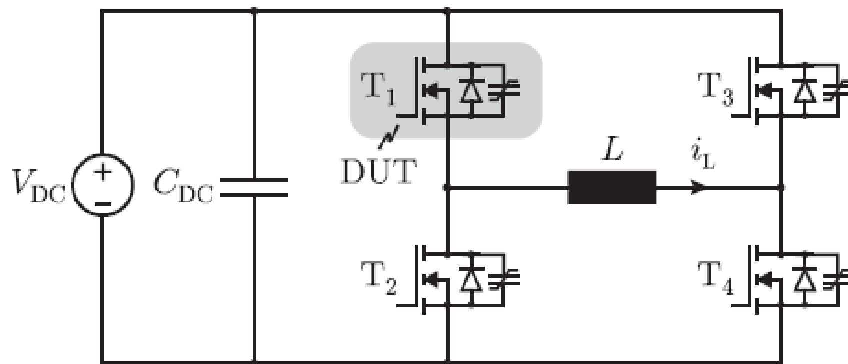


Figure 20. Full bridge used for the calorimetric measurement, with T1 as DUT. From [108]

In [103], a calorimetric test setup is described (Figure 21 (a)). In Figure 21 (b), the modified half-bridge circuit used as a topology is depicted, which has an additional switch contained in the calorimeter, in series with the top switch.

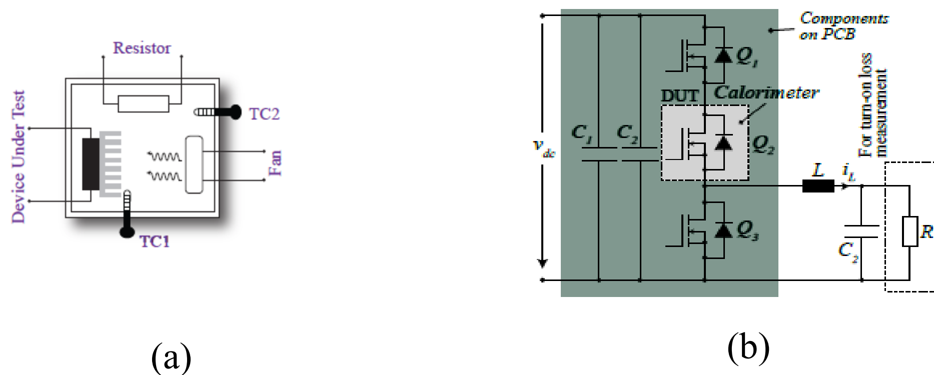


Figure 21. Calorimetric measurement experimental scheme: (a) Calorimeter schematic, comprising the calibration resistor, the fan, the DUT, and the thermocouples; (b) Equivalent circuit of the experimental setup presented in [103]. From [103]

A novel modulation scheme is introduced which enables the segregation of the individual losses, that is one of the most critical issues in calorimetry, as it can be seen in Figure 22.

More specifically, it can be possible to write:

$$P_{calo} = \frac{T_{cal} - T_{amb}}{R_{TH-cal}} \quad (14)$$

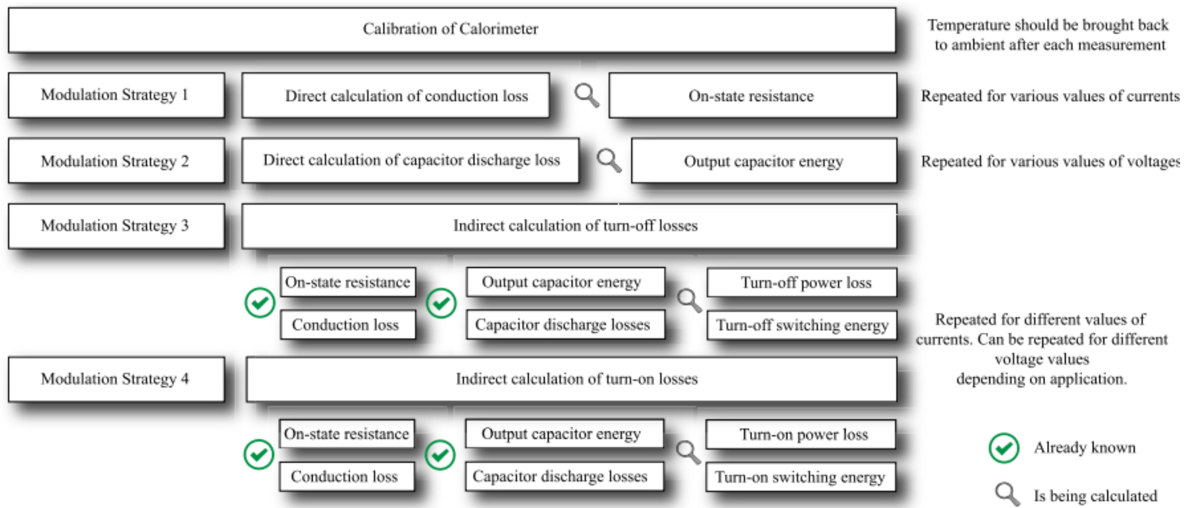


Figure 22. An example of a flowchart to separate the power losses, by employing various modulation strategies. From [103]

Calorimetric methods mainly measure losses in continuous conduction. There are problems related to the C_{oss} measure in soft switching, while in hard switching case the non-correct estimation of turn-on switching energy is balanced by the turn off one. The modified half-bridge configuration comprises the DUT inserted in series with one of the devices in a half-bridge topology.

Now, a brief outline of temperature measurements method will be given. First of all, in Figure 23, it is represented the power device soldered on PCB and attached to a heatsink, as in real-world applications; moreover, the main heat paths are represented, also with a schematic of the thermal resistance and lumped-equivalent circuit.

In the following, four common methods, found in scientific literature, and reported in [106], are listed: flow density measurement, the temperature equivalent measurement, that needs to design a temperature insulation box with good isolation performance, the double jacket test, and temperature sensor measurement methods [104]. In the last case, only two thermocouples were especially necessary in this measurement, so it was easy to be applied. The loss measurement includes two parts, as in [112]: calibration experiments and main experiments. The experimental measure relies on two thermocouple temperatures in a copper block, more specifically in the upper and lower surfaces. In this case, a simple model, illustrated in Figure 23, is necessary.

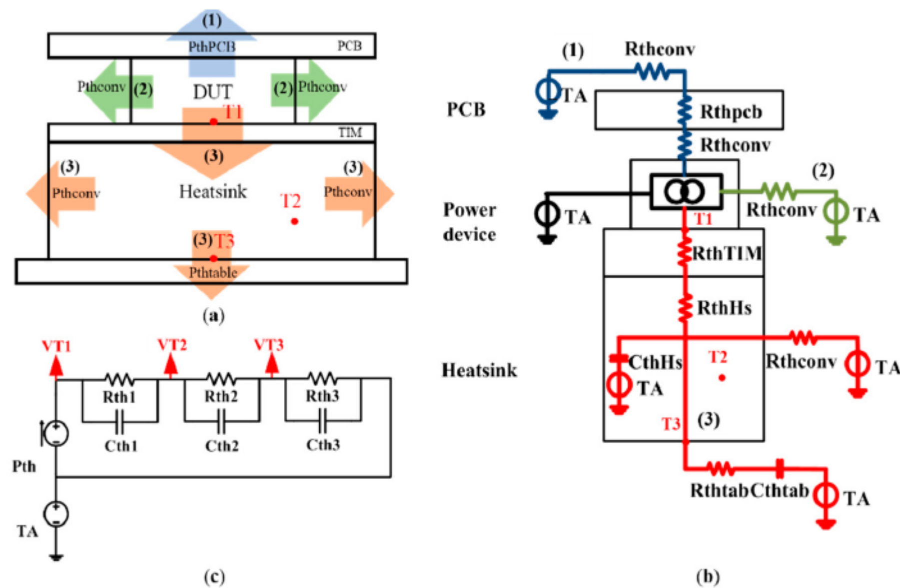


Figure 23. (a) Power device, which is the DUT, is soldered on a PCB on one side, while from the other side, a heatsink is attached, by means of a Thermal Interface Material (TIM). The main heat path is related to the heatsink, which has a high thermal conductivity. (b) Thermal model, related to the various paths and heat transfer modes. (c) Lumped equivalent circuit model, including heatsink. From [106]

Now, the method presented in [111], [112] is recalled. In the first, there is a calibration phase. With a known DC input and with a temperature measure, it is possible to compute the thermal resistance by means of the relation reported in the figure. In the second, the power losses are computed, with the same relation and known thermal resistance value. In Figure 24, it is showed graphically this two-step procedure that makes use of the simplest formula. Obviously, the operating experimental conditions, between calibration and measurement, like fan velocity or DUT and equipment position, must be as close as possible.

In the following basic formula [107], it is recalled the basic principle of losses measurements with a calorimeter:

$$P = \frac{C_{Th}\, \Delta\vartheta}{\Delta\tau}\ , \tag{15}$$

where C_{th} is the system's thermal capacitance, $\Delta\vartheta$ and $\Delta\tau$ are, respectively, the temperature difference and the measurement time.

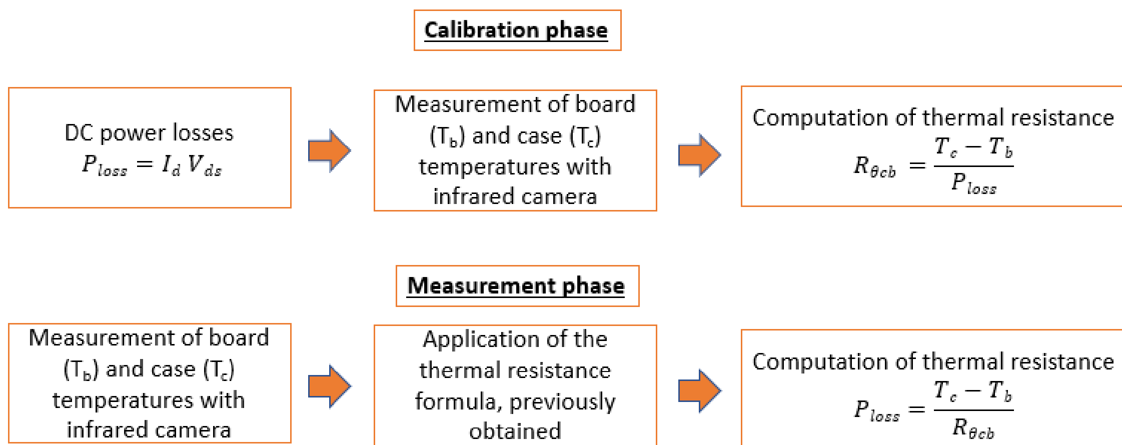


Figure 24. Thermal loss method, valid for any device. Calibration and measurement phases are graphically depicted. Adapted from [110]

An innovative and more simper procedure is developed in [15]. This method is based on the analysis the heatsink temperature rise, and on a thermal model in which the parameters should be identified by means of a fitting procedure (Figure 25). But several (up to twenty) minutes are necessary to characterize a single operating point. Hence, a new procedure is proposed in that paper, that is an "ultra-fast transient calorimetric measurement method", which relies on the case temperature method. In this way, the transient behaviour of case temperature is characterized, and a shorter thermal time constant can be used. The temperature, in both methods, is obtained by resolving a circuit with thermal resistances and capacitances, as depicted in Figures 25 and 26 [15]. The formulas used are here recalled:

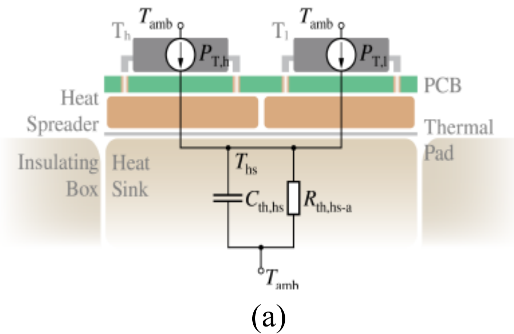
$$\begin{bmatrix} \dot{T}_{c,h} \\ \dot{T}_{c,l} \end{bmatrix} = \begin{bmatrix} -\frac{R_{th,h}+R_{th,m}}{C_{th,h}\,R_{th,h}\,R_{th,m}} & \frac{1}{C_{th,h}\,R_{th,m}} \\ \frac{1}{C_{th,l}\,R_{th,m}} & -\frac{R_{th,l}+R_{th,m}}{C_{th,l}\,R_{th,l}\,R_{th,m}} \end{bmatrix} \begin{bmatrix} T_{c,h} \\ T_{c,l} \end{bmatrix} + \begin{bmatrix} \frac{P_{T,h}}{C_{th,h}} \\ \frac{P_{T,l}}{C_{th,l}} \end{bmatrix}, \quad (16)$$

$$\dot{T}_{hs} = -\frac{P_{T,h}+P_{T,l}}{C_{th,hs}}, \quad (17)$$

where P_{Th} and P_{Tl} are the power losses of the high and low switches, respectively, while $T_{c,h}$ and $T_{c,l}$, $R_{th,h}$ and $R_{th,l}$, and $C_{th,h}$ and $C_{th,l}$ are the case temperatures, thermal resistances, and the thermal capacitances of the high and low switches, respectively.

Moreover, no customized heatsink is mandatory. In a half bridge topology, the power losses in the two switches can be measured separately, because the two case temperatures are considered. In that paper, it is also pointed out that a high frame rate and resolution infrared camera should be

used, in order to maintain a good accuracy. The novel method is graphically reported in Figure 26.



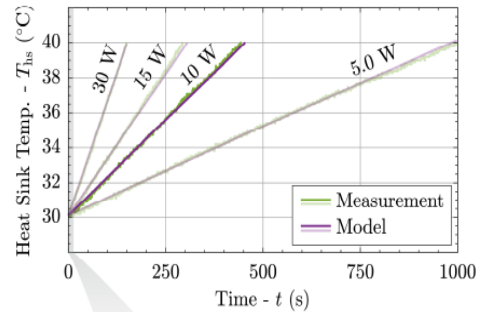
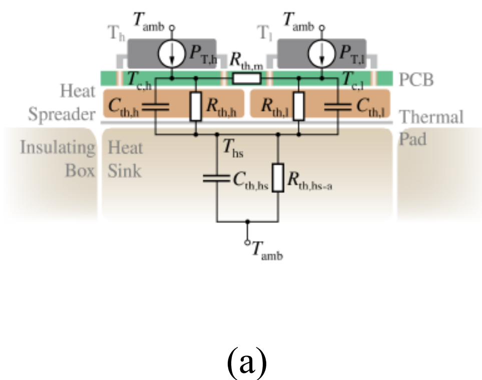
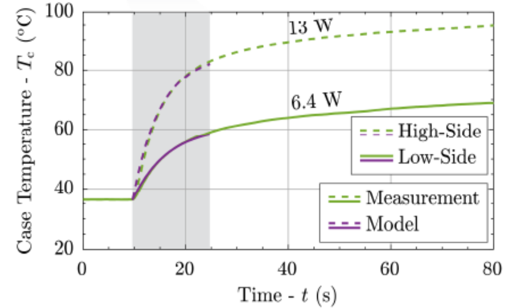


Figure 25 (a)**:** Heatsink temperature rise-based method. Electrical equivalent circuit. From [15]

Figure 25 (b)**:** Heatsink temperature rise-based method. Time versus heatsink temperature. From [15]





(a) (b)

Figure 26. Case temperature-based rise method: (a) Equivalent electric circuit; (b) Time versus case temperature. From [15]

To conclude this paragraph, in recent years a method based on infrared thermal imaging has been proposed to obtain the losses at the die level, by removing the device package's resin. The test bench was a resonant inverter [141].

1.5. Comparison among the methods and open problems

Comparisons among loss measurement or estimation methods have been presented in some papers, based on certain parameters such as accuracy, speed, cost, and so on [106], [108], [110]. In this review, the comparison among the electrical, analytical, and thermal models, is made by means of the mathematical formulation used, both in analytical, mixed, and experimental methods. The comparison is based on the comparisons aforementioned and on the papers accessed in this chapter. In Table 1, the comparison is presented.

In many papers found in literature, as it has been outlined in the previous sections, many analytical models have been proposed. However, usually to validate the model a comparison with a DPT is made, but this can be misleading, as these methods can bring to results far from reality. In Table 2, the issues which are still a hot research topic for the determination of the converter's efficiency, have been listed. There are many papers that treat the topics related to dynamic on-state resistance in GaN-based devices, calorimetric methods in comparison with electric ones, output capacitance contribution to power losses, parasitic elements computations, and non-linearity inherent in power devices. Coupled with the issues, some selected references have been inserted.

Table 1. Comparison among the literature methods.

Parameters	Thermal-Calorimetric	Analytical/Behav.	Electrical
Accuracy	High	It depends on the model	Low
Speed	Medium-slow	Fast-medium	Fast
Cost	Medium-High	Low	Medium
Complexity	High	It depends on the model	Medium

Table 2. Open issues related to power losses estimation and some useful references.

Open issues	Selected References
Dynamic R_{dson}	[95], [96], [99], [131], [154]
Very fast slew rates – parasitic elements	[26], [44]-[30], [32], [33]
Output capacitance	[140], [148], [151]
Electrical vs. calorimetric	[103], [107], [108], [111], [15]
Non-linearity	[63], [65], [67]

In Figures 27 and 28, diagrams summarizing the power losses estimation methods, and modeling and simulation-related techniques, respectively.

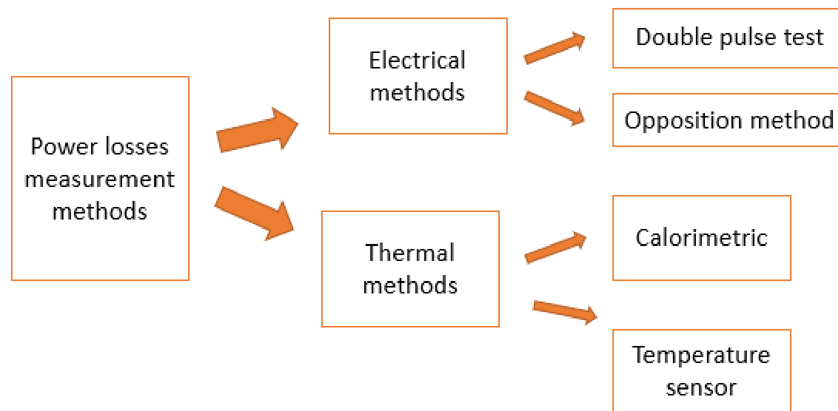


Figure 27. Summarizing diagram reporting the power losses estimation method techniques.

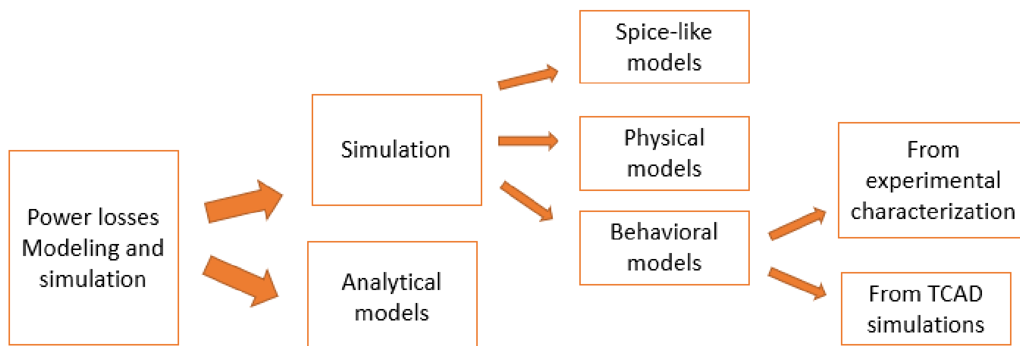


Figure 28. Summarizing diagram on power losses modeling and simulation estimation techniques.

1.6 Conclusions

A review on power losses methods has been executed. Both electrical and thermal measurements, analytical and experimental methods, silicon and wide band-gap (SiC and GaN) devices, have been considered, including issues and advantages for each method. Therefore, in this chapter a comprehensive overview of all these frameworks, power devices materials, and important aspects has been done. Moreover, a comparison has been presented, as well as a summary of the hot topics regarding the losses estimation methods, such as dynamic on state resistance, soft-switching techniques, calorimetric methods, and the problem of high voltage and current slew rates in relation to traditional double pulse tests. The importance of models to compute power losses also in design stages, regardless the particular topology and modulation used, has been focused, highlighting thermal and reliability [152] issues related to the converter's efficiency.

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PART II: SIC POWER MODULES FOR TRACTION INVERTERS

2. SIC POWER MODULES FOR TRACTION INVERTERS IN AUTOMOTIVE APPLICATIONS

This chapter has been taken (with some modifications) from the following published paper:

- **G. Mauromicale**, A. Raciti, S.A. Rizzo, G. Susinni, L. Abbatelli, S. Buonomo, V. Giuffrida, "SiC Power Modules for Traction Inverters in Automotive Applications," *45th Annual Conference of the IEEE Industrial Electronics Society (IECON)*, Lisbon, Oct. 14-17, 2019

Nowadays, there is a great research effort in the field of electric vehicles. In such a context, SiC power modules play a key role for their effective and widespread diffusion especially due to their ability at improving the performance of the traction inverter. The advantages and issues related to SiC traction modules are analyzed in this work giving also guidelines for viable solutions. More specifically, electrical and thermal problems, safety and reliability issues, challenges from device paralleling and module layout as well as power efficiency, have been investigated. The aim of this work is to collect all these aspects that must be carefully considered at the SiC power modules design stage. The main merit of this overview is their analysis performed by means of on field experience, in terms of experimental tests, finite element analysis, and circuit simulations.

2.1 Introduction

In the last decades, the problems arising from the pollutant emissions in transportations are becoming more and more important [1]. In this context,

Electric Vehicles (EVs) are acquiring an important role because they can mitigate this issue [2][3][4]. EVs can be grouped in several categories, with respect to the presence of electrical components and converters used in the car: mild hybrid and hybrid [5][6], solar hybrid [7], plug-in [8] and battery EVs [9].

Wide band-gap (WBG) materials such as Silicon Carbide (SiC) [10] and Gallium Nitride (GaN) [11] may give a boost for their diffusion [12]. WBG materials have superior electrical and thermal characteristics compared with the Silicon (Si) ones [13]. Thanks to their good feature, SiC MOSFETs have smaller power losses in comparison with Si IGBTs. The power losses may be subdivided into conduction losses and switching losses, as already outlined in previous chapter regarding the power losses types. The first represent around the 80% of the total losses in traction inverter applications. Notwithstanding, SiC MOSFETs have a very small on resistance and this parameter has, in some cases, a weak increment when the temperature increases making them more efficient than Si IGBTs. Moreover, the efficiency of SiC-based converter is higher than that of the IGBT-based ones at light load, which is the most frequent working condition for the electric motor [14]. Further advantages are the ability of SiC MOSFETs to operate at higher junction temperature [15], up to around 200 °C, and the absence of the external freewheeling diode, which is instead fundamental in IGBT applications. In fact, SiC MOSFETs exploit the good properties of their body diode, thus SiC modules occupy a smaller area for dies than Si ones. In automotive applications these features are very important [16]. On the other hand, SiC modules present more EMI and crosstalk issues [17]. Moreover, the application of active Miller clamp is suitable in SiC based applications, in order to mitigate transient gate-source positive and negative overvoltages.

Very high power is often required in automotive applications due to accelerations that involve a peak power about double in comparison with the nominal one. Furthermore, such a power has to be delivered in few seconds. Therefore, the power modules must withstand these stressful transients. SiC based power modules are able to cope with these requirements. An example of SiC based power module design for traction applications is given in [18], along with its finite element electrical and thermal characterization. Another design of a full-SiC module is presented in [19], accomplished by an experimental comparison between the SiC based solution and the IGBT based one, highlighting power density and efficiency good features.

This chapter is organized as follow: in Section 2.2, electro-thermal issues are discussed. In Section 2.3 problems related to paralleling SiC MOSFETs are outlined, while in Section 2.4 reliability topics such as short circuit and unclamped inductive switching are dealt with. Finally, in Section 2.5 issued related to layout are analysed, and in Section 2.6 the conclusions are drawn.

2.2 Electro-thermal issues

The problem of heat dissipation is of crucial importance when dealing with automotive applications. Obviously, the devices junction temperature should be kept under its maximum acceptable value. If this condition is not respected, then thermal runaway phenomena could happen. For instance, in discrete devices only self-heating phenomenon must be considered [20]. In addition to self-heating, also cross-heating effects have to be taken into account when we consider the case of power modules, in order to model the mutual influences among close dice [21][22].

With reference to the electrical issues, in fact, it is important to consider the power losses, both in conduction and switching operations, as it has already discussed in previous chapter. They are connected both to the heat generation and to system efficiency [23]. Moreover, current and voltage values during stress conditions (unclamped inductive switching, short circuit, and so on) must be carefully handled.

Circuit simulations and finite element analysis (FEA), especially multi-physics ones, are useful in application development considering a given mission profile. FEA enables the modeling of thermal and electromagnetic behaviors of the SiC power module. The multi-physics tools evaluate the electro-thermo-mechanical behavior of the converters enabling lifetime estimations. FEA simulations for evaluating the thermal fatigue could also be carried out. By means of FEA, it can be computed the temperature distribution field of the simulated structure, so that the hotspots or the cooler zones can be identified. However, other methods can bring to the estimation of the temperature in a module. For instance, in [24] the temperature field within a power electronics module is obtained by using the Fourier series. The method is then compared with FEA simulations and experimental tests to show its effectiveness.

Another method, suitable for the computation of the junction temperature of discrete devices and modules, is the use of electrical networks modelling the thermal impedance. Foster or Cauer equivalent electrical networks are commonly used to evaluate the junction temperature of power devices or modules. These networks are constituted by elementary Cauer or Foster cells, where a cell is an elementary RC circuit. The thermal capacitance must be considered only during the thermal transient. Instead, the use of thermal resistance is sufficient for studying the

steady-state condition. The following formula is used for the computation of the junction temperature [25]:

$$T_j(t) = Z_{th(j-f)}(t)\,[P_{sw}(t) + P_{cond}(t)] + T_{heatsink} \quad (1)$$

where $P_{sw}(t)$ and $P_{cond}(t)$ are the switching and the conduction power losses, respectively, and $Z_{th(j-f)}$ is the junction-fluid thermal impedance. It can be computed by the following analytic expression:

$$Z_{th(j-f)}(t) = \sum_{i=1}^{n} R_i\,(1 - e^{-\frac{t}{\tau_i}}) \quad (2)$$

where n is the model order, $\tau_i = R_i \cdot C_i$ is the time constant of an elementary circuit, while R and C are the parameters of the network.

From electrical issues point of view, in [26] a study comparing two SiC based power modules has been performed. An optimized module with PCB embedded die technology has been introduced by the authors and compared with a standard one having wire bonds and direct bond ceramic substrate. The results, with respect to switching features and electromagnetic inferences, show a better behavior for the novel module. In [27], a comparison among various modules with different characteristics has been performed. Thus, it has been pointed out that SiC module improves efficiency and total harmonic distortion but worsens the electromagnetic emission.

We carried out some simulations for different SiC modules that are discussed in the following. The first module considered is STA5 R&D full-SiC package, representative of a conventional plastic module solution. It is used to perform a thermal evaluation. The structure of the model used for

fluid dynamics analysis is reported in Fig. 1. The system comprises a heat-sink for cooling of SiC devices mounted in the module. Thermal energy is transferred by conduction in the solid materials (devices, DBC, heat-sink), while both conduction and convection are responsible for the transfer in the fluid. The cooling system taken into account is a rectangular box. A water/glycol solution flows inside the box at the inlet and it exits at the outlet. The ambient temperature is fixed at all the boundaries and a constant flow is fixed for each step of the simulation. The flow-rate has been evaluated in the range 1-12 l/min. The boundary conditions are of insulation for all outer surfaces, except those of the inlet and outlet boundaries.

Fig. 1. Simulated module structure.

Once that the simulation setup is fixed, the simulations to obtain the temperature distribution are performed. In Fig. 2, thermal maps of the top view and the baseplate surface are depicted, with the velocity of the flow set to 10 l/min. Looking at the temperature distribution, it can be noted that the devices near the inlet of the fluid are the coolest ones.

This tool can help in choosing the ideal switches position to minimize mutual influences in terms of cross-heating. The final aim is to estimate the $Z_{th(j-f)}$, knowing the power applied to the structure, the fluid temperature, and the junction temperature of the warmer dice.

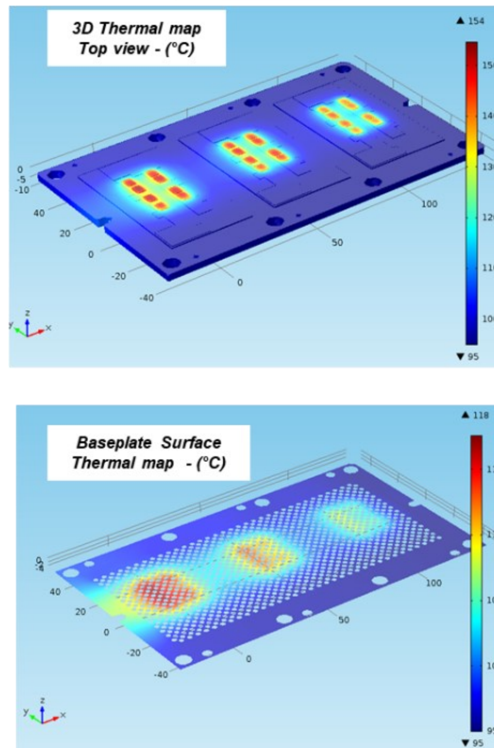

Fig. 2. 3D Thermal maps – Top view and baseplate surface of the STA5 package.

Other simulations have been carried out by using proprietary package tool (STMicroelectronics, ST PowerStudio) [25]. In detail, an engineering sample (internal version) has been developed, to deal with SiC power modules used in automotive applications. The tool allows the computation of the junction temperature, the conduction and switching losses of the device and the body diode, in a module with certain characteristics. ST PowerStudio imports electrical and thermal data, acquired by means of experimental tests (dynamic characterization) and simulations. Then, these data are modelled through polynomial fitting procedures. Finally, power losses and temperature evaluations are performed using a dedicated model. The computation strategy also considers the self-heating effect. Finally, the tool computes the average junction temperature and the temperature ripple [25]. Figs. 3-5 show the simulation setup and results obtained in a real-world case study on an EV using a module developed by

STMicroelectronics. More in detail, it is a 1200 V and typical 3.5 $m\Omega$ SiC module named ACEPACK^{TM} DRIVE. In particular, in this module each switch comprises eight dice in parallel. Fig. 3 depicts a screen shot of the input data, while Fig. 4 depicts a screen shot of the output data. The input data are referred to custom technical specifications, particularly to the inverter peak power condition

Input Data

	Limits	
t_sim: Simulation time (s)	0.001 ÷ 30	3.000
Iph: RMS Phase Current (A)	0.01 ÷ 600	340.00
Pout: Output Power (W)	0.1 ÷ 20000	219259.6
Vdc: DC Link Voltage (V)	20 ÷ 960	800.0
fsw: Switching Frequency (kHz)	1 ÷ 40	8
fsine: Output Frequency (Hz)	0.1 ÷ 500	250.00
PF: Power Factor	0.1 ÷ 1	0.8
MI: Modulation Index	0.01 ÷ 1	0.95
Tflu: Fluid Temperature (°C)	25 ÷ 100	50
Ths: Heatsink Temperature (°C)	25 ÷ 125	65.0
Vgs OFF: Vgs OFF Voltage (V)	-5 ÷ -1	-5

Rg (Ω) 1.2 ÷ 9
ON/OFF 3.3 3.3

Fig. 3. Screen shot of the input data.

Output Data

	T1	D1
Conduction Loss (avg) (W)	433.06	91.61
Switching Loss (avg) (W)	123.30	35.01
Total Loss (avg) (W)	556.37	126.63
Junction Temp. (Max) (°C)	168.24	168.24
Junction Temp. (avg) (°C)	151.44	151.44
T1+D1 Total Loss (avg) (W)	682.99	
System Total Loss (avg) (W)	4097.96	
Heatsink Temperature (Max)	65.00	
Heatsink+TIM Rth (°C/W)	0.0037	

Fig. 4. Screen shot of the output data.

. In Fig. 5 (a), the variation of the junction temperature is depicted. In Fig. 5 (b), a zoomed view at steady-state is shown, that is the swing of the temperature according to the motor frequency, is performed. The average

junction temperature is about 150 °C and remains under the amplitude of the maximum rating (with a further margin), thus permitting the limits to be respected. In conclusion, with this tool it is possible to understand if a designed module, for example with a certain number of paralleled dice, can work in specific conditions.

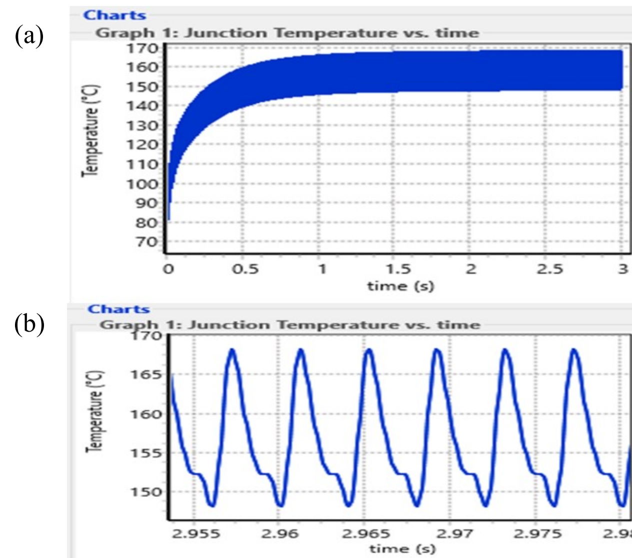

Fig. 5. (a) Junction temperature variation as a function of the time (b) zoomed view of the steady-state junction temperature.

2.3 Unbalance Problems From Paralleled Dice

The need of high power in EVs involves the use in the modules of several SiC MOSFETs connected in parallel, which can bring some issues [28]. More specifically, from many points of view (reliability, lifetime, efficiency, and so on) it is high desirable that all these devices work in the same conditions, during normal operation as well as when stressful conditions occur. On the other hand, such a desirable condition is very difficult to be reached due to many reasons that must be carefully considered. Production spreads on drain-source on state resistance $R_{DS(on)}$ and gate threshold voltage V_{th} are two important factors to be considered,

when looking at the device parameters. Also mismatches on the gate driver, printed board circuit (PCB) layout or on the power circuit have to be taken in consideration. Indeed, a combination of these phenomena determines the global behavior of paralleled devices [29], [30]. Current imbalances due to different features among the dice may cause thermal issues and may worsen the short circuit robustness of discrete devices or modules.

When dealing with paralleled dice, reliability analyses are related to different thermal transients. Three kinds of steps of transient thermal analysis can be defined with the aim of studying thermal jumps on each device. The first one is fast transient thermal analysis (~ 100 μs), because of the switching at die level. The second analysis relies on medium thermal transient time (~4 ms), as a consequence of the sinusoidal signal. The third possible analysis is the slow thermal transient (~5$\pm$10 s), connected to the thermal impedance of the whole system. Circuit models and simulations are useful in defining the proper set-up for parallel operations. In [30], [31], a statistical analysis of on resistance and threshold voltage parameters fluctuations on paralleled SiC MOSFETs is performed by using a SPICE model. The investigation is accomplished by fitting the model with experimental data. Then, electro-thermal Monte Carlo SPICE simulations are done, showing the impact of the aforementioned parameters on energies and currents in parallel operation. When several devices are placed in parallel, the wasted energy during turn-off, E_{off}, is greater than the expected value obtained by summing the energies of the single switch [29].

We carried out some simulations, by using a self-heating model, to obtain results for a two SiC dice module by means of a SPICE software. The temperature behavior is simulated for three cases. The common test conditions are: bus voltage equal to 400 V, current 200 A, switching frequency 10 kHz and $T_{heatsink} = 50°\text{C}$. Three possible cases have been

investigated. Each case is referred to the high or low side of one of the three legs. In detail, a device with typical $R_{DS(on)}$ and V_{th}, a device with both maximum $R_{DS(on)}$ and V_{th}, or a device with both minimum $R_{DS(on)}$ and V_{th} have been considered. More specifically, a typical $R_{DS(on)}$ is $20\ m\Omega$ (at 25 °C, $V_{GS} = 18V$) while minimum and maximum values can be included, in the whole temperature range, in an interval spanning from $\pm 35\%$ (at ambient temperature) to $\pm 15\%$ (at high temperature). Instead, the typical threshold voltage is $V_{th} = 3.1\ V$ (at 25 °C and with a current equal to 1 mA), while maximum and minimum values can be in a range of $\pm 400\ mV$ in comparison with the typical one.

In the first case, a die with $R_{DS(on)}$ and V_{th} at maximum value and the other die with minimum $R_{DS(on)}$ and V_{th} have been simulated. In the second one, both dice present typical $R_{DS(on)}$and V_{th}, while in the third case have both maximum $R_{DS(on)}$ and V_{th}. In Fig. 6, the junction temperature variation for the three cases under test are shown. Regarding the first case, the temperature depicted is the maximum one between the paralleled dice. It is worth to note that different $R_{DS(on)}$ values between the paralleled dice cause power conduction losses, while the switching ones are affected primarily by V_{th}, but also by $R_{DS(on)}$, because of the higher turn-on and turn-off current.

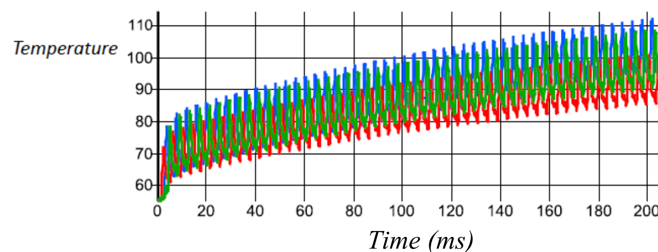

Fig. 6. Junction temperature variation (°C) for the three cases.
Blue curve: first case. Red curve: second case. Green curve: third case.

Now, we focus on the worst case in terms of spread, and consequently of unbalance, that is the first one. As it can be seen in Fig. 7, there is a large current imbalance between the two paralleled dice. In this case, we are in medium thermal transient.

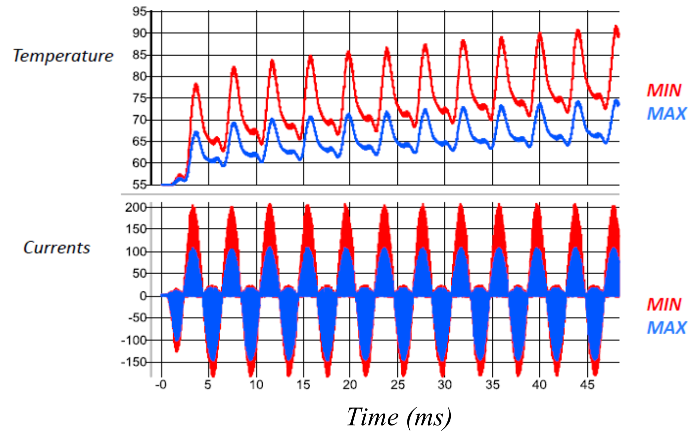

Fig. 7. Temperature (°C) and currents (A) of the paralleled devices, case 1. Red curve: minimum $R_{DS(on)}$ and V_{th}. Blue curve: maximum $R_{DS(on)}$ and V_{th}.

In this framework, simulations with a predefined range of productive spread are useful. More specifically, the selection of devices with similar parameters (maximum difference chosen a priori) is important to reduce thermal jumps, which may be dangerous from the reliability point of view. For example, it may be useful a selection on $R_{DS(on)}$. In such a way, an appropriate choice enables the reduction of unbalance and, consequently, the temperature is kept under the maximum permissible value.

In order to mitigate the problems arising from device paralleling, another solution may be the adoption of integrated gate resistor. The related benefits are the compactness of the overall solution, and the decrease of the switching losses unbalance due to different threshold voltages of paralleled devices. On the other hand, integrated gate resistor requires a greater chip

size and a further gate pad for active Miller clamp. Moreover, this solution has a high process spread, which in turn worsens the switching losses.

2.4 Reliability issues: UIS and short-circuit

In the framework of the reliability, in this paragraph are treated two issues: unclamped inductive switching (UIS) and short-circuit (SC) [32][33]. UIS operation frequently occurs in automotive applications due to energy release from inductive loads, such as motors and actuator controlled solenoids, to the fuel injector coil circuit, and antilock braking module [34][35]. Normally, UIS is performed without the presence of freewheeling diode for the recirculation of the current. Hence, the energy accumulated in the inductor is reversed in the power switch at turn-off leading to overvoltage [36]. This phenomenon, as well as a SC event, may lead the MOSFET in breakdown or avalanche operation. During UIS, significant parameters are the avalanche energy and the current through the device, which may lead the device to failure. Moreover, the higher the current before UIS, the higher the current derivative at turn-off and, therefore, the overvoltage and the avalanche energy.

A comprehensive investigation on robustness properties of SiC is presented in [37], also by means of 2D TCAD electro-thermal simulations. The impact of devices parameters spread on avalanche breakdown transients in paralleled SiC MOSFETs is analysed in [38], where an experimental study is performed. Instead, in [39] a UIS study, on two commercial 1200 V 80 $m\Omega$ SiC devices, has been carried out. In [40], the authors have tested several SiC based half bridge modules, in order to assess their ruggedness, with results showing the SiC capability to withstand SC events, while during UIS test the majority of modules failed.

SC condition is a consequence of various failure mechanisms. SC capability is related to the so-called SC time. The SC event can lead to avalanche operation and overvoltage stress that may be mitigated with the adoption of two-level turn-off circuit [41]. In the following, the experimental result on ACEPACK^{TM} DRIVE module is presented for a SC test performed according to the standards. In this context, a shoot trough case, i.e. when both switches in half bridge are in on condition, is considered. The schematic of the circuit is shown in Fig. 8, where it is mentioned the adoption of the kelvin pin, in order to decouple signal and power paths [42]. The test conditions are the follow: bus voltage equal to 800V, $T_{j(start)} = 25°C$, for high side $R_{g-HS} \cong 0\ \Omega$, and $V_{GS-HS} = +18\ V$, for low side $R_{g(on)} = 3.3\ \Omega$, $R_{g(off)} = 4.7\ \Omega$ and $V_{GS-LS} = -5/18\ V$.

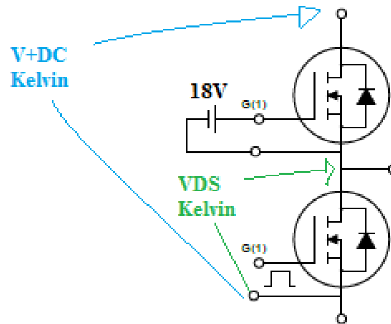

Fig. 8. Circuit representation of the shoot-trough case.

In Fig. 9, oscilloscope experimental traces are shown. It can be noted the short circuit event at the turn off. In this case, the parasitic inductances involved, coupled with high switching current, are the ones that bring the device in avalanche operation. We note that in this case the low side (LS) drain-source voltage is partially shared with high side (HS) switch, allowing less stress on the devices.

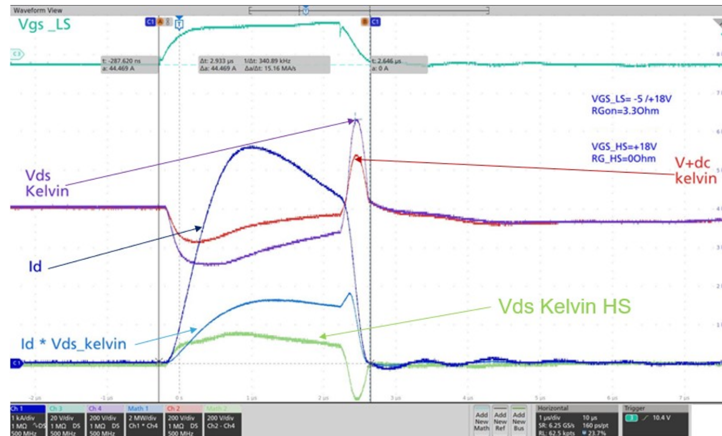

Fig. 9. Short circuit experimental traces. Each unit is equal to 1µs/div.

2.5 Layout issues

From the point of view of layout issues, various phenomena can arise. One of the problems is the existence of parasitic inductances. Hence, the evaluation of the inductance matrix with the values of all existing paths is very useful and can be obtained by FEA [43]. Key issues that can be mitigated by improving the layout are the negative and positive transient overvoltages occurring in the power module. More specifically, the influence of parasitic elements such as source inductance L_S and gate-Miller capacitance C_{gd}, coupled with high switching frequencies, can lead to positive and negative overvoltages in the module switches.

To describe the problem, let us consider one leg of a three-phase inverter of a module (Fig. 10). When the derivative of the drain-source voltage is positive, there could be a spurious turn-on, the so-called Miller turn-on, due to parasitic capacitive effect [44]. On the other hand, when the derivative is negative then a gate-source negative overvoltages may occur. They are more dangerous than the positive ones [17] since negative V_{GS} spikes may damage the device gate oxide. Hence, from the reliability point of view it is important to limit this issue. Examples of waveforms related to the positive and the negative overvoltages are illustrated in [17].

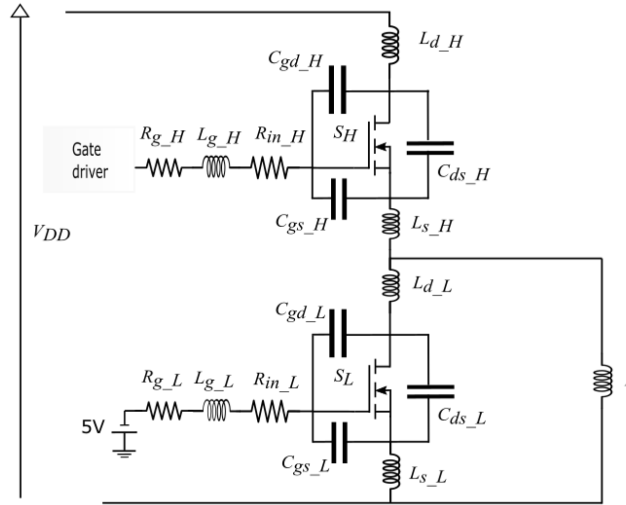

Fig. 10. Half-bridge configuration.

In addition, parasitic inductances evaluation and simulation are essential in case of paralleled dice. In this context, it is possible to estimate the inductive and resistive contributions of different paths in the power modules again by means of FEA.

Another approach for parasitic parameters extraction, both in discrete devices and in half bridge power modules, has been developed in [45], where two-port parameters (scattering S and impedance Z) have been used. More specifically, firstly S-parameters are measured, then they are converted into Z-parameters.

In order to better highlight the problem, double pulse tests on a not optimized R&D prototype module are carried out and the experimental traces are shown in Fig. 11. The quantities are referred to the LS device being off ($V_{GS} = -5V$), while the HS one is turning on. In this case, the diode reverse recovery can play a role in the first part of the switching period (few nanoseconds), if we consider these overvoltages. This behavior involves the negative overvoltage spike on V_{GS}.

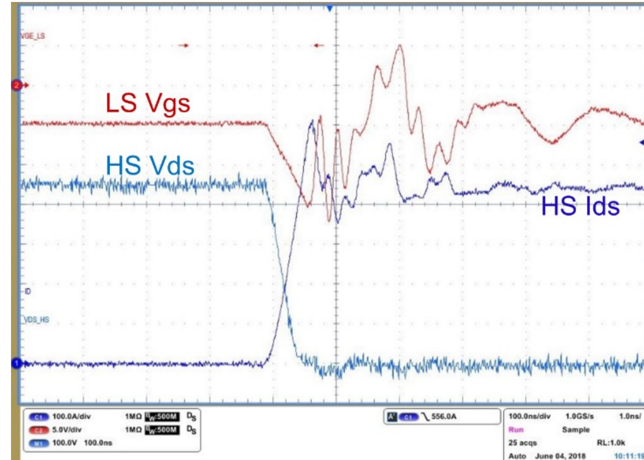

Fig. 11. Experimental traces for negative overvoltage. Each unit is equal to 100ns/div.

The design of optimized module layout, in terms of source inductance minimization, has to be considered as a guideline to deal with this phenomenon. The minimization is obtained bringing the kelvin pins as near as possible to the dice, thus reducing the inductance paths. Parasitic inductance reduction is also obtained making both HS and LS kelvin pins symmetric among the gate, although this further optimization is done primarily to balance the signals. In fact, the behavior of LS and HS may be very different, referring to dice waveforms, when these guidelines are neglected.

2.6 Conclusions

In SiC modules for traction inverters framework, several issues, descriptions, solutions, experimental and numerical results have been reported in this chapter. An analysis of electro-thermal issues has been performed, as well as electrical, thermal and fluid dynamics simulations in order to assess possible thermal constrains or electrical performances. Then, problems related to parallel connection of many SiC dice have been taken into account with thermal simulations. Unclamped inductive

switching and short circuit have been discussed, with an experimental test on a SiC module prototype. Finally, layout problems have been considered, giving a theoretical description of negative and positive overvoltages, and displaying experimental results and possible guidelines in order to prevent this phenomenon. We have considered real cases, which came from on-field experience. In conclusion, this work may help the designers to pay attention to all these issues when they deal with SiC power modules.

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3. DIRECTLY COOLED SILICON CARBIDE POWER MODULES: THERMAL MODEL AND EXPERIMENTAL CHARACTERIZATION

This chapter has been taken (with some modifications) from the following published paper:

- **G. Mauromicale**, A. Cascio, M. Papaserio, D.G. Cavallaro, G. Bazzano, A.A. Messina, S. Patanè, M. Calabretta, A. Sitta, "Directly Cooled Silicon Carbide Power Modules: Thermal Model and Experimental Characterization," *PCIM Europe digital days 2021; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*, 2021, pp. 1-5

This chapter presents a 3D Finite Element Model (FEM) and fluid dynamics simulation to investigate the behavior of a directly cooled SiC module structure, to go deeply in one of the topics already outlined in the chapter 2. Furthermore, a two-step experimental procedure to thermally characterize the module is also reported. It comprises a calibration and, subsequently, the thermal impedance computation. The proposed FEM model is compared with experimental test results in order to demonstrate its effectiveness.

3.1 Introduction

Usually, it is of paramount importance to model heat in the power module, including the heatsink, for establishing the dies thermal behavior

[1]. This is mandatory for reliability assessment [2], [3]. In the reliability framework, power cycling tests are employed to experimentally test SiC based power devices and modules [4]. These types of tests follow the specifications provided by the AQG324 guideline [5]. The target of power cycles is to enhance the failure mechanisms related to the fatigue of package interconnections, such as wire bonding and substrate attach [6], [7].

Thermal behavior and, consequently, reliability strongly depend on the die attach technique, too. In fact, both soldered and silver sintered solutions can be implemented. However, the latter is preferable to optimize thermal performances and reliability [8]. Due to higher thermal conductivity, sintering slightly enhances power dissipation while realizing a more reliable joint, both for passive and active thermal stress, between die and substrate. Considering the high current which flows in the module, it is expected that they would encounter various thermal reliability issues originating from their high power density, hence the cooling system plays a key role in reliability. Direct liquid cooling, with pin-fin at the module baseplate, is implemented as a method for allowing an efficient heat exchange [9]. In general, simulation studies are being more and more important in power module development [10]. In this chapter, a SiC liquid cooled power module is studied from both experimental and simulation points of view. Furthermore, cross-heating among dies connected in parallel in these structures must be carefully addressed [11]. A Finite Element Analysis (FEA) is carried out with the aim of simulating the module thermal behavior. The proposed model considers the mutual interactions between the dies, as previously mentioned. Various environmental conditions are simulated accounting for the heat flux in multiple layers comprising cooler, package, and the baseplate.

The final aim of this work is to evaluate, both experimentally and numerically, the transient thermal impedance of a directly cooled SiC power module. The chapter is organized as follows: in Section 3.2, firstly the SiC power module is briefly described, then the experimental setup and results are reported and the experimental tests are described. In Section 3.3, the simulation activity is outlined, including thermal and fluid dynamics aspects. Finally, in Section 3.4 a comparison between the two frameworks is given, and in Section 3.5 the conclusions are drawn.

3.2 Module description and experimental results

3.2.1 Module description

The simulation and the experimental trials described in the present chapter have been performed on ST ACEPACK DRIVE®, a power module that contains SiC devices arranged in a three-phase inverter topology, already presented in the previous chapter. More specifically, each switch is made up by eight dies in parallel. The power module's thermal dissipation system is simulated considering both the conduction and the convection heat transfer modes, reproducing the real cooling system behavior, as depicted in Fig. 1.

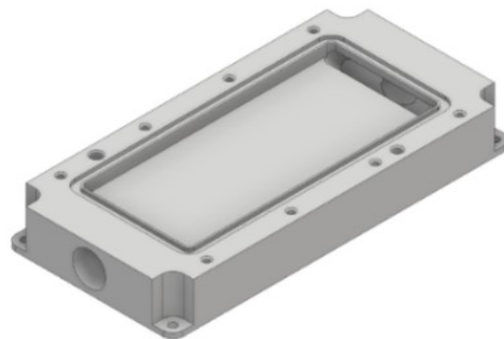

Fig. 1 Cooler structure examined in the chapter.

Directly liquid cooling, with pin-fins at the module baseplate, is implemented for an efficient heat exchange in terms of cooling performances and dimension.

3.2.2 Experimental results

In this sub-section, experimental results obtained will be showed. The aim is to compute thermal impedance of the power module described above. The Alpitronic's equipment for power cycling is used in the test. It contains a hydraulic circuit which can adjust the cooling flow rate [12]. The experimental tests are compliant with AQG 324. Now, a brief description of the used method is reported. Regarding the experimental test, the virtual junction temperature can be calculated by using the body diode drop voltage during the off-state period, when a negative V_{GS} voltage is applied to the SiC MOSFET. Then, it is possible to compute the thermal impedance Z_{th}. The power module is subjected to self-heating due to high current (hundreds of A) flowing in power devices [12]. Temperature-sensitive electrical parameter is a technique used in this type of characterization, which relies on different electric semiconductor device parameters that depend on temperature [6], [8], [13]. The formula is reported here below:

$$Z_{th}(t) = \frac{(T_j(t_0) - T_{fluid}(t_0)) - (T_j(t) - T_{fluid}(t))}{V_{DS,max} \cdot I_{LOAD}} \quad (1)$$

where t_0 is time, equal to 100 μs in this framework, at which the first measure is executed, T_j and T_{fluid} are, respectively, the virtual junction temperature and the fluid temperature, while $V_{DS,max}$ is the maximum MOSFET forward volage and I_{LOAD} is the current. The calibration of body diode drop voltage has been done heating the coolant by external

temperature unit. Thermal equilibrium between fluid and power modules is reached when the power module embedded-NTC temperature and the body diode drop voltage are constant with respect to the time. This procedure is repeated for each calibration temperature. Fig. 2 shows a typical calibration curve in which body drop voltage (V_{SD}) has been plotted with temperature that ranges between RT and 100 °C.

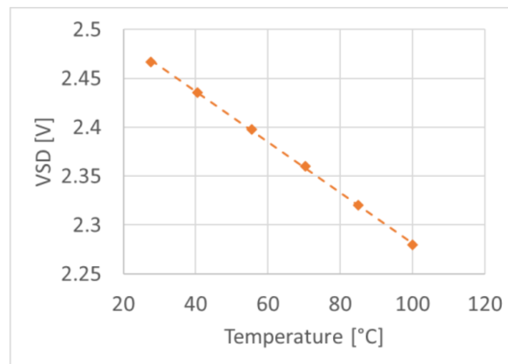

Fig. 2 Drop diode voltage vs temperature calibration curve.

3.3 Simulations

In this section, the simulation setup and conditions data are given, showing also some pictures on thermal and fluid dynamic results. The power module's thermal dissipation system is simulated considering both the conduction and the convection heat transfer modes, reproducing the real cooling system, as depicted in Fig. 1. A solution made up by water and glycol (in the ratio of 50/50 %) flows in the cooler from the inlet to the outlet manifolds, fixing a flow rate of 6 l/min, which implies a laminar flow inside of the cooling system. The air temperature around the modules is maintained fixed at a typical ambient value, while the fluid inlet temperature is established at 50°C. The outlet fluid temperature is a simulation output. This fixed set-up has allowed the simulation of the temperature distribution. Fig. 3 depicts the fluid dynamics simulation

output in terms of fluid velocity. Fig. 4 shows the simulated thermal map, as obtained powering on two switches. It can be observed that the simulated temperatures are quite similar in the considered dies. By applying the well-known formula previously explained, the $Z_{thj\text{-}fluid}$ can be computed having the information about the average switch junction temperature, the fluid temperature, and the power applied to the DUTs.

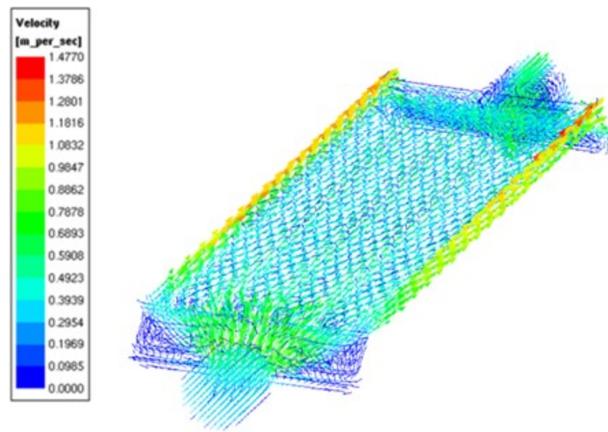

Fig. 3 Fluid velocity inside the cooler.

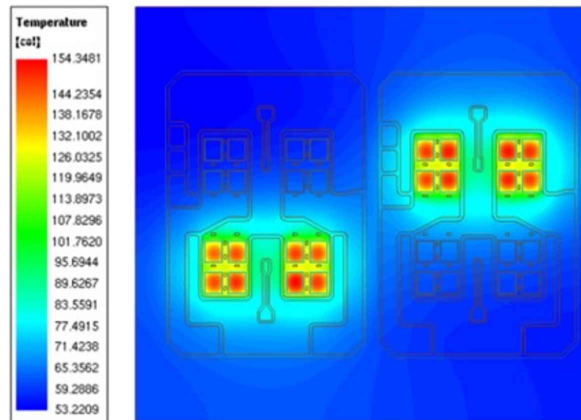

Fig. 4 Thermal map.

Moreover, in order to consider the cross-coupling heat flow occurring among the dice, the mutual thermal impedance between one die, which is dissipating the power losses, and its neighbor one, with both that are just

sensing the temperature dissipated by the single die, has also been evaluated [14]-[16]. In Fig. 5, the normalized thermal impedance is shown. The blue curve represents the thermal behavior of the die where the power losses is provided, while the other three curves are referred to the neighbor devices. The observed delay between the curves is due to the heat propagation in the material, the geometry, and the distance from the source and the other dies.

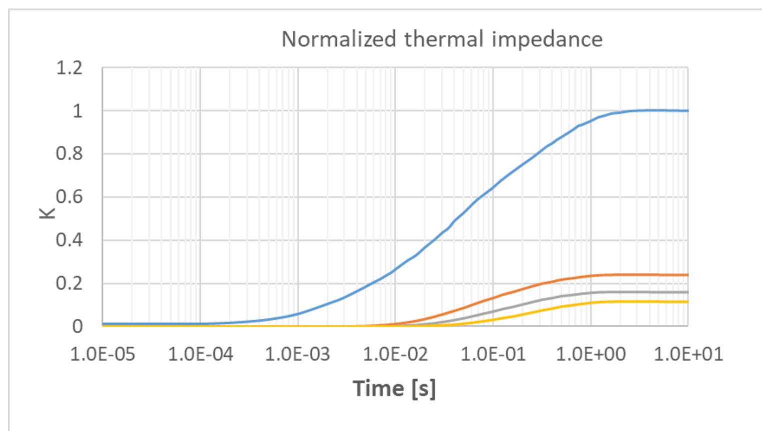

Fig. 5 Simulated thermal impedance semi-logarithmic graph

3.4 Comparison between experimental and simulation results

Experimental tests with the same conditions are performed in order to calibrate the developed model. In this section, a comparison between experimental and simulation results, which are presented previously in the chapter, is executed. The graph depicted in Fig. 6 shows a good correspondence between the experimental and the FEA thermal impedance results, thus confirming the goodness of the model. More in detail, it is possible to note that there is a little misalignment, between the two curves, in the central zone of the graph (0.001 s-0.1 s).

In particular, there is a slightly delay of the measured curve, probably due to different capacitance values in the two cases.

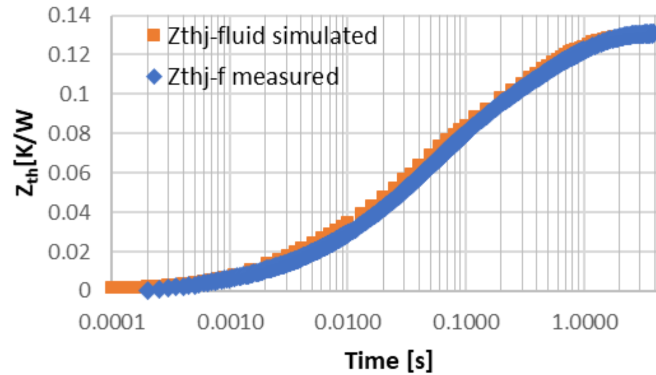

Fig. 6 Measured and simulated thermal impedance semi-logarithmic graph.

3.5 Conclusions

In this chapter, a directly cooled power module, made up of silicon carbide, has been studied both experimentally and numerically. The experimental method, using body diode drop voltage measurement during the off-state period, has been outlined considered. Then, thermal simulations, considering also module's fluid dynamics, have been carried out. It has been seen how the simulation results fit quite well with the experimental ones, as it has been pointed out in the work. More specifically, the testing phase has coped with the thermal impedance evaluation. Then, a finite element and fluid dynamics simulation has been considered to compute the same quantities obtained in the experimental phase.

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PART III: GAN-BASED POWER DEVICES

4. ANALYSIS OF THE IMPACT OF THE OPERATING PARAMETERS ON THE VARIATION OF THE DYNAMIC ON-STATE RESISTANCE OF GAN POWER DEVICES

This chapter has been taken (with some modifications) from the following published paper:

- **G. Mauromicale**, S.A. Rizzo, N. Salerno, G. Susinni, A. Raciti, F. Fusillo, A. Palermo, R. Scollo, "Analysis of the impact of the operating parameters on the variation of the dynamic on-state resistance of GaN power devices," *2020 2nd IEEE International Conference on Industrial Electronics for Sustainable Energy Systems (IESES)*, Cagliari, Italy, 2020, pp. 101-106.

In this chapter, on-state dynamic drain-source resistance ($R_{DS(ON)}$) phenomenon in GaN based power switches is analyzed. Dynamic $R_{DS(ON)}$ may increase the power losses in converters, thus reducing the benefits of using GaN power devices in this field. The operating parameters having an impact on dynamic $R_{DS(ON)}$ are investigated by analyzing the research works available so far from industry and academia. The objective of this work is to highlight the key operating parameters that influence this phenomenon, in order to give useful information to designers. Another objective is the identification of the lack of information on the topic, thus suggesting the analysis necessary for an all-embracing understanding of the influence on dynamic $R_{DS(ON)}$ due to the different operating conditions. To these aims, the collected data are harmonized since the variety of test conditions and

the different methods adopted to report the results and to obtain them. The comparison has highlighted that the working frequency is the main factor influencing the dynamic $R_{DS(ON)}$. Moreover, the analysis has drawn attention to the necessity to make extensive experimental analyses on various technology types and mission profiles. Finally, the main research topic to be properly investigated concerns the deep analysis of the correlations among the parameters which affect the dynamic $R_{DS(ON)}$

4.1 Introduction

In previous two chapters, SiC power devices were discussed, considering, in particular, module solutions used in traction applications [1]. Instead, in the next two chapters Gallium Nitride (GaN) based devices will be studied. GaN-based technology is promising in many applications [2]-[11] because the GaN power devices have better figure-of-merits in comparison with the silicon ones [6]. More specifically, the superior physical properties lead to a low specific R_{ON} and leakage, a high breakdown voltage and a zero reverse recovery charge [5], [10]. Moreover, the very low parasitic capacitances result in smaller switching losses. Hence, there is an improvement also in efficiency and maximum reachable frequency in power converters [3]. Higher power density is reached thanks to these reasons in low and medium voltage power applications. In Fig. 1, a comparison between the efficiency of Si and AlGaN/GaN High Electron Mobility Transistors (HEMTs) power devices is reported.

GaN devices have many applications in power electronics, both in automotive [13], [14] and industrial fields. Emerging LiDAR systems, on board chargers, wireless power transfer, LED lighting [15], data centres, and power supplies for servers are some of the current or potential

applications of these power devices [2], [7]. Notwithstanding, there are still several hindrances that must be overcome both from physical and application points of view. There are reliability problems, switching oscillations related to high slew rates of voltages and currents, and dynamic on state drain source resistance ($R_{DS(ON)}$) [4].

Dynamic $R_{DS(ON)}$ may be very higher than the static one. At present, on-state dynamic resistance in GaN devices still remains one of the principal issues, even if several technological improvements have been made to reduce the converter losses [2]. On the contrary, this problem is today absent in Si-based switches, because of the developed optimized passivation process, that is more difficult in GaN ones, with traps in different parts of the device [16].

The chapter is organized as follow: in Section 4.2, first an outline of the various types of GaN devices is given, then a short explanation of the physical phenomena leading to dynamic $R_{DS(ON)}$ is reported. In Section 4.3, a literature review of the parametric dependence regarding dynamic resistance is discussed. In Section 4.4, the analysis of the results is explained and, finally, the conclusions are reported in Section 4.5.

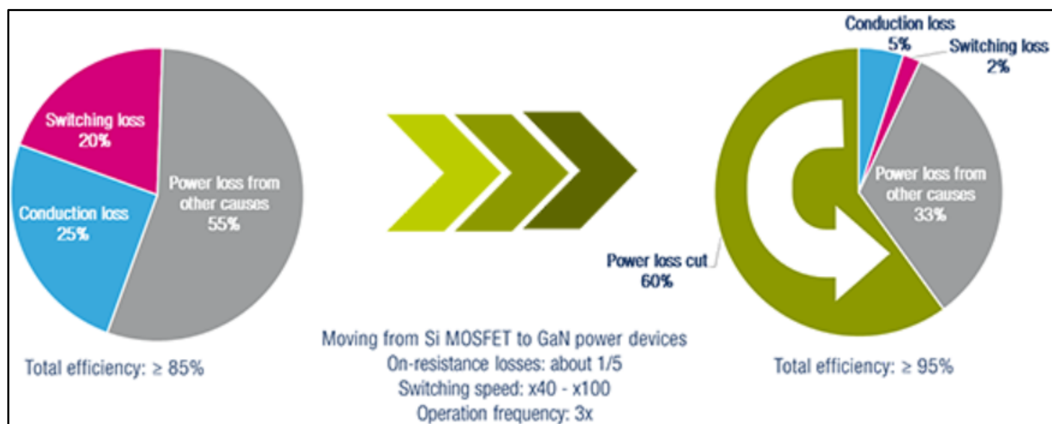

Fig. 1. Efficiency and power losses in Si and GaN based power devices. Credits by [12]

4.2 Dynamic Resistance in Gan Power Devices

4.2.1 GaN power devices types

In this section, a brief outline of the various technologies of GaN power device is given. There are both lateral and vertical devices, even if the second ones are nowadays at prototype stage. More specifically, free-standing GaN substrate, Gan-on-GaN vertical devices, are nowadays under development but they are still not commercial products [2]. On the other hand, lateral devices are already available, and the incoming ones have very promising performance. These devices need a Si or SiC substrate, thereby obtaining, respectively, GaN-on-Si or GaN-on-SiC power devices.

In the device structure, shown in Fig. 2, at AlGaN/GaN interface, there is the formation of 2DEG two-dimensional electron gas, that is the channel.

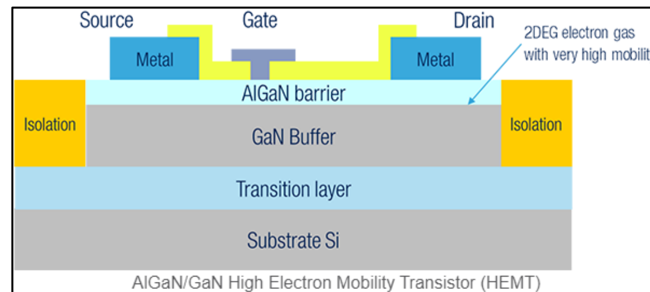

Fig. 2. Lateral GaN HEMT physical structure. Credits by [12]

GaN devices are inherently depletion mode, that is normally-on devices [9]. However, normally-on devices are nowadays not used anymore, since normally-off ones ensure more reliable and safe operations, also reducing the leakage current and simplifying the driving circuit [2], [9]. The most common normally-off device technologies are: p-GaN and recessed gate devices. In the first case there is a p layer, in such a way the 2DEG cannel is depleted, while in the second one the AlGaN barrier layer is removed and the recessed gate region is passivated [5], [11]. Another possibility to

make normally-off devices is the adoption of the cascode configuration, although it is less considered. It consists of a low voltage Si MOSFET which drives the GaN normally-on transistor in a series configuration [5]. Among the normally-off devices, HEMT devices are today the most common in the market since they are the most promising ones. Regarding the breakdown voltages, there are power devices until 650 V, and others with voltages of 100 V or even behind this value [6].

4.2.2 Physical mechanisms behind the dynamic on-state resistance phenomenon

The dynamic on state resistance phenomenon is also called current collapse. It pertains some charges released into the 2DEG channel inside the switch during the turn-on [2]. More specifically, some charges are trapped in the buffer and the surface parts of the device due to the high electric fields in the device during the off state [17]. Hot electrons, generated in the channel during the switching events, can be trapped in the buffer layer or in the gate passivation region. During turn-on, the charge previously trapped are released (detrapped) in the channel, thus involving an increase of the $R_{DS(ON)}$ [18]. In Fig. 3, the trapped charges due to the different mechanisms are shown. Therefore, two main mechanisms of charge trapping exist in GaN devices. One is related to the off-state voltage: it depends on this voltage as well as the time it is sustained (i.e. the off time). The other mechanism is due to the concurrent occurrence of current and voltage during hard switching transients. In this case, some electrons in the 2DEG channel have enough energy, due to the simultaneous high current and large electric field, to be trapped. The number of trapped electrons is influenced by the off voltage, the gate resistance and the drain current [19].

Trapping and detrapping time constants are important to understand also the impact of the application parameters, since, for example, low on-state time interval may imply to have not enough time to complete the detrapping of the electrons [19]. The trapping-detrapping phenomenon may be modelled by means of RC networks, in order to simulate system with different trapping and detrapping time constants [17].

Some solutions, at device level, have been devised to mitigate this phenomenon: hole compensation and photon pumping, buffer stack optimization, and vertical GaN-on-GaN device technology [2]. Extensive experimental results of current collapse free operation in a GaN-on-GaN Schottky barrier diode are reported in [20].

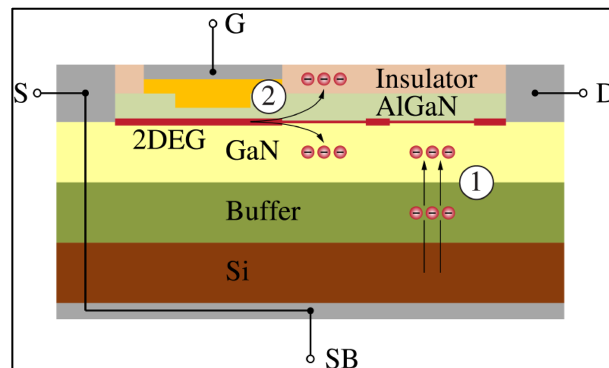

Fig. 3. Mechanisms leading to dynamic $R_{DS(ON)}$: 1) off state trapping, 2) effect of hot electrons. Credits by [19]

4.3 Dependence Of Dynamic $R_{DS(ON)}$ On Operating Parameters

There is a widespread interest on the impact of the operating conditions on the variation of the value of the dynamic $R_{DS(ON)}$ [2], [16]-[41]. The first issue is the use of the appropriate measurement technique. There are various methods to measure the dynamic on state resistance, developed by using several circuits with active and passive components, and with

different laboratory instruments [16]-[18], [21], [22]. It is not possible to carry out the measure only with an oscilloscope, therefore a clamping circuit is necessary in order to correctly measure the small on state voltage after the fast dropping from the high blocking voltage [30], as it was outlined in the first chapter of this thesis. Therefore, it is important to measure the quantities in a very short time, which can be also in the range of hundreds of nanoseconds [31]. In various works, different measurement circuits able to reduce the measure delay time (due to the switching transient) and to accurately measure the $R_{DS(ON)}$ value are proposed [17], [22]. There are two main approaches to measure the dynamic $R_{DS(ON)}$. An approach is related to on wafer measurements, which is used especially for physical devices optimization. The main issues are the parasitic elements it may introduce and the loss of information since it does not catch the initial part of the on-state. Another approach is related to specific fabricated boards in order to simulate the real power electronics applications and mission profile [2]. In the following, the operating parameters tested using the latter approach that have investigated in literature for the dynamic $R_{DS(ON)}$ have been only considered.

According to the trapping mechanisms described before, off-state voltage may probably affect the dynamic $R_{DS(ON)}$ and, consequently, it has been widely investigated so far. Therefore, also the off-state time influences the dynamic resistance, due to the aforementioned charge trapping time constant [17]. Similarly, the switching frequency is a quantity that may affect the dynamic resistance. In particular, a key feature of GaN devices is the fast switching ability enabling them to be operated at high switching frequencies. Thereby permitting lower switching losses as well as power converters with smaller magnetics components. On the other hand, the frequency increment would be a candidate for performance

worsen in terms of the dynamic resistance and, consequently, more conduction losses that, in turn, involve a decrease in converter's efficiency [24], [34]. Duty cycle is related to the switching frequency and off time, then it also has an indirect impact on the variation of the dynamic resistance [19], [34], [36]. The load current is another important parameter to be considered [36]. The temperature must be also considered since it is connected to the generation of hot electrons in the device. In this case, two causes of the increase of resistance can be distinguished: one due to the self-heating effect and another one related to the trapping. In [21], the two effects are decoupled to make evident the different contribution on dynamic resistance. For example, the reduction of the pulse duration is a solution to avoid the contemporary presence of the two effects [34]. Gate resistance at turn off and turn on have been taken into account in terms of its impact on dynamic resistance. Instead, in a half bridge topology, the effect of crosstalk (discussed in chapter 2, on SiC power modules, but the principle of operation is similar in GaN devices) on the dynamic resistance of the complementary device can be neglected because it does not influence dynamic $R_{DS(ON)}$. [18].

Hard switching is employed in a lot of applications and exhibits high value of current and voltage at switching transients, then, in these applications charging trapping occurs. Indeed, also in soft switching topologies [4] this problem is of concern, even if in a less severe way [26]. In soft switching, there is not the contribution of the trapped charges due to the hot electrons. This is due to the lack of intersection between the current and the voltage that occurs during the hard switching transient. Nevertheless, there is the contribution of the off-state voltage and off state time [19]. Double pulse test on inductive or resistive loads is important to assess the values of dynamic $R_{DS(ON)}$. Tests to obtain I/V are used in the

standard characterization of devices physical features and in the optimization process stage. It is worth to note that pulses duration is highly variable among the experimental tests made in literature. JEDEC standard defines the test conditions for the three tests mentioned above [29]. Multi-pulses tests can simulate a more realistic working condition of devices in comparison to the double pulsed ones [21], [22], because in the initial pulses the dynamic resistance would not be stabilized yet. In this perspective, continuous switching operations, that can be closer to the behaviour of the converter, are useful to fully understand the impact of $R_{DS(ON)}$ in real applications [40]. For example, in [34] the authors consider a step-down topology to carry out the experimental tests. One of the observed phenomena is the not complete recovery (detrapping) of the trapped charges when a limited number of pulses is considered [19].

In general, dynamic $R_{DS(ON)}$ worsens in power applications with high values of frequency, voltage, current and temperature. For this reason, even if there are difficulties in reaching at the same time all the possible real conditions, it is useful to make experimental tests toward this direction [26].

4.4 Analysis Of The Influence Of The Working Parameters On The Dynamic $R_{DS(ON)}$

In this section, the results of the analysis are given, pointing out the most important parameters in power conversion applications. In the following analyses, 23 papers from the literature are analyzed [16]-[28], [32]-[41]. More in detail, the parameters introduced in the previous section are analyzed in each work, considering their impact on dynamic $R_{DS(ON)}$. The aim is to understand their influence on dynamic resistance, thus understanding the critical ones. Only experimental data with graphical or

numerical proofs have been considered, thereby excluding the results obtained by means of simulation or theoretical analysis. Moreover, the tests performed on the wafers or on vertical devices have been neglected.

For each operating parameter examined, a mark has been assigned according to its impact on the dynamic $R_{DS(ON)}$. Ideally, the mark may be considered as the slope of the trend curve interpolating the variation of the resistance with the variation of the given parameter. It is worth to note that, for each paper, more than one mark may be assigned to a given parameter, according to the number of case studies. More specifically, a distinction among the experimental results provided in a paper has been considered in case of a change in the device part number or technology, breakdown value, measurement methods (soft, partial soft, hard, and resistive switching) and number of pulses. Each of them represents a different case study. For example, when in a work the results on the impact of a given parameter for three different device technologies are reported (three case studies), three marks have been assigned for each analysis regardless the mark values (that is, three marks are considered also when two marks or all are equal among them). According to this distinction, 70 case studies have been obtained from the 23 papers.

The marks have been assigned only to the operating parameters more investigated in literature:

1. off voltage,
2. off time,
3. load current,
4. frequency,
5. temperature.

Obviously, a parameter could not be investigated in a paper at all, or partially considered (that is in a subset of the case studies). In other words, in each paper, a specific set of analyses is accomplished. Hence, there are papers that have not performed any analysis with respect to one or more of the considered parameters. Instead, in other cases, there are several case studies in which a specified parameter is analyzed in the same paper, because, as said before, there are changes in device technologies, breakdown value or manufacturer or measurement conditions. Therefore, in these papers a parameter has more than one mark. According to this, Table I reports the number of marks assigned to each operating parameter.

The simplest way to compare the impact of the different parameters is the classification of the average mark they obtain. The average mark for each parameter has been computed according to the number of marks available for it (Table I). The average marks have been normalized with respect to the greatest average one. The resulting quantities are depicted in Fig. 4, that shows that the switching frequency is the most influential parameter. Moreover, off voltage and temperature have almost the same impact, which is also high.

Table I. Number of Marks assigned to each Parameter.

Working parameters	Number of marks
off voltage	49
off time	16
frequency	44
temperature	25
load current	20

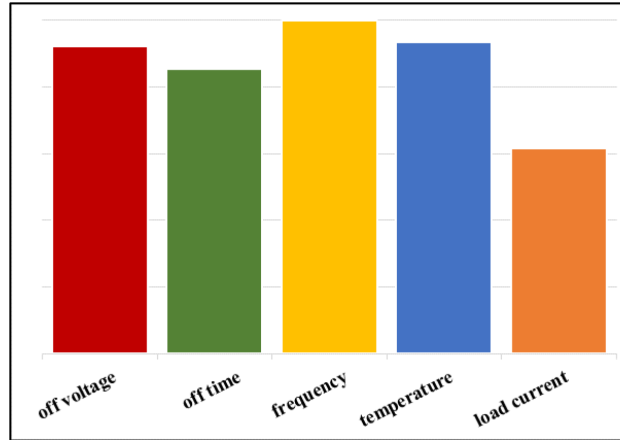

Fig. 4. Average marks normalized with respect to the greatest average one.

Although Fig. 1 provides useful information, there are some weaknesses in using directly the average marks. They are due to the partial information provided in the different case studies. In fact, the measure methods, the devices types and the working conditions considered are usually very different. Moreover, each paper considers a particular collection of parameters examined experimentally, rarely almost all or all the possible ones. The following example aims at better highlighting a weakness of the previous approach. Let us assume that in a case study both off voltage and temperature are investigated, and their marks are respectively 8 and 7. In another case study, the off voltage is only analyzed and its mark is 5. Therefore, the temperature receives the highest mark in comparison to the off voltage, but this conclusion could be misleading. More specifically, the two case studies can be very different between them due to the different tests conditions, the different methods adopted to report the results and to obtain them, and so on. Therefore, the different impact (then different mark) of the off voltage in the two cases could be due to these differences. In the second case the impact of the off voltage could be attenuated by the specific test, and if the effect of temperature was investigated it would be attenuated too, thus obtaining again a lower

average mark then the off voltage. Therefore, if this analysis was available the temperature would receive the lowest mark in comparison to the off voltage. On the other hand, the lacking information involves the misleading result.

The comparison of the marks on the basis of each single case study solves this problem. In detail, for each case study, the marks have been normalized with respect to the greatest one for the given case study. In details, being $M_{p,k}$ the mark assigned to the p-th parameter for the k-th case study ($k=1,\dots,70$), the normalized mark, $N_{p,k}$, has been computed as follows:

$$N_{p,k} = \frac{M_{p,k}}{M_{m,k}}$$
$$M_{m,k} = max\left(M_{p,k}\right) \quad p = 1, \dots, 5 \tag{1}$$

After that, the average value of the normalized quantities, $N_{p,k}$, has been computed for each parameter similarly to the previous analysis. Finally, the average values have been normalized again with respect to the highest value and the results are shown in Fig. 5, which is then obtained similarly to Fig. 4. In this case, the most influential parameter is the off voltage, although the switching frequency presents very close influence level. Then, in order of impact level, there are the temperature and, in last position, equally off time and load current.

Although the normalization of the marks of a single case study enables to overcome the limitation of the direct use of the average values, it may introduce other bias especially when only one parameter is analyzed in a case study. For example, if only the load current is analyzed in a case

study, the highest normalized value (that is 1, according to equation in 1) is assigned to it regardless its mark is low or high.

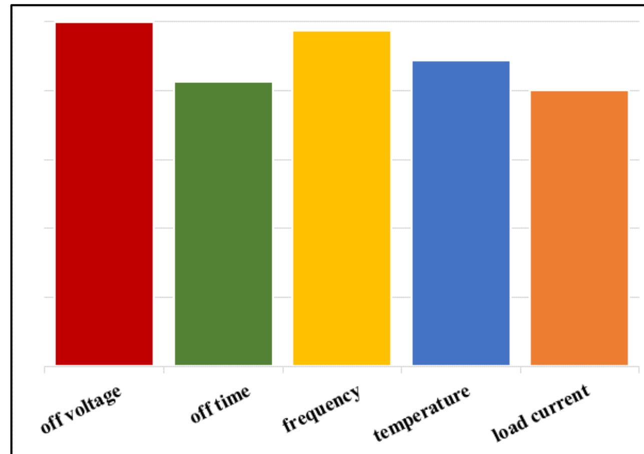

Fig. 5. Average of the normalized marks on single case study basis. The values have been further normalized with respect to the greatest average one.

Therefore, if in the 20 (see Table I) case studies, the load current reports a low impact (then low mark), but in many of these case studies it is analyzed alone, the load current presents high average normalized mark although its impact is low.

Therefore, another comparison mechanism is introduced on the basis of each case study, where a “match” is considered for each couple of parameters. For each case study, the difference between the marks of the two parameters playing the match has been computed and the related scores have been assigned to the parameters. The following example provides a better understanding of the comparison mechanism. Let us assume 8, 7, 5 have been the marks given to, respectively, frequency, temperature and off time in a given case study. Then 1 and 3 are the scores assigned to the frequency, -1 and 2 to the temperature, -2 and -3 to the off time. In this way, it is simpler to better understand the different influence of the parameters. On the other hand, the number of used case studies is reduced since the comparison mechanism discards those where only one parameter

is investigated (since no match is available). Although the number of case studies is reduced, more than one score (difference) could be assigned to a parameter in a case study, because there is more than one match when there are more than two parameters. Table II reports the number of matches considered for each parameter.

Once the scores have been computed for each match of all the case studies and assigned to the related parameters, the average value of these quantities has been computed. After that, the results have been mapped into the interval [0,1] and normalized with respect to the greatest quantity. The graphical results of this comparison are reported in Fig. 6. The switching frequency is again the parameter that has the greatest impact on the dynamic $R_{DS(ON)}$. Although the off voltage and temperature show a high impact, their influence is below the frequency with an increased distance in comparison to the previous analysis. Similar considerations are valid for the load current and, especially, for the off time. This comparison mechanism reveals a limited impact of the off time, differently from the previous analysis.

From the inspection of the three figures, it can be noted that, regardless the analysis mechanism, the frequency is the parameter most influencing the increment of the dynamic on state resistance.

Table II. Number of Scores assigned to each Parameter.

Working parameters	Number of matches
off voltage	58
off time	31
frequency	28
temperature	46
load current	33

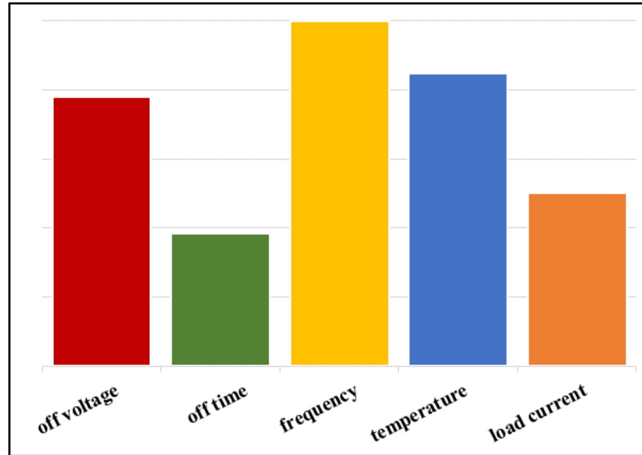

Fig. 6. Average scores. The values have been normalized with respect to the greatest average one.

4.5 Conclusions

In this chapter, the influence of the working parameters on the dynamic on-state resistance in GaN power devices has been investigated by means of a deep analysis of the literature. The investigation has revealed that the working frequency is the parameter with the major impact on the dynamic $R_{DS(ON)}$. Moreover, off voltage and temperature also influence the variation of the dynamic resistance.

To perform the comparison, the data recovered have been harmonized, giving possible ways to understand how they can be interpreted in a not misleading form. In fact, the several different types of experimental tests make hard to give a unique interpretation of the data. Therefore, this work would be a starting point for a better understanding of the impact of the working conditions.

An important aspect arising from the study is that the mutual interactions among the parameters are rarely reported. Therefore, the deep analysis of the correlations among the parameters that affect the dynamic resistance is the main research topic to be properly investigated.

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5. INTEGRATED ELECTROMAGNETIC-THERMAL APPROACH TO SIMULATE A GAN-BASED MONOLITHIC HALF-BRIDGE FOR AUTOMOTIVE DC-DC CONVERTER

This chapter has been taken (with some modifications) from the following published paper:

- **Mauromicale, G**.; Sitta, A.; Calabretta, M.; Oliveri, S.M.; Sequenzia, G. Integrated Electromagnetic-Thermal Approach to Simulate a GaN-Based Monolithic Half-Bridge for Automotive DC-DC Converter. Appl. Sci. 2021, 11, 8302

New and more integrated power devices are useful to guarantee the performances in electric vehicles, in terms of thermal management, size reduction, and low power losses. In this chapter, a GaN-based system in package solution is simulated to assess the structure temperature submitted to a Joule heating power loss. The monolithic package solution involves a half-bridge topology, as well as a driver logic. A novel integrated electromagnetic and thermal method, based on finite element simulations, is proposed in this work. More specifically, dynamic electric power losses of the copper interconnections are computed in the first simulation stage, by an electromagnetic model. In the second stage, the obtained losses' geometrical map is imported in the finite element thermal simulation, and it is considered as the input. Hence, the temperature distribution of the package's copper traces is computed. The simulation model verifies the proper design of copper traces. The obtained temperature swing avoids any thermal-related reliability bottleneck.

5.1 Introduction

As already outlined in the previous chapter about gallium nitride (GaN), high-efficiency converters are possible when GaN devices are employed, because they have higher breakdown electric field and low on-state resistance.

High electron mobility transistors (HEMTs) are currently being employed on the market. From a physics point of view, GaN-on-Si technology, that is, with GaN on a silicon substrate, is today industrially mature. With reference to the voltage classes, in the context of power devices, both high voltage (HV, until 650 V) and low-voltage (LV, under 100 V) switches do exist today.

Miniaturization can be possible because there is a low contribution in parasitic elements, such as intrinsic device capacitances, that results in lower heating, and, as a consequence, a smaller die and occupied area by the package [1]. This also results in low power losses. In the GaN framework, new LV and HV power devices are important, among the others, for the following applications: DC-DC converters, onboard chargers, adapters, wireless charging, class D amplifiers, flyback SMPS, boost converters, and LiDAR [2]. In Figure 1, the possible applications of Si, SiC, and GaN devices, in terms of output power and operating frequency, are depicted [3]. For LV applications, GaN devices are commonly employed in monolithic packages, because they dissipate lower switching and conduction losses. The principal challenges currently present in the design and application of GaN-based power devices mainly rely on thermal management [4], parasitic contributions with high switching frequency (high dv/dt and di/dt slew rates coupled with parasitic elements) [5], reliability [6], and dynamic on-state resistance. The last topic is the increase in drain-source resistance, as a consequence of trapping

phenomena during the transition between off and on states [7–10]. A parametric analysis of the impact of parameters, such as off voltage and time, frequency, current, and temperature, based on the available literature, is presented in [11]. This item has been already treated in previous chapter, therefore in this chapter it will be not focused anymore. High-frequency operation would reduce the passive components requirements; however, the interaction between parasitic inductances and capacitances, and dv/dt and di/dt, can produce more losses [12], switching oscillations [13,14], and false turn-on [15]. Related to this issue, there exists a more general topic regarding the power losses, in terms of both models and experimental methodologies [16–19]. Moreover, the hysteretic losses related to the output capacitance must also be taken into account, especially in soft-switching applications (i.e., where there is not a hard intersection between the drain-source voltage and drain current at the transient stage) [20].

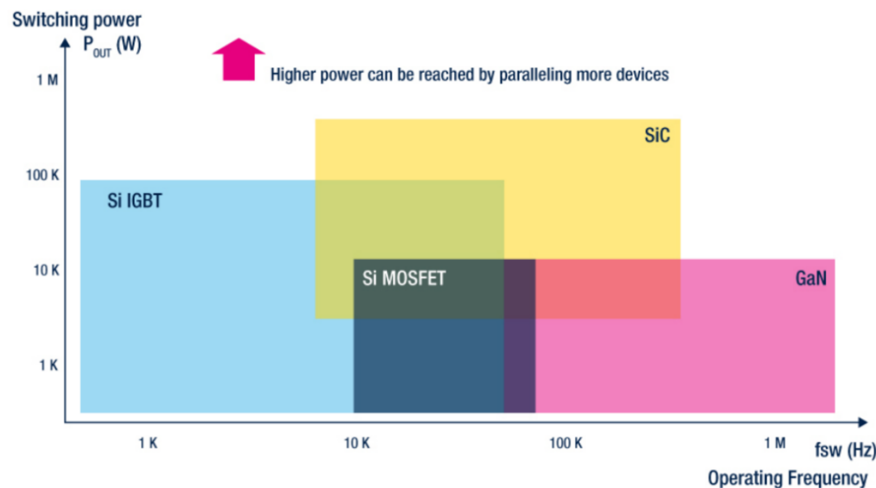

Figure 1. Application framework, based on output power and operating frequency, for Si-based IGBTs and MOSFETs, and SiC- and GaN-based power devices. Image from [3]

From the back-end side [21], integrated packaging solutions for WBG-based devices are gaining attention [22–24], because they can furtherly reduce the occupied area and, as a consequence, the power density. Nevertheless, the package integrity must be assured, also from a structural point of view [25]. In this thesis, a system in package (SiP) GaN-based power device is considered [2]. In general, monolithic integration solutions usually comprise half- or full-bridge topologies, the driver, the protection, and the control logic [26].

GaN-based power switches are usually surface-mounted devices (SMDs), i.e., they are directly soldered on the printed circuit board (PCB). Regarding the cooling, traditionally, the SMDs have been bottom-side cooled. There exist, in this case, several solutions to cool the device in the application, among them there are: PCB thermal vias, copper pads beneath the device, heatsink (if present) attached to the PCB bottom. Nowadays, double side cooled power SMDs are spreading. They have the exposed pad on the top of the package. In such a way, this solution is more advantageous because the heatsink can be directly attached to the top of the package, thus ensuring a more pronounced heat exchange. Then, also another heatsink would be present on the bottom side of the PCB. Regardless of the cooling systems used on the package and at the applications level, the heat removal from the GaN power device is critical, either for the die and for copper traces dissipation inside the package [4, 27–29].

Numerical simulations are today commonly used in industry frameworks, also in order to validate various design proposals, without spending time and cost on releasing many prototypes. These techniques are nowadays also widespread for power electronics [30, 31].

However, to the best of our knowledge, an integrated simulation approach, using finite element model (FEM)-based software packages, starting from electromagnetic output to calculate the temperature of interconnects, has not been proposed for power devices. The aim of the study is to calculate the copper traces temperature, induced by package electromagnetic self-heating by means of an integrated simulation. This approach is made by electromagnetic and thermal FEM. The electromagnetic FEM calculates the spatial distribution of power losses due to a dynamic current input at 500 kHz. The power losses geometrical output map is indeed exported in the post-process of electromagnetic FEM and imported in the pre-process of thermal FEM. The copper traces temperature is finally calculated considering the imported power losses' map as simulation input. This can be possible if an integration among the two physical environments is accomplished. The test vehicle considered in the thesis is a GaN-based 2SPAK SiP, from STMicroelectronics. The rest of the chapter is organized as follows: in the following section, the integrated simulation methodology is outlined, while in Sections 5.3 and 5.4, respectively, the electromagnetic and thermal simulation setups and results are shown and discussed. In the end, some conclusions are drawn.

5.2 Package Description and Integrated Simulation Methodology

5.2.1 Integrated GaN Package Description

A brief outline of the innovative package will be made in the following [26, 32]. As it was stated in Section 1, these solutions are becoming increasingly used in industry, for Si- and WBG-based power devices [23, 33–38]. The SiP solution, from STMicroelectronics, presented in this chapter has a 100 V breakdown voltage, and it is used in a 48 V–12 V DC-DC converter application. The package has been named 2SPAK and

comprises a half-bridge and the control logic. It allows, if the layout design is carefully addressed, a more compact solution, reducing the contribution of parasitic elements. In this case, vias connect GaN metals directly to the pads, reducing parasitic contribution and improving the thermal performance [32]. In addition, the PCB must also be designed in order to minimize parasitic elements, again, for EMI issues [39]. 2SPAK permits a bulk capacitor position, in PCB, a reduction of length interconnections [32]. In general, oscillations and overshoots must be minimized [40].

The package analyzed in this work is a bond-wire free one in order to improve thermal performances and reduce parasitic losses. It has an exposed slug on the top. Therefore, top side cooling helps the heat exchange, thereby making it possible to lower the system's thermal resistance or reducing the heatsink size.

5.2.2 Simulation Methodology Outline

In this section, a description of the method proposed in this work is given. FEM-based tools are used for both the steps considered in the analysis.

In the first phase, the computer-aided design (CAD) package geometry is used to make an electromagnetic finite element simulation using Ansys Q3D, thereby obtaining the current and voltage maps, and the output power map, as will be explained in more detail in Section 3. The last map represents the losses due to the Joule heating phenomenon in copper traces. It is the link between electromagnetic and thermal simulation due to the fact that such a geometrical map represents the output of electromagnetic FEM and the input of thermal FEM employed with COMSOL Multiphysics. Then, the same geometry is employed to thermally simulate the system, by imposing appropriate thermal boundary conditions, i.e., the

power losses' geometrical map and as discussed in-depth in Section 4. In Figure 2, a scheme of the proposed flow is depicted.

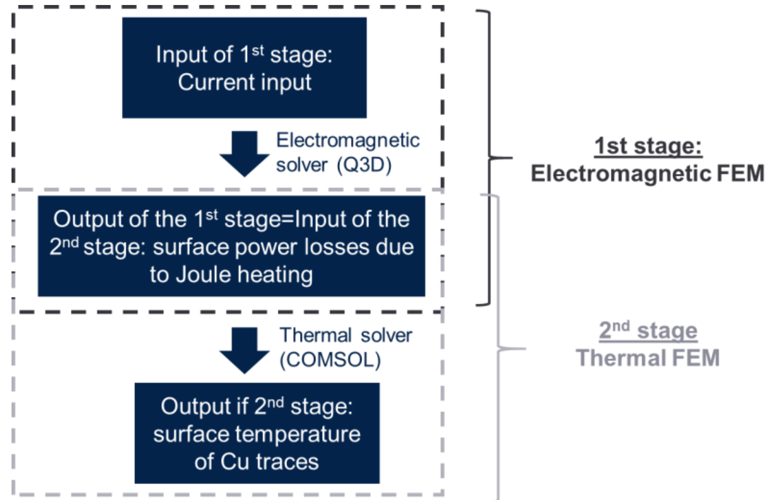

Figure 2. Workflow of the proposed method.

5.3 Electromagnetic Simulation

The used software for the electromagnetic simulation is Q3D Extractor, from Ansys, designed for those calculation types. In particular, by using this tool, it is possible to compute the current and voltage inside the package, as well as the parasitic resistive and inductive contributions at the chosen frequency. More specifically, Q3D Extractor allows to find out the equivalent resistance, inductance, capacitance and conductance network of a specific electronics product, that can be then exported to a like-SPICE environment. This software usually supports the design of electronics packages and connectors, thus permitting optimizing the electric performances [41].

5.3.1 Q3D Extractor Theory

Q3D Extractor solver considers the quasi-static approximations for Maxwell's equations. It can be assumed that when one of the first-order

time derivatives of electric and magnetic induction fields (but not both) is different from zero, the other one is negligible. The main consequence of this technique is that electromagnetic signals cannot propagate and the scalar fields at time t in a certain point P are only dependent on the electromagnetic sources' values at time t. This formulation can be used if it is established that the system length is much smaller in comparison to the wavelength associated with the maximum operating switching frequency of the power device. A general indication is that the structure dimension should be less than 1/10 of a wavelength that is inversely proportional to frequency. Considering that the simulations are carried out at a frequency f equal to 500 kHz and assuming c equal to the speed of the light in vacuum, the wavelength $\lambda = \frac{c}{f} \cong 0.6$ km is higher (much more than 10 times) than the maximum package dimension (approximately 10 mm), confirming the validity of the quasi-static hypothesis.

Moreover, the Q3D extractor solver distinguishes between "DC" and "AC" analysis [41]. In the case of DC analysis, both resistance and inductance are quite constant with the frequency. Quasi-static electric solver is employed for DC calculation. When AC analysis is considered, inductance decreases in comparison to DC value remaining not dependent by frequency. On the contrary, resistance increases with the root square of frequency and the quasi-static magnetic solver is considered. The physical reason is the eventual occurrence of the skin effect that reduces the effective cross-section for current flow, resulting in increased resistance and decreased magnetic field. A remarkable difference between DC and AC analysis is relative to the mesh. In the case of DC analysis, a three-dimensional tetrahedral mesh is needed to account for the current distribution for the DC case, meanwhile, a two-dimensional triangular

mesh is considered for the AC problem to model the whole current distributed on the conductor skin. Q3D software automatically chooses between DC and AC analysis. Fixing the frequency, if the conductor thickness is enough large (i.e., three times the skin depth) AC analysis should be carried out. Otherwise, if conductor thickness is lower than the skin depth, as in the specific case study, DC analysis results are most appropriate [41].

5.3.2 Electromagnetic Simulation Setup

The considered power dissipation is related only to copper traces losses. According to this, the device (die) is shorted, and it is modelled with conductive copper elements in this simulation. Hence, no Si and GaN die contributions have been considered in this simulation because the focus is on the interconnections. In Table 1, the material data, retrieved from suppliers, used in the electromagnetic simulation, have been reported.

Table 1. Material properties used for electromagnetic simulation.

Material	Simulated Objects	Relative Permittivity	Relative Permeability	Bulk Conductivity [S/m]	Dielectric Loss Tangent
Copper	Traces, vias, die	1	0.999991	58 × 106	0.02
Copper-CuFe2P	Lead-frame	1	0.999991	39 × 106	0.02
Sinter paste	Solder	1	0.99998	3.3 × 106	0
Encapsulant	Case	5	1	0	0.02

Figure 3 shows the considered package’s ports. In yellow, depicted are the seven ground ports in parallel, and in green the switch ports in parallel. As previously mentioned, the simulation is performed in DC at a frequency

equal to 500 kHz and fixing current at 90 A. As imposed by boundary conditions, the current travels from ground to switch ports.

This condition, which is very stressful in terms of current, will be considered as the case study for the import of power losses in the thermal simulation in the next section. The copper trace thickness is equal to 32 μm. According to the DC regime, as explained in Section 5.3.1, a three-dimensional tetrahedral mesh with adaptive refinement has been implemented.

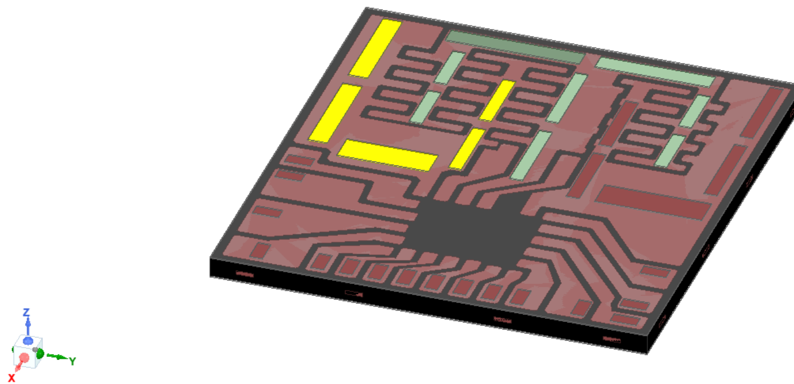

Figure 3. Electromagnetic simulation setup. In yellow, depicted are the ground ports in parallel and in green the switch ports in parallel.

5.3.3 Electromagnetic Simulation Results

Figures 4 and 5 show, respectively, the voltage map (V) and the surface current density (A/m^2), while Figure 6 depicts the volumetric loss density (W/m^3).

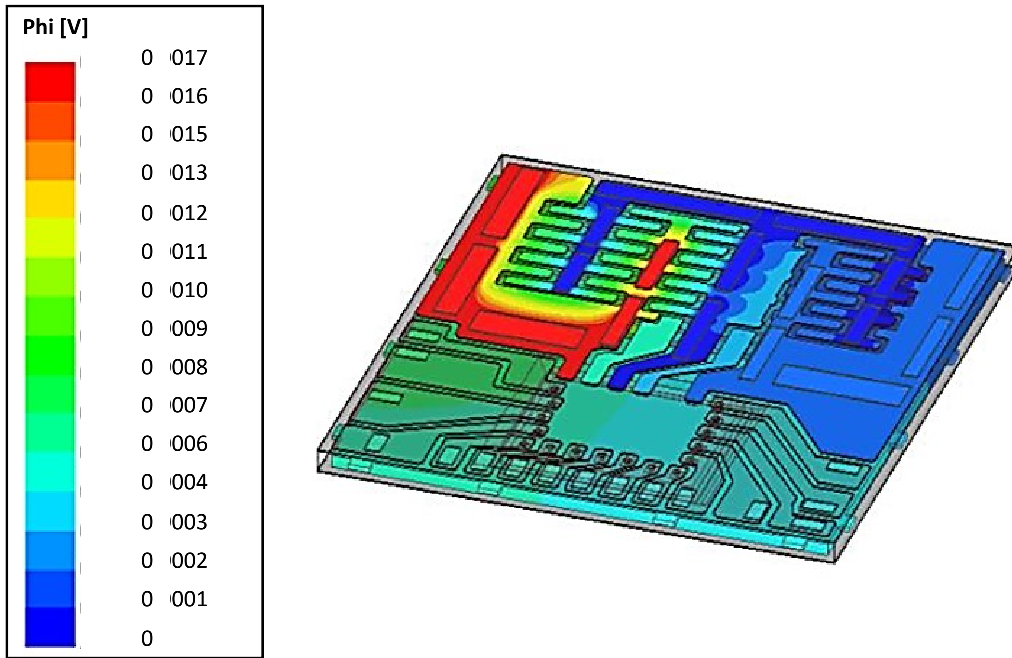

Figure 4. Voltage map, with a current equal to 90 A at 500 kHz as input.

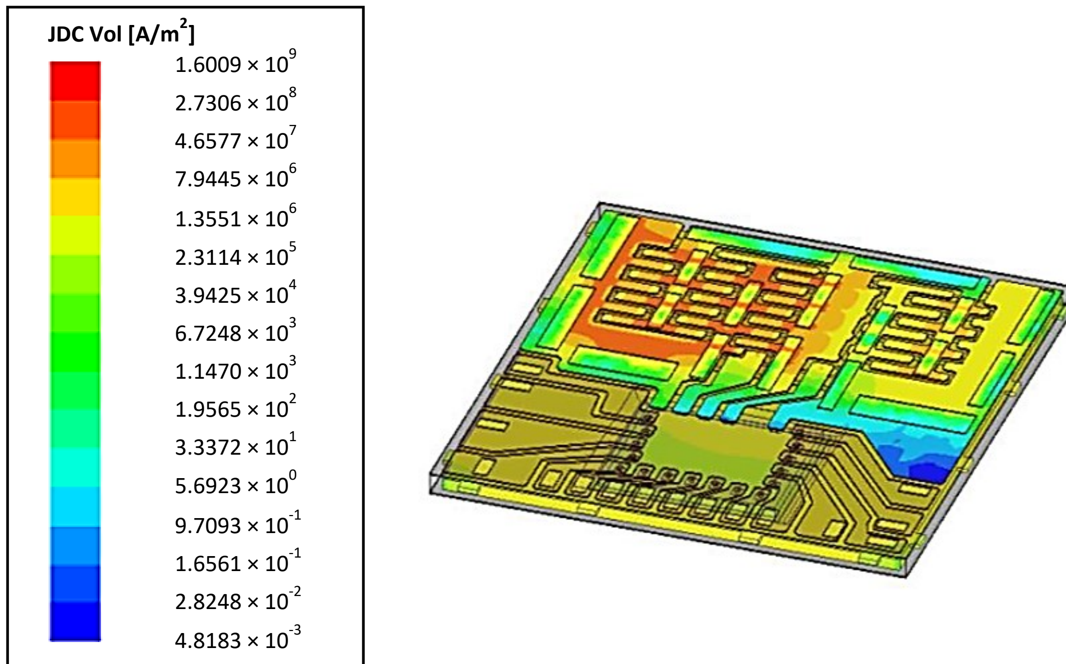

Figure 5. Surface current density, with a current equal to 90 A at 500 kHz as input.

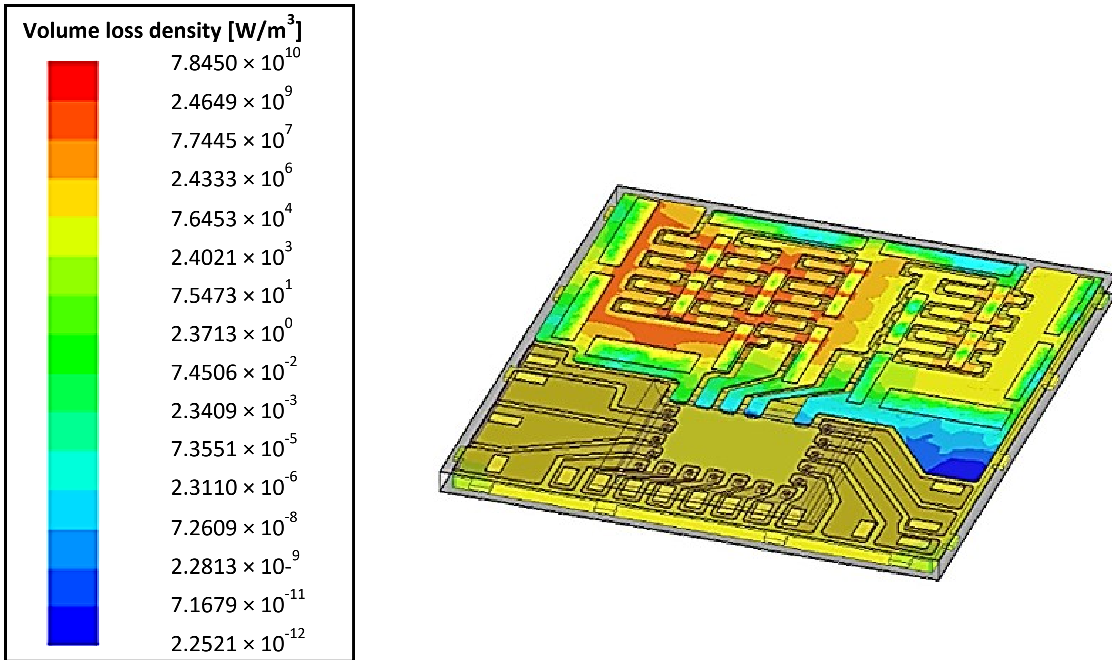

Figure 6. Volume loss density, with a current equal to 90 A at 500 kHz as input.

Regarding the voltage map, it is possible to see the voltage drop between the two poles of the conductive path, while from Figure 5 there are no particular current crowding phenomena. The most relevant power losses concentration is at the edges of copper pads due to geometry discontinuities in such places. Specifically, the volumetric loss density will be the input of the following thermal simulation. Then, the power loss geometrical map is exported in the thermal simulation, which has an identical geometry, point by point. The total amount of power losses is 0.46 W.

5.4 Thermal Simulation

5.4.1 Thermal Resistance Calibration and Model Simplification

As it was stated in sub-Section 5.2.2, surface power loss has been imported in the thermal simulation environment from the output of the electromagnetic simulation. More specifically, power losses have been mapped onto the geometrical xyz coordinates. This obtained association

has been exported in a dedicated text file that has been imported in the thermal simulation. The CAD model geometry must be exactly the same as the previous electromagnetic stage, in order to ensure the proper power loss mapping in both simulation environments. It is performed a steady-state simulation, by using the FEM-based COMSOL software, in order to obtain the temperature field inside the package.

In the first instance, thermal resistance $R_{th,j-a}$ at steady-state between junction (i.e., the chip) and ambient was calculated [4]. It was considered to place the package on a 1.6 mm-thick PCB with four copper layers, as depicted in Figure 7; a 100 µm-thick solder was interleaved between the PCB and the package. Convective heat flux was implemented as a boundary condition, with a convective coefficient equal to 10 W/m^2K that reproduces the heat exchange with still air at 20 °C. Heat power (1 W) was forced on the top junction surface. $R_{th,j-a}$ was finally calculated as the difference between the average junction temperature and air temperature (20 °C) and results equal to 40 °C/W.

In the following, and in the framework of the presented integrated electromagnetic-thermal approach, a simplified thermal FEM has been developed. In this last thermal model, PCB was not modeled in order to make the simulation simpler and quicker. An equivalent heat transfer coefficient has been searched for to be applied on the SiP-exposed pad in order to fit the Rth,j-a found in the previous and more detailed (i.e., with PCB) simulation (40 °C/W). The obtained equivalent heat transfer coefficient was 750 $W/(m^2\ K)$, not representative of real heat exchange with the air, being only a fitting parameter. Three-dimensional tetrahedral mesh is considered. In Table 2, the material properties or the simulated objects, retrieved from suppliers, are shown.

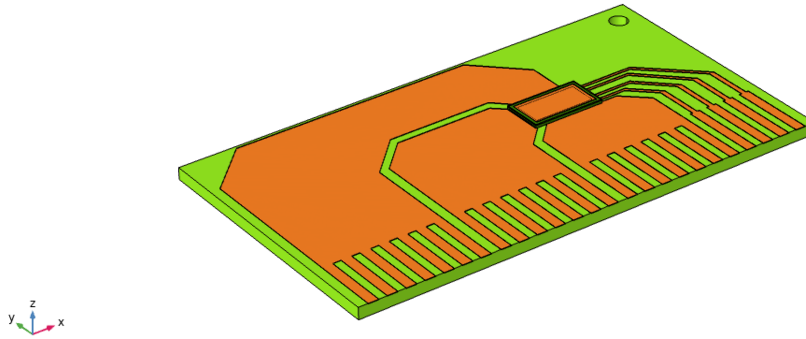

Figure 7. Implemented geometry for $R_{th,j\text{-}a}$ computation with printed circuit board and package.

Table 2. Material properties used for thermal simulation.

Material	Simulated Objects	Thermal Conductivity [W/(m K)]	Density [kg/m^3]	Heat Capacity at Constant Pressure [J/(kg K)]
Copper	Traces, vias, die	398	8960	385
Copper-$CuFe_2P$	Lead-frame	262	8920	385
Sinter paste	Solder	75	9520	460
Encapsulant	Case	0.79	2000	880

5.4.2 Thermal Simulation Results

Copper traces temperature map is the output of this simulation. Temperature and temperature swing are important parameters in the power device's and converter's operation. In fact, a safe thermal operation must be ensured for reliability needs. More specifically, the temperature swing is of paramount importance in this regard, and it must be kept at low values. Considering that the starting temperature is 20 °C, the temperature swing is equal to around 19 °C; in fact, the maximum temperature reached is equal to around 39 °C. A first-order check, to estimate the likelihood of the model, has been performed to calculate the $R_{th,j\text{-}a}$ obtained by dividing the

temperature swing induced by electromagnetic losses (19 °C) with the total dissipated power (0.46 W). The so-obtained $R_{th,j-a}$ is ~41 °C/W, quite aligned with the case in which a 1 W power dissipation occurs in the device. A thermal map of the internal part of the package is depicted in Figure 8. These temperature values are due to package surface losses, and they can assure the targeted SiP lifetime. Furthermore, there is quite a uniform temperature distribution in the package, and there are no critical hotspots in any part of the structure. This could be explained by the fact that copper traces are well spatially distributed inside the SiP. In the end, it can be possible to say that this current load is not critical for the thermal behavior of the copper interconnections in this GaN-based SiP.

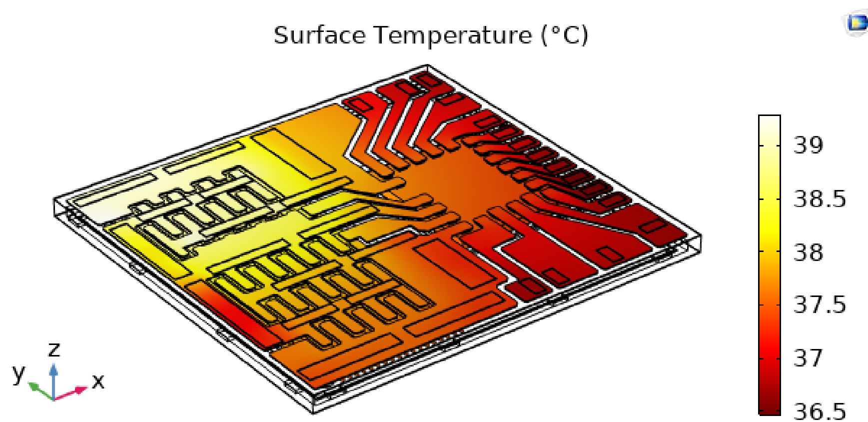

Figure 8. Temperature distribution inside the package. Temperature swing is equal to around 20 °C.

5.5 Conclusions

In this chapter, an integrated methodology, in order to study both electromagnetically and thermically an LV GaN SiP, called 2SPAK, is presented. The methodology considers only finite element-based simulations. The first stage of the flow relies on electromagnetic

computation, which is aimed at obtaining the surface power loss. Then, in the second stage, a thermal simulation has been performed with, as power input, the power losses'map calculated by the first electromagnetic simulation. The temperature swing due to copper losses is below 20 °C and does not represent an issue for package reliability, considering the elastic regime deformation of the copper layer, without any fatigue lifetime consumption. In future work, this methodology will be further exploited and extended in its capabilities, e.g., including die self-heating in the simulation.

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PART IV: SURFACE MOUNTED HIGH AND LOW VOLTAGE SILICON POWER DEVICES

6. MODELING AND THERMAL ANALYSIS OF COOLING SOLUTIONS FOR HIGH VOLTAGE SMD PACKAGES

This chapter has been taken (with some modifications) from the following published paper:

- **G. Mauromicale**, D. Nardo, A.Scuto, G. Sorrentino, L. Abbatelli, G. Scelba, G. Scarcella, "Modeling and Thermal Comparison of Cooling solutions for High Voltage SMD packages," *PCIM Europe 2021.*

In this chapter, an experimental investigation on thermal behavior of TO-LL, D2PAK, and H2PAK surface mount device (SMD) packages is presented, by considering different number of PCB layers, different copper pads number and thickness, and thermal vias number and diameter. Moreover, an effective thermal equivalent circuit model has been investigated and validated with the experimental measurements, obtaining a good compromise between accuracy and computational burden.

6.1 Introduction

As already said in previous chapter, regarding WBG-based devices, the thermal management plays an important role in high power semiconductor device packaging. In fact, the thermal resistance associated to the various package solutions is a very important measure for the cooling performance of the device, imposing the carrying power limits, the last related to power losses and junction temperature [1]-[4]. Innovative packages for Silicon (employing SJ technology for high-voltage structures) and WBG power

devices and modules would develop new system solutions both in industrial and automotive frameworks [5], [6]. The case of WBG MOSFETs and HEMTs has been already treated: instead, in this and in the next chapter, the focus will be on SMD-based packaged employing silicon-based devices. SMD-based [7] novel packages permit the reduction of the parasitic inductances associated with the long leads on packages like the TO-220 or TO-247, thus reducing the converter losses and switching stresses. However, thermal management of the present-day SMD-based power device designs still remains a barrier to efficiency, and several technical issues related primarily to thermal design need to be properly addressed in order to avoid a significant derating [8]. For this reason, the use of SMD devices was limited to medium and low power applications due to the cooling constraints.

Traditionally, through hole packages are mounted to a heat sink to dissipate the power loss of the device. On the contrary, top-side cooled SMD packaging solutions, such as TO-LL, D2PAK and H2PAK, can enable fast switching and high efficiency in reduced size and weight. In fact, for these packages it is not mandatory to use an heatsink, especially for low power applications. In the bottom side cooling case, thermal vias can be useful to reduce the system thermal resistance, helping to evenly distribute the heat into the board area, thereby enhancing the heat exchange [9]-[11]. Furthermore, also copper thermal pads can be used, either integrated in the package or added between the board and the power device package. Technical literature is rich of references concerning the thermal modeling and characterization of power semiconductor devices and cooling systems. In [1], a detailed analytical model is developed, taking into account all the heat transfer modes, aiming to thermal vias and thermal pads design optimization. Parametric optimization is based on the

following quantities: copper layers, number of inner and outer vias, via diameter, filling material, and spacing between vias. In [12], a thermal model of the system is proposed, based on a suitable thermal vias design, which relies on closed-form expressions to compute thermal resistance, including conduction and convection phenomena.

Finite element methods can provide high precision at the cost of slow computing speed [13]. However, in most cases, these simulations are also the benchmark to test analytical models. A different approach based on the use of equivalent RC thermal networks can be easily integrated into circuit simulators. These models provide an easy way to realize a synchronized electrical and thermal simulation. The drawback of equivalent RC thermal networks is the limited accuracy at high frequency or the high dissipation conditions. In most cases the thermal models consider the self-heating phenomenon [14], [15].

As beforementioned, among the new SMD packaging, D2PAK, H2PAK 7lead, and TO-lead less (TO-LL) can be considered the most diffused packages [4], [16]. The main purpose of the following analysis is to evaluate the thermal performances of TO-LL, D2PAK and H2PAK packages by considering different PCB layout configurations.

In the next sections, modeling and experimental validation will be addressed, also making a comparison between the results carried out with the two approaches

6.2 Thermal System Modeling

The identification of an equivalent thermal network for the estimation of the temperature distribution within the package has to kept into account different issues related to the thermal vias, which can be considered empty or filled with other thermally conductive materials such as copper or solder

[1]. Moreover, vertical and radial heat flows should be considered, even if, in a first approximation, the vertical one has been experienced to be the dominant one and thus will exploited in this section.

A suitable analytical thermal model has been devised in this chapter, representing a good compromise in terms of accuracy and computational burden. The model is a lumped-parameter approximation based on a limited number of resistive circuit elements, which accounts for conduction and convection resistances. A schematic of the the system layout is reported in Fig. 1, which also shows the thermal resistances that must be accounted to asses the lumped parameter thermal model of the system. With this scope, each equivalent thermal resistance will be computed either by using standard relationships available in the technical literature [1], [17]-[23]. The inputs required to model these resistances are the geometric and constitutive characteristics of the system layout, the power loss and the assumed ambient temperature; correspondingly, the model outputs will be the system overall equivalent thermal resistance and the case temperature.

In Fig. 1, $R_{J\text{-}C}$ models the thermal resistance between the junction and the case, which can be retrieved from datasheet. R_{PD} describes the conductive resistance that the power device opposes to the heat flow between the junction temperature node, T_J, and the top surface temperature node, T_S. This is followed by the convective-radiative resistance between the device top surface and the ambient air, $R_{S,top}$. It is worth noting that the equivalent resistance of these two terms is much greater than the resistance encountered in all the other parallel branches that act on temperature nodes T_a and T_J. Hence, this upper branch is commonly eliminated from the equivalent circuit [20].

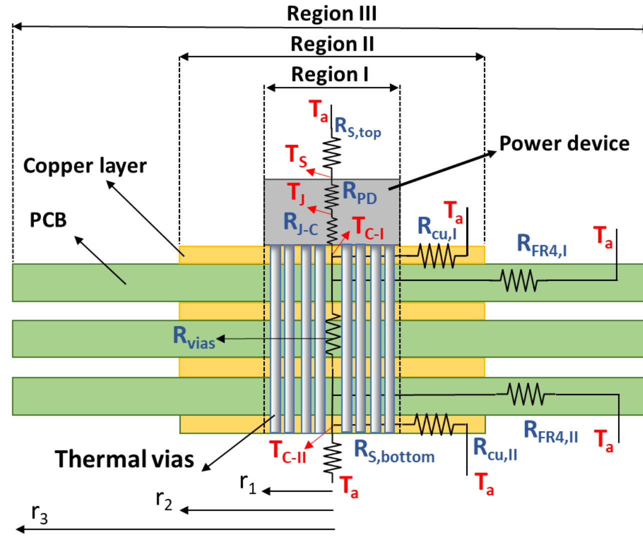


Fig.1 System geometry, with three regions considered in the formulas, and equivalent thermal resistances. The structure is not in scale.

The thermal resistance of the vias, R_{vias}, acts along the vertical symmetry axis of the system. In accordance with [1], this term is calculated as the equivalent thermal resistance of the parallel connection between the via filler (air or solder) and the vias copper plating at the walls, whose thickness is 25 μm in the set-up under consideration in the present study.

As this last equivalent resistance is much lower than the other terms discussed in the following, with the aim of simplifying the equivalent resistive thermal model, it will be neglected.

$R_{S,bottom}$ is the convective-radiative thermal resistance at the bottom surface of bottom of region *I*, which is uniformly connected to the top copper plate through the vias; hence, it can be assumed isothermal at $T_{C\text{-}II}$ and:

$$R_{S,bottom} = \frac{1}{\mathrm{hA}} \qquad (1)$$

The two elements $R_{Cu,I}$ and $R_{Cu,II}$ account for the combined conductive, convective, and radiative resistance of the copper annular regions exposed to natural convection and surrounding the power device and, respectively, the bottom area of Region-I.

In a similar fashion, the two elements $R_{FR4,I}$ and $R_{FR4,II}$ account for the combined conductive, convective, and radiative resistance of the FR4 annular regions exposed to natural convection; in this case these terms are computed with respect to area surrounding the top and bottom copper plate.

In order to draw an equivalent thermal resistance scheme, it is convenient to proceed to the fundamental model simplification that consists in neglecting the thermal resistance of the vias, R_{vias}, which is, in fact, much lower than any other term.

Hence, the equivalent thermal resistance circuit reported in Fig. 2 relies on this assumption and on the following consequent simplifications:

- $T_{C-I} \approx T_{C-II}$; hence, a unique temperature node potential, T_C, can be assumed for both top and bottom copper layers;
- the two elements $R_{Cu,I}$ and $R_{Cu,II}$ can be modeled as a unique element, R_{Cu}, that accounts for the conductive, convective and radiative heat transfer along the two region of the external copper layers that surround Region-I;
- similarly, the two elements $R_{FR4,I}$ and $R_{FR4,II}$ will be modeled by a single term, R_{FR4}, that accounts for the conductive, convective and radiative heat transfer along the top and bottom FR4 layers surrounding Region-II.

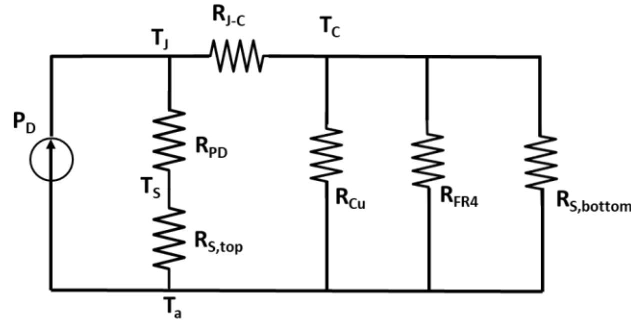


Fig. 2 Equivalent thermal circuit.

Considering the pseudo-square geometry of both the power device and the connected copper plate, a rigorous analytical description of R_{Cu} and R_{FR4} terms is not available; hence, in order to achieve an analytical description, the thermal profile that is established in the actual geometry can be approximated to the axisymmetric radial one that would arise in a circular geometry. The radius has been obtained by imposing an equal area for the actual geometry and for the circular one. Under this assumption, both these resistances can be estimated by adopting the solution originally derived for a single circular fin [17]-[23], that has been shown to hold for the thermal modelling of copper pads and PCB [17], [18]. These analytical solutions, expressed in terms of Bessel's expansion approximation, read as follows:

$$R_{Cu} = \frac{1}{2\pi k_{Cu} t_{Cu} a r_1}\left(\frac{K_1(ar_2)I_0(ar_1)+I_1(ar_2)K_0(ar_1)}{I_1(ar_2)K_1(ar_1)-I_1(ar_1)K_1(ar_2)}\right) \quad (2)$$

$$R_{FR4} = \frac{1}{2\pi k_{FR4} t_{FR4} b r_2}\left(\frac{K_1(br_3)I_0(br)+I_1(br_3)K_0(br_1)}{I_1(br_3)K_1(ar_2)-I_1(ar_2)K_1(br_2)}\right) \quad (3)$$

with:

$$a = \sqrt{\frac{N_{Cu} \cdot h}{k_{Cu} \cdot t_{Cu}}} \;\; ; \;\; b = \sqrt{\frac{N_{FR4} \cdot h}{k_{FR4} \cdot t_{FR4}}} \qquad (4)$$

In these equations, k_{Cu} and k_{FR4} are the thermal conductivity of copper and FR4, respectively, whereas t_{Cu} and t_{FR4} are the thickness of their external layers, exposed to natural convection; r_1, r_2 and r_3, are the equivalent radii delimiting the annular regions used to approximate the pseudo-sqare footprint of the region of the copper layer and of the PCB surrounding the power device and, respectively, the copper layer. I_0 and I_1 are the modified Bessel functions of the first kind, order zero and one, respectively, while K_0 and K_1 are the modified Bessel functions of the second kind, order zero and one, respectively.

Parameters a and b depend on N_{Cu} and N_{FR4}, the number of copper and FR4 annular surfaces exposed to natural convection, which are then both $N_{Cu}=N_{FR4}=2$ for the present study. Moreover, they depend on the heat transfer coefficient, h, is the heat transfer coefficient accounting for both convection and radiation at the surface of the element. A reliable evaluation of this parameter represents a major issue; in fact, it can be considered as the sum of two coefficients: i) the convective heat transfer coefficient, h_{conv}, and a radiadive heat transfer coefficient, h_{rad}. The coefficient h_{conv} mainly depends on temperature in natural convection whereas in forced convection it mainly depends on the air velocity imposed by the fan. Typical range of variation are:

- 8-20 W/m^2K in natural convection in (still) air;
- 100-200 W/m^2K in forced convection with air;
- 1000-2000 W/m^2K in forced convection with water.

In the range of temperature of the application under study, the radiative heat transfer coefficient h_{rad} represents a reliable and symple way to linearise the radiative heat transfer, which, otherwise, should be expressed as a function of the fourth power of the absolute surface temperature. Therefore, in the following analysis, typical heat transfer coefficients for the three regions have been supposed, calibrating them by comparing simulations with the experimental measures. This choice leads to set h= 18 W/m^2 K in eq. (1), h= 15 W/m^2 K in eq.(2) and h= 12 W/m^2 K in eq. (3).

As all the thermal resistances in the equivalent thermal circuit in Fig. 2 can be evaluated either from datasheets or by the reported analytical solutions, the equivalent total board to ambient thermal resistance can be calculated

$$R_{thj-amb} = R_{J-C} + R_{Cu} \,//\, R_{FR4} \,//\, R_{S,bottom} \qquad (5)$$

The above expression has been obtained by suppressing the contribution of the upper branch to the overall heat transfer, as the equivalent thermal resistance due to the series $R_{S,top}$ and R_{PD} [20].

6.3 PCB Realization and Experimental Results

A simple experimental setup is used to thermally characterize different cooling solutions. Several daughter boards have been realized and used to compare different configurations. In particular, Figs. 3 and 4 show, as an example, two considered configurations with different vias number and diameters, while Fig. 5 depicts the circuit scheme of PCBs utilized during the experimental tests.

The copper area is 168 mm^2 for each layer, while the entire PCB area is 5 cm x 3.6 cm. Four PCB layouts have been considered for each package. The first comprises 2 layer, 35 µm copper thickness, 0.3 mm vias diameter. The second has 2 layer, 70 µm copper thickness, 16x16 vias with 0.3mm diameter vias.

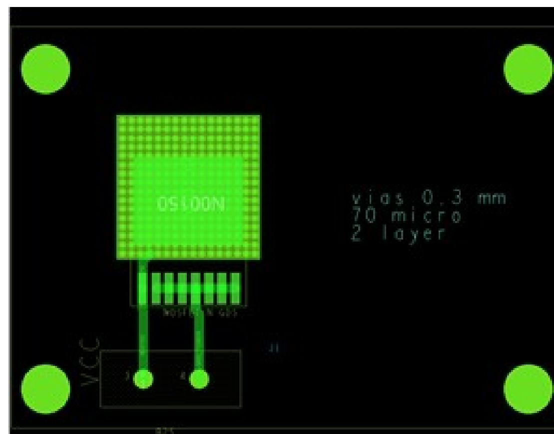


Fig. 3 Layout with TO-LL package, vias with diameter of 0.3mm and 70 µm thickness, two copper layers.

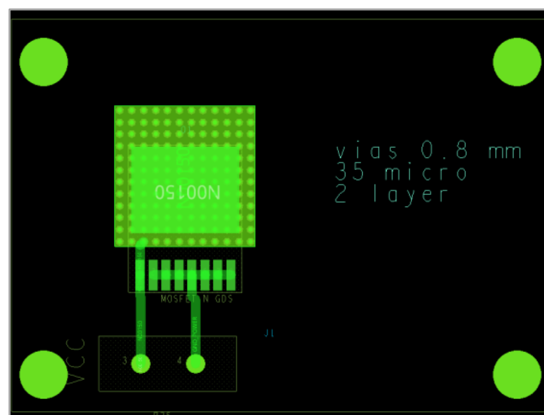


Fig. 4 Layout with TO-LL package, vias with diameter of 0.8mm and 35µm thickness, two copper layers.

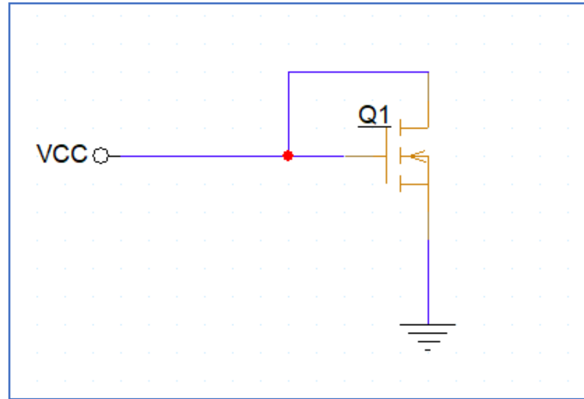


Fig. 5 Circuit scheme of the experimental boards.

The third layout has 2 layer, 35 µm copper thickness, 12x12 vias with 0.8 mm diameter. Finally, the fourth board type features 4 layer, 35 µm copper thickness, 16x16 vias with 0.3 mm diameter.

The experimental setup aimed at the thermal characterization consists of the daughter board under test, in which the device gate and drain are connected to the V_{cc} provided by an external power supply, as it can be seen in the Fig. 5. A photo of the experimental setup is shown in Fig. 6. The case temperature is measured by using a FLIR E30 thermo camera. The ambient temperature has been continuously monitored, and its value has been kept at around 25 °C. Three different operating points have been considered for each layout, measuring the temperature and corresponding drain currents and drain to source voltages, allowing to evaluate the dissipated power by each SMD device.

By measuring the ambient and case temperatures, T_{amb} and T_c by means of the infrared camera, and computing the dissipated power P_d as the product between the drain-source voltage and drain current, the equivalent resistance of the circuit can be estimated by:

$$R_{thj-amb} = \frac{T_C + (P_d \cdot R_{thj-c}) - T_{amb}}{P_d} \quad (6)$$

The Figs. 7-8 show the values of the equivalent thermal resistance versus the dissipated power, for two of the four considered cases, while some numerical results of the measured quantities for the four PCB cases studied are showed in Table 1. In this table, a thermal comparison among the four cases is given, by indicating the case temperatures and the experimental thermal resistance. It can be noted that the lowest thermal resistance value is obtained with the second considered configuration. Figs. 9-10 displays some thermal images of power devices under tests, underlying the temperature distribution around the chip and PCB. These thermal maps clearly show the temperature distributions in copper pad, PCB, and package regions. It can be noted that the higher temperature is in the package region, but also copper layers and part of the PCB reach high values, hence also these parts contribute to the heat exchange.

In Table 2, a comparison among the three packages considered in this work is given, in order to compare the measurement results in the analyzed board cases. The analysis shows that the best PCB layout, allowing to extract the major thermal power flow, is realized with 2 layer, 70 μm copper, 16x16 vias with 0.3 mm diameter. Moreover, by comparing the results related to the 2-layer configuration with different vias diameter (0.3 mm and 0.8 mm), it is highlighted that larger vias allows a better thermal dissipation.

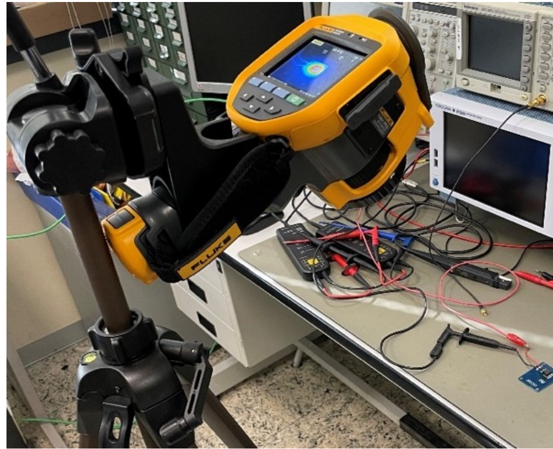


Fig. 6 Experimental setup.

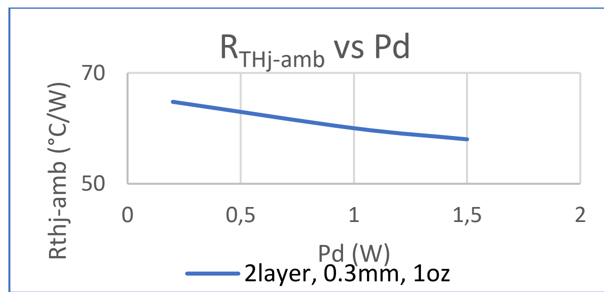
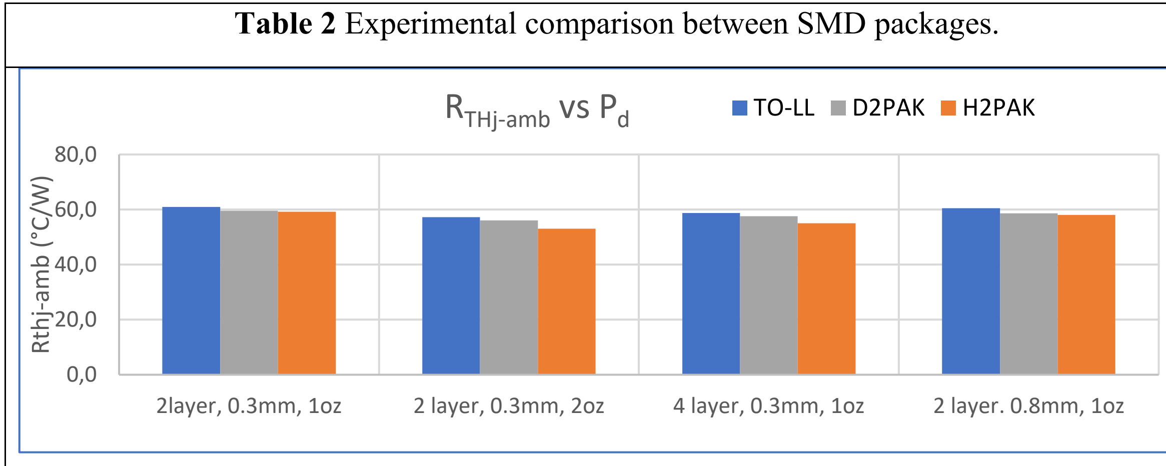


Fig. 7 Thermal resistance experimental values, 2-layer copper planes, thickness 35µm, thermal vias diameter equal to 0.3 mm.

Table 1 Experimental thermal values for TO-LL package.

2 layer, 0.3 mm, 1 oz			2 layer, 0.3 mm, 2 oz			4 layer, 0.3 mm, 1 oz			2 layer. 0.8 mm, 1 oz		
P_{diss}	T (°C)	Rth_{j-amb} (°C/W)	P_{diss}	T (°C)	$R_{thj-amb}$ (°C/W)	P_{diss}	T(°C)	$R_{thj-amb}$ (°C/W)	P_{diss}	T(°C)	$R_{thj-amb}$ (°C/W)
0,172	36	64,783	0,183	36	60,873	0,184	36,5	63,33	0,187	37	65,208
0,87	76,5	60,025	0,84	70,9	55,473	0,824	71,4	57,141	0,858	75,40	59,571
0,329	101	58,016	1,365	99,5	55,409	1,362	100	55,896	1,38	102,00	56,627
Average $R_{thj-amb}$		60,942			57,252			58,789			60,469

Table 2 Experimental comparison between SMD packages.



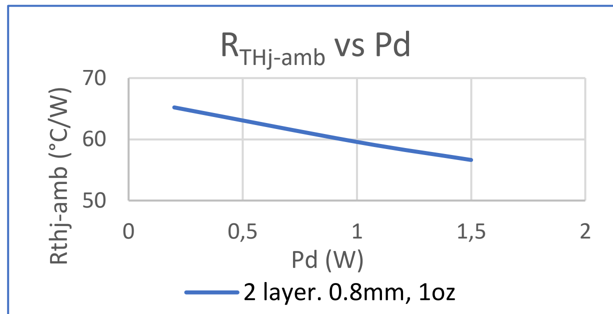


Fig. 8 Thermal resistance experimental values, 2-layer copper planes, thickness 35 µm, thermal vias diameter equal to 0.8 mm.

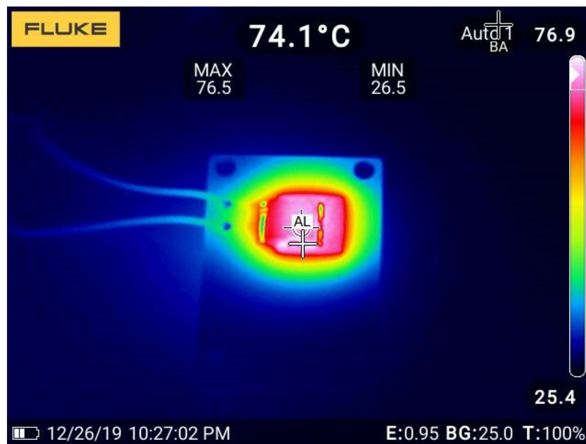


Fig. 9 Thermal map of TOLL, 2-layer copper planes, thickness 1oz, thermal vias diameter equal to 0.3 mm.

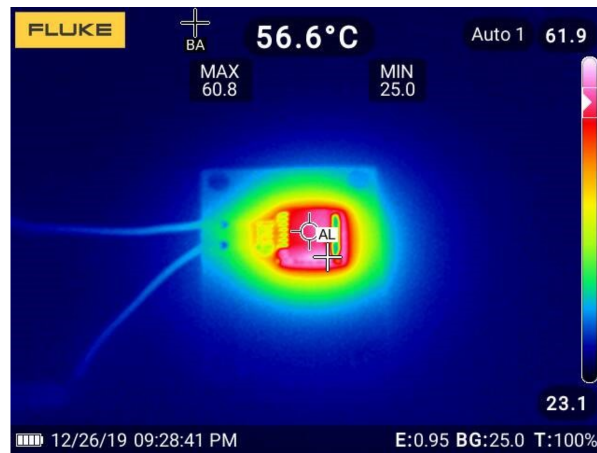


Fig. 10 Thermal map of TOLL, 2-layer copper planes, thickness 1oz, thermal vias diameter equal to 0.8 mm.

6.4 Comparison Between Experimental and Model Results

Although of general validity, the proposed model has been applied to the thermal analysis of the TO-LL package. The comparison between experimental data and analytical results is reported in Table 3, for the layout realized with two copper layers, 35 µm thickness, and thermal vias diameter equal to 0.3mm. The table lists the measured (T_{meas}) and analytical (T_{ana}) case temperatures evaluated at three different dissipated power operating conditions. A good agreement can be observed between the experimental data and that predicted through the analytical model. In fact, the error between measured and model data is less than 3%.

Table 3 Comparison between experimental and modeling results.

TO-LL package	2 layer, 35 µm,0.3mm vias diameter		
Measured power points	**P (W)**	**$T_{experimental}$ (°C)**	**$T_{modeling}$ (°C)**
Point one	**0,172**	**36**	**35.2**
Point two	**0,87**	**76,5**	**76,4**
Point three	**1,33**	**101**	**103,5**

6.5 Conclusions

This study analysed the experimental thermal behaviour of SMD TO-LL, H2PAK, and D2PAK packages, by means of a suitable set of characterization boards, and addressed the assessment of a lumped-parameter thermal model. The main advantage of the modelling approach consists in the simplicity of implementation and in the low computational burden, which is obtained through a limited number of simplifying assumptions. Nonetheless, the comparison between experimental tests and model results highlights satisfactory accuracy of the model prediction.

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7. MULTI-PHYSICS MODELS OF A NOVEL LOW-VOLTAGE POWER SEMICONDUCTOR SYSTEM-IN-PACKAGE FOR AUTOMOTIVE APPLICATIONS

This chapter is treated (with some modifications) from the following paper, submitted to *IEEE Transaction on Transportation Electrification*:

- **G. Mauromicale,** M. Calabretta, G. Scelba, G. Scarcella, A Sitta, "Multi-Physics Models Of A Novel Low-Voltage Power Semiconductor System-In-Package For Automotive Applications," submitted to a *IEEE Transactions on Transportation Electrification*.

This chapater analyzes, by means of finite-element simulations, a low-voltage power semiconductor system-in-package devoted to automotive applications, which integrates a MOSFET-based half bridge and a controller. Three simulation physical domains integrated in a unique flow are considered: thermo-mechanical, electromagnetic, and thermal numerical models. The aim is to develop a new comprehensive methodology which starts with a thermo-structural simulation of the package, then computes the on-state resistance and parasitic components to assess the electrical behavior of the package. Finally, a simulation check is made to verify if the power device performances are thermally consistent with applicative conditions.

7.1 Introduction

As already explained in previous chapters, innovative power semiconductor devices are gaining attention from both academic and industrial communities, for novel applications in industrial and automotive frameworks. Both hybrid and full-electric electric vehicles markets are rapidly growing [1]. Furthermore, renewable energy sources require an efficient and robust electronic power unit to properly convert the power delivered to the grid. Hence, both power device and package technological improvements are mandatory. Low-voltage (LV) power devices are employed in the first application, while high voltage (HV) devices are used for high-power HV applications such as traction or charging converters. For LV devices, silicon (Si) technology is traditionally considered for this kind of applications [2]-[4]. Although wide band-gap materials, such as silicon carbide (SiC), and gallium nitride (GaN), are spreading in LV and HV automotive applications [5], as it has been proved in this thesis for these two materials in previous Parts, Si-based devices will still have, in the next years, a large market share in semiconductor industry, also with new developments, among which there are induced avalanche operation and distributed shield resistance [6]. While HV silicon MOSFETs have been considered in the previous chapter, the LV structures will be the subject of this one. LV range is considered roughly from 30 V to 100 V, and the chosen breakdown voltage, for a specific device, depends strongly on the specific applicative requirements, i.e. the required operation voltage of the converter in which the device is inserted. In nominal operation, typically these packages must withstand high currents in the order of several tens of A. Therefore, achieving a very low drain-source on-state electric resistance power device is fundamental to ensure the proper efficiency.

The applications of LV power semiconductor devices would be several, in many fields. Among the relevant ones, there are: voltage regulator modules for power factor correctors or motherboards in data centers with higher efficiency and power density and in automotive framework, auxiliary DC-DC converters in electric vehicles, point of load converters, motor control applications, electric power steering, and electronic parking brake [7]-[9]. A brief recall of technologies for LV power devices is given in [10], [11]. While in HV field Si MOSFETs the super-junction structures are currently the most used, the trench-gate technology of Si LV devices is nowadays the one employed in almost all semiconductor industry [12]. The design phase of these switches is related to the packaging and to the compatibility between the package (back-end) and the semiconductor device (front-end). In this context, modeling and simulation strategies in the design stage are of paramount importance, because they can evidence issues at an infant stage, reducing the costs and the time to market, and permitting the comparison among different design options in a quick way. Design adjustments can be easily evaluated by means of specific simulation software, which usually employ finite element method (FEM). In this way, the need of too many physical prototypes can be avoided, saving costs and development time [13], [14]. FEM are useful for thermal analysis, also to identify abnormal operations, which are usually required to be sustained; among these there are avalanche phenomenon, short circuit, and linear mode operation [15], [16]. However, in this work only stationary thermal simulation will be considered, as it is important in a first order evaluation of the device's behavior. Reliability is another primary requirement for several power device applications [17], [18], especially for harsh environments such as the automotive one [19], [20]. In general, there exist

techniques which can fully support package's reliability optimization during the engineering phase. Such methodologies can be experimental and numeric, or a mix of them, e.g. in the case of simulations ran in parallel with experimental condition monitoring methods, that assess the device health state during the normal operation in applicative field [21], [22]. With reference to manufacturing phase, the processes related to fabrication, such as die attach, molding, and attach on printed circuit board (PCB), are of paramount importance [23]. In fact, a weak solder joint reliability results in a weakness of the whole package.

The aim of this chapter is to give an overview of the various physical issues that can be encountered in the design phase of a LV system-in-package (SiP) [24], integrating two Si-based trench-gate power MOSFETs in the half-bridge configuration, that is with low side (LS) and high side (HS), together with gate drivers, diagnostic, and protections circuitries. The SiP is designed for automotive applications, such as DC/DC switching voltage regulators for CPU and memory supply (synchronous step-down DC/DC converters). In literature, several valid simulation approaches are addressed, but they usually do not consider either mechanical, electromagnetic, and thermal physics in a unique flow, that is with various simulations for a unique design of the power device [13], [25]-[28]. In some cases, more comprehensive, i.e. multi-physics, approaches have been developed, see for example [14], [23], [29]. However, there are differences with this chapter will present. In [23], the main focus is on the simulation of die-attach joints fatigue. Instead, in [14] the aim is related to application-like and converter-level power module's assessment, in fact the package-related thermo-structural simulation is not executed, while in the present analysis this aspect is very important. With reference to [29], in that work

parasitic simulation is not present, experimental electric benchmark is not addressed, and resin glass transition is not modeled. Hence, this work, in comparison to previous studies, will give a novel methodology to perform simulations focused on the package, involving electromagnetic, mechanical, and thermal physical domains.

The reason to develop the simulation flow explained in the following is to give a complete and sufficiently detailed insight for the various physical domains of the device's design process. The methodology starts from a thermo-mechanical simulation, which has the aim of providing a comparative evaluation between different packaging designs from a structural point of view. More specifically, the output of this simulation will be the cumulated plastic work inside the solder joints, useful to forecast the package's lifetime. Then, an electromagnetic simulation is executed to identify the parasitic elements and the drain-source on-state resistance. The electrical model is able to distinguish the various resistive components. At the end, a thermal simulation is necessary to assure that the device can withstand a thermal load and application-like boundaries, thereby assuring a safe operation. Fig. 1 depicts the FEM-based simulation workflow exploited in the following study.

The rest of the chapter is organized as explained in the following. In Section 7.2, a brief outline on the package issues in LV devices and the simulated one is given, while Section 7.3 deals with thermo-structural simulations, including a simulation case-study. Sections 7.4 and 7.5 describe, respectively, the electromagnetic and thermal simulations, while in the last Section some conclusions are drawn.

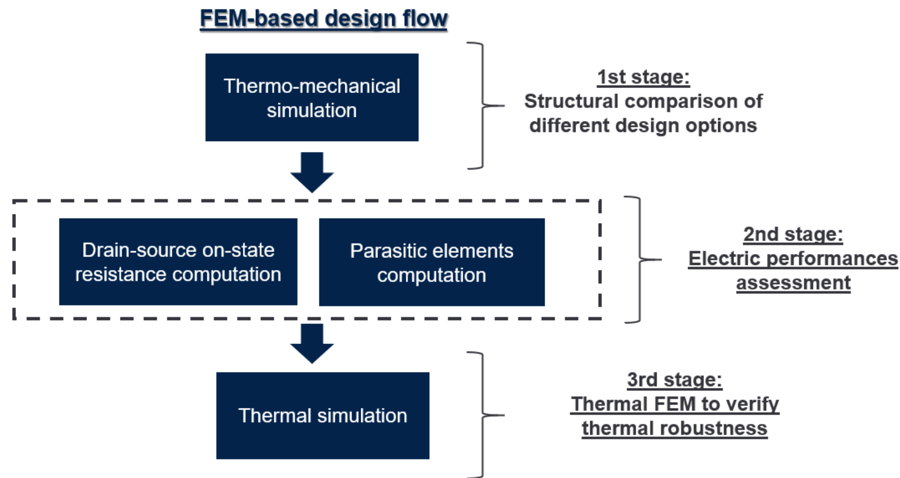

Fig. 1 Proposed FEM flow for robust design of LV package.

7.2 Package-Related Features In LV Devices

In this paragraph, some aspects related to LV packages will be briefly outlined. The miniaturization of innovative LV power devices is increasing more and more in last years, thereby permitting a more evident power density increase in power electronic converters [30]. This result can be achieved also because these power MOSFETs are surface-mounted devices (SMDs), directly soldered on the board [28], like the package presented in this chapter. From the LV back-end point of view, in recent years two main novelties have arisen in industry: the integration of more switches and/or control circuitry, and the adoption of copper clips in substitution of the classic wire bonds [11], [31]. Regarding the integration, SiP solutions are gaining an increasing attention [32]. They can include, for example, an integrated half bridge, and, optionally, the gate driver control logic, as in the case of the package presented in this work. Figs. 2 (a) and (b) display, respectively, the 3D external visualization and the 3D CAD model of the simulated SiP, without resin and highlighting LS and HS. With regard of the electric properties, the SiP has a breakdown voltage of 30 V, a

maximum output current capability equal to 50 A, and a switching frequency up to 1.5 MHz. Moreover, protections and sensing circuits are both present. In this way, a more compact solution can be reached, and a higher switching frequency operation can be assured in final application. In line to this, packages thickness is continuously shrinking in this kind of power devices. Additionally, MOSFETs have an integrated body diode inside. In fact, another possible application of LV devices lies in synchronous rectification framework. Nowadays, electrical performances must be assured in final application. In this regard, the electric resistance is strictly related to the conduction power losses. Instead, the other principal type of losses in power semiconductors is due to turn-on and turn-off transients, i.e. the switching power losses, strongly dependent from the operating switching frequency [11]. Higher switching frequency is currently employed because of the stronger device capabilities. It can lead to passive components (such as inductors) and filters size reduction. However, parasitic inductances (overall the stray, or source, contribution), as well as internal capacitances, coupled with higher ramps of currents and voltages, can lead to overshoots and oscillations [33]. In this context, low inductance packages are needed: for this purpose, leadless or quad flat no-lead (QFN) packages have been developed.

The LV packages structure usually comprises silicon die, solder, wire bonding or clip, and a copper leadframe (LF), which includes the external leads. Source clip-based devices, also called wire bond-less ones, can enhance electrical performances, in comparison to the classic wire-bond solution, reducing the resistive contribution [29] and improving reliability performances by the depletion of bond-wire liftoff failure mechanisms

[34]. In the simulated package, two clips are present for the connections of the two MOSFETs, as depicted in Fig. 2 (b).

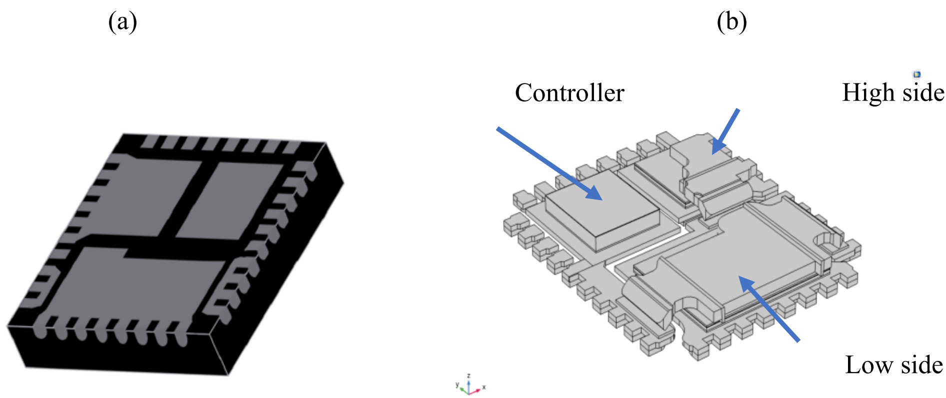

Fig. 2. (a) Simulated device; (b) CAD model, without molding compound,

7.3 Thermo-mechanical analysis

7.3.1 Problem formulation

Reliability-related assessments are often performed employing dedicated tests that enhance application-related failure modes. Test conditions are designed in order to accelerate wear-out occurrence with respect to typical mission profile [35], [36]. One of these experiments are passive thermal cycles, which are aimed to verify solder joint reliability. This procedure can be also simulated by finite-element based codes. In this framework, a thermal cycle between -65 and 150 °C is considered, with 1 hour duration, will be employed in this chapter. The coefficient of thermal expansion (CTE) is an important quantity carried out in these tests, allowing the evaluation of the stresses in power semiconductor packages, because CTE different values among the various components (e.g., between molding compound and PCB) can induce stress in structures [27]. Voids, cracks, or delamination phenomena can affect the thermal

performances, and the mechanical reliability of the entire package. The Anand visco-plastic model is employed in the simulation proposed in this chapter: this is a non-linear constitutive model for solder compounds chosen to model the solder inelastic behaviour [37]. Both time-dependent and time-independent inelastic strain phenomena are considered in this model, related to creep and plasticity [38]. The basic equations of the Anand model, here briefly recalled, are [39]:

$$\dot{\varepsilon}_p = A \exp\left(\frac{Q}{RT}\right) \left[\sinh\left(\xi \frac{\sigma}{s}\right)\right]^{\frac{1}{m}} \quad (1)$$

$$\dot{s} = h\,(\sigma, s, T)\,\dot{\varepsilon}_p = \left[h_0 \cdot \left|1 - \frac{s}{s^*}\right|^{a} \cdot sgn\left(1 - \frac{s}{s^*}\right)\right]\ \dot{\varepsilon}_p \quad (2)$$

$$s^* = \hat{s}\ \left[\frac{\dot{\varepsilon}_p}{A} \exp\left(\frac{Q}{RT}\right)\right]^{n} \quad (3)$$

where $\dot{\varepsilon}_p$ is the non-elastic strain rate, A is the pre-exponential factor, Q is the activation energy, R is the gas constant, T is the absolute temperature, ξ is the stress multiplier, σ is the equivalent (Von-Mises) stress, s is the state variable that represents the material resistance to the plastic flow, m is the strain rate sensitivity, h_0 is the hardening constant, h is the hardening function. s^* is the saturation value of the deformation resistance and it is expressed in (3), where a is the hardening strain rate sensitivity, $\hat{s}$ is the saturation coefficient, and n is the sensitivity of the strain rate for the saturation value of the deformation resistance. The nine parameters appeared in the above equations are resumed in Table I. The numerical values used in this work are taken from [40].

From the visco-plastic model, knowing the cumulated plastic work, is possible to estimate the cycles to failure number. Regarding the thermal fatigue lifetime prediction of chip solder joints, there exist various methods. The Darveaux method will be used in the design comparison made in this work. It relies on the following relationships, that compute the number of cycles to failures considering the initiation and the propagation of the cracks inside the solder parts [27] [26], [39]:

$$N_F = N_0 + \frac{l_0}{\frac{dl}{dN}} \tag{4}$$

$$N_0 = K_1 \, (\Delta W)^{K_2} \tag{5}$$

$$\frac{dl}{dN} = K_3 \, (\Delta W)^{K_4} \tag{6}$$

where N_F is the lifetime number of cycles, N_0 is the cycles number to crack starting, l_0 is the characteristic length of the solder joint, $\frac{dl}{dN}$ is the rate of crack propagation, $K_1=37.97$ *cycles/*MPa^{K_2}, $K_2=-2.8$, $K_3=1.4e-3$ *mm/(cycles* $\cdot MPa^{K_4}$*)*, and $K_4=1.16$ are empirical constants (numerical values are from [37]), while ΔW is the visco-plastic work accumulated in a passive cycle. In this simulation, l_0 has been chosen equal to the solder length. One of the main aims of this kind of simulations is the board level reliability (BLR) assessment, together with that related with the internal solders [39]. BLR is important because it can provide information about the mechanical robustness of the solders, which usually are tin (Sn)- silver (Ag)- copper (Cu)-based (SAC), used to connect the package to the board.

For this reason, a BLR simulation is performed, as it will be detailed in the next sub-section.

Table I Anand parameters

Symbol	**Description**	**Measurement unit**	**Numerical values (from [55])**
A	pre-exponential factor	s−1	3501
Q/R	Arrhenius term	K	9320
$\hat{s}$	saturation coefficient	MPa	30.2
ξ	multiplier of stress	dimensionless	4
m	strain rate sensitivity	dimensionless	0.25
h_0	hardening constant	MPa	180000
s_0	deformation resistance initial value	MPa	21
n	strain rate sensitivity of saturation	dimensionless	0.01
a	strain rate sensitivity of hardening	dimensionless	1.78

7.3.2 Simulation case study

The goal of the simulation, performed in COMSOL Multiphysics 5.6, is to predict the number of cycles to failure, in order to identify the most critical solder layers from a structural point of view. Because the trial is based on BLR, external solder joints will be focused. The properties of materials used in the simulation are reported in Table II. The simulated solders compounds are SAC (lead-free), for soldering the package on the board, and PbSnAg-based solder for die and clip attachments, inside the package. Glass transition of the resin is modeled in the simulation, taking into consideration that at this temperature (equal to 120 °C) the Young

modulus of molding compound significantly decreases, from 27.4 GPa to 1 GPa. In addition, CTE is increased from 10 ppm/K to 38 ppm/K.

Glass transition leads to an additional stress on the solder that can be seen on the visco-plastic energy dissipation. The main part of visco-plastic energy density is accumulated during the temperature transitions inside the cycle. The model has been validated in a previous work by the authors [27]. Briefly, the number of cycles at which crack starts and the crack propagation in solder layers have been monitored by employing a passive temperature cycle and performing periodically (500 cycles) scanning electron microscopy on cross-sections to detect crack initiation and evolution.

In the following, some model features (including the package's manufacturing) have briefly recalled. Pre-stress phase from 300°C to -65 °C is employed to reproduce thermal stress from assembly process [41]. Firstly, mechanical stress coming from die attach process is produced cooling the device from die attach stress-free temperature (PbSnAg melting point) to room temperature (RT). Then, die attached on leadframe is heated at molding temperature (180 °C). Molded package is cooled at RT and heated at 220 °C, which is the PCB attach stress-free temperature (SAC 305 melting point). Finally, packaged attached on PCB is cooled at -65 °C, the initial temperature of thermal cycle.

According to experimental characterization analysis (dynamic mechanical analysis), it has been measured the storage modulus of the resin versus temperature, as well the CTE versus temperature trend. Four thermal cycles have been implemented, because they are sufficient to assess that the visco-plastic dissipation in one cycle is stabilized to a constant value. The package is considered as assembled on PCB. For each cycle, the

temperature has a range between -65 °C to 150 °C, while the duration is equal to one hour, and dwell and ramp times are equal to fifteen minutes.

In Fig. 3, there is a focus on a solder joint and on a corner pad: the two CAD elements are highlighted in red. Corner pads, placed at the four corners of the package, can be useful to improve the structural features of the power device. In this case study, the QFN SiP is simulated both with and without corner dummy pads. Fig. 4 depicts the visco-plastic dissipations in the solder joints of the package attached on PCB. Instead, in Table III the numerical comparison between the two designs is reported, both in terms of normalized average value of plastic work in critical solder (i.e., the most stressed) and for normalized Darveaux cycles to failure. The values refer to the last thermal cycle of the BLR trial and are normalized with respect to the "original" design without corner pads. The better fatigue-based performance is reached if it is employed the package with corner pads, which improve the "anchoring" of the entire package.

Table II Material properties for the thermo-mechanical simulation.

Material	***E [GPa]***	***CTE [ppm/K]***	***Poisson coefficient***
Copper	117	16.4	0.34
Copper - board	117	16.4	0.34
Resin (T_g = 120°C)	27.4/1	10/38 (α_1/α_2)	0.34
Silicon	169	3	0.23
Solder PbSnAg	13.8	29	0.35
Solder SAC	41.7	22	0.35
Tape driver	2.5	60	0.44
FR4 (board)	19.4	15	0.11

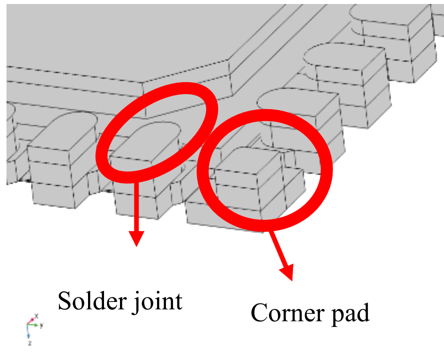

Fig.3. Corner pad and considered solder joint for cycle to failure number computation.

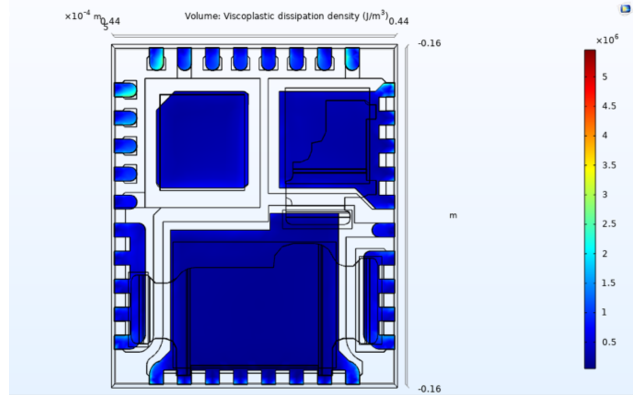

Fig.4. Visco-plastic density in solder joints at the end of the final cycle of BLR simulation without corner pads.

Table III Normalized values of visco-plastic dissipation and number of cycles to failure for the two design options.

Design option	ΔW	N_F
Without corner pads	1	1
Package with corner dummy pads	0.72	1.56

7.4 Electromagnetic simulations

In this section, FEM electric and electromagnetic simulations on the considered package will be presented.

7.4.1 Drain-source on-state resistance computation

Drain to source resistance, also called $R_{DS(on)}$, is a fundamental parameter to assess LV power devices electrical characteristics during the on-state period as it is strictly related to the conduction losses. It must be a very low value. In fact $R_{DS(on)}$, for this kind of packages, is in the size of a few mΩ. In this context, FEM simulation is employed in the proposed analysis, applied to the integrated package considered in previous sections. Various cases have been considered in order to distinguish the resistive

contributions due to package [11]. More specifically, resistive contributions of source front metal, brazable (or wet) metal, clip, and of the entire package will be computed and experimentally benchmarked.

Two different simulations have been realized: once related only to the HS of the bridge of the QFN SiP, while in a following step only the LS has been considered. The molding compound is not modeled, as it influences in a marginal way the electric performances due to its very low conductivity. With reference to the material composition, the following statements are applied: wet metal has assumed as titanium, with thickness equal to 1 μm; front metal is considered as aluminum-based, with a thickness of 4.5 μm; silicon resistivity has been calibrated to fit the experimental total package resistance for LS device. Fig. 5 (a) depicts the two implemented metal parts, while Table IV lists the electrical conductivities of the various materials presented in the simulation performed in COMSOL. An electric stationary simulation is performed and benchmarked with experimental results. With reference to boundary conditions, a potential of 1 V is imposed on drain, while ground (0 V) is set on source part in all the simulated cases. The total resistance value obtained in experimental test of case 1 is used to normalize the experimental and simulated values obtained in the cases 2 and 3. In case 2, the measurement terminals are chosen in such a way that the difference between case 1 and case 2 provides the clip contribution including the front metal as well. In this case the contribution from package input (pin) to the driver is considered, thereby excluding the clip resistance. In simulation, voltage is read on a point matrix placed on die source pad, as done for the experimental test.

Case 3 is only simulation-based, because it was not possible to measure this quantity experimentally: it permits to obtain only the clip contribution

if it is considered the difference with the resistance value obtained in case 1. The considered path is from clip solder to drain (in this case, source is placed on clip solder/clip contact surface). This case is very useful, because in such a way the solely clip resistance can be obtained, without the front metal. Fig. 5 (b) shows the electric potential in LS MOSFET.

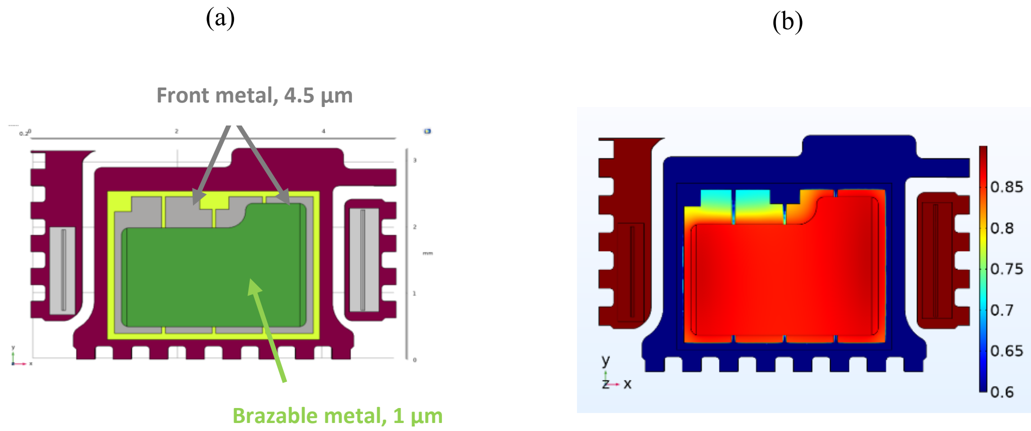

Fig. 5. (a) LS front (in grey) and wet (in green) metals. (b) LS MOSFET electric potential (V).

Table IV Electrical conductivities of the stack materials.

Material	***Electric conductivity S/m***
PbSnAg solder	5.0×10^6
Aluminium front metal	3.7×10^7
$CuFe_2P$	3.5×10^7
Wet metal	1.43×10^7

In Table V, the normalized $R_{DS(on)}$ values for LS device, obtained both experimentally and numerically, are reported. It can be noted that also in case 2 simulations fit quite well the measured values. This statement is valid also for the HS case, for brevity not reported here.

Table V Simulation and experimental results for LS - normalized $R_{ds(on)}$

Normalized $R_{DS(on)}$	CASE 1 Die+clip	CASE 2 Input to driver	CASE 1 – CASE 2 (Difference) Clip contribution + front metal	CASE 3 Simulation	CASE 1 – CASE 3 (Difference) Only the clip
Experiment	1	0.69	0.31	-	-
Model	1	0.73	0.27	0.86	0.14

7.4.2 Parasitic elements computation

High frequency operation of power converters, especially for innovative power semiconductor devices, brings to high voltage and current slew rates which, coupled with parasitic elements, in turn lead to overvoltages and overshoots. At this stage of the presented workflow, resistive and inductive contributions for the main electric paths inside the SiP are evaluated by means of Ansys Q3D extractor software, which resolves the Maxwell equations accounting for electric and magnetic fields, considering quasi-stationary approximation [41]. The evaluation is performed at 1 MHz, a frequency reasonably high to highlight the parasitic contributions. Table VI reports the material properties chosen in the simulation case study. Various possible paths can be considered in the simulation: two cases among the most critical ones are studied. The first regards the net form LS drain to HS source, while the second one considers the path between LS source and driver power ground (PGND). In Fig. 6, the net from LS source to driver is showed, while in Table VII the resistance and inductance obtained values are provided, for this path and for that from LS drain HS source, as explained before.

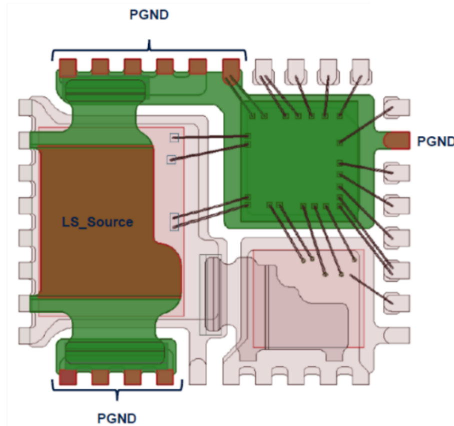

Fig. 6. LS source - drive net path

Table VI Material properties for the electric simulation.

Material	Object	Relative Permittivity	Relative Permeability	Bulk Conductivity [S/m]	Dielectric Loss Tangent
Copper	Bond wire	1	1	58×10^6	0
Copper C194	LF, clip	1	0.99991	55×10^6	0
95.5Pb-5.0Sn-2.5Ag	Solder	1	1	5×10^6	0
FR4 epoxy	Molding compound	4.4	1	0	0.02

Table VII Simulation results of parasitic resistance and inductance for LS device at 1 MHz

Analyzed path	Resistance [mΩ]	Inductance [nH]
LS drain - HS source	1.50	0.57
LS source - driver PGND	0.23	0.12

It can be noted that the values are quite low; however, they must be considered coupled with the high slew rates occurred in operation of

converter. For this reason, these values could be inserted in a Spice-like model, in order to simulate the entire topology.

7.5 Thermal numerical modeling

7.5.1 Brief overview on thermal management

Temperature reached inside the package, and in general the way to dissipate the heat due to power losses, are critical points in power devices design. These topics, already treated in the thesis, are here briefly recalled for LV-based SMDs. In terms of thermal management, SMD-based packages with exposed thermal pads are present on the market, either bottom- or top-side cooled. In any case, drain pad helps in heat transfer to PCB. The system's temperature limit is given by the PCB, because of its insulating electrical features which result in a poor thermal conductivity. Thermal management is one of the first requirements either for discrete or module-based packages [13]. There exist several ways to cool LV power devices. They can or cannot include the presence of heatsink, thermal vias, PCB copper pads, natural or forced convection, and so on [28]. All heat transfer modes can be modeled by a FEM software: the conduction one is related to the thermal conductivities of the material stack, while convection and radiation are the related to the heat exchange with the ambient. In FEM codes, the convection can be modeled by using an equivalent heat transfer coefficient, while the radiation can be accounted for by using the same coefficient, adequately "corrected" [13]. In this framework, thermal FEM enables the evaluation of the reached temperature due to the real heating input (dissipated power on die) and boundaries (e.g., convection cooling).

7.5.1 Simulated case study

The following analysis is carried out by using the COMSOL Multiphysics 5.6 software. Table VIII lists the material properties employed in thermal simulation. The simulation setup, inspired by JEDEC 51-3 standard, consists of the package, attached on a 1.6 mm-thick PCB (15 mm x 15 mm), having four copper layers: the internal ones have a thickness of 70 µm, while those related to power and ground planes have a 35 µm thickness. As thermal boundary conditions, a surface power (1 W) has injected on the active area of the die, both for HS and LS devices of the QFN SiP alternatively, and a heat transfer coefficient is set equal to 10 W/m^2K, that reproduces a still-air convection condition. The obtained junction-to-ambient thermal resistance of the LS device is equal to 45.6 °C/W. A thermal map is showed in Fig. 7. Assuming a dissipated power equal to 2 W, which represents a severe condition, it is possible to apply the classic formula, reported below:

$$T_j = T_{amb} + P \cdot R_{th,j-a}, \tag{7}$$

where T_j and T_{amb} are, respectively, the junction and the ambient temperature, P is the dissipated power, and $R_{th,ja}$ is the junction to ambient thermal resistance. Considering a T_{amb} equal to 20 °C, the junction temperature will result approximately 111 °C, which is below the maximum rating for PCB of 120 °C. This implies that a safety operation can be assured for a thermally not favorable operation of the LS MOSFET. In fact, the PCB limits the thermal behavior of the system, being the “bottleneck” with respect to the maximum reachable temperature, especially in case of still-air convection, like in considered simulation. In

final application, more design solutions can be added to better dissipate the heat generated in die: among the others, there exist thermal vias beneath the package or the adoption of fans (forced convection), which can increase the heat transfer coefficient.

Table VIII Material properties for the thermal simulation.

Material	Thermal conductivity [W/m K]	Density [kg/m^3]	Heat capacity at constant pressure [J/kg K]
Copper	401	8960	385
Resin	0.84	1860	800
PbSnAg	35.3	11020	130
Silicon	156	2330	735
SnAgCu	58	7370	232
FR-4	0.35	1900	1369
Aluminm	237	2700	900

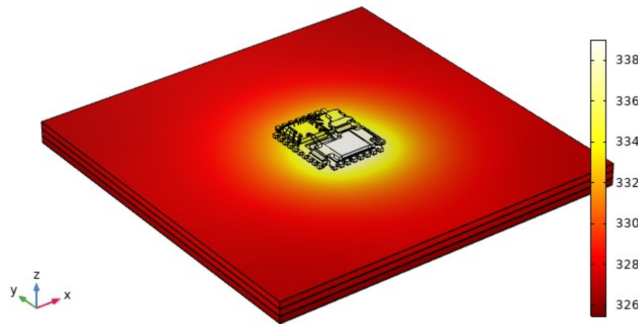

Fig. 7. Thermal map (temperature in K) of the package without resin, when the power is applied on LS MOSFET die.

7.6 Conclusions

In this chapter, a multi-physics numerical flow has been presented, that can help the design phase of a low-voltage QFN system-in package power

device devoted to automotive applications, which comprises two power MOSFETs arranged in a half bridge and a driver. The novel comprehensive numerical methodology takes into account thermo-mechanical, electromagnetic, and thermal simulations. More specifically, firstly different design options were structurally evaluated, considering the solder degradation. Then, an electromagnetic simulation has been executed, in order to evaluate the different resistive contributions and the parasitic resistive and inductive quantities due to various paths. At the end, the package must be compliant with converter's thermal management: hence, a thermal simulation has been necessary to check the temperature reached inside the package. If the simulation results were not compliant with desired features, design actions would be adopted: for example, in electromagnetic domain the contact area between clip and die would be enlarged. Instead, in thermal domain it would be possible to act both on the die (for example, with larger die area) and on the cooling system, with vias, forced convection, heatsink, and the other possible thermal management solutions outlined in the chapter. Therefore, also in early-stage corrective actions would be adopted to improve the design. A future development of the presented activity could be related to the implementation of thermo-mechanical methods for other reliability tests closer to applicative conditions, like active power cycle or intermittent operational life. Another extension could be focused on the numerical reproduction of some thermal management strategies, employing computational fluid dynamics method, and aimed to accurate temperature estimation during application.

7.7 References

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GENERAL CONCLUSIONS

In this Ph.D Thesis, various issues regarding innovative power semiconductor-based devices, both in silicon (Si) and wind-band gap (WBG) materials, have been analysed. In WBG environment, silicon carbide (SiC) and Gallium nitride (GaN) materials have been dealt with, as the innovative devices are extensively based on those materials. Application related to electric mobility (hybrid and full electric vehicles) and industrial field (e.g., servers) have been studied.

The focal points treated in the doctoral work are outlined in the following.

- Various innovative Si-, SiC-, and GaN-based power devices have been analyzed in the presented activities, either with reviews and new studies.
- Reviews on power losses firstly, and then on on-state dynamic resistance in GaN HEMTs, have been presented. The first has encounterd, either for Si and WBG devices, all the most important topics in modeling, simulation, and experimental evaluation of conduction and switching losses, either with electric and thermal methods. For electric techniques, the main features and issues have been outlined, giving also an insight into the issues related to the utilization of new devices, for example the higher switching frequency or the non-linearities in turn-on and turn-off switching chracteristics. Both calorimetric and temperature sensor thermal methods, which are spreading in recent years to compute losses, have been reviewd. This comprehensive work, both in terms of methodologies and considered technologies, is innovative in

comparison with previous works, which point out only certain techniques or only a single technology. In the second review, all the most important applicative parameters, that are off voltages and times, switching frequency, load current, and temperature, which have an impact on dynamic resistance, have been analyzed, classifying them by a comprehensive review, pointing out the most important ones (frequency, temperature, and off voltage). The data considered in the analysis have been taken from the available data in literature.

- A complete overview of the main issues encountered in SiC-based power modules for traction inverters design has been developed, with the aim of consider the applicative conditions, and taking into account insutrial on-field experience. In particular, an electrical simulation has been made to compute power losses with given applicative input parameters (inverter peak power condition). In addition, a thermal finite element method (FEM) simulation, including the contribution of self-heating and cross-coupling to study the temperature distribution, has been developed. The topic regarding parallel connection of devices has been studied by considering the spreading of electric resitance and treshold voltage in a circuit-based model, obtaining the junction temperature. In this context, the selection of devices with similar parameters would be important to reduce thermal jumps. Finally, items related to reliability, like short circuit and avalanche operation, with an experimental test, and transient gate-source overvoltages related to layout issues (giving also some possible solutions), have been treated.

- Moreover, a comparison between experimental characterization and finite-elements simulations has been proposed to evaluate the transient thermal impedance of a directly cooled SiC power module, resulting in an excellent agreement between tests and numerical models. The experiments are performed by using a power cycling equipment. This is useful in terms of degradation studies.
- Characterization and modeling (both analytical and numerical) new comprehensive flows have been developed for Si and WBG-based devices, considering application-like conditions, in order to finalize a robust design of devices and modules.
- More in detail, an analytical model is developed for high-voltage Si MOSFETs, which accounts for complex thermal phenomena (conduction, convection, and radiation). The model is made up of a set of equations (among the other, the modified Bessel's ones) for a simplified system comprising various regions, to obtain an equivalent thermal circuit. Experimental characterization boards were designed and fabricated, thereby permitting an experimental thermal comparison among different surface mounted device (SMD) packages, and the calibration of the model. The simplifactions made on the model have permitted the achievement of low computational burden and easy implementation.
- In simulation activity for GaN and Si power devices, multi-physics models have been integrated in new design flows: in particular, electro-magnetic and/or thermo-mechanical and/or thermal domains have been analyzed for various devices and SMD packages.

- Two innovative finite-element based simulations flows have been proposed, for GaN and low-voltage Si devices, respectively.
- In the first case, electromagnetic and thermal FEM simulations have been integrated to study the copper traces behaviour of a system-in-package. In particular, the power loss is computed in the first stage of the numerical flow, then the loss map has been imported in the thermal simulation, in order to compute the package's temperature. The computed temperature swing, as a consequence of copper losses, is below 20 °C. By these simulations, it has been possible to state that the package reliability is not reduced, because of the copper layer's elastic regime deformation, without any fatigue lifetime consumption.
- Instead, in the second case, a complete thermo-mechanical-electromagnetic FEM flow has been developed, to cover multi-physics device's issues encountered in low-voltage packages. The test vehicle was a Si-based system-in-package. A visco-plastic model has been employed to study the solder joint reliability from a structural point of view, by evaluating the lifetime. Then, drain-source on-state resistance is computed, because it is a foundamental quantity for power semiconductor devices. Electromagnetic simulations have been also performed to evaluate resistive and parasitic parasitic package's contributions:

this is important because of the high slew rates reachable by modern devices. Finally, a thermal simulation has been executed to chech the thermal behavior of the package. Despite other approaches presented in literature, this methodology comprises all the multi-physics numerical models which help the design of new devices with possible early-stage corrections, with a strong focus on the package-related issues in a comprehensive manner.

In general, this Thesis has presented several methods and techniques to analyze modeling, simulation, and applicative issues of innovative GaN-, SiC-, and silicon-based discrete and module solutions, considering either packages or the devices, giving a comprehensive and global view most modern items in power electronics field.

Future work would consider in a more extensive way the reliability of power devices for harsh environments, such as the automotive ones. This aim can be achieved with both extensive experimental campaigns and more sophisticated numerical models. The experimental tests can be developed to determine the reliability-related acceleration factors connected to various failure mechanisms, when particular environmental conditions, such as high temperature, high humidity, high voltage, and so on, are reproduced. On the other hand, numerical models can be developed, with an adequate calibration on experimental data if prototypes are available, to simulate design changes and assessments, and to estimate lifetime predictions in a more integrate and complete way.

Scientific production during the Ph.D. course

1. **G. Mauromicale**, A. Raciti, S. A. Rizzo, G. Susinni, L. Abbatelli, S. Buonomo, V. Giuffrida, A. Raffa, "Improvement of SiC power module layout to mitigate the gate-source overvoltage during switching operation," 2019 AEIT International Conference of Electrical and Electronic Technologies for Automotive (AEIT AUTOMOTIVE), Torino, Italy, 2019, pp. 1-6.
2. **G. Mauromicale**, A. Raciti, S. A. Rizzo, G. Susinni, G. Parise and L. Parise, "E-mobility: Safety, Service Continuity and Penetration of Charging Systems," 2019 AEIT International Conference of Electrical and Electronic Technologies for Automotive (AEIT AUTOMOTIVE), Torino, Italy, 2019, pp. 1-6. Also speaker at the conference.
3. L. Abbatelli, A. Raciti, R. Scollo, **G. Mauromicale**, S. A. Rizzo, A. Scuto, D. Nardo, N. Salerno, G. Susinni, "Effects of parasitic components on SJ MOSFET suitable for UAV," 2019 AEIT International Annual Conference, Firenze, September 18-20, 2019. Also speaker at the conference.
4. **G. Mauromicale**, A. Raciti, S.A. Rizzo, G. Susinni, L. Abbatelli, S. Buonomo, V. Giuffrida, "SiC Power Modules for Traction Inverters in Automotive Applications," 45th Annual Conference of the IEEE Industrial Electronics Society (IECON), Lisbon, Oct. 14-17, 2019. Also speaker at the conference.
5. **G. Mauromicale**, A. Raciti, S.A. Rizzo, G. Susinni, F. Fusillo, A. Palermo, F. Scrimizzi, "Efficiency of available GaN devices in a synchronous-rectifier buck converter," 45th Annual Conference of the IEEE Industrial Electronics Society (IECON), Lisbon, Oct. 14-17, 2019.
6. G. Susinni, **G. Mauromicale**, A. Raciti, S.A. Rizzo, F. Fusillo, A. Palermo, R. Scollo, F. Scrimizzi, "Si and GaN Devices in Quasi Resonant Flyback converters for Wall Charger Applications", 2019 IEEE Energy Conversion Congress and Exposition (ECCE), Baltimore, Maryland (USA), 2019.
7. **G. Mauromicale**, S.A. Rizzo, N. Salerno, G. Susinni, A. Raciti, F. Fusillo, A. Palermo, R. Scollo, "Analysis of the impact of the operating parameters on the variation of the dynamic on-state resistance of GaN power devices," 2020 2nd IEEE International Conference on Industrial Electronics for Sustainable Energy Systems

(IESES), Cagliari, Italy, 2020, pp. 101-106. Also speaker at the conference (remotely).

8. **G. Mauromicale**, A. Cascio, M. Papaserio, D. Cavallaro, G Bazzano, A.A. Messina, S. Patanè, M. Calabretta, A Sitta, "Directly Cooled Silicon Carbide Power Modules: Thermal Model and Experimental Characterization," *PCIM Europe digital days 2021; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*, 2021, pp. 1-5. Also speaker at the conference (remotely).
9. **G. Mauromicale**, D. Nardo, A.Scuto, G. Sorrentino, L. Abbatelli, G. Scelba, G. Scarcella, "Modeling and Thermal Comparison of Cooling solutions for High Voltage SMD packages," *PCIM Europe digital days 2021; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*, 2021. Also speaker at the conference (remotely).
10. A. Sitta, **G. Mauromicale**, G. Sequenzia, A. A. Messina, M. Renna and M. Calabretta, "Thermo-mechanical finite element simulation and visco-plastic solder fatigue for low voltage discrete package," *2021 22nd International Conference on Thermal, Mechanical and Multi-Physics Simulation and Experiments in Microelectronics and Microsystems (EuroSimE)*, 2021, pp. 1-6.
11. A. Sitta, **G. Mauromicale**, V. Giuffrida, A. Manzitto, M. Papaserio, D. Cavallaro, G. Bazzano, M. Renna, S.A. Rizzo, M. Calabretta, "Paralleling Silicon Carbide MOSFETs in Power Module for Traction Inverters: a Parametric Study," *2021 22nd International Conference on Thermal, Mechanical and Multi-Physics Simulation and Experiments in Microelectronics and Microsystems (EuroSimE)*, 2021, pp. 1-5.
12. **G. Mauromicale,** A. Sitta, M. Calabretta, S. M. Oliveri, e G. Sequenzia, «Integrated Electromagnetic-Thermal Approach to Simulate a GaN-Based Monolithic Half-Bridge for Automotive DC-DC Converter», *Applied Sciences*, vol. 11, n. 18, pag. 8302, set. 2021.
13. L. Anoldo, G. Piccione, **G. Mauromicale**, A. Sitta, E. Fazio, M. Calabretta, A. Lionetto, A. Messina, M. Di Guardo, S. Patanè, "Thermal simulation of a 7kW interleaved module for fast automotive charger," *2021 IEEE International Conference on Environment and Electrical Engineering and 2021 IEEE Industrial and Commercial Power Systems Europe (EEEIC / I&CPS Europe)*, 2021, pp. 1-5.

An extension of this work has been submitted to *IEEE Transactions on Industry Applications*.

14. **G. Mauromicale,** M. Calabretta, G. Scelba, G. Scarcella, A Sitta, “Multi-Physics Models Of A Novel Low-Voltage Power Semiconductor System-In-Package For Automotive Applications,” submitted to a *IEEE Transactions on Transportation Electrification*.
15. **G. Mauromicale**, G Scarcella, G. Scelba, “Power losses estimation methods in silicon and WBG semiconductor devices – A Review”, in preparation, to be submitted to a *Journal*.