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Analysis and design of converters based on SiC devices with advanced control techniques

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In memory of my father..
To my family..

"Niente e nessuno ha sempre torto. Anche un orologio fermo ha ragione due volte al giorno"
John Steinbeck

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Summary

This dissertation consists of chapters:

In the chapter 1 an introduction and the challenges of this research activity has been discussed. Moreover, the main research activity papers have been listed and summarized to be known.

The chapter 2 is an overview of the state of the art both technologies and applications in the industrial field regarding concern widebandgap semiconductors, semiconductor applications in the development of power converters.

The chapter 3 explores and studies the front-end power converter, proposing the various families of known topologies. In particular, they deal with three-phase topologies for applications such as rectifiers or more generically bidirectional three-phase conversion systems.

The chapter 4 takes up the concepts that concern the problems of design of electronic power converters by proposing new advanced development methods that can optimize the design phases of a converter.

The chapter 5 focuses on advanced techniques for the development and validation of controls for electronic converters or those that are also useful for electric drives. Study and prototype solutions have been presented.

The chapter 6 studies the methods of automatic optimization of power converters using optimization methods and tools, so an application study was presented.

The chapter 7 brings together and describes some of the application prototypes of advanced control and validation techniques. At the same time, specially designed and built platforms are presented, on which experimental tests were performed in the laboratory.

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Glossary

2LC Two Level Converter. 39, 42, 46, 47, 48, 52, 55, 56, 57, 58, 59, 60, 61, 62, 64, 71, 73, 77

3LNPCC Three Levels Neutral Point Clamped Converter. 44, 46, 50, 52, 63, 64, 65, 66, 67, 68, 69, 77

3LTTC Three Levels T-Type Coverter. 44, 46, 48, 50, 52, 70, 71, 72, 74, 75, 76, 77

3LVR Three Level Vienna Rectifier. 199, 200, 207

6SVR Six Switch Vienna Rectifier. 41, 43

ADC Analog to Digital Converter. 199, 205

ADS Advanced Design System. 91, 94

AFE Active Front End. 219, 220, 222

ASIC application specific integrated circuit. 110

AVG Average. 47, 48, 50, 52

BBC Bidirectional Battery Chargers. 219, 220, 221, 222, 227

BOM Bill Of Materials. 26

BSG Belt Starter Generator. 142, 148, 149

BV Breakdown Voltage. 14, 40, 42, 52

CCM Continuous Conduction Mode. 26, 39, 93

CLB Configurable Logic Blocks. 117, 118

DAB Dual Active Bridge. 219, 220, 221, 223, 224

DCM Discontinuos Conduction Mode. 37

DMA Direct Memory Access. 128

DPF Displaicement Power Factor. 32

DSP Digital Signal Processors. 113, 114, 119

ECU Electronic Control Unit. 111, 149, 155, 158

EDA Electronic Design Automation. 91

EM ElectroMagnetic. 91, 92, 94, 95, 101, 104, 105

EMC ElectroMagnetic Compatibility. 5, 6

EMF Electromotive Force. 156

EMI ElectroMagnetic Interference. 6, 91

EV Electric Vehicle. 25, 27, 43, 124

FDTD Finite Difference Time Domain. 94

FEA Finite Element Analysis. 146

FEM Finite Element Method. 94

FET Field Effect Transistor. 26

FIFO First In First Out. 128

FIR Finite Impulse Response. 113

FPGA Field Programmable Gate Array. 6, 7, 110, 112, 113, 114, 115, 116, 119, 121, 124, 127, 128, 135, 142, 145, 158

FRD Fast Recovery Diodes. 25, 26

FxP Fixed Point. 122

G2V Grid-to-Vehicle. 219, 220, 222, 223, 224

GAN Gallium Nitride. 5, 16

GUI Graphic User Interface. 128, 203

HDL Hardware Description Language. 114, 118, 119

HEMT High Electron Mobility Transistor. 28

HEV Hybrid-Electric Vehicle. 155, 219

HIL Hardware In the Loop. 5, 111, 112, 133, 135, 142, 148, 149, 155, 158, 163, 164

IGBT Insulated Gate Bipolar Transistor. 11, 12, 21, 25, 26

IM Induction Machine. 138, 139, 140, 142, 145, 146, 148, 149

IPQC Improved Power Quality AC / DC Coverter. 42

ISE Integrated Synthesis Environment. 142, 158

LLC Resonant Converter. 27

LUT-2D Two Dimensional Look Up Table. 158

LUT-1D One Dimensional Look Up Table. 142, 143, 147

LUTs Look Up Table. 117, 118, 119, 130, 160, 202

MCU Micro Controller Unit. 119, 121

MIL Model In the Loop. 111

MLC Multi Level Converter. xvi, 39, 42, 216

MOCVD Metal Organic Chemical Vapor Deposition. 21

MOSFET Metal Oxide Semiconductor Field Effect Transistor. 11, 12, 19, 53, 199, 207, 219, 220, 221, 222, 225

NPC-SCHB Neutral Point Clamped - Simmetric Cascaded H-Bridges. 41, 44

OBC On Board Charger. 27

PAL Programmable Array Logic. 115

PCB Printed Circuit Board. xi, 5, 17, 18, 91, 92, 94, 95, 96, 100, 101, 102, 104, 105, 106, 107

PF Power Factor. 32, 33, 34

PFC Power Factor Controller. 6, 24, 33, 39, 93, 133, 207, 219, 220, 222

PHEV Plug-in Hybrid Electric Vehicle. 43, 219

PIL Processor In the Loop. 111

PiN Positive Intrinsic Negative. 12, 25

PWM Pulse Wide Modulation. 128, 134, 148, 157, 158, 160, 193, 196, 199, 201, 202, 207, 219, 220

PXI PCI eXtensions for Instrumentation. 148

RAM Random Access Memory. 118, 119, 130, 142, 147

RMS Root Mean Square. 47, 48, 50, 52

Rth Thermal Resistance. 85, 86, 88

RTI Real Time Interface. 163, 164

Si Silicon. 25, 40, 42, 46

SiC Silicon Carbide. 5, 16, 25, 26, 32, 40, 46, 53, 77, 91, 92, 93, 95, 97, 100, 106, 199, 207, 219, 220, 221, 225

SiC-JFET SiC-Junction gate Field Effect Transistor. 28

SiC-JBS SiC-Junction Barrier Schottky. 24, 26

SIL Software In the Loop. 111

SMB Standard Model Based. 164

SMED State Machine Event Driven. 93, 201, 202, 203

SP Simulation Platform. 131, 133

SRAM Static Random Access Memory. 115

SRM Switched Reluctance Motor. 155, 156, 157, 158, 163, 164

TCR Temperature Coefficient of Resistance. 26

THD Total Harmonic Distortion. 32, 33, 36, 38, 208, 224

V2G Vehicle-to-Grid. 6, 215, 219, 220, 222, 224

VHDL VHSIC Hardware Description Language. 7, 110, 114, 116, 118, 119, 142, 158

VI Virtual Instrument. 128

VOC Voltage Oriented Control. 81, 82, 216, 218

VR Vienna Rectifier. 40, 92, 106

VSC Voltage-Sourced Converter. 80

WBG Wide Band Gap. 5, 11, 12, 14, 15, 16, 32, 89, 90, 200

ZCS Zero Current Switching. 19

ZVS Zero Voltage Switching. 19

Chapter 1

Introduction

In recent years, power electronics has shown a rapid and vast technological development in relation to various areas ranging from renewable energies, with distributed systems, to the implementation of advanced conversion systems for all electro-mobility vehicles. In particular, despite the increasing power involved, this last application requires a continuous in terms of weights and volumes and it represents a continuous technological challenge in terms of materials and devices used for the construction of electronic power converters. Current technologies, being based on the use of silicon electronic devices, have both the low thermal and the maximum working frequency limits. These limitations have led to the need to develop new electronic power devices based on cutting-edge technologies, called Wide Band Gap (WBG), able to overcome the existing restriction. The use of WBG devices is winning and advantageous in terms of performance and is a great solution in many applications of power electronics, making it possible to define extremely ambitious new objectives, such as the possibility of creating vehicles for the space exploration with electric propulsion . Just for this example it is clear the need for electronic power converters to innovate in terms of power density as well as to achieve the necessary reliability. The purpose of this study is to understand the characteristics of WBG technologies such as Silicon Carbide (SiC) and Gallium Nitride (GAN), to explore the advantages and disadvantages of devices composed of such materials and to evaluate their behavior and convenience through simulations and loss modeling in applications such as static converters. During the study period, converter prototypes have been developed taking into account the needs for the use of WBG devices. Real time Hardware In the Loop (HIL) simulation methods have been analyzed, studied and implemented to demonstrate their effectiveness in the design of drives and power converters. Critical issue is related to the power converters that use devices WBG leading to some ElectroMagnetic Compatibility (EMC) phenomena that cover an increasingly preponderant role due to the high di/dt and dv/dt and that for this reason make the development of layout and PCBs a fundamental issue. For this reason electromagnetic simulation methods for the emulation of these phenomena have been studied. The analysis and study of innovative electronic power converters that use WBG devices aims to achieve higher efficiency values around 99%, also obtaining an increasing in power density both from the point of view of the volume and the weight.

1.1 Contribution to research

The PhD thesis begins with a research proposal concerning an extremely interesting topic in recent years which is the study and analysis of electronic power converters that use new generation semiconductors that have the potential to obtain very high energy efficiency systems .

Considering the relevance of this topic also for industries, STMicroelectronics (Catania) wanted to collaborate in this research, giving rise to a continuous commitment for the whole period of the doctorate.

In the first research period, the state of the art was analyzed with regards both technologies and applications in the industrial field. The first objective was to try to mature concepts that concern widebandgap semiconductors, semiconductor applications in the development of power converters based on known and non-known topologies (chapter 2).

In particular, the study focused on a particular family of power converters, among which there are the three-phase AC / DC Power Factor Controller (PFC) rectifiers that are used in more and more industrial and civil environments (section 3.1), for this as an application test-bench, a three-phase multilevel rectifier with a PFC capability has been studied and analyzed (section 7.1).

The reason for these research lies in the fact that the benefits linked to the use of semiconductor devices operating at high switching frequencies lead to a greater influence in phenomena related to ElectroMagnetic Interference (EMI) / EMC (section 4.2) [1] or thermal stress phenomena related to the high operating temperatures of these devices (section 4.1).

Furthermore, the possibility of operating at high frequencies makes it possible to operate with high bandwidth controls, since the switching one, ie the one linked to switching disturbances, has undergone a considerable increasing. For this reason, high bandwidth controls have been analyzed and developed with the industrial goal of finding an implementation strategy compatible with very low cost microcontroller platforms (section 7.1) [2] and [3].

During the period of study and design of these control systems, feasibility analysis and development of real time emulators of Field Programmable Gate Array (FPGA) (section 5.1 and chapter 5) have been developed obtaining interesting results both in terms of implementative optimizations (section 5.8.1). Following the studies, various FPGA-based emulators were implemented and tested, among those,some are currently operating in the R&D of companies to test their control systems (section 5.9) [4–9].

To complete the studies concerning the advanced development of power converters, in-depth investigation on the techniques of *"Multi-Objective Design"* have led to interesting results in the use of genetic algorithms in the field of power electronics (chapter 6)

Further applications have concerned the design of bidirectional three-phase converter topologies for Vehicle-to-Grid (V2G) applications, also in this case trying to focus on all the design issues related to the use of devices with high switching frequencies (section 7.2).

Comparative studies between various three-phase topologies for *V2G* application have shown relevant results to determine which one lead to the greatest benefit in the use of

WBG devices and which therefore operate at high switching frequency (section 3.3).

Also with regard to single-phase applications, studies concerned multistage converters for "Battery charger" applications [10] or interleaved [3]

During the PhD course there were also the opportunity to participate to master thesis work that dealt with issues close to the research project. In *"Optimization of a Vienna rectifier using multi-objective genetic algorithms, A.Costa"* has been studied the feasibility of using genetic algorithms in the field of electronic power converters, in *"FPGA-based implementation of high dynamic control strategies for induction motor drive, G.Lucifora"* a implementation of a high performance control for electric motors implemented on a FPGA platform based on autogeneration systems has been studied, of VHSIC Hardware Description Language (VHDL) code at high level, in *Analysis and implementation of bidirectional power converters for automotive applications, D.Nicastro* a study and implementation on simulator of an electronic power converter for automotive application is described, in *Three phase PLL algorithm for low cost grid connected power application,V. Palermo* various structures for phase estimator for PFC Rectifier application were compared to identify the strategy that has the best compromise between effort and precision in relation to the use on very low cost microcontrollers, in *Advanced modeling of polyphase induction machines for hardware in the loop simulations,R. Di Dio* there is a feasibility analysis followed by the implementation of a real time emulator of an asynchronous electric drive for the validation of automotive control units.

1.1.1 My Bibliography

Hardware in the loop for failure analysis in AC motor drives [5]
BEST PAPER AWARDS

The paper deals with an extensive experimental analysis of failures in ac motor drives exploiting a Hardware In the Loop (HIL) implementation. As many types of faults lead to stop the drive operation, a suitable approach for the realization of an appropriate test bench consists in the replacement of some hardware with an embedded system based on a FPGA board and high level graphical programming language. Such system is also used to evaluate different designs using FPGAs for both control systems and modeling of the electromechanical components. Two different numerical implementation concepts are considered: fixed point and single precision point. Differently than standard approach for FPGA programming, normally based on hardware description languages, the proposed method exploits an environment software platform with a high level abstraction that leads to obtain a good trade-off between accuracy and hardware resources also allowing a faster prototyping procedure. The proposed HIL approach has been used to study some common faults occurring on the inverter stage of a standard motor drive, evaluating the behavior of different control algorithms and their response in real-time.

Failure analysis of AC motor drives via FPGA-based hardware-in-the-loop simulations [7]

The paper deals with an extensive analysis of power converters failures in AC motor drives by exploiting the capability of a hardware-in-the-loop (HIL) simulation platform to emulate the real-time behavior of electrical machines and power converters. In this way it is possible to investigate the effects of power converter faults in electrical drives with the aim to propose solutions that allow to reduce the periods of drives inoperability. In this paper, a suitable realization of a test bench combining an embedded system based on a FPGA board with a high-level graphical programming language is proposed to replace part of the electrical drive hardware. Differently than standard approaches for FPGA programming, which are normally based on hardware description languages, the proposed solution exploits an environment software platform with a high level of abstraction that leads to a good trade-off between accuracy and hardware resources, also allowing a faster prototyping procedure. The proposed HIL solution has been used to study some common faults occurring in power converters, evaluating the behavior of a standard drive operating with different control algorithms.

A high efficiency interleaved PFC front-end converter for EV battery charger [3]

Nowadays, an increasingly present application in the automotive field is the battery charger that usually consists of two high efficiency parts: an AC/DC converter with power factor correction (PFC) capability and a DC/DC converter. In this paper, a three-channel interleaved Power Factor Correction (PFC) based on a new digital controller STNRGPF01 operating in Continuous Conduction Mode (CCM) is presented addressing high efficiency. In the considered applications, the most challenging control issues are the input current control and the fast overcurrent protections. Exploiting mixed signal control approach some benefits have been obtained and confirmed by experimental results on a 3 kW prototype.

Real-Time Emulation of Induction Machines for Hardware in the Loop Applications [6]

A FPGA-based dynamic model of three-phase induction machines is presented in this work. The model includes the effects of temperature in the stator and rotor resistances and magnetic saturation in the magnetizing and leakage inductances, according to the stator and rotor currents. Moreover, iron core losses have been properly modeled. The proposed implementation ensures high accuracy of the simulations in a wide range of operating conditions, keeping a reasonable computational burden. Experimental tests confirm the matching between the results provided by the hardware in the loop system and those coming from the experimental rig, the last including an electronic control unit used in automotive systems.

RealTime emulation of a three-phase vienna rectifier with unity power factor operations [4]

BEST PAPER AWARDS

In this paper a FPGA-based dynamic model of a three-phase Vienna Rectifier with unity power factor operations has been developed addressing applications as stationary chargers for electric vehicle or telecom rectifiers. Such a model has been implemented to be used in a Hardware In the Loop (HIL) system where the power converter has been replaced with an embedded system based on a FPGA board. The proposed system has been designed to test converter control algorithms in a fast and safe way. The proposed solution exploits an environment software platform with a high level abstraction, obtaining a good trade-off between accuracy and hardware resources, also allowing a faster prototyping procedure. The HIL implementation has been compared with that of the experimental rig, confirming a good agreement in terms of accuracy and dynamic behavior.

Real-time emulation of a three-phase Vienna rectifier with DC voltage control and power factor correction [8]

The paper deals with the accomplishment of a FPGA-based dynamic model of a three-phase Vienna rectifier controlled in order to feature unity power factor operations. Such a model has been developed for the Hardware In the Loop (HIL) implementation of a test rig in which the power converter is replaced with an embedded system using a FPGA board. The proposed approach has been fostered mainly to test different converter control algorithms in a fast and safe way. Such solution is based on a software platform environment with a high-level abstraction that ensures a good trade-off between accuracy and hardware resources, also allowing a fast prototyping procedure. The results obtained by the HIL implementation have been compared with those of a fully hardware experimental rig, confirming a very good agreement in terms of accuracy and dynamic behavior.

Modelling and Simulation of a Bidirectional SiC-based Battery Charger for V2G applications [10]

This work deals with the study of a bidirectional battery charger with SiC-MOSFETs devices, from the design, modelling and simulation stages to the realization of a laboratory prototype. The battery charger consists of a high efficiency 5 kW single-phase bidirectional power converter suitably designed for grid to vehicle and vehicle to grid applications. It is composed by two stages: an AC/DC PFC Synchronous converter and a insulated DC/DC Dual Active Bridge modulated in phase-shift. In order to optimize the design, an accurate model has been implemented and accurate simulations have been carried out able to evaluate the system performance in several operating conditions.

Mixed Signals Based Control of a SiC Vienna Rectifier for On-Board Battery Chargers [2]

The main aim of this work is to investigate the feasibility of implementing a low-cost mixed-signal based control solution for a SiC three-level Vienna rectifier addressing electric vehicle on-board battery charger applications. The proposed solution allows to achieve almost unitary power factor operation as well as higher control loop bandwidths and lower total harmonic distortions in comparison with standard all-digital implementation using low-cost digital platform. A detailed description of the combined digital-analog approach

is provided, as well as an experimental validation of the proposed solution for a 12kW on-board battery charger.

Analysis of PCB parasitic effects in a Vienna Rectifier for an EV battery charger by means of Electromagnetic Simulations [1]

The aim of this work is to investigate the impact of the PCB (Printed Circuit Board) electrical parasitic parameters on the performances of a SiC Three-Level T-type rectifier used for electric vehicle battery chargers. The short switching times of the SiC devices enables high switching frequency at very high efficiency. On the other hand, as the time derivative of the current increases (as a rule of thumb we can set 1A/ns as a breaking point), PCB parasitics start to play a significant role and may cause the degradation of the performances or even a design failure, if not taken into account right from the first design stage. Industry standard EDA (Electronic Design Automation) tools can be used to extract a model for the PCB to evaluate all the unwanted effects introduced by the physical realization of the board layout. For the scope of the current study, the software Advanced Design System, ADS by Keysight Technologies has been used to extract an S-parameter based model of the PCB and co-simulate it with the circuit components. Results obtained with and without the PCB model are finally compared for two different design iterations.

FPGA-Based Design and Implementation of a Real Time Simulator of Switched Reluctance Motor Drives [9]

The purpose of this work is to present an effective technical solution devoted to simulations of switched reluctance motor drives, which is designed and implemented on a Hardware In the Loop real time simulator that takes into account the nonlinear characteristics of the motor phase inductances and parameter variations. The proposed solution features low computational efforts and ensures high accuracy in the provided outcomes. The implemented model is verified by comparing the results achieved by the proposed solution with that obtained by a standard model-based design environment, assessing the simulation fidelity of the hardware in the loop simulation.

Chapter 2

State of the art

Power electronics is a field in continuous evolution: from the first mercury rectifiers invented in the early 1900s to the transistors and diodes of the early 1950s to get to modern Metal Oxide Semiconductor Field Effect Transistor (MOSFET) and Insulated Gate Bipolar Transistor (IGBT)". Now the components are made of semiconductors, because they allow the switching to happen with few losses; the switching speed and the type of control greatly affect the design of the system, which must obviously ensure minimum losses and maximum efficiency Silicon (Si), being an intrinsic semiconductor, has long been the most used material for these components thanks to its low cost and great availability; it can also be doped with elements of the III group such as boron (B), gallium (Ga) and indium (In) or with elements of the V group such as phosphorus (P) and arsenic (As) obtaining respectively a p-type doping (creation of energy states in the forbidden band near the valence one) and an n-type (creation of energy states in the forbidden band near the conduction band). However, in recent years the power and frequency of use have increased considerably and pure or doped silicon is no longer able to operate effectively under the required conditions; innovative materials begin to appear, called Wide Band Gap (WBG) semiconductors, which have only recently begun to be produced on an industrial scale. Among these, two in particular attract attention: they are silicon carbide (SiC) and gallium nitride (GaN). Distributed generation, which is the basis of all renewable energy sources, which with the complicity and interest of large retailers and the pressing commitment to environmental sustainability are requiring, for the realization of the entire energy production and distribution chain , devices that are increasingly efficient in terms of space and performance. The traction of electric-hybrid vehicles, which is a relatively immature sector and which still has a large margin of research and development. Nowadays the electric-hybrid vehicle is not a standard but it will have to be in the very short term, given that many countries of considerable importance in terms of market are imposing in the immediate future the prohibition of circulation for vehicles that use exclusively endothermic engines. This leads to a natural and important investment that all related companies are entering in the various areas of R&D, starting from storage systems, to electrical drives and electronic converters. The latter will be the field of interest of the research project with the aim of developing new technical solutions in order to make the most of new technologies

related to WBG devices.

2.1 Wide Band Gap Materials

Only since the last decade have the WBG semiconductors made their appearance in the commercial field. This is because silicon semiconductors were able to operate effectively; however, now silicon has reached its limits in power and frequency, especially in recent applications such as optoelectronics or electric vehicles, as shown in fig. 2.1. In general, the requirements for any converter are compactness, light weight, high power density, high efficiency and optimal operation in difficult conditions. When it comes to difficult conditions, the main aspect is the high working temperature: the maximum junction temperature limit is 150°C so it is necessary to keep the temperature of chips and silicon components below that value. For high-power converters, natural air dissipation is not enough, a fluid cooling is required but it is heavy and takes up more space; having said that, it is clear that semiconductors capable of operating even at high temperatures decrease the costs and dimensions of the conversion equipment. It is known that heat comes mainly from conduction and switching losses with high currents of the semiconductors themselves. Bipolar components such as IGBTs and Positive Intrinsic Negative (PiN) diodes have larger losses than unipolar ones such as MOSFETs and Schottky diodes, but they are more suitable for high power because increasing the voltage values also increases the breakdown voltage; in this case the silicon die must be larger. Normally, then, a greater frequency of switches is preferred because the dimensions of the components are smaller and the output is smoother, so that only a small filter against harmonics would be sufficient. Then, a converter that operates in a range of high frequencies can be more comfortable for the user since it is not noisy, or rather it produces noise at a frequency that is not audible to the human ear [11]. WBG semiconductors surpass the theoretical limits of silicon and therefore offer sensitive improvements in performance and allow it to operate in harsh conditions. When compared with silicon, they have the following advantages[12]:

- Lower on-resistance;
- Higher breakdown Voltage;
- Higher thermal conductivity;
- High temperature operation;
- Greater reliability;
- Excellent recovery;
- High frequency operation.

However, at present there are also the following disadvantages considering that it is a technology being developed

- Defects and dislocations in SiC and difficulty in manufacturing GaN;
- high cost;
- Limited availability;
- High temperature packaging technology in development;

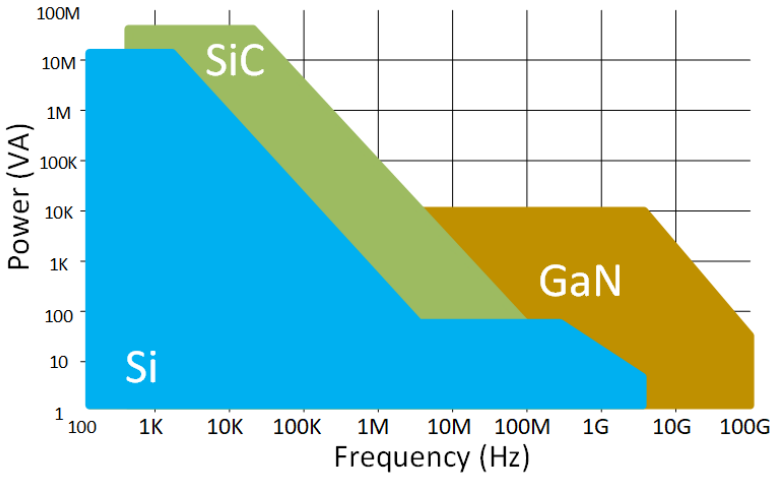

Figure 2.1: Devices Application

The properties listed can best be demonstrated by analyzing the physics behind it. The Wide Band Gap semiconductors have much wider forbidden bands than the silicon ones: this naturally translates into a greater breakdown electric field, but also in the possibility of operating at high temperatures [13] and in reducing the susceptibility to radiation given that the energy levels to move an electron are greater. (fig. 2.2)

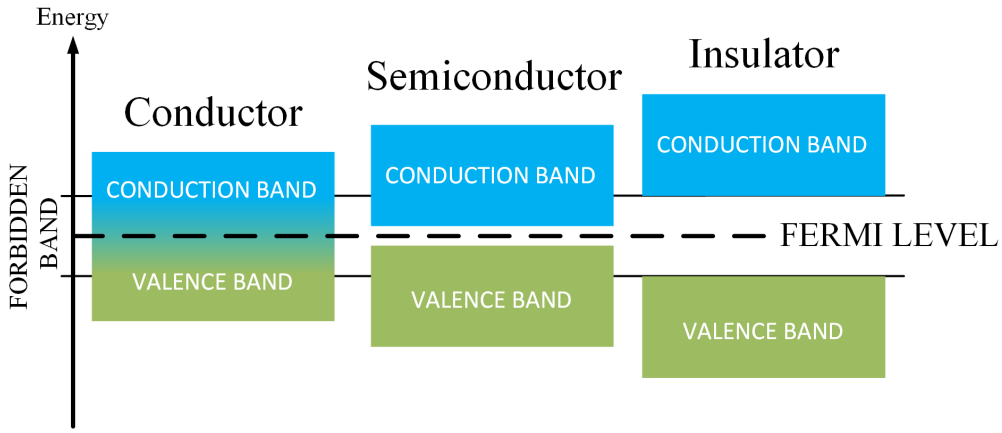

Figure 2.2: Energy levels of material

Then, as the temperature increases, the thermal energy of the electrons in the valence band also increases, until at a temperature threshold they have an energy that allows them to pass the energy gap that exists between the valence band and the conduction band. This transition condition causes an uncontrolled flow of electrons, therefore the behavior required is to have a wide energetic gap allowing the material to operate at high temperature. A large band gap results in a greater electric breakdown field, ie greater Breakdown Voltage (BV). The BV is the voltage at which the junction that when gate and source are short-circuited is cut off and consequently the current begins to flow between source and drain, multiplying by avalanche effect.One of the main benefits in the realization of WBG devices is that at the same breakdown voltage the semiconductor layers can be thinner and therefore providing higher doping levels results in lower resistances. A further source of energy that involves an uncontrolled passage of electrons and electromagnetic radiation, therefore, as identically to thermal energy, a wider forbidden band decreases the effect of radiation on semiconductors and avoids unwanted and uncontrollable conduction. If you think of an application as the automotive it is immediate to think that these features represent an important benefit. Safety and reliability are fundamental requirements and in general for all applications where the malfunction of the drive risks compromising the entire process; sectors particularly sensitive to these problems are also: industrial, military, aerospace and renewable energy and it is shown that WBG devices have a much lower rupture index than silicon technology.

2.2 Wide Band Gap Semiconductors

The Wide Band Gap semiconductors have much wider forbidden bands than semiconductors such as silicon (Si 1.12ev) or gallium arsenic (GaAs 1.4ev): this naturally translates into a large electric break field, but also in the possibility of operating a high temperature and in reducing the susceptibility to radiation without losing the electrical characteristics (fig. 2.3).

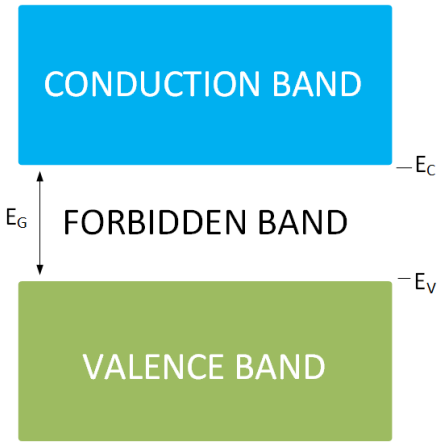

Figure 2.3: Semiconductor energy band

As the temperature increases, the thermal energy of the band also increases, until a certain temperature reaches the energy necessary to pass into the conduction band. For silicon this threshold is 150 °C instead the WBG semiconductors, since they have a much larger band, can reach a much higher temperature without the energy of the electrons being enough to pass to the conduction band. It is clear that, as the bandwidth increases, the temperatures reached will be higher and one consequence is that, radiation can excite electrons in a similar way to thermal energy, so a wider band gap prevents unwanted and uncontrollable conduction.

Property	**Si**	**GaAs**	**4H-SiC**	**GaN**	**Diamond**
Band gap $E_g[eV]$	1.12	1.43	3.26	3.4	5.45
Electric breakdown field $E_c[MV/cm]$	0.3	0.4	2÷4	3.3	>5.6
Relative dielectric permittivity ϵ_r [-]	11.9	13.1	9.9	9	5.6
Electron mobility $\mu_n[cm^2/V \cdot s]$	1500	8500	950	900/2000	2000
Hole Mobility $\mu_n[cm^2/V \cdot s]$	600	400	115	850	850
Thermal conductivity $\lambda[W/cm \cdot s]$	1.5	0.46	4	1.3/3	21
Saturated e drift velocity $v_{sat}[\cdot 10^7 cm/s]$	1	1	2	2.3	2.7

Table 2.1: Physical characteristics of Si and the major WBG semiconductors at 300K [12]

A large band gap means more breakdown electric field, ie higher breakdown voltage. The breakdown voltage is the voltage for which the body-drift diode (interdict) collapses and consequently the current begins to flow between source and drain, multiplying by avalanche effect and gate - source are short-circuited. With the same breakdown voltage value, the WBG semiconductor layers can be thinner, higher doping levels are obtained and the drift region resistances are lower. For example, the breakdown voltage of a PN-junction diode is given by eq. (2.1).

$$V_B \approx \frac{\epsilon E_c^2}{2qN_d} \tag{2.1}$$

where q represents the charge of the electron (-1.602×10^{-19} C) and N_d is the concentration of the material. Using the parameters shown in (table 2.1) and assuming for all materials an inverse current of 10 µA and the same value of N_d, we get that the breakdown voltage of the silicon diode is about 50 V; instead that of SiC, GaN and diamond is respectively 4150 V , 4550 V e 8200 V: a value that is 83, 91 and 164 times higher than that of silicon. Another consequence of the high electric breakdown field and of the greater doping concentration is the reduction of the width of the drift region. Note that the drift region is not the region of space charge, whose width depends on the quality of the doping. The width of the drift region is given by eq. (2.2).

$$V_{drift}(V_B) \approx \frac{2V_B}{E_C} \tag{2.2}$$

At the same breakdown voltage, the amplitude of the drift region is inversely proportional to the electric breakdown field: consequently the drift region of silicon carbide, gallium nitrite and diamond is respectively 9, 11 and 18 times narrower than to that of silicon (fig. 2.4).

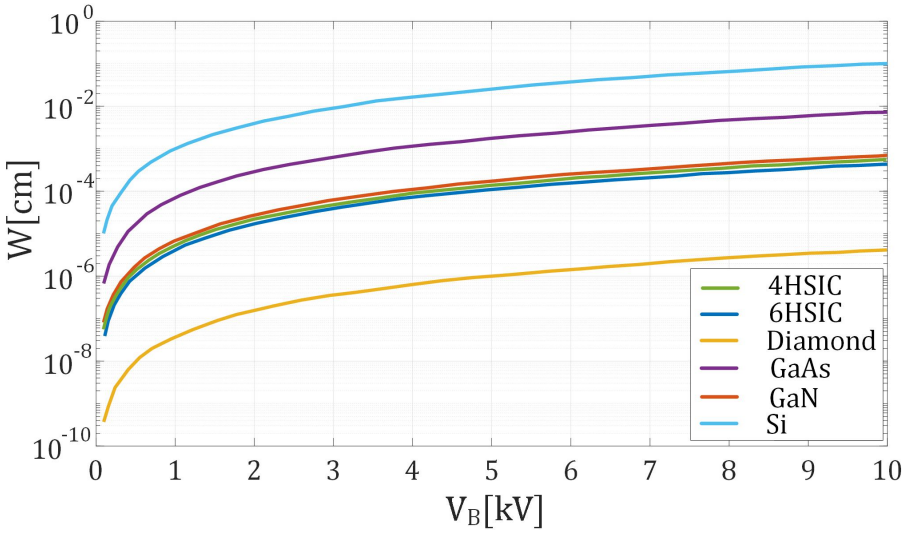

Figure 2.4: Drift region vs Beakdown voltage [12]

Another important parameter is the on-resistance of the drift region. Referring to the previous example of a pn junction diode, we have that for a unipolar device the on-resistance is given by eq. (2.3).

$$R_{on} = \frac{4V_B^2}{\epsilon_r E_C^3 \mu_n} \tag{2.3}$$

The on-resistance of the silicon device drift region is about 10 times higher than that of Silicon Carbide (SiC) and Gallium Nitride (GAN) components. Furthermore, the contact resistance and the channel resistance must also be taken into account when calculating the on-resistance; these two resistances are dominant for low breakdown voltage values but can instead be neglected for high breakdown voltages: in fact the eq. (2.3) is a good approximation for the on resistance of Wide Band Gap semiconductors (fig. 2.5).

The thinner semiconductor layers have a lower density of minority carriers and these are an important parameter to define the reverse recovery current: in fact, given the same characteristics, a component with a larger die, designed for higher currents, will have a larger charge and then will have a larger reverse recovery current.

The capacity of a semiconductor to switch at high frequency is directly proportional to the speed of drift in saturation: looking at the data reported in table 2.1, we immediately notice that the drift speed of silicon carbide and nitride of gallium is twice that of silicon. The consequence is that WBGs can operate safely at higher frequencies. In addition, a higher saturation drift speed is equivalent to a more rapid emptying of the charges in

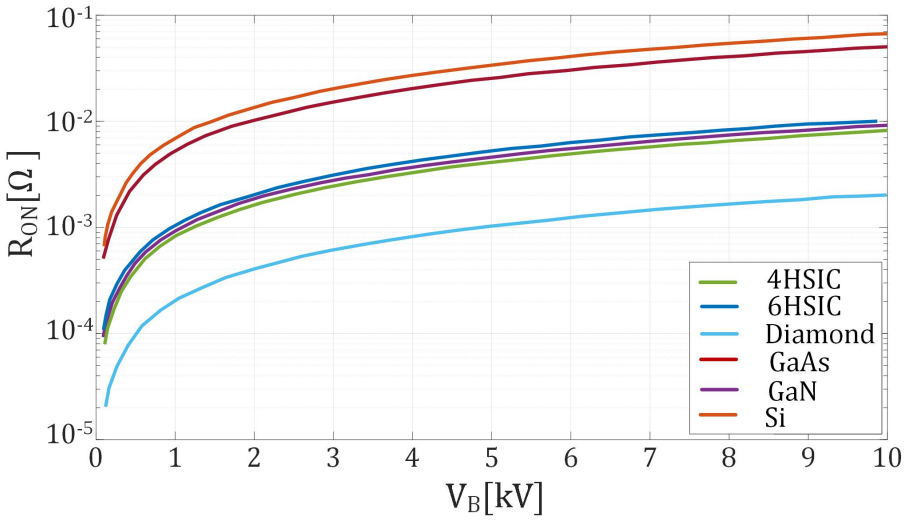

Figure 2.5: Resistance of the drift region for each material at different breakdown voltages [12]

the space charge zone; this means a shorter recovery time and a lower reverse recovery current. The ability to work at high temperatures, as well as from a wider band gap, also depends on the thermal conductivity of the material because at the same time any device has a thermal derating. There are several ways to evaluate thermal resistance: we can consider the thermal resistance between junction and case ($R_{th,j-c}$) or the thermal resistance between junction and environment ($R_{th,j-a}$). In the first method we have that ($R_{th,j-c}$) is inversely proportional to λ according to eq. (2.4) deriving from the Fourier law,where l is the length of the material measured along a path parallel to the heat flow, S represents the section perpendicular to the heat flow.

$$R_{th,j-c} = \frac{l}{\lambda S} \tag{2.4}$$

Obviously, a higher λ means a lower thermal resistance, ie the heat generated by the component is more easily transmitted to the dissipation elements and therefore that the temperature of the component grows less. A typical way to measure $R_{th,j-c}$ is the "copper cold plate measurement" (fig. 2.6): the component under test, connected to a small predefined Printed Circuit Board (PCB) and is maintained at its position by a pneumatic piston. The temperature is kept constantly at 25 °C and the thermocouple monitors the heat dissipated by the solder bumps and by the PCB to evaluate only the heat removed from the water-cooled heat sink and therefore obtain a true value of $R_{th,j-c}$.

With the second method instead we have that $R_{th,j-a}$ is obtained simply from the ratio between the temperature difference between junction and environment and the power dissipated by the component, eq. (2.5).

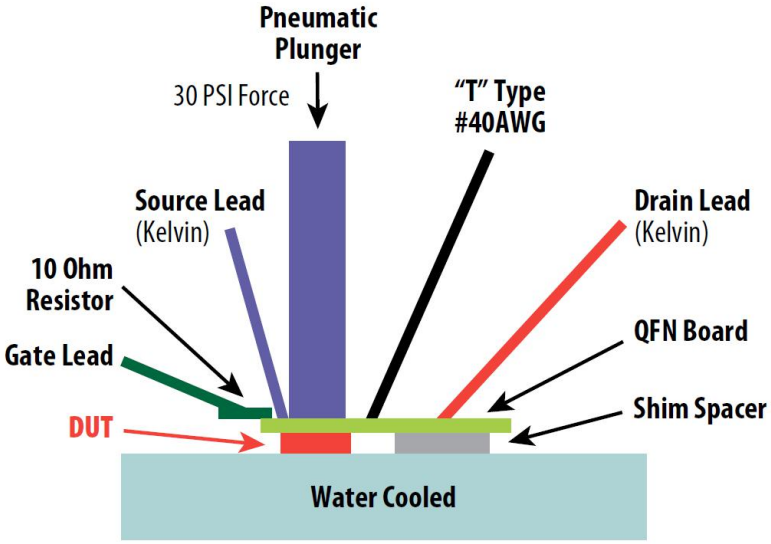

Figure 2.6: Copper cold plate measurement test [14]

$$R_{th,j-a} = \frac{T_j - T_a}{P_{diss}} \tag{2.5}$$

The thermal resistance between junction and environment is a useful parameter when external heat sinks are not connected and therefore in those cases in which it is desired to compare the thermal performances of different packages. Usually the $R_{th,j-a}$ is measured by mounting the component under test on a FR-4 PCB with single-sided copper of 2 ounces (56.7 g) and an area of 1 square inch (645.16 mm^2); half a square inch is connected to the source while the other half is connected to the drain.

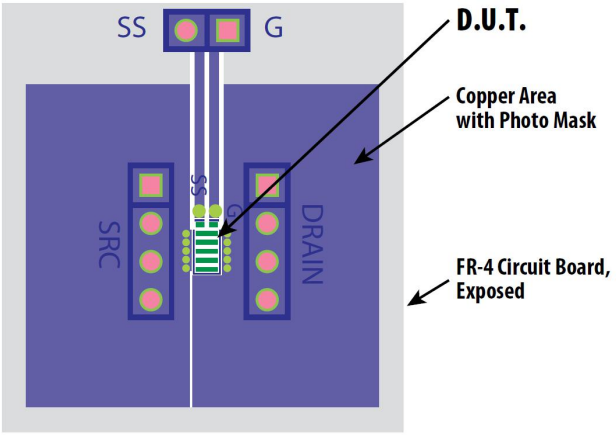

Figure 2.7: Circuit board layout for $R_{th,j-a}$ measurement with $1in^2$ copper area.[14]

The component under test is suspended in a closed box of volume equal to $1ft^3$ ($0.028\,32\,m^3$) and at the temperature of 25 °C; after it is forced to an "ON" state for 1000 seconds at a junction temperature of 125 °C. Finally, $R_{th,j-a}$ is calculated using the eq. (2.5). However, note that the ambient air pressure changes with altitude; consequently the effectiveness of air cooling also changes. A study showed that a component working at 8000 ft (2438.4 m) is warmer than 20% compared to an equal one working at sea level. It is therefore necessary to take into account also the derating factors of the thermal resistance (table 2.2).

Altitude[ft]	**Multiplier factor**
0	1
3000	1.1
5000	1.14
7000	1.17
8350	1.2

Table 2.2: Derating $R_{th,j-a}$

It is possible to make a comparison of the materials using the *"FoM"* figure of merit. eq. (2.6);

$$FOM_{BALIGA} = \epsilon_r \mu E_C^3 \tag{2.6}$$

where μ is the mobility of majority holders. This figure of merit is good for evaluating materials when the losses are mainly conduction and therefore at relatively low frequencies. However, at high frequencies switching losses cannot be ignored; considering the variety of frequencies and values of current and voltage involved it is difficult to choose a parameter that offers the best performance in all operating conditions. One of the most popular figures for selecting MOSFETs is eq. (2.7), with R_{ON} which represents the on-resistance while Q_{iss} is the input charge at the gate.

$$FOM = R_{ON} * Q_{iss} \tag{2.7}$$

These parameters respectively reflect the conduction losses and the switching losses and are connected to each other; in general, a component with lower value of Q_{iss} will have a slightly higher R_{ON}. Obviously there are also other parameters that affect the performance of the MOSFET, such as output capacity, threshold voltage and avalanche energy; but the most important are just R_{ON} and Q_{iss}. Particular circuit topologies may influence the merit figure of the MOSFETs; compare for example a traditional synchronous buck converter with a resonant one: in the latter the MOSFET switching takes place when the drain-source voltage V_{DS} or the drain current I_D pass through zero, obtaining respectively the Zero Voltage Switching (ZVS) and Zero Current Switching (ZCS); in this way the energy stored in the capacity can be reused instead of being lost as in traditional converters.

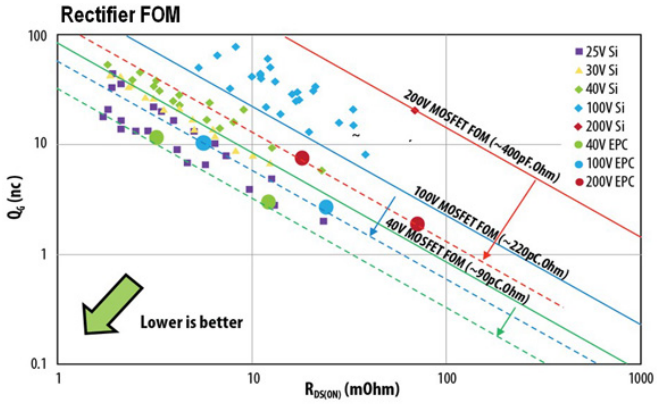

Figure 2.8: Rectifier FOM ($R_{DS_{ON}}$ vs. Q_G) for eGaN FETs [15]

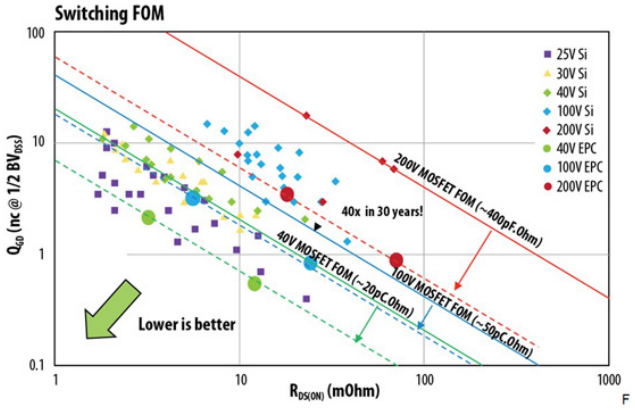

Figure 2.9: Switching FOM ($R_{DS_{ON}}$ vs. Q_{GD}) for various eGaN FETs and MOSFETs[15]

2.2.1 Silicon Carbide

Silicon carbide is a naturally available material in the form of moissanite (fig. 2.10); but since the latter is very rare, the majority of SiC is synthetic. The simplest manufacturing process consists in combining silica sand and carbon in an "Acheson" furnace with graphite resistance in a temperature range between 1500 °C and 2500 °C; the silicon vapors, a resultant product of the fabrication system of ferro-silicic alloys, can be converted into SiC by a chemical reaction with graphite at 1500 °C. The material that forms in the furnace varies in purity depending on the distance from the heat source represented by the graphite resistance: colorless crystals or those with pale colors have the highest degree of purity and are found near the graphite resistance, while the crystals more dark and distant. Typical impurities that influence the electrical conductivity of silicon carbide are aluminum and nitrogen.

Extremely pure silicon carbide can be obtained with the "Lely" process: in an argon environment at 2500 °C SiC sublimates powder in reactive silicon, carbon, silicon dicarbide

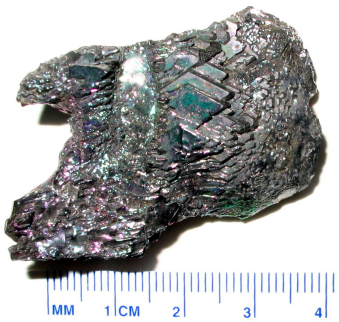

Figure 2.10: Crystal of Moissanite [16]

(SiC_2) and disilicon carbide (Si_2C) and then deposit it in the form of crystalline flakes on a colder substrate; in this way, crystals with a 6H-SiC structure are created. Usually the cubic SiC is created with the Metal Organic Chemical Vapor Deposition (MOCVD); one can also use thermal decomposition processes such as pyrolysis. Silicon carbide exists in about 250 crystalline forms. They are variations of the same chemical compound, identical in two dimensions and different in the third. They can therefore be seen as overlapping layers in a certain sequence. Silicon carbide α(α-SiC) is the most common crystalline type, with a hexagonal structure similar to wurzite, and is formed at temperatures above 1700 °C; instead with lower temperatures the type exbeta (esbeta-SiC) is obtained with zincblende structure. The high sublimation temperature (2700 °C) makes silicon carbide a material that can be used in furnaces; it is a material that does not melt at any pressure and is chemically inert. It also has a very low thermal expansion coefficient ($4 \times 10^{-6}\,\mathrm{K}^{-}1$) and has no phase changes, which would cause problems if they occurred during thermal expansions. SiC can be doped with nitrogen and phosphorus (*n-type*) or aluminum, boron, gallium and beryllium (*p-type*).

As already mentioned, there are several crystal structures of SiC. All the symbols in the denomination of the various crystal structures have a meaning: the number "3" in 3C-SiC refers to the periodicity of the stacking of the double layer and the letter "C" indicates a cubic crystalline structure. Similarly, in 4H-SiC and 6H-SiC the number indicates the periodicity of the stacking sequence and "H" refers to the hexagonal symmetry of the crystal lattice. Silicon carbide has been a material known for a long time, since the 1950s, but the main problems have always been the quality of the material and the cost. At the beginning the major obstacle to industrial production was the elimination of imperfections: in fact the components with SiC crystals had a poor capacity to withstand reverse voltage. Furthermore it was difficult to create a good interface between SiC and oxide, so the development of silicon carbide based MOSFETs and IGBTs was slower. However, recent technological advances have led to the creation of SiC-based materials without microchannels in which defects such as screw dislocations and basal plane dislocations are extremely reduced ($10^4\,\mathrm{cm}^{-2}$); in this way the degradation of the component is almost eliminated.

The production cost is higher than that of a silicon device but with the superior

performance of the SiC it is already possible to obtain a system with excellent performance and commercially competitive. The most used is the 4H-SiC with wurzite-like structure that allows a high breakdown voltage ($> 1000\,\mathrm{V}$) and virtually without current limitations. The wurzite crystalline structure is the cause of the piezoelectric effect, which involves the generation of electric current by mechanical displacement; however this process also works in reverse: the current flowing in the component induces a strong mechanical stress which is the basis of the degradation of the components during their life. The ability to work at high temperatures is excellent: at $600\,^{\circ}\mathrm{C}$ the problem is not the concentration of charges but the limitations due to packaging and metal contacts. This robustness would virtually allow components to be placed close to heat sources such as a vehicle engine. Silicon carbide can also be the bulk material for epitaxy, a very interesting fact because on this substrate it is possible to grow GaN crystals: in fact it is possible to create MOSFETs with excellent electrical characteristics.

2.2.2 Gallium Nitride

Gallium nitride is a very hard, fracture-resistant material with a wurzite crystalline structure; various semiconductors and compounds possess this type of structure. Since the latter is not symmetrical, piezoelectricity phenomena can be observed. There is also GaN with a zincblend structure.

The material is not toxic or flammable, however the processing of the materials from which it is obtained (gallium chloride and ammonia) can present health and environmental risks. Gallium nitride can be doped with different materials (silicon, germanium, selenium, oxygen, magnesium, beryllium and zinc); dopants add gallium impurities and the most widely used are silicon and oxygen (n-type dopants) and magnesium (p-type dopant). The n-type doping for GaN is simpler than the p-type doping because the related dopants have a lower activation energy and a much greater electronic mobility; moreover, before being able to act as an acceptor, magnesium must be separated from the hydrogen with which it forms compounds.

Usually the reagents for the production of GaN are put in a quartz furnace at $1000\,^{\circ}\mathrm{C}$ with a pressure lower than 100 atm for about 10 min. However, it is more common to find semiconductors in which the GaN crystals are made to grow as a thin film on a different bulk material (for example silicon, but also ZnO, sapphire, diamond and others); the most widespread manufacturing processes are molecular beam epitaxy (MBE), metal organic chemical vapor deposition (MOCVD) and hydride vapor phase epitaxy (HVPE, to which the reaction reported above refers). For commercial purposes the most used technique is the last one because the creation of the GaN film layers is two orders of magnitude faster than the other two while ensuring the absence of fractures, a low degree of impurities and a good efficiency of doping; the MBE instead guarantees an extremely high level of purity despite being very slow. Note that GaN's epitaxial growth techniques are now widely mastered, so the central issue here is the substrate material. The ideal bulk material would be the GaN itself because it makes possible the homoepitaxy without mismatch of the crystal lattice between substrate and thin film and therefore the density of dislocations would be low ($10^6\,\mathrm{cm}^2$). The problem is the production cost of bulk GaN,

about $100 euro/cm^2$, which is much more expensive than SiC: for this reason it is currently only available in small wafers.

Substrate	GaN	4H-SiC	Sapphire	Si
Crystal mismatch	Null	+3.5%	-16%	-17%
Thermal mismatch	Null	+33%	-25%	+113%
Electrical resistance	Low	Low	Very High	Very Low
Thermal resistance	-	0.3x	3x	0.9x
Wafer	2"	4"	8"	∀
Cost $[euro/cm^2]$	100	10	1	0.1

Table 2.3: Interface comparison of materials [17]

Currently, the best substrate available on the market could be silicon given its considerably low cost. Silicon wafers with a GaN epitaxial layer can be easily manufactured by conventional semiconductor production lines since the experimental validity of this heteroepitaxia in wafers up to 8 "has already been demonstrated; however it remains a difficult process: the big obstacle would be the high values of mismatch reported in table 2.3.

2.2.3 Conclusion

In conclusion, the breakdown electric field of gallium nitride and silicon carbide, which is higher than that of silicon, is the characteristic that allows operating at higher voltages and lower leakage currents. The high mobility and electronic saturation speed make it possible to operate at high frequencies (table 2.1). SiC has an electronic mobility lower than that of Si, while that of GaN is higher than all: this means that gallium nitride is the preferable material at higher frequencies. Greater thermal conductivity means a greater ability to conduct heat and therefore greater efficiency in higher temperature environments; silicon carbide has the highest thermal conductivity so it is able to operate better at higher power densities than silicon or gallium nitride. It could therefore be said that SiC is preferable when working in power applications, ie with high voltage and current values, while GaN is better used in the field of optoelectronics and radio frequencies, where the voltages remain relatively low and are required high breakdown electric fields. Considering the data provided by the main companies operating in the sector, it can be assumed that, taking into account the components currently on the market, for voltages higher than 1000 V it is better to use silicon carbide while at higher voltages low gallium nitride is preferable in most cases.

As can be seen in fig. 2.11, silicon has now reached its theoretical limits; for this reason it is necessary to use materials that allow for greater performance and consequently replace the current silicon components. It can also be said that the real challenge is currently played between GaN and SiC: silicon can still be competitive thanks to its low cost and ease of production but WBG semiconductors have much better physical characteristics (fig. 2.12).

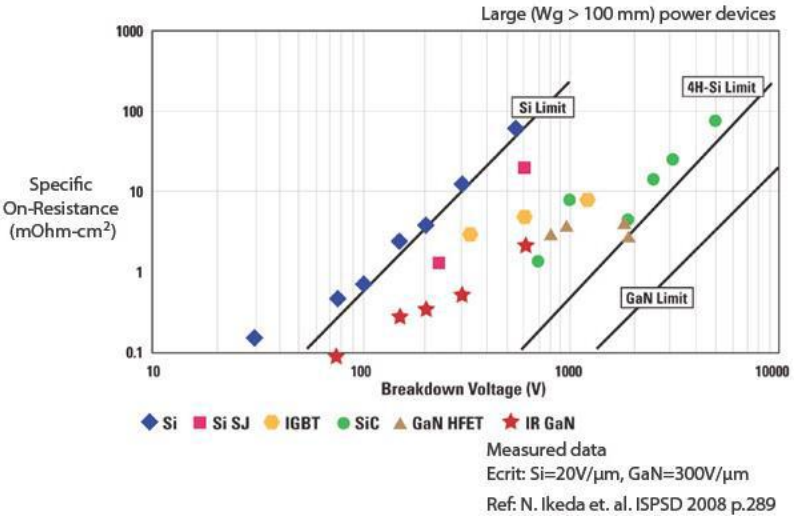

Figure 2.11: Comparison FoM Si vs SiC vs GaN

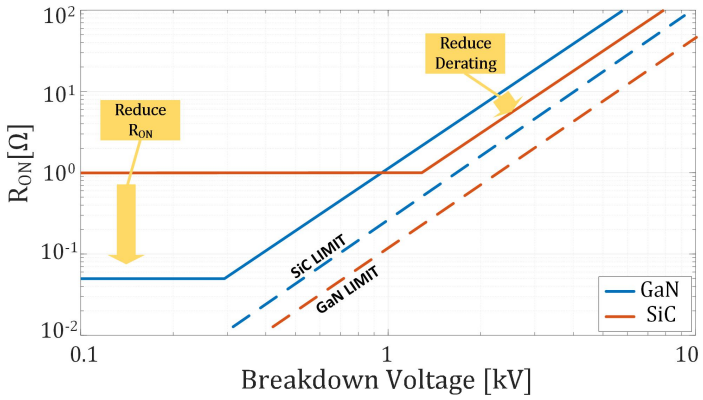

Figure 2.12: SiC vs. GaN: Today transistors of both materials face their respective challenges. Below about 1 kV GaN has the edge over SiC because of much lower channel resistances and above SiC is in the lead because of the necessary derating of GaN devices.[17]

In conclusion, the silicon carbide and gallium nitride components have superior performance to the silicon ones in almost every field of application.

2.3 SiC-based Power Converter

The SIC technologies began to be used in the 2000s in Power Factor Controller (PFC) applications with the adoption of SiC-Junction Barrier Schottky (SiC-JBS) diodes. Subsequently, other applications such as photovoltaics have opened the doors to the use of SIC

and FET, but the recent success is related to on-board chargers and DC-DC converters are driving the growth of SiC. Finally the recent adoption in the Electric Vehicle (EV) inverter, the grow of 650 V devices in multilevel application, and adoption in server supplies and 5G telecom rectifiers promises rapid growth.

2.3.1 SiC Device in Power converter

Advantages of using SiC FETs over IGBTs have been amply demonstrated [18–22]. According to (section 2.2) the wider bandgap of SiC allows to obtain voltage blocking layers with about 100 times less resistance than corresponding Silicon (Si) devices. SiC MOSFETs with steadily improving performance are now available from 650-1700V, both as planar [23] and trench structures[24]. At 1200V and above, silicon MOSFETs give way to IGBTs, which provide a lower conduction loss at high load currents, but since the lower conduction loss results from conductivity modulation, this comes with a penalty in switching losses. IGBTs are typically used with anti-parallel fast recovery PiN diodes, which also contribute to switching losses, since the stored charge in these diodes must be removed before the diodes can sustain an off-state voltage. In fig. 2.13 is compared the on-state characteristic of a SiC compared to a typical 200A, 1200V IGBT. At all operating conditions below 200A, lower conduction losses are possible with SiC, especially given the absence of a knee voltage. In fig. 2.14 is compared the third quadrant characteristics in freewheeling mode for IGBTs with Si Fast Recovery Diodess (FRDs), SiC FETs and SiC MOSFETs. In the absence of an antiparallel or integrated SiC Schottky diode, the conduction loss for SiC MOSFETs is much higher than for FRDs typically used with IGBTs. Both the SiC MOSFET and Cascode FET offer low Q_{RR} operation (often 10X lower than Si FRDs). Therefore, SiC FETs can switch much faster than their IGBT counterparts, but synchronous switching is a must for SiC MOSFETs to avoid excessive 3^{rd} quadrant conduction losses.[25, 26]. Furthermore, SiC also has 3X the thermal conductivity of Si to obtaining good results in high temperature environment.

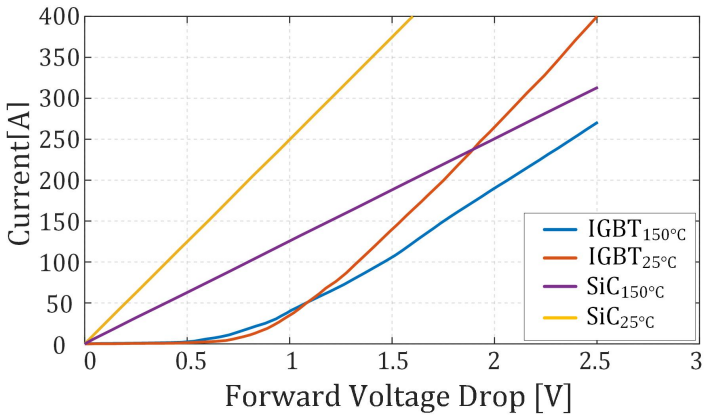

Figure 2.13: On-state voltage drop of SiC FETs vs IGBTs in 1st quadrant conduction

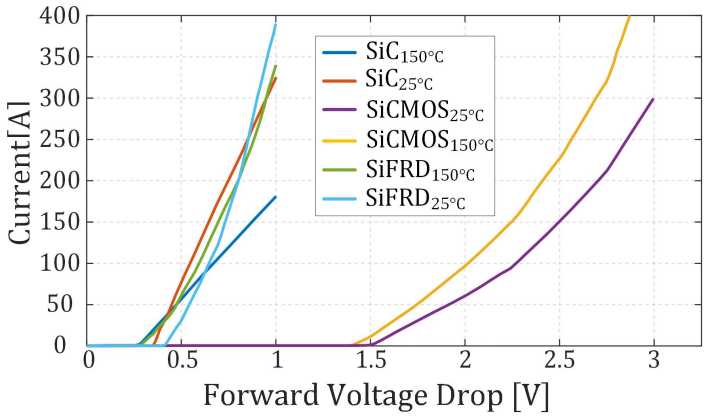

Figure 2.14: Typical 3rd quadrant conduction characteristics of Si FRDs used with IGBT, SiC FETs and SiC MOSFETs without the use of anti-parallel Schottky diodes

2.3.2 SiC Diodes in PFC and Boost converters

Since the absence of stored charge leads to much-reduced E_{ON} losses in the Field Effect Transistor (FET), then the use of SiC diodes in PFC circuits and boost converters is widespread. In fact, the advantage of using a SiC-JBS diode increases with voltage. Even without the use of SiC FETs as the main switching device, these diodes offer a path to increased efficiency and higher operating frequency [27–30].

2.3.3 SiC in hard switched circuits

table 2.4 captures the key datasheet parameters of interest when evaluating switch technologies for hard switched applications. For server power supplies, telecom rectifiers and onboard chargers that operate with bus voltages of 400V, the totem-pole PFC topology, or 3-phase active frontend rectifier may be used depending on power levels. Some benefits of use SiC device are:

1. An high switching frequencies allow to reduce the inductor size then improve power density and cut Bill Of Materials (BOM) costs.

2. All the SiC solutions offer excellent low Q_{RR} diodes, and consequently, much reduced E_{ON} losses in fact, high E_{ON} losses preclude the use of silicon superjunction FETs in Continuous Conduction Mode (CCM), even those with low Q_{RR}, due to excessive losses and poor recovery characteristics.

3. Used with Kelvin source packages, designers can push for 2-3X higher hard switching frequencies than obtained with Silicon. It also helps that all SiC FET options have a lower Temperature Coefficient of Resistance (TCR), i.e. a smaller increase of R_{ON} with temperature (table 2.4).

Parameter	Superjunction FETs	SIC FETs
R_{DS}@25 °C	8	0.75
R_{DS}@175 °C	24	1.5
$R_{DS} \cdot E_{oss}$	480	255
$R_{DS} \cdot Q_g$	4x	1x
$R_{DS} \cdot Q_{rr}$	100x	1x

Table 2.4: parameters useful for assessing technologies for hard switching [31]

2.3.4 SiC in soft-switched circuits

The use of the phase-shift full-bridge and Resonant Converter (LLC) circuit for DC-DC conversion is widespread, both in server power supplies and telecom rectifiers, as well as EV On Board Charger (OBC) and DC-DC converters. The value of wide-bandgap switches in general, and SiC based FETs in particular in these applications come from a few main characteristics:

1. SiC FETs have low C_{OSS}, which allows a fast V_{DS} transition at turn-on, which then allows the use of high switching frequency or wide input/output voltage ranges.

2. The turn-off loss with soft turn-on switching may be estimated as the measured hard switched turn-off energy minus the energy stored in the output capacitance, expressed as E_{OFF}-E_{OSS} and the turn-off energy is extremely low for SiC FETs.

3. Low $R_{DS_{ON}}$ values combined with high voltage ratings enable operation of DC-DC converters at 800V.

4. SiC FETs have low reverse recovery charge and very high voltage slew rate capability, in the range of 100 to 200 V/ns. This practically eliminates dv/dt induced failures without resorting to carrier lifetime reduction.

2.3.5 SiC in EV Traction Inverters

All the loss benefits of SiC FETs in hard switching provide much benefit in EV traction inverters, but if the operating frequencies for the motor drive are low, the main benefit must come from lower conduction losses. A key characteristic of the switch needed for EV applications is to withstand short circuit faults of various types. This requires the switch to withstand the entire bus voltage (400V for 650V devices, 800V for 1200V devices), while simultaneously conducting a high current when the gate is fully on, for a period of 2 µs ÷ 6 µs until the desaturation circuitry detects the short condition after an applied blanking time of 0.5 µs ÷ 2 µs. Then the driver tries to softly turn the switch off. During this time, the switch may experience a temperature rise of 300 °C ÷ 500 °C in a few µs, and must turn-off safely nonetheless. Furthermore, the switch should handle up to 100 or 1000 such events with no shift in device parameters. SiC devices are generally more robust

in this mode, since these vertical devices absorb the heat in their volume, whereas GaN High Electron Mobility Transistors (HEMTs) are lateral devices that develop the heat in the ultra-thin 2-D electron gas.

2.3.6 SiC Benefits for circuit protection

In SiC-Junction gate Field Effect Transistors (SiC-JFETs) device [32], as shows in fig. 2.15, V_{TH} does not decrease with temperature, this concept obtain an excellent current limiting and short circuit capability of SiC-JFETs, and the ability of SiC-JFET devices to withstand 4X higher energy dissipation than silicon devices before destruction, makes these devices very useful in circuit breakers [33], inrush current limiters and as load switches. SiC-JFETs offer the lowest available $R_{DS_{ON}}$ at a given chip size with lower operating conduction losses, without compromising the robustness of these devices to withstand repetitive overstress events.

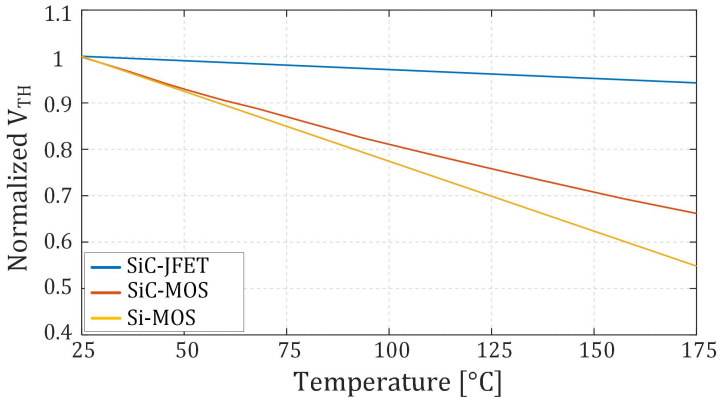

Figure 2.15: Normalized change in V_{TH} with temperature for Si MOSFETs, SiC JFETs and SiC MOSFETs.

2.4 Chapter bibliography

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Chapter 3

Front-end Power Converters

The research in the field of power converters has made significant progress in recent decades, in fact thanks above all to the continuous development of the semiconductor industry it has been possible to use different technologies to obtain devices with high performance in terms of power and switching frequency (section 2.2) . This has allowed, over the years, to build converters that are increasingly competitive on the market so as to be able to best meet the requirements of the various applications. It is important to point out that the specifications of a converter do not only concern the electrical characteristics but also the constructive ones such as weight and volume. In fact, for example, in the Automotive sector there is a demand for reduced volumes due to the physically limited space. In general, a significant feature common to all converters, especially those used in electric vehicles, is a high power density (W/cm^3).

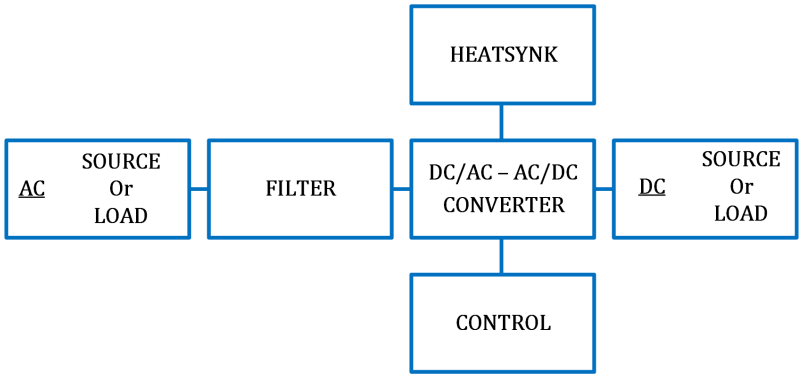


Figure 3.1: Power electronic converter structure

From a more generic point of view (fig. 3.1), a front-end *1-phase* or *3-phases* power converter is composed of different parts, each of which must be accurately evaluated in the design phase:

- Filter
- Active converter

- Control system
- Heatsynk system

3.1 PFC Rectifier

This chapter focuses on the study of front-end three-phase AC/DC electronic power converters capable of achieving a high power density. The objective is to analyze the typologies that are able to meet the requirements imposed by Power Quality compatibly with the use of Wide Band Gap (WBG) devices, in particular Silicon Carbide (SiC) diodes and switches.

The main electrical quantities of interest are summarized [34]:

The Power Factor (PF) is defined as the ratio between the modules of the active power and the apparent one, representing, in terms of power, the portion of active power supplied to the load and in sinusoidal voltage term according to eq. (3.1) where $\cos\phi_1$ represent the Displaicement Power Factor (DPF) in relation at fundamental sinusoidal term.

$$PF = \frac{P}{S} = \frac{V_s * I_{s1}\cos\varphi_1}{V_s I_s} = \frac{I_{s1}}{I_s}\cos\varphi_1 \quad \cos\varphi_1 = DPF \tag{3.1}$$

The Total Harmonic Distortion (THD) is an index of the distortion of the real waveform of the current with respect to the sinusoidal component. The THD is normally indicated in percentage terms.eq. (3.2).

$$THD_i = \frac{\sqrt{\sum_{n\neq 1} I_{1,rms}^2}}{I_{n,rms}} \tag{3.2}$$

There is a relationship that links the THD and the PF ($\cos\varphi$) of the network frequency quantities.(eq. (3.3))

$$PF = \frac{cos\varphi}{\sqrt{1 + {THD_i}^2}} = \frac{DPF}{\sqrt{1 + {THD_i}^2}} \tag{3.3}$$

Therefore, PF is influenced both by the phase shift of the quantities at the fundamental frequency and by the harmonic distortion. Ultimately, in order to obtain a PF value close to 1, it is necessary to maximize the power factor and minimize the THD.

In industrial applications the main rule for the development of rectifier in EN 61000-3-12[35] which concerns all electrical equipment directly connected to the public low-voltage distribution network with phase currents between 16 A and 75 A.

The table 3.1 shows the amplitude limits of the harmonics fed into the network based on the short-circuit ratio R_{SCE}.

A first classification (fig. 3.2) of front-end three-phase rectifiers is based on the nature of the systems used to control the PF: Passive, Hybrid, Active.

	I_h/I_{ref}					
R_{SCE}	I_3	I_5	I_7	I_9	I_{11}	I_{13}
33	21.6	10.7	7.2	3.8	3.1	2
66	24	13	8	5	4	3
120	27	15	10	6	5	4
250	35	20	13	9	8	6
>350	41	24	15	12	10	8

Table 3.1: Amplitude limits of harmonics

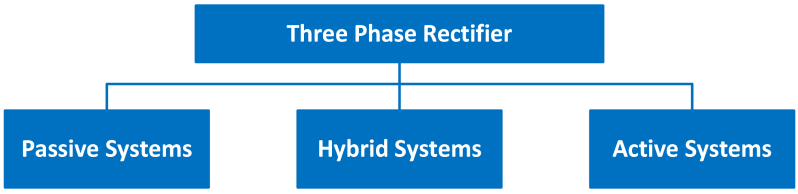


Figure 3.2: Class of Three phase Rectifier

3.1.1 Passive PFC

An uncontrolled rectifier used mains frequency (fig. 3.3) uses diodes to obtain an output waveform which is the envelope of the composition of the positive half-wave of the sinusoidal input voltages with the negative half-waves overturned with respect to the axis of the times. As can be seen from fig. 3.4, with this topology the input phase currents are strongly distorted with respect to the sinusoidal waveform. fig. 3.5 shows the phase current spectrum obtainable with two different values of the filter capacity, which shows the considerable amplitude of the current harmonics present.

The objective of the Power Factor Controller (PFC) is to obtain a power factor as close as possible to the unit and a low THD of the line current. To approach these values with diode rectifiers, various devices are used, from the simple one that provides for the addition of a DC side inductor (figs. 3.7 and 3.9) or AC side inductor (figs. 3.6 and 3.8) to more complex methods such as, for example, the "Passive Third Harmonics Injection" which can reduce the THD up to the value by about 5%, still obtaining values of the PF far from the unit [36].

3.1.2 Hybrid PFC

Hybrid systems are characterized by the use of active devices that switch to the network frequency. There are various topologies that try to obtain satisfactory results in terms of the quality of the current waveform, but present strong limits due to the low switching frequency which, being equal to those of the network , involves the use of very bulky and heavy passive components.

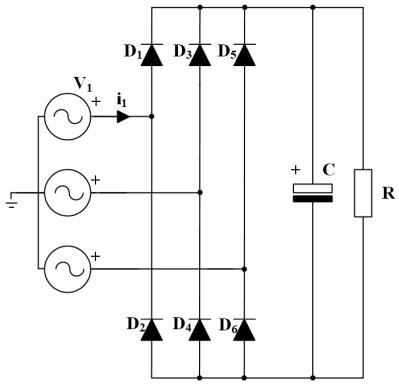


Figure 3.3: Diode Rectifier

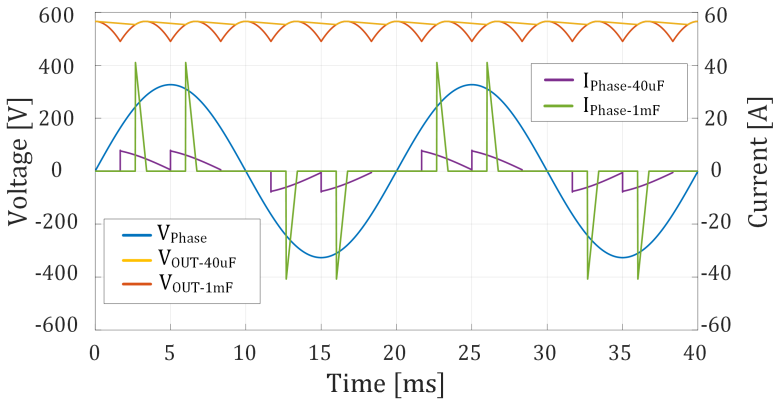


Figure 3.4: Typical phase voltages and currents of diode rectifiers

Among the best known, we cite the Minnesota topology (fig. 3.10) [37], which consists of a transformer and two boost converters that allow the control of the output voltage but with a low efficiency .

The Korea configuration [38] (fig. 3.11), on the other hand, has a high efficiency of around 99%, but does not allow to control the amplitude of the output voltage

Another hybrid topology is the "electronic inductor" cite [39] (fig. 3.12) which has good performances in terms of efficiency and power density.

Ultimately, the use of hybrid systems, even if it allows to obtain high performance values, for many applications is not convenient due to the low power density, moreover, the obtainable PF values, even if high, are not sufficient to satisfy the recent regulations imposed on the performance of converters.

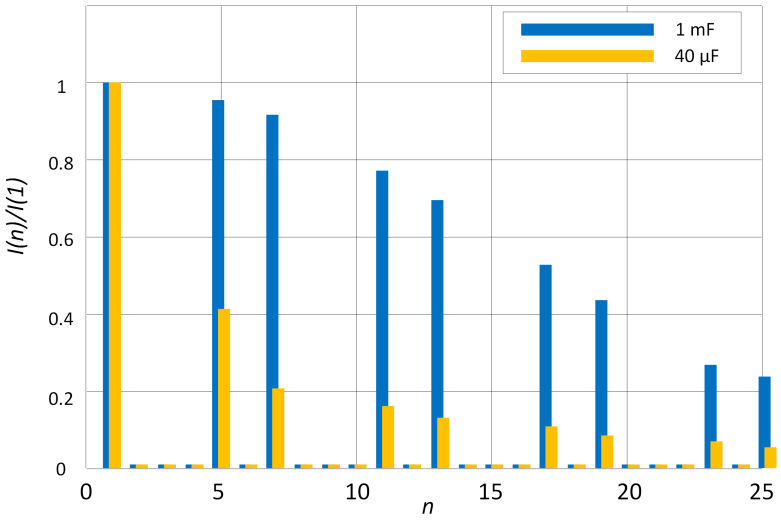


Figure 3.5: Rectifier current spectrum

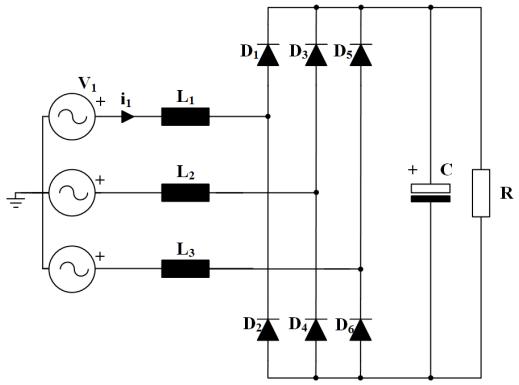


Figure 3.6: Passive PFC with AC side inductor

3.1.3 Active PFC

The most advanced class of rectifiers is that of rectifiers with Active PFC which allows to obtain converters with high efficiency and power density. These converters use high switching frequencies, therefore, the value of the passive components required undergoes a considerable reduction compared to the classes of converters considered previously.

This family of converters is divided into two large classes, as shown in fig. 3.13

Phase Modular Systems In the case of Phase Modular Systems converters, a single-phase rectifier is used for each of the three phases. The typologies belonging to this family are:

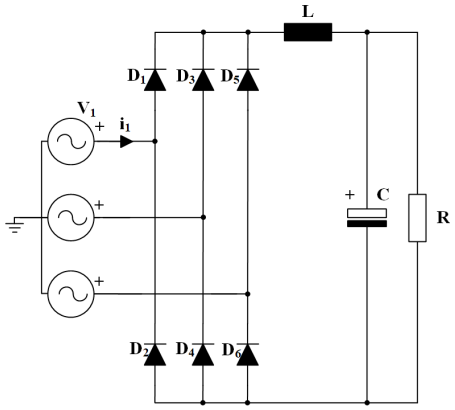


Figure 3.7: Passive PFC with DC side inductor

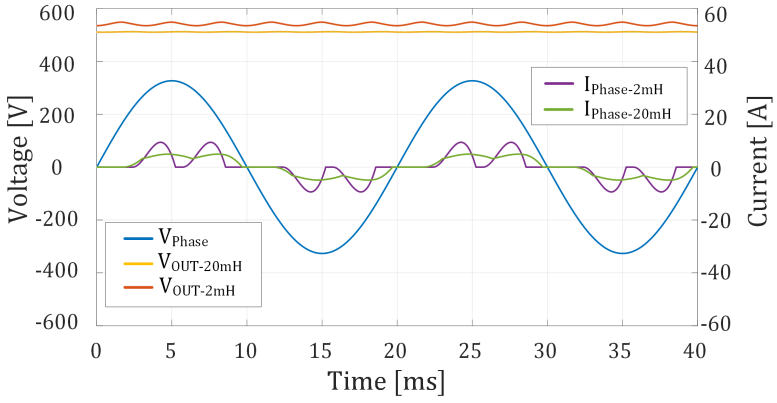


Figure 3.8: Typical phase voltages and currents of Passive PFC with AC side inductor

Wye-Rectifier The typology Wye-Rectifier (fig. 3.14) is often used for the realization of high power rectifiers or that operate with high input voltages (>400V). The converter can be seen as the set of three single-phase star-connected rectifiers, therefore, the devices used may have a lower voltage than the output voltage of the rectifier.

However, this typology requires an additional DC/DC stage (fig. 3.15) for balancing the output voltage of the individual phases, thus resulting in an increase in the components and complexity of the control algorithm to be implemented.

Delta Rectifier In the Delta topology (figs. 3.16 and 3.17), the devices are subjected to the maximum value of the Input voltage must therefore be suitably sized.

It has been shown that these topologies allow higher efficiency values than the "Why" topology which reaches 97% but, on the other hand, there is a worsening of the THD. In addition, the power density in this case also increases reaching interesting solutions with

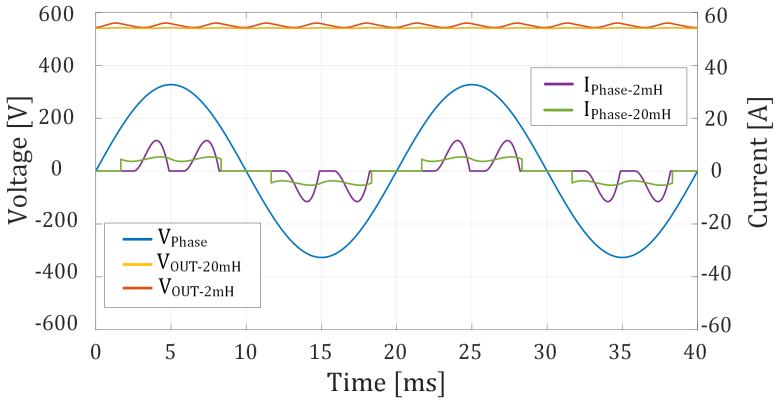


Figure 3.9: Typical phase voltages and currents of Passive PFC with DC side inductor

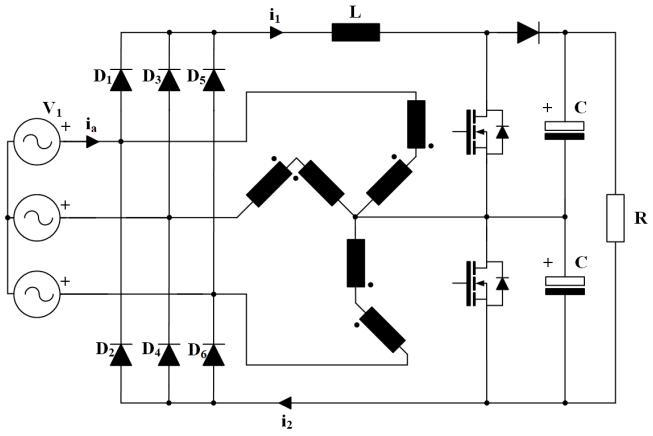


Figure 3.10: Minnesota topology

a value of $2400W/dm^3$ [40].

In conclusion, both topologies require high-value capacitors to compensate for the fluctuation of the instantaneous power of the individual phases as well as additional measures to balance the outputs.

Phase Modular Systems These rectifiers are made up of topologies that minimize the current ripple and the output unbalance, therefore, they allow to decrease the value of the output capacitance obtaining an improvement in terms of power density. As reported in fig. 3.18, they are classified in "Boost" topologies [41, 42] and “Buck” [43, 44].

The basic topology for these converters is shown in fig. 3.19 in which there is a single switching device. The standard control method is the Discontinuos Conduction Mode (DCM) (fig. 3.21) with a constant duty, without feedback. On the other hand, this strategy has several drawbacks among which high current peaks which require the oversizing of the

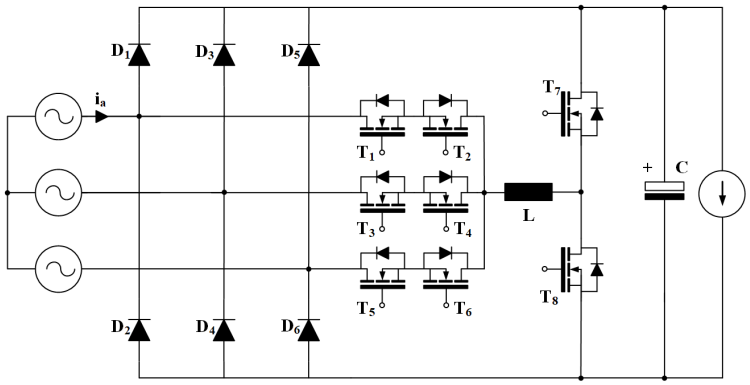


Figure 3.11: Korea topology

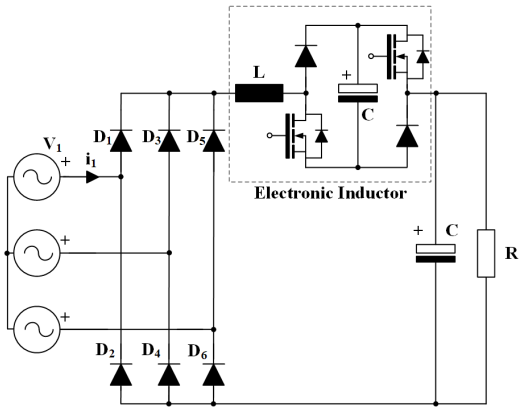


Figure 3.12: "Electronic Inductor" Topology

devices, the high value of the input inductance and nevertheless, a remaining current distortion which implies a high THD value.

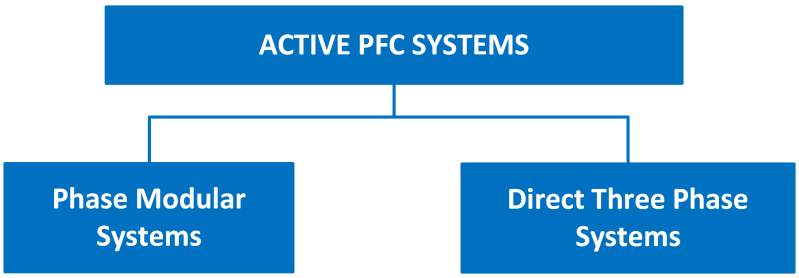


Figure 3.13: Active PFC

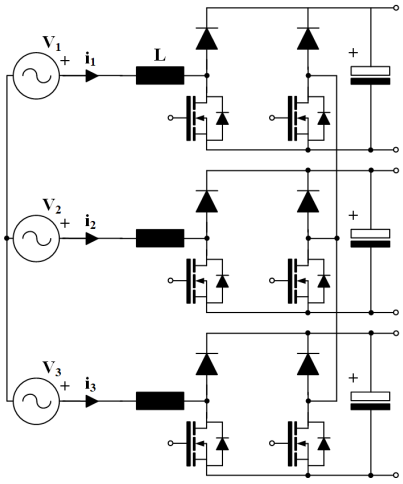


Figure 3.14: Wye Rectifier

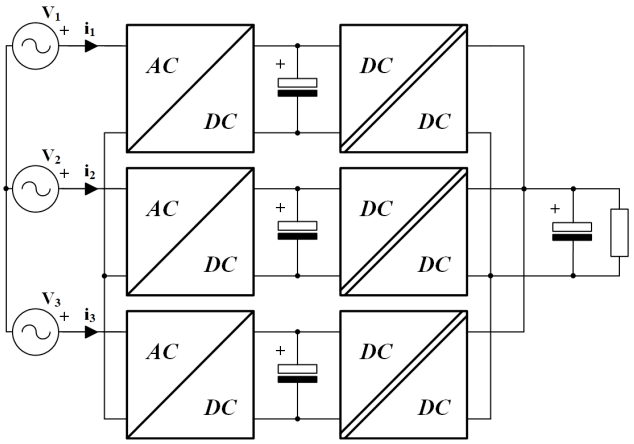


Figure 3.15: Balancing stage Wye-rectifier

Another control method widely used in the active current-controlled PFCs is the Continuous Conduction Mode (CCM) (fig. 3.20) which is characterized by the fact that the current in the input inductors is not canceled except by the passage of the zero of the fundamental component.

A further distinction of the converters is based on the number of voltage levels, divided into Two Level Converter (2LC) or Multi Level Converter (MLC). For example, with the same characteristics, a three-level rectifier has a lower current ripple with consequent possibility of reducing the value of the inductors of the boost stage with respect to a two levels. Furthermore the output devices and capacitors are subject to a halved working

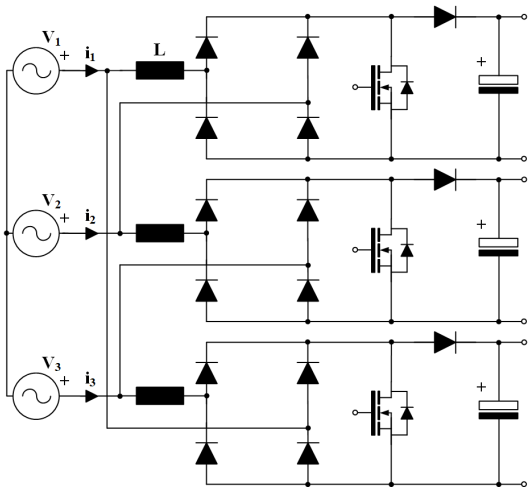


Figure 3.16: Delta Rectifier

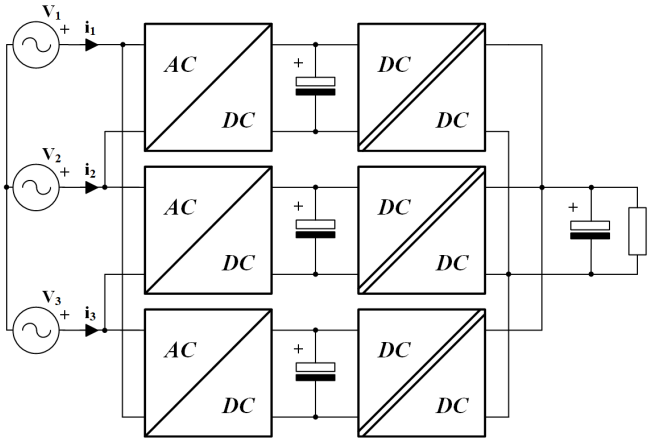


Figure 3.17: Balancing stage Delta-rectifier

voltage with respect to the total output voltage. This feature allows the use of devices with a lower nominal voltage, with obvious advantages in terms of performance and costs, according to section 3.3.2 and [45]. Moreover, these topologies exploit the characteristics of SiC devices which, in addition to having high Breakdown Voltage (BV) and low losses, allow working at higher frequencies than equivalent Silicon (Si) devices.

Vienna Rectifier A particular 3Levels three-phases rectifier scheme is the Vienna Rectifier (VR) which uses three bidirectional switches. This topology also has the intrinsic characteristic that, in the event of a short circuit fault in the device of a leg, the same

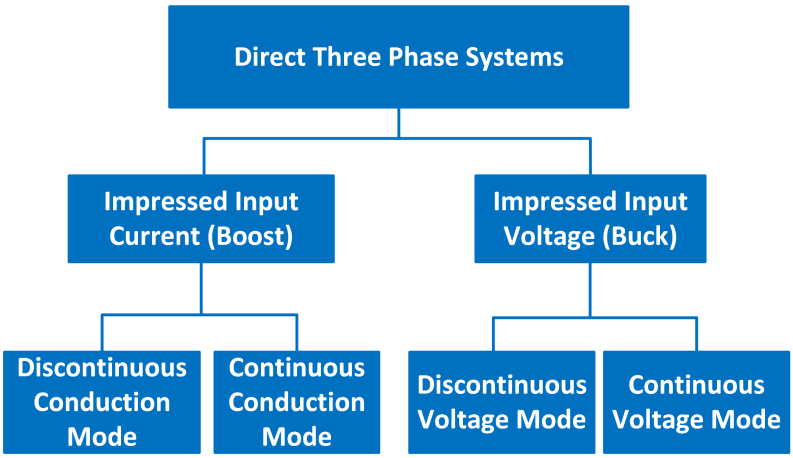


Figure 3.18: Direct Three Phase Systems

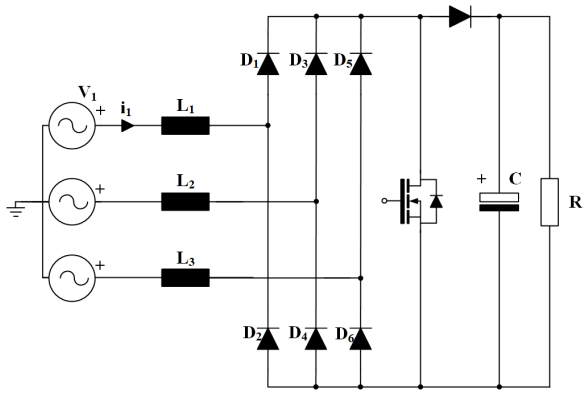


Figure 3.19: Boost Topology

short circuit is not reported either in input or output. The topology consists of an active device and 6 diodes per leg, as shown in fig. 3.22. [46]

In addition to the standard Vienna topology, there are various alternatives based on the same concept, one of which is the Six Switch Vienna Rectifier (6SVR) (fig. 3.23) used to reduce losses of conduction following the reduction of the number of diodes in series to the current paths.[47].

In fig. 3.24 a further diagram is shown which consists of a unidirectional T-Type converter controlled as a rectifier in which it is also necessary to use diodes able to withstand the entire output voltage . The advantage of this topology is the high efficiency that in the case of rectifiers from 10 kW at 50 Hz reaches 99%.

Another interesting topology is the Neutral Point Clamped - Simmetric Cascaded H-Bridges (NPC-SCHB) (fig. 3.25). The main advantage of this topology is the very high

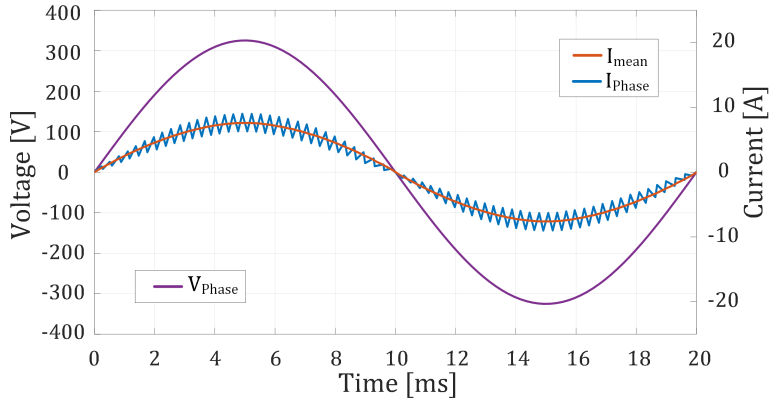


Figure 3.20: Continuos Conduction Mode

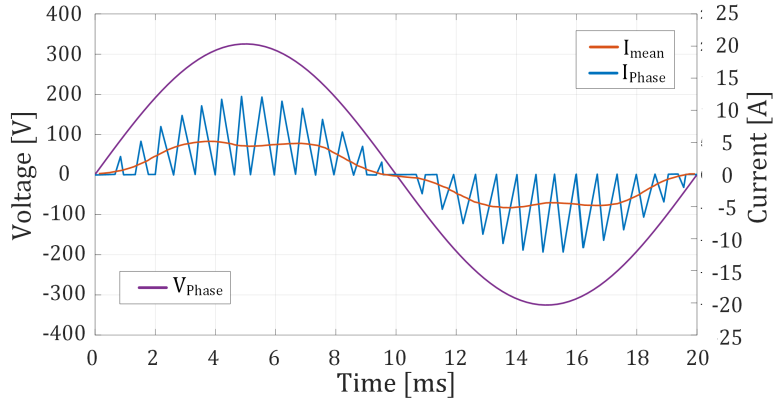


Figure 3.21: Discontinuos Conduction Mode

efficiency. For example, in a system with $f = 50Hz$ $f_{sw} = 70kHz$ it can reach 99% in a 10kW device even with the use of conventional Si devices [48].

As highlighted, MLC topologies allow the use of devices with lower BV than 2LC. However, considering a high-level rectifier with the aim of improving performance, we note that there is an unjustified increase in the resources required for the control and a considerable difficulty in realizing the topology.[49]

Further details on the characteristics of some controlled rectifiers Improved Power Quality AC / DC Coverters (IPQCs) are described in [50]

An overview of the topologies adopted showing their performance and taking into account the application fields is in [51]

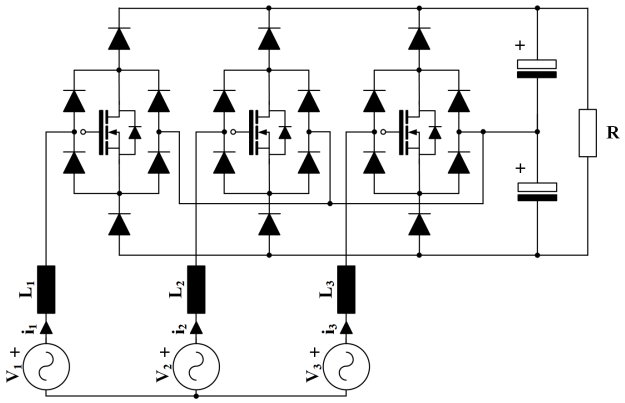


Figure 3.22: Original Vienna Topology

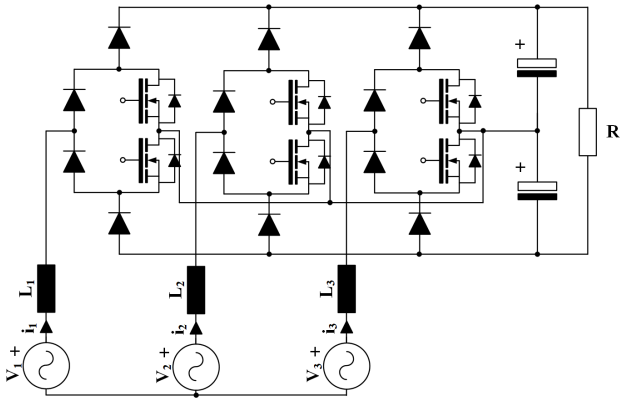


Figure 3.23: 6SVR Topology

3.2 Bidirectional converter

Currently an electric car, considering an average route, can cover about 150 km. Many companies, in collaboration with electricity suppliers, are building a dense network of recharging points. The best solution would be to use electricity produced from renewable sources to power cars. From this point of view the concept of "Mobile Smart Grid" is born, that is a complete system of hardware and software able to intelligently manage the interaction between Electric Vehicle (EV) or Plug-in Hybrid Electric Vehicle (PHEV), electrical networks and production units, to optimize the use of the network and production capacity. In such a system the batteries of electric cars will become points where they can store electricity, of an "intermittent" nature of renewable sources. This solution would transform the vehicle from a simple user to an integral and interconnected part with

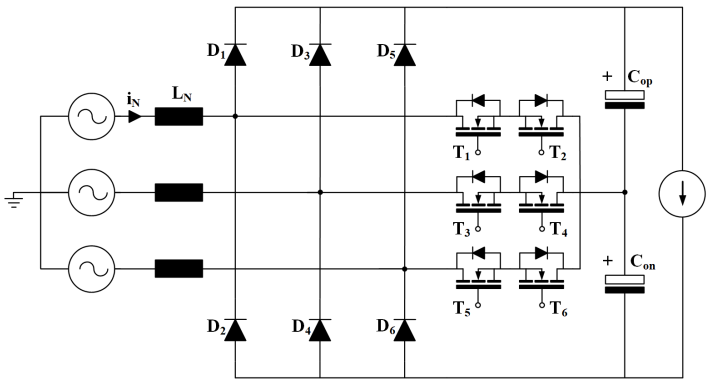


Figure 3.24: Vienna T-Type topology

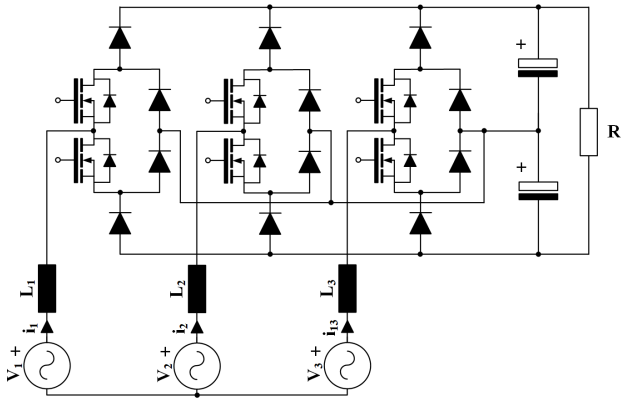


Figure 3.25: NPC-SCHB Topology

the smart grids themselves (fig. 3.26[1]). For these purposes two-way topologies have been developed both at two and at three levels.

The most widespread topology is the basic two-level six-switch (fig. 3.27) which is economical and simple to make but which has limitations in the switching frequency with consequent need for high-value boost inductors.

Interesting alternatives at three levels are instead made up of the Three Levels T-Type Coverter (3LTTC) (fig. 3.28) and the Three Levels Neutral Point Clamped Converter (3LNPCC) (fig. 3.29). Both have a high efficiency, obtaining the best results if used at high switching frequency. These topologies present greater circuit and control complexity, also in consideration of the large amount of devices to be controlled.

[1] Fleetcarma - The Latest in Vehicle to Grid (V2G) Charging

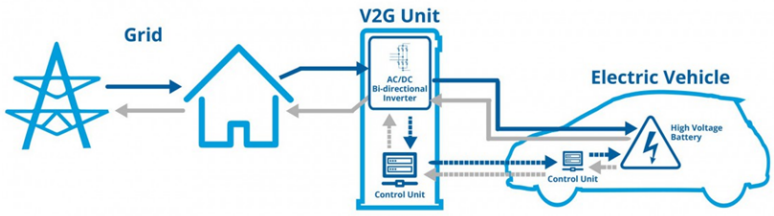


Figure 3.26: Vehicle to Grid concept

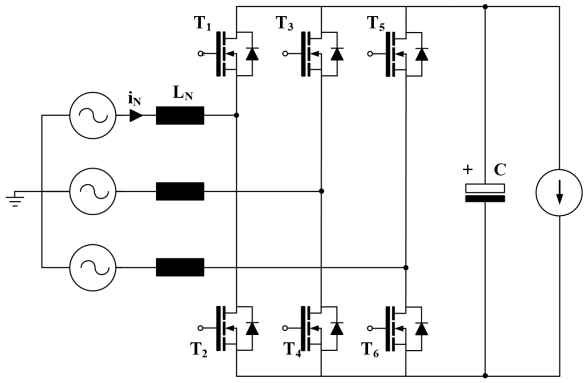


Figure 3.27: 3Phase 2Levels Converter

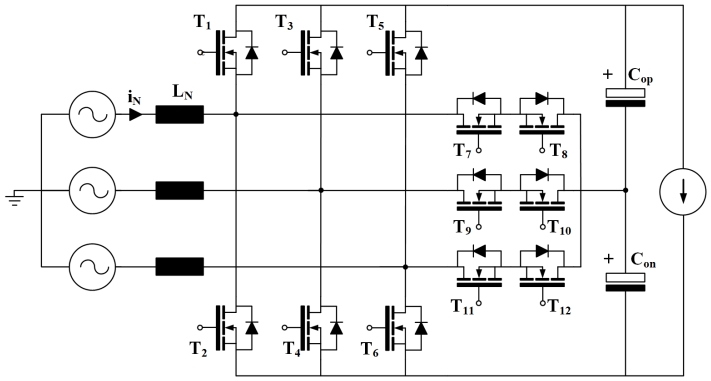


Figure 3.28: 3LTTC Topology

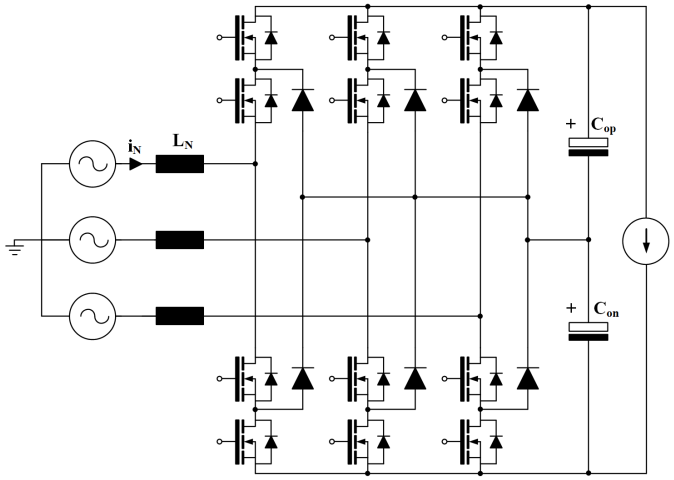


Figure 3.29: 3LNPC Topology

3.3 Comparison Three-Phase Topologies

A comparative study of the topologies highlighted in fig. 3.30 was performed considering the design specifications (table 3.2).

For completeness the work reported in the literature are reported ranging comparing the realization of converters 2-Levels or 3-Levels or the results obtained with SiC devices than the Si; In [52] it is shown that for a 42 kW 3LTTC converter operating at 25 kHz you can achieve losses of about 3-4 times lower than a 2LC. In [53] the benefits of using SiC against Si are demonstrated based on switching conduction losses. In [54] there is an increase in the efficiency of 3LNPCC and 3LTTC converters by 2% compared to 2LC converters.

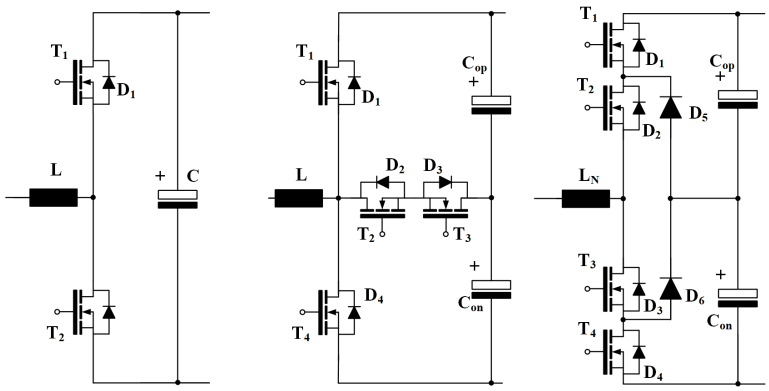


Figure 3.30: Focus on Phases of converters (*left:*2LC *center:*3LTTC *right:*3LNPCC)

Parameters	
$\hat{V_{LN}}$	$230V_{rms}$
V_{DC}	$800V$
ΔV_{DC}	5%
P	$12kW$
$\hat{I_L}$	$24A$

Table 3.2: Specifics of application

3.3.1 2-Levels Converter

2LC - Device stress Taking into account the specifications (table 3.2) of this comparative analysis, the analytical ralations of the electrical magnitudes of the topical 2LC in question are described. Considering the Root Mean Square (RMS) currents in eqs. (3.5) and (3.8) Average (AVG) currents in eqs. (3.4) and (3.7) and voltage stress in eqs. (3.6) and (3.9).

$$I_{avgT1,T2} = \frac{\hat{IL}}{2\pi}\left(1 + \frac{M\pi}{4}\cos\varphi\right) \tag{3.4}$$

$$I_{rmsT1,T2} = \sqrt{\frac{\hat{IL}^2}{2\pi}\left(\frac{\pi}{4} + \frac{2M}{3}\cos\varphi\right)} \tag{3.5}$$

$$V_{maxT1,T2} = V_{bus} \tag{3.6}$$

$$I_{avgD1,D2} = \frac{\hat{IL}}{2\pi}\left(1 - \frac{M\pi}{4}\cos\varphi\right) \tag{3.7}$$

$$I_{rmsD1,D2} = \sqrt{\frac{\hat{IL}^2}{2\pi}\left(\frac{\pi}{4} - \frac{2M}{3}\cos\varphi\right)} \tag{3.8}$$

$$V_{maxD1,D2} = V_{bus} \tag{3.9}$$

In fig. 3.31 it is clearly seen how the link with angle of phase displacement voltage-current φ modifies the working point of the devices and in particular in fig. 3.32 in both $Rectifier\varphi = 180°$ and $Inverter\varphi = 0°$.

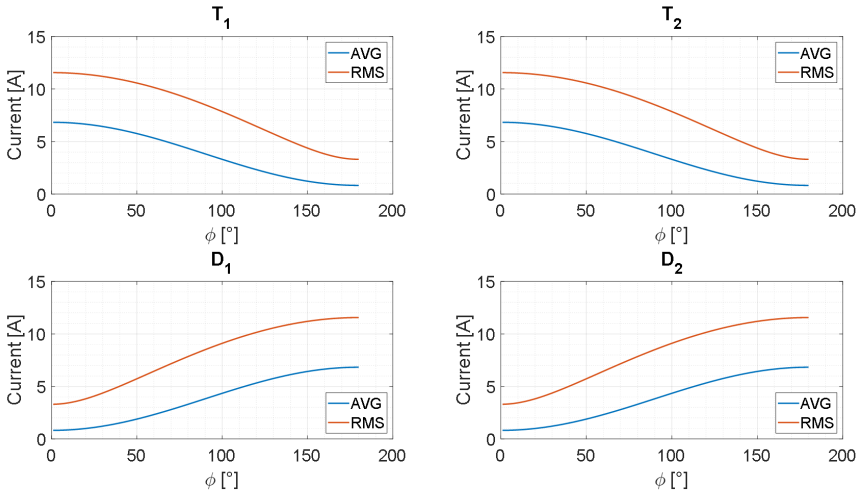


Figure 3.31: AVG and RMS current of each device in 2LC topology with varying φ

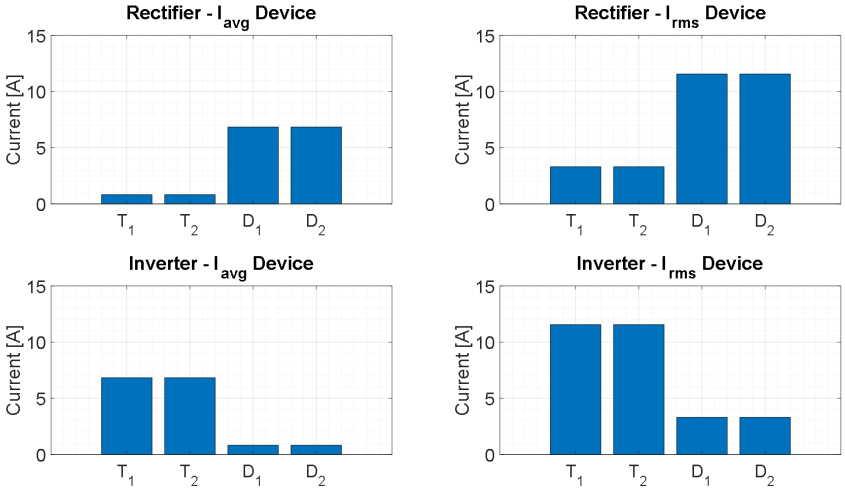


Figure 3.32: AVG and RMS current of each device in 2LC topology in $Rectifier\,\varphi = 180°$ and $Inverter\,\varphi = 0°$

3.3.2 3-Levels T-Type Converter

3LTTC - Device stress Also for the topology 3LTTC, considering the project specifications (table 3.2), the analytical equations of the electrical quantities are described, considering the RMS currents in eqs. (3.14) to (3.17), the AVG currents in eqs. (3.10) to (3.13) and the voltage stress in eqs. (3.18) to (3.21).

$$I_{avgT1,T4} = \frac{M\hat{IL}}{4\pi}\Big(\sin\varphi + \Big(\pi - \varphi\Big)\cos\varphi\Big) \tag{3.10}$$

$$I_{avgD1,D4} = \frac{M\hat{IL}}{4\pi}\Big(\sin\varphi - \varphi\cos\varphi\Big) \tag{3.11}$$

$$I_{\text{avg T2,T3}} = \frac{\hat{IL}}{4\pi}\Big(1 - \frac{M}{4}(2\sin\varphi - (2\varphi - \pi)\cos\varphi\Big) \tag{3.12}$$

$$I_{avgD2,D3} = \frac{\hat{IL}}{\pi}\Big(1 - \frac{M}{4}(2\sin\varphi - (2\varphi - \pi)\cos\varphi\Big) \tag{3.13}$$

$$I_{rmsT1,T4} = \sqrt{\frac{M\hat{IL}^2}{4\pi}\Big(\frac{8}{3}\sin^4\frac{\varphi}{2})\Big)} \tag{3.14}$$

$$I_{rmsD1,D4} = \sqrt{\frac{M\hat{IL}^2}{2}\Big(\frac{4}{3\pi}sin^4(\frac{\varphi}{2})\Big)} \tag{3.15}$$

$$I_{\text{rms T2,T3}} = \sqrt{\frac{\hat{IL}^2}{4\pi}\Big(1 - \frac{4M}{3\pi}\cos^2\varphi\Big)} \tag{3.16}$$

$$I_{rmsD2,D3} = \sqrt{\frac{\hat{IL}^2}{4}\Big(1 - \frac{4M}{3\pi}(1 + \cos^2\varphi)\Big)} \tag{3.17}$$

$$V_{maxT1,T4} = \frac{V_{bus}}{2} \tag{3.18}$$

$$V_{maxD1,D4} = V_{bus} \tag{3.19}$$

$$V_{\text{max T2,T3}} = \frac{V_{bus}}{2} \tag{3.20}$$

$$V_{\text{max D2,D3}} = \frac{V_{bus}}{2} \tag{3.21}$$

In fig. 3.33 we clearly see how the link with the phase-shift voltage-current φ affects the working point of the devices and in particular in fig. 3.34 are shown the work points varying φ and in $Rectifier\varphi = 180°$ $Inverter\varphi = 0°$.

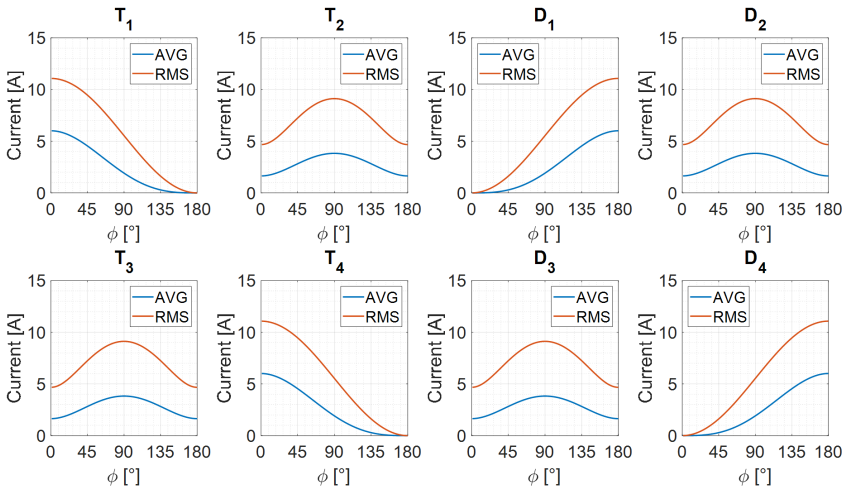


Figure 3.33: AVG and RMS current of each device in 3LTTC topology with varying φ

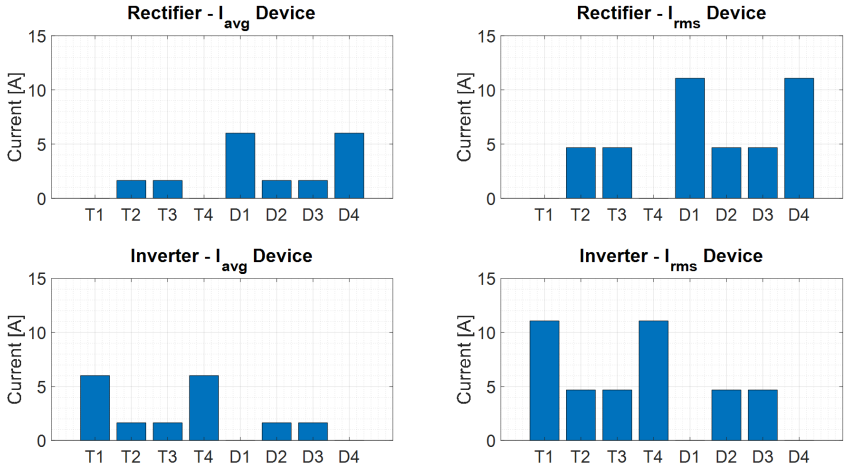


Figure 3.34: AVG and RMS current of each device in 3LTTC topology in *Rectifier* $\varphi = 180°$ and *Inverter* $\varphi = 0°$

3.3.3 3-Levels NPC Converter

DEVICE STRESS – 3LNPCC Finally, for the topology, 3LNPCC considering the project specifications (table 3.2), the analytical equations of the electrical quantities of the examined topology are described, considering the RMS currents in eqs. (3.17) and (3.27) to (3.31), AVG currents in eqs. (3.22) to (3.26) and the voltage stress in eqs. (3.32) to (3.36).

$$I_{\text{avgT1,T4}} = \frac{M\hat{IL}}{4\pi}\Big(\sin\varphi + (\pi-\varphi)\cos\varphi\Big) \tag{3.22}$$

$$I_{\text{avg D1,D4}} = \frac{M\hat{IL}}{4\pi}\Big(\sin\varphi - \varphi\cos\varphi)\Big) \tag{3.23}$$

$$I_{\text{avg T2,T3}} = \frac{\hat{IL}}{4\pi}\Big(1 - \frac{M}{4}(\sin\varphi - \varphi\cos\varphi)\Big) \tag{3.24}$$

$$I_{\text{avg D2,D3}} = \frac{M\hat{IL}}{4\pi}\Big(\sin\varphi - \varphi\cos\varphi\Big) \tag{3.25}$$

$$I_{\text{avg D5,D6}} = \frac{\hat{IL}}{\pi}\Big(1 - \frac{M}{4}(2\sin\varphi - (2\varphi-\pi)\cos\varphi\Big) \tag{3.26}$$

$$I_{\text{rms T1,T4}} = \sqrt{\frac{M\hat{IL}^2}{4\pi}\Big(\frac{8}{3}\sin^4\frac{\varphi}{2}\Big)} \tag{3.27}$$

$$I_{rmsD1,D4} = \sqrt{\frac{M\hat{IL}^2}{2}\Big(\frac{4}{3\pi}\sin^4\frac{\varphi}{2}\Big)} \tag{3.28}$$

$$I_{rmsT2,T3} = \sqrt{\frac{r_{0,T}\hat{IL}^2}{4\pi}\Big(1 - \frac{8M}{3\pi}\sin^4\frac{\varphi}{2}\Big)} \tag{3.29}$$

$$I_{rmsD2,D3} = \sqrt{\frac{r_{0,D}M\hat{IL}^2}{4\pi}\Big(\frac{4}{3\pi}\sin^4\frac{\varphi}{2}\Big)} \tag{3.30}$$

$$I_{rmsD5,D6} = \sqrt{\frac{\hat{IL}^2}{4}\Big(1 - \frac{4M}{3\pi}(1+\cos^2\varphi)\Big)} \tag{3.31}$$

$$V_{maxT1,T4} = \frac{V_{bus}}{2} \tag{3.32}$$

$$V_{maxD1,D4} = \frac{V_{bus}}{2} \tag{3.33}$$

$$V_{maxT2,T3} = \frac{V_{bus}}{2} \tag{3.34}$$

$$V_{maxD2,D3} = \frac{V_{bus}}{2} \tag{3.35}$$

$$V_{maxD5,D6} = \frac{V_{bus}}{2} \tag{3.36}$$

In fig. 3.35 it is clearly seen how the link with the angle of phase displacement of the voltage φ influences the working point of the devices and in particular in fig. 3.36 the working points are shown in the conditions $Rectifier\varphi = 180°$ $Inverter\varphi = 0°$.

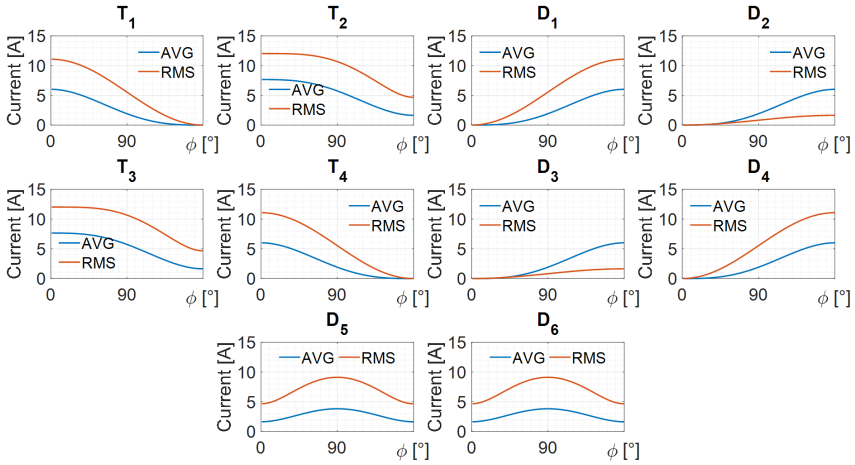


Figure 3.35: AVG and RMS current of each device in 3LNPCC topology with varying φ

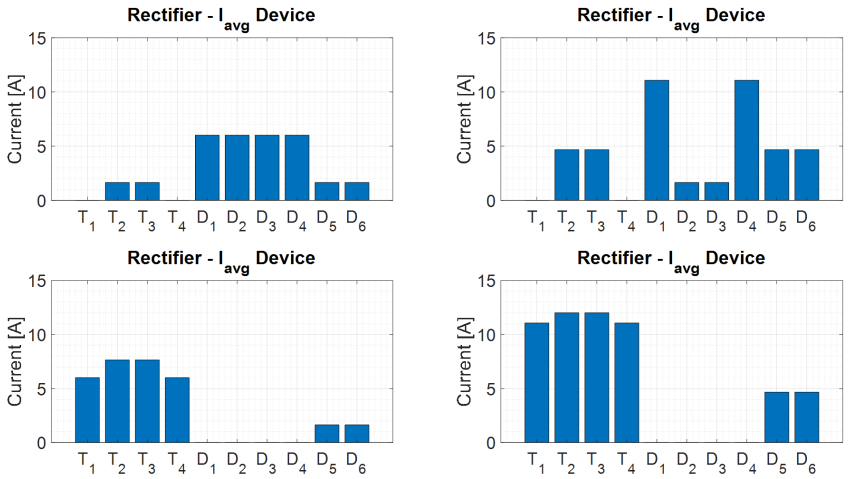


Figure 3.36: AVG and RMS current of each device in 3LNPCC topology in *Rectifier* $\varphi = 180°$ and *Inverter* $\varphi = 0°$

3.3.4 Device stress

Analyzing the relation of the operating voltages, 3LNPCC (eqs. (3.32) to (3.36)), 3LTTC (eqs. (3.18) to (3.21),) and 2LC (eqs. (3.6) and (3.9)) has been noted that the main distinction concerning the three topologies is that the 2LC needs the use of devices with an BV greater than V_{DC} and the same also for the devices of the vertical leg $T_1 - D_1$ and $T_4 - D_4$ of the converter 3LTTC, instead for the devices of the horizontal leg $T_2 - D_2$ and $T_3 - D_3$ of the 3LTTC and for all the converter devices 3LNPCC devices can be used with BV greater than $V_{DC}/2$ which have more performing parameters in terms of switching

losses.

The first comparative analysis takes into account table 3.3 considering the use of SiC Metal Oxide Semiconductor Field Effect Transistors (MOSFETs) and SiC diodes by STMicroelectronics.

	2LC	3LNPCC	3LTTC
$T_1\|D_1$	SCT30N120	SCTH35N65G2	SCT30N120
$T_2\|D_2$	SCT30N120	SCTH35N65G2	SCTH35N65G2
$T_3\|D_3$	-	SCTH35N65G2	SCTH35N65G2
$T_4\|D_4$	-	SCTH35N65G2	SCT30N120
D_5	-	STPSC20065	-
D_6	-	STPSC20065	-

Table 3.3: Summary data of SiC MOSFETs and diodes used for comparison in the individual topologies

3.3.5 Converter Losses comparison

The conversion losses in the inverter can be divided in two categories.

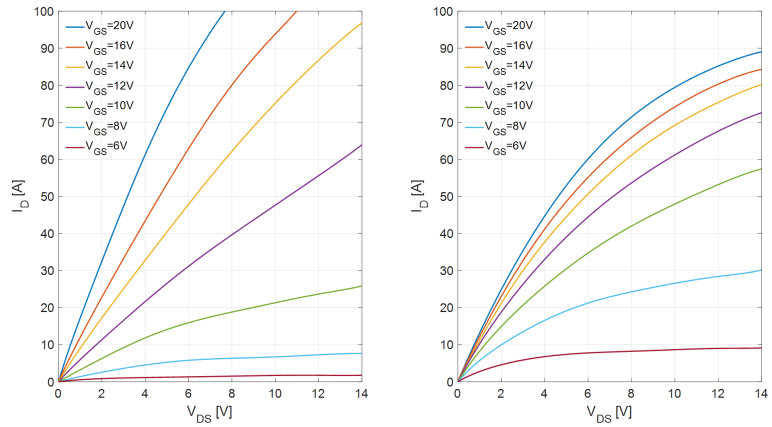
- Conduction loss P_C
- Switching loss P_S

Conduction losses The conduction losses are due to device on-state voltage drop. They calculated by averaging the conduction losses in each switching cycle as shown in eq. (3.37). Where P_C is the total device conduction losses, switching period is T. $V_f(t)$ is the forward voltage of the device, $i(t)$ is the current flow through the device in the conduction period. The value of $V_f(t)$ is calculated in eq. (3.38).

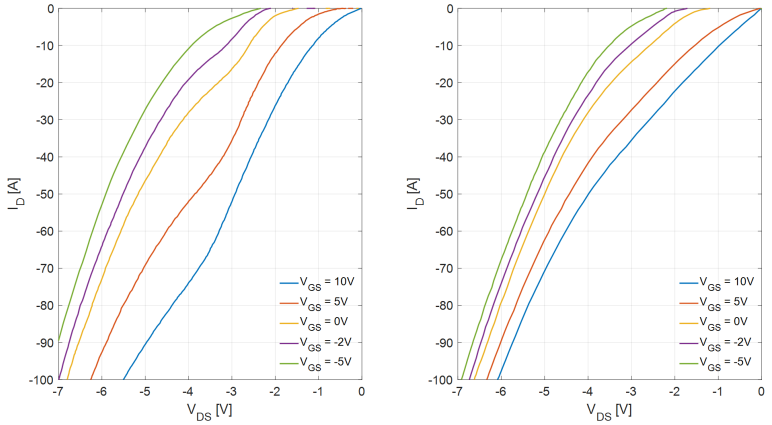
$$P_C = \frac{1}{T}\int_0^T V_f(t)i(t)dt \tag{3.37}$$

$$V_f = V_{f0} + r_f i(t) \tag{3.38}$$

Where V_{f0} is the device forward voltage at no load and device forward resistance is r_f. The values of V_{f0} and r_f are calculated using the datasheet of device characteristics provided by manufacturing companies as shown in fig. 3.37. The r_f, in the IGBT, is the ratio between the collector emitter voltage difference and the collector current difference $r_f = \Delta V_{ce}/\Delta I_c$ while V_{f0} is the value in the curve corresponding to the actual collector current flow in the device. Substituting the eq. (3.38) into eq. (3.37) and using the definition eqs. (3.39) and (3.40) gives eq. (3.41) or according to a MOSFET datasheet in eq. (3.42)



(a) Forward



(b) Reverse

Figure 3.37: Output characteristic SCTH35N65 $T_J = 25 - 175°C$.

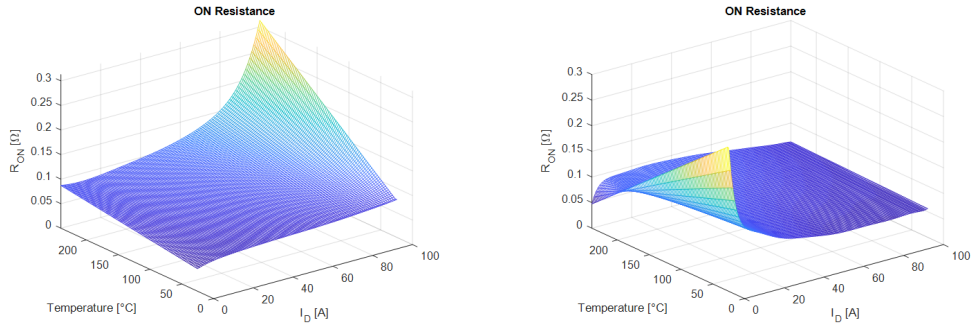
$$i_{avg} = \frac{1}{T}\int_0^T i_o(t)dt \tag{3.39}$$

$$i_{rms}^2 = \frac{1}{T}\int_0^T i_o^2(t)dt \tag{3.40}$$

$$P_C = V_f I_{avg} + r_f I_{rms}^2 \tag{3.41}$$

$$P_C = R_{DS_{ON}} I_{rms}^2 \quad , \quad r_f = R_{DS_{ON}} \tag{3.42}$$

Switching losses The switching losses are the total sum of on-state switching losses and turn-off switching losses. They depend on the device characteristics, switching frequency



(a) Forward (b) Reverse

Figure 3.38: Processed $r_T(i,T)$, obtained by MATLAB®

and device current. The switching loss for the device is calculated as eq. (3.43)

$$P_S = \frac{f_s}{2\pi}\int_0^{T_S} k_1 i d\omega t = \frac{k_1 f_s}{2\pi}\int_0^{\pi+\theta} I_m \sin(\omega t - \theta) d\omega t = \frac{k_1 f_s I_m}{\pi} = \frac{f_s}{\pi} E_{sw} I_m \tag{3.43}$$

Where k_1 is got from the switching energy graph in the device datasheet.

The comparison considers the switching and conduction losses [45, 55–57] taking into account the three topologies of fig. 3.30, in a range of frequencies of $10\,\text{kHz} \div 100\,\text{kHz}$ hertz and the operating conditions of the table 3.2.

2LC - Power Losses

Conduction losses In a converter, 2LC as shown by eqs. (3.44) and (3.45), the contribution of conduction losses between $T_1 - T_2$ and $D_1 - D_2$ is related and counterbalanced to the phase shift φ which quantifies the current passing through the single device (section 3.3.1). In fig. 3.39 and **??**, the results obtained are shown.

$$P_{C\,T1,T2} = \frac{V_{0,T}\hat{IL}}{2\pi}\left(1 + \frac{M\pi}{4}\cos\varphi\right) + \frac{r_{0,T}\hat{IL}^2}{2\pi}\left(\frac{\pi}{4} + \frac{2M}{3}\cos\varphi\right)^2 \tag{3.44}$$

$$P_{C\,D1,D2} = \frac{V_{0,D}\hat{IL}}{2\pi}\left(1 - \frac{M\pi}{4}\cos\varphi\right) + \frac{r_{0,D}\hat{IL}^2}{2\pi}\left(\frac{\pi}{4} - \frac{2M}{3}\cos\varphi\right)^3 \tag{3.45}$$

[2] $V_{0,T}$: Value of initial transistor voltage drop and $r_{0,T}$: Value of transistor incremental resistance

[3] $V_{0,D}$: Value of initial diode voltage dropand $r_{0,D}$: Value of diode incremental resistance

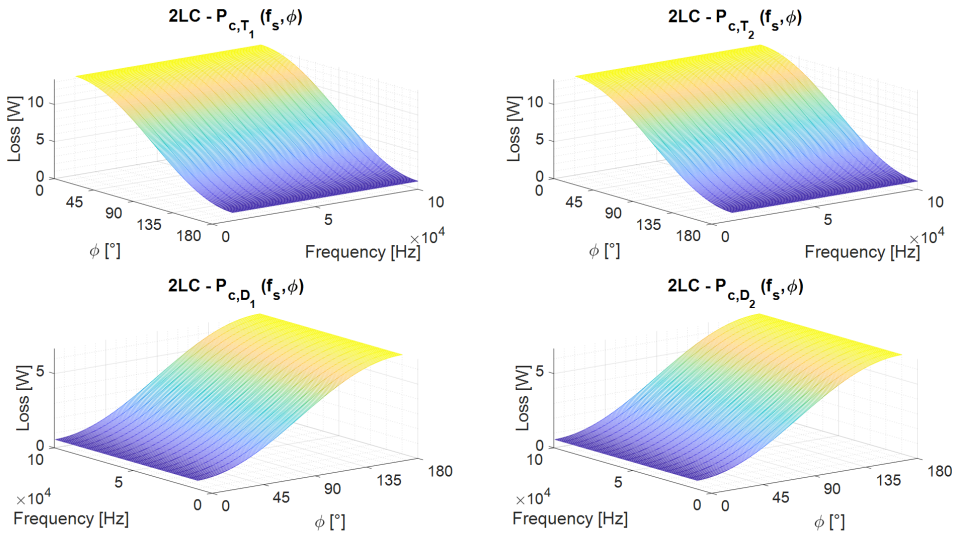


Figure 3.39: Conduction losses in 2LC topology with varying φ and f_{SW}

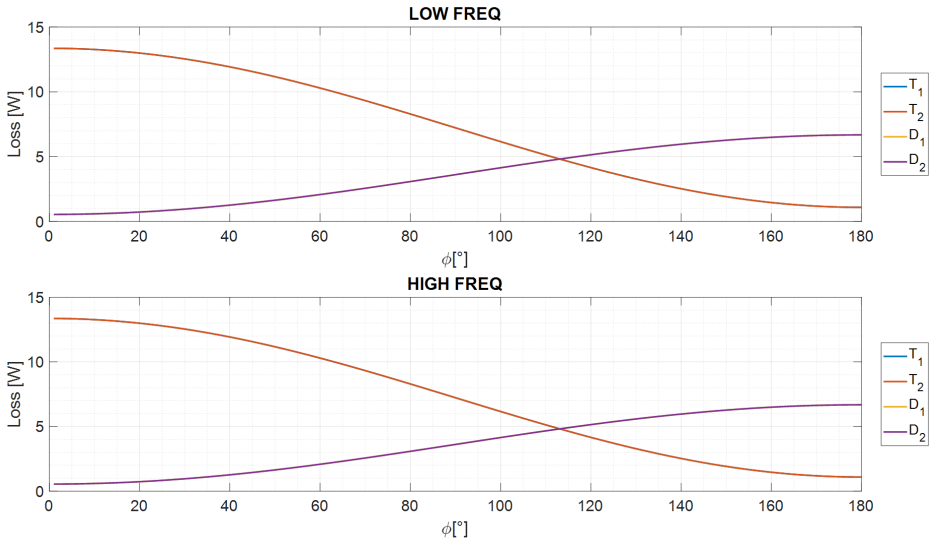


Figure 3.40: Conduction losses in 2LC topology at $f_{SW} = 10\,\text{kHz}, 100\,\text{kHz}$ varying φ

Switching losses Switching losses in 2LC, related to the f_{SW} according to eqs. (3.46) and (3.47) where V_{ref} and I_{ref} represent the correction parameters and π that represents the duration of the sinusoidal half-wave.

$$P_{ST1,T2} = \frac{f_s}{\pi}(E_{on} + E_{off})\frac{Vdc}{V_{ref}}\frac{\hat{IL}}{I_{ref}} \tag{3.46}$$

$$P_{S\,D1,D2} = \frac{f_s}{\pi} E_{err} \frac{V_{dc}}{V_{ref}} \frac{\hat{IL}}{I_{ref}} \tag{3.47}$$

In the switching losses of 2LC, shown in fig. 3.41, the increase with frequency does not show any dependence on the phase shift φ and this consideration is verified in fig. 3.42 where the behavior on both sides of the analyzed frequency range is highlighted ($f_{sw} = 10kHz \div 100kHz$)

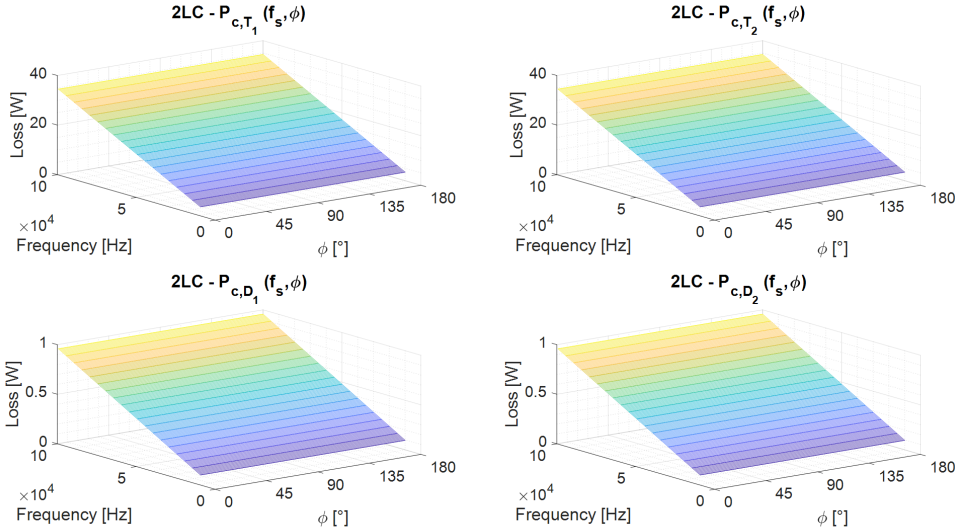


Figure 3.41: Switching losses in 2LC topology with varying φ and f_{SW}

Switching and conduction losses percentages for individual devices in $Rectifier\varphi = 180°$ $Inverter\varphi = 0°$, are shown in fig. 3.43, which gives information on the contribution of each device.

In conclusion, in fig. 3.44 are shown the total losses contribution of the single devices in 2LC converter and the relative switching and conduction losses expressed in $Watt$ (fig. 3.45) and in global form in fig. 3.46

In fig. 3.47 the global results of the converter are shown distinguishing the total switching conduction losses and the efficiency with variations of f_{sw} and φ while in fig. 3.48 the efficiencies of the converter in the two operating conditions are shown at varying frequency.

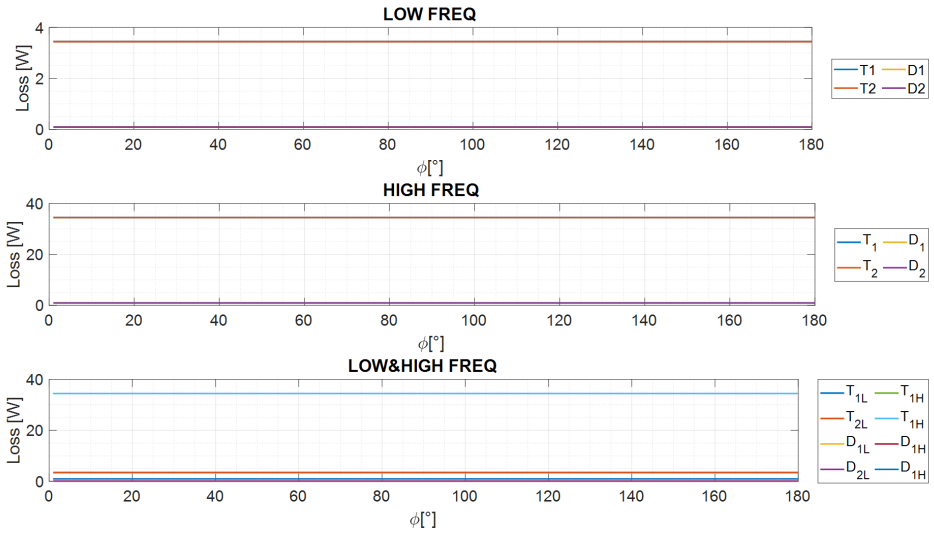
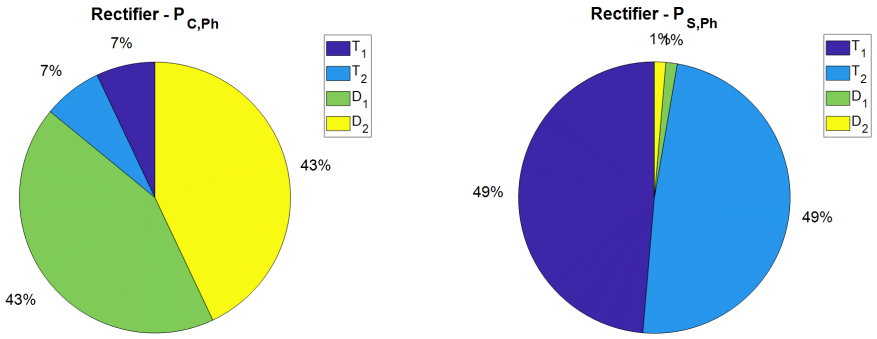
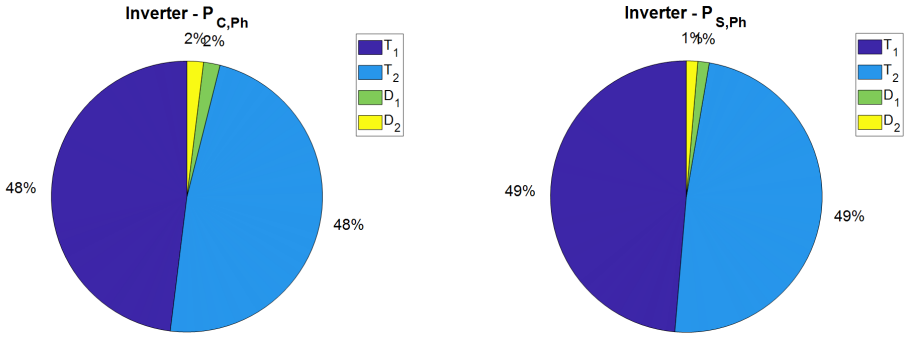


Figure 3.42: Switching losses in 2LC topology at $f_{SW} = 10\,\text{kHz}, 100\,\text{kHz}$ varying φ



(a) Rectifier



(b) Inverter

Figure 3.43: Contribution of each device in Switching and conduction losses for 2LC

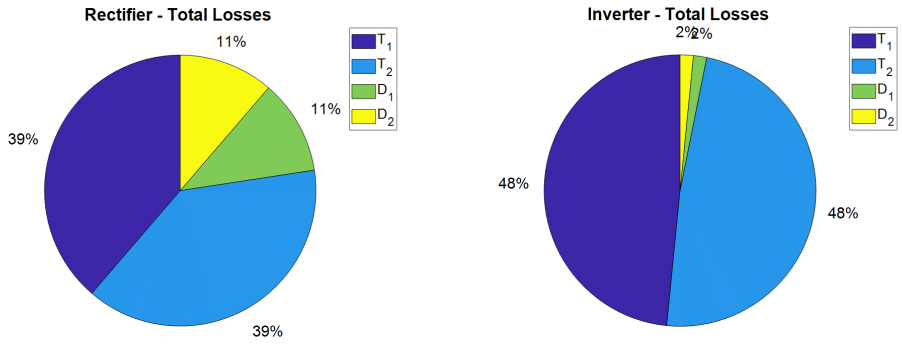


Figure 3.44: Total losses percentages for each devices in 2LC

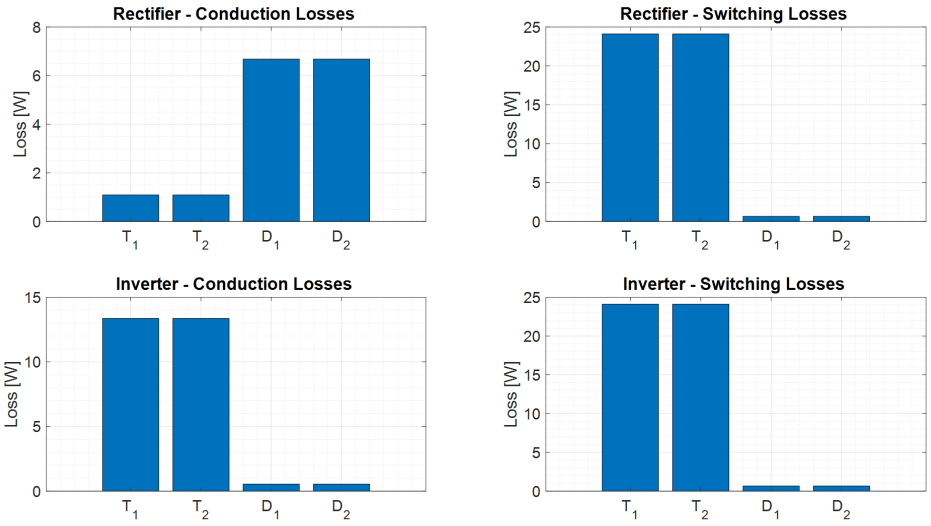


Figure 3.45: Contributions in conduction and switching losses of various devices in 2LC

Figure 3.46: Contributions of the total losses of the various devices in 2LC

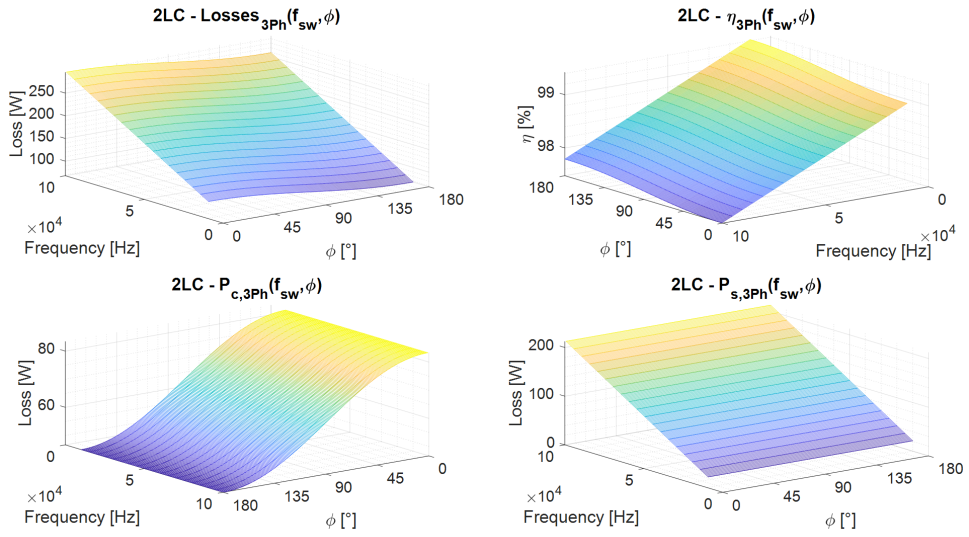


Figure 3.47: Switching losses, conduction, totals and efficiency of the 2LC global converter varying f_{sw} and φ

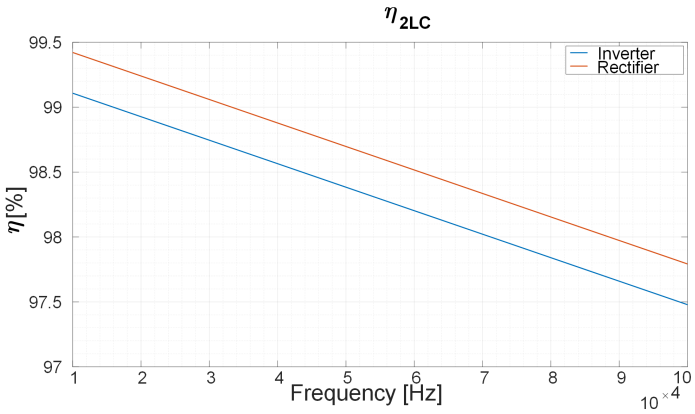


Figure 3.48: Efficiency of the 2LC converter with varying f_{sw}, in $Rectifier\varphi = 180°$ and $Inverter\varphi = 0°$

3LNPCC - Power Losses

Conduction losses In the case of 3LNPCC the conduction losses are shown in **??**, and also in this topology there is a direct dependence with φ (section 3.3.3). In fig. 3.49 the results and in fig. 3.50 a focus in low frequency condition $f_{SW} = 10kHz$ and $f_{SW} = 100kHz$ are shown.

$$
\begin{aligned}
P_{C\,T1,T4} &= \frac{V_{0,T} M \hat{IL}}{4\pi}\left(\sin\varphi + (\pi-\varphi)\cos\varphi\right) + \frac{r_{0,T} M \hat{IL}^2}{4\pi}\left(\frac{8}{3}\sin^4\frac{\varphi}{2}\right) \\
P_{C\,D1,D4} &= \frac{V_{0,T} M \hat{IL}}{4\pi}\left(\sin\varphi - \varphi\cos\varphi\right) + \frac{r_{0,T} M \hat{IL}^2}{4\pi}\left(\frac{4}{3\pi}\sin^4\frac{\varphi}{2}\right) \\
P_{C\,T2,T3} &= \frac{V_{0,T} \hat{IL}}{4\pi}\left(1 - \frac{M}{4}\left(\sin\varphi - \varphi\cos\varphi\right)\right) + \frac{r_{0,T} \hat{IL}^2}{4\pi}\left(1 - \frac{8M}{3\pi}\sin^4\frac{\varphi}{2}\right) \\
P_{C\,D2,D3} &= \frac{V_{0,D} M \hat{IL}}{4\pi}\left(\sin\varphi - \varphi\cos\varphi\right) + \frac{r_{0,D} M \hat{IL}^2}{4\pi}\left(\frac{4}{3\pi}\sin^4\frac{\varphi}{2}\right) \\
P_{C\,D5,D6} &= \frac{V_{0,D} \hat{IL}}{\pi}\left(1 - \frac{M}{4}\left(2\sin\varphi - (2\varphi-\pi)\right)\cos\varphi\right) + \frac{r_{0,D} \hat{IL}^2}{4}\left(1 - \frac{4M}{3\pi}(1+\cos^2\varphi)\right)
\end{aligned}
\tag{3.48}
$$

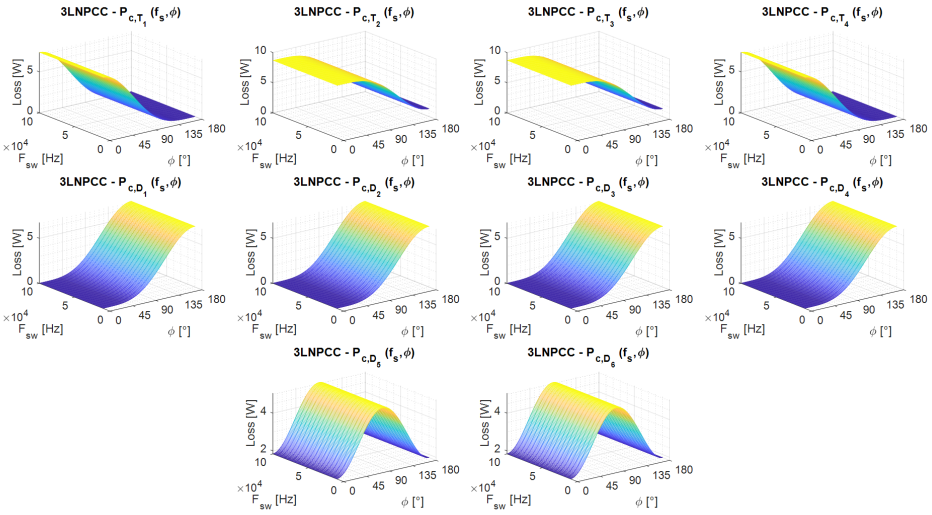


Figure 3.49: Conduction losses in 3LNPCC topology with varying φ and f_{SW}

[4] $V_{0,T}$: Value of initial transistor voltage drop and $r_{0,T}$: Value of transistor incremental resistance

[5] $V_{0,D}$: Value of initial diode voltage dropand $r_{0,D}$: Value of diode incremental resistance

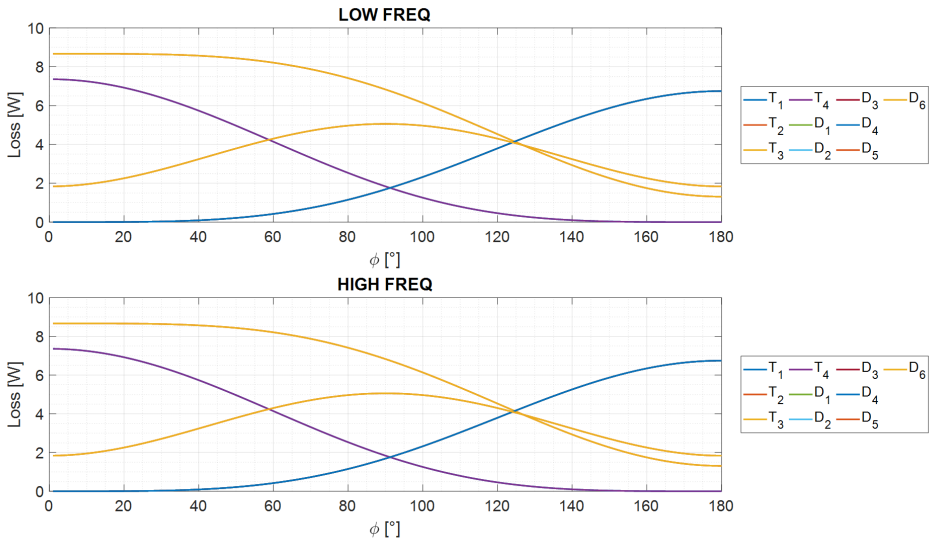


Figure 3.50: Conduction losses in 3LNPCC topology at $f_{SW} = 10\,\text{kHz}, 100\,\text{kHz}$ varying φ

Switching losses Interesting is the dependence of switching losses from φ unlike the topology2LC, eq. (3.49) (fig. 3.51) and in $f_{SW} = 10kHz - 100kHz$ (fig. 3.52), further observation concerns the diodes D_2 e D_3 which work only as rectifier diodes, with zero switching loss.

$$\begin{aligned}
P_{S\,T1,T4} &= f_s(E_{on} + E_{off})\frac{1}{2}\frac{Vdc}{Vref}\frac{\hat{IL}}{Iref}\left(\frac{1+cos(\varphi)}{2\pi}\right)\\
P_{S\,D1,D4} &= f_s E_{err}\frac{1}{2}\frac{Vdc}{Vref}\frac{\hat{IL}}{Iref}\left(\frac{1-cos(\varphi)}{2\pi}\right)\\
P_{S\,T2,T3} &= f_s(E_{on} + E_{off})\frac{1}{2}\frac{Vdc}{Vref}\frac{\hat{IL}}{Iref}\left(\frac{1-cos(\varphi)}{2\pi}\right)\\
P_{S\,D5,D6} &= f_s E_{err}\frac{1}{2}\frac{Vdc}{Vref}\frac{\hat{IL}}{Iref}\left(\frac{1+\cos\varphi}{2\pi}\right)\\
P_{S\,D2,D3} &= 0
\end{aligned} \tag{3.49}$$

In fig. 3.53 is shown the contributions of the switching and conduction losses for the individual devices in Rectifier mode and Inverter Mode, in which it is visible that for the element $T_i - D_i coni = 1 \cdot 4$ the weight of conduction and switching losses is strongly influenced by the φ angle.

In conclusion, in fig. 3.54 the total percentage losses of the individual devices of the 3LNPCC converter are shown and the relative switching and conduction losses expressed in $Watt$ (fig. 3.55) and globally in fig. 3.56.

In fig. 3.57 the global results of the converter are shown, distinguishing the total switching conduction losses and efficiency with variations of f_{sw} and φ while in fig. 3.58 the efficiencies of the converter in the two operating conditions are shown at varying

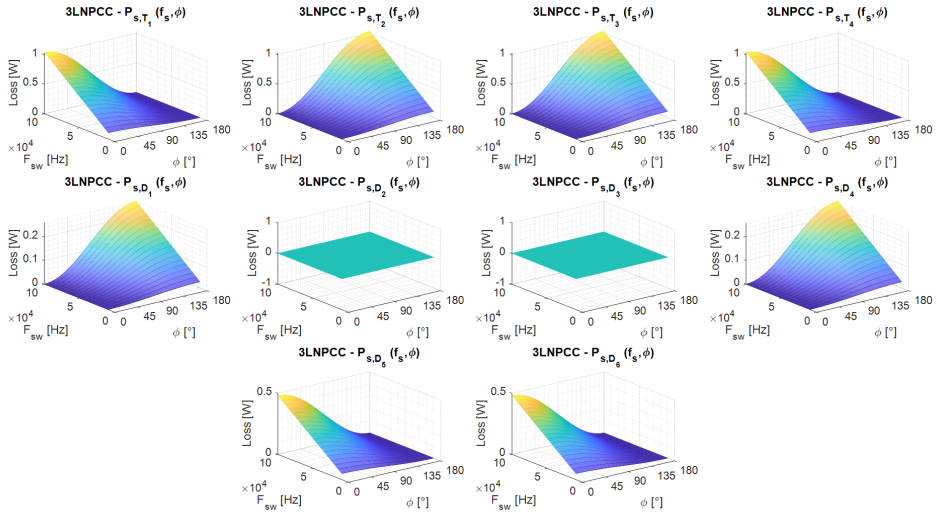


Figure 3.51: Conduction losses in 3LNPCC topology with varying φ and f_{SW}

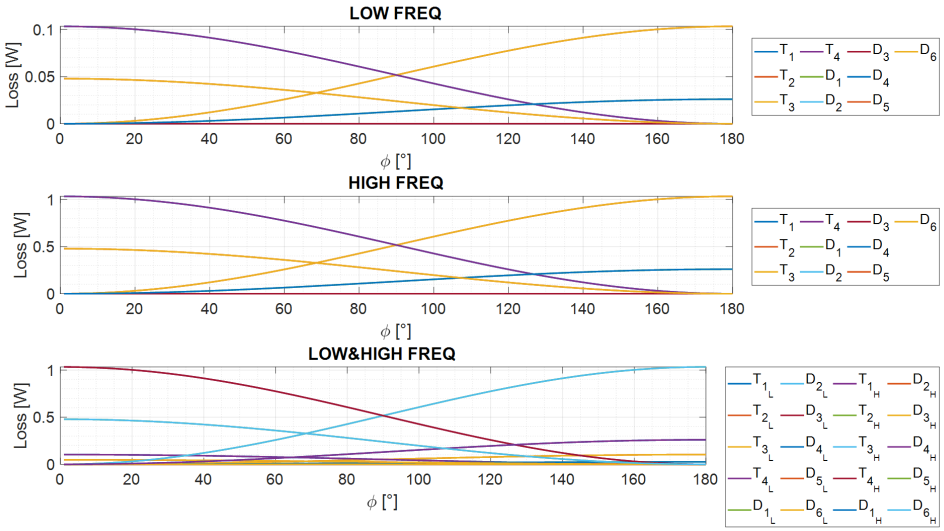
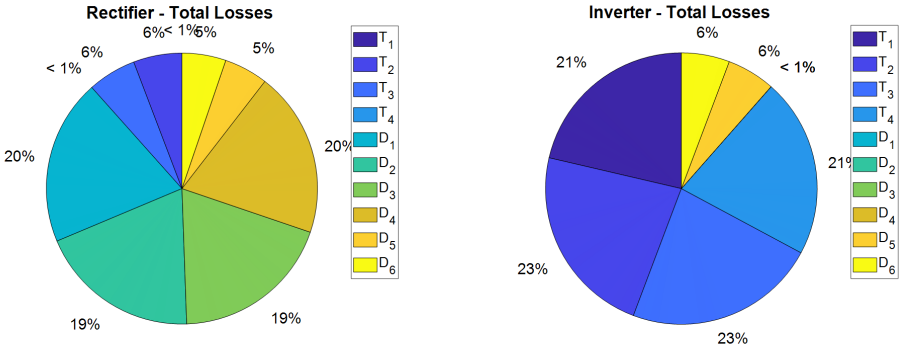
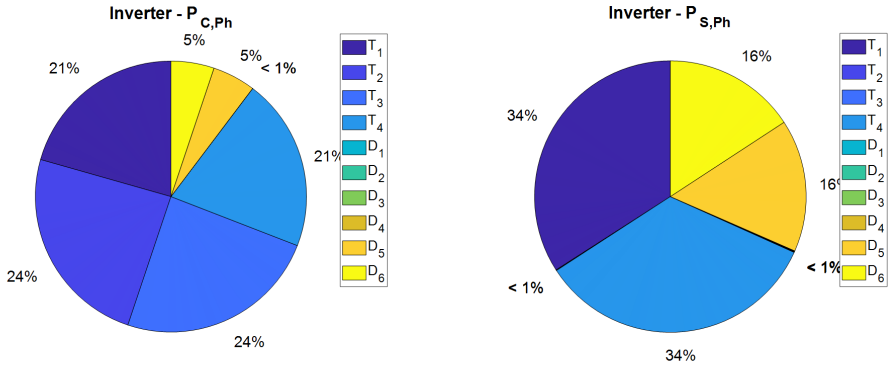


Figure 3.52: Switching losses in 3LNPCC topology with varying φ and f_{SW}

frequency.



(a) Rectifier



(b) Inverter

Figure 3.53: Switching and conduction losses percentages for each devices in 3LNPCC

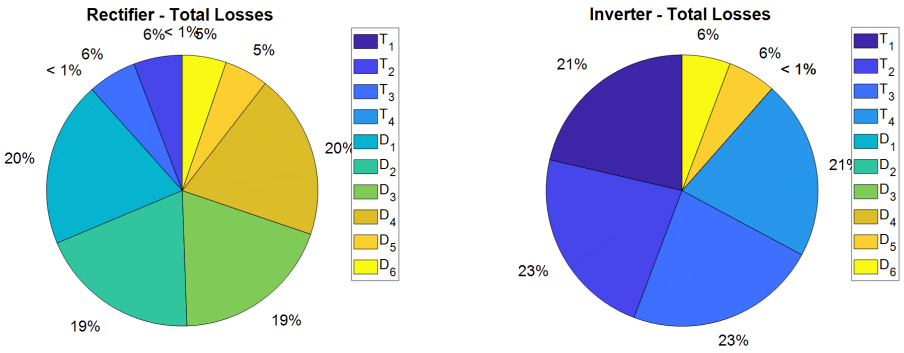


Figure 3.54: Total losses percentages for each devices in 3LNPCC

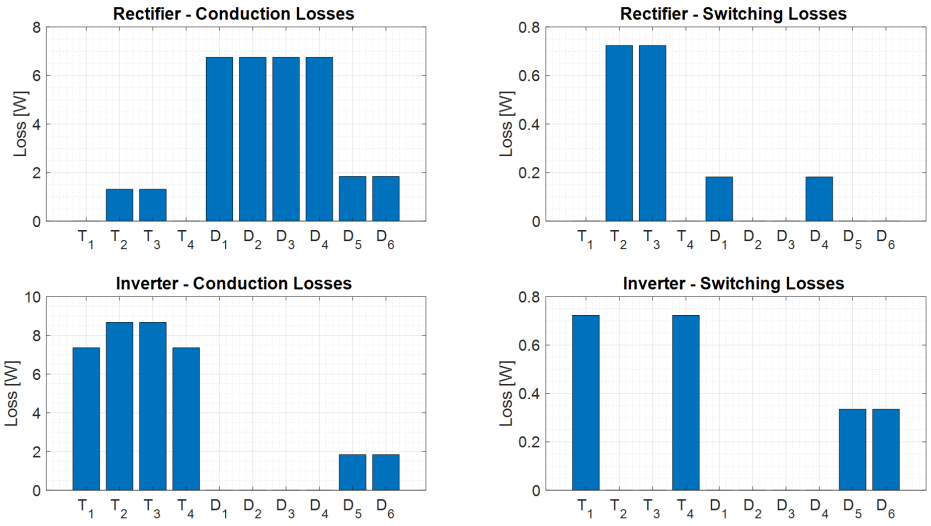


Figure 3.55: Contributions in conduction and switching losses of various devices in 3LNPCC

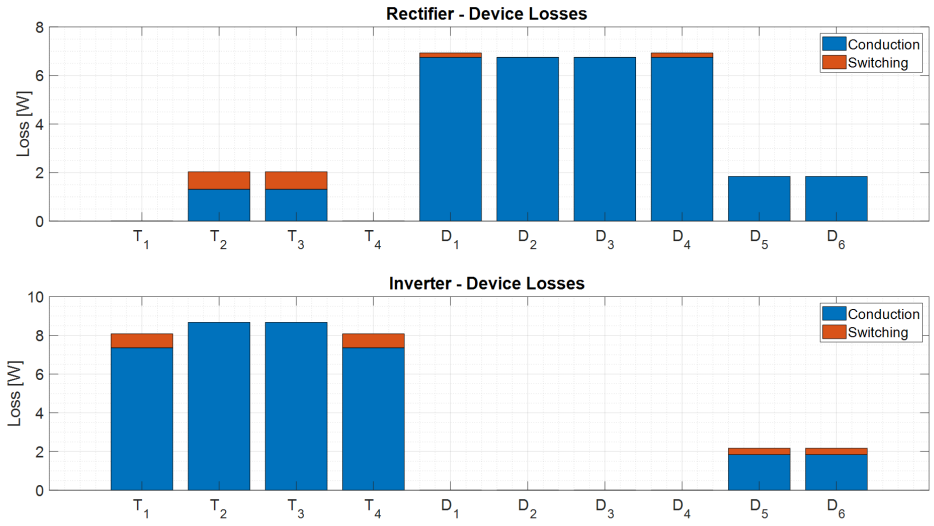


Figure 3.56: Contributions of the total losses of the various devices in 3LNPCC

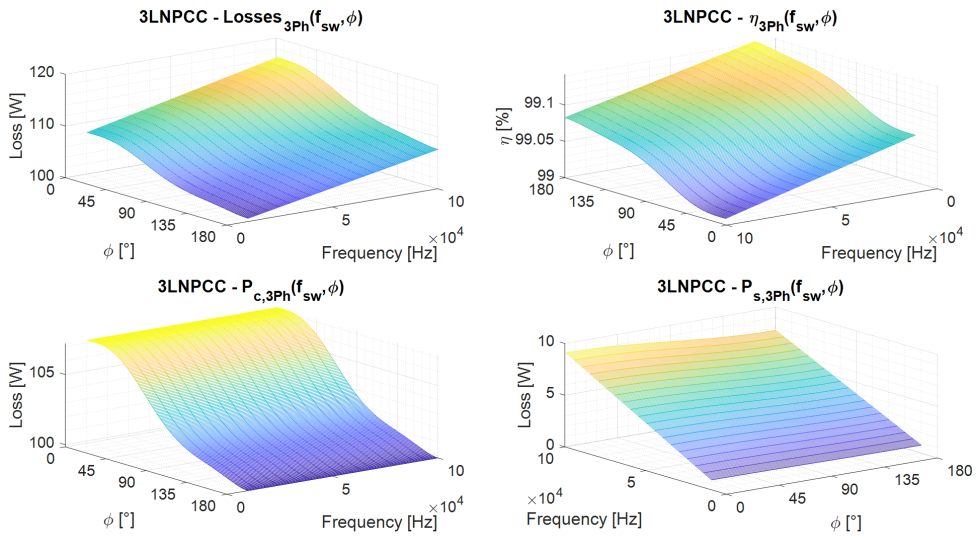


Figure 3.57: Switching losses, conduction, totals and efficiency of the 3LNPCC global converter varying f_{sw} and φ

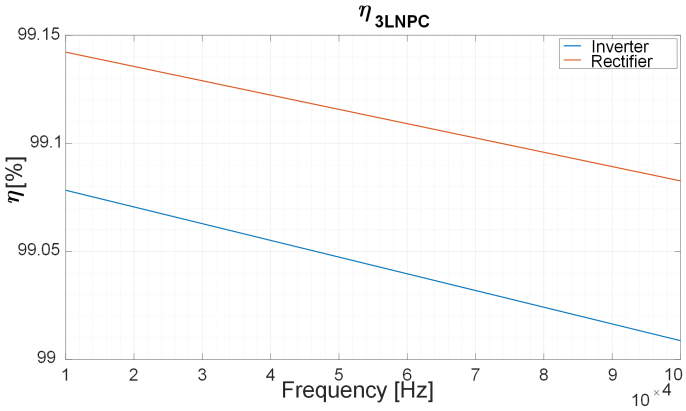


Figure 3.58: Efficiency of the 3LNPCC converter with varying f_{sw}, in $Rectifier\varphi = 180°$ and $Inverter\varphi = 0°$

Power Losses – 3TTC

CONDUCTION LOSSES – 3LTTC In case of the converter 3LTTC the conduction losses are the eq. (3.50), and also for this topology there is a direct dependence with φ (section 3.3.2), note that the contribution of T_2 and T_3 is equivalent in both operational cases ($Rectifier\varphi = 180°$ $Inverter\varphi = 0°$) since the horizontal leg works the same way.

In fig. 3.49 the results are shown and a focus in low frequency condition $f_{SW} = 10kHz$ and $f_{SW} = 100kHz$ in fig. 3.50.

$$
\begin{aligned}
P_{C\,T1,T4} &= \frac{V_{0,T} M \hat{IL}}{4\pi}\left(\sin\varphi + (\pi-\varphi)\cos\varphi\right) + \frac{r_{0,T} M \hat{IL}^2}{4\pi}\left(\frac{8}{3}\sin^4\frac{\varphi}{2}\right) \\
P_{C\,D1,D4} &= \frac{V_{0,T} M \hat{IL}}{4\pi}\left(\sin\varphi - \varphi\cos\varphi\right) + \frac{r_{0,T} M \hat{IL}^2}{2}\left(\frac{4}{3\pi}\sin^4\frac{\varphi}{2}\right) \\
P_{C\,T2,T3} &= \frac{V_{0,T} \hat{IL}}{4}\left(1 - \frac{M}{4}\left(2\sin\varphi - (2\varphi-\pi)\cos\varphi\right) + \frac{r_{0,T} \hat{IL}^2}{4}\left(1 - \frac{4M}{3\pi}(1+\cos^2\varphi)\right)\right. \\
P_{C\,D2,D3} &= \frac{V_{0,D} \hat{IL}}{4}\left(1 - \frac{M}{4}\left(2\sin\varphi - (2\varphi-\pi)\cos\varphi\right) + \frac{r_{0,D} \hat{IL}^2}{4}\left(1 - \frac{4M}{3\pi}(1+\cos^2\varphi)\right)\right.
\end{aligned}
\tag{3.50}
$$

[67]

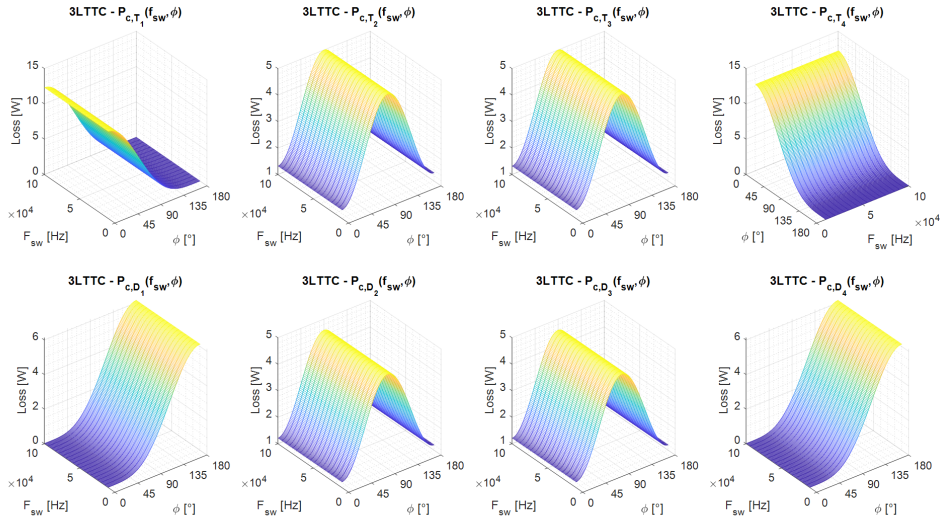


Figure 3.59: Conduction losses in 3LTTC topology with varying φ and f_{SW}

[6] $V_{0,T}$: Value of initial transistor voltage drop and $r_{0,T}$: Value of transistor incremental resistance

[7] $V_{0,D}$: Value of initial diode voltage dropand $r_{0,D}$: Value of diode incremental resistance

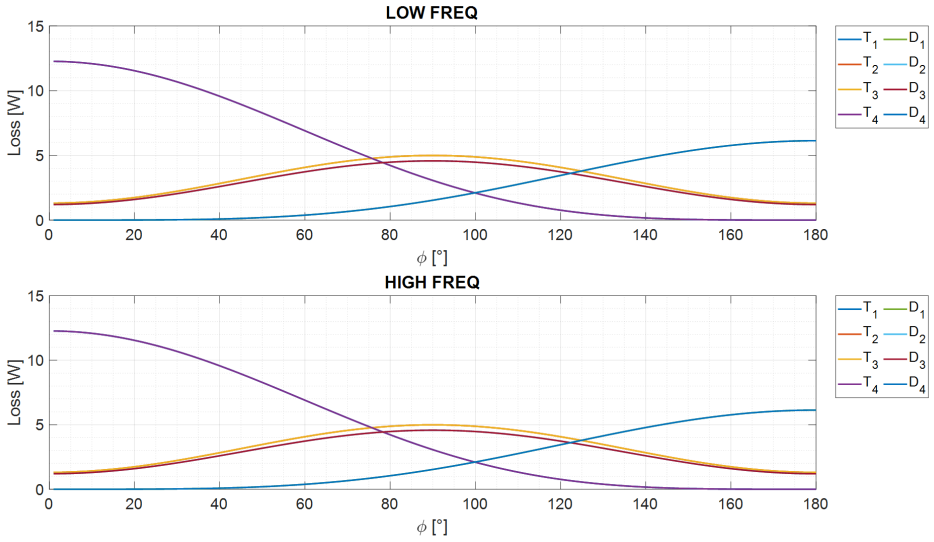


Figure 3.60: Conduction losses in 3LTTC topology at $f_{SW} = 10\,\text{kHz}, 100\,\text{kHz}$ varying φ

SWITCHING LOSSES – 3TTC Interesting is the dependence of switching losses from φ,(eq. (3.51) and fig. 3.61) and in $f_{SW} = 10kHz - 100kHz$ (fig. 3.62).

$$\begin{aligned}
P_{S\,T1,T4} &= f_s(E_{on} + E_{off})\frac{1}{2}\frac{Vdc}{Vref}\frac{\hat{IL}}{Iref}\left(\frac{1+\cos\varphi}{2\pi}\right)\\
P_{S\,D1,D4} &= f_s E_{err}\frac{1}{2}\frac{Vdc}{Vref}\frac{\hat{IL}}{Iref}\left(\frac{1-\cos\varphi}{2\pi}\right)\\
P_{S\,T2,T3} &= f_s(E_{on} + E_{off})\frac{1}{2}\frac{Vdc}{Vref}\frac{\hat{IL}}{Iref}\left(\frac{1-\cos\varphi}{2\pi}\right)\\
P_{S\,D2,D3} &= f_s E_{err}\frac{1}{2}\frac{Vdc}{Vref}\frac{\hat{IL}}{Iref}\left(\frac{1+\cos\varphi}{2\pi}\right)
\end{aligned} \tag{3.51}$$

As for the topology 2LC, the percentage contributions of swicthing and conduction losses for the single devices in $Rectifier\varphi = 180°$ $Inverter\varphi = 0°$, shown in fig. 3.63, are related to the condition of the converter.

In conclusion, in fig. 3.64 the total percentage losses of the individual devices of the converter 3LTTC are shown and in global form in fig. 3.66

In fig. 3.67 the global results of the converter are shown distinguishing the total switching conduction losses and efficiency with variations of f_{sw} and φ instead in fig. 3.68 are shown converter efficiencies in the two operating conditions with varying frequency.

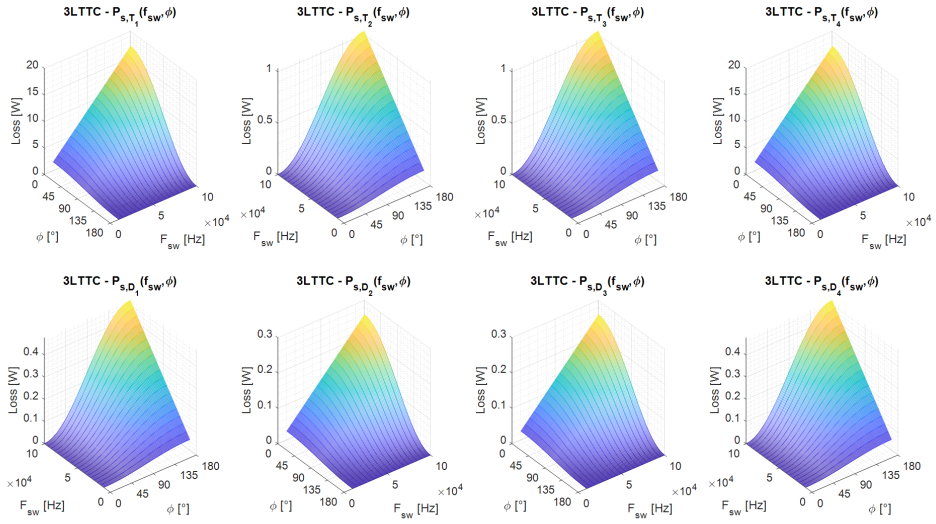


Figure 3.61: Switching losses in 3LTTC topology with varying φ and f_{SW}

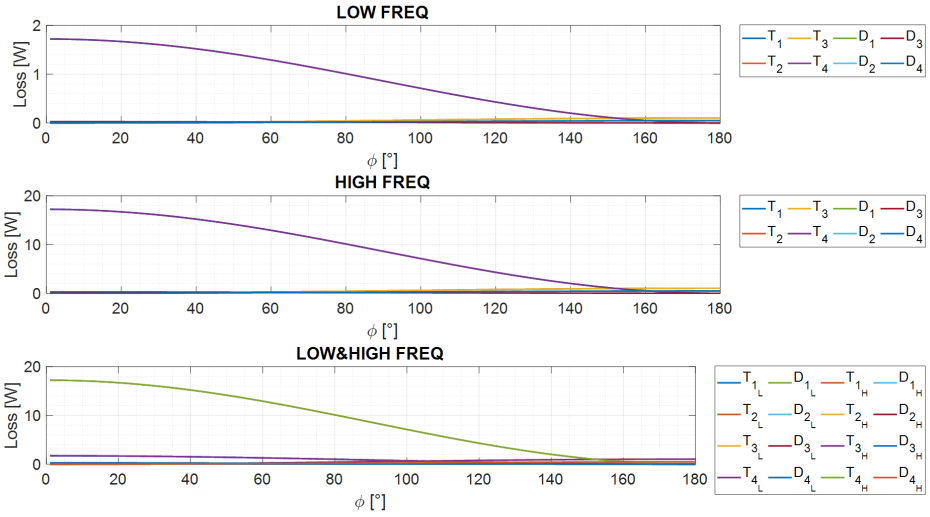
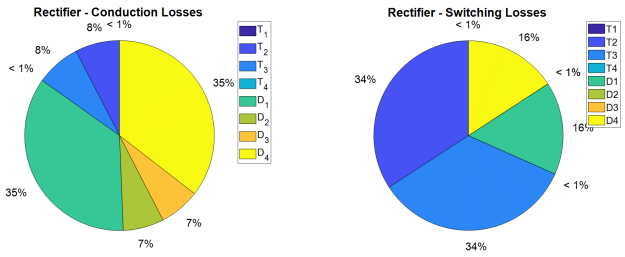
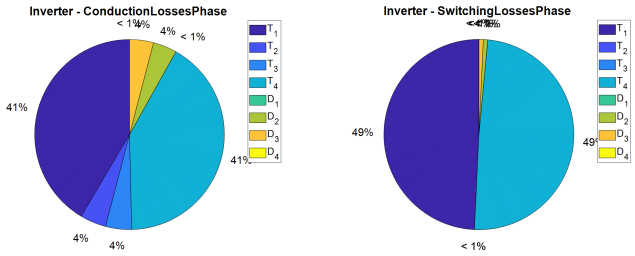


Figure 3.62: Switching losses in 3LTTC topology with varying φ



(a) Rectifier



(b) Inverter

Figure 3.63: Switching and conduction losses percentages for each devices in 2LC

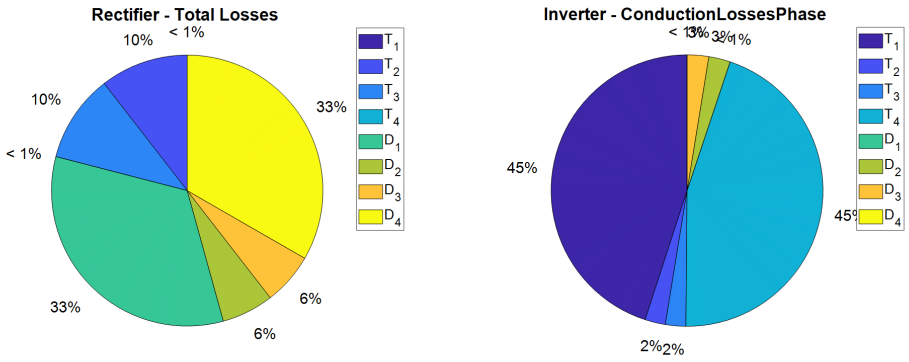


Figure 3.64: Total losses percentages for each devices in 3LTTC

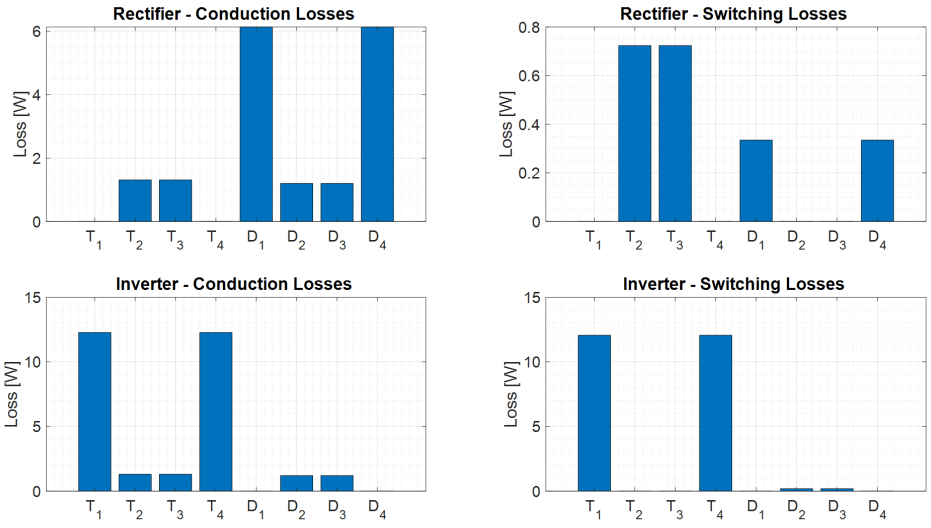


Figure 3.65: Contributions in conduction and switching losses of various devices in 3LTTC

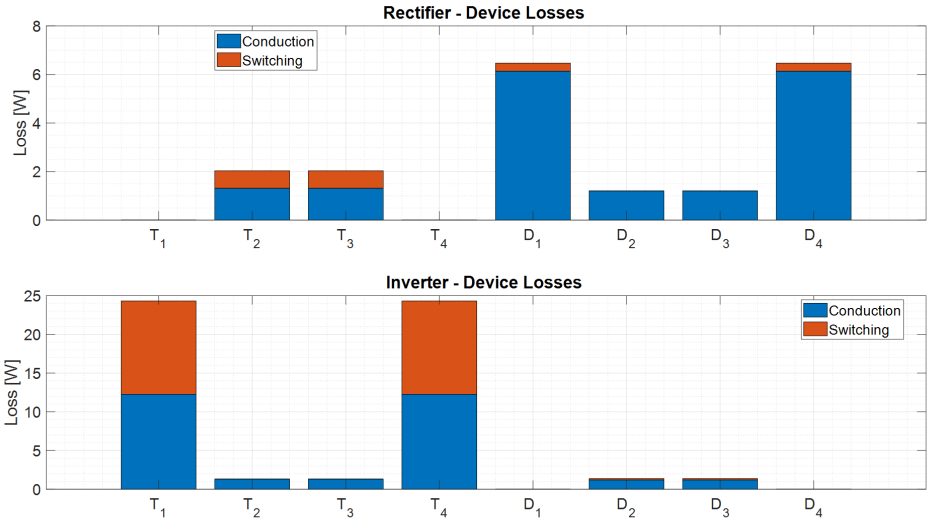


Figure 3.66: Total losses for each devices in 3LTTC

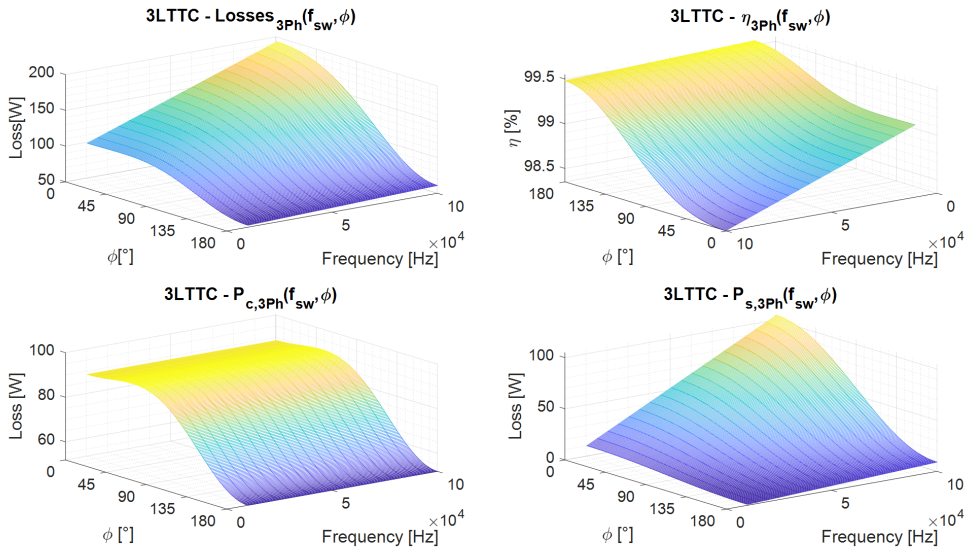


Figure 3.67: Switching losses, conduction, totals and efficiency of the 3LTTC global converter varying f_{sw} and φ

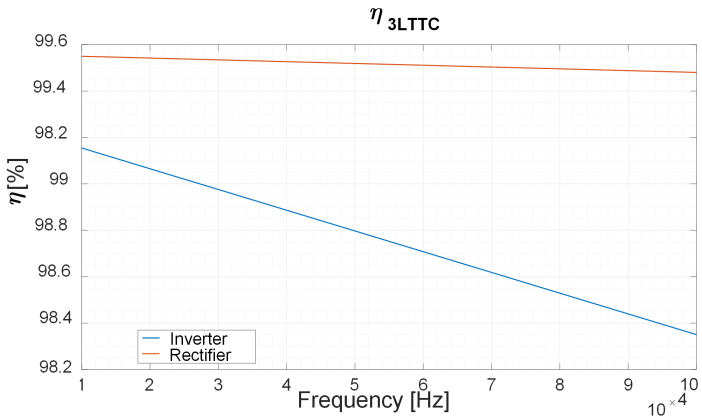


Figure 3.68: Efficiency of the 3LTTC converter with varying f_{sw}, in $Rectifier\varphi = 180°$ and $Inverter\varphi = 0°$

3.3.6 Comparison of converter efficiencies

In this paragraph, summarizing the data previously obtained, the three topologies are directly compared in terms of conduction and switching losses in the operating conditions and on the considered frequency range (fig. 3.69)

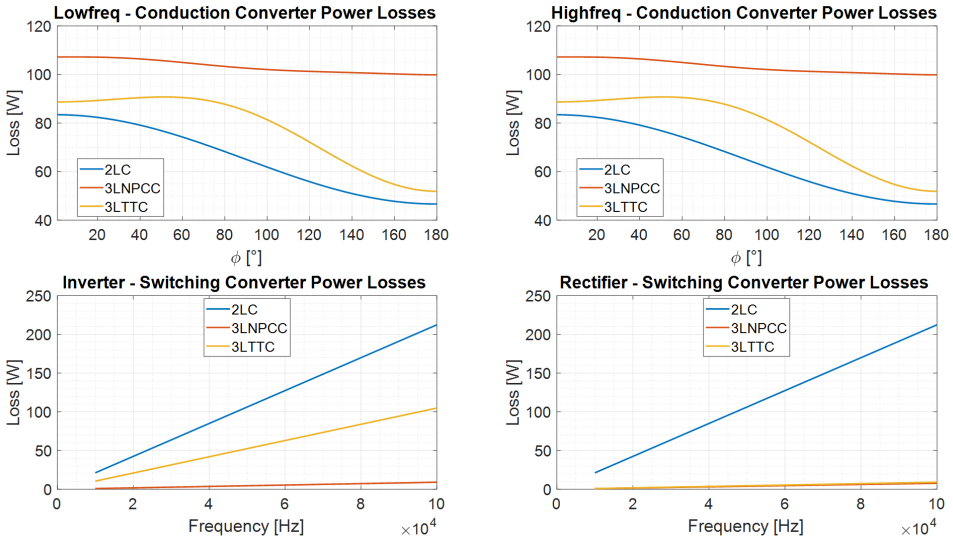


Figure 3.69: Direct comparison Topology losses

In figs. 3.70 and 3.71 is shown the comparison of 2LC,3LNPCC and 3LTTC in terms of efficiency in $Rectifier\varphi = 180°$ and $Inverter\varphi = 0°$ and at both value side of the frequency range and a global view in fig. 3.72

fig. 3.71 fig. 3.72

Ultimately, given that the goal is to obtain a converter with very low losses and high power density with high frequency, surely the topologies that obtain the highest performances are the 3LTTC and the 3LNPCC demonstrating in terms ofefficiency the advantage of a multi-level topology on SiC technology-based applications

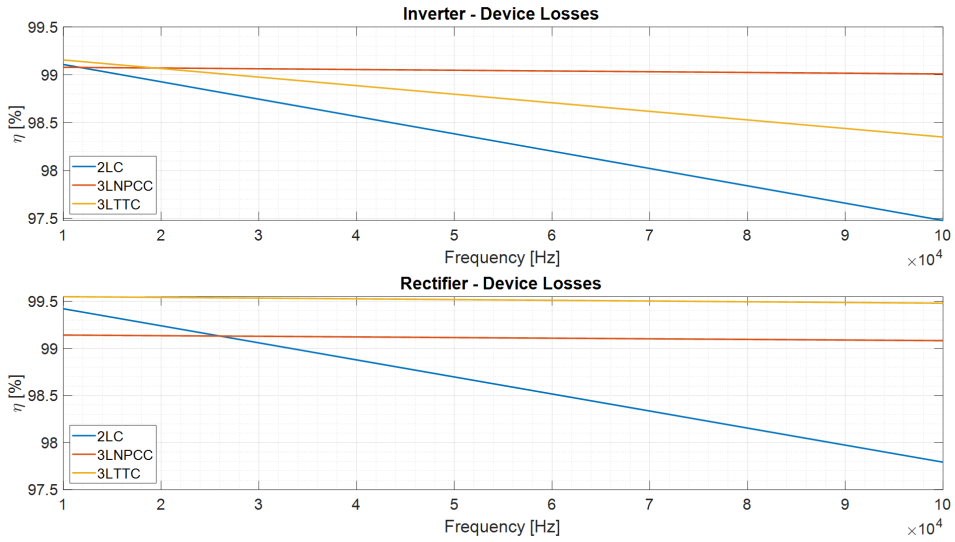


Figure 3.70: Direct comparison of topology efficiencies vs $f_s w$

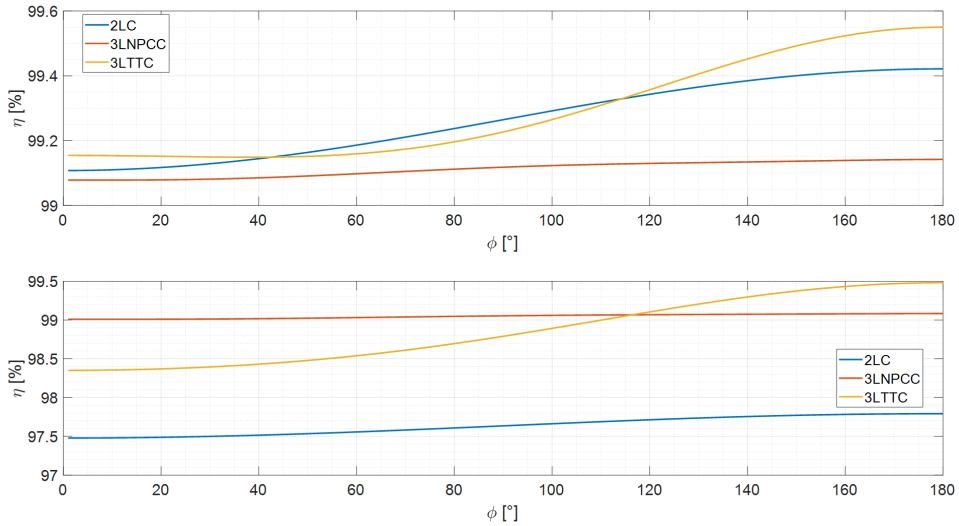


Figure 3.71: Direct comparison of topology efficiencies vs φ

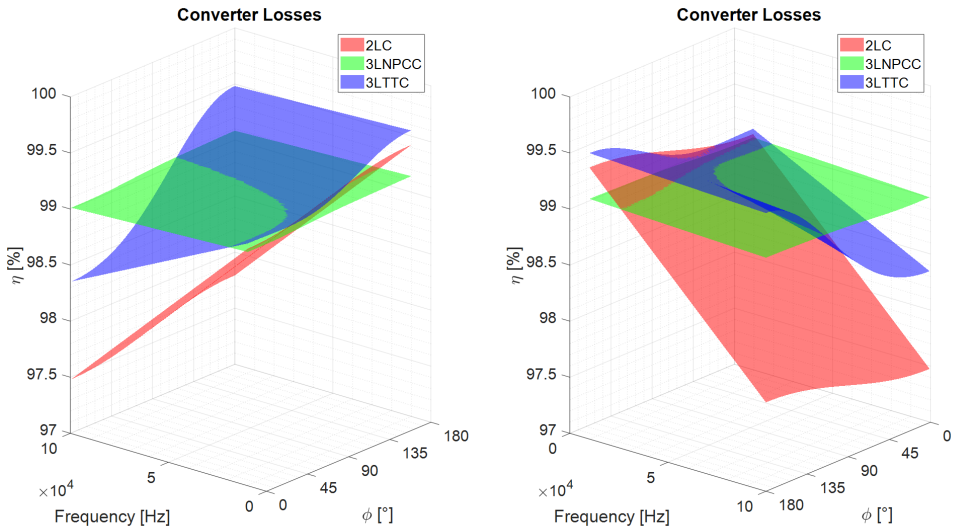


Figure 3.72: Direct topologies efficiency comparison

3.4 Modeling and Control of Converter

Taking into consideration a generic bidirectional converter of fig. 3.73. The relationships of the electrical quantities in play are eq. (3.52) and assuming that the system is balanced according to eq. (3.53), by applying the transformation matrices (appendix A) we obtain the equivalent relationships in the system in stationary quadrature and in the rotary system to the fundamental pulsation (eq. (3.54)) and (eq. (3.55)).

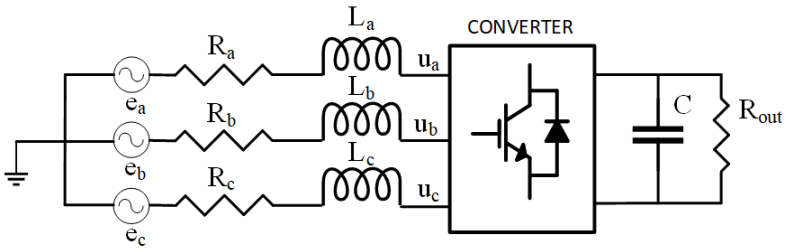


Figure 3.73: Voltage-Sourced Converter (VSC) principle scheme

$$\begin{cases} L\dfrac{di_a}{dt} + Ri_a = u_a - e_a \\ L\dfrac{di_b}{dt} + Ri_b = u_b - e_b \\ L\dfrac{di_c}{dt} + Ri_c = u_c - e_c \end{cases} \tag{3.52}$$

$$\begin{cases} e_a + e_b + e_c = 0 \\ i_a + i_b + i_c = 0 \end{cases} \tag{3.53}$$

$$\begin{cases} L\dfrac{di_\alpha}{dt} + Ri_\alpha = u_\alpha - e_\alpha \\ L\dfrac{di_\beta}{dt} + Ri_\beta = u_\beta - e_\beta \end{cases} \tag{3.54}$$

$$\begin{cases} L\dfrac{di_d}{dt} + Ri_d - \omega Li_q = u_d - e_d \\ L\dfrac{di_q}{dt} + Ri_q + \omega Li_d = u_q - e_q \end{cases} \tag{3.55}$$

Since the converter command variables are the voltages to the leg nodes referred to ground, the relations are rewritten to highlight these voltages (eq. (3.56)).

$$\begin{cases} u_d = L\dfrac{di_d}{dt} + Ri_d - \omega L i_q + e_d \\ \\ u_q = L\dfrac{di_q}{dt} + Ri_q + \omega L i_d + e_q \end{cases} \tag{3.56}$$

In the command relations it is possible to notice that there is a mutual interaction between the variables of the two axes and that therefore an independent control is not possible

What is shown is that by acting and controlling the inductance voltage drops (eq. (3.57)) it is possible to decouple the relations of the two axes by controlling them independently (eq. (3.58)),then replacing the eq. (3.58) to the eq. (3.55) we get the eq. (3.59) and rewriting we get the eq. (3.60), with a schematic representation like the fig. 3.74.

$$\begin{cases} L\dfrac{di_d}{dt} + Ri_d = \left(k_p + \dfrac{k_i}{s}\right)(i_d^* - i_d) \\ \\ L\dfrac{di_q}{dt} + Ri_q = \left(k_p + \dfrac{k_i}{s}\right)\left(i_q^* - i_q\right) \end{cases} \tag{3.57}$$

$$\begin{cases} u_d = \left(k_p + \dfrac{k_i}{s}\right)(i_d^* - i_d) - \omega L i_q + e_d \\ \\ u_q = \left(k_p + \dfrac{k_i}{s}\right)\left(i_q^* - i_q\right) + \omega L i_q + e_q \end{cases} \tag{3.58}$$

$$\begin{cases} L\dfrac{di_d}{dt} + Ri_d - \omega L i_q = \left(k_p + \dfrac{k_i}{s}\right)(i_d^* - i_d) - \omega L i_q \\ \\ L\dfrac{di_q}{dt} + Ri_q + \omega L i_q = \left(k_p + \dfrac{k_i}{s}\right)\left(i_q^* - i_q\right) + \omega L i_q \end{cases} \tag{3.59}$$

$$\begin{cases} L\dfrac{di_d}{dt} = 1/L\left(k_p + \dfrac{k_i}{s}\right) i_d^* - 1/L\left(R + \left(k_p + \dfrac{k_i}{s}\right)\right) i_d \\ \\ L\dfrac{di_q}{dt} = 1/L\left(k_p + \dfrac{k_i}{s}\right) i_q^* - 1/L\left(R + \left(k_p + \dfrac{k_i}{s}\right)\right) i_q \end{cases} \tag{3.60}$$

Once the heart of the vector control has been described, in fig. 3.75 is shown the overall block diagram of the Voltage Oriented Control (VOC) in which the two control rings, the transformation blocks, the phase generator PLL and the modulator are visible.

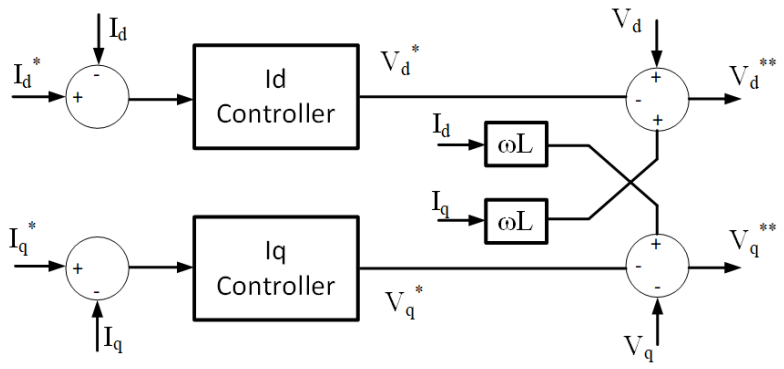


Figure 3.74: Decoupling Current Control scheme

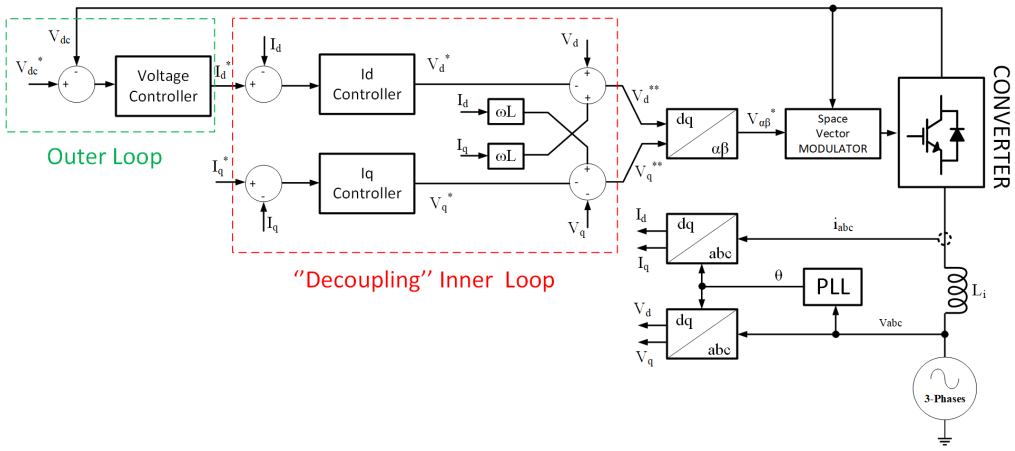


Figure 3.75: Block diagram of VOC

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Chapter 4

Design issue in WBG converter

As discussed in sections 2.2 and 2.3.1 the nominal operating temperatures of SiC devices, higher than those of the devices in Si and likewise the highest switching frequencies of SiC-based applications, they involve important problems concerning the thermal and electromagnetic interaction with what surrounds them.

Thermal problems, for example, may concern materials suitable for electrical insulation and thermal dissipation such as thermal pads. Electromagnetic problems arise from the higher dv/dt and di/dt that make the knowledge and modeling of all those parasitic phenomena such as capacitance and inductance present in the PCBs of electronic power converters of fundamental importance.

4.1 Thermal in WBG converter

The thermal resistance (Rth(junction-ambient)) of a system is made up from a number of component parts as shown in Fig.4.1.

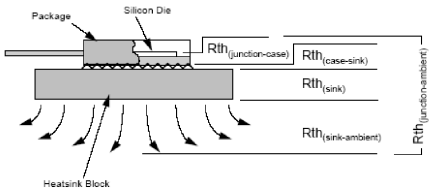


Figure 4.1: Build-up of Thermal Resistance in a System

The designer of a system has varying amounts of influence over the component parts of the overall thermal resistance of his design:

- Thermal Resistance (Rth)(junction-case) - this has been determined during the design and manufacture of the product. The system designer has no direct influence.
- Rth(case-sink) (or Contact Thermal Resistance) - determined by the size and quality of the contact areas between the package and the sink, the use of intermediate

materials and the contact pressure. Hence, the system designer can have a large influence over this parameter.

- Rth(sink) and Rth(sink-ambient) - determined by heatsink design, i.e. material and shape. System designer will choose optimum sink matching both performance and cost requirements.

Thermal resistances for packages and heatsinks can be determined from datasheets and although the contact thermal resistances can also be taken from manufacturer's data, this figure is generally typical and for a single set of specified conditions. Hence, it is possible for a designer to gain better or worse contact thermal resistances depending on parameters that he prescribes.

There are a number of factors that affect the contact thermal resistance, one of the factors being the contact force with which the package is pushed against the heatsink.

Package cases and heatsink surfaces can never be perfectly flat. Hence contact between the two will only occur at several points allowing an air gap between the surfaces (Fig.4.2). Since air is a very good thermal insulator this means that the contact thermal resistance is much greater than it would be if the two surfaces were in perfect contact (no air gap). However, as the contact force (pushing the two surfaces together) increases then so will the number of points at which the two surfaces contact one another and the air-gap will be reduced, in turn reducing the contact thermal resistance.

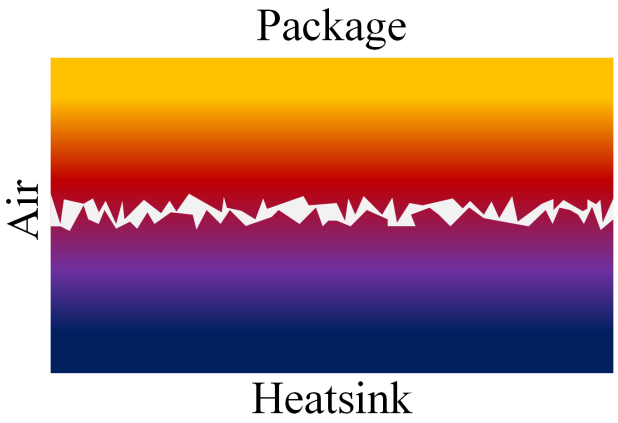


Figure 4.2: Diagram Showing the Effect when two non perfect surfaces meet

As the contact force is increased, the contact thermal resistance decreases. However, this does not follow a linear relationship and shows diminishing returns in thermal resistance reduction for increases in the contact force (Fig.4.3). A rapid initial fall-off in contact thermal resistance is replaced by a more gradual reduction with increased contact force. The minimum contact force should therefore be no lower than the point at which these rapid reductions in thermal resistance end this occurs at approximately 20N.

The minimum contact force of 20 N mentioned in previous is purely that, the minimum force. Any force applied above that figure will still show gains in reduced contact thermal

resistance until the maximum force that the package can withstand before the device characteristics are altered or the package is destroyed. This maximum limit figure has been measured to be 200N. However, these gains are not free, for in general terms a greater contact force means a larger, more expensive clamping system. A contact force should therefore be chosen that optimises both the thermal and the cost requirements of the system.

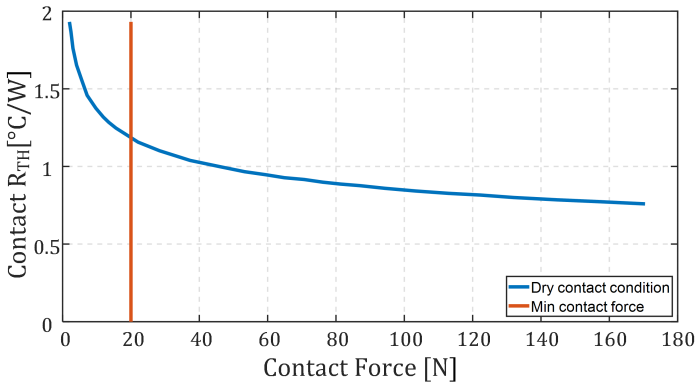


Figure 4.3: Minimum Contact Force

Contact As mentioned previously, the contact conditions between the package and the heatsink will affect the contact thermal resistance. Contact conditions encompass a number of areas including: surface roughness, surface cleanliness, paint finishes and intermediate materials. The surface roughness of the heatsinking material should be no greater than 0.02mm over the area where the device is to be mounted. Surface cleanliness during assembly of package and heatsink is imperative, even if a thermal grease or other material is subsequently added. Unclean surfaces can be held apart by dirt or grease thus increasing the thermal resistance. However, normal paint finishes (up to 50 µm thick) have been shown to have little effect on thermal resistance, this therefore leaves intermediate materials as an area for discussion.

Intermediate Materials Contact between two non-perfect surfaces will result in an air gap between them. The most common method of overcoming this is to use a thermally conductive heatsinking compound to fill the gaps between the surfaces and hence lower the contact thermal resistance. This compound also has the advantage that it prevents moisture from penetrating between the surfaces. Thinly applied, these compounds are advantageous as they fill the air gaps and do not further increase the distances between the surfaces. Thickly applied they can hold the two surfaces apart and increase the contact thermal resistance. The following graph displayed in Fig.4.4 shows the contact thermal resistance for 'dry' conditions (no compound) and the thermal resistance using compound, both are plotted against contact force. The metal heatspreader on the back of the most common package is non-electrically isolated from the pinouts of the device within, i.e. in

the case of a MOSFET the heatspreader is the drain contact, for an IGBT the collector. Hence in cases where devices are not electrically paralleled but share the same heatsink, it is necessary to insert an electrically isolating material between the package and the heatsink block.

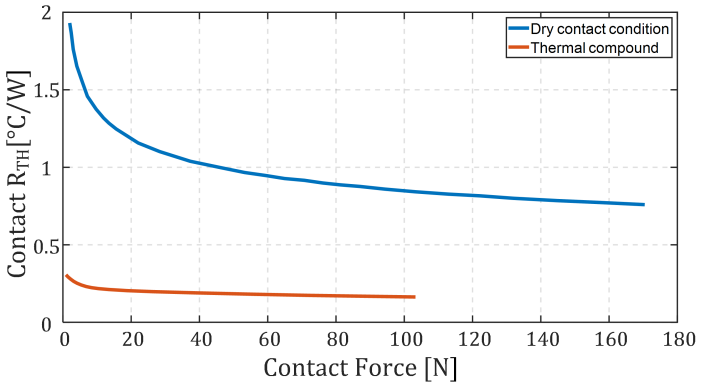


Figure 4.4: Contact Thermal Resistance for Dry and Compound conditions, plotted against contact force

At the minimum stated contact force of 20 N the following contact resistances can be achieved (Tab.4.1):

Contact Conditions	**Rth(c-s) @ 20N Contact Force**
'Dry' (no compound)	1.2°C/W
Thermal Compound	0.2°C/W

Table 4.1: Contact Condition

The pad obviously has a direct and detrimental effect on the contact resistance as insertion adds an extra resistance into the build-up. Again, the contact thermal resistance is dependant on contact pressure. The following graph, shown in Figure 1.5, illustrates the higher thermal resistance when using an isolator pad, adding a new line to the thermal resistance curve. The isolator used to plot the line was a typical silicone loaded pad. Therefore, it should be noted that when electrically isolating a device from a heatsink the thermal resistance of the system will increase.

- Mica insulators have been in use for over 35 years and are still commonly used as an insulator. Mica is inexpensive and has excellent dielectric strength, but it is brittle and is easily cracked or broken. Because mica used by itself has high thermal impedance, thermal grease is commonly applied to it.
- The thermal grease flows easily and excludes air from the interface to reduce the interfacial thermal resistance. If the mica is also thin [50 µm – 80 µm], a low thermal impedance can be achieved. However, thermal grease introduces a number of

problems to the assembly process. It is time-consuming to apply, messy and difficult to clean. Once thermal grease has been applied to an electronic assembly, solder processes must be avoided to prevent contamination of the solder. Cleaning baths must also be avoided to prevent wash-out of the interface grease, causing a dry joint and contamination of the bath. Assembly, soldering and cleaning processes must be performed in one process while the greased insulators are installed off-line in a secondary process. If the grease is silicone-based, migration of silicone molecules occurs over time, drying out the grease and contaminating the assembly.

- Polyimide films can be used as insulators and are often combined with wax or grease to achieve a low thermal impedance. These polyimide films are especially tough and have high dielectric strength.
- Silicone pad are thermally conductive insulators designed to be clean, grease-free and flexible. The combination of a tough carrier material such as fiberglass and silicone rubber which is conformable provides the engineer with a more versatile material than mica or ceramics and grease. This material minimize the thermal resistance from the case of a power semiconductor to the heat sink. They are materials electrically isolate the semiconductor from the heat sink and have sufficient dielectric strength to withstand high voltage.

Thermal Conductivity The time rate of heat flow through a unit area producing a unit temperature difference across a unit thickness eq. (4.1). Thermal conductivity is an inherent or absolute property of the material.

$$k = \frac{dq}{dt}\frac{z}{A\Delta T} \tag{4.1}$$

Thermal Impedance A property of a particular assembly measured by the ratio of the temperature difference between two surfaces to the steady-state heat flow through them.(eq. (4.2))

$$Z_\theta = \frac{z}{kA} + R_i \tag{4.2}$$

In fig. 4.5 is shown a thermal data obtained with thermal camera of the converter study in in section 7.1.

4.2 Parasitic effects issue in WBG converter

With the introduction Wide Band Gap (WBG) devices into the market, the new goal is to obtain new designs of converter that exploit those highspeed power switches.The market wants to have more efficient and compact systems, which translates to better and cheaper systems, this driving many companies and designers to prototype systems with these switches. These newer designs are not without their challenges, and designers are beginning to realize that traditional design methodologies need to be augmented.

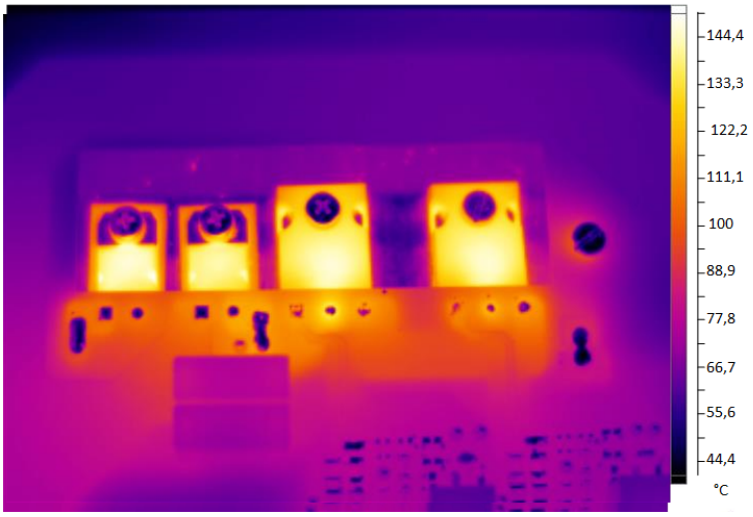


Figure 4.5: Thermal image of the phase switching cell

This chapter illustrates these challenges and uses a design methodology that can help ensure success with fewer design spins. To meet the demand for higher power densities, power electronics engineers must be able to shrink the physical size of their products and remove the heat to maintain reliability. To help reduce the size, designers can raise the switching frequency of converters, which allows a decrease in the size of the energy storage components, so the WBG it's a good choice because allows higher frequency operation with relatively low losses in the switches. However, increasing the switching frequency and decreasing the switching time requires careful considerations for layout and design since the change in voltage versus a given change in time (dv/dt) and a change in current versus a given change in time (di/dt) are very high.

The main design rules in high frequency converter are:

- Minimize capacitances to ground or other nodes at high dv/dt nodes
- Reduce parasitic impedances in high (di/dt) branches
- Guard or shield high-impedance signal nodes, such as the gate of a drive transistor with appropriate guard rings and shields.

In the frequency domain, a fast switch under hard switched condition produces harmonics well into the hundreds of MHz. Within the power converter, harmonic energy produced must be converted to power in the load to maintain efficiency. This means parasitic effects that absorb energy or prevent it from being converted into load power must be reduced.[58]

1. **Skin Effect** The skin effect confines current near the surface of the conductor and increases the effective resistance of the conductor and at high frequencies, this effect

becomes more dominant. Thick conductor traces and solid vias have diminishing performance returns in physical designs as the frequency increases because of the skin effect.

2. **High di/dt Through Printed Circuit Board (PCB) Traces** High di/dt generates resistive and inductive spikes across components and layout parasitics to produce voltage spikes, noise, and ElectroMagnetic Interference (EMI) and this means that all traces have undesirable parasitic inductance. Decreasing trace length is an effective way to lower inductance and resistance. Generally, the capacities term is small and is neglected because the trace width is small. Increasing the trace width, providing a ground plane a small distance under the trace, and employing coplanar traces are all effective means to help increase capacitance and lower the effective inductance.

3. **Relative Ground** In a switching converter, all points on a trace or ground plane have unique voltages relative to any other point on the trace. In a high-speed power circuit, ground is a relative term, since each location on a trace will have a slightly different voltage. The effects of these ground voltage mismatches cause a decrease in noise immunity. The layout parasitic of the PCB traces need to be included in the simulation to see this effect. It is difficult to estimate the values of the parasitic inductance. Therefore, for proper analysis, we should include the parasitic impedance of the layout in the simulation by using an ElectroMagnetic (EM) model extracted using a field solver.

4.2.1 Analysis of PCB parasitic effects in a Vienna Rectifier for an EV battery charger by means of Electromagnetic Simulations

The aim of this work is to investigate the impact of the PCB electrical parasitic parameters on the performances of a Silicon Carbide (SiC) three-level T-type rectifier used for electric vehicle battery chargers. The short switching times of the SiC devices enables high switching frequency at very high efficiency. On the other hand, as the time derivative of the current increases (as a rule of thumb we can set 1A/ns as a breaking point), PCB parasitics start to play a significant role and may cause the degradation of the performances or even a design failure if not taken into account from the first design stage. Industry standard Electronic Design Automation (EDA) tools can be used to extract a model for the PCB to evaluate all the unwanted effects introduced by the physical realization of the board layout. For the scope of the current study, the software Advanced Design System (ADS)[1] has been used to extract an S-parameter based model of the PCB and co-simulate it with the circuit components. Results obtained with and without the PCB model are finally compared for two different design iterations.

[1] ADS - electronic design automation software system produced by Keysight EEsof EDA, a division of Keysight Technologies

This work deals with the analysis of the power conversion stage, realized by a Vienna Rectifier (VR) [46], whose circuital scheme is shown in Fig.4.6. Being a multilevel topology, the VR has the advantage of reducing the electrical stresses on the power devices with lower voltage variation 3.1. With this topology, the current is drawn from the main at unity power factor, thus minimizing the line distortion and maximizing the real power available from the utility outlet[59]. The four operation states of the converter are displayed Fig.4.7, selected on the basis of the grid phase current $i_{L_j}(with j = a, b, c)$ polarity, and the status of the bidirectional switches Q_j.

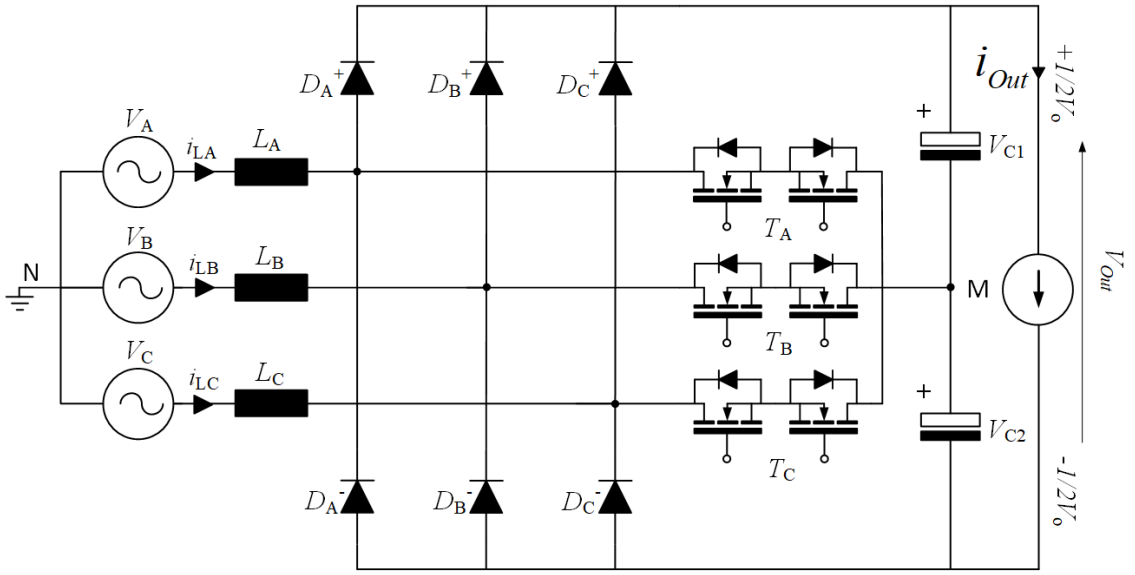


Figure 4.6: Circuital scheme of the 3-Phase/3-Level Vienna Rectifier

In this study the VR has been equipped with SiC devices that are capable of higher blocking voltages, higher switching frequencies and higher junction temperatures than standard silicon devices. Thanks to the achievable high switching frequencies ($fs = 70kHz \div 200kHz$), a considerable reduction of the size and cost of passive components can be accomplished [60], [45]. Both factors and the use of very fast switching power devices, e.g.SiC MOSFETs and diodes, have the unwanted side effect of accentuating the influence of parasitics on the correct operation of the system. As a matter of fact, the detrimental effect of the electrical parasitic parameters due to the not-ideal physical behavior of the PCB would, if not properly managed, significantly impact the operation of the power converter eventually leading to malfunction or catastrophic failure. Consequently, without the mitigation described here, the reliability would be also reduced. To avoid multiple design iterations, consisting in the costly realization of different version of updated prototypes, suitable preliminary simulations of the prototype can be performed at the design stage, aimed to handle the high frequency issues previously described in the paper. Ideally, the approach described here can be adopted from the very beginning of the design phase. However, for the current study, the EM co-simulation approach, that will be better described in the next paragraphs, has been adopted only after the fabrication of the first prototype.

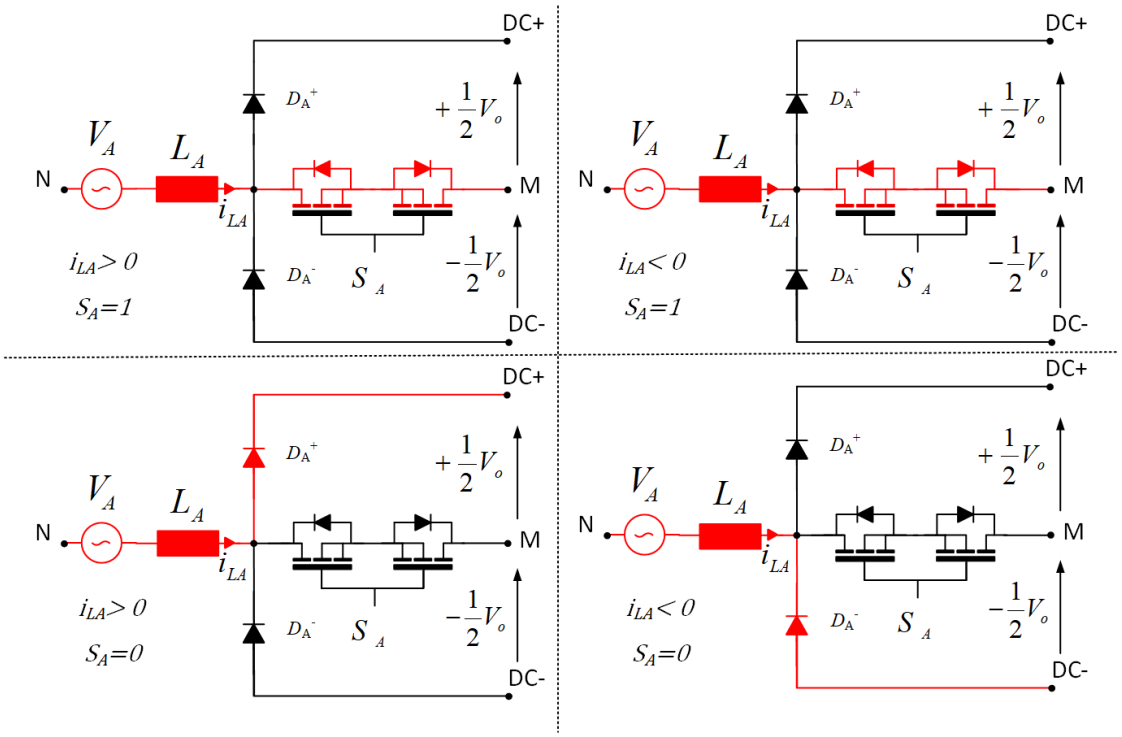


Figure 4.7: modes of operation of the generic phase

Main technical performances are listed in Tab.4.2. The driving circuit of the SiC MOSFETs consists of 3 (Rev. A board) and 6 (Rev. B board) galvanically isolated single gate drivers. To obtain a constant output voltage as well as Power Factor Controller (PFC) behavior a mixed signal control board unit is used. It implements average current Continuous Conduction Mode (CCM) algorithm, by means of the State Machine Event Driven (SMED) peripherals of the STNRG388A "STMicroelectronics" mixed mode controller by to obtain the control signals for the SiC MOSFETs. Main components are listed in Tab.4.3.

Parameter	**Value**
$V_{AC_{LL}}$	400 V
f_{AC}	50 Hz
V_{OUT}	800 V
P_{OUT}	11 kW
f_s	70 kHz
$Efficiency$	>98%
PF	>0.99
PF	<5%

Table 4.2: Design Specification

Component	Part Number
SiC High Power Schottky Diode	ST STPSC20H12
SiC Power MOSFET	ST SCTH35N65G2V
Galvanically Isolated Single Gate Driver	ST STGAP2S
Mixed Signal Controller	ST STNRG388A
475 µH Inductor	WURTH 750317156
470 uF High Voltage Capacitor	VISHAY MAL215759471E3

Table 4.3: Main parts of the converter

Proposed Design Methodology The proposed design methodology is based on the EM simulation of the PCB layout and the co-simulation of such EM extracted model with the circuit components [58]. The flow is based on the Keysight software ADS, which integrates in the same design environment EM solvers and circuit simulators, enabling a very effective design flow. The EM solver used for this work is Momentum RF®, that adopts a quasi-static formulation of the Method of Moments[2] [61]. This method is suitable to solve Maxwell's electromagnetic equations for planar structures embedded in a multilayered dielectric substrate. Thanks to the use of the pre-computed Green's functions, the Method of Moments is more efficient in terms of computational resources and number of unknowns, compared to other numerical methods that can be adopted to solve the electromagnetic problem, like Finite Element Method (FEM)[2] and Finite Difference Time Domain (FDTD)[2]. The output of the analysis is an S-parameter model for the PCB. S-parameters are combined with the electrical model of the circuit components (EM co-simulation) so that the overall electrical response of the circuit can be evaluated. Depending on the actual physical realization of the PCB, on the frequency of operation and on the signals applied to the circuit, several different phenomena can take place.

Main effects are:

- Voltage spikes observed on the control voltages at the transition between the OFF and ON state of the switches.
- Capacitive coupling and proximity effects between close traces
- Skin effect present in conductive traces and via holes
- Voltage drop across the ground plane, leading to ground bounce phenomena and increased noise level.

Due to the distributed nature of the S-parameter model, an EM co-simulation approach inherently accounts for all possible parasitic effects so that the prediction of the real circuit

[2]Wikipedia - Computational electromagnetics analysis URL.

performances is extremely accurate. Note that an S-parameter model is defined in the frequency domain. When used in a time domain analysis, the simulator will create an equivalent time domain model applying specific convolution algorithms that convert the multi-port bi-lateral frequency response into a multi-port bilateral impulse response.

The accuracy of the simulation results and the maximum frequency of phenomena that can be reproduced by the simulator are strictly related to the frequency range in which the S-parameter model is defined. In particular, the highest frequency of interest is set by the rise time and the fall time of the signals adopted to drive the switches. For this reason, although the analysis has been performed with a $70kHz$ switching frequency, being the rising and falling edges of the applied signals in the range of some nanoseconds, the EM model of the PCB was extracted up to the GHz range. In this perspective it becomes clear why parasitics of the PCB may have a considerable impact on the circuit behavior [62].

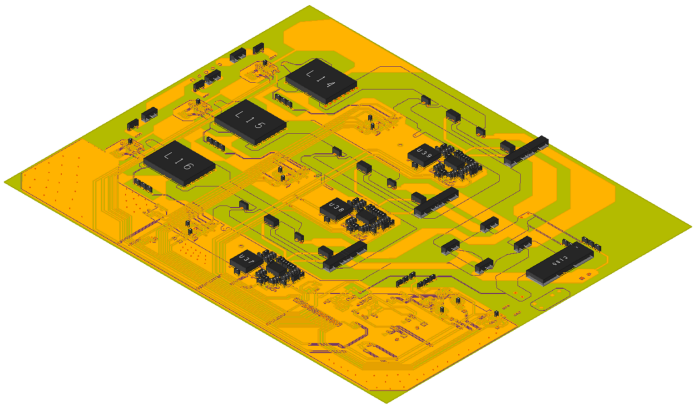
The frequency range of the PCB S-parameter model is not the only factor influencing the quality of the simulation results. An accurate model for the power switches and all the other active devices are also key factors to correctly reproduce the measurement results. Power switches are modeled by means of SPICE-like behavioral models provided by the vendor, in which the gate network is modeled with a linear RC circuit and non-linear effects in C_{GD} and C_{DS} are properly taken into account. In order to set and validate the procedure, instead of approaching the EM co-simulation flow from the design stage, it has been adopted after the first fabrication spin (PCB Rev A Fig.4.8) of the prototype so as to help the troubleshooting of the first design iteration and improve the layout of the second iteration.

Pre-layout analysis: Schematic only simulation Two different PCB layouts were analyzed: PCB Rev A is a 2-layer FR4 (Fig.4.8) while PCB Rev B is a 4-layer FR4 (Fig.4.9). The PCB layouts and the corresponding stackups are shown in (Fig.4.10 and Fig.4.9) with the main geometry constraints.

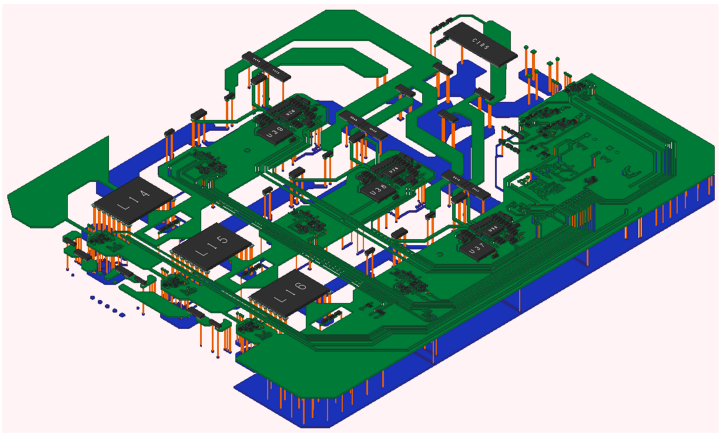
A preliminary circuit only simulation has been performed to evaluate the circuit performance neglecting the parasitic effects introduced by the PCB. The simulated circuit scheme is shown in Fig.4.12. The circuit is fed with sinusoidal sources of amplitude ($V_{RMS} = 220V$) operating at 50 Hz, in a classical 3-phase "Wye" configuration.

Control signals for the SiC switches are generated separately and applied to the three phases of the circuit with the proper relative phase and duty cycle, to provide the expected 800 V rectified voltage across the 60 Ω load. The networks (Fig.4.13) are used to provide a correct gate load and to properly shape the control signals rise and fall time.

Inductor and capacitor models include parasitics. As mentioned, active components (diodes and MOSFETs) are modelled by means of SPICE based models. Results are summarized in Fig.4.14. The control signals are applied directly at the MOSFET nodes (G_i and S_i in Fig.4.12, i = 1,2,3) and the connections to ground are ideal. V_{GS} doesn't show any disturbances and the circuit behaves as expected. These results confirm the correct circuit design and the proper duty cycle modulation of the control signals. This analysis will set a baseline for the following steps.



(a) All



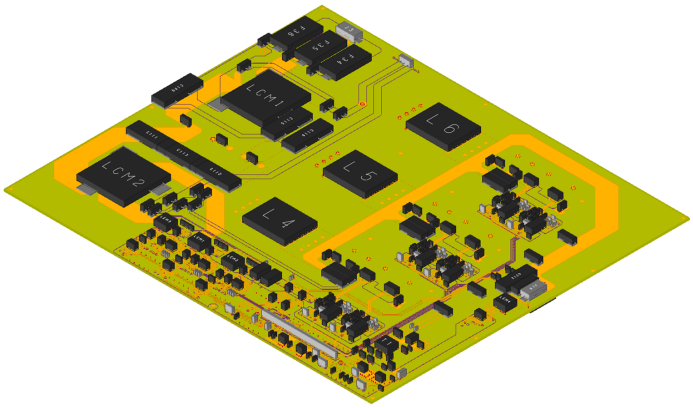
(b) Etch

Figure 4.8: Board Layout REVA.

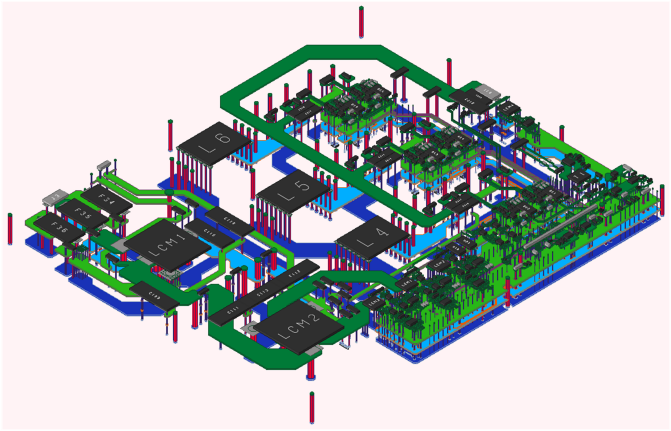
Post-layout analysis: EM model and circuit cosimulation The simulation setup used for the co-simulation is shown in Fig.4.15. Circuit components and drive signals are the the ones in the pre-layout simulation and, as already mentioned, the effects related to the presence of PCB parasitics are modelled with an S-parameter matrix, extracted with an electromagnetic simulation of the layout. The reconnection of the electrical models of the circuit components with the S-parameter model of the board is automatically performed by the simulator tool by means of the so called circuit partitioning. Control signals and AC sources are applied externally.

First iteration result In Fig.4.16 are shown the co-simulation results for the input AC currents of the three phases (Fig.4.16 a) and the rectified output voltage (Fig.4.16 b).

Results are consistent with the ones obtained with the pre-layout analysis. However, when measured in the lab, the first version of the converter suffered from the presence of voltage spikes on the gate terminals. These signals could be detected already in low



(a) All



(b) Etch

Figure 4.9: Board Layout REVB.

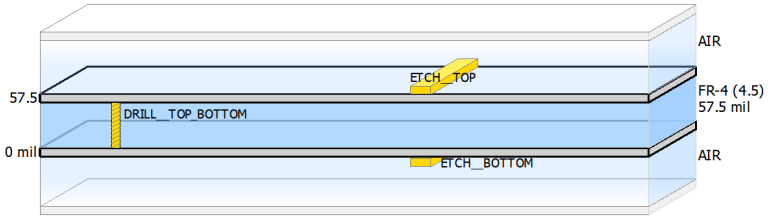


Figure 4.10: PCB RevA stackup

power conditions, exceeding the SiC device V_{GS} breakdown voltage still during the ignition phase, leading to a failure of the application. Voltage spikes can be easily reproduced in the post-layout simulation. In 4.18.a are shown V_{GS} signals of all six switches in which is clearly visible the continuous overshoots that overcome the typical breakdown voltage

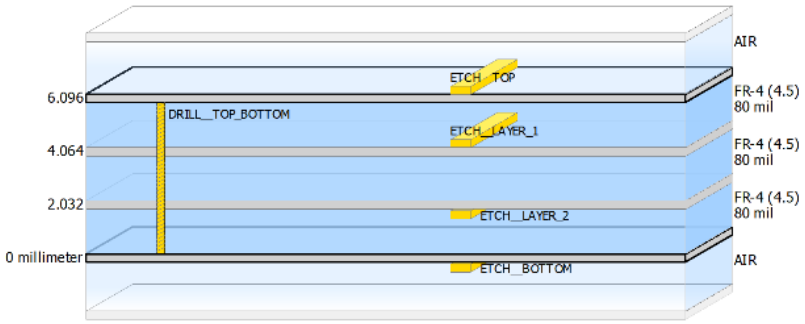


Figure 4.11: PCB RevB stackup

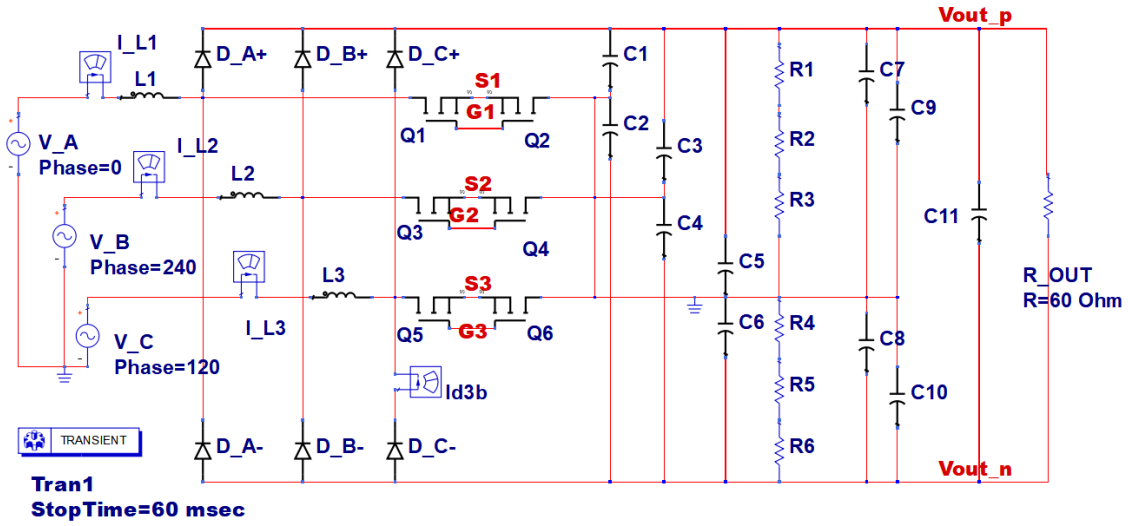


Figure 4.12: Circuit only setup

(22V) during the AC cycle (4.18.b). Recurrence of voltage spikes in all the switches ensures that this is a truly simulated phenomenon and that the spikes are not produced by accidental numerical errors in the simulation. This is even more evident in results shown in 4.18.c, in which the time resolution is pushed to the ns scale (max time step in the simulation is set to 0.6 ns), and the voltage ringing related to the spikes appears. 4.18.c also shows that the simulator is able to predict parametric oscillations [63] [64],occurring during a switching transient in presence of parasitic inductances in the driver circuit, according to the equivalent circuit represented in Fig.4.17. The fundamental frequency of the oscillation is 13.6 MHz

This effect has been also experimentally verified (Fig.4.19). To avoid the board failure, measurements were performed in low power conditions ($V_{RMS} = 42V$). Therefore, measured parametric oscillations are not so pronounced as the simulated ones. Oscillation frequency is in the same range as the simulation. (17.5 MHz). The discrepancy in the oscillation frequency between measurements and simulations is due to the fact that the driver

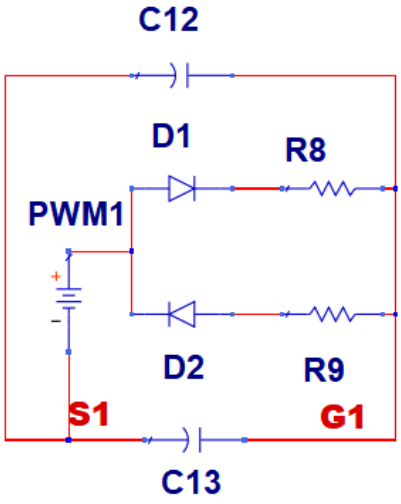


Figure 4.13: Driver circuit for Q_1 and Q_2. The other phases use similar circuits

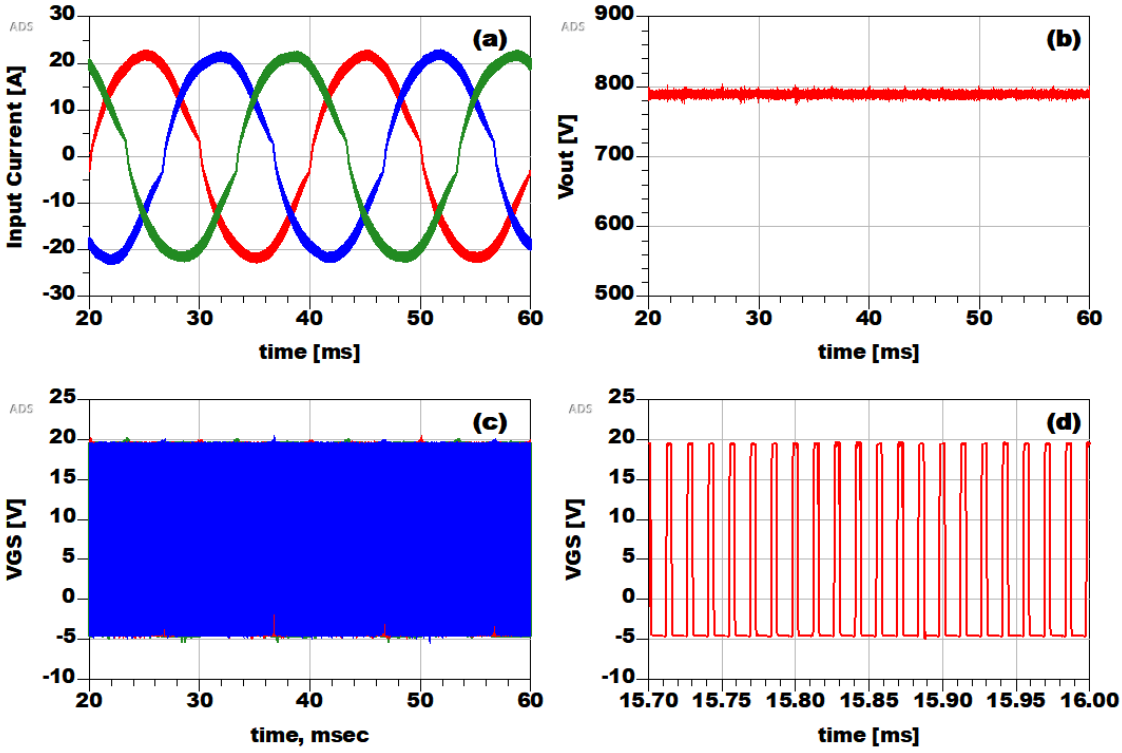


Figure 4.14: Simulation results of "schematic only" circuit. (a) Input Current. (b) Output Voltage. (c) V_{GS} of the switches. (d) Focus on V_{GS} for Q_1.

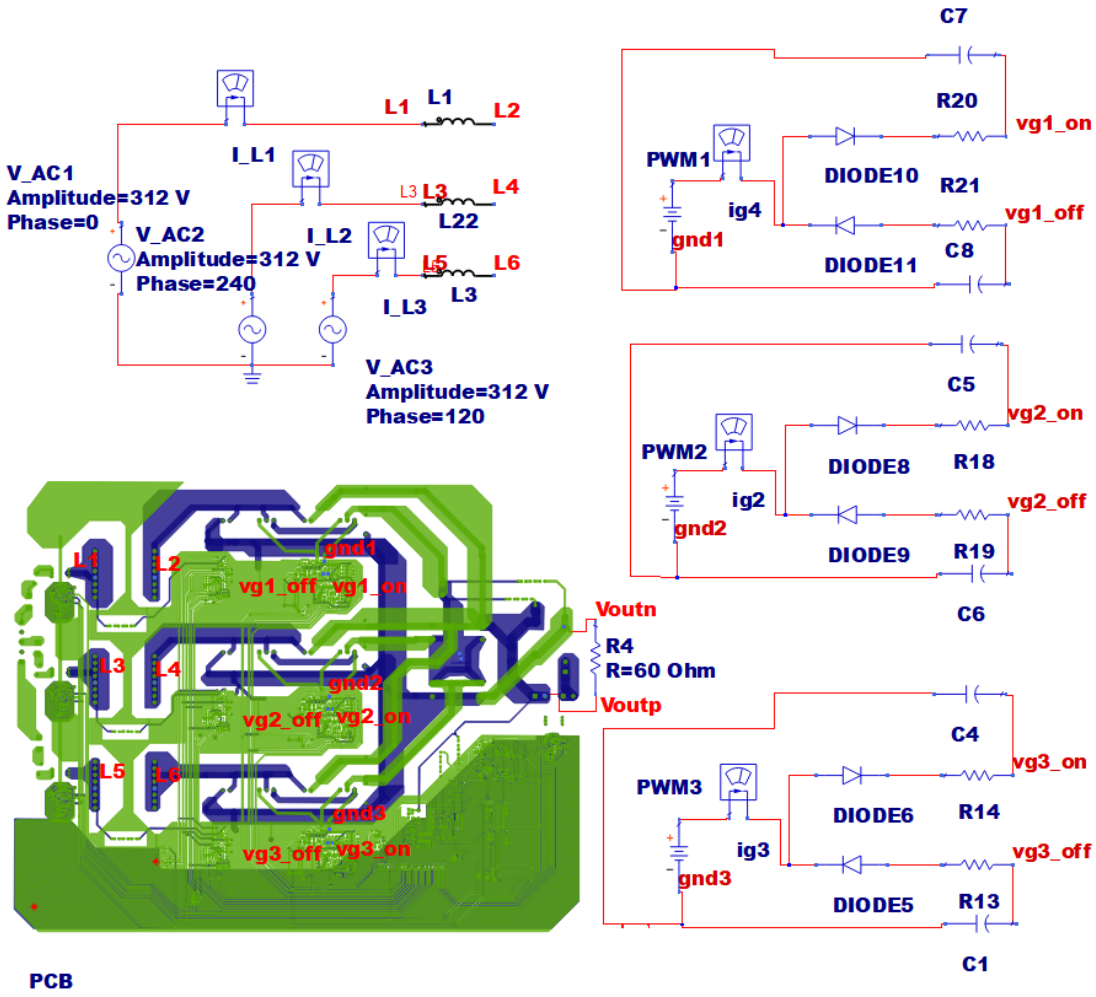


Figure 4.15: Simulation Setup. The EM model of the PCB is represented with a look-alike symbol. Circuit components included in the analysis are the same as pre-layout simulation

output impedance is not included in the simulation setup. There is an apparent contradiction between the clean simulated input current and output voltage and the extremely noisy and spiky driving signals. However, these results are not surprising. The electrical model used for the SiC switches doesn't include the breakdown region. In case the SiC is driven with a V_{GS} exceeding the breakdown voltage, the model provides the same $R_{DS_{ON}}$ as if used in normal operating conditions. As a result, I_{IN} and V_{OUT} are insensitive to the spikes.

Parasitic inductance estimation Although the parasitic effects have a distributed nature, the S-Parameter model of the PCB can be used to provide an estimation of the parasitic inductance of the driver circuit. This is just a "first order" approximation that neglects all the coupling and the capacitive effects and it only focuses on the dominant

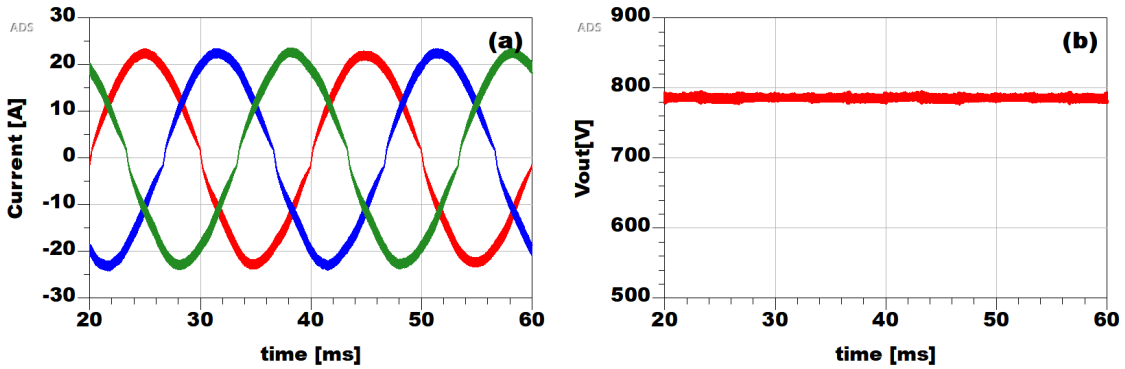


Figure 4.16: Input current and output voltage. Circuit co-simulation

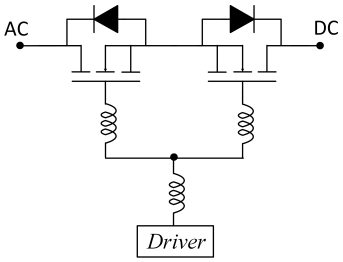


Figure 4.17: Equivalent model of the driver circuit

parasitic parameter. Power MOSFETs are connected to the driver through traces lying on top and bottom PCB layers. (Fig.4.20a). Roughly speaking, the associated parasitic inductance is proportional to the area encircled by the current loop created by the connections between power MOSFET and the driver. Current loops corresponding to Q_1 and Q_2 are shown in Fig.4.20a. The estimation of the inductance can be performed by running an S-parameter simulation of the EM extracted model of the traces, having the S-parameter port at the driver output (port 1) and the gate terminal shorted with the source (Fig.4.20.b). From the reflection coefficient $S_{1,1}$, the inductance L can be derived as follows:

In 4.3 Z_L is the impedance seen from port 1 and f is the simulation frequency. In Fig.4.22, the loop inductance of Q_1 and Q_2 drive circuit are plotted. Results for the other two phases are similar. The parasitic inductance of Q_1 is about $83nH$, compared with the $40nH$ inductance corresponding to Q_2. The significant unbalance between the two loop inductances of PCB RevA reflects the asymmetry in the layout. The traces feeding Q_1 are longer and the corresponding encircled area is larger. Consequently, the parasitic inductance is more than double compared to Q_2. The variation of the loop inductance versus frequency (especially for Q_1) is related to the distributed nature of layout parasitics: a simple series inductance model is not able to account for all possible parasitic effects. Nevertheless, this simple analysis provides a relevant indication about the main cause of

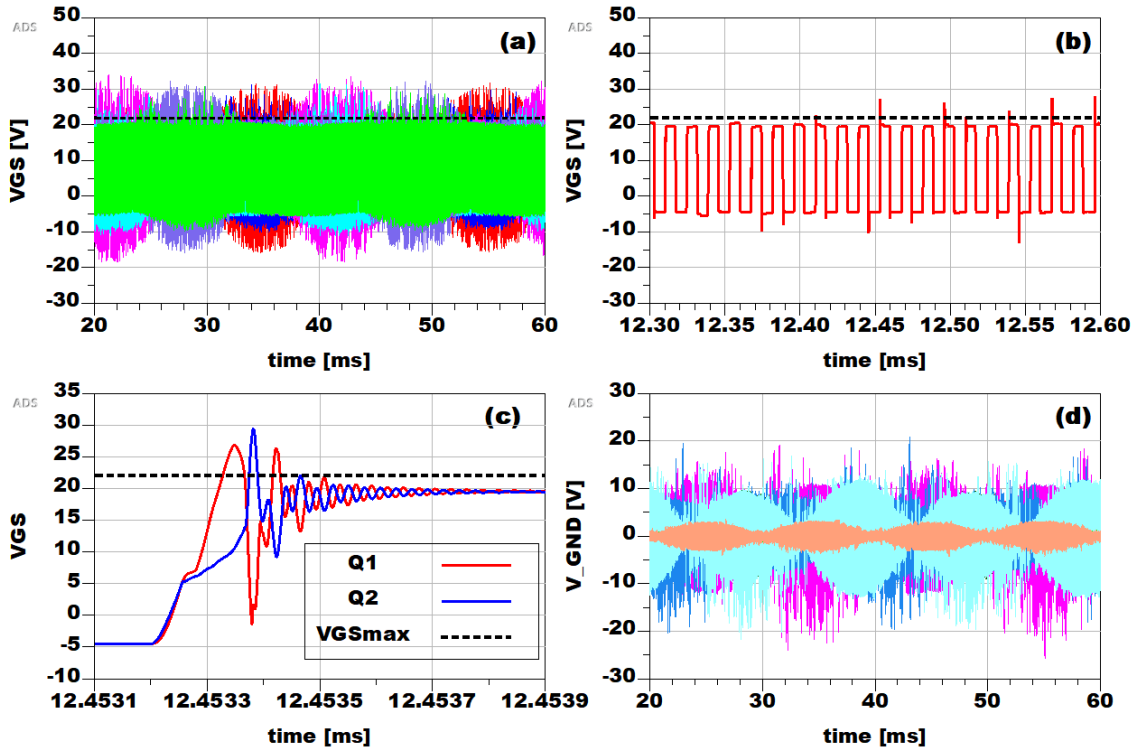


Figure 4.18: Simulation results for PCB Rev A post-layout analysis. (a) V_{GS} of all six switches. (b) Focus on V_{GS1}. Surge voltage spikes are evident and recurrent in the EM co-simulation results. (c) Parametric Oscillations for Q_3 and Q_4. (d) Ground bounces.

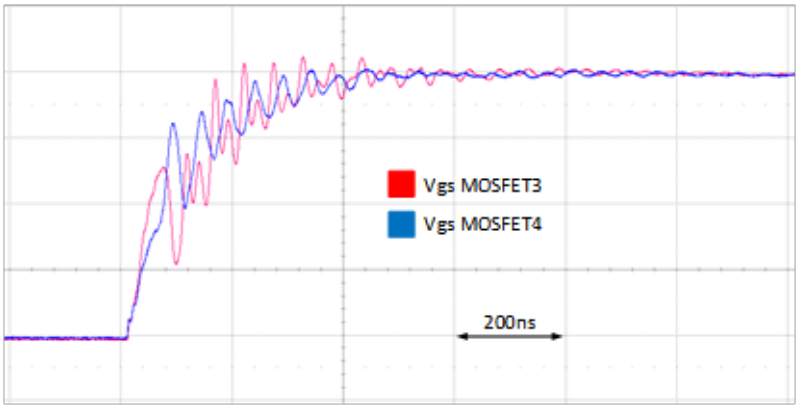


Figure 4.19: Measured V_{GS} for Q_3 and Q_4 in experimental real setup.

the surge voltage on the driver signals. Note also that the power switch input capacitance is $1.5nF$. Taking into account the $83nH$ inductance estimated for the bias loop, we would

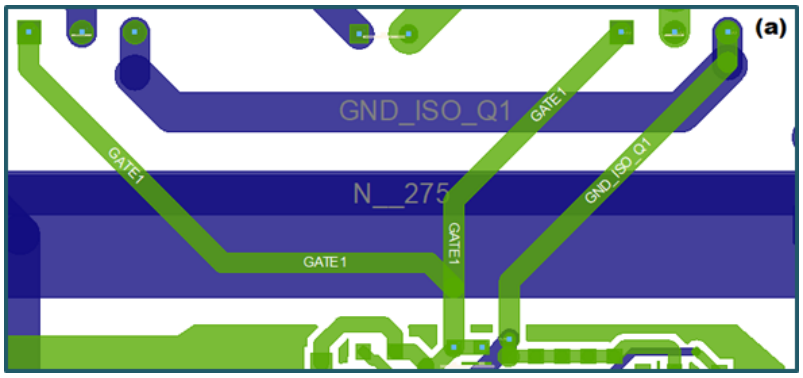


Figure 4.20: Current loops in the Power MOSFETs drive circuit for one of the phases

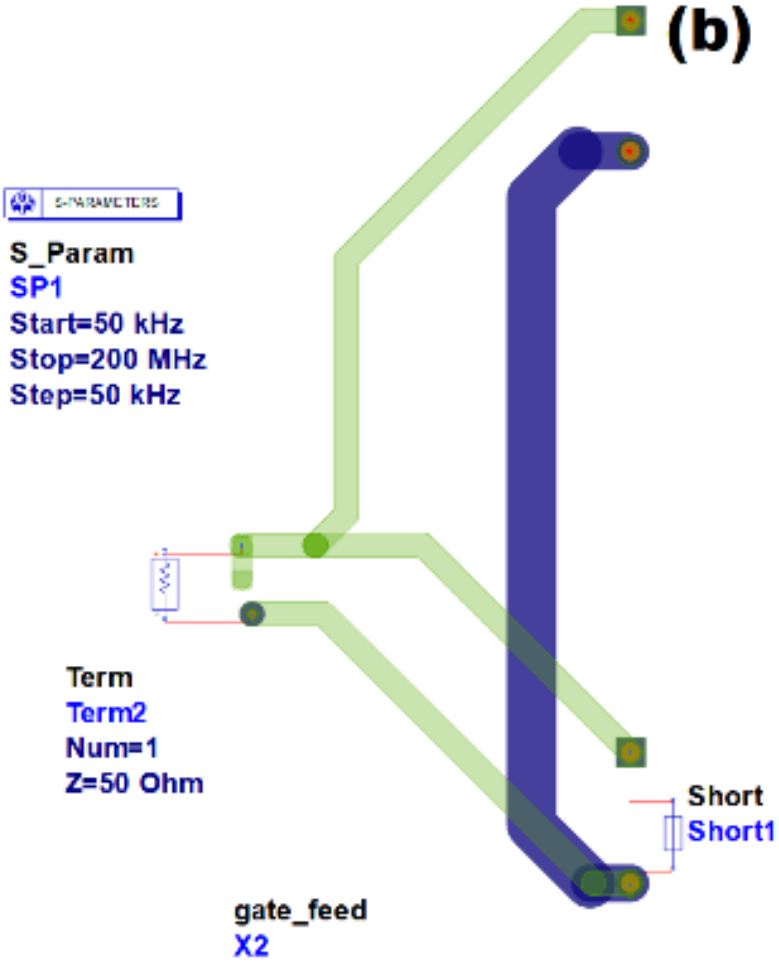


Figure 4.21: Current loops in the Power MOSFETs drive circuit for one of the phases.

expect a resonance frequency of $14.2MHz$, that is extremely close to the oscillation frequency ($13.5MHz$) estimated with the EM cosimulation. In the second iteration PCB, loop inductances are symmetrical and significantly lower (blue line and light blue line in Fig.4.22).

$$Z_L = Z_0 \frac{1 + S_{1,1}}{1 - S_{1,1}} \tag{4.3}$$

$$L = \frac{imag\,(Z_L)}{2\pi f} \tag{4.4}$$

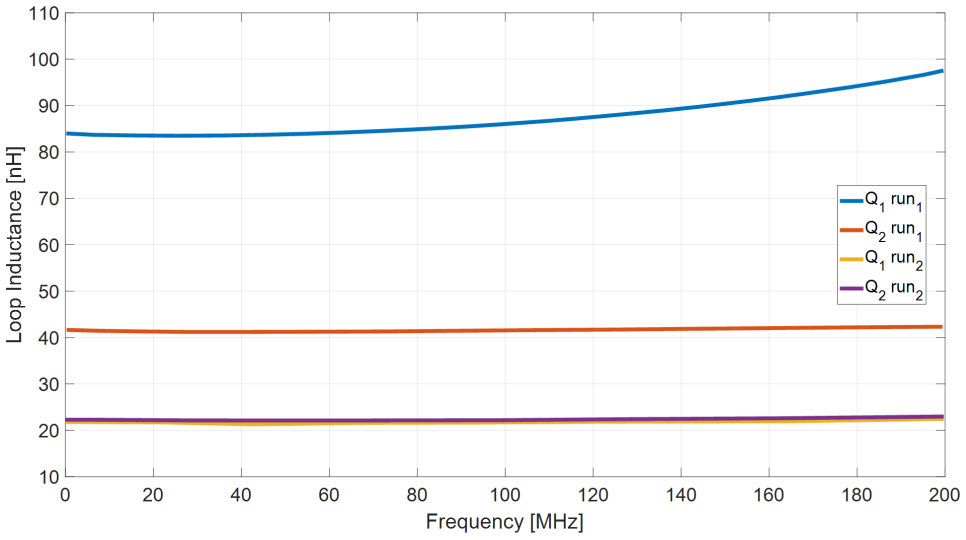


Figure 4.22: Loop inductance of Q_1 and Q_2 drive circuit

Second Iteration Results Simulation results provided a fundamental guidance to correctly redesign the board layout with some consistent improvements. Main target choosen for Rev B design are:

- The drive circuit of the two SiC switches of the same phase must completely decoupled. Each switch is driven with a dedicated driver.
- The two drive circuits of the same phase are designed with perfect symmetry - The layout geometry must be modified in order to minimize the gate inductance
- The number of layers of the PCB is increased to four. This choice enables the use of an RF-like good practice approach, leading to better shielding and improved isolation between critical traces, and to a good ground reference for the control signals.

Main components used for the second iteration are the same as the ones use in the first board release. The converter prototype using the second iteration board is shown in Fig.4.23. Post-layout simulation results are shown in Fig. 4.24. Improvements in the performance are significant. Noise in the drive signals has been largely reduced while the surge voltages have been significantly shortened. V_{GS} instantaneous value remains safely below its maximum rating ($V_{GS_{max}} = 22V$). Parametric oscillations and ground bounces have been also limited. Measurement results (Fig.4.25) confirm simulation data.

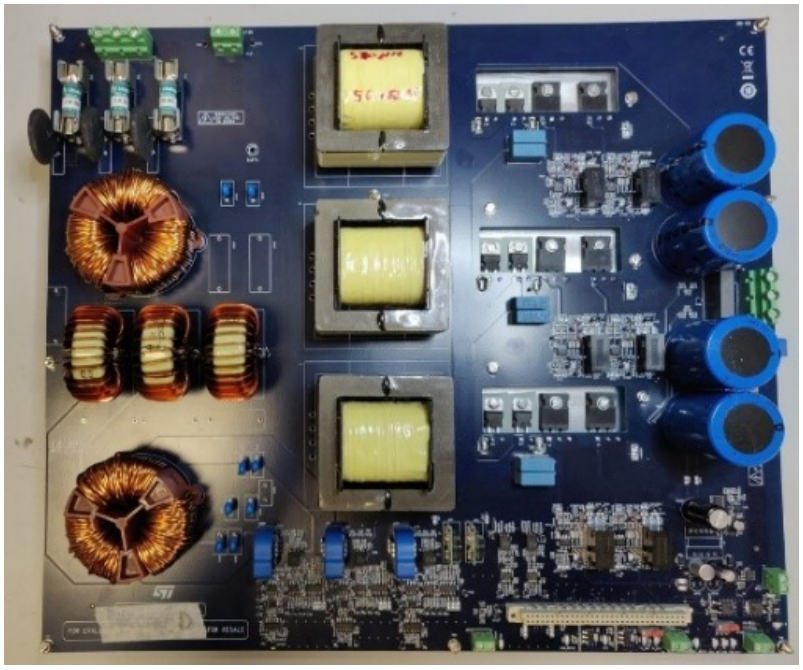


Figure 4.23: PCB Rev.B of the Vienna rectifier

In Fig.4.26 the frequency spectrum of Q_1 drive signal of the two PCB versions is compared. At the lower end of the frequency range, the two spectra are almost overlapped. In the range from $10MHz$ to $40MHz$ a significantly higher amount of energy is present for Rev A. This result is consistent with the different intensity of parametric oscillations discussed in the previous chapter. A deeper discussion on the frequency response of the rectifier is not addressed in the current paper and it is deferred to a future publication.

Conclusions PCB parasitics may dramatically degrade the performances of high-power high frequency designs if not properly considered from the early design stage. The results of the study discussed in the present work show how a non-optimal layout may lead to a design failure. To solve such a issue, a new design flow has been proposed based on both pre-layout and post-layout circuit analysis. EM co-simulation has been demonstrated to be an effective approach to predict the impact of PCB parasitics on the overall circuit performance, making available a tool capable to estimate unwanted coupling between the electrical traces and to provide valuable information for a successful design. This

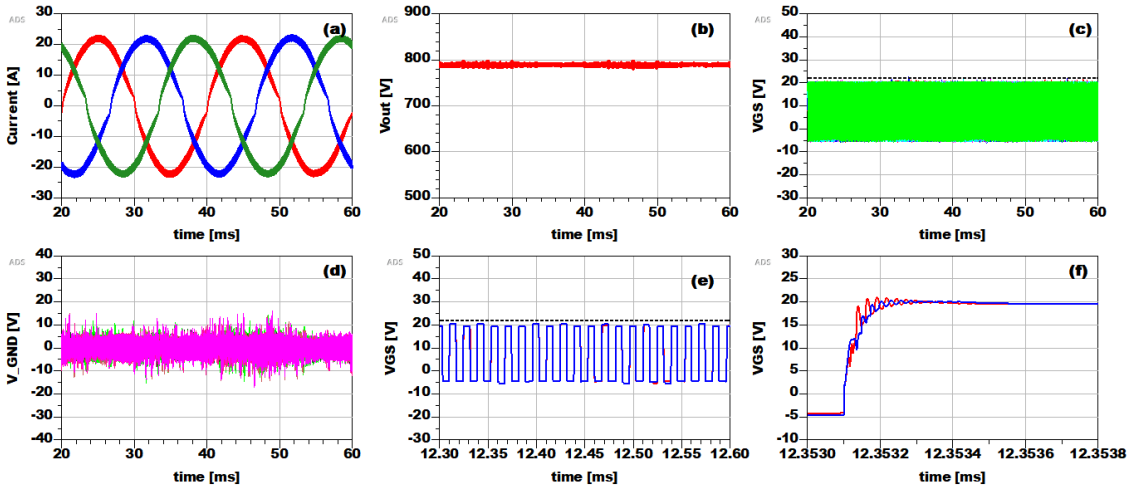


Figure 4.24: Post-layout simulation results for PCB RevB. (a) Input Current. (b) Output Voltage. (c) Drive signals. (d) Ground bounces (e) Drive voltage for Q_1 and Q_2 in a 300 µs scale. Results for the other two phases are similar. (6) Parametric oscillations for Q_3 and Q_4. Lower inductance and layout symmetry mitigate the oscillations.

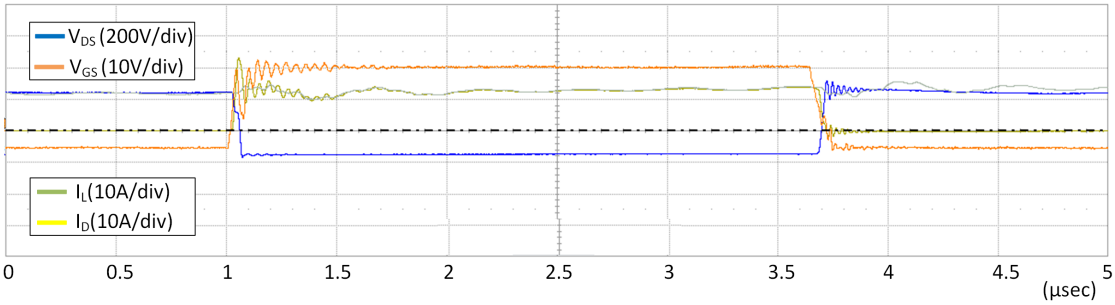


Figure 4.25: Switching behavior of PCB Rev.B at 50% load RON=22 Ω; ROFF=12 Ω

methodology has been applied to the analysis, the troubleshooting and the redesign of a $11kW$ VR using SiC power devices operated at $70kHz$. The ability to extract an electrical model for the PCB layout and to run a circuit co-simulation represents a unique and powerful tool that helps the designer to evaluate possible source of errors and design risks so that he can target a successful single iteration design process.

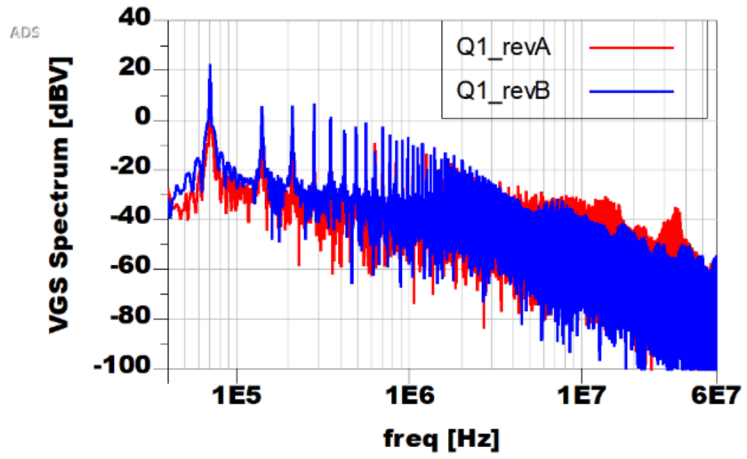


Figure 4.26: Frequency Spectrum of V_{GS} signal. Comparison between PCB RevA and PCB RevB

4.3 Chapter bibliography

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Chapter 5

Real time emulator of Converters

5.1 Model based System Desgin - MIL SIL PIL HIL

The Model-based Design method for software engineering is solely based on a representation of the software interacting with its environment, called model. This model can be understood as a graphic implementation specification of the system components. The key feature of this method is that the model can be run for simulation or system-testing purposes at any step of the development process. This means that the system behavior can be assessed right from the requirements phase of the project until series production without the need to change system description.

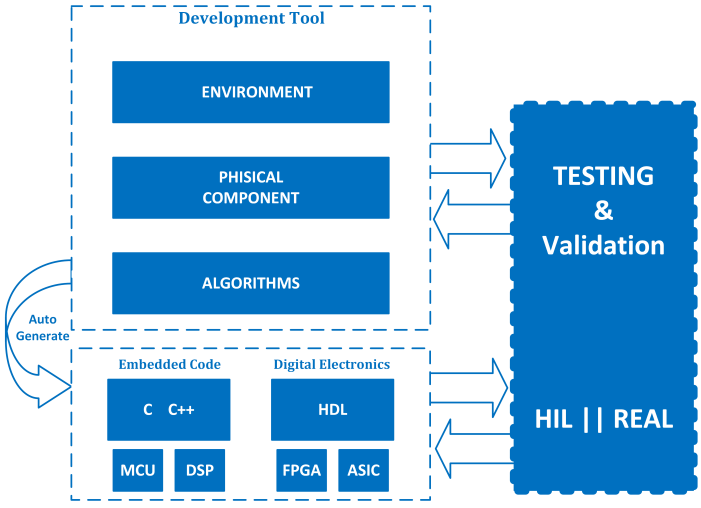


Figure 5.1: Model-based Design Workflow

Fig.5.1 illustrates the workflow of Model-based Design: Starting with the system model, containing both descriptions of the system under construction as well as the corresponding

environment, the code for the target platform is automatically generated, which may be C or $C++$ code for microcontrollers or digital signal processors as well as VHSIC Hardware Description Language (VHDL) or Verilog for Field Programmable Gate Array (FPGA) or Application specific integrated circuit (ASIC) designs.

The main advantage of this method is that the engineer never has to abandon the model in favor of another development tool. Thus, the need for an initial system sketch, a first mock-up, a prototype etc. is not given. All process phases (feasibility study, simulation, coding for prototypes and series, verification) are based on the same model. The process of Model-based Design is known for quite some time now. However, it is hard for the potential user of this method to assess the suitability for his project at hand.

The Benefits of Model-based Design are:

- Consistent documentation and implementation: The model description is a very appropriate source for the system documentation.
- Coding errors: Automatic code generation completely eliminates coding errors, making implementation specification (model) and actual implementation consistent as well.
- Documentation effort: As stated before, the model's graphic representation make it appropriate for documentation purposes and significantly reduce documentation costs.
- Communication improvements: The model can easily be understood be each and every project member, allowing simple but effective presentations for discussions of technical details or outsourcing of code development into other teams.
- Continuous verification and validation (V&V): is a key bonus of this method, allowing tests at every project stage. Problems can be tackled in the earliest possible stage, reducing the costs for late and potentially risky product changes.
- Possibility of major changes at late project phases:Due to the block oriented and therefore modular workflow as well as the automatic code generation, large functional blocks may be replaced at a late project stage.
- Code re-use: The simulation blocks can be included into an own library without extra effort, because they automatically exist as modules.
- No coding effort: Target specific implementation requires a lot of effort in development and debugging and may require an expert engineer.
- Less debugging: Extensive simulations reduce the need for in-system debugging.

At each step of design a specific approach using only software or both, software and hardware, is used to test the designed controller according to the predefined requirements. In addition, the tests should cover most of the potential operating conditions, and cover all the parts of the developed control logic. The tests are performed by keeping control

logic in a loop with the plant model. These tests are called X-In-the-Loop (XIL) tests, which include Model In the Loop (MIL), Software In the Loop (SIL),Processor In the Loop (PIL), and Hardware In the Loop (HIL) tests. The XIL is used for both tuning and V&V.

- **MIL :** MIL tests are used when the controller is being developed. In this stage, a model that represents the plant is used to provide the signals required by the controller. Both controller and model are developed and run on the same computer. Any fundamental problem in the control logic can be detected at this step.
- **SIL:** The developed control model after passing MIL tests language description is compiled to generate a system-function block which is a computer blocks. SIL is the cheapest way to test the production code without any hardware. [65]
- **PIL:** In PIL, the control model is compiled and the generated production code is loaded on the embedded target processor. Unlike MIL and SIL, the controller and plant model are on two separate PCs.
- **HIL:** In HIL, both model and controller are compiled and the generated codes will be uploaded on the related hardware. The generated code of the controller is uploaded on the Electronic Control Unit (ECU), and the generated code of plant is uploaded on the model simulator (Fig.5.2).

Particular relevance in the studies was given precisely to the HIL analyzing the various problems and developing strategies and platforms that would bring out the potential in the industrial field on the issues of electric drives and power converters (5).

5.1.1 Hardware In the Loop in power conversion

HIL simulation allow a dynamic test with a technique that simulates the I/O behavior of a physical system that interfaces to an electronic controller in real-time [66]. The keyword is "dynamic" because the values of stimulus signals generated by a simulator are a function of an electronic controller's response from the previous cycle. Other variables such as test profiles and in-line analysis results may also influence the calculation of stimulus values, but it is their dependence on the response from a unit under test that differentiates HIL simulation from other test techniques.

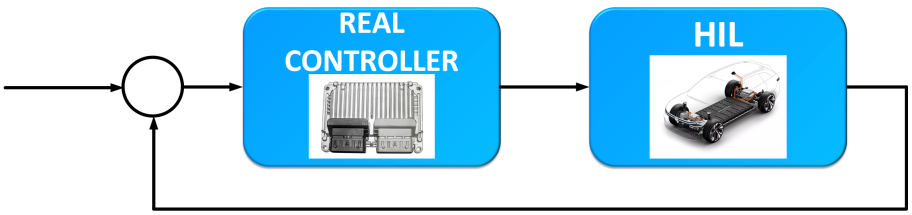


Figure 5.2: HIL concept

A HIL simulator can be use to emulate the current state of the system being controlled in a closed loop plant (Fig.5.2). Typically the HIL hardware consist in a embedded electronics or a general purpose computer system provided by I/O interface to emulate the sensors and actuator. To accurately represent how different operating conditions affect a controller electrically, a HIL simulator must create the impedance or loads, that an electronic controller experiences in real-world operation. In addition to being able to interface electrically with an electronic controller, a HIL simulator must determine the correct values to be produced in order to exercise or test the device. State charts, programming languages, and dynamic system models are commonly used to represent the I/O behavior (dynamic response) of a physical system. However, it is critical that a HIL simulator al so be able to produce these values with accurate timing characteristics. This typically requires a real-time operating system to ensure all signals can be updated at a rate that will preserve the realistic representation of a physical system in time. Depending on the complexity of a system being simulated and the fidelity of its representation, parallel processing techniques such as FPGAs, multi-core processors, and deterministic distributed processing interfaces may be necessary to complete output response calculations while maintaining timing accuracy (Fig.5.3).

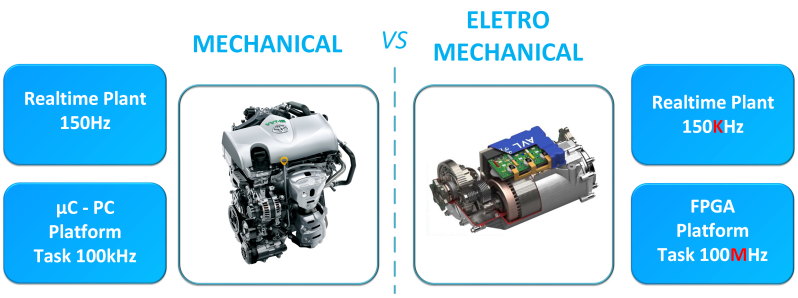


Figure 5.3: Thermal Motor vs Electrical Motor

The increasing complexity inherent in every system, in particular in the automotive or aerospace environment, works against business pressures to reduce development cost and increase product quality. Fortunately, HIL simulation has proven to be a practical solution to these diverging challenges [67]. While HIL simulation does not replace the need for physical testing, it does enable engineers to tests earlier in the development cycle providing the following benefits:

- Make educated design decisions – evaluate specific design alternatives early in the development process based on test data
- Resolve errors more efficiently – identify design errors earlier when they are less expensive to correct
- Achieve greater testing capacity – enable “lights-out” testing of systems where unmonitored physical testing is not possible

- Increase test coverage – test embedded controllers under extreme conditions that might not be practical for physical testing due to safety or equipment damage concerns
- Increase test repeatability – isolate deficiencies in electronic controllers even if they occur only under certain circumstances

5.2 FPGA technology

FPGA and Digital Signal Processors (DSP) offer unique and different options for signal processing. While DSPs will continue to be used for many of today's challenging applications, FPGAs have evolved as highly capable reconfigurable signal processors that complement DSPs in many ways.
DSPs have been the primary choice for signal processing applications for many years. While they are still widely used for many applications today, the higher performance and algorithm complexity, is fueling a rate of growth that Moore's Law [1] is hard pressed to keep up with.
As such, another option has emerged. FPGAs have evolved to become reconfigurable signal processors that warrant serious consideration for many of today's signal processing design challenges. A number of design criteria determine the best use of FPGAs and DSPs for signal processing applications. In addition, FPGAs can be complementary to DSPs. Industry analysts deem these criteria to be important for designers of today's DSP systems: performance, design flexibility, the effort and time required to execute the design, power consumption, the cost of the device and the overall system cost.

One of the fundamental differences between FPGAs and DSPs is that FPGAs feature hundreds of MACs and multipliers that can be used to build parallel DSP structures. A fully parallel 256-tap Finite Impulse Response (FIR) built using an FPGA could provide throughput as high as $500MS/s$. Again, control and memory operations may reduce this somewhat, but what is evident is that FPGAs can process samples at rates that are an order of magnitude higher than DSPs.
FPGAs allow to make changes during the design phase and once the design has reached production and this is important as it significantly helps to mitigate design risk and caters to specification changes. Traditional DSPs provide a hardware architecture that is fixed, yet can be programmed in multiple ways.
While DSP vendors go to great lengths to ensure that the mix of hardware features (e.g., I/Os, peripherals) meets the majority of customer needs, there will always be instances where users want additional features that are not offered. FPGAs, on the other hand, are hardware reconfigurable; the architecture can be changed multiple times. As the design or algorithm changes, the architecture can be modified at the same time. For example, if

[1] Moore's Law asserts that the number of transistors on a microchip doubles every two years, though the cost of computers is halved.

the designer of a filtering system determines that the sample rate for the system being designed has to be higher than originally anticipated, then it may warrant additional filter performance. The designer may opt to exploit more of the available parallel resources in the FPGA in order to cater to that additional performance requirement. FPGAs also allow the inclusion of other system components such as microprocessors for low rate control, serial transceivers that deliver multi-gigabits per second throughput, logic circuits and memory and peripheral interfaces.

In the past, FPGAs were typically programmed using hardware description languages Hardware Description Language (HDL) such as VHDL and Verilog, and many hardware designers implementing DSP functions into FPGAs today still prefer this approach. But, programming methodologies from leading FPGA vendors have evolved to include design entry from environments such as MATLAB® and Simulink®, which are more familiar to non-traditional FPGA designers such as system engineers and DSP algorithm developers and programmers.

Fig.5.4 shows how multiple tools can interface and allow today's diverse teams to essentially work in the language of the problem with which they are most familiar. The diagram shows that today, FPGA-based signal processing systems can be built using a combination of Simulink® models, MATLAB® code, HDL code and C. With such design tools, DSP designers who are unfamiliar with HDLs can manipulate the FPGA's resources and even program the FPGA from high-level design tools like Simulink® and MATLAB®.

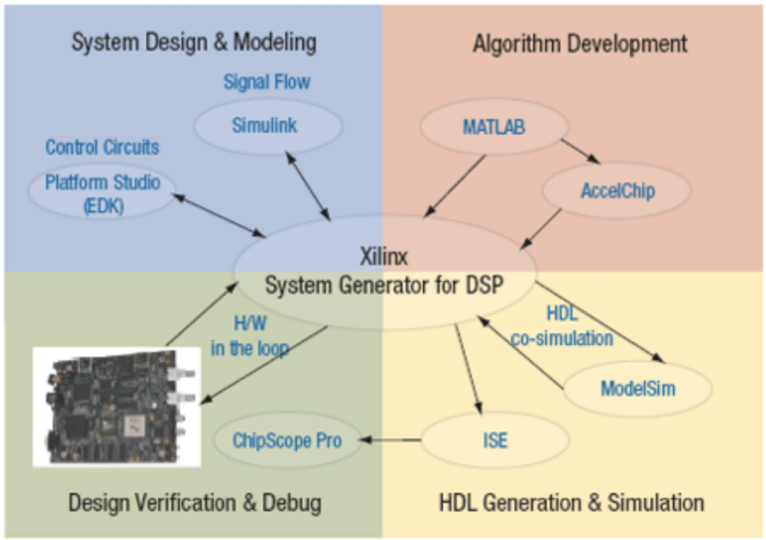


Figure 5.4: Accessing FPGAs in multiple ways using System Generator for DSP

5.3 HIL platform FPGA-based

FPGAs[2] are reprogrammable silicon chips designed to be configured by a customer or a designer after manufacturing. FPGA chip adoption across all industries is driven by the fact that FPGAs combine the best parts of application-specific integrated circuits (FPGAs) and processor-based systems. FPGAs provide hardware-timed speed and reliability, but they do not require high volumes to justify the large upfront expense of custom FPGA design. In Fig.5.5 there is an example of an FPGA board.

Figure 5.5: FPGA development board

There are several types of FPGAs, which include both one-time programmable devices and reprogrammable devices a large number of times. The first, called One Time Programmable (OTP) components, consist of components whose operating status changes permanently, allowing the configuration to remain on when the device is switched off. The second category includes devices based on Static Random Access Memory (SRAM)technology, which must be reprogrammed at each power-up, having a volatile configuration memory.

FPGA circuits are elements that have intermediate characteristics with respect to the FPGA devices and to those with Programmable Array Logic (PAL) architecture on the other.

The use of FPGAs components has some advantages over FPGAs:

- They are standard devices whose functionality to be implemented is not set by the manufacturer and can therefore produce large-scale low-cost

[2]Ross Freeman, the cofounder of Xilinx, invented the first FPGA in 1985.

- Their genericity makes them suitable for a large number of applications such as consumer, communications, automotive, and so on
- They are programmed directly by the end user, enabling the scheduling, simulation, and test time of the application to fall.

The great advantage over FPGAs is that they can make any changes or fix errors by simply reprogramming the device at any time. For this reason, they are used extensively in the prototyping phases, since errors can be solved simply by reconfiguring the device. The design environment is also more user-friendly and relatively easy to learn. Conversely, large numbers of applications are uneconomic because the unit price of the device is higher than that of the FPGAs (which, conversely, have high design costs). The cost of these devices is now declining rapidly: this makes them increasingly a viable alternative to standard cell technology. They are usually programmed with languages like Verilog or VHDL, but you should not forget the "schematic-entry" mode, which allows a quick and simplified approach to that technology while being of equal potential.

Unlike processors, FPGAs are truly parallel in nature (Fig.5.6), so different processing operations do not have to compete for the same resources.

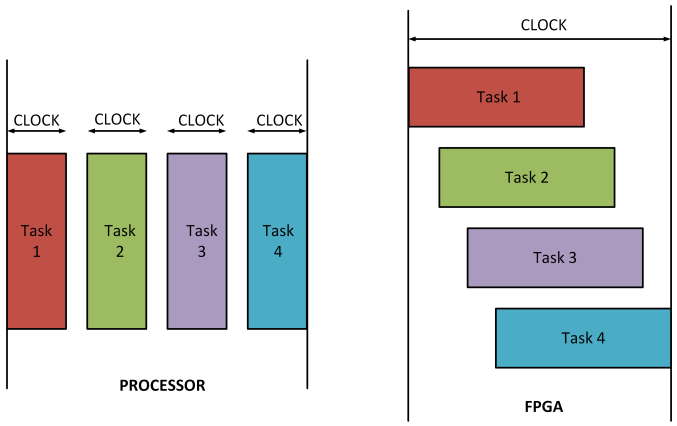


Figure 5.6: Sequenced vs Paralleled

Each independent processing task is assigned to a dedicated section of the chip, and can function autonomously without any influence from other logic blocks. As a result, the performance of one part of the application is not affected when you add more processing.

5.4 Structure of an FPGA

FPGAs contain an array of programmable logic blocks, (called configurable logic block, CLB, or logic array block, LAB, depending on vendor), I/O pads,and a routing channel that are hierarchy of reconfigurable interconnects that allow the blocks to be "wired together", like many logic gates that can be inter-wired in different configurations (Fig.5.7).

Logic blocks can be configured to perform complex combinational functions, or merely simple logic gates like AND and XOR. In most FPGAs, logic blocks also include memory elements, which may be simple flip-flops or more complete blocks of memory.

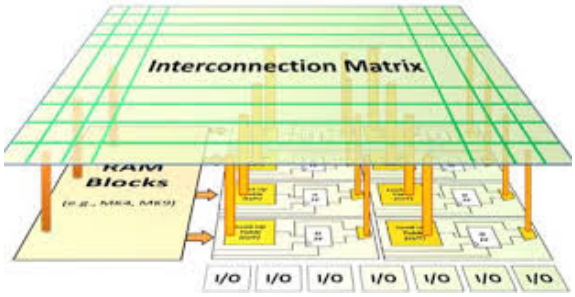


Figure 5.7: FPGA Interconnection matrix

Every FPGA chip is made up of a finite number of predefined resources with programmable interconnects to implement a reconfigurable digital circuit and I/O blocks to allow the circuit to access the outside world like in the Fig.5.8.

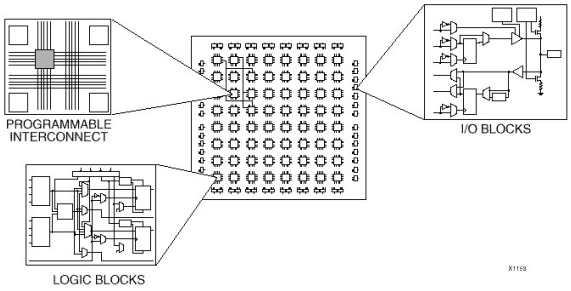


Figure 5.8: FPGA main parts

FPGA resource specifications often include the number of configurable logic blocks, number of fixed function logic blocks such as multipliers, and size of memory resources like embedded block RAM. Of the many FPGA chip parts, these are typically the most important when selecting and comparing FPGAs for a particular application. The Configurable Logic Blocks (CLB) are the basic logic unit of an FPGA. It consit of of a few logical cells (called ALM, LE, slice etc.). Sometimes referred to as slices or logic cells, CLBs cell consists of a Look Up Table (LUTs) a full adder "FA", a D-type flip-flop "DFF", and on mux to bypass the dFF in the case of cells purely combinatorial.

The representation of a tipical cell is shown in Fig.5.9.

Various FPGA families differ in the way flip-flops and LUTs are packaged together, so it is important to understand flip-flops and LUTs .

Flip-flops are binary shift registers used to synchronize logic and save logical states between clock cycles within an FPGA circuit. On every clock edge, a flip-flop latches the 1 or 0 (TRUE or FALSE) value on its input and holds that value constant until the next clock edge.

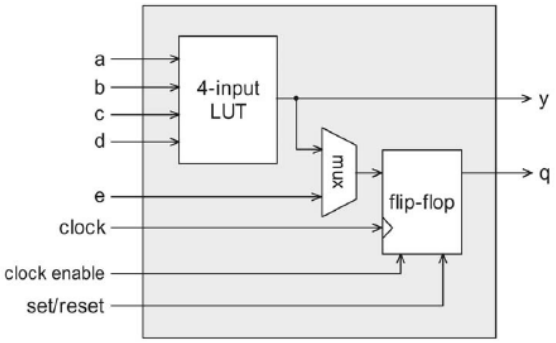


Figure 5.9: FPGA Logic Block

LUTs part map one any combinatorial function some inputs 1 output. Much of the logic in a CLB is implemented using very small amounts of Random Access Memory (RAM) in the form of LUTs. It is easy to assume that the number of system gates in an FPGA refers to the number of NAND gates and NOR gates in a particular chip. But, in reality, all combinatorial logic (ANDs, ORs, NANDs, XORs, and so on) is implemented as truth tables within LUT memory. A truth table is a predefined list of outputs for every combination of inputs.

5.5 Traditional FPGA Design Tools

Through the first 20 years of FPGA development, hardware description languages (HDLs) such as VHDL and Verilog evolved into the primary languages for designing the algorithms running on the FPGA chip. These low-level languages integrate some of the benefits offered by other textual languages with the realization of on an FPGA architecture circuit. The resulting hybrid syntax requires signals to be mapped or connected from external I/O ports to internal signals, which ultimately are wired to the functions that house the algorithms. These functions execute sequentially and can reference other functions within the FPGA. However, the true parallel nature of the task execution on an FPGA is hard to visualize in a sequential line-by-line flow. HDL reflect some of the attributes of other textual languages, but they differ substantially because they are based on a dataflow model where I/O is connected to a series of function blocks through signals. Then to verify the logic created by an FPGA programmer, it is common practice to write test benches in HDL to wrap around and exercise the FPGA design by asserting inputs and verifying outputs. The test bench and FPGA code are run in a simulation environment that models the hardware timing behavior of the FPGA chip and displays all of the input and output signals to the designer for test validation. The process of creating the HDL test bench and executing the simulation often requires more time than creating the original FPGA HDL design itself. Once you have created an FPGA design using HDL and verified it, you need to feed it into a compilation tool that takes the text-based logic and, through several complex steps, synthesizes your HDL down into a configuration file or bitstream that contains

information on how the components should be wired together. As part of this multistep manual process, you often are required to specify a mapping of signal names to the pins on the FPGA chip that you are using.

5.6 High-Level Synthesis Design Tools

The emergence of graphical design tools, such as LabVIEW® or Simulink® has removed some of the major obstacles of the traditional HDL design process. In addition, so that previous intellectual property (IP) is not lost, you can use the software above to integrate existing VHDL into your LabVIEW®/Simulink® FPGA designs. Then to simulate and verify the behavior of your FPGA logic, LabVIEW and Simulink offers features directly in the development environment. Without knowledge of the low-level HDL language, you can create test benches to exercise the logic of your design. Both LabVIEW® and Simulink® FPGA compilation tools automate the compilation process, so you can start the process with a click of a button and receive reports and errors, if any, as compilation stages are completed. If timing errors do occur in FPGA design, the tools highlights these critical paths graphically to expedite the debugging process. The adoption of FPGA technology continues to increase as higher-level tools, the standard microprocessor, and the FPGA architecture are making FPGAs more accessible. It is still important, however, to look inside the FPGA and appreciate how much is actually happening when block diagrams are compiled down to execute in silicon. Comparing and selecting hardware targets based on flip-flops, LUTs, multipliers, and block RAM is the best way to choose the right FPGA chip for your application. Understanding resource usage is extremely helpful during development, especially when optimizing for size and speed.

5.7 Numeric Rappresentation Fixed vs Float

Floating point math offers a wider range of numbers and more precision than fixed point math, various types of processors (DSPs, Micro Controller Units (MCUs), etc.) can be use this to do math function. Knowing the difference between "Fixed Point" FxP and "Floating Point" FP, and when to use which type of math can make a difference in terms of a faster calculation or a more precise calculation. A fundamental difference between the two is the location of the decimal point: fixed point numbers have a decimal in a FxP and FP numbers have a sign. Then Both types of numbers are set up in sections, and there's a placeholder for every portion of a number.

The floating number representation of a number has two part: the first part represents a signed fixed point number called mantissa. The second part of designates the position of the decimal (or binary) point and is called the exponent.

Only the mantissa m and the exponent e are physically represented in the register (including their sign). A floating-point binary number is represented in a similar manner except that is uses base 2 for the exponent. A floating-point number is said to be normalized if the most significant digit of the mantissa is 1.

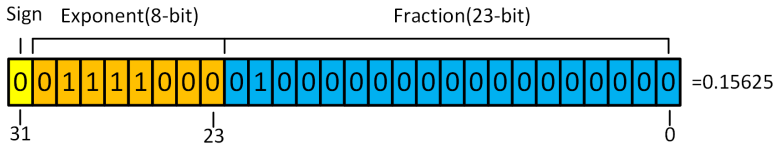


Figure 5.10: Single-precision floating-point number representation of number 0.15625 in the IEEE 754-1985 standard.

So, actual number is $(-1)s \cdot (1+m) \cdot 2^{(e-Bias)}$, where s is the sign bit, m is the mantissa, e is the exponent value, and Bias is the bias number.

Note that signed integers and exponent are represented by either sign representation, or one's complement representation, or two's complement representation.

According to IEEE 754 standard, the floating-point number is represented in following ways:

- Half Precision (16 bit): 1 sign bit, 5 bit exponent, and 10 bit mantissa
- Single Precision (32 bit): 1 sign bit, 8 bit exponent, and 23 bit mantissa (Fig.5.10)
- Double Precision (64 bit): 1 sign bit, 11 bit exponent, and 52 bit mantissa
- Quadruple Precision (128 bit): 1 sign bit, 15 bit exponent, and 112 bit mantissa

Fixed point numbers have a certain number of reserved digits that are on the left side of the decimal for the integer portion of the number. The numbers to the right of the decimal point are reserved for the fractional part of the number and this represent the precision of the numerical representation.

Very large numbers and very small numbers will have to fit in the same number of placeholders, what is actually bits, separated by the decimal in the same place, regardless of the number. For instance, if a fixed-point format will represent money, the level of precision might be just two places after the decimal.

The code for a fixed-point processor is written with respect to the decimal, which is in a fixed position. Fixed point math, independent of processor speed, is easier to code with and faster than floating point math. Fixed point is adequate unless you know that you will be dealing with higher numbers than the fixed-point unit can handle. Fixed-point numbers often are set up to use the most significant bit to represent a positive or negative sign. This means that a 4-bit unsigned integer has a range of 0 to 15 (because 24 = 16), while a 4-bit signed integer has a range of -8 to 7 . Again, this is because, in a number that has only 4 bits in which to represent it, there are only 16 total possible numbers that can be represented. (I.e., 24 = 16, where 4 is the total number of bits wide that the processor can handle in this example).

Floating point numbers also fit into a specific pattern. In fact, the Institute of Electrical and Electronics Engineers (IEEE) has a standard for representing floating-point numbers (IEEE 754). A floating-point number doesn't have a fixed number of bits before and after

a decimal. Rather, a floating-point number is defined by the total number of bits reserved for expressing a number. Like fixed-point numbers, floating point numbers have a predetermined number of bits to hold the floating-point number, which has a sign (positive or negative number) as well as a number (i.e., mantissa) with an exponent. All of this has to fit in the data path allotted for the processor, which could be 16-bit, 32-bit, or 64-bit, etc. In Fig.(Fig.5.10) is shown how a 32-bit wide floating point number might be expressed. Floating point numbers store as many precision bits as will fit in the data path, and the exponent determines the location of the decimal point in relation to the precision bits. The length of the exponent and mantissa would reflect the largest and smallest numbers anticipated by the application.

Moreover,floating-point numbers lose precision in that they only have a fixed number of bits with which to express a real number (e.g., 16-, 32- or 64-bit) and can seem confusing and complicated, but it's also time-consuming for a processor. Doing math using floating point numbers can involve several steps to account for differences in exponential values. The IEEE 754 standard, first published as late as 1985, resolved problems having to do with creating portable code with respect to floating point conventions. Prior to the standard, companies handled floating point math as they saw fit, making code difficult to port from one type of processor architecture to another. Many articles and white papers have been written about how to best use floating point numbers since processors can be quite literal in comparing numbers and overflowing the highest possible number is going to roll the number over to zero. Simply put, floating point numbers can be much more complicated than fixed numbers with regard to how processors handle them.

5.8 Mathematical and Numeric Rappresentation issue

Compatibly with what has been said in (5.7), in programmable electronics such as FPGA, FPGA and MCU that do not use accelerators such as DSPs, the use of a fixed point numerical representation is advantageous in terms of speed of execution. In particular, in FPGA or ASIC which base their operation on logical blocks, this representation is the only basic choice for executing mathematical relationships.

Although very high performance, FPGAs have some implementation limitations, in fact they manage to perform operations such as sums and products but operations such as divisions and, above all, trigonometric operations cannot be operated as a simple operator. Many articles propose solutions for optimized implementations of operations such as the divisor [68], trigonometric functions, cite [69] or mathematical functions that are more complex like the FFT [70].

Clearly an algorithm which can be the control one is constituted by a set of fundamental network operations and also for this type of processes an optimization draft is necessary to allow the benefits of using an FPGA not to be compromised [71].

Of particular importance is also the problem of running on processes designed with numerical representation at floating point on systems based on Fixed pOint [72] [73].

Recalling that an FxP representation has a limited and specific operatic arange and moreover the precision of the representation is linked to the choice of the number of bits

set for the integer and decimal part and frequently get overflow problems or bad precision that leads to the total correlation with the value in Floating point to represent.

This problem has also been addressed by laying the foundations for an automated iterative algorithm (5.8.1) created in Matlab which is very useful where it is necessary to obtain a good representation in terms of error as in the case of HIL processes, HIL, this is the real time emulator is generated starting from the analytical equation that comes from the physical laws of the process and that in the validation phase are compared with a model referring to a floating point that does not need attention on the representation like the fixed point.

5.8.1 Proposed Fixed-Point self-tuning algorithm

As explained in section 5.8 the use of Fixed Point (FxP) requires particular attention due to the possibility that a number is truncated or that part of the information to be lost is lost due to incorrect numerical representation. For this purpose a selftuning algorithm has been developed (Fig.5.11) which allows to obtain the FxP representation parameters (word, binary) (5.1) following specifications on the precision, expressed in relative terms and which can also take into account the actual numerical range of the variable to be represented.

$$FxP = Q[QI][QF] \tag{5.1}$$

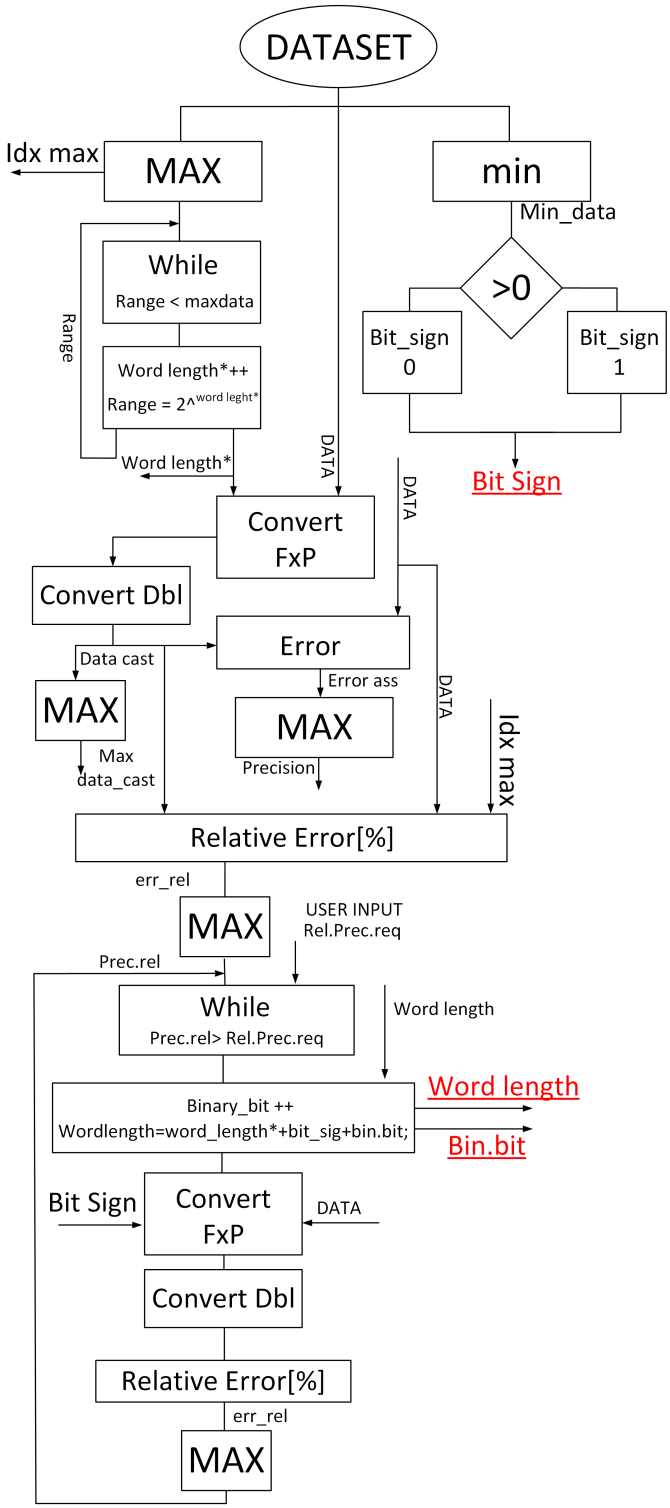


Figure 5.11: Selftuning FxP Algorithm

5.9 HIL study and development

Further studies focused on real time emulation systems based on FPGAs platforms, focused on the study of mathematical models and implementation strategies that could be used optimally on such hardware systems, able to emulate hardware platforms such as high power electronic converters and electrical drives in the automotive field. The platforms studied and developed after being tested have found use within the research laboratories of international companies to be able to test microcontrollers-based control platforms during the development and validation phases, anticipating tests on real systems and benefiting from all the criteria extensively described above.

In recent years, the opportunity to simulate power converters via HIL systems is becoming increasingly attractive in most of the safety critical applications,[5, 74–76]. FPGA based emulators is an interesting option due to their trends in peak performance, power consumption and sustained performances. Different implementations have been recently investigated and the one based on the combination of embedded system based on a FPGA board and high level graphical programming language is surely a promising way as it ensures satisfying performances and low investment costs, [77]

5.9.1 RealTime Emulation of a Three-Phase Vienna Rectifier with Unity Power Factor Operations

FPGA-based dynamic model of a three-phase Vienna Rectifier with unity power factor operations has been developed addressing applications as stationary chargers for electric vehicle or telecom rectifiers. Such a model has been implemented to be used in a Hardware In the Loop (HIL) system where the power converter has been replaced with an embedded system based on a FPGA board. The proposed system has been designed to test converter control algorithms in a fast and safe way. The proposed solution exploits an environment software platform with a high level abstraction, obtaining a good trade-off between accuracy and hardware resources, also allowing a faster prototyping procedure. The HIL implementation has been compared with that of the experimental rig, confirming a good agreement in terms of accuracy and dynamic behavior.

THREE-PHASE VIENNA RECTIFIER MODELING According with (inserire capitolo VIENNA) the Vienna rectifier power topology is used in high- power, three-phase power factor correction applications such as off-board electric vehicle Electric Vehicle (EV) chargers, telecom rectifiers, and as active front-end of grid connected converters [46]. The realization of the AC/DC input stage with uncontrolled three-phase bridges is motivated by the requirement of a high-power density, high reliability, robustness, and low cost. However, the latter solution produces significant low-order current harmonics in the main grid, negatively impacting on the normal operation of other local loads. In [50] is presented an interesting overview of a three phase PFC AC/DC converter. In literature different works have been presented addressing the design of both the average model [78] [79] and the steady state model [80] of the Vienna rectifier. The power converter topology is shown in Fig.5.12.

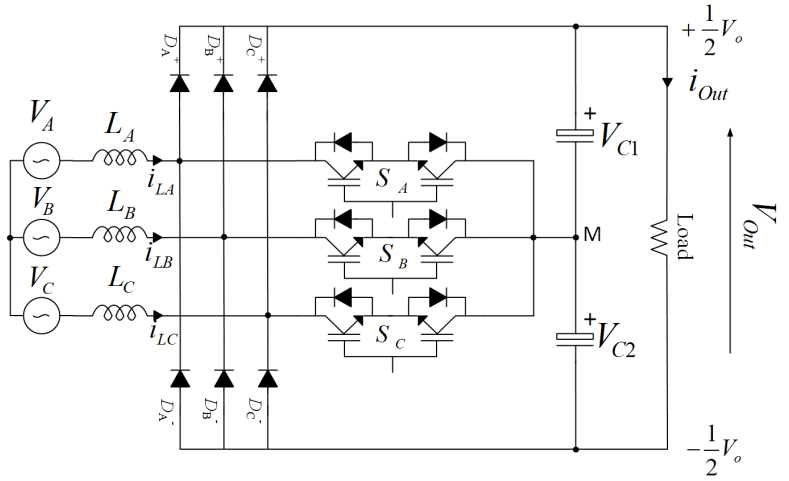


Figure 5.12: Vienna Schematic

The modelling of this converter has been suitably developed for testing control algorithms which must be able to satisfy the power quality standards for grid connected systems [81] [82]. According to the topology, shown in Fig.5.12 an average model of the Vienna Rectifier has been considered where the power devices are considered ideal. The bidirectional power switches of a generic phase *"j"* $= a, b, c$ are modelled with an ideal devices (5.2) driven by the signal *"*S_j*"*,$(j = a, b, c)$, Fig.5.13:

$$S_{\mathrm{j}} = \begin{cases} 0\, if\ S_{\mathrm{j}}\ is\ "off" \\ 1\, if\ S_{\mathrm{j}}\ is\ "on" \end{cases} \tag{5.2}$$

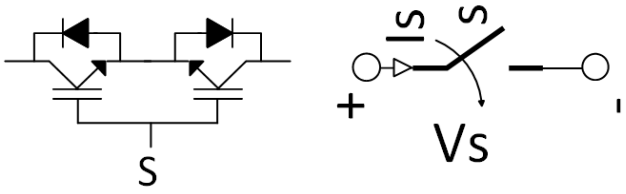


Figure 5.13: Ideal switch model.

The dynamic model of the power converter is given by the relationships 5.3,5.4,5.5, according to the state of bidirectional switches. The available states of the power converter for each converter leg are displayed in Fig.5.14.In the relationships V_{S_j} is the phase voltage, V_{C_1} is the high side capacitor voltage, V_{C_1} is the low side capacitor voltage, R is the load, i_{S_j} the inductor current and i_j is the phase current.

$$V_{S_j} = L_S \frac{di_{S_j}}{dt}$$

$$C_1 \frac{dV_{C_1}}{dt} + \frac{V_{C_1} + V_{C_2}}{R} = 0 \qquad S_j = 0 \quad i_j > 0 \tag{5.3}$$

$$C_2 \frac{dV_{C_2}}{dt} + \frac{V_{C_1} + V_{C_2}}{R} = 0$$

$$V_{S_j} = L_S \frac{di_{S_j}}{dt} + V_{C_1}$$

$$i_{S_j} = C_1 \frac{dV_{C_1}}{dt} + \frac{V_{C_1} + V_{C_2}}{R} \qquad S_j = 0 \quad i_j > 0 \tag{5.4}$$

$$C_2 \frac{dV_{C_2}}{dt} + \frac{V_{C_1} + V_{C_2}}{R} = 0$$

$$V_{S_j} = L_S \frac{di_{S_j}}{dt} + V_{C_1}$$

$$C_1 \frac{dV_{C_1}}{dt} + \frac{V_{C_1} + V_{C_2}}{R} = 0 \quad S_j = 0 \quad i_j < 0 \tag{5.5}$$

$$i_{S_j} = -C_2 \frac{dV_{C_2}}{dt} - \frac{V_{C_1} + V_{C_2}}{R}$$

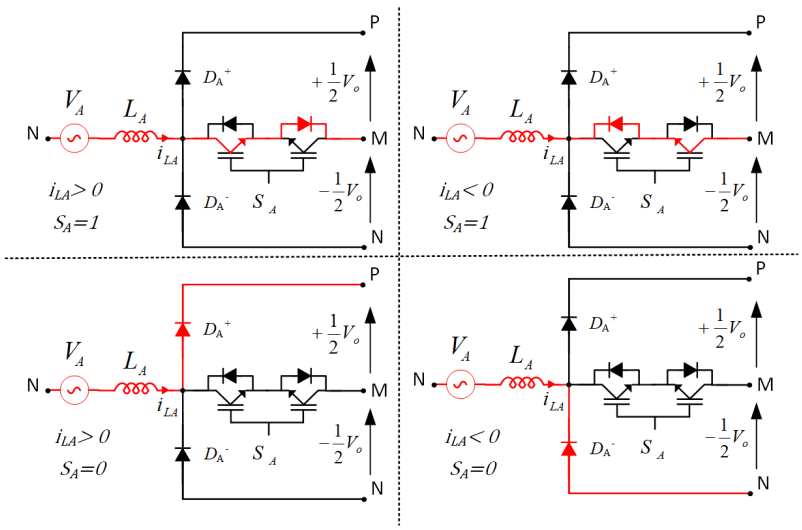


Figure 5.14: Current paths for the available switching states

For the three-phase systems, a matrix representation of the model is given in (eqs. (5.6) to (5.8)).

$$\begin{bmatrix} \frac{di_{sa}}{dt} \\ \frac{di_{sb}}{dt} \\ \frac{di_{sc}}{dt} \end{bmatrix} = \frac{1}{L_s} \left[\begin{bmatrix} V_{sa} \\ V_{sb} \\ V_{sc} \end{bmatrix} + \begin{bmatrix} (S_a - 1) \\ (S_b - 1) \\ (S_c - 1) \end{bmatrix} \begin{bmatrix} f^+_{(i_{sa})} V_{C1} - f^-_{(i_{sa})} V_{C2} & 0 & 0 \\ 0 & f^+_{(i_{sb})} V_{C1} - f^-_{(i_{sb})} V_{C2} & 0 \\ 0 & 0 & f^+_{(i_{sc})}) V_{C1} - f^-_{(i_{sc})} V_{C2} \end{bmatrix} \right] \text{[3]} \tag{5.6}$$

$$\frac{dV_{C1}}{dt} = \frac{1}{C_1} \left[\begin{bmatrix} f^+_{(i_{sa})} & f^+_{(i_{sb})} & f^+_{(i_{sc})} \end{bmatrix} \begin{bmatrix} (1 - S_a)\, i_{sa} \\ (1 - S_b)\, i_{sb} \\ (1 - S_c)\, i_{sc} \end{bmatrix} - \frac{V_{C1} + V_{C2}}{R} \right] \tag{5.7}$$

$$\frac{dV_{C2}}{dt} = \frac{1}{C_2} \left[\begin{bmatrix} f^-_{(i_{sa})} & f^-_{(i_{sb})} & f^-_{(i_{sc})} \end{bmatrix} \begin{bmatrix} (1 - S_a)\, i_{sa} \\ (1 - S_b)\, i_{sb} \\ (1 - S_c)\, i_{sc} \end{bmatrix} - \frac{V_{C1} + V_{C2}}{R} \right] \tag{5.8}$$

The overall FPGA logic interconnection block diagram of the Vienna rectifier model is summarized in Fig.5.15

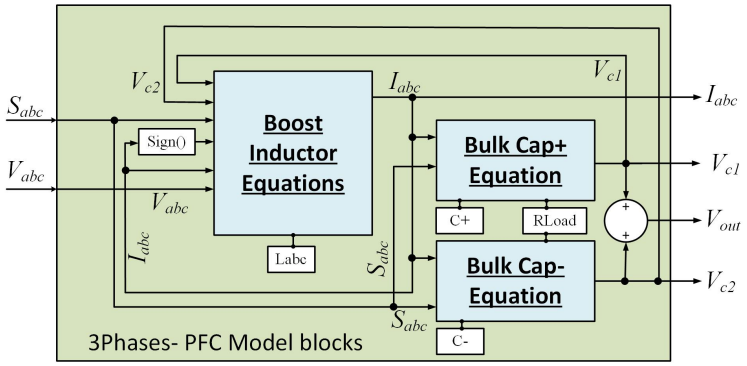


Figure 5.15: Overal FPGA logic interconnection block diagram of the Vienna rectifier model.

HIL TEST BENCH SETUP The scheme of the proposed test bench is shown in Fig.5.16 It is based on a modular architecture, composed by the following components: an integrated controller, a programmable FPGA and, a chassis for housing I/O modules. This hardware environment can be interfaced via Ethernet connection to the external control

[3] $f^+_{(i_{si})} = \frac{1 + sign(i_{si})}{2}; i = a, b, c$ $\quad f^-_{(i_{si})} = \frac{1 - sign(i_{si})}{2}; i = a, b, c$ $\quad sign(i_S) = \begin{cases} 1 \, if \, i_S > 0 \\ -1 \, if \, i_S < 0 \end{cases}$

systems. With regards to the software platform, NI LabVIEW FPGA Module is used to extend the LabVIEW graphical code on the target FPGA, allowing a fast and effective design of very complex systems, and at the same time providing debug functionality. A Graphic User Interface (GUI) in Windows environment is implemented to create a supervisory control and monitoring the host application to exchange data and commands with the FPGA. The Virtual Instrument (VI) called FPGA-VI is downloaded in the FPGA memory which is physically located inside the module "chassis" NI-cRIO9104 of the CompactRIO development platform of National Instrument and indicated as TARGET.

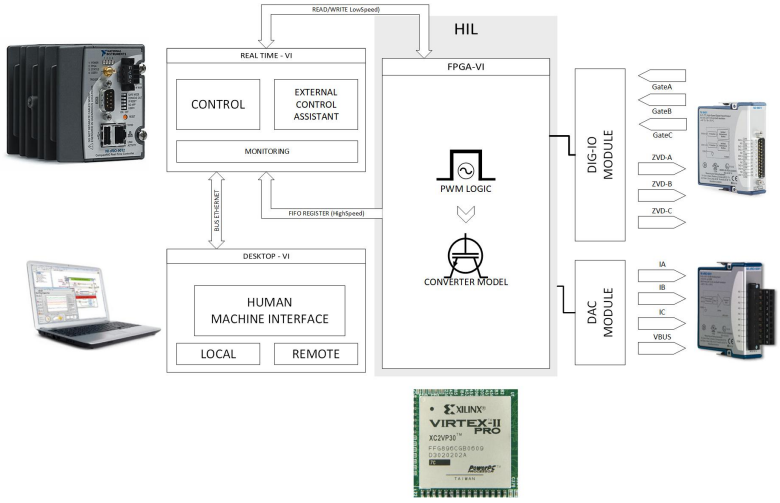


Figure 5.16: Block diagram of the HIL test bench

The models of the power converter, AC grid voltage emulation and standard triangular carrier generator of the Pulse Wide Modulation (PWM), used to test the control with internal modulator, are implemented in the FPGA-VI. The I/O devices NI-cRIO9201[4] and NI-cRIO9263[5] modules interface the mathematical model to the external control unit. By using First In First Out (FIFO) registers, the FPGA-VI also manages real-time communication exploiting Direct Memory Access (DMA). The last allows to monitor the model variables in the User Interface.

The control algorithm of the Vienna Rectifier has been implemented in the control unit board of Fig.5.17 based on STMicroelectronics STNRG388[6] (more details in Chap.7.1.1). The control algorithm is depicted in Fig.5.18. It features a modular architecture in which each phase is able to operate independently of the behaviour of the other phase currents [46][83].

It can be noted a nested control structure in which the inner current loop ensures high dynamic behaviour, while the external voltage loop allows to maintain a constant

[4]National Instrument - Voltage input C-Module.

[5]National Instrument - Voltage output C-Module.

[6]STMicroelectronics - Digital controller for power conversion applications.

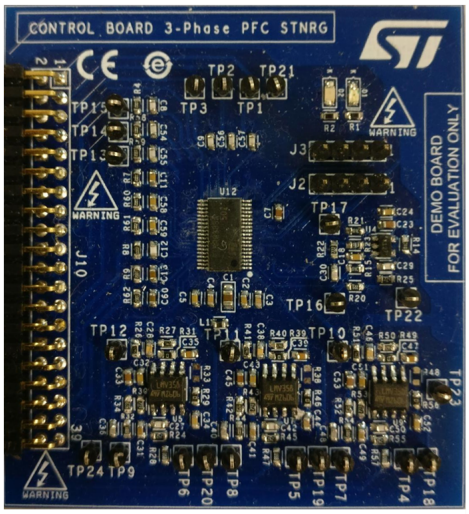


Figure 5.17: Control unit

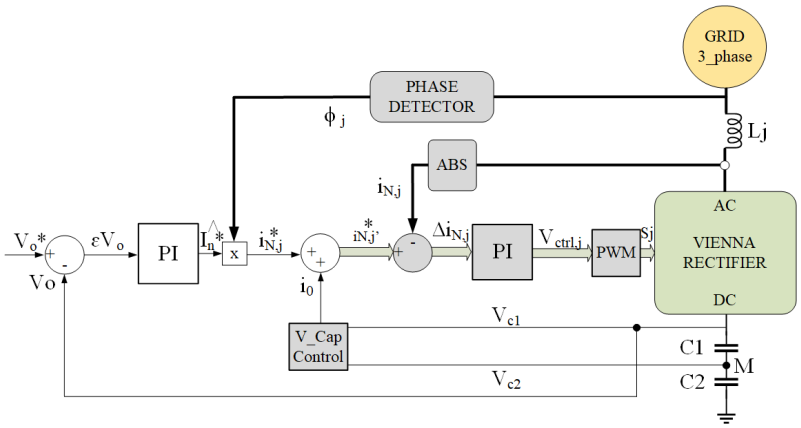


Figure 5.18: Block diagram of the implemented control algorithm

output DC voltage V_O for every load condition. The other blocks of the control algorithms are the voltage phase detector based on the zero crossing detection phase voltages and the "abs" blocks providing the rectified phase currents. The considered model has been implemented by using the High Throughput Math Functions FPGA LabView blocks. The equation (5.6) is depicted in Fig.5.20, while the relationships (5.7) and (5.8) have been implemented according to Fig.5.19.

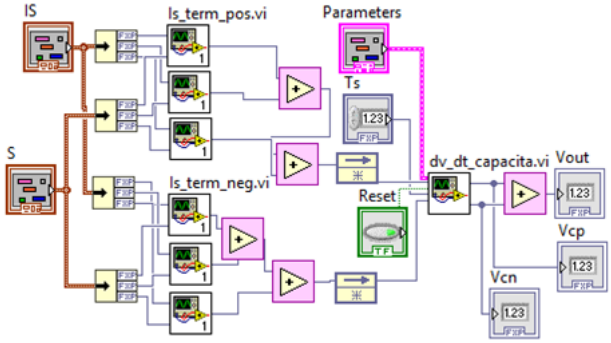


Figure 5.19: FPGA implementation of the eq. (5.7) (5.8)

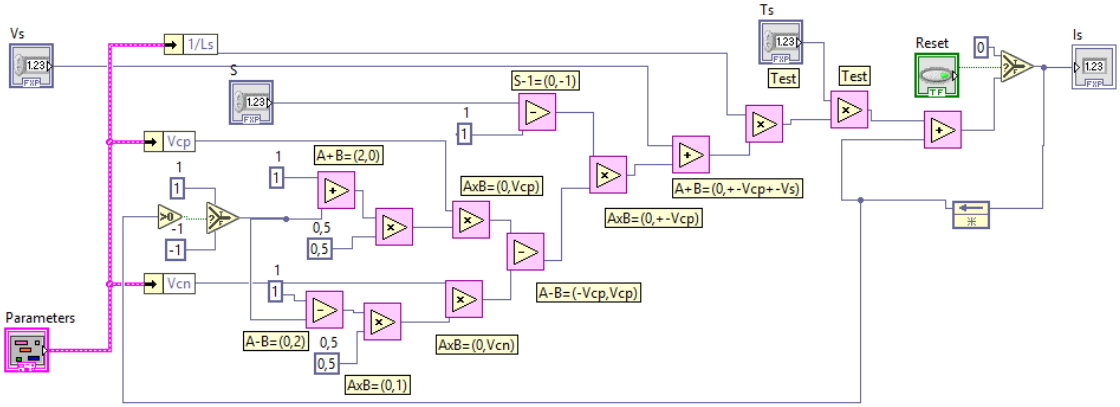


Figure 5.20: FPGA implementation of the relationship (5.6)

COMPUTATIONAL EFFORTS ANALYSIS The Vienna Rectifier model has been suitably connected to the other tasks according to Fig.5.16. Besides the model, the carrier generator and AC source have been implemented as shown in Fig.5.21,Fig. 5.22 and Fig.5.23.

The proposed Vienna Rectifier modelling can be considered a good trade-off between computational efforts and accuracy. The first metric can be evaluated in terms of total slices, slice registers, slice LUTs and block RAMs (Tab.5.1). The results of device utilization report for the rectifier , carrier generator , and a AC source are displayed in Fig.5.24. In this case, the base clock of FPGA is set to $10MHz$, while the carrier modulator is executed with the maximum FPGA clock equal to $40MHz$. The LUTs are used to minimize the computational efforts. In particular, they include 255 points to represent the triangular carrier signal and the sinusoidal waveforms of the AC source. Tab.5.1 shows a detailed view of the timing analysis results.

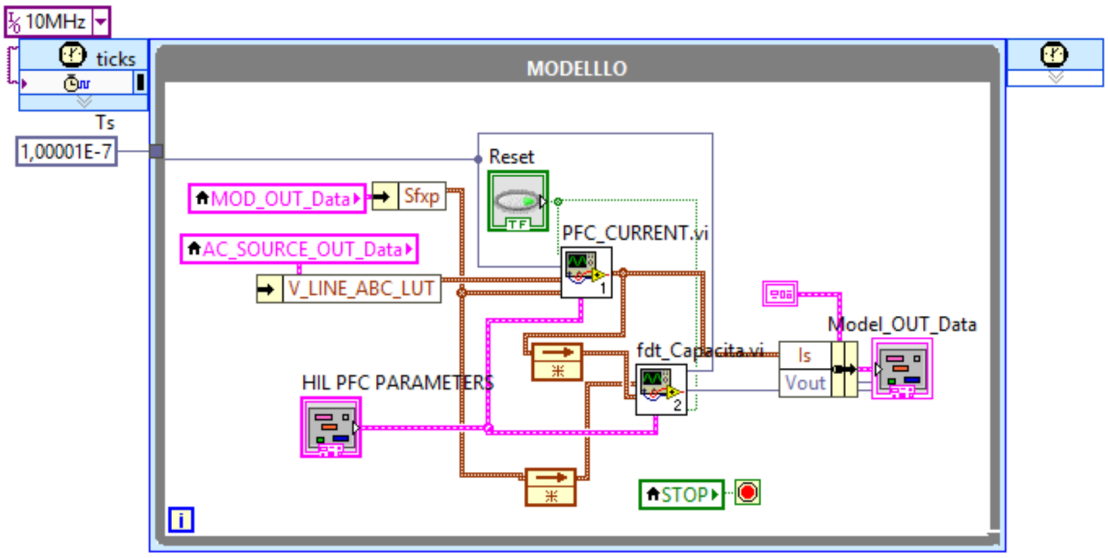


Figure 5.21: Overall Vienna rectifier model according to (eqs. (5.6) to (5.8))

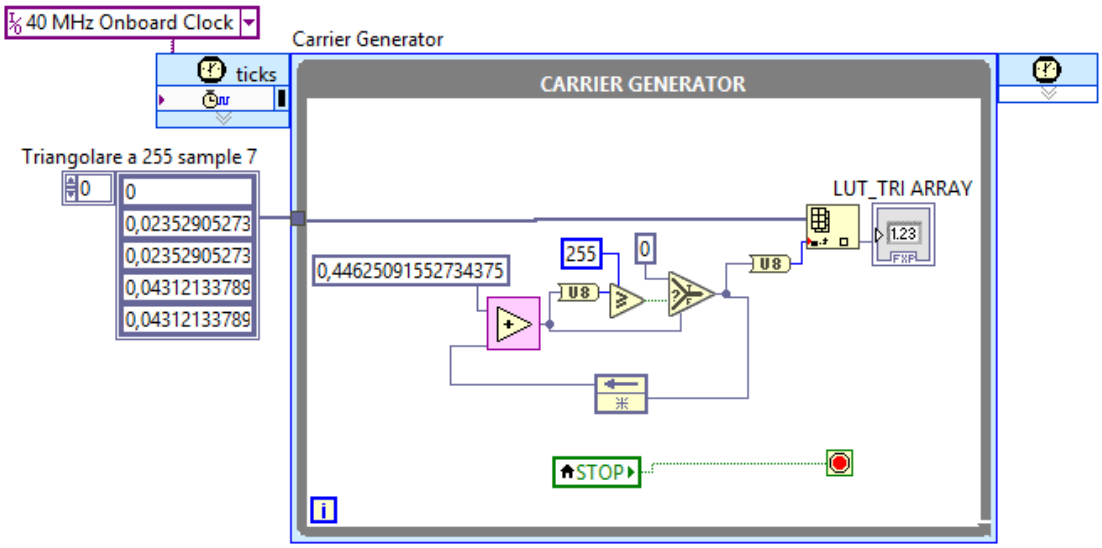


Figure 5.22: Implementation of the carrier generator

EMBEDDED TESTBENCH In order to verify the effectiveness of the HIL system, some off-line tests have been performed during both typical and abnormal operations. Initially, the control algorithm of Fig.5.18 has been executed on the same FPGA where the model is implemented. The results have been compared with those carried out with Matlab Simulink, a high-precision floating-point Simulation Platform (SP). The technical specifications of the emulated power converter are listed in Tab.5.2, according to (eqs. (5.9)

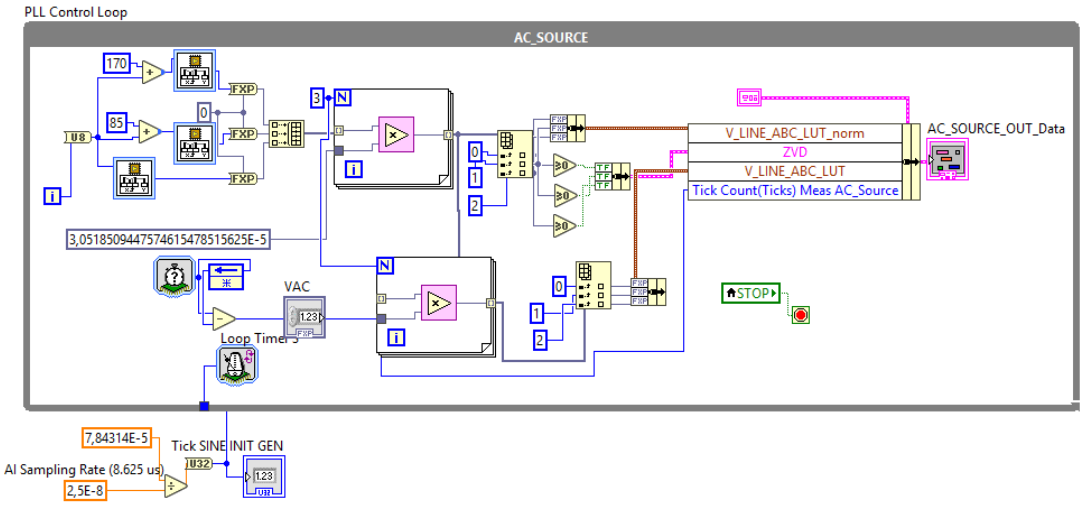


Figure 5.23: Implementation of the AC source.

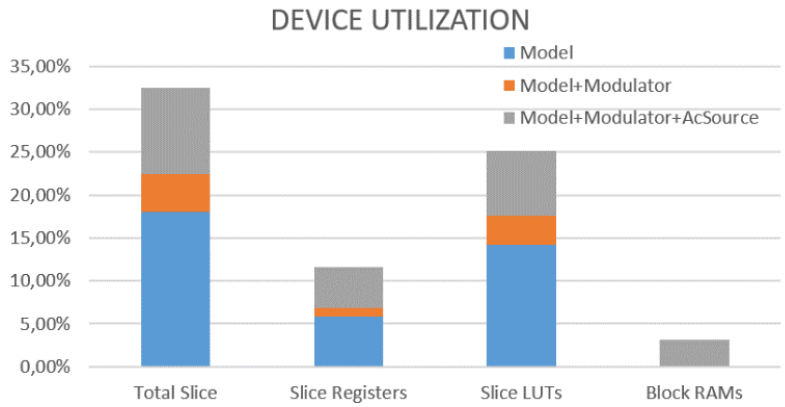


Figure 5.24: Computational effort required by the proposed modeling

to (5.11)).

$$M = \frac{\hat{U_N}}{\hat{V_O}/2} = 0.815 \tag{5.9}$$

$$L_N = \frac{V_O}{f_S \Delta i_L} \frac{\sqrt{3}}{4} M(1 - M\frac{\sqrt{3}}{2}) = 0.475mH, \Delta i_L = 5A \tag{5.10}$$

$$C_O = \frac{P_O}{2\,\pi\, f_{line}\, \Delta V_O\, V_O} = 0.955\,\mathrm{mF}, \Delta V_O = 10\,\mathrm{V} \tag{5.11}$$

The HIL system has been evaluated by assuming that the power converter is operated at rated conditions. Fig.5.25 shows the AC side voltage and current waveforms of two

Device utilization	
Total Slices	32,50%
Slice Registers	11,60%
Slice LUTs	25,20%
Block RAMs	3,10%
Timing	
MiteClk	33,00 MHz
40MHz Onboard Clock	41,71 MHz_{max}
10MHz	10,03 MHz_{max}
Execution	
Converter model	10 MHz
Internal modulator	40 MHz
FPGA clock	40 MHz

Table 5.1: Implementation analysis

Parameter	**Value**
$V_{AC_{LL}}$	400 V
f_{AC}	50 Hz
V_{OUT}	800 V
P_{OUT}	11 kW
f_s	70 kHz
L_i	475 µH

Table 5.2: Technical specification of the Vienna Rectifier converter

phases, and it is worth noting an effective phase alignment between such quantities, confirming Power Factor Controller (PFC) functionality. This result agrees with that related with the SP, as shown in Fig.5.26.

A voltage drop in the grid has been emulated as shown in Fig.5.27 In particular, a drop of the grid voltages from 311 V to 180 V at rated load is considered. The DC output voltage keeps a limited variation during the transient. Same test has been simulated with SP and a reasonable accuracy of the HIL results is confirmed, as shown in Fig.5.28.

Finally, a test of the proposed FPGA-based model with a significant load variation has been done. The results from the HIL platform and SP are shown in Fig.5.29 and Fig.5.30, respectively, confirming a satisfactory response of the system.

REAL-TIME TESTING The proposed control algorithm has been implemented in a mixed signal hardware and software system based on STNRG388[7] by STMicroelectronics.

[7]STMicroelectronics - Digital controller for power conversion applications.

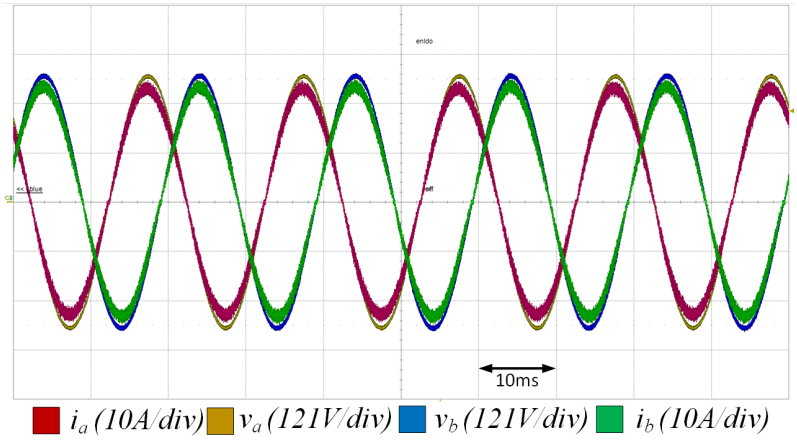


Figure 5.25: HIL system:AC quantities at rated conditions

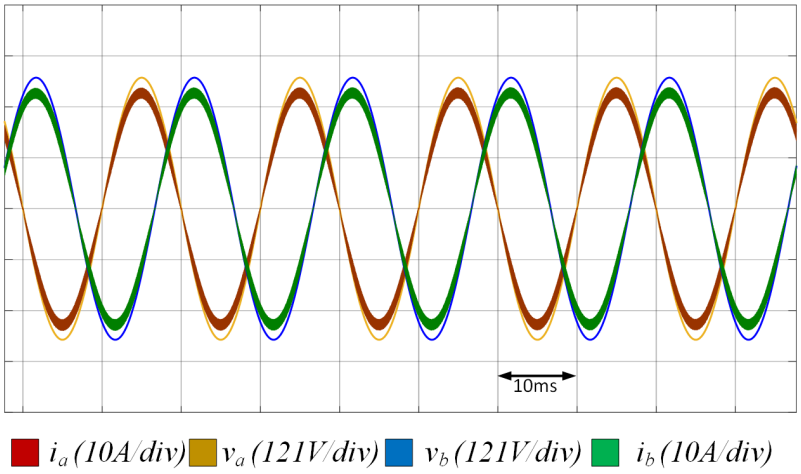


Figure 5.26: SP: AC quantities at rated conditions

The experimental setup is shown in Fig.5.31. The PWM signals from the control unit are acquired by the NI-cRIO9401[8], while another NI-cRIO9401[8] module produces the phases zero voltage edges and NI-cRIO9263[9] Analog Output module generates the output signals of the power converter model in terms of phase currents and output voltage.

Fig.5.32 shows the transient of the modelled system as a consequence of a voltage drop in AC source: the red trace represents the current feedback of a phase $i_{N,j}$, while the yellow trace is the reference current $i^*_{N,j'}$; the blue trace is the response of current control in terms of voltage value $V_{ctrl,j}$, used in the modulator to obtain the PWM signal

[8]National Instrument - Digital I/O C-Module.

[9]National Instrument - Voltage output C-Module.

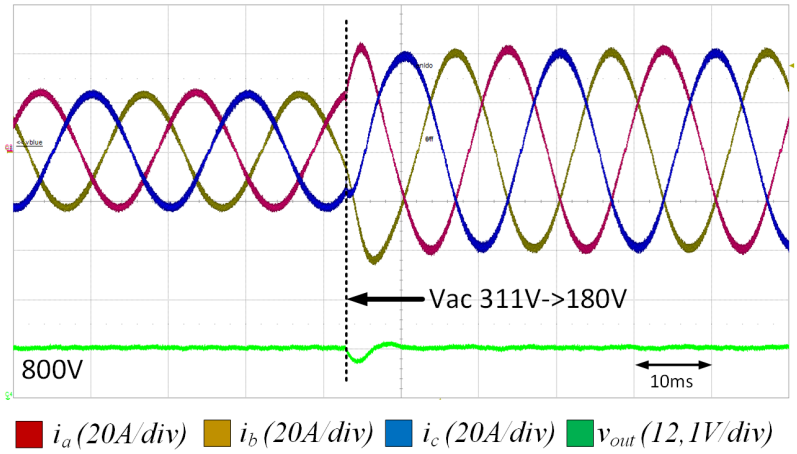


Figure 5.27: HIL: voltage drop test

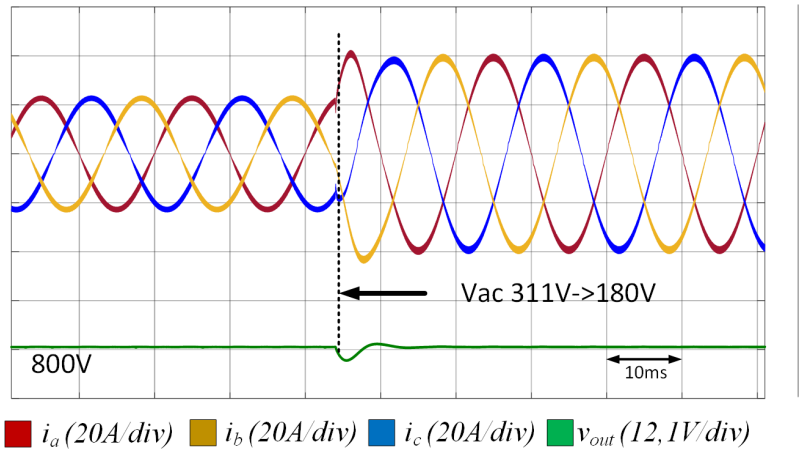


Figure 5.28: SP: voltage drop test

and the green trace shows the DC output voltage V_o. It is possible to note a good tracking capability of the control algorithm. Other results of the same test are shown in Fig.5.33, in particular the three input currents and the DC output voltage are shown. Note that all the phases behave in the same way.

CONCLUSION This activity shows the potential of an FPGA based emulation system that uses a high-level programming language for the implementation of the control of power electronics converters. Such an approach has been used to test a three-phase Vienna Rectifier control with power factor correction operation. An accurate model of the system has been implemented in a HIL using an FPGA board and used to design and test the control algorithm. The results show a good accuracy, confirming the consistency of the proposed approach for testing different control strategies as well as to properly tune the

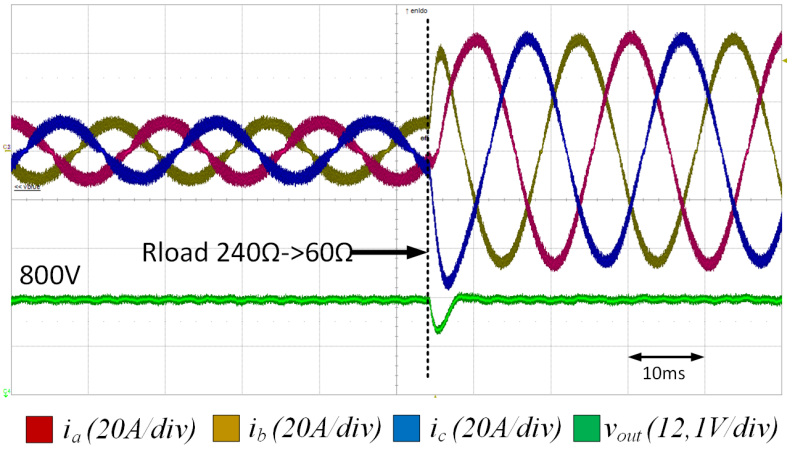


Figure 5.29: HIL: Load transient

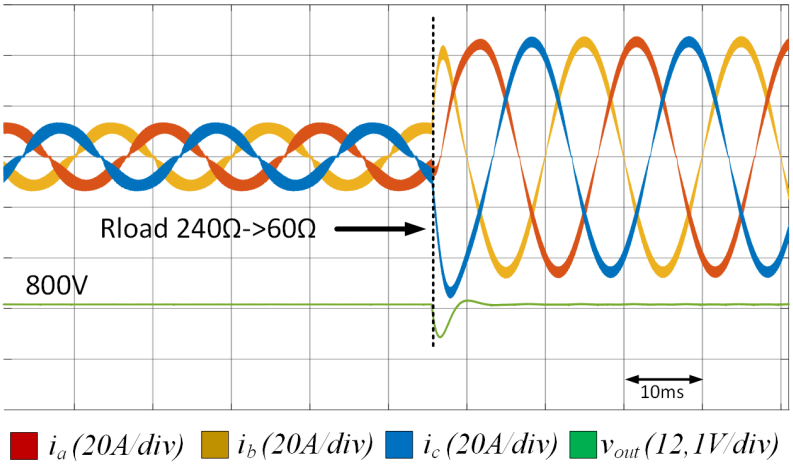


Figure 5.30: SP: Load transient

parameters of every regulators avoiding the risk of disruptive events in the real power board.

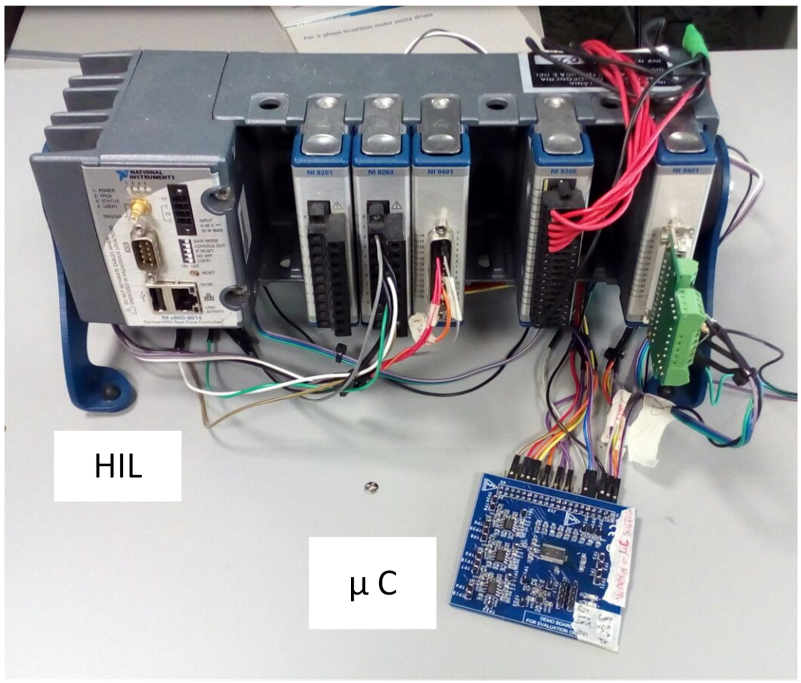


Figure 5.31: HIL testbench

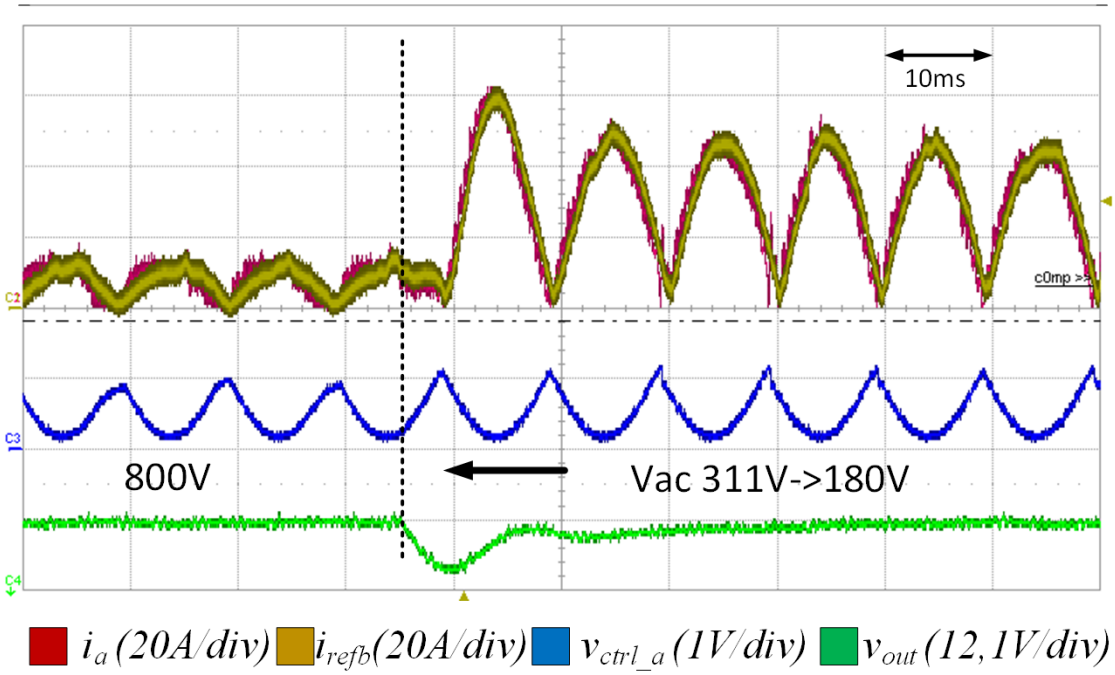


Figure 5.32: Current Control in HIL voltage drop test

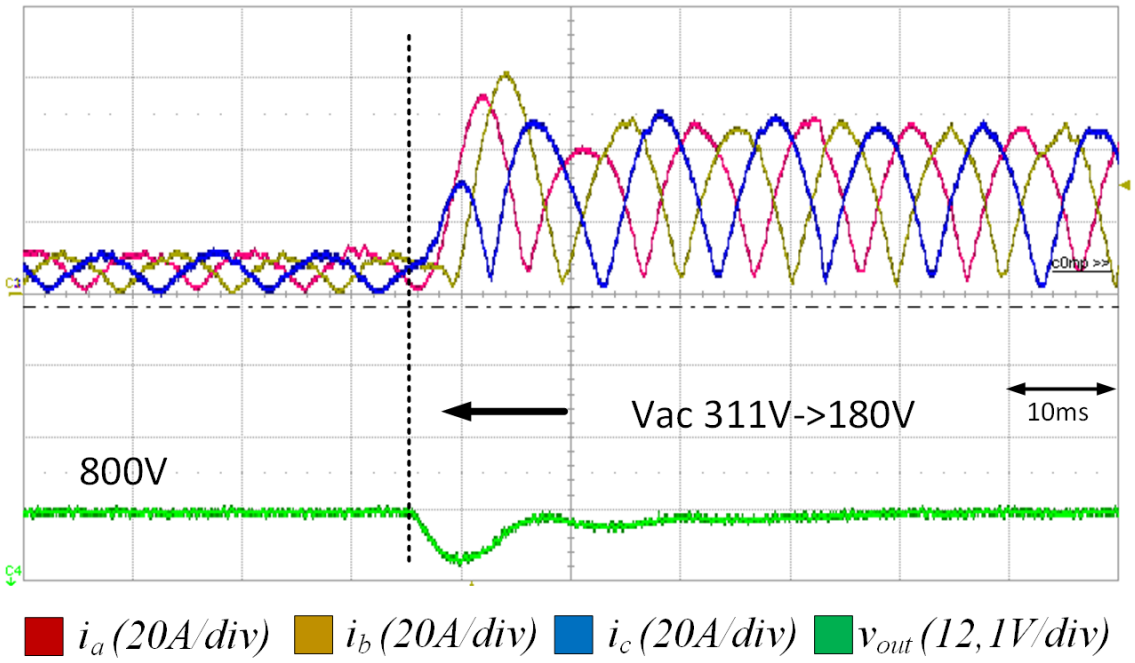


Figure 5.33: HIL voltage drop test

5.9.2 Real-Time Emulation of Induction Machines for Hardware in the Loop Applications

A FPGA-based dynamic model of three-phase induction machines is presented in this work. The model includes the effects of temperature in the stator and rotor resistances and of magnetic saturation in the magnetizing and leakage inductances, according to the stator and rotor currents. Moreover, iron core losses have been properly modeled. The proposed implementation ensures high accuracy of the simulations in a wide range of operating conditions, keeping a reasonable computational burden. Experimental tests confirm the good matching between the results provided by the hardware in the loop system and those coming from the experimental rig, the last including an electronic control unit used in automotive systems.

DYNAMIC MODEL OF THE INDUCTION MACHINE The dynamic model of the three-phase Induction Machine (IM) can be properly described by exploiting the generalized theory of electrical machines, [84, 85]. Basically, the traditional model of the induction machines in the *abc* reference frame is referred to an orthogonal arbitrary reference frame $qd0$ rotating at a generic angular speed ω. The stator and rotor voltages equations in the $qd0$ reference frame are (5.12) according Table.5.3, while the stator and rotor fluxes equations are given by (5.13) in which all the rotor quantities are referred to the stator and both magnetizing and leakage inductance are depending on the magnetizing current i_m (5.14)

$$
\begin{aligned}
v_{qs} &= R_s(T)\, i_{qs1} + p\lambda_{qs} + \omega\lambda_{ds} \\
v_{ds} &= R_s(T)\, i_{ds1} + p\lambda_{ds} - \omega\lambda_{qs} \\
v_{os} &= R_s(T)\, i_{0s1} + p\lambda_{0s} \\
v'_{qr} &= R'_r(T)\, i'_{qr} + p\lambda'_{qr} + (\omega - \omega_r)\, \lambda'_{dr} = 0 \\
v'_{dr} &= R'_r(T)\, i'_{dr} + p\lambda'_{dr} - (\omega - \omega_r)\, \lambda'_{qr} = 0 \\
v'_{0r} &= R'_r\,(T)\, i'_{0r} + p\lambda'_{0r} = 0
\end{aligned}
\tag{5.12}
$$

$p = d/dt$	*derivative operator*
$\omega - \omega_r$	*angular speed of the qd0 reference frame and rotor angular speed*
$v_{qs} - i_{qs} - \lambda_{qs}$	*q axis stator voltage, current and flux*
$v_{ds} - i_{ds} - \lambda_{ds}$	*d axis stator voltage, current and flux*
$v_{os} - i_{os} - \lambda_{os}$	*o axis stator voltage, current and flux*
$v_{qr} - i_{qr} - \lambda_{qr}$	*q axis rotor voltage, current and flux referred to the stator*
$v_{dr} - i_{dr} - \lambda_{dr}$	*d axis rotor voltage, current and flux referred to the stator*
$v_{or} - i_{or} - \lambda_{or}$	*o axis rotor voltage, current and flux referred to the stator*
$i_{qFe} - i_{dFe} - i_{oFe}$	*qd0 axes stator currents used in the modeling of iron losses*
$R_S - L_{ls}$	*stator resistance and leakage inductance*
$R_S - L_{ls}$	*rotor resistance and leakage inductance*
L_M	*magnetizing inductance*
R_{Fe}	*stator iron resistance*

Table 5.3: Induction machine nomenclature

$$
\begin{aligned}
\lambda_{qs} &= L_{ls}\,(i_m)\, i_{qs} + L_M\,(i_m)\left(i_{qs} + i'_{qr}\right) \\
\lambda_{ds} &= L_{ls}\,(i_m)\, i_{ds} + L_M\,(i_m)\,(i_{ds} + i'_{dr}) \\
\lambda_{0s} &= L_{ls}\,(i_m)\, i_{0s} \\
\lambda'_{qr} &= L'_{lr}\,(i_m)\, i'_{qr} + L_M\,(i_m)\left(i'_{qr} + i_{qs}\right) \\
\lambda'_{dr} &= L'_{lr}(i_m)\, i'_{dr} + L_M\,(i_m)\,(i'_{dr} + i_{ds}) \\
\lambda'_{0r} &= L'_{lr}(i_m)\, i'_{0r}
\end{aligned}
\tag{5.13}
$$

$$
i_m = \sqrt{\left(i_{qs} + i'_{qr}\right)^2 + \left(i_{ds} + i'_{dr}\right)^2} \tag{5.14}
$$

The nonlinear dependence of magnetizing inductance L_M, L_{ls}, L'_{lr} on the current im for the IM considered in this study, is shown in Fig.5.34,[86–89].

while the linear dependence of stator and rotor resistance R_S, R_R on the temperature T is shown in Fig.5.35.

The representation of iron losses in the IM model is a complicated task. In this study the stator iron losses are associated to that of an equivalent constant resistance R_{fe}, subjected to the difference between the power supply voltage and the stator resistance voltage drop, the last depending on the stator currents, [90],[91]. Hence, the considered IM model also includes the equations(5.15),(5.16).

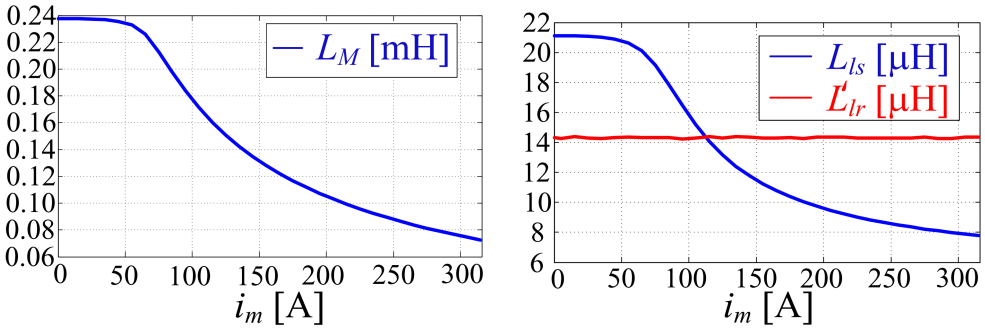


Figure 5.34: L_M , L_{ls} and L'_{lr} vs i_m for the considered IM.

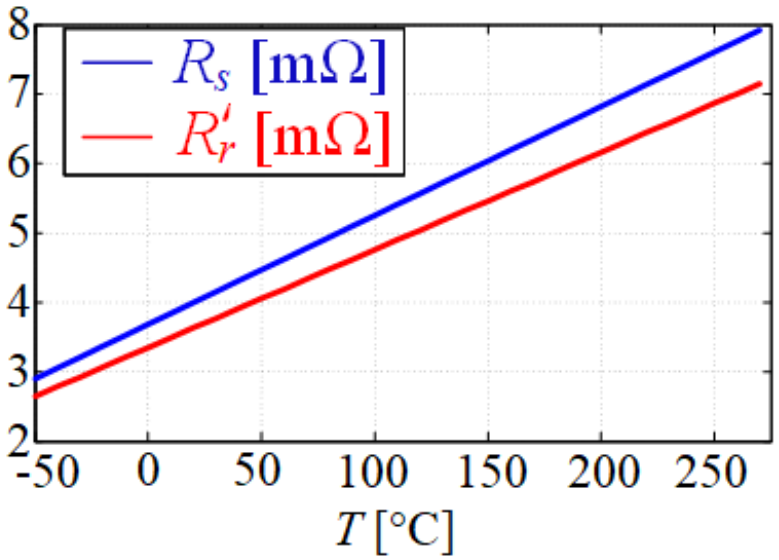


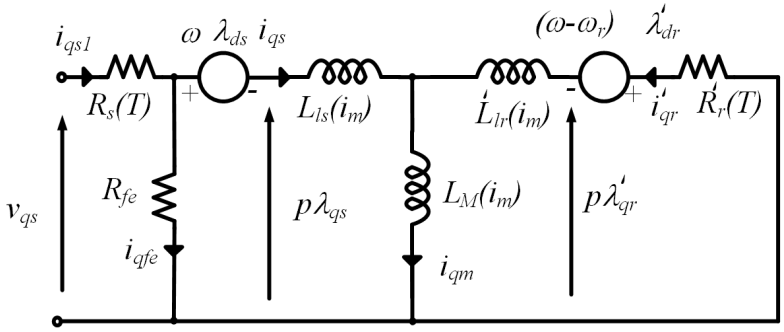
Figure 5.35: FPGA R_s and R'_r vs T for the considered IM

$$\begin{cases} R_{fe} i_{qfe} = p\lambda_{qs} + \omega\lambda_{ds} \\ R_{fe} i_{dfe} = p\lambda_{ds} - \omega\lambda_{qs} \\ R_{fe} i_{0fe} = p\lambda_{0s} \end{cases} \tag{5.15}$$

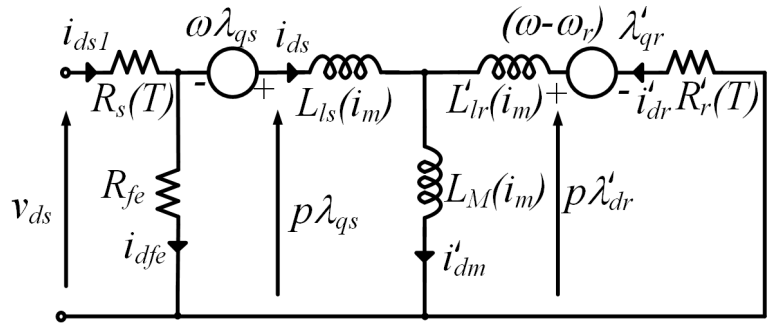
$$\begin{cases} i_{qs1} = i_{qs} + i_{qfe} \\ i_{ds1} = i_{ds} + i_{dfe} \\ i_{0s1} = i_{0s} + i_{0fe} \end{cases} \tag{5.16}$$

The equivalent circuital representation of the dynamic IM model in the $qd0$ reference frame is shown in Fig.5.36, in which R_{Fe} is inserted in a transversal branch of the q and d axes circuits, beside the stator resistance.

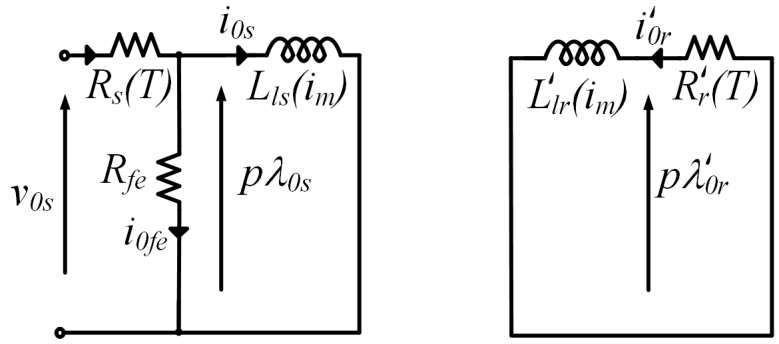
The electromagnetic torque expression in the $qd0$ reference frame is given by (5.17):



(a) axis q



(b) axis d



(c) axis o

Figure 5.36: Equivalent circuits of the induction machine model, including iron losses.

$$T_e = \frac{3}{2}\left(\frac{P}{2}\right)(\lambda_{ds} i_{qs} - \lambda_{qs} i_{ds}) \tag{5.17}$$

Finally, the Newton's law of rotational motion (5.18) describes the relationship between T_e, the load torque T_L, the inertia J and the frictions B of the mechanical system.

$$T_e = T_L + J\frac{d\omega_r}{dt} + B\omega_r \tag{5.18}$$

IMPLEMENTATION OF THE IM MODEL IN THE HARDWARE IN THE LOOP SYSTEM The IM model including iron losses, saturation effects and thermal behavior has been implemented on a Xilinx Integrated Synthesis Environment (ISE) Design Suite. The HIL is composed by the following electronic boards:

- DS1006[10] processor board with 4 core arm technology,
- DS2211[11] Central I/O board for hardware-in-the-loop simulation
- DS5203[12] FPGA Module based on Xilinx®technology

Each board has a specific function for real time model execution. DS1006[10] ($sampletime = 500ms$) manages DS5203[12]/DS2211[11] and executes slow model plant parts, for instance, thermals dynamics or Soft-ECU.

The DS2211[11] provides the electrical interface between the simulator and the control unit. The DS5203[12] ($sampletime = 10ns$) ensures high speed signal processing; for this reason, the power module, the electrical machines, resolver and current sensors are simulated by FPGA. The FPGA model has been developed by using Xilinx tool chain, that allows VHDL autocoding from simulink blockset. The structure of the HIL system setup is depicted in Fig.5.37; the principal technical specifications of the FPGA can be found in Table.5.4, while that of the emulated induction machine are listed in Table5.5. This IM is used as Belt Starter Generator (BSG)) for light duty hybrid vehicles. The IM model is executed at $Ts = 100ns$, while the maximum frequency of the electrical stator quantities is limited to $300Hz$. The aforementioned dynamic model has been initially realized in simulink and then converted in Xilinx blocks. The block diagram of the IM model in the FPGA-based HIL system is shown in Fig.5.38. Reference frame transformations blocks have been used to refer voltages and currents to the $qd0$ reference frame.

The variability of the magnetizing and leakage inductances as a function of the magnetizing current has been implemented on the Xilinx platform through the ports RAM. Since it is very difficult to calculate the square root function with the FPGA blocks, the inductive parameters have been related to the square of the magnetizing current. One Dimensional Look Up Table (LUT-1D) are used to relate each inductive parameter with

[10]The DS1006 Processor Board is based on a quad-core AMD Opteron™ x86 processor with 2.8 GHz clock frequency.

[11]The DS2211 HIL I/O Board is the central I/O board for hardware-in-the-loop simulation, especially in the field of automotive electronics.

[12]The DS5203 FPGA Board features the freely programmable Xilinx®Virtex-5 FPGA with ISE support or the powerful Xilinx Kintex®-7 with Vivado®support. In addition, the board offers 6 ADC, 6 DAC and 16 digital I/O channels.

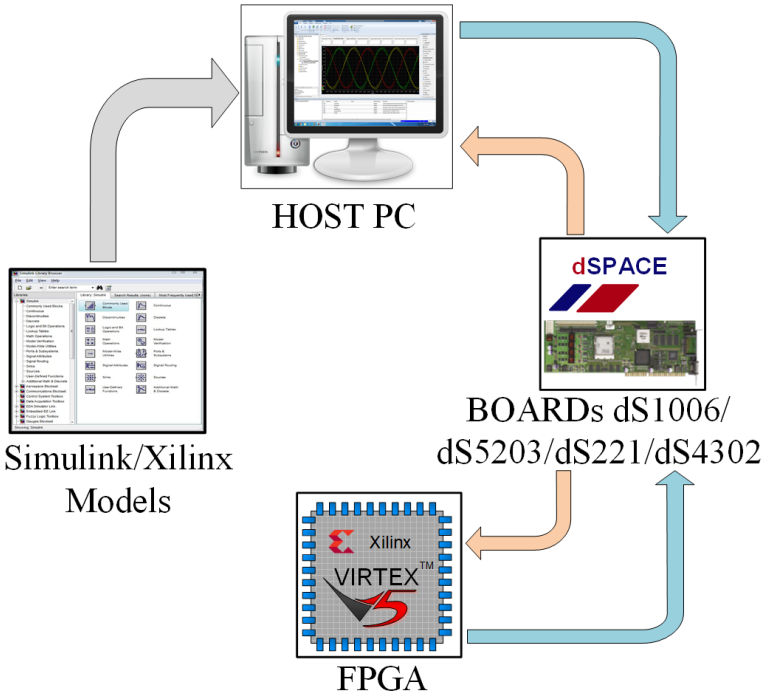


Figure 5.37: Hardware in the loop system setup.

Array row x col	120 x 30
Slices	7200
Max Distributed RAM	480 kb
Total I/O Banks	16 Digital channel usable as input or output 6 Analog input (15 V max range) 6 Analog output (15 V max range)

Table 5.4: Technical specifications of the Virtex-5 FPGA

the magnetizing current i_M. Moreover, the LUTs-1D associated to the inductive parameters are bounded by using lower and upper inductance limits. After having calculated the fluxes by (5.12), and as in Fig.5.39, the stator and rotor currents, calculated at each sampling time k, can be determined according to(5.19 e (5.20).

Electrical parameters	
R_s	4.79 mΩ
R'_r	4.34 mΩ
L_{ls}	14.1 µH
L'_{lr}	14.4 µH
L_M	0.16 mH
Mechanical parameters	
P	6 poles
J	8162 $kg \cdot mm2$
B	0.03 $kg \cdot mm2/s$
T_{max}	$30N \cdot m$
FPGA parameters	
f_{clock}	100 MHz
T_s	100 ns

Table 5.5: Technical specifications of the Induction Machine and Hardware In the Loop execution time

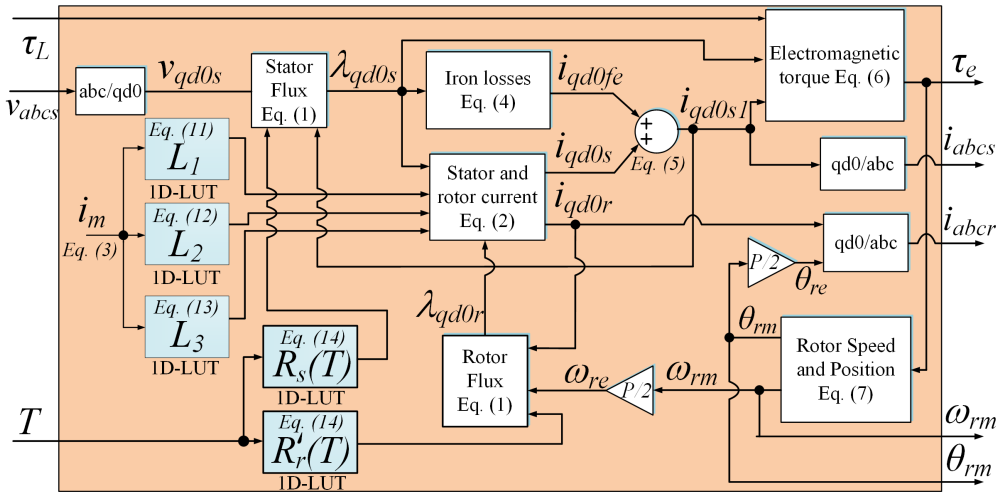


Figure 5.38: FPGA implementation of the IM model.

$$\begin{cases} i_{qs}(k) = \dfrac{\lambda_{qs} L_r(k) - \lambda_{qr} L_M(k)}{L_s(k) L_r(k) - L_M^2(k)} \\ i_{ds}(k) = \dfrac{\lambda_{ds} L_r(k) - \lambda_{dr} L_M(k)}{L_s(k) L_r(k) - L_M^2(k)} \\ i_{qr}(k) = \dfrac{\lambda_{qr} L_r(k) - \lambda_{qs} L_M(k)}{L_s(k) L_r(k) - L_M^2(k)} \\ i_{dr}(k) = \dfrac{\lambda_{dr} L_r(k) - \lambda_{ds} L_M(k)}{L_s(k) L_r(k) - L_M^2(k)} \end{cases} \tag{5.19}$$

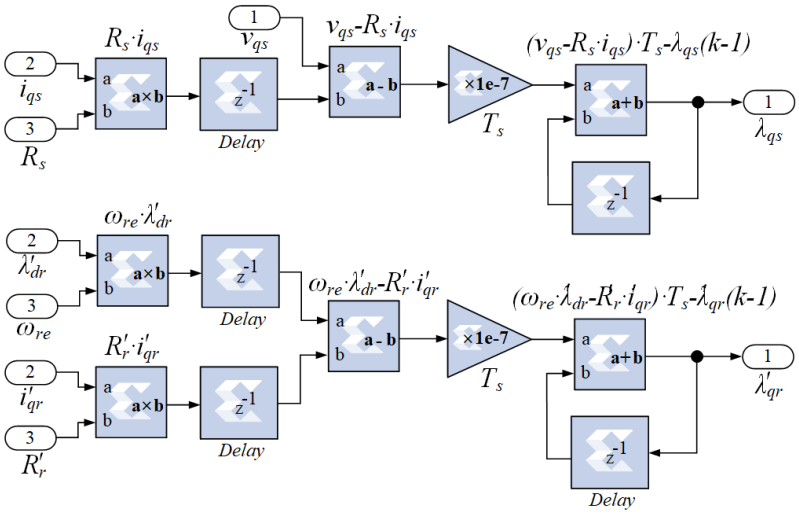


Figure 5.39: Xilinx block diagram of the implemented λ_{qs} and λ'_{qr} calculations

$$\begin{cases} L_s(k) = L_{ls} + L_M(k) \\ L_r(k) = L'_{lr} + L_M(k) \end{cases} \tag{5.20}$$

The implementation of the IM model in FPGA makes use of auxiliary quantities in order to keep low computational efforts. In particular, three auxiliary quantities are defined in (5.21),(5.22),(5.23).

$$\Gamma_1(k) = \frac{L_s(k)}{L_s(k) L_r(k) - L_M^2(k)} \tag{5.21}$$

$$\Gamma_2(k) = \frac{L_r(k)}{L_s(k) L_r(k) - L_M^2(k)} \tag{5.22}$$

$$\Gamma_3(k) = \frac{L_M(k)}{L_s(k) L_r(k) - L_M^2(k)} \tag{5.23}$$

For the considered IM, the waveforms of Γ_1, Γ_2 and Γ_3 are shown in Fig.5.40. The saturation phenomenon has been implemented according to Fig.5.41, where Γ_1, Γ_2 and Γ_3 have been described as a functions of i_m. The RAM blocks have been realized discretizing the Γ_1, Γ_s and Γ_3 curves in 512 points, in order to carry out inductances values featuring 9 bit of resolution.

The vectors given in inputs to the RAM addresses have been scaled by a factor of 1000 to increase the resolution; the outputs are then multiplied by a factor of 1000. The calculated $\Gamma_1(i_m)$,$\Gamma_2(i_m)$ and $\Gamma_3(i_m)$are the address of the three RAMs exploited to implement the stator and rotor currents calculations in the $qd0$ reference frame.

The block diagram in Xilinx code of the i_{qs} and i'_{qr} calculations is shown in Fig.5.43. A similar implementation has been used for the calculation of ids and i'_{dr}.

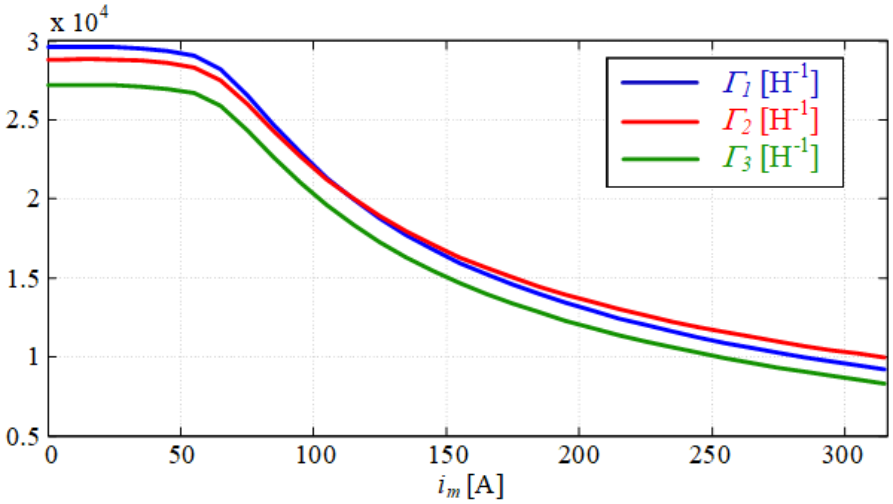


Figure 5.40: Γ_1, Γ_2 and Γ_3 vs i_m

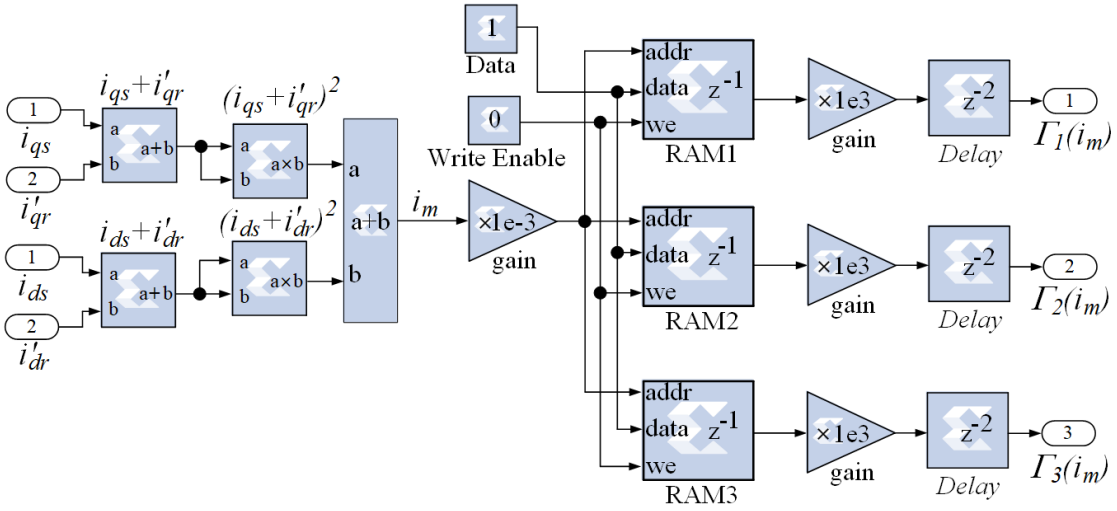


Figure 5.41: Xilinx block diagram of the implemented $\Gamma_1(i_m)$, $\Gamma_2(i_m)$ and $\Gamma_3(i_m)$

The fluxes are computed from the voltage equations. The block diagram in Xilinx code of the λ_{qs} and λ'_{qr} calculations is shown in Fig.5.39. The same structure is required for the λ_{ds} and λ'_{dr} evaluation.

The variations of the stator and rotor resistances with the operating temperature can be derived from the Finite Element Analysis (FEA) and it has been integrated in the proposed model by describing the thermal behavior of the IM exploiting the polynomial equation (5.24), [92], [93] where C is the heat capacity of the motor, T is the temperature, I_{rms} is the rms motor current amplitude and $k2$, $k1$, $k0$ are constant coefficients. The

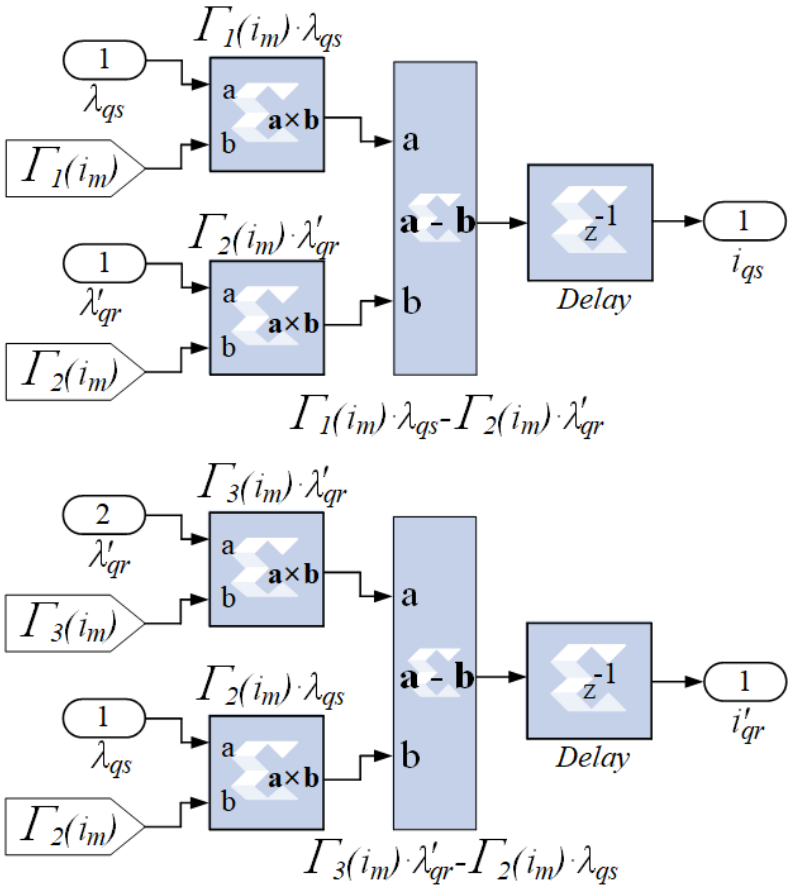


Figure 5.42: Xilinx block diagram of the implemented i_qs and i_qr calculations

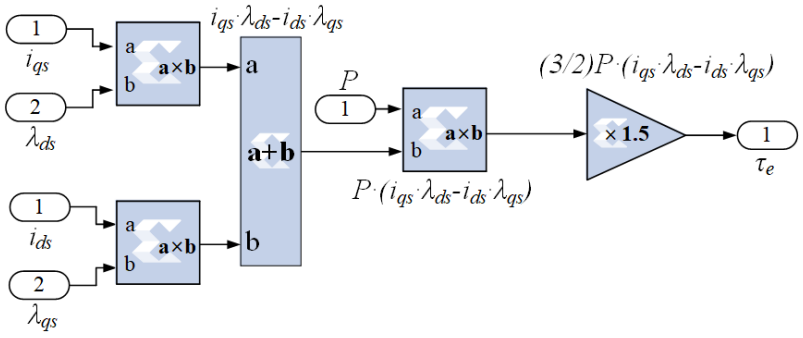


Figure 5.43: Xilinx block diagram of the implemented τ_e calculations

stator and rotor resistances variation with the temperature is implemented by using LUT-1D. The RAM blocks have been realized discretizing the $R_s(T)$ and $R'_r(T)$ curves in 512

points, in order to feature 9 bit of resolution in the output resistances values, Fig.5.44.

$$C\frac{dT}{dt} = k_2 I_{rms}^2 + k_1 I_{rms} + k_0 \tag{5.24}$$

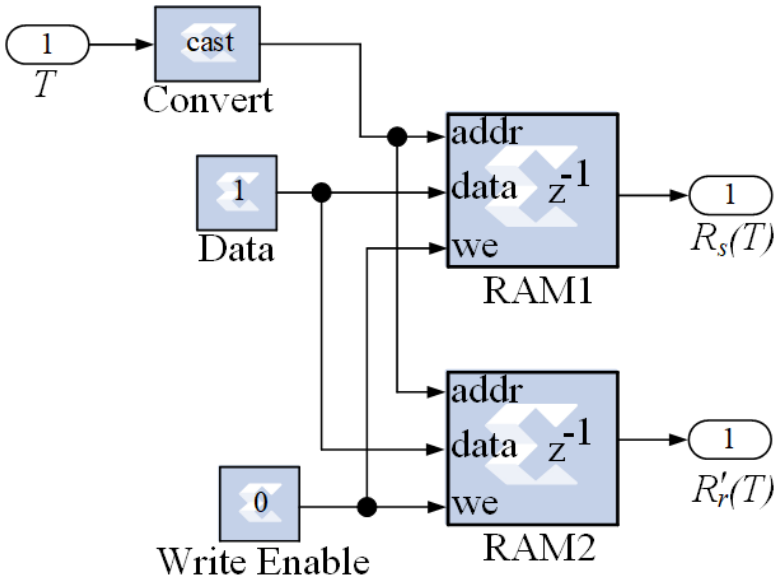


Figure 5.44: Block diagram of the stator and rotor resistance calculations

VALIDATION OF THE MODEL IMPLEMENTATION

- **Offline Simulations** Firstly, the proposed model has been evaluated by comparing a traditional model implementation in the block diagram environment simulink, and Xilinx blocks based implementation of the IM model. In both cases the model has been executed by setting a fixed-step discrete solver. The nameplate of the IM is the one reported in Table.5.5. A straightforward comparison of both implementation is shown in Fig.5.45 and Fig. 5.46; a direct-on-line motor starting is shown, in which the electrical and mechanical quantities carried out with both executions have been compared. It is worth noting that at each instant time the quantities carried out from both implementations are very nearly the same.

- **Experimental tests** The HIL solution has been also experimentally validated in the 15 kW BSG application, whose nameplate is the same considered for the previous simulations. The machine is supplied by a 20 kW three phase PWM inverter. The HIL system consists of a PCI eXtensions for Instrumentation (PXI) with the

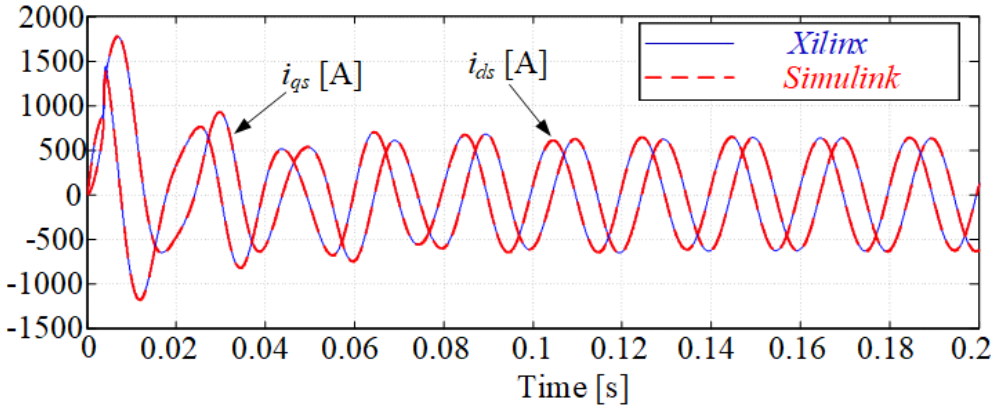
simulator real-time boards described in the previous paragraphs: [13]/[14]/[15]; a load-box is used as physical interface between the simulator and electronic control unit. The last contains electrical loads to replicate the real vehicle electrical conditions. A DC power supply is used to provide 13 V to the simulator, ECU and load-box. A host-PC is exploited to implement a simple user interface to impose the torque target to the ECU and analyze the closed loop system in real-time. The same HIL system implements the power converter, position and current sensors. A space vector modulation has been used to drive the IM,[94]. Fig.5.47 depicts the HIL solution while the experimental test rig is shown in Fig. 5.48. The tested motor is mechanically linked to an IM drive controlled by a field oriented control algorithm. The last drive is used to impose the rotational speed profile of the emulated mechanical system. Fig.5.49 shows the experimental results obtained by operating the BSG under a torque control. In particular, a reference torque profile is imposed to the tested IM drive at a constant rotational speed $\omega_{rm} = 6000\,\text{rpm}$ and the torque T_e is measured. Moreover, same torque profile and control algorithm have been interfaced to the HIL system in which the proposed implementation of the IM is executed. By looking at Fig.5.49 it is clearly visible a good agreement between the experimental results and that obtained by the HIL, in terms of rotational speed ω_{rm}, amplitude of the motor phase current I and torque T_e, fully satisfying the requirements in terms of accuracy of the control applications.

In the work, an accurate implementation of a FPGA-based dynamic model of three-phase induction machines is presented including the magnetic saturation and temperature effects on the parameters values of the model. The simulations and experimental tests confirm the effectiveness of the proposed HIL system. With regards to the computational burden, the model has been successfully performed at $T_s = 10ns$, in parallel to the execution of the analytical models associated to the power converter, rotor position and current sensors.

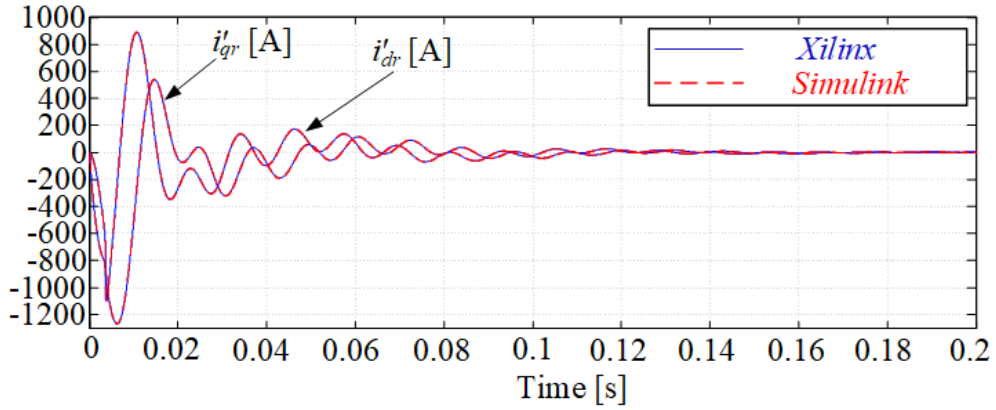
[13]The DS5203 FPGA Board features the freely programmable Xilinx®Virtex-5 FPGA with ISE support or the powerful Xilinx Kintex®-7 with Vivado®support. In addition, the board offers 6 ADC, 6 DAC and 16 digital I/O channels.

[14]The DS1006 Processor Board is based on a quad-core AMD Opteron™ x86 processor with 2.8 GHz clock frequency.

[15]The DS2211 HIL I/O Board is the central I/O board for hardware-in-the-loop simulation, especially in the field of automotive electronics.

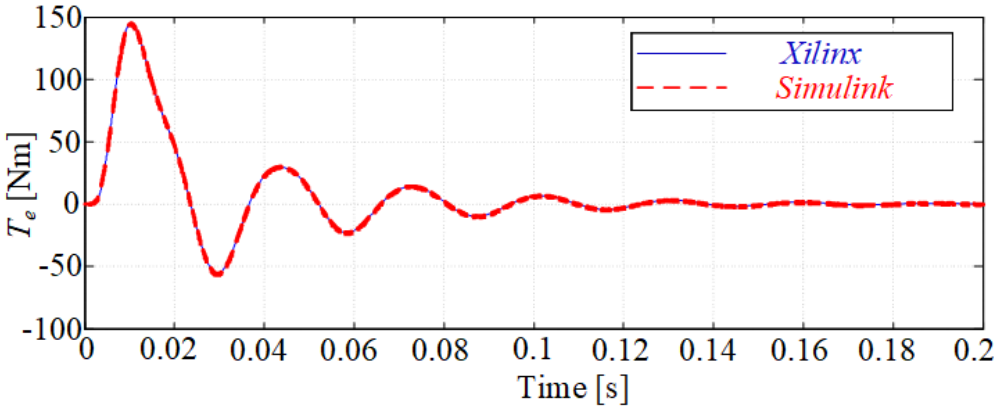


(a) i_{ds},i_{ds}

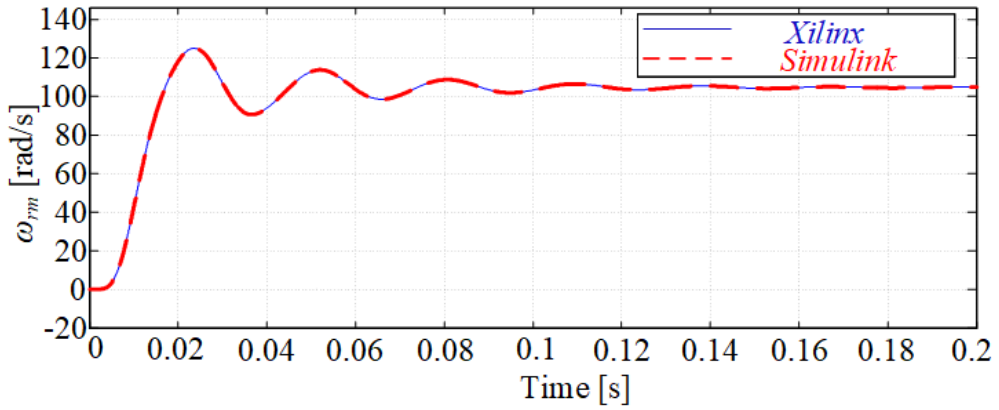


(b) i'_{dr},i'_{dr}

Figure 5.45: Comparison between the quantities waveforms obtained by the Xilinx and Simulink based blocks implementations.



(a) T_e



(b) $\omega_r m$

Figure 5.46: Comparison between the mechanical quantities waveform obtained by the Xilinx and Simulink based blocks implementations.

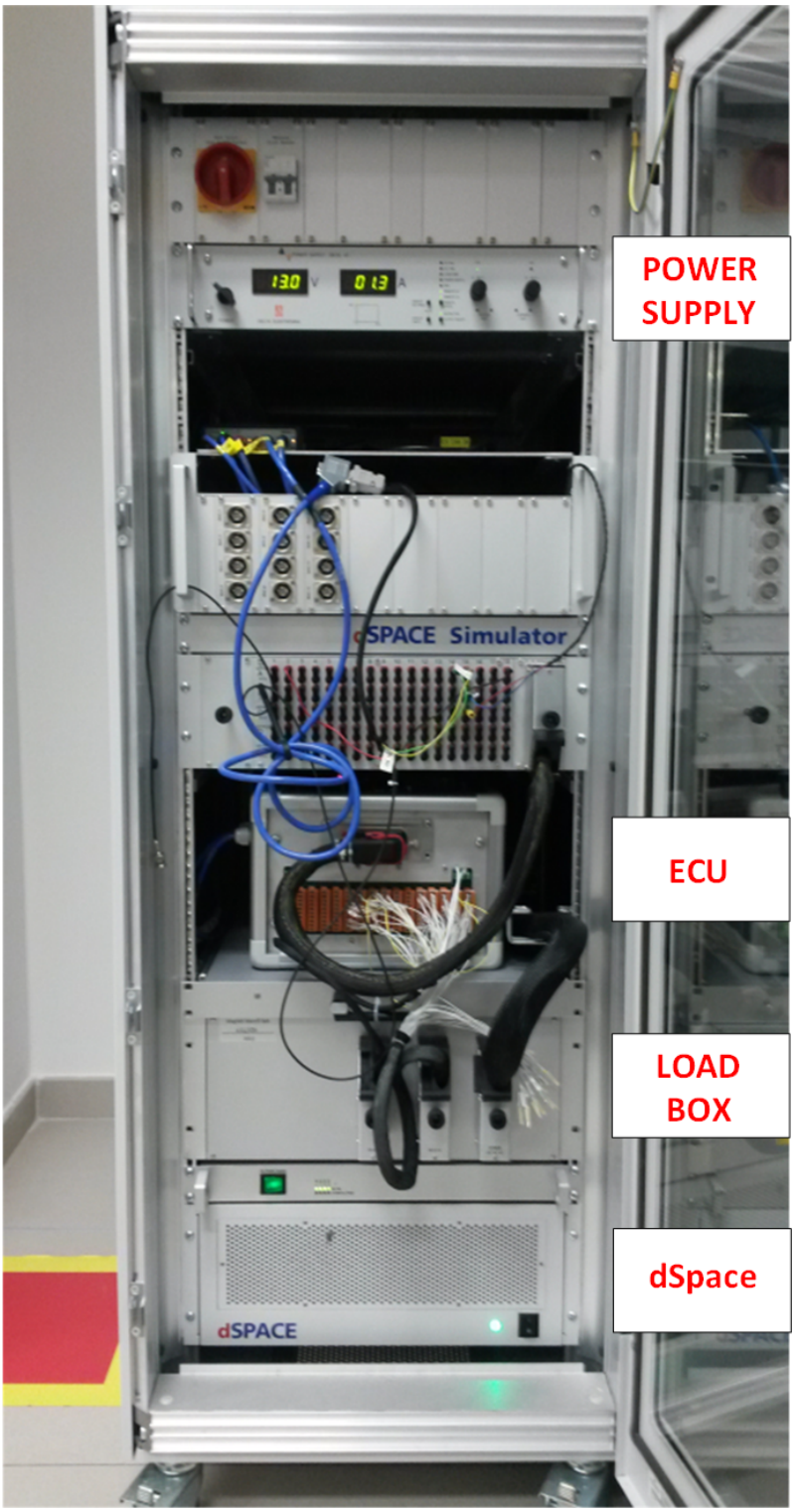


Figure 5.47: HIL solution built for testing a starter-alternator application

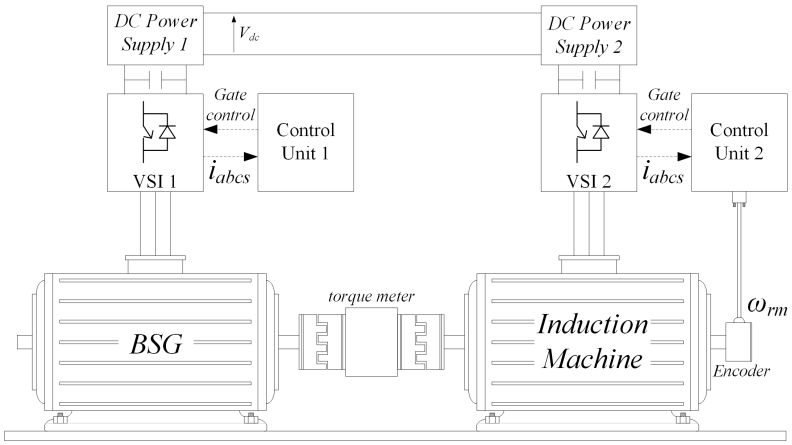
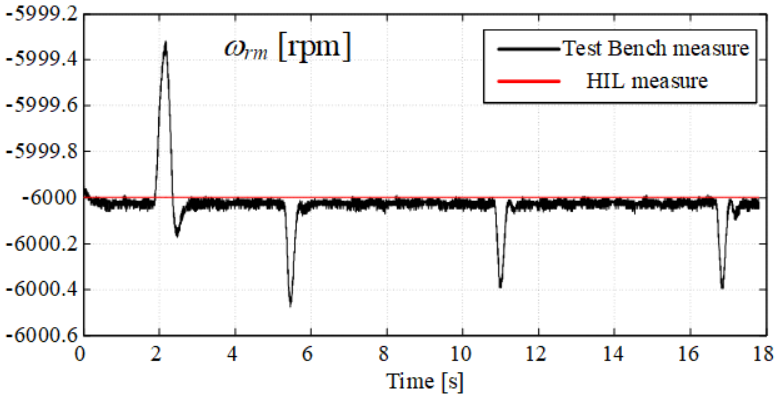
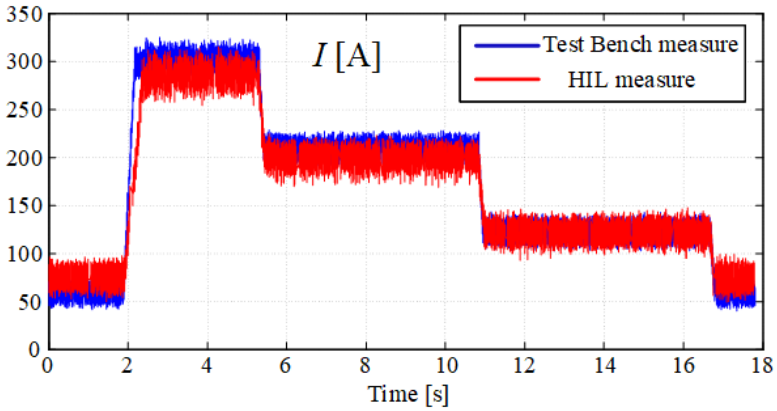


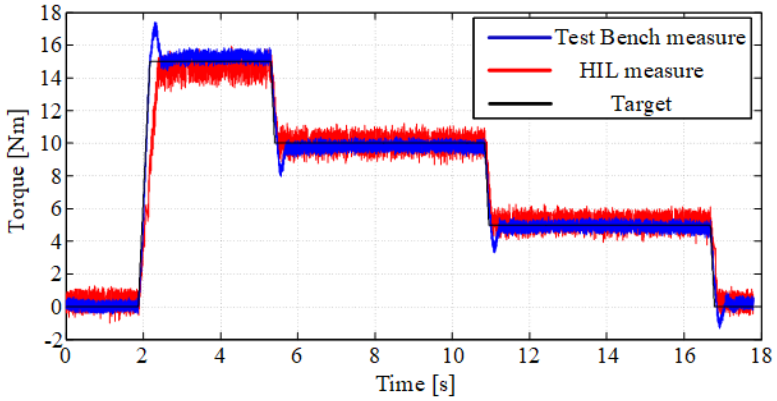
Figure 5.48: Experimental test rig



(a) ω_{rm}



(b) *Current*



(c) *Torque*

Figure 5.49: Comparison between the results achieved by the experimental tests and that carried out by the HIL system.

5.9.3 FPGA-Based Design and Implementation of a Real Time Simulator of Switched Reluctance Motor Drives

A Switched Reluctance Motor (SRM) drive has been described in detail and emulated by exploiting a FPGA-based HIL simulator with the aim to test the vehicle control strategies developed in the ECU. Switched reluctance motor is considered a good candidate for the next generation of Hybrid-Electric Vehicle (HEV) as this electrical machine features various advantages, such as simple structure, low cost, rotor robustness, possibility to operate at high temperatures and at high rotational speeds. Moreover, the SRM is a rare-earth-free-motor and thus it is not subjected to the high price and the supply variability of rare earth materials [95]. The analytical model of the SRM, as well as the pulse width modulator and power converter have been realized by the HIL simulator, providing the hardware inputs and outputs necessary to the implementation of the current and speed control loops. Moreover, the nonlinearities due to B-H characteristics of the magnetic material and the dependence of phase flux linkages on both the rotor position and current magnitude have been included in the modeling of the motor. The proposed implementation can be considered a good trade-off between accurate modeling, computing resources and time of simulation. This modeling solution is aimed at testing and evaluating control algorithms for SRM drives. Moreover, the proposed FPGA-based implementation of the SRM drives is easily adaptable for evaluating a wide variety of different motor configurations, power converter designs and control strategies.

Switched Reluctance Motor Drive Model

Switched Reluctance Machine Model Since the mutual inductance between the phase windings of the SRM machine is very small, in the following analysis it is assumed that the mutual coupling between the phases of the SRM stator is negligible, [95],[96]. The voltage v_h measured at the terminals of each h-motor phase (with $h = a, b, c, d$) is given by the sum of two contributions: the voltage drop on the motor phase resistance R_s and the rate of the flux linkages λ_h, where the magnetic flux λ_h is expressed according to (5.26), as the product of the motor phase currents ih and inductance L_s; the last parameter can be expressed as a function of the rotor position of h-phase θ_h, defined by mod operator according to (5.29), and current i_h. Substituting (5.26) in (5.25) the voltage v_h can be written as (5.27):

$$v_h = R_s i_h + \frac{d\lambda_h(\theta_h, i_h)}{dt} \tag{5.25}$$

$$\lambda_h = L_S(\theta_h, i_h) i_h \tag{5.26}$$

$$v_h = R_s i_h + L_S(\theta_h, i_h)\frac{di_h}{dt} + \frac{dL_S(\theta_h, i_h)}{d\theta_h}\frac{d\theta_h}{dt} i_h \tag{5.27}$$

$$E_h = K_b \omega_{rm} i_h \tag{5.28}$$

$$\theta_h = \theta_{rm} mod \left(\frac{2\pi}{p_r}\right) \tag{5.29}$$

$$K_b = \frac{dL_S(\theta_h, i_h)}{d\theta_h} \tag{5.30}$$

$$v_h = R_s i_h + L_S(\theta_h, i_h)\frac{di_h}{dt} + E_h \tag{5.31}$$

The last addend of (5.27) represents the induced Electromotive Force (EMF) E_h, (5.28), where w_{rm} is the angular speed (5.34), pr is the number of rotor poles, K_b can be considered equivalent to an EMF constant related to the inductance variation. Substituting (5.28), (5.29).(5.30) in (5.27) we get the final expression of the motor phase model, (5.31). The nonlinearities due to $B - H$ characteristics of the magnetic material and the dependence of phase flux linkages on both the rotor position and current magnitude have been included in L_S. The equivalent electric circuit of the single motor phase winding of the SRM (Fig.5.50) is shown in Fig.5.51.

$$T_{eh} = i_h^2 \frac{\partial L_S(\theta_h, i_h)}{\partial \theta_h} \tag{5.32}$$

$$T_e = \sum_{h=1}^{n} T_{eh} \tag{5.33}$$

$$\begin{cases} T_e = T : L + J\dfrac{d\omega_{rm}}{dt} + F\omega_{rm} \\ \omega_{rm} = \dfrac{d\theta rm}{dt} \end{cases} \tag{5.34}$$

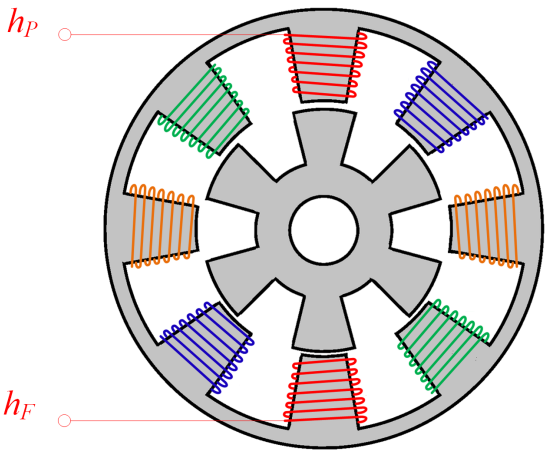


Figure 5.50: 8/6 Switched Reluctance Motor

The electromagnetic torque provided by the single motor phase winding of the SRM is given by (5.32), while the total electromagnetic torque is obtained as the sum of the

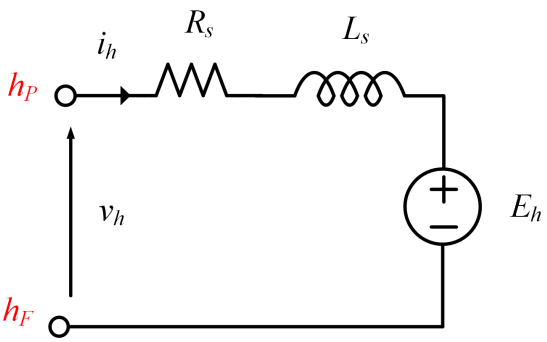


Figure 5.51: Equivalent circuit of the single motor phase

electromagnetic torques generated by each motor winding (5.30). Finally, the Newton's law describing the mechanical system is given by (5.34).

PWM Modulator and Power Converter Models H-bridges inverters have been employed to drive the SRM phases, Fig. 5.52, whose output voltages are determined combining the implementation of a standard bipolar PWM technique and assuming that the power converters consist of ideal devices according to (5.35).

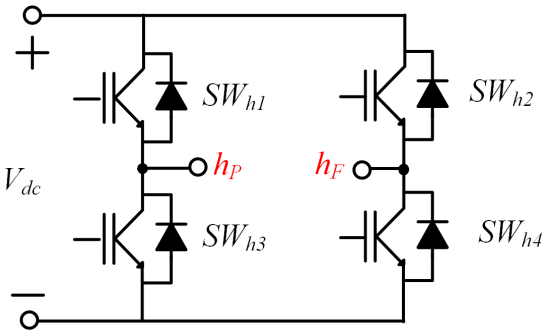


Figure 5.52: Equivalent circuit of the converter used to drive the SRM.

$$\begin{cases} v_h = V_D C \quad if \quad SW_{h1} = SW_{h4} = ON \quad \& \quad SW_{h2} = SW_{h3} = OFF \\ v_h = -V_D C \quad if \quad SW_{h1} = SW_{h4} = OFF \quad \& \quad SW_{h2} = SW_{h3} = ON \end{cases} \tag{5.35}$$

Hardware In The Loop Simulation Technique

hardware in the loop workbench The HIL test bench is composed by the following dSPACE®electronic boards: DS1006[16], DS2211[17], DS5203[18]. Each board has a specific function for real time model execution. DS1006[16] (sample time = 50 µs) manages DS5203[18]/DS2211[17] and executes the current and speed control algorithms that will be implemented in the ECU. The DS2211[17] provides the electrical interface between the simulator and the control unit. The board DS5203[18] (FPGA clock period = 10 ns) ensures high speed signal processing, allowing to properly emulate the power module and the electrical machines, by exploiting the parallelism and pipe-lining capabilities of the FPGA. The FPGA model has been developed by using Xilinx tool chain, that allows VHDL autocoding from simulink blocksets. In particular, the implementation of the SRM, PWM modulator and power converter has been realized by using the Matlab/Simulink – Xilinx ISE.

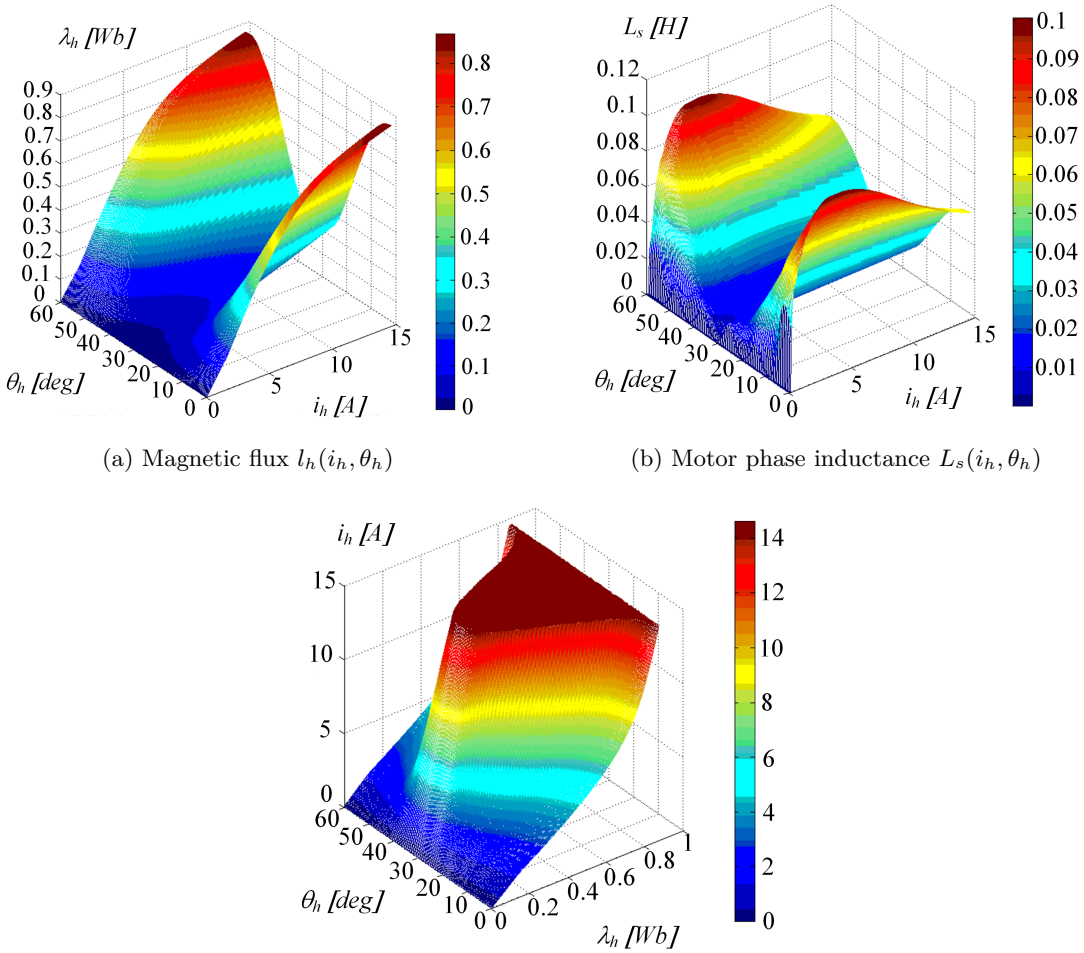
Flux linkage and current profiles measurement Among the various methods presented in literature [96],[97],[98],[99], the flux linkage and current profiles have been determined measuring the transient current responses when step voltages are applied to the SRM phases through a DC power supply. The tests have been executed at locked shaft, for different voltages and rotor angle positions; the flux-linkage surfaces $\lambda_h(i_h, \theta_h)$ and $L_S(i_h, \theta_h)$ have been computed by applying (5.29) and (5.29) to the experimental measures and the obtained values stored in Two Dimensional Look Up Table (LUT-2D). Fig.5.53 shows the post processing results for a SRM whose technical specifications are listed in Table.5.6. The inverse characteristic $i_h(l_h, q_h)$ is then computed and used in the SRM model. The electromagnetic torque provided by each motor phase is obtained through an appropriate processing of the surface $L_S(i_h, \theta_h)$ shown in Fig.5.53. In particular, the surface $\dfrac{\partial L_S(i_h, \theta_h)}{\partial \theta_h}$ has been firstly computed from $L_S(i_h, \theta_h)$ and then used in (5.32) to calculate $T_e(i_h, \theta_h)$, Fig.5.54. The last surface has been used to directly compute the electromagnetic torque, starting from rotor position and motor phase currents.

SRM drive implementation on a Standard Model-Based design environment (SMB) The dynamic model of the SRM indicated in Table.5.6 I has been initially implemented in Simulink, a well-known graphical model-based design environment. A block diagram of the different parts composing the SRM model are shown in Fig.5.55, including through 2D-LUTs the nonlinearities due to magnetic saturation and the dependence of phase flux linkages on both the rotor position and current magnitude. The effects of

[16]The DS1006 Processor Board is based on a quad-core AMD Opteron™ x86 processor with 2.8 GHz clock frequency.

[17]The DS2211 HIL I/O Board is the central I/O board for hardware-in-the-loop simulation, especially in the field of automotive electronics.

[18]The DS5203 FPGA Board features the freely programmable Xilinx®Virtex-5 FPGA with ISE support or the powerful Xilinx Kintex®-7 with Vivado®support. In addition, the board offers 6 ADC, 6 DAC and 16 digital I/O channels.



(a) Magnetic flux $l_h(i_h, \theta_h)$

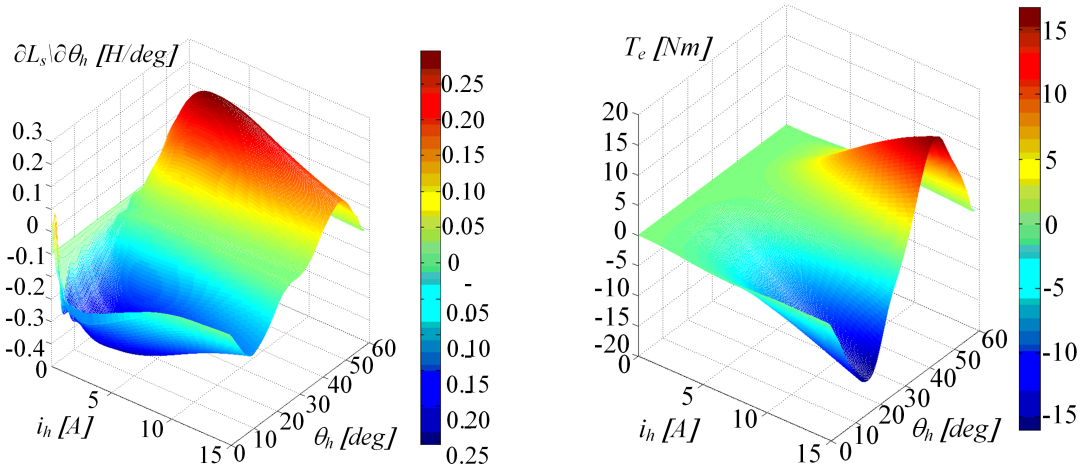
(b) Motor phase inductance $L_s(i_h, \theta_h)$

(c) Motor phase current $i_h(l_h, \theta_h)$

Figure 5.53: Post processing results.

V_{DC}	600 V
I_n	9 A
R_S	10 mΩ
p_S	$8 poles$
p_R	$6 poles$
J	0.0082 kgm^2
F	0.01 kgm^2/s
T_n	15 N m

Table 5.6: Technical specifications of the 8/6 SRM.



(a) Incremental inductance $\frac{\partial L_s(i_h,\theta_h)}{\partial \theta_h}$

(b) torque $T_e(i_h,\theta_h)$

Figure 5.54: Post processing mechanical results produced by each motor phase.

long cables connecting the motor and power converter have been neglected in this study, [100],[101]. The PWM modulated power converter has been implemented according to the relationships (5.35). Because of the switching frequency, $f_{sw} = 40\,\text{kHz}$, a satisfying level of accuracy has been achieved by setting the execution time $T_s = 100\,\text{ns}$, which significantly affects the time needed to complete the offline simulations. Moreover, significant memory requirements are necessary even for few seconds of simulation.

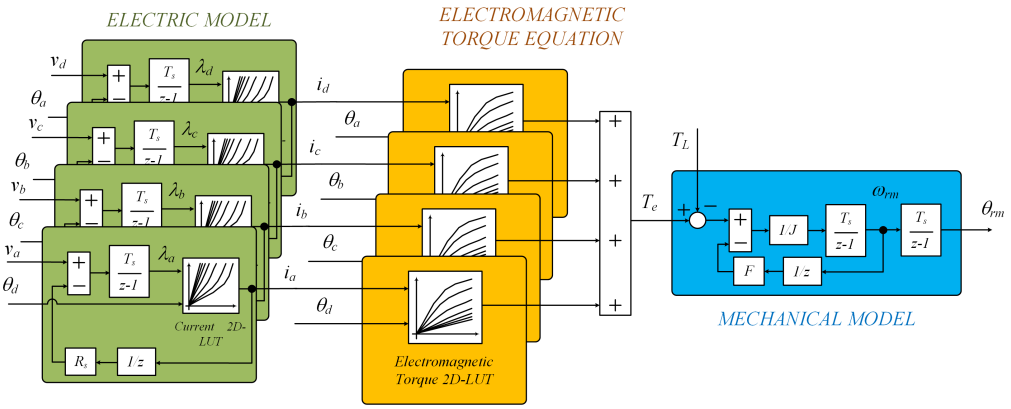


Figure 5.55: Block diagram of the 8/6 SRM model implementation in a generic model-based design enviroment

In order to maintain limited computational resources, the number of LUTs used in the Xilinx blockset implementation has been reduced avoiding the redundancies of Fig.5.55, thus yielding to a downsampling of the calculated quantities. In particular, a single LUTs

was sequentially used in the estimation of the flux, by implementing a multiplexing scheme, where the computation of (eqs. (5.25) to (5.32)) for each motor phase is performed sequentially, Fig.5.56. Similar approach has been used to compute the electromagnetic torque. Depending on the number of motor phases the effects of the downsampling (a few ns) can be considered negligible if compared to the electrical and mechanical time constants of the electromechanical system. The SRM model has been tested in a closed loop control as depicted in Fig.5.57, where the current (torque) loop is nested inside the speed loop in order to ensure good dynamic behavior. The Switch control signal generator is necessary to establish the optimal turn-on and turn-off angles. The control algorithm has been implemented in the processor side of the dSpace DS1006[19].

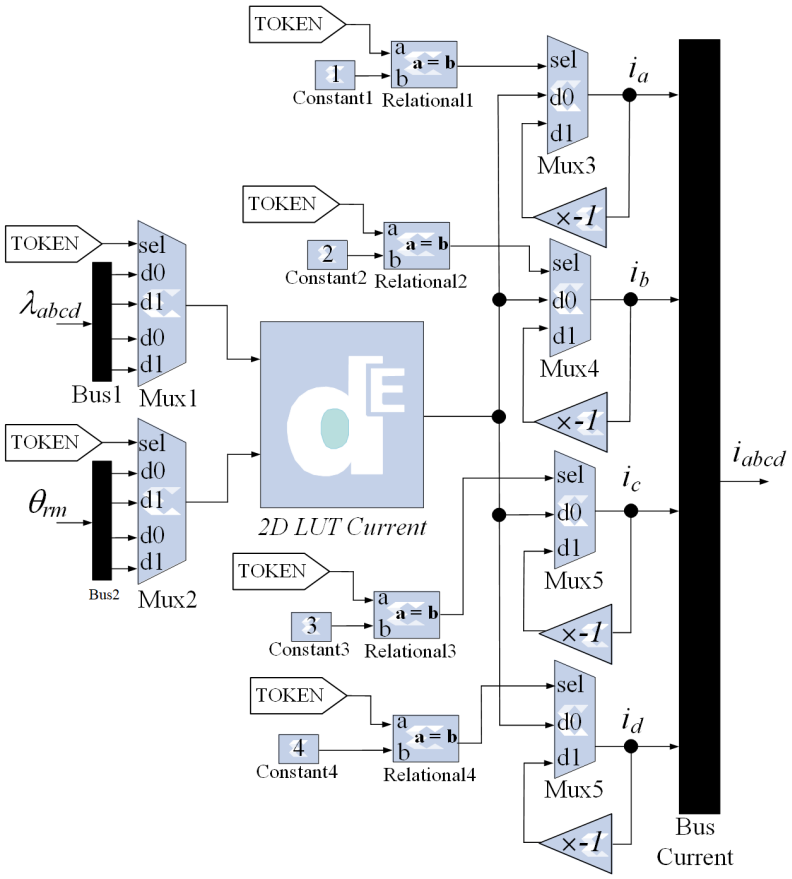


Figure 5.56: Implementation of optimized current calculation by exploiting a multiplexing approach.

Fig.5.58 shows the block diagram of the emulated position sensor, also implemented in

[19]The DS1006 Processor Board is based on a quad-core AMD Opteron™ x86 processor with 2.8 GHz clock frequency.

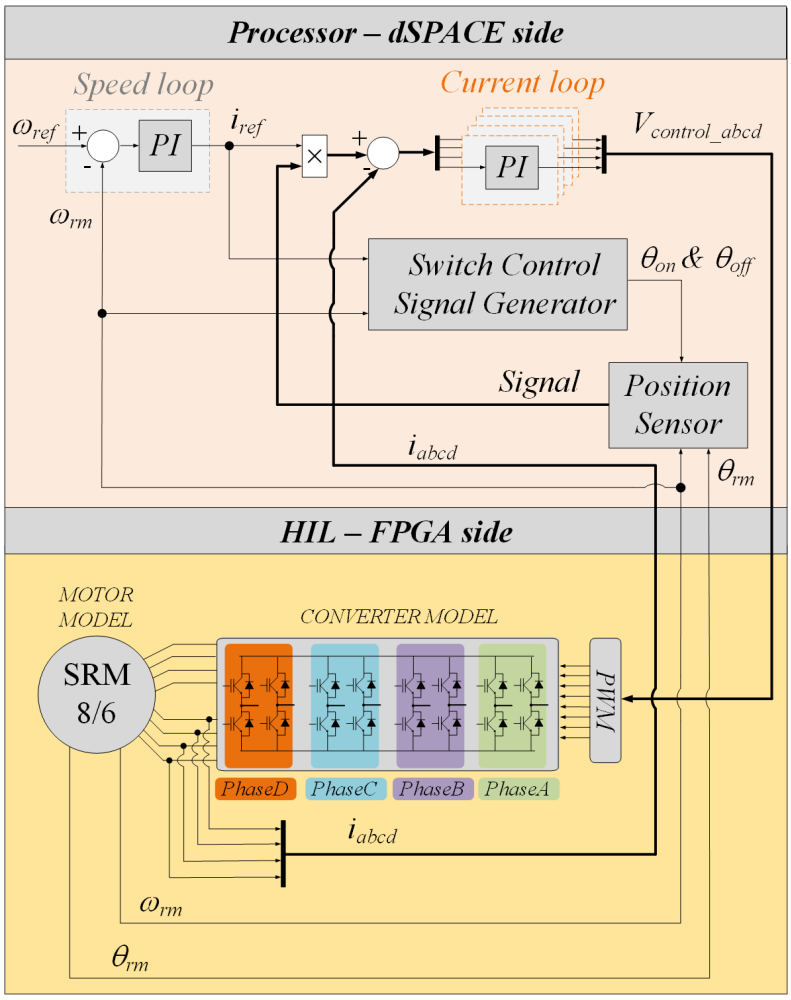


Figure 5.57: Block diagramm of the control algorithm.

the processor-dSPACE side, while Fig.5.59 displays the Xilinx-Block diagram of the PWM Modulator, implemented in the HIL-FPGA side, where the control signal of $h - phase$, $V_{control_h}$, is compared with a single triangular carrier signal at the frequency f_{sw}.

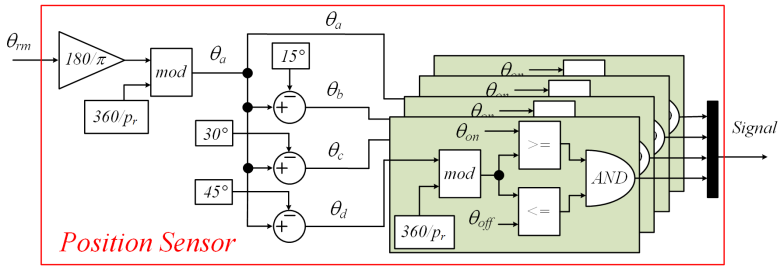


Figure 5.58: Simulink implementation of the activation signals of motor phases

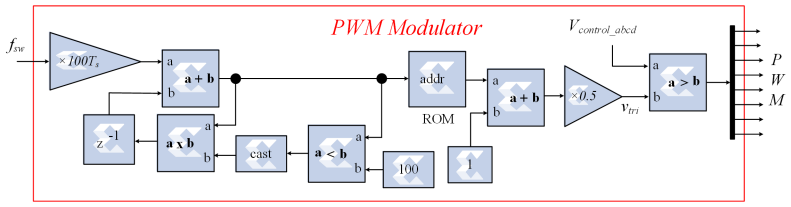


Figure 5.59: Xilinx block diagram of PWM Modulator

In order to maximize the output electromagnetic torque, each SRM phase is properly activated for an appropriate rotor position interval defined by a switch on θ_{on} and a switch off $theta_{off}$ angles, whose values are depending on the rotor speed and load conditions. In the following model validation, the switch on and switch off angles are established according to the maximum of $\frac{\partial L_s(i_h,\theta_h)}{\partial \theta_h}$. According to Fig.5.59, four activation angles have been calculated starting from the mechanical rotor whose phase shifts reflect their spatial position. The resultant signals are compared with the thresholds θ_{on} and $theta_{off}$. The signals outgoing from the *AND* operation represent the activation signals of the converters supplying the motor phases. Fig.5.60 displays the above mentioned signals associated to the phase current a. Similar command signals are obtained for the other phases, suitably phase shifted.

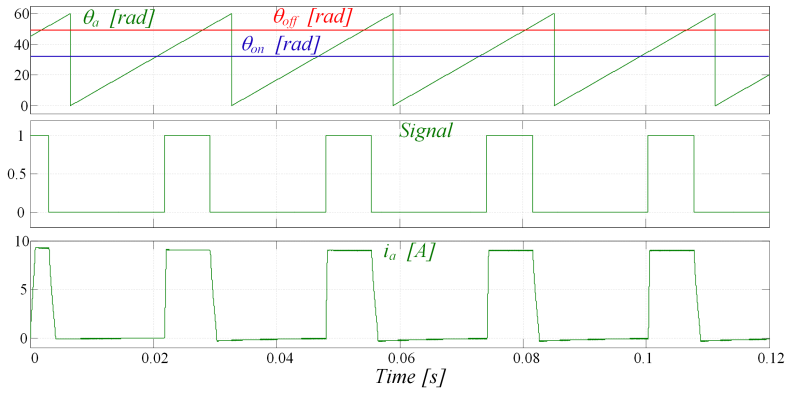


Figure 5.60: Activation commands associated to the phase a. Test conducted at constant speed $w_{rm} = 40rad/s$ and feeding each phase with a current of $i_h = 9A$

Hardware In The Loop Simulation Technique The effectiveness of the proposed Real Time Interface (RTI) modelling method has been initially evaluated through a sequence of transients applied to the SRM of Table.5.6. In particular, Fig.5.62 displays a sequence of startup followed by a transient load applied to the SRM drive. The bandwidth of the current and speed control loops are $BW_c = 250Hz$ and $BW_s = 30Hz$, respectively. The results confirm the accuracy provided by the simulation implemented in the FPGA-based HIL system. In fact, even during sudden transients very limited errors are

appreciable by comparing the results of the RTI compared to that coming from the Standard Model Based (SMB) implementation. The RTI modelling of the SRM has been also tested on two other SRM configurations: SRM6/4 and SRM10/8 whose block example (5.61)data configuration are given in Table.5.7. The results are displayed in Fig.5.63 and Fig.5.64. More specifically, the motor phase currents are shown for each motor configuration as well as the differences between the main quantities carried out by the SMB and RTI models. The motors are operated at even for the other SRMs, driven by the same power converter topology, a very good accuracy has been appreciated.

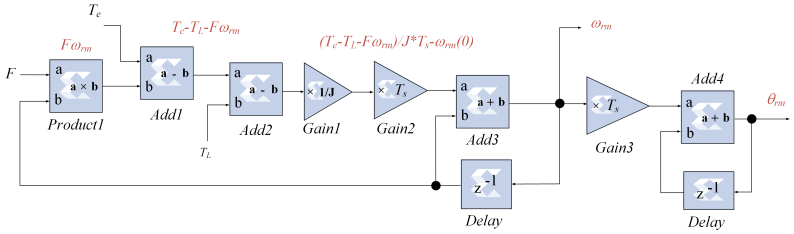


Figure 5.61: Xilinx Block Diagram used for the computation of the rotor position and mechanical speed.

Block	**Resolution**	
	Number of bits	**Binary Point**
Product1-Add1-Add2	32	16
Gain1-Gain2-Add3-Gain3	50	32
Gain4-Add4-Gain5	45	32

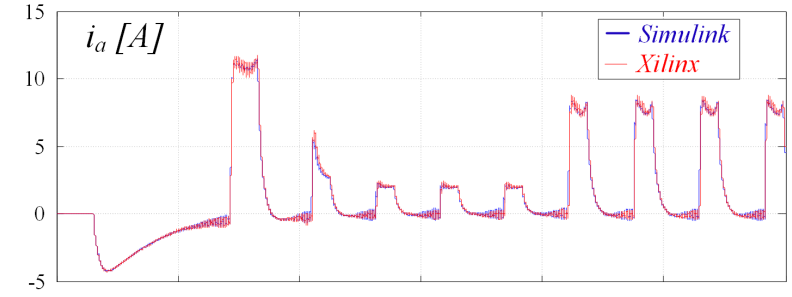
Table 5.7: FxP mechanical speed configuration

Hardware In The Loop Simulation Technique The performance of the HIL implementation have been evaluated by exploiting the timing analysis tool. The Table.5.8 summarizes the hardware FPGA resources and the latency; the last metric must be the minimal in order to avoid undesired control instability. Moreover, it is clearly visible from the available resources that additional dynamics can be included in the SRM drive model, such as the thermal model of the electrical machine.

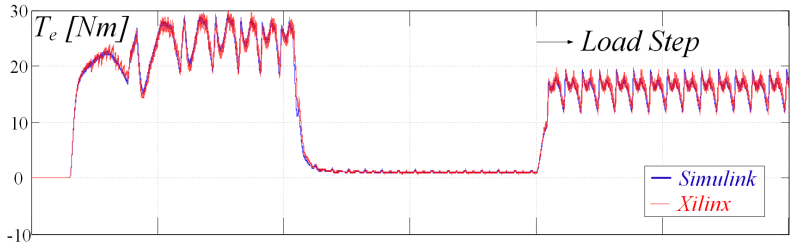
Conclusions The proposed modeling approach has been validated for different SRM configurations, and under steady state and transient conditions, allowing to obtain satisfactory results in terms of accuracy. It has been also verified that the realized models require a limited hardware FPGA resources and quite low latencies. This model can be easily exploited to verify the effectiveness of more sophisticated control strategies and power converters topologies devoted to SRM drives.

FPGA Utilization Summary			**Timing Analysis Report**		
Slice Logic Utilization	**Used**	**Available**	**Source**	**Destination**	**Path Delay**
Number of Slice Registers	6138	28800	V_abcd	Electromagnetic Torque	12.36 ns
Number of Slice LUTs	8176	28800	V_abcd	Mechanical Speed	9.96 ns
Number of BlockRAM/FIFO	59	60	Load Torque	Electromagnetic Torque	2.143 ns
Total Memory used (KB)	2070	2160	Load Torque	Mechanical Speed	2.543 ns

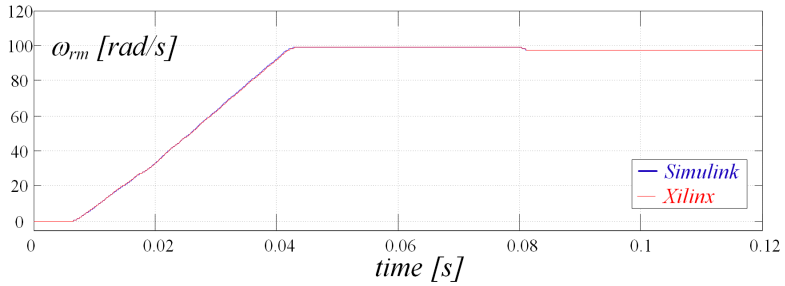
Table 5.8: FPGA Utilization Summary



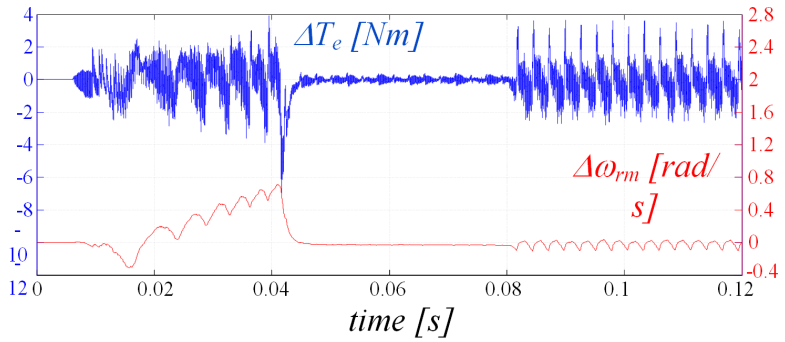
(a) Current Phase



(b) Electromagnetic Torque

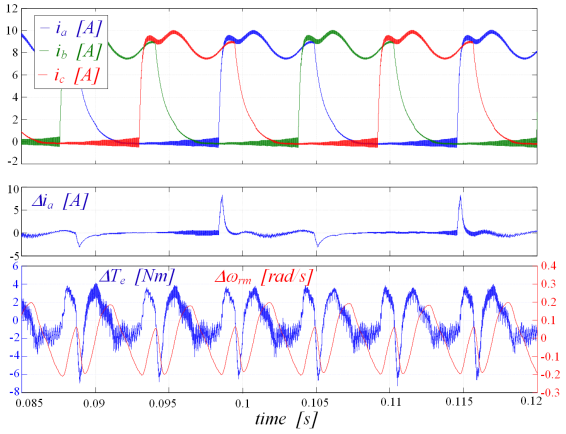


(c) Rotor speed

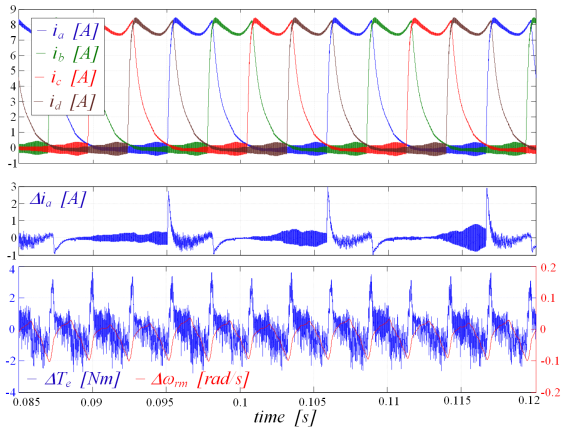


(d) Error

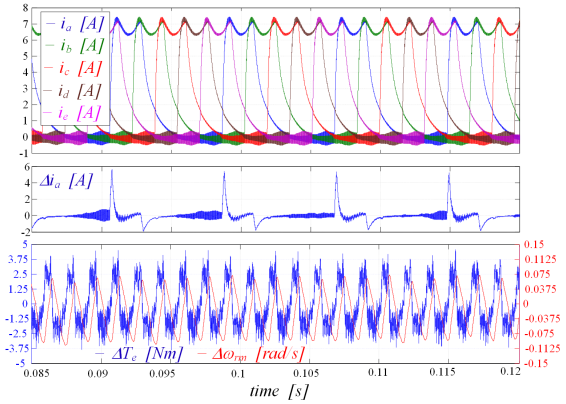
Figure 5.62: Comparisons between RTI and SMB. Speed transient speed from $\omega_{rm} = 0rad/sec$ to $\omega_{rm} = 100rad/sec$ followed by a step load from $T_L = 0Nm$ to $T_L = 15Nm$.



(a) SRM 6/4



(b) SRM 8/6



(c) SRM 10/8

Figure 5.63: Comparisons between SMB and RTI results for different configurations of Switched Reluctance Motors, in steady state conditions $\omega_{rm} = 100rad/s$ and $T_L = 15Nm$.

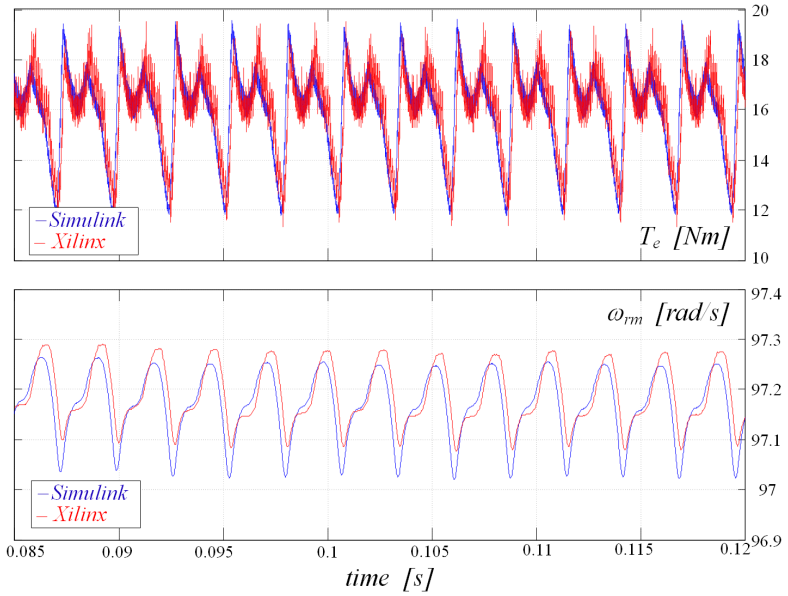


Figure 5.64: Comparisons between Simulink and Xilinx implementations in case of SRM 8/6: electromagnetic torque and mechanical speed

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Chapter 6

Multi-objective Optimization

In the past 20 years, evolutionary multi-objective optimization has become a popular and useful field of research and application. Power electronic circuits are complex systems, many different parameters and objectives have to be taken into account during the design process. Implementation of multi-objective optimization seems to be attractive idea, which used as designer supporting tool gives possibility for better analysis of the designed system.

This work has been focused on the study of genetic algorithms applied to a Vienna rectifier for multi-objective optimization. The scope is to find the values of inductor and capacitance that minimize the size and therefore the cost of the components and that meet certain constraints like the current ripple and the voltage ripple.

6.1 Multi objective optimization and genetic algorithms

In the real word, there are many optimization problems which involve multiple objective functions which must be satisfied simultaneously. They are called multi-objective optimization problems and usually their objectives are in conflict with each other[102]. Considering a single-objective optimization, the problem is reduced to find the global maximum or minimum of a function. However, when it comes to multi-objective optimization, the functions can be different and, in most cases, go against each other.

A characteristic example is the size of the passive components when the value varies: an inductor of 700 µH will be larger than one of 200 µH with the same ferromagnetic material and conductor section. The first inductor will therefore be ideal for application that want to reduce the current ripple in a DC-DC boost converter but it will involve a volume and therefore a greater cost. On the other hand the second inductor will be cheaper and lighter but will result in a greater current ripple. For each problem to be solved, a specific function must be built, called the Fitness function or objective function, which represents the measure of the validity of the solution with respect to the problem.

In this scenario genetic algorithms have begun to take hold thanks to different characteristics:

- Do not require any derivative information.

- Relatively simple to implement.
- Flexible and have a wide-spread applicability.

6.1.1 Genetic algorithm

The basic principles of Genetic Algorithms were first highlighted by Holland in 1975 [103]. A genetic algorithm is a heuristic optimization method inspired by natural selection and the biological evolution of species. During the execution the algorithm iteratively modifies an initial population called chromosome to obtain one that satisfies the requests. Mathematically these are composed of $X = [x_1, x_2, x_3 \cdots x_n]$ a variables vector corresponding to the function input $F(X)$

According to the classical principles of natural evolution, each individual transmits part of his genetic heritage to the following generations and also, sometimes, individuals are born with genetic variations with respect to the original species. The phases of the genetic algorithm can be divided mainly into three step: selection, crossing and mutation. In the first phase, after the initial parents have been chosen randomly, individuals to be reproduced are chosen who will transmit their genetic traits to subsequent generations. The respective fitness value is calculated and an appropriate arrangement of individuals is determined so as to choose the most promising individuals to become parents. After the choice, the second phase takes place in which the chosen parents are crossed among themselves to create the new generation, an offspring population, of the same number as the previous one. The innovative feature of genetic algorithms is the third phase, missing in the various evolutionary algorithms: the mutation phase. Indeed, a random variation is introduced to the offspring population which will therefore have a genetic heritage different from that of the parents. Here at the bottom a flow chart is added with the various steps representing the genetic algorithm.

- Step 1: Set $t = 1$ number of iterations. Randomly generate N solutions to form the first population P_1. Evaluate the fitness of solutions in P_1.
- Step 2: "Crossover" Generate an offspring population Q_t as follows.
  1. Choose two solutions x and y from P_t based on the fitness values.
  2. Using a crossover operator (Fig.6.1), generate offspring and add them to Q_t.
- Step 3: "Mutation" Mutate each solution $x \in Q_t$ with a predefined mutation rate (Fig 6.2)
- Step 4: "Fitness Assignment" Evaluate and assign a fitness value to each solution $x \in Q_t$ based its objective function value.
- Step 5: "Selection" Select N solutions from Q_t based on their fitness and assigned them to P_{t+1}.
- Step 6: If the stopping criterion is satisfied, terminate the search and return the current population, else, set $t = t + 1$ go to Step 2.

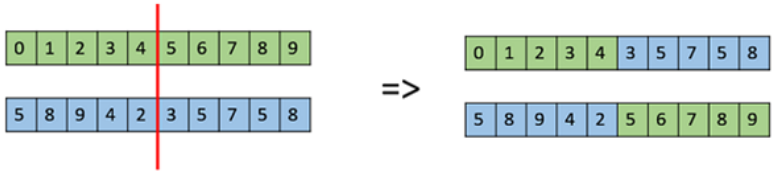


Figure 6.1: Crossover

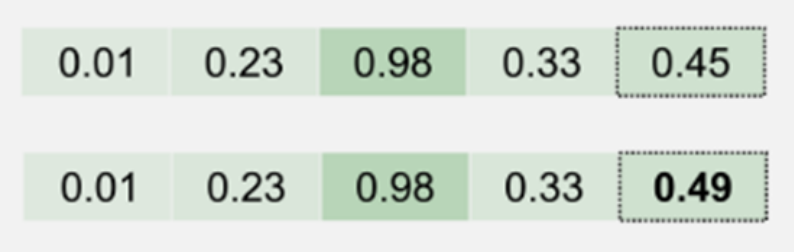


Figure 6.2: Mutation

Typical stop criteria can be: maximum number of iterations t, if the relative variation of the fitness function or of the variables is less than a tolerance value, maximum execution time etc. A well-known theorem, again due to Holland and called the schema theorem, ensures that, under certain hypotheses, individuals with high fitness values tend to grow exponentially in the population through the crossover mechanism, thus ensuring the convergence of the genetic algorithm towards an optimal solution. Moreover the proof of the schema theorem is based on the hypothesis of binary coding, but Wright (1991) extended it to the case of coding with real numbers; Wright himself has shown that a real number codification is to be preferred in the case of continuous optimization problems. However, due to complex non-linear interaction phenomena (epistaticity) between groups of values of a string representing an individual, the genetic crossover operation does not always produce acceptable results, and sometimes it happens that, starting from two extremely promising parents , get a decidedly less valid descendant. The algorithm used in this paper is the NSGA II [104], developed by Kalyanmoy Deb in 2000, and is the acronym of non-dominated sorting genetic algorithm, .This algorithm was created to solve the problems of the NSGA predecessor as the high computational complexity of non-dominated sorting that passes from $O(M * N^3)$ to $O(M * N^2)$ where M is the number of objectives and N is the size of the population. It also improves elitism because, unlike other genetic algorithms, it does not take into consideration only the best among the offspring but ranks the population formed by parents and offspring. This improves the performance of a genetic algorithm.

6.1.2 Multi-objective

In case of more than one fitness function that may conflict with one with the other, the problem become a multi-objective optimization [105]

Definition of a general multi-objective optimization problem is

$$Maximize\, or\, Minimize F(x) = (f(x)_1, f(x)_2 \cdots f(x)_n)\ Subject\, to \begin{cases} g(x)_m = 0 \\ h(x)_k < 0 \end{cases}$$

Mainly two different paths can be followed for multi-objective optimization. The first is to create a combination of the objective functions in a single composite function: a typical approach is that of the weighted sum but the main problem lies in the correct selection of weights. In practice it can be very difficult to calculate the weights exactly and small variations can significantly change the result. For these reasons it is customary to prefer the second way, the identification of an area call Pareto front. The solutions so found will be non-dominant among them, one cannot improve in one objective without going to lose another. Genetic algorithms appear to be an excellent multi-objective optimization approach for the ability to search simultaneously in different regions of the solution space. This is convenient in non-convex, discontinuous or multi-modal problems in which it is no longer possible to find an optimal value but a sets of acceptable solutions. Fig 6.3 explains the concept of non-dominance in the Pareto front: the points going from 1 to 6 represent the variables of the state vectors that, replaced in the two objective functions, will give rise to a set of point of coordinates $P_n(f_1, f_2)$.Once the points are represented, a definition for dominance is needed:

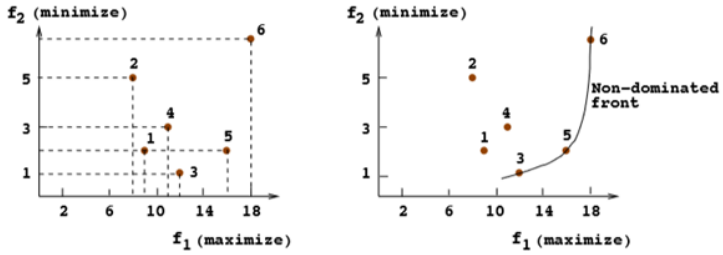


Figure 6.3: Non dominant front

Definition: A solution $x(1)$ is said to dominate another solution $x(2)$ if both the following conditions are true:

1. The solution $x(1)$ is no worse than $x(2)$ in all objectives. Thus, the solutions are compared based on their objective function values.

2. The solution $x(1)$ is strictly better than $x(2)$ in at least one objective.

Applying the definition build the non-dominated front, in which to pass to a lower f_2 value it is necessary decrease f_1, which goes against the goal of maximizing f_1. This trade-off property between the non-dominated points makes the practitioners interested in finding a wide variety of them before making a final choice.

The main objectives of a multi-objective optimization are:

1. Find a set of solutions belonging to the Pareto front

2. Find a set of different solutions that can best represent the Pareto front

Unlike the single objective the user, who needs only one solution, will have a set of excellent results from which he will have to get only one.

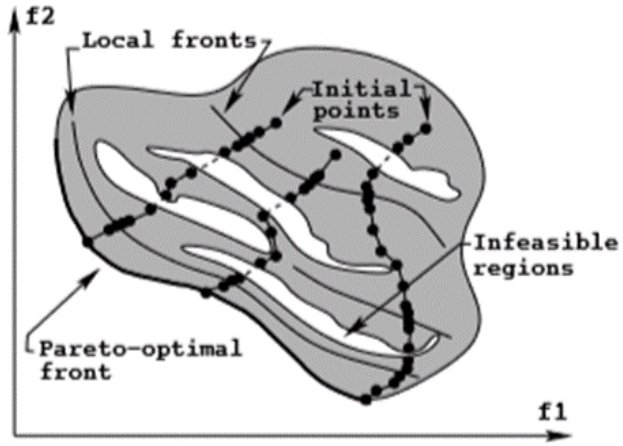


Figure 6.4: Convergence to Pareto front

However, during the course of an optimization task, the algorithm must overcome a number of difficulties, such as infeasible regions, local optimal solutions, flat regions of objective functions, isolation of optimum, etc., to converge to the global optimal solution (Fig. 6.4)t of Pareto-optimal solutions, the above balancing act must have to perform in every single simulation. Since simulations are performed independently, no information about the success or failure of previous simulations is used to speed up the process. When a population member overcomes certain difficulties and make a progress towards the Pareto-optimal front, its variable values and their combination reflect this fact. After getting all the results a Decision Maker is required, an expert user, who takes into consideration the pros and cons of all solutions based on non-technical but qualitative considerations.

There are mainly three approaches:

1. A priori. DM information is used to focus the search on the desired Pareto front instead of the entire border. If the constraints so imposed are too restrictive and the initial population too far away, there is a risk that the algorithm may diverge.

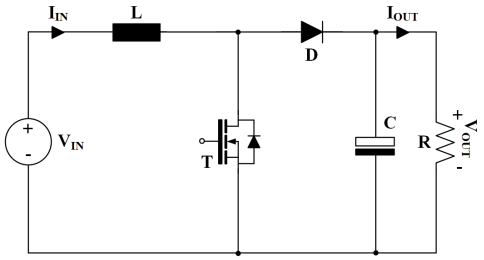
2. Iterative approach: the DM information is integrated into the algorithm, classifying the solutions obtained according to their preferences each t population. This integration makes the optimization much more complicated and therefore slower.

3. A posteriori: DM information is used after obtaining the solutions from the algorithm. The free growth of the population makes this approach applicable only to problems from two to four objectives.

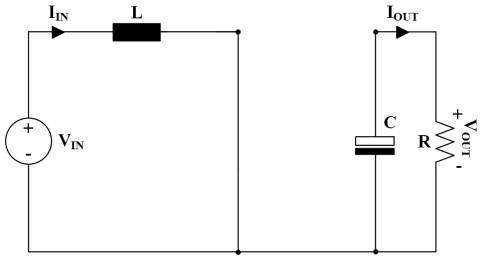
6.2 Application test bench

6.2.1 DC/DC boost converter

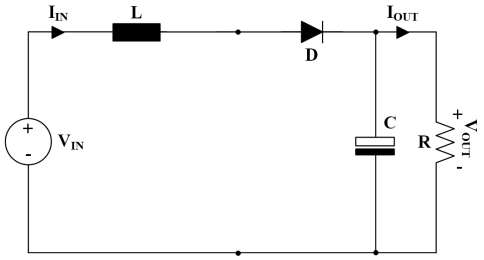
Initially it was decided to use an approach with the model in state space and validate the results calculated using the algorithm [106]. Taking the figures Fig. 6.5c and Fig. 6.5b it is necessary to calculate the matrices A,B,C,D which will multiply the state variables x and the input u to obtain the outputs y.



(a) Topology



(b) ON State



(c) OFF State

Figure 6.5: Equivalent circuits of the DC/DC boost converter.

$$\begin{cases} x' = Ax + Bu \\ y = Cx + Du \end{cases}$$

$$x_1 = i_L \mid x_2 = v_C \mid x = [x_1\, x_2] \mid u_1 = v_{in}$$

$$\begin{bmatrix} x_1' \\ x_2' \end{bmatrix} = \begin{bmatrix} 0 & 0 \\ 0 & -\frac{1}{RC} \end{bmatrix} \begin{bmatrix} x_1 \\ x_2 \end{bmatrix} + \begin{bmatrix} 1/L \\ 0 \end{bmatrix} u_1$$

While during the OFF state Fig. 6.5c are:

$$\begin{bmatrix} x_1' \\ x_2' \end{bmatrix} = \begin{bmatrix} 0 & -1/L \\ 1/C & -\frac{1}{RC} \end{bmatrix} \begin{bmatrix} x_1 \\ x_2 \end{bmatrix} + \begin{bmatrix} 1/L \\ 0 \end{bmatrix} u_1$$

Adding the matrices considering the duty cycle

$$\bar{A} = A_{(ON)}d + A_{(OFF)}(1-d)$$

$$\bar{A} = \begin{bmatrix} 0 & 0 \\ 0 & -\frac{1}{RC} \end{bmatrix} d + \begin{bmatrix} 0 & -1/L \\ 1/C & -\frac{1}{RC} \end{bmatrix} (1-d) = \begin{bmatrix} 0 & -\frac{1-d}{L} \\ \frac{1-d}{C} & -\frac{1}{RC} \end{bmatrix}$$

$$\bar{B} = B_{(ON)}d + B_{(OFF)}(1-d)$$

$$\bar{B} = \begin{bmatrix} 1/L \\ 0 \end{bmatrix} d + \begin{bmatrix} 1/L \\ 0 \end{bmatrix} (1-d) = \begin{bmatrix} 1/L \\ 0 \end{bmatrix}$$

And finally:

$$\begin{bmatrix} x_1' \\ x_2' \end{bmatrix} = \begin{bmatrix} 0 & -\frac{1-d}{L} \\ \frac{1-d}{C} & -\frac{1}{RC} \end{bmatrix} \begin{bmatrix} x_1 \\ x_2 \end{bmatrix} + \begin{bmatrix} 1/L \\ 0 \end{bmatrix} u_1$$

$$\begin{bmatrix} y_1 \\ y_2 \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix} \begin{bmatrix} x_1 \\ x_2 \end{bmatrix} + \begin{bmatrix} 0 \\ 0 \end{bmatrix} u_1$$

Once the matrices have been obtained, it was decided to work on the optimization of five objectives:

1. $Current\,ripple = \dfrac{(V_{in}d)}{(f_{sw}L)}$
2. $Voltage\,ripple = \dfrac{I_{out}d}{f_{sw}C}$, $I_{out} = (1-d)I_{in}$
3. Total Losses:
   - $Switching\,losses = E_{sw}f_{sw}$

- $Switch\,conduction\,losses = I_{out}^2 dR_{sw}$
- $Diode\,conduction\,losses = I_{out}^2(1-d)R_D$

4. Peak voltage

5. Settling time

As can be seen in Fig. 6.5b and Fig. 6.5c, the diode will be in conduction only in the T_{off} of the switch, that is when it will be directly polarized by the voltage drop V_{in} and V_o, while the transistor will be conducting when it is closed during T_{on}.

It is calculated the response to the 300V step considering however both the capacitor and the inductor with a residual charge. The DC-DC boost has been sized for these values (Tab.6.1) (the losses introduced by the resistive part of the inductor and capacitor have been neglected compared to those of semiconductor).

V_{in}	$300V$
I_{in}	$26.6A$
V_{out}	$400V$
I_{out}	$20A$
d	0.25
R_{out}	20Ω
$Power$	$8kW$
R_{sw}	0.03Ω
R_D	0.03Ω
L	$700\mu H$
δL	$\pm 50\%$
C	$200\mu F$
δC	$\pm 50\%$
f_{sw}	$50kHz$
Δfsw	$\pm 50\%$

Table 6.1: Parameters of DC-DC boost

After executing the algorithm 10 times different solutions have been obtained and one has been taken as a good trade-off with respect to the different fitness functions. Than the values were implemented in the model in state space and in a model realized in Simulink to see the current and voltage ripple caused by the commutation of the switch.

It was decided to start the validation of the method from two equations and going to complicate it after analysing the results.

Two objectives In the two-dimensional case, the study focused on minimizing the input current ripple, caused by the switch, and minimizing losses in conduction and switching. The variables that come into play with these equations will be the inductance value and the

frequency while the trade-off will be only on the frequency since increasing it decreases the current ripple but will increase the switching losses. The results obtained from the algorithm are shown in Fig. 6.6 and Fig. 6.7 with an initial population of 1000 and crossover at 0.8.

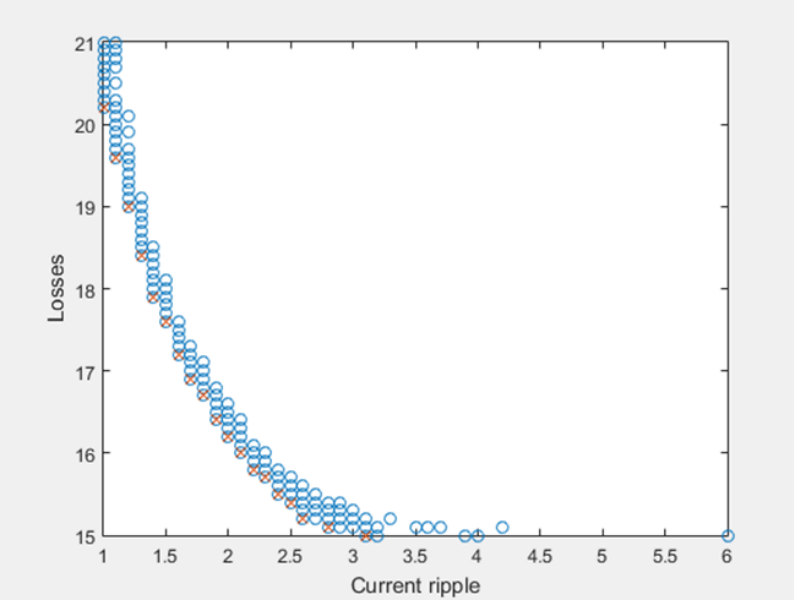


Figure 6.6: Pareto front with two objectives

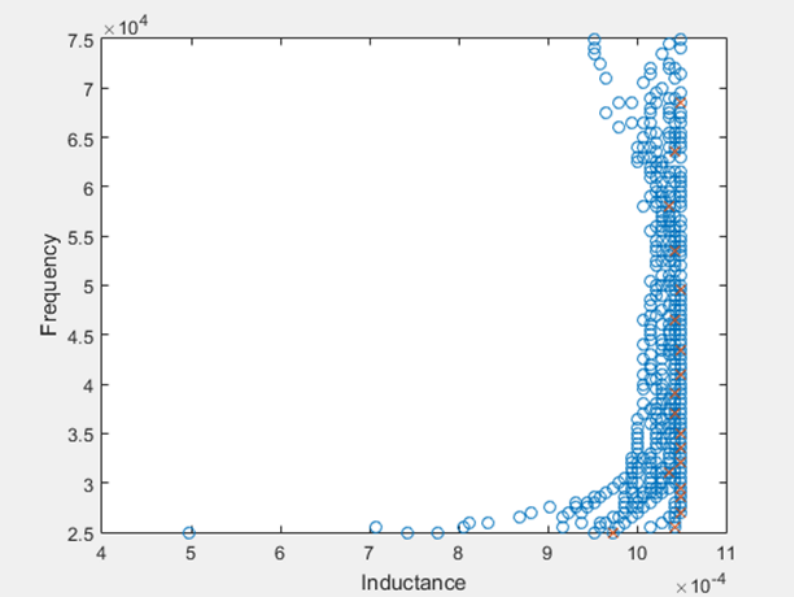


Figure 6.7: Variables that belong to the Pareto front

The algorithm was iterated ten times to space the Pareto front, but this caused, taking into account the set of results, dominated values (blue circles). Through a post-processing algorithm the choice of non-dominated values was re-run. The red crosses curve represent the Pareto front and the values that the Decision Maker can take into consideration for the design of the inductance and the frequencies (Tab. 6.2).

	Current ripple [A]	Losses[W]	Inductance [μH]	Frequency [Hz]
1	3	15	1001	25000
2	2.7	15.1	1050	26000
3	2.6	15.2	1050	27000
4	2.5	15.4	1036	28500
5	2.4	15.5	1050	29500
6	2.3	15.7	1036	31000
7	2.2	15.8	1050	32000
8	2.1	16	1050	33500
9	2.0	16.2	1050	35000
10	1.9	16.4	1050	37000
11	1.8	16.7	1043	39500
12	1.7	17	1043	41500
13	1.6	17.2	1050	43500
14	1.5	17.6	1036	47000
15	1.4	18	1050	50000
16	1.3	18.4	1043	53500
17	1.2	18.9	1050	57500
18	1.1	19.6	1036	63000
19	1.0	20.2	1043	68500

Table 6.2: Results of the optimization with two objectives

It can be noted that even if the trade-off is only on the frequency, the inductance value varies from 1050 μH to 1001 μH thus varying the results obtained making them unreliable. This is due to the fact that the algorithm is not able to understand the objective functions but analyses the problem as if it were a black box Fig. 6.8

Figure 6.8: Black box

Regardless of the functions present, the genetic algorithm will only see the populations

(X_t) and the corresponding fitness values (Y_t) and, based on the latter, will choose those with the highest rank to generate the next population (X_{t+1})

	Current ripple [A]	Losses[W]	Inductance [μH]	Frequency [Hz]
1	2.9	15	1050	25000
2	2.7	15.1	1050	26000
3	2.6	15.2	1050	27000
4	2.5	15.4	1050	28500
5	2.4	15.5	1050	29500
6	2.3	15.7	1050	31000
7	2.2	15.8	1050	32000
8	2.1	16	1050	33500
9	2.0	16.2	1050	35000
10	1.9	16.4	1050	37000
11	1.8	16.7	1050	39500
12	1.7	17	1050	41500
13	1.6	17.2	1050	43500
14	1.5	17.6	1050	47000
15	1.4	17.9	1050	50000
16	1.3	18.4	1050	53500
17	1.2	18.9	1050	57500
18	1.1	19.5	1050	63000
19	1.0	20.2	1050	68500

Table 6.3: New Results of the optimization with two objectives

Re-executing the algorithm by setting the inductance to the maximum project value, the values in the (Tab.6.3) and new Pareto front will be obtained Fig. 6.9 and Fig.6.10.

Three objectives In this second case study a third fitness function was added, depending on both the capacity value and the frequency value.

$$Voltage\,ripple = \frac{I_{out}d}{f_{sw}C}, I_{out} = (1-d)I_{in}$$

The decrease in losses this time will not only lead to an increase in the ripple current but also an increase in the ripple voltage. In Fig.6.11 both the values calculated by the genetic algorithm and the non-dominated values present in the Pareto front were plotted. Fig.6.12 shows the values of inductance, capacity and frequency which result in the Pareto front.

In Fig. 6.13 and Fig. 6.14 instead only the non-dominated points are represented in order to make the spatial position of these ones clearer.

Also in the three objectives the algorithm was executed more than once to spacing out in the solution plan and, in post processing, the values in the Tab.6.4 were obtained.

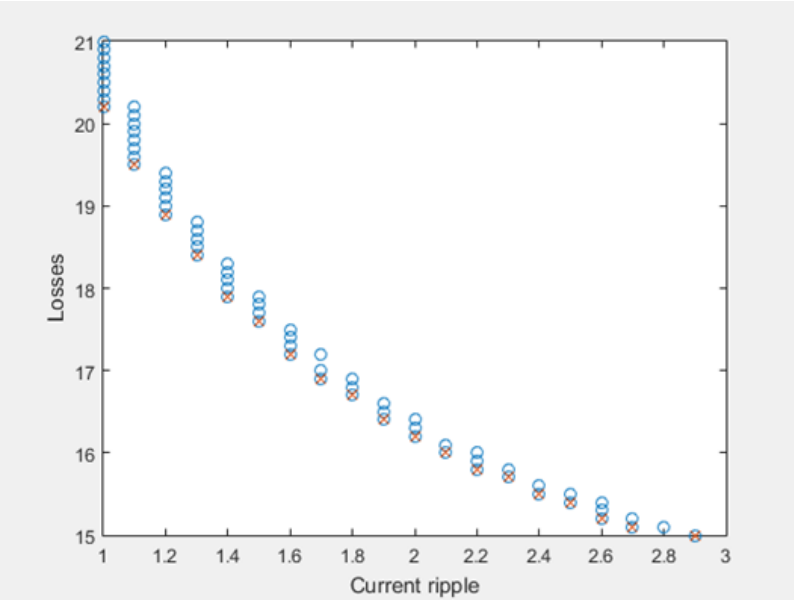


Figure 6.9: New Pareto Front with two objectives

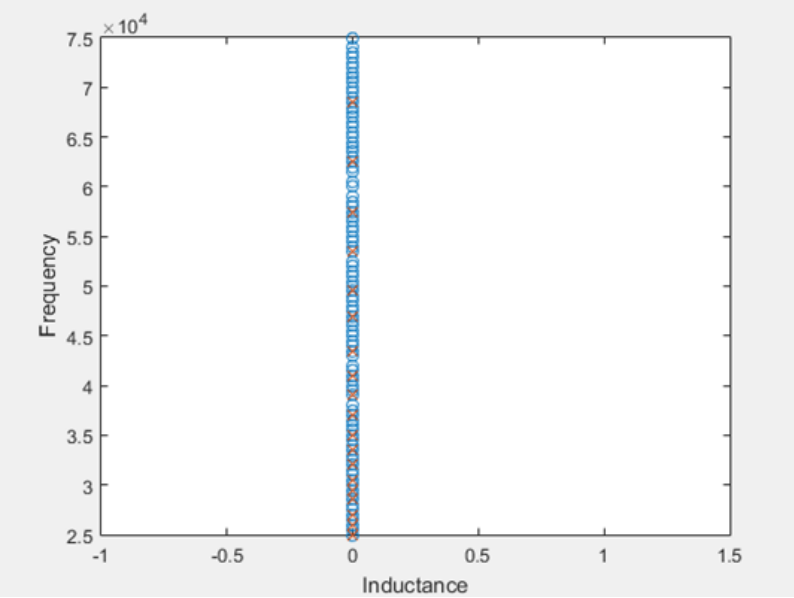


Figure 6.10: New variables that belong to the Pareto front

To avoid that the results are the same due to the approximations made it is necessary to increase the level of precision. However, this involves a higher calculation effort, a high number of solutions and a not perfect repeatability. It's possible to note that for a few objective functions and with a restricted range the discretization of the Pareto front is feasible and almost repeatable, this is no longer true for more numerous functions and free

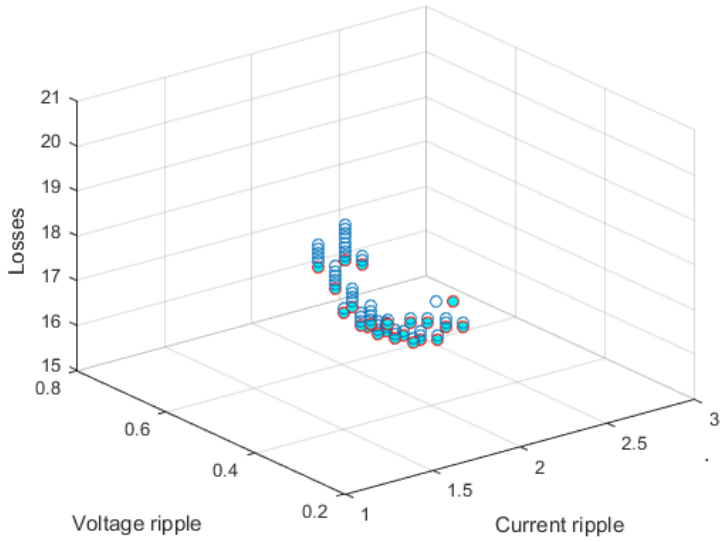


Figure 6.11: Solutions of the genetic algorithm with three objectives

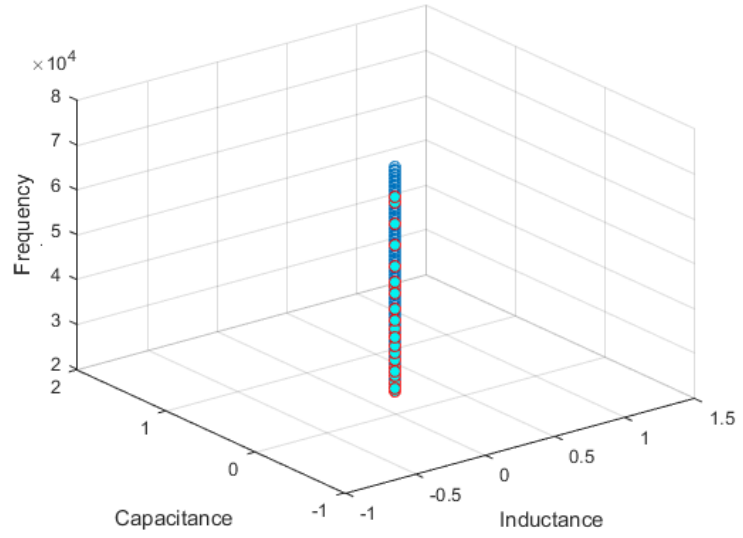


Figure 6.12: Variables that generate the solution with three objectives

to act in a larger space.

Two possible approaches can be distinguished with the genetic algorithm:

- In the case of a few simple functions or having a finite dataset of values as inputs, it is possible to discretize the entire Pareto front and get a single solution repeatable.

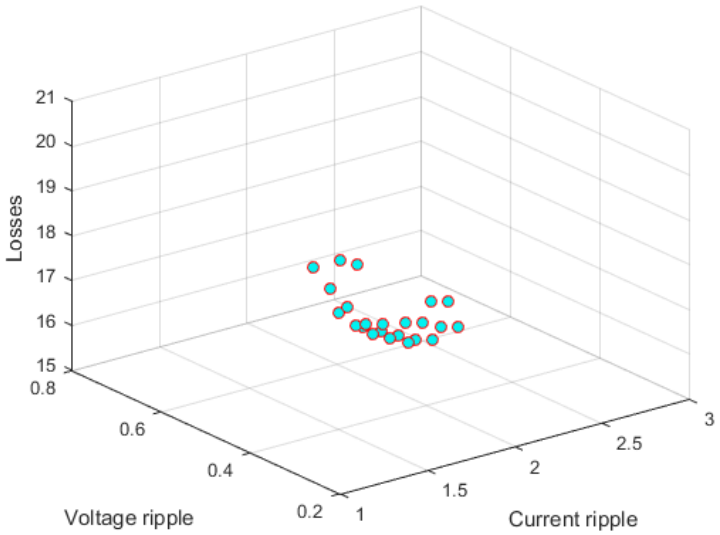


Figure 6.13: Pareto front with three objectives

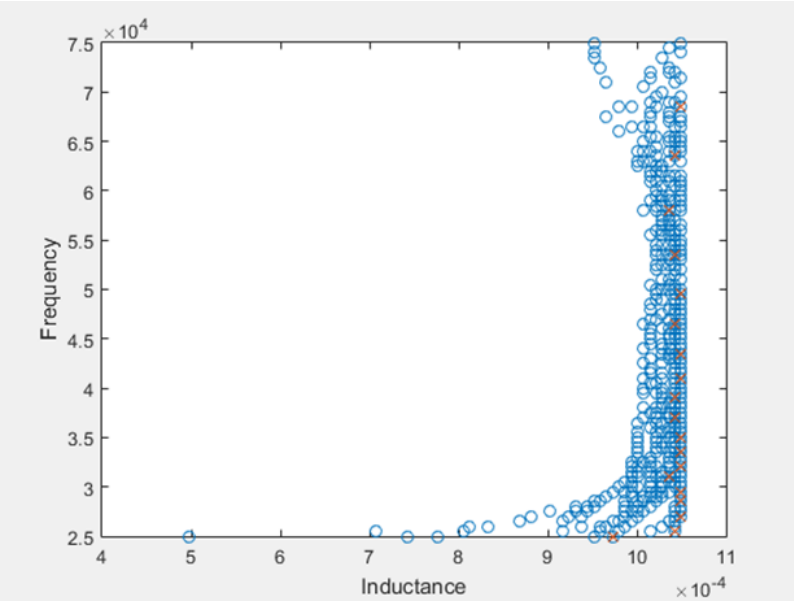


Figure 6.14: Variables that belong to the Pareto front

It can be seen like a Monte Carlo method but more efficient [107] [108]

- For more objectives and more complex function it is not possible to know, with an acceptable deviation, all the values of the curve. It then passes to the repeatability not of the single value but to the repeatability of the Pareto front.

	△Current[A]	△Voltage[V]	Losses[W]	Induct.[μH]	Capacit.[μF]	Frequency[Hz]
1	1.1	0.2	20	1050	300	67000
2	1	0.2	20.2	1050	300	68500
3	1.5	0.3	17.8	1050	300	48500
4	1.4	0.3	17.9	1050	300	49500
5	1.3	0.3	18.4	1050	300	53000
6	1.2	0.3	18.9	1050	300	57500
7	1.1	0.3	19.5	1050	300	62500
8	1.9	0.4	16.5	1050	300	37500
9	1.8	0.4	16.7	1050	300	39000
10	1.7	0.4	16.9	1050	300	41000
11	1.6	0.4	17.2	1050	300	43500
12	1.5	0.4	17.6	1050	300	47000
13	2.3	0.5	15.7	1050	300	30500
14	2.2	0.5	15.8	1050	300	32000
15	2.1	0.5	16	1050	300	33500
16	2.0	0.5	16.2	1050	300	35000
17	1.9	0.5	16.4	1050	300	37000
18	2.7	0.6	15.1	1050	300	26000
19	2.6	0.6	15.2	1050	300	27000
20	2.5	0.6	15.4	1050	300	28500
21	2.4	0.6	15.5	1050	300	29500
22	2.9	0.7	15	1050	300	25000
23	2.8	0.7	15.1	1050	300	25500

Table 6.4: Results of the optimization with three objectives

The purpose of this approaches is to obtain information on the set of Fitness functions and to have acceptable results but which are not so repeatable. Considering the complexity of the cases it was decided to opt for the second method, such as in this reference [109] [110] [111].

Five objectives After this clarification, the results obtained with five objective functions with integer inputs and free to move in a much wider range will now be shown. This is done because, not being able to guarantee the repeatability of the single point, it is necessary at least to obtain results that lie on the Pareto curve.

To view the results, three variables were chosen in two graphs in which the colors is modified by the fourth Fig.6.15 and by the fifth variable fig. 6.16

Among the results it was decided to choose the one with the values of the Tab.6.5 which represents a good compromise for all the functions.

Fig. 6.17 and Fig. 6.18 shows the plot of the 3 step responses of the converter:

	Minimum	Maximum
L	300 µH	1000 µH
C	10 µF	1000 µF
F_{sw}	10 kHz	100 kHz

Table 6.5: Constrains of input variable

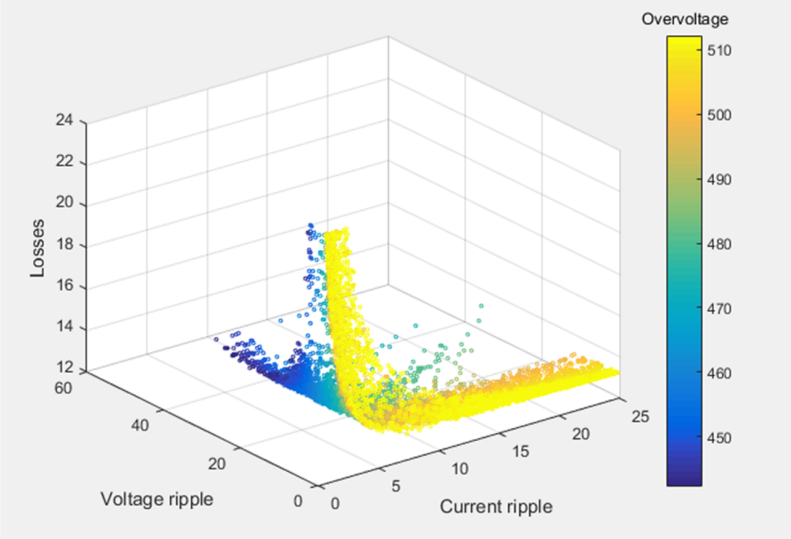


Figure 6.15: Pareto front with five objectives without the Settling time

- The one with the red crosses derives from the equations in state space considering an ideal case without losses.
- That red line always derives from the equations in state space but considering the losses in the diode and in the switch.
- The yellow one derives from the model of the Boost realized on Simulink considering

Parameters		
Inductance [μH]	Capacitance [μF]	Frequency [Hz]
825	140	13000

Results				
Current ripple [A]	Voltage ripple [V]	Peck-voltage [V]	Settling time [s]	Losses[W]
6.99	27.47	456.33	0.002	13.56

Table 6.6: Value and results for five objectives

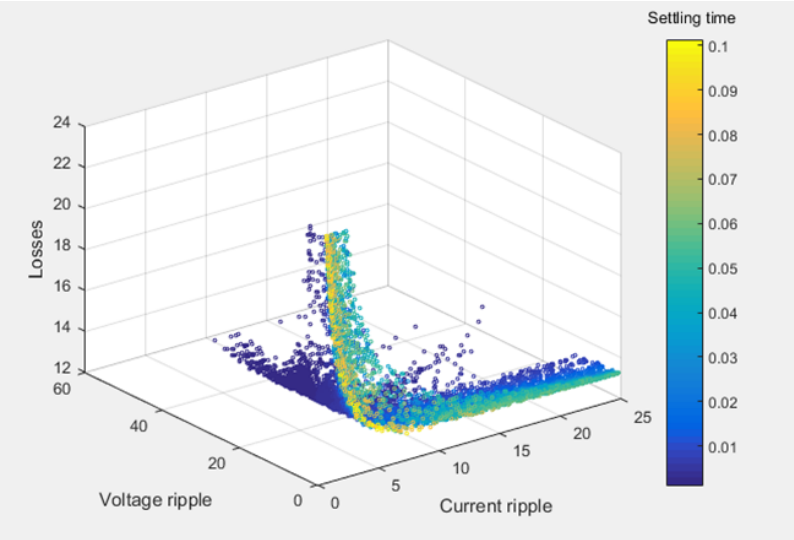


Figure 6.16: Pareto front with five objectives without the Overvoltage

the losses.

The same considerations for the currents with blue crosses, red line and yellow line. It can be noted that the results are verified from the pointers in the plot.

$$\Delta I \simeq 7\,\mathrm{A} \quad \Delta V \simeq 27\,\mathrm{V} \quad \hat{V} \simeq 456\,\mathrm{V} \quad Ta_{5\%} \simeq 2\,\mathrm{m\,sec}$$

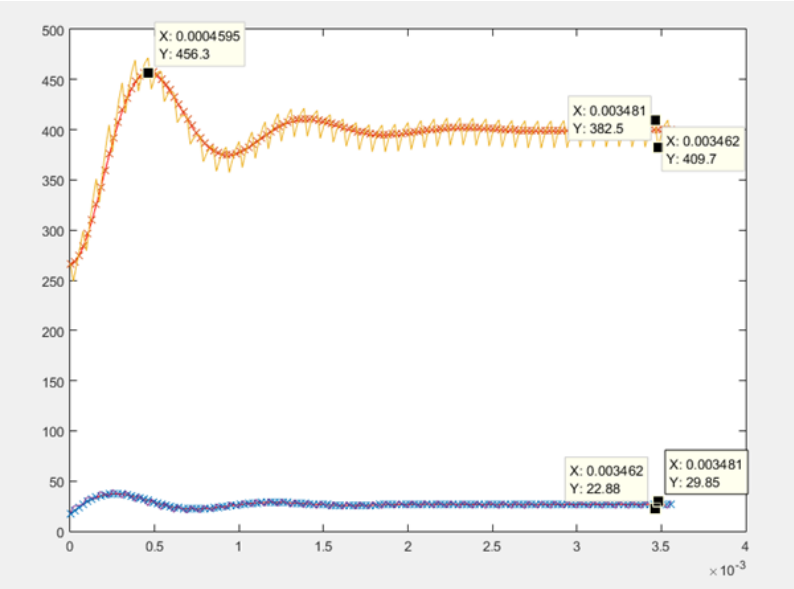


Figure 6.17: Step response of the DC-DC boost

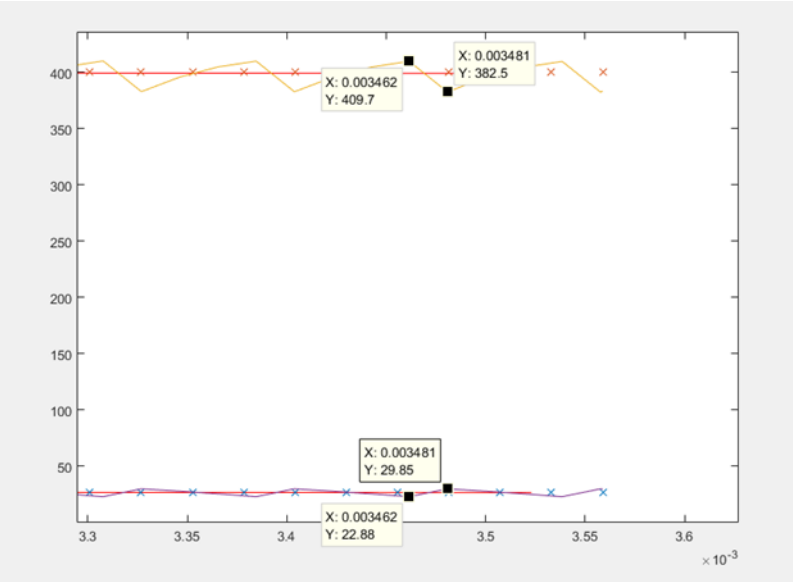


Figure 6.18: Zoom in of the step response

6.2.2 Vienna boost converter

After having made our considerations on the simplest case of the boost and having analysed the possible approaches of multi-objective optimization using genetic algorithms, it was decided to work with the following objective functions:

- Booster inductor volume.
- Volume of output capacitors.
- Losses in semiconductors.

These Fitness Functions will be subject to two constraints

- Input ripple to the inductor less than 10
- Ripple of output voltage from the two capacitors below 10%

This is done because, from the design point of view, it is not important to have precise values for the variations of I_L and V_C but which remain included in prefixed constraints.The input ripple can be calculated from eq. (6.1)

$$I_L = \frac{V_{DC}}{8 \times L_{boost} \times F_{sw}} \tag{6.1}$$

According to eqs. (3.50) and (3.51) shown in Chap.3.3.5 and table 6.7, the semiconductor losses in the three legs of the Vienna that will be directly proportional to the switching frequency as in the DC-DC boost.

V_{0_T}	0.85 V
V_{0_D}	1.25 V
r_{0_T}	40 mΩ
r_{0_D}	25 mΩ
M	1
I_L	24 A
I_{ref}	25 A
V_{DC}	800 V
V_{ref}	600 V
E_{ON}	610 µJ
E_{OFF}	2.37 µJ
E_{RR}	222 µJ

Table 6.7: Device Parameters

For the calculation of the voltage ripple an experimental equation has been realized that takes into account two main contributions: a low frequency voltage variation, with fundamental equal to six times the network frequency, and a high frequency voltage variation caused from switching. Both ripples depend on the value of the capacitance and the switching frequency but in different ways. Going to calculate the ΔV for different combinations of F_{sw} and C_{out} a two-dimensional fitting was performed and the Fig. 6.19 was obtained

This will be used to constrain the maximum voltage exiting the Vienna during the execution of the genetic algorithm.

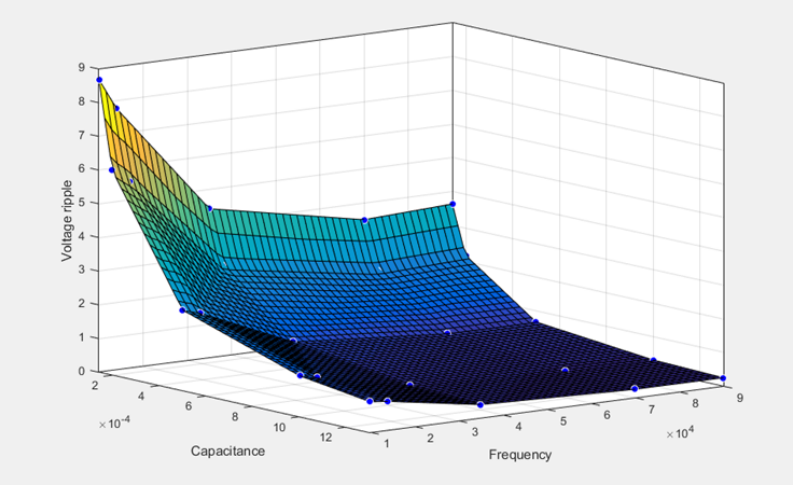


Figure 6.19: Voltage drop in relation to frequency and capacitance

Also for the sizing of C and L, an experimental formula was used.

A pair of capacitor made by Vishay were taken and a fit was performed between the value of the capacitance and the size of the component Fig.6.20

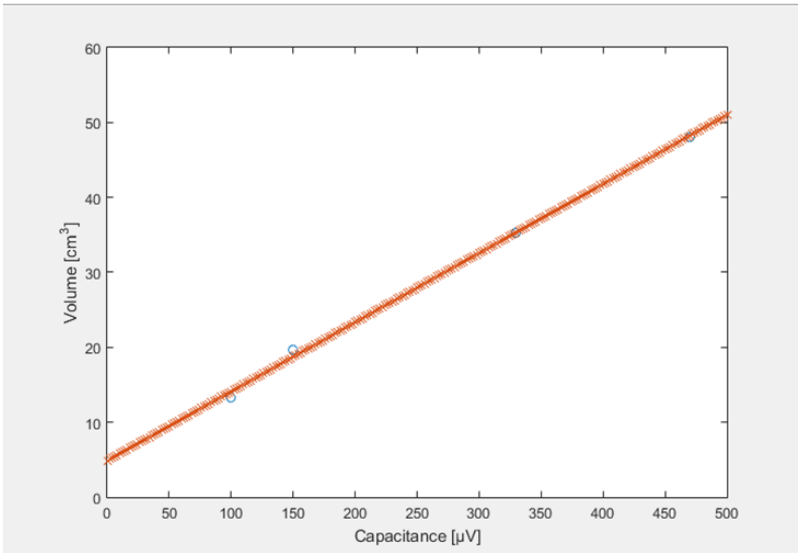


Figure 6.20: Relation between volume and capacitance

$$Volume = A * Capacitance + B$$
$$A = 0.092259931645821$$
$$B = 4.878806401438919$$

For the inductor instead it can be shown that the area product is also related to the volume of the inductor [34] by:

$$A_W A_{core} \propto \ Vol_L^{\frac{4}{3}}$$

$$A_W A_{core} \propto \ \frac{LI_{peak} I_{rms}}{J_{max} B_{sat}} \propto E_L \propto LI_L^2$$

Combining the two equation above the inductor volume can be expressed as [112]:

$$Vol_L \propto \ \left(LI_L^2\right)^{\frac{3}{4}}$$

So is possible to find the volume of inductor knowing the inductance and the current if the design technology is kept the same (conductor type, core material, geometry).

$$Vol_L = K_{VL0} \ \left(LI_L^2\right)^{K_{VL1}}$$

Where K_{VL0} and K_{VL1} are proportionality regression coefficients found by reference inductor realized by Siemens with conductor made by copper (Series 3-AC 4EUXX) Fig. 6.21

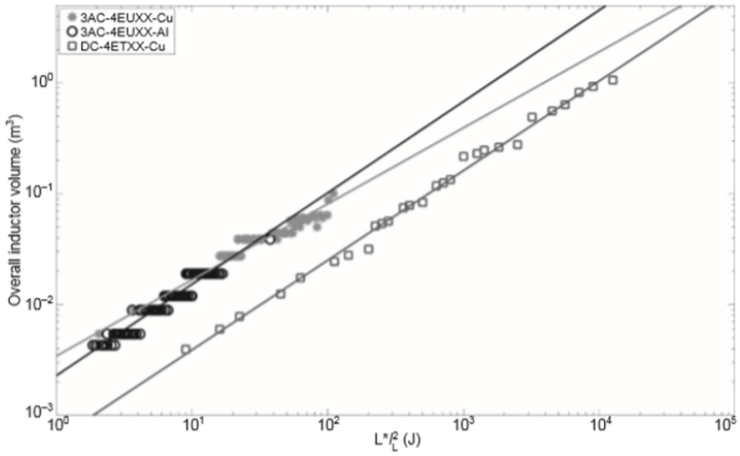


Figure 6.21: Relation between volume and LI_L^2

After defining the objective functions and the constraints, the genetic algorithm is performed ten times with an initial population of one thousand individuals and a crossover of 0.8 Fig. 6.22 and Fig 6.23. The Vienna prototype was built for a nominal Power of 11KW, connected directly to the LV, with a control system in Pulse Wide Modulation (PWM) and a current loop for the output current.

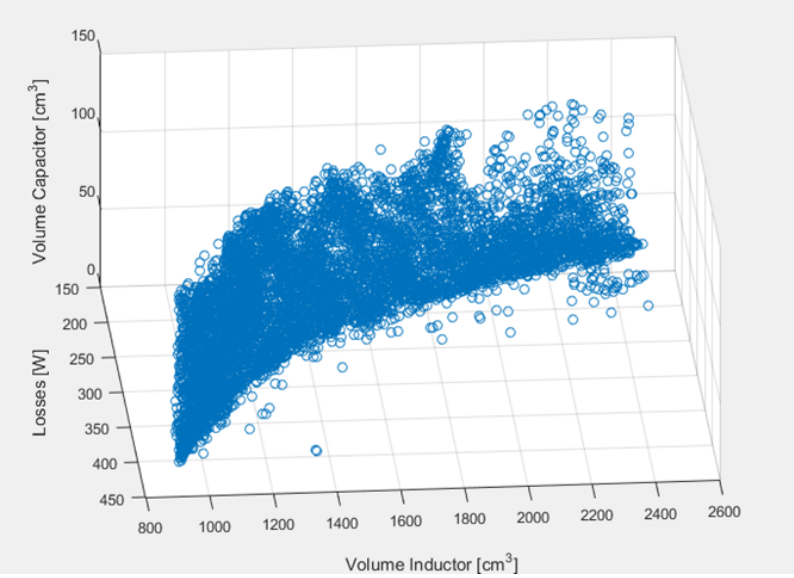


Figure 6.22: Pareto front for the Vienna with three objectives

Among the solutions obtained, three acceptable solutions have been taken Tab. VII:

1. The one that minimizes the size of the inductor and the capacitor size

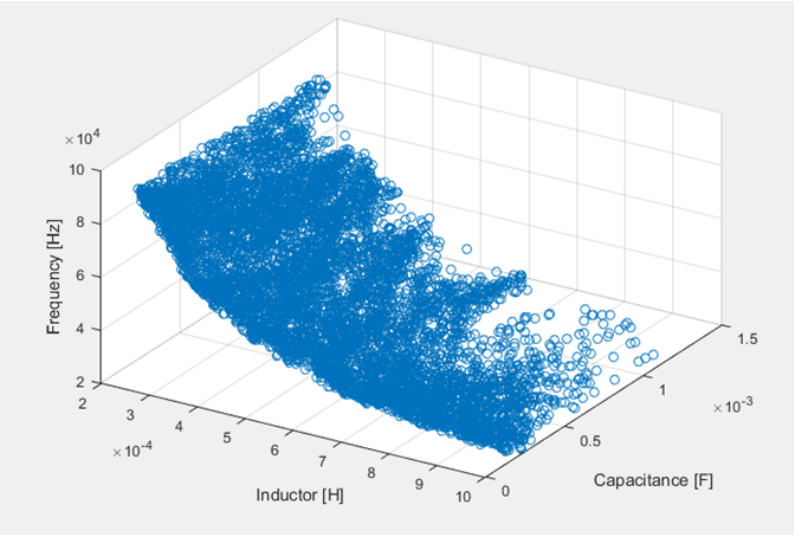


Figure 6.23: Variables that belong to the Pareto front of the Vienna

2. The one that minimizes losses
3. A trade-off between the objective functions

	Vol.L[cm^3]	Vol.L[cm^3]	Losses[W]	Induct.[μH]	Capacit.[μF]	Freq.[Hz]	Effic.[%]
1	907.2	18.3	441	230	146	88900	95
2	2446	31.5	173.1	976	289	20500	98
3	1443	45.6	268.1	452	441	44800	97

Table 6.8: Value and results for the Vienna rectifier

It is necessary to calculate the FFT (Fast Fourier Transform) and analyse the goodness of the solution.

Regarding the output voltage is necessary to have a very low THD to guarantee a good quality of the DC voltage Fig 6.24. Indeed the value is equal to 0.04% and the first harmonic have an amplitude of 0.02% of the DC component.

For input current it is necessary to comply with IEC 61000. With reference to commercial and industrial environments, the 5th harmonic is less than 1.2% respect to the fundamental at 50Hz Fig. 6.25. Moreover the total harmonic distortion is equal to 7.39% and in the general, for industrial application, it is necessary to have a value less than 8%.

6.3 Conclusion

Using only mathematical calculations the engineer should be able to observe how changes of one or more parameters will affect the desired system properties and functionalities. In

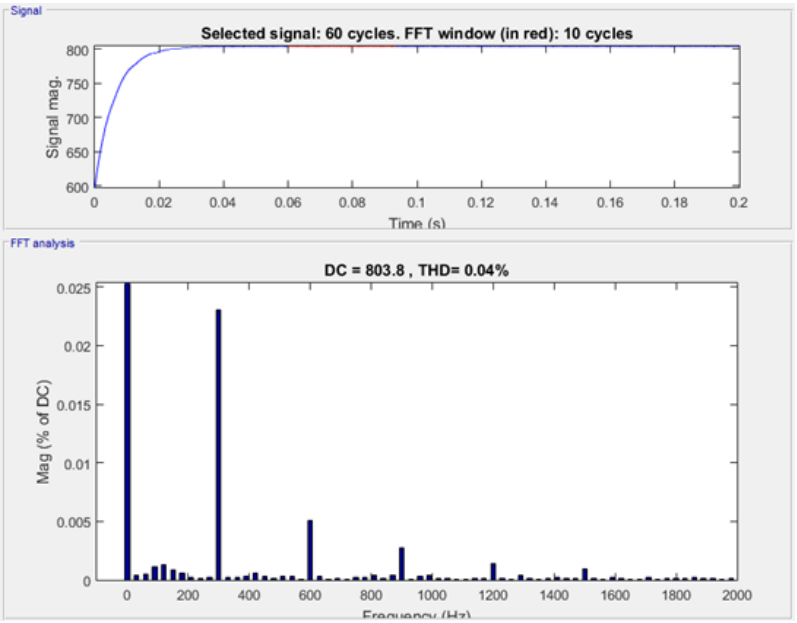


Figure 6.24: FFT of the V_{out}

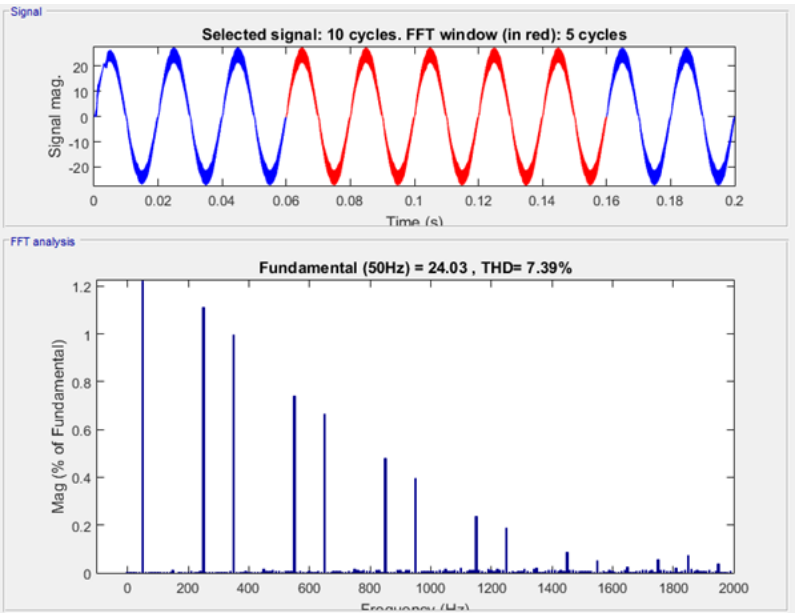


Figure 6.25: FFT of the I_{in}

the analysis of the DC-DC Boost two methodology have been shown and the most suitable for complex design was chosen. It is important to emphasize that the repeatability can be associated only to the Pareto front and not to the single point. With this approach the Decision Maker get more information about the system and can choose wisely the

operation point. Possible future developments may be to integrate the control equations to calculate the values of the PI coefficients in the current loop and in the voltage loop. Another possible application that can be done for the Vienna rectifier is the comparison of different type of modulation [113] like PWM, Selective Harmonic Elimination (SHE) Modulation and Optimized Harmonic Stepped Waveform (OHSM).

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Chapter 7

Proposed Prototype

7.1 Mixed Signals Based Control of a SiC Vienna Rectifier for On-Board Battery Chargers

This work deals with the implementation of a suitable control strategy for the AC/DC stage, realized by a three phase Three Level Vienna Rectifier (3LVR) [46], whose circuital scheme is shown in Fig.7.1. Being a multilevel topology, the 3LVR has the advantage of reducing the electrical stresses on the power devices(Chap.3.3), ensuring small current distortion. In fact, this topology allows to draw the utility current at unity power factor, minimizing the line distortion and maximizing the real power available from the utility outlet. Moreover, it features a simple construction, high efficiency and high reliability as it requires very few active power switches respect other equivalent topology [46]. This converter is driven according to the four modes of operation displayed Fig.7.2, selected on the basis of the grid phase current i_{L_j} (with $j = a, b, c$) polarity and the status of the bidirectional switches S_j. In this study the 3LVR has been equipped with Silicon Carbide (SiC) Metal Oxide Semiconductor Field Effect Transistors (MOSFETs), which are capable of lower $R_{DS_{ON}}/A$, higher switching frequencies and higher junction temperatures than silicon devices(Chap.2.2). Thanks to the high switching frequencies, in the range $fs = 70kHz \div 200kHz$, a considerable reduction of the size and cost of passive components can be achieved (Chap.3) [45, 60] instead at the same time the high frequency can be generate some issue in particular applications (Chap.4.2) [100, 101]. From a control point of view, an active rectifier is controlled by implementing two nested feedback control loops [114–116] and many studies also analyze sensorless solution [117–119]. The inner current control loop ensures unity power factor operations, while the external control loop performs the output DC voltage regulation. The bandwidth of the current loop must be sufficiently larger (ten or more times) than that of the voltage one in order to almost decouple the dynamics of the two control loops. The digital implementation of the control structure requires control units including hardware peripherals such as Analog to Digital Converter (ADC) and Pulse Wide Modulation (PWM). Consequently, the sampling/conversion process performed by the ADC introduces a delay degrading the controller response during transients. In addition, the whole control algorithms must be executed suitably fast in order to not compromise

the performance and stability of the system [120].

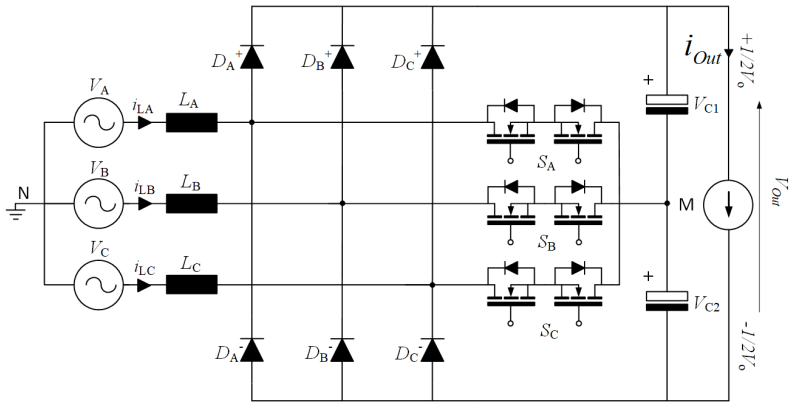


Figure 7.1: Circuital scheme of the three phase Three-Level Vienna Rectifier

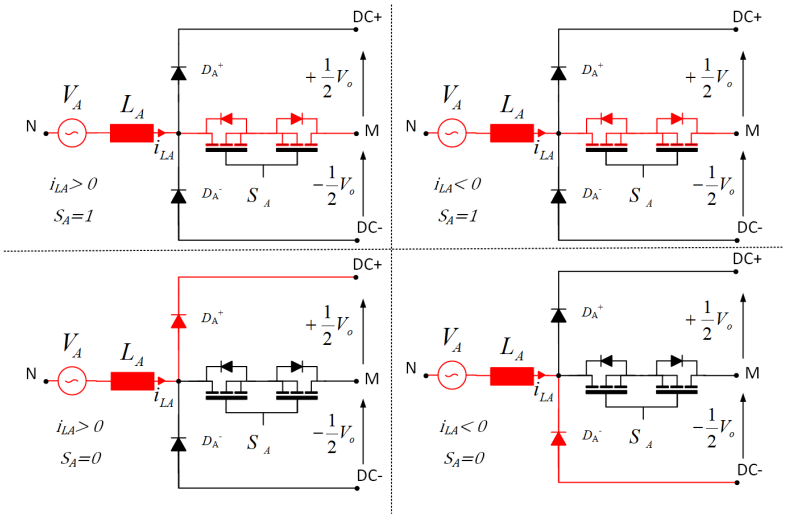


Figure 7.2: Circuital scheme of the three phase Three-Level Vienna Rectifier (a), and modes of operation of the phase A as example (b).

The last issue becomes more and more severe when the switching frequency of the power converter increases, as in case of Wide Band Gap (WBG) devices-based power converters. This could affect the minimum cost value to be considered for the control units that hardly can be reduced unless a different control approach is adopted. In this activity, a mixed-signal control architecture is investigated where the high bandwidth control loops are implemented using analog technology, leading to fast transient response under load and voltage steps. The proposed implementation represents a good tradeoff between performances and costs. Although the proposed Mixed Signal Control has been applied in this paper on the 3LVR shown in Fig.7.1, it is of general application and it can be virtually implemented in any other active power rectifier converter with minor

modifications.

7.1.1 Proposed mixed-signal control architecture

The block diagram of the proposed mixed-signal controller architecture is shown in Fig.7.3, where the main parts of the control system are highlighted by dashed lines. As mentioned above, the analog control stage implements a high bandwidth current loop, while the outer voltage control is digitally performed. Although a single current loop is indicated in Fig.7.3, three identical channels, one per each phase, have been realized. In addition, a PWM modulator and a zero-voltage detection-based phase estimator need to be implemented in order to properly perform the power factor correction and the voltage synthesis on the AC side of the power converter.

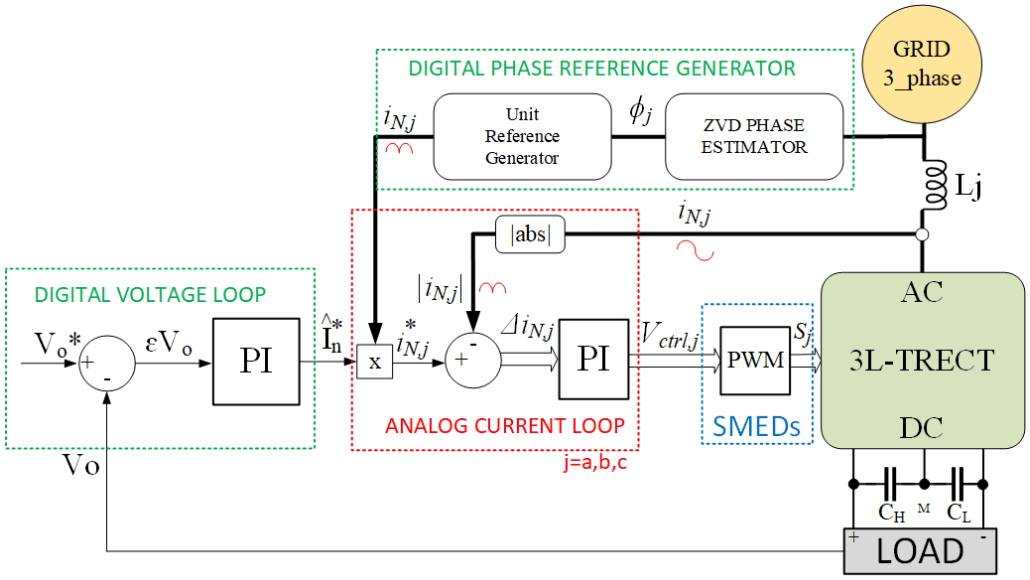


Figure 7.3: Block diagram of the proposed mixed-signal controller architecture.

The proposed control scheme (fig. 7.12)has been implemented in a digital controller, a STNRG388A[1] (Table.7.1). The IC is a part of a family of digital controller for power conversion application and is based on low cost STM8[2] and includes six advanced programmable and independent State Machine Event Drivens (SMEDs); they are advanced programmable PWM generator signals that can be controlled by both external events (I/O signals) and internal events (counter timers) (Fig.7.4). SMEDs are operated in parallel and independently by the software code executed in the microcontroller. In the proposed implementation, the SMEDs have been exploited to implement the carrier-based PWM

[1]STMicroelectronics - Digital controller for power conversion applications.

[2]STMicroelectronics - Digital 8 bit Microcontroller platform.

modulator. They perform the comparison between the voltage control references and the carrier signal, using the comparator event inputs of the SMEDs.

STNRG388A
6 programmable SMED "State Machine Event Driven"
High Resolution PWM Generation (1.3ns)
Transactions triggered by sync/async external events or internal timers
4 analog comparators
4 ADC analog to digital converters
low propagation time (50ns)

Table 7.1: Technical specifications of the STNRG388A[3]

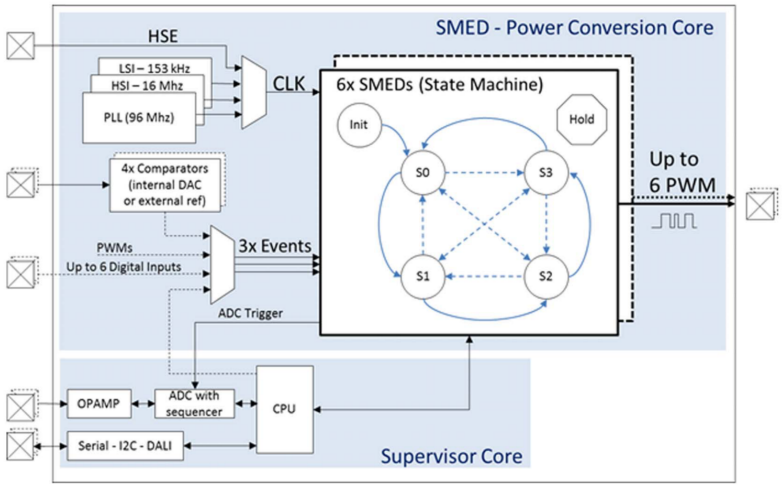


Figure 7.4: Block diagram of STNRG388A[3]

The block diagram of Fig.7.5 provides a graphical representation of the functions implemented in the SMED, in the microcontroller and by the external analog circuit. The algorithm carrying out the phase and frequency estimation of the grid voltage vector is implemented in the STNRG388 according to the scheme shown in Fig.7.6, where these quantities are computed starting from the detection of the grid voltage zero crossing points. The voltage control loop is sequentially executed in the STNRG388A[3] as well as the generation of the reference currents i_{ref_j} (with $j = a, b, c$).

The sinusoidal waveforms of the reference currents are determined by means of a Look Up Table (LUTs), synchronized to the AC grid, that consist of 500 sample normalized to the timer counter. The PWM signals applied to the bidirectional switches of the power converter are generated by comparing the V_{ctr_j} with a carrier signal from an analog wave generator, as it is shown in Fig.7.9 and according to (7.2). The other three SMEDs are exploited to produce PWM signals whose fundamental harmonic features same frequency

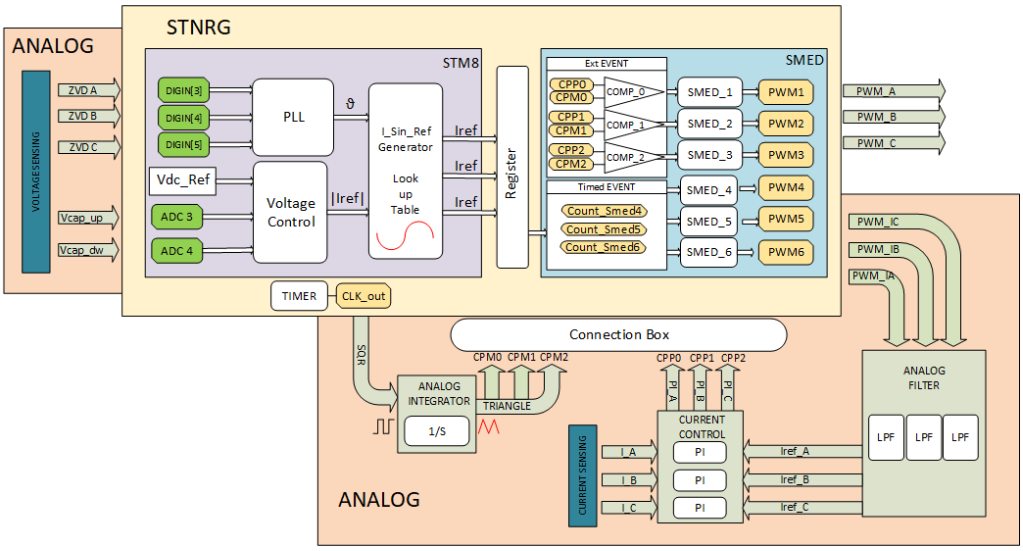


Figure 7.5: Block diagram of the proposed mixed-signal control implementation.

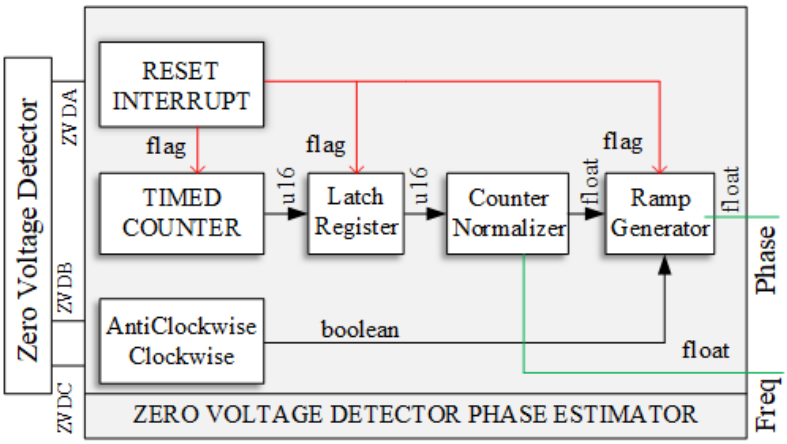


Figure 7.6: Block diagram of the frequency and phase estimation algorithm

and phase of i_{ref_j}, with $j = a, b, c$. The SMEDs are configured by using a dedicated Graphic User Interface (GUI), linking the external input/outputs to the state machines and by defining the operation rules. The signals i_{ref_j} (with $j = a, b, c$) from the SMEDs are filtered by using three analog Sallen-Key second order low pass filters with a cutoff frequency equal to 1560 Hz and quality factor $Q = 0.6$ to obtain an attenuation at the SMEDs frequency of $-24dB@40kHz$. The Sallen-Key architecture is displayed in Fig.7.10 according to (7.3). Finally, the PI controller of the current loop has been realized according to the circuital scheme of Fig.7.8 and equation (7.1), whose proportional and integral gains can be fixed by tuning the value of the two resistors R_i , R_f and one capacitor C_fz.

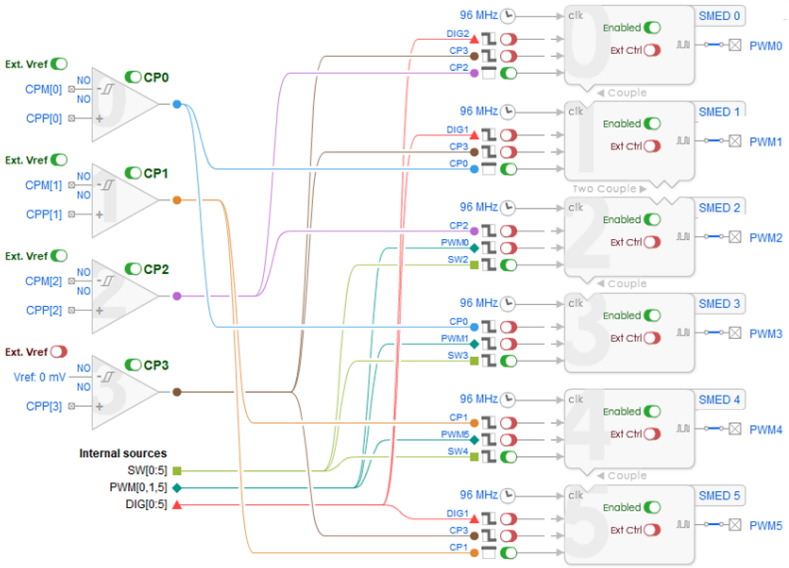


Figure 7.7: state machine configuration

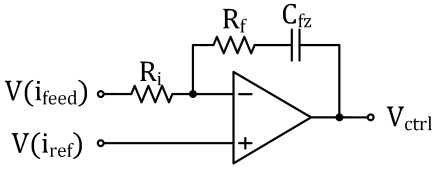


Figure 7.8: PI Controller

$$C(s) = K_P\left(\frac{s+\frac{1}{T_i}}{s}\right) \iff C(s) = \frac{R_f}{R_i}\left(\frac{s+\frac{1}{R_f C_{fz}}}{s}\right) \tag{7.1}$$
$$K_P = \frac{R_f}{R_i} \quad T_i = R_f C_{fz}$$

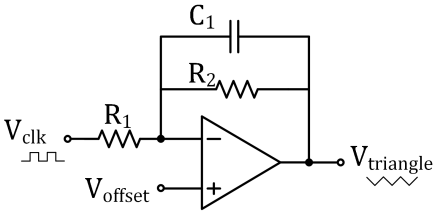


Figure 7.9: Carrier wave generator

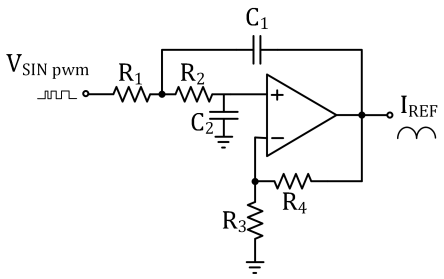


Figure 7.10: "Second Order Butterworth" low pass filter

$$\begin{aligned} A_{DC} &= -\frac{R_2}{R_1} \\ A_{AC}(s) &= -\frac{R_2}{R_1}\frac{1}{1+sC_1R_2} \\ f_0 &= \frac{1}{2\pi C_1 R_2} \end{aligned} \tag{7.2}$$

$$\begin{aligned} A_{DC} &= -\frac{R_4}{R_3} \\ f_c &= \frac{1}{2\pi\sqrt{R_1C_1R_2C_2}} \end{aligned} \tag{7.3}$$

Current control loop tuning

The generic structure of the considered current control loop in the Laplace domain is shown in Fig.7.11. It consists of the plant $P(s)$ approximated by the inductance of the main AC grid, the transfer function of the PI controller $C(s)$ and the transfer function taking into account the delay times due to the ADC conversion, sensing and conditioning circuits $M(s)$.

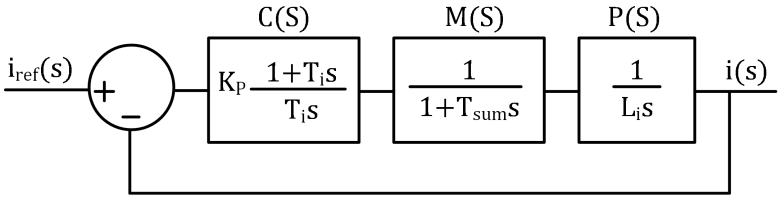


Figure 7.11: Structure of the current control loop

$$\begin{aligned} L(s) &= C(s)\,M(s)\,P(s) \\ H(s) &= \frac{L(s)}{1+L(s)} \end{aligned} \qquad , L_i = 514\ \mu H \tag{7.4}$$

Starting from the knowledge of the closed loop transfer function $H(s)$, the grid parameter L_i and the global delay T_{sum}, it is possible to compute the values of the PI controller

gains according to the symmetrical optimum criterion [121, 122] in (7.5) where the factor $\alpha > 1$ links the control parameters to the desired open loop phase margin $\psi = 60°$ and crossover frequency $\omega_c = 10kHz$ the parameters obtained are $K_P = 3{,}95$, $T_i = 130\mu sec$ and $\alpha = 1{,}73$

$$\left.\begin{aligned} K_P &= \frac{L_i}{\alpha T_{sum}} \\ \alpha &= \frac{1+\cos\psi}{\sin\psi} \end{aligned}\right| \begin{aligned} T_i &= \alpha T_{sum} \\ \omega_c &= \frac{\sqrt{\alpha}}{T_i} \end{aligned} \tag{7.5}$$

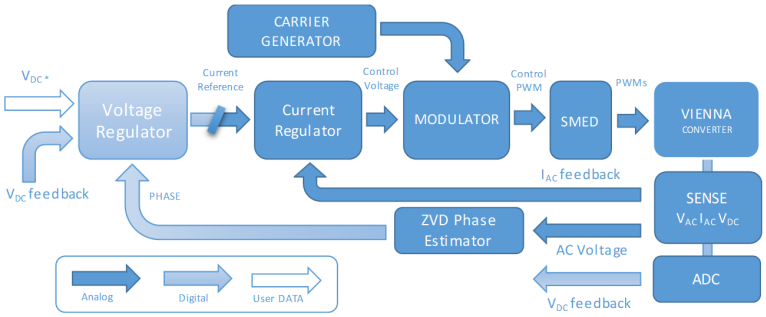


Figure 7.12: Block diagram of Mixed Signal Control algorithm

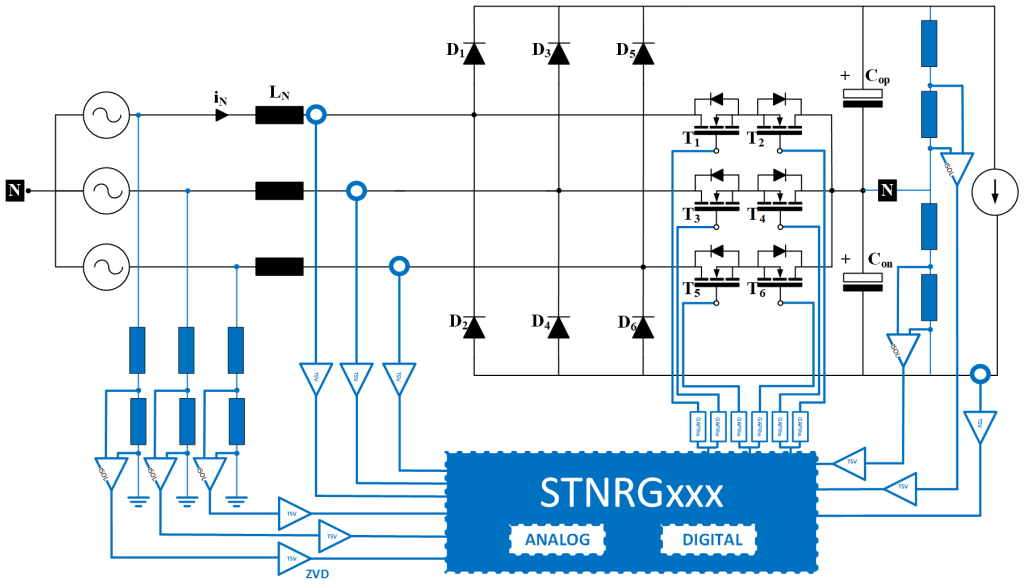


Figure 7.13: Logic schematic of the converter

7.1.2 Experimental validation

The mixed-signal control strategy presented in the previous section has been tested on the 12 kW battery charger prototype including a 3LVR able to convert a balanced three-phase power supply featuring 400 V − 50 Hz AC in a DC output voltage of 800 V(7.13). This first power stage is PWM operated at fs=70kHz and driven by the control board shown in Fig.7.14, specifically designed for this application. The power section has been realized using SiC diodes, STPSC20H12[4], as input rectifier and SiC MOSFETs, SCTW35N65G2[5] (55 mΩ − 650 V), as bidirectional power switch in the three legs of the converter. The board is also equipped with on board auxiliary power supply, based on high voltage smart IC for flyback converter, VIPer26K[6] to obtain a self-provided isolated dual output (12V – 7V). The sensing circuits needed by the control unit are integrated in the battery charger board displayed in Fig.7.15. A high power 3-phase AC source is used to emulate the main grid, while a high power DC electronic load is used as load. A precision Network Power Analyzer has been connected to monitor the power quality of the electrical quantities.

Experimental tests have been carried out on the 3LVR to verify the feasibility of the proposed control solution during transient and steady state operations. Fig.7.16 shows the start-up of the power converter, the pre-charging operation of the DC link capacitors via a passive current limiter circuit and the burst packet can be noted. Then, an active charging is performed to increase the dc-link voltage to the rated value. Finally, a load step is applied to verify the effectiveness of the Power Factor Controller (PFC) control. The active rectifier is operated according to the working conditions listed in Table.7.2 .

$V_{AC_{ph,n}}$	230 V_{rms}
I_{ACref}	17.5 A_{rms}
f_{sw}	70 kHz
L_{AC}	514 μH
R_{eqL}	20 mΩ
I_{satL}	26A
I_{Load}	15A
f_{AC}	50 Hz
S_{AC}	12 kVA

Table 7.2: Vienna Rectifier working conditions

fig. 7.22 displays a sequence of load transients, from no load to full load and back, highlighting the capability of the proposed control method to properly track the load condition even under sudden current transients, still performing the PFC functionality and other load tests has been shown in figs. 7.17 to 7.21.

[4]STMicroelectronics - 1200V 20A power Schottky silicon carbide diode.

[5]STMicroelectronics - SiC Power MOSFET, 650 V, 45 A,55 mΩ(typ., TJ=25°C) in an HiP247 package.

[6]STMicroelectronics - High voltage converter Fixed frequency VIPer^{TM} plus family 60kHz.

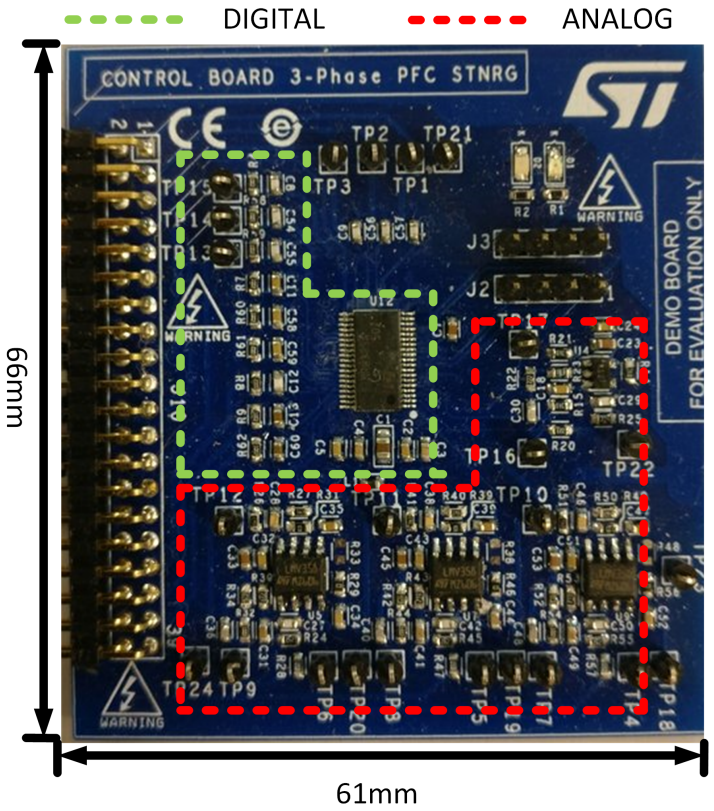


Figure 7.14: Prototype of the control board used in the proposed mixed-signal control architecture

In Fig.7.23 an overview of analog current regulator signals is shown. In particular, the last plot, the behaviors of the signal are in according with the PFC mode of the regulator and the scale factor of the analog circuit that changes the signal to be compliant with the remaining parts.

Addressing the steady state of the experimental test shown in Fig.7.23, the measured Total Harmonic Distortion (THD) of the phase currents is equal to 4,7%, while the power factor is equal to 0.992 and the efficiency is about 98,4%. Fig.7.24 displays the efficiency and Fig.7.25 the power factor curves vs the DC output power, with constant DC output voltage.

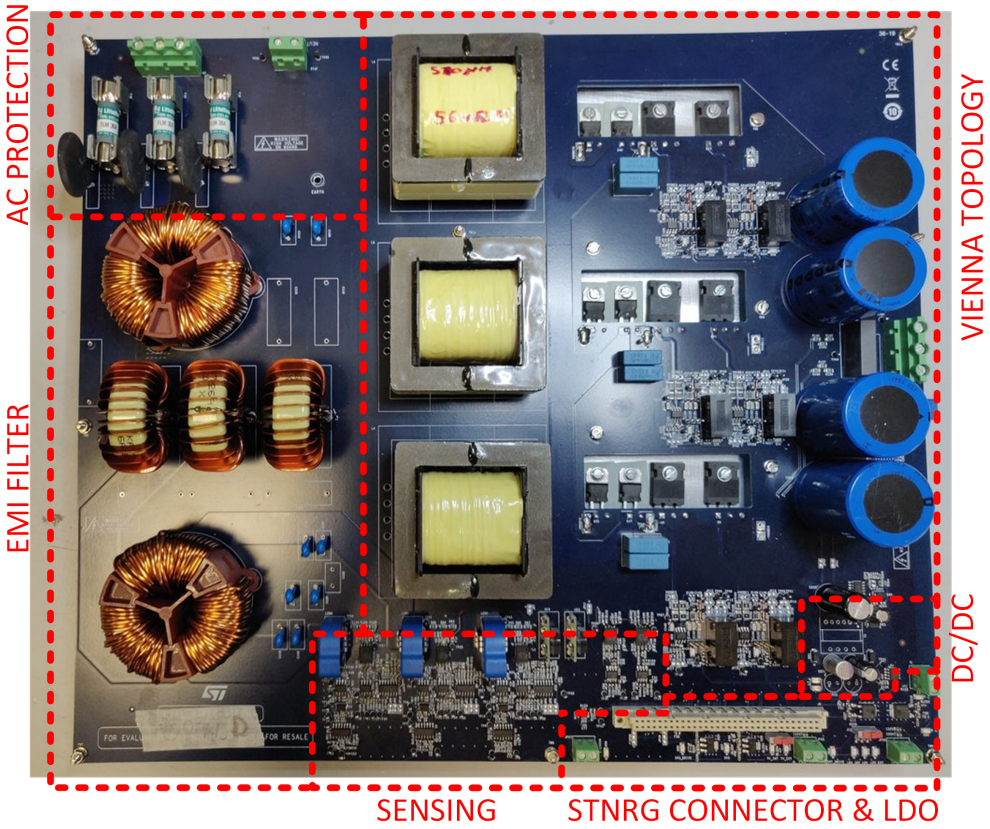


Figure 7.15: Battery Charger Prototype

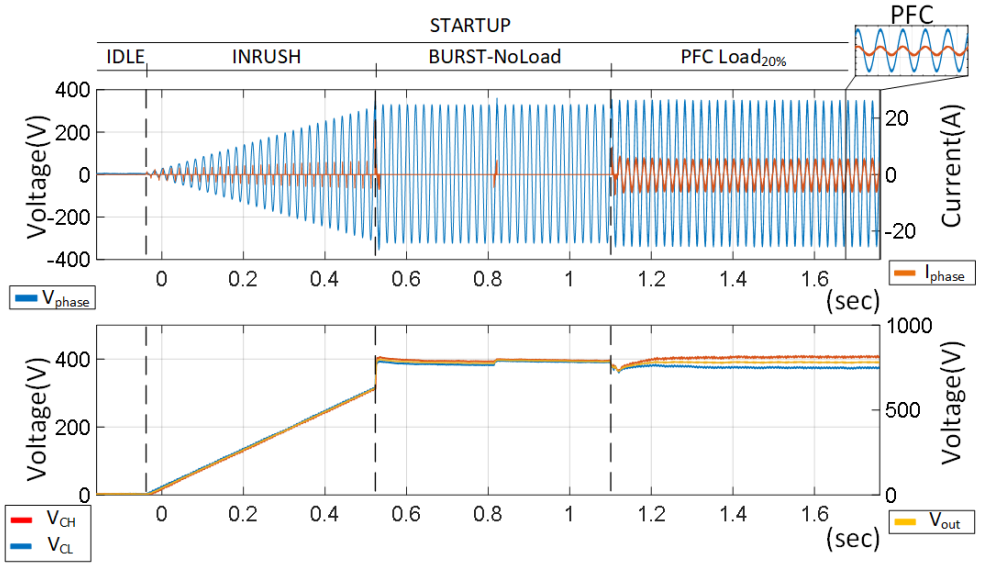


Figure 7.16: Startup followed by a 20 load step.

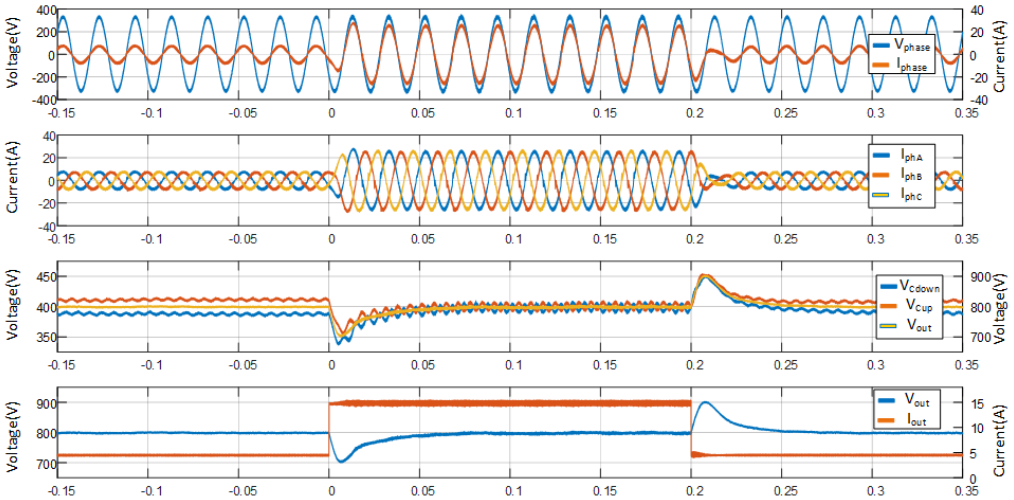


Figure 7.17: Test PFC step load 30% – 100% – 30%

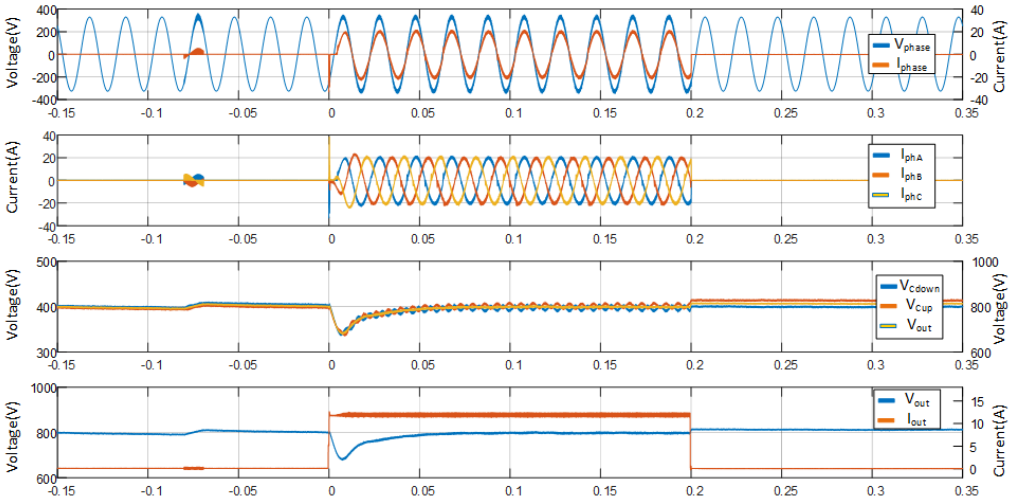


Figure 7.18: Test PFC step load 0% – 80% – 0%

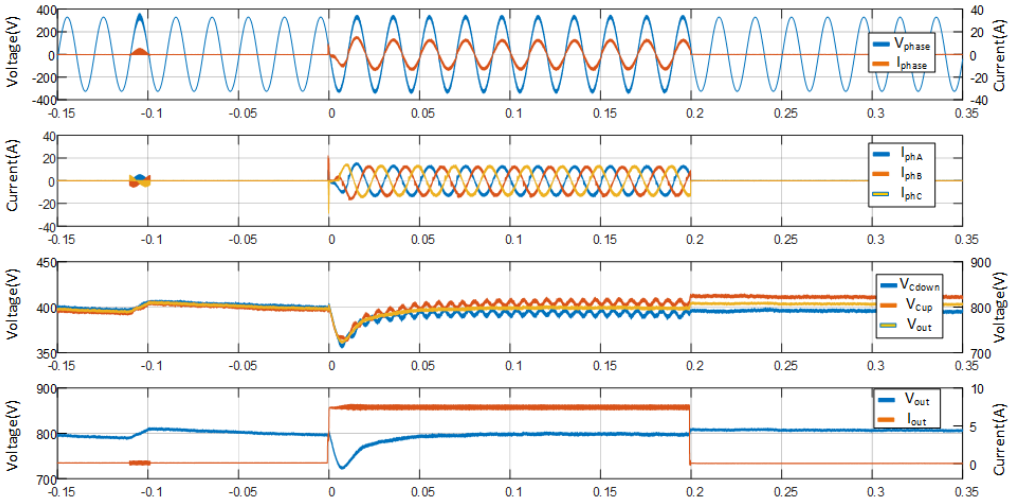


Figure 7.19: Test PFC step load 0% – 50% – 0%

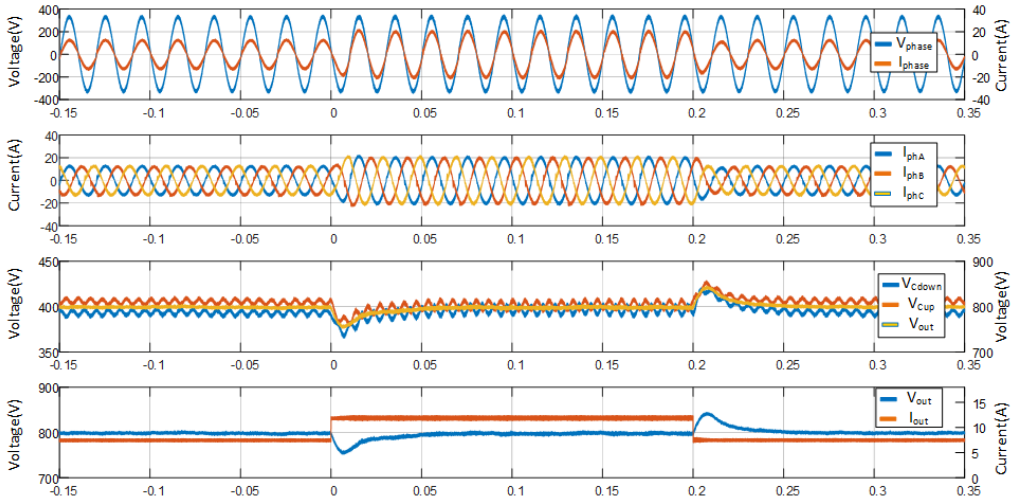


Figure 7.20: Test PFC step load 50% – 80%50%

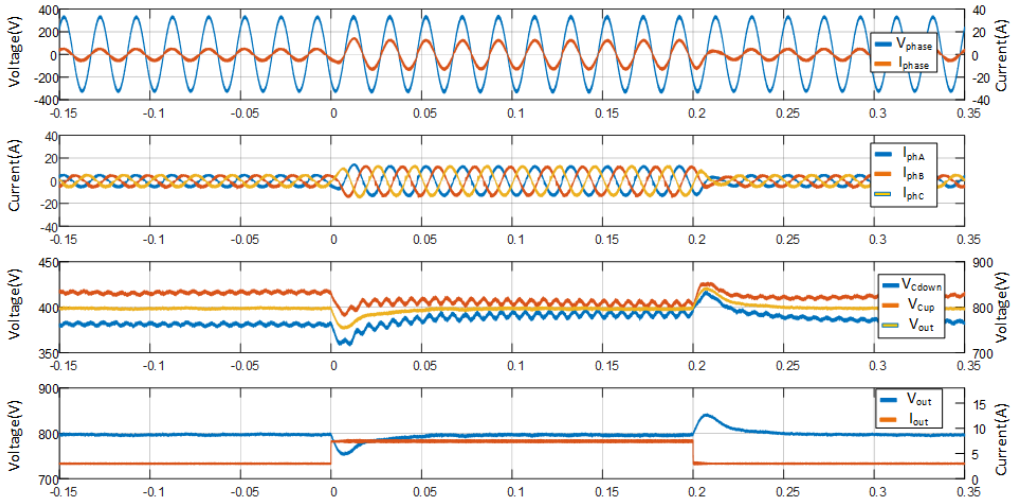


Figure 7.21: Test PFC step load 20% – 50% – 20%

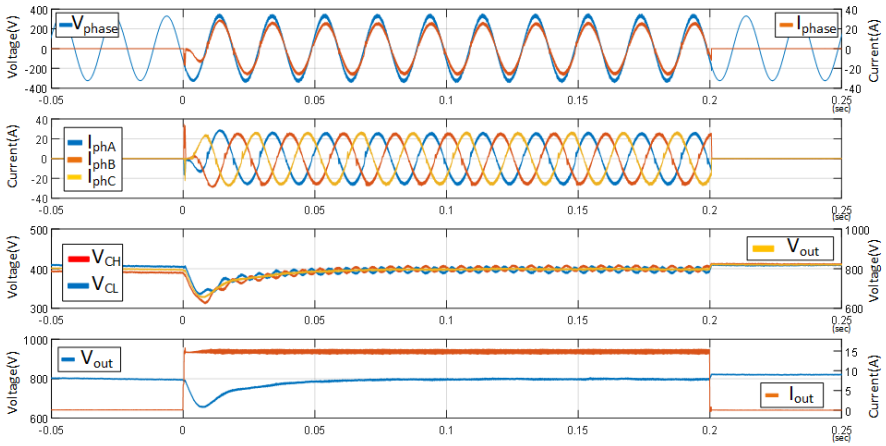


Figure 7.22: Sequence of load tests: zero load - full load – zero load

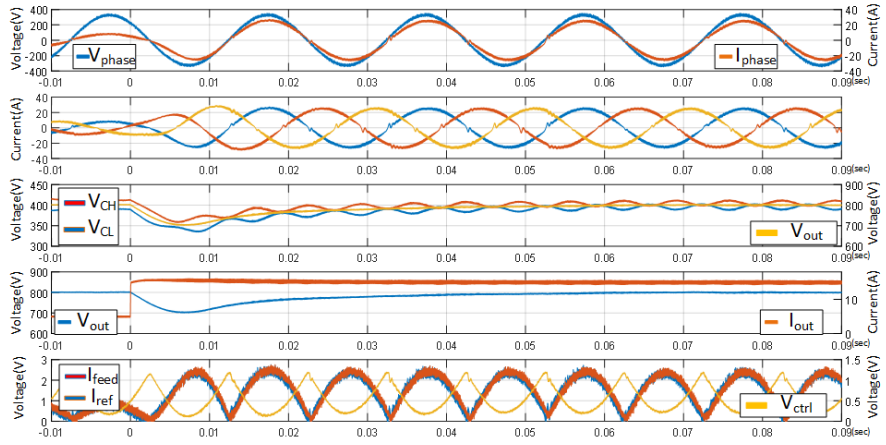


Figure 7.23: Overview of current control analog signal during a load transient.

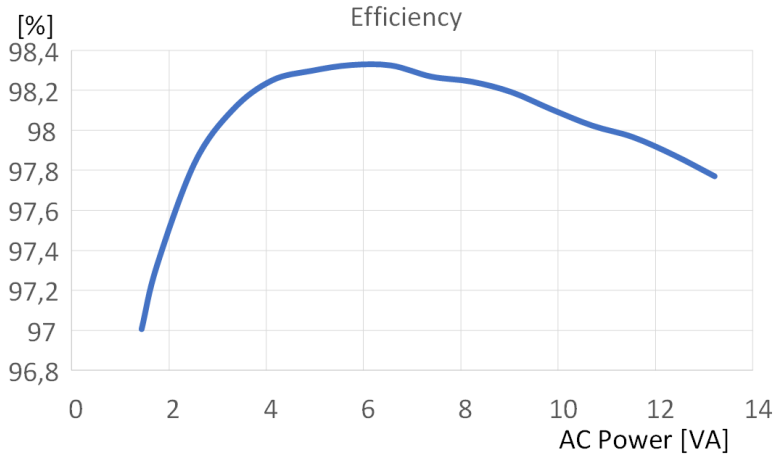


Figure 7.24: Figure of merit of converter efficiency and PF at 400VAC-LL IN and 800VDC OUT.

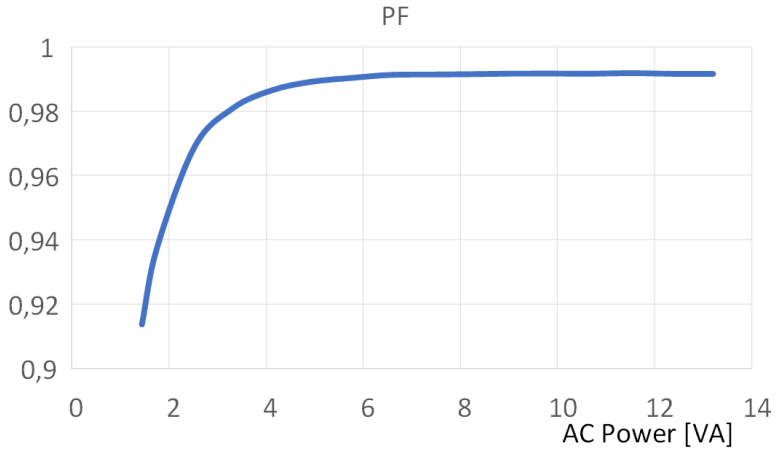


Figure 7.25: PF of converetre

7.2 SiC 3Phase Multilevel converter based on high performance mixed-signal MCU for bidirectional Vehicle to Grid automotive applications in SiC technology

This chapter describes some details of the realization of a prototype electronic power converter consisting of a three-phase topology with three levels, better described and analyzed in (Chap.3.3.2). The objective of this development study concerned the use of a latest-concept micro-controller (STM32G474[7]) which integrates a mixed signal structure (more details in Chap.7.1.1) to obtain a converter with the characteristic of managing energy flows in both directions (Vehicle-to-Grid (V2G)) using vectorial techniques with high computational resources in order to to achieve optimal results in terms of energy efficiency and power quality. The converter specifications are shown in the Tab.7.3 and in Fig.7.26 the principle diagram of the conversion is shown.

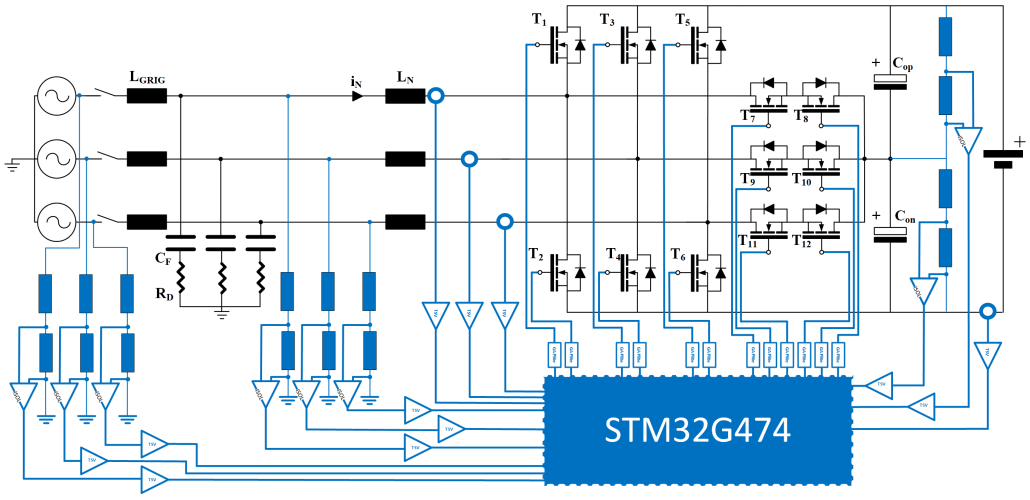


Figure 7.26: Bidirectonal MLC Schematic

The Prototype power board is shown in Fig.7.27, in the left side there is the front-end part composed by thermal and fuse protection, the grid connection relay, the AC-sensing and the LCL filter, im the right side are positioned the controlled switches, the control connector, DC bus with sensing and the auxiliary power supply in Fig.7.28 is shown the prototype control board in witch is found the MCU and the analog protection circuit.

[7]STMicroelectronics - STM32G4 Series of mixed-signal MCUs with DSP and FPU instructions.

$V_{AC_{ph,n}}$	230 V_{rms}
I_{ACref}	21 A_{rms}
f_{sw}	100 kHz
L_{AC}	505 μH
R_{eqL}	20 mΩ
I_{satL}	26A
I_{Load}	19A
f_{AC}	50 Hz
S_{AC}	15 KVA

Table 7.3: Bidirectional Multi Level Converter (MLC) working conditions

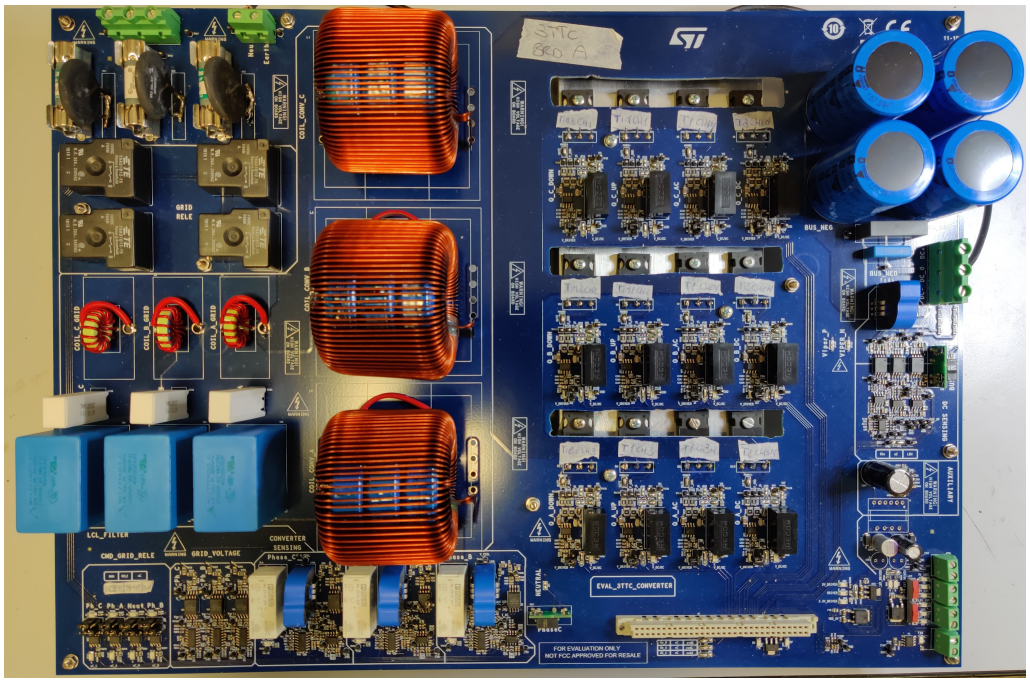


Figure 7.27: Bidirectional Power Board

7.2.1 Specification of the prototype

7.2.2 Control strategy

In according to Chap.3.4 a Voltage Oriented Control (VOC) was implemented to obtain the bidirectional behavior control and the schematic block is shown in 7.29 for the AC to DC energy flow and 7.30 for the DC to AC energy flow.

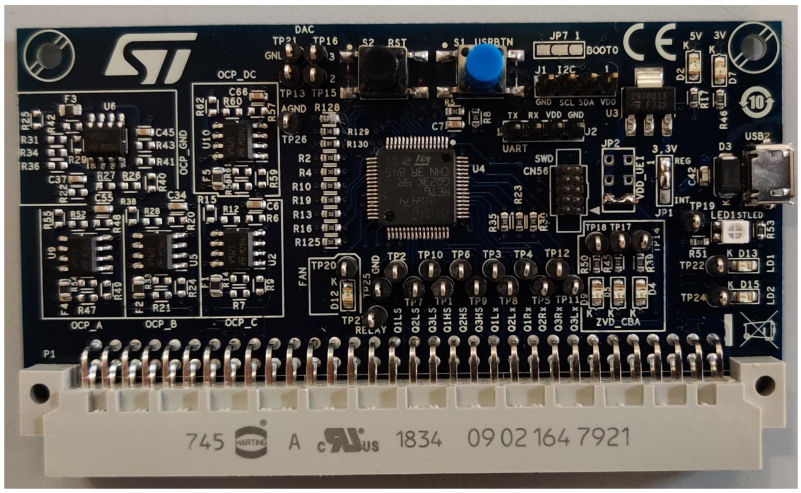


Figure 7.28: Control board

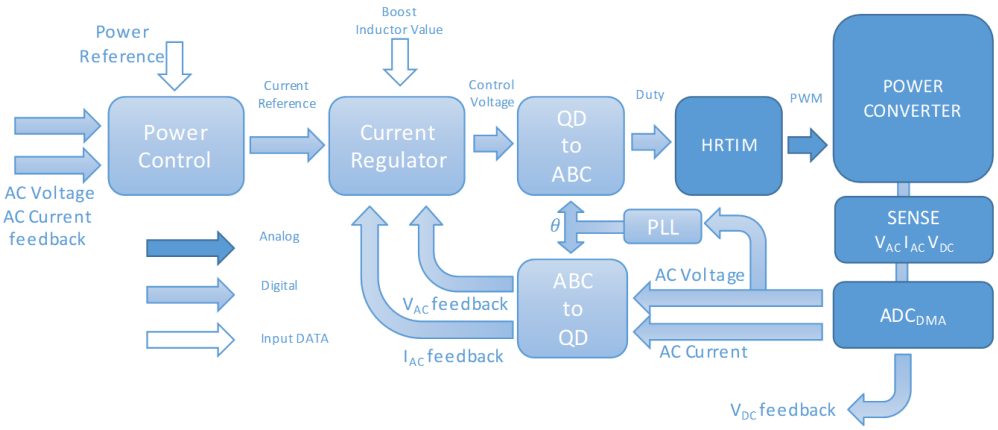


Figure 7.29: G2V control structure

7.2.3 Software development

Shown in the Fig.7.31 is the structure of the code implemented in the microcontroller, the development was based on the concept of creating a structure with levels so as to be able to lay the foundations of a library dedicated to digital power that is not strictly linked to the microcontroller used and which can be integrated with all the application skills for the various power converters. The structure consists of:

1. **API layer** Application Programming Interface dedicated to Digital Power Control (linked to the application)

2. **Peripheral layer** Interface for the use of microcontroller devices (linked to the MCU)

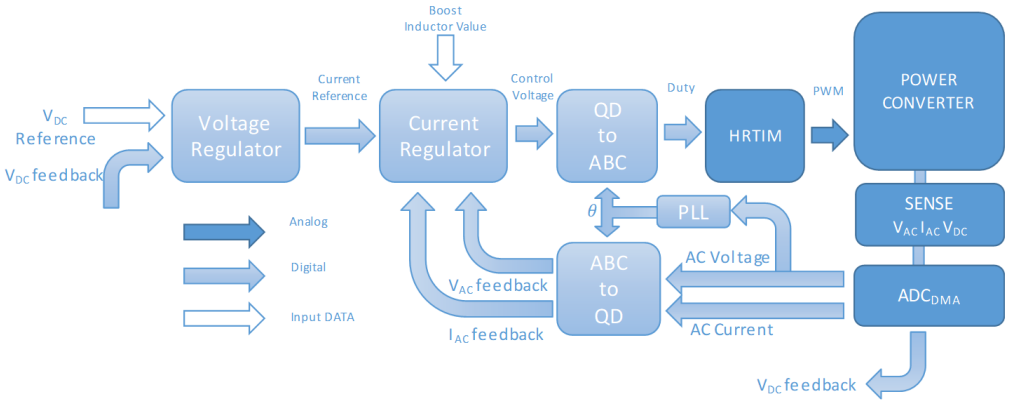


Figure 7.30: V2G control structure

3. **Bridge layer** Interface for the cooperation with the I/O from DATA Layer (linker MCU-Application)

4. **DATA layer** Storage of the raw and processed data

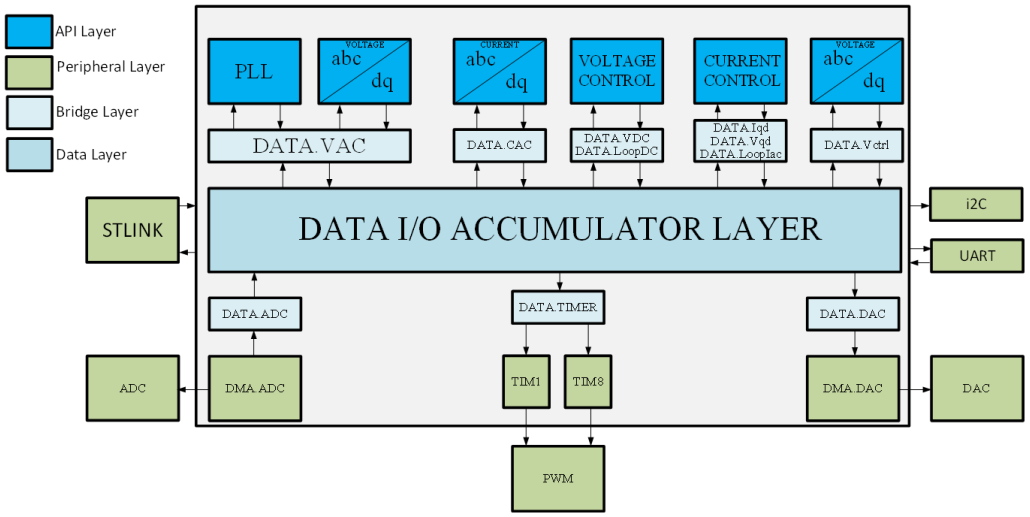
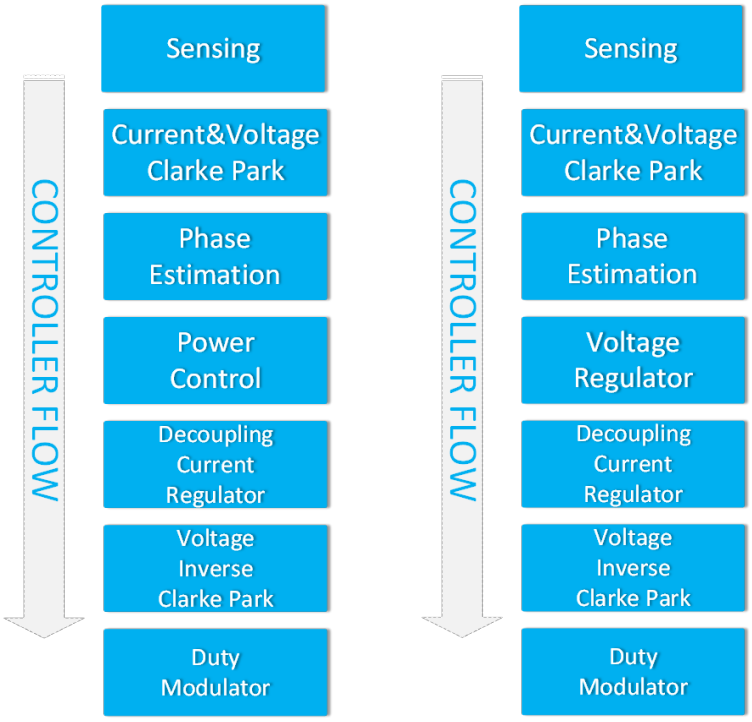


Figure 7.31: Librarystructure

The VOC control process is represented in the flow diagram of Fig.7.32.



(a) V2G (b) G2V

Figure 7.32: Bidirectional MLC Flowchart.

7.3 Bidirectional SiC-based Battery Charger for V2G applications

This work deals with the study of a bidirectional battery charger with SiC-MOSFETs devices, from the design, modelling and simulation stages to the realization of a laboratory prototype. The battery charger consists of a high efficiency 5 kW single-phase bidirectional power converter suitably designed for Grid-to-Vehicle (G2V) and V2G applications. It is composed by two stages: an AC/DC PFC Synchronous converter and a insulated DC/DC Dual Active Bridge (DAB) modulated in phase-shift. Due to the increasing number of Plug-in Hybrid Electric Vehicle (PHEV) and Hybrid-Electric Vehicle (HEV) connected to the distribution system, smart onboard and off-board Bidirectional Battery Chargers (BBC) are becoming essentials components for managing the energy flows between the vehicles and the AC mains. Recently, BBC have been also designed for V2G applications, as utilizing energy storage in EVs leads beyond any doubt to economic and environment benefits. Several bidirectional battery chargers have been treated in literature,(Chap.3.2) [81, 123–126] in an effort to provide a compact, efficient and cheap solution.

The converter investigated in this activity is a 5 kW singlephase BBC based on two conversion stages: an Active Front End (AFE) PWM Rectifier connected to the utility grid,

cascade connected to a DAB isolated converter. Such architecture has been adopted for its strengths as bidirectional power flow, galvanic isolation, high efficiency in a wide operating range and reduced size and weight due a significant increasing of the switching frequency thanks to the use of SiC MOSFETs power devices (Chap.2.3) [127]. The connection to the utility grid is accomplished with a PFC. Design, modelling and simulations have been performed to evaluate the feasibility and the performance of the considered BBC in a wide operating range.

Bidirectional Battery Charger Design As shown in Fig.7.33, the power conversion topology investigated in this study is a single-phase SiC-based converter. The converter consists of two conversion stages. The first stage is the AFE which is connected to the grid through a LCL filter, while the second stage is realized via a DAB.Phase Shift modulation has been used in the DAB stage, consists in the implementation of the control algorithm that set the phase shift between the switching signals of the two legs while maintaining the duty cycle of every switching pattern equal to 50%. During the G2V mode the phase shift is controlled in order to let the energy flow towards the battery. On the contrary, a suitable opposite phase shift is imposed to the control signals when the converter works in V2G mode when the energy flow is directed from the battery to the AC grid.

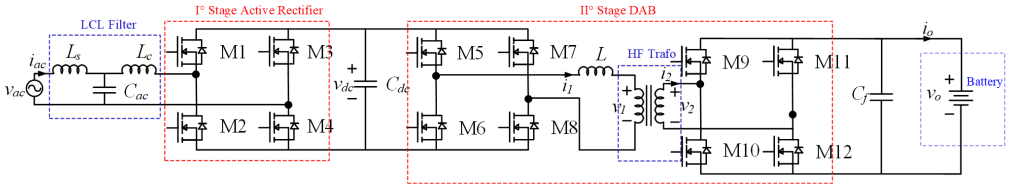


Figure 7.33: Converter topology.

Active front-end Rectifier The AFE, or Synchronous Rectifier, is connected via a filter to the utility grid and it performs the AC/DC conversion with the power factor correction. It is a SiC-based H-Bridge converter. A bipolar PWM has been implemented, whose switching frequency is fixed at $f_sw = 100kHz$, while the modulating signal is elaborated from the knowledge of the voltage grid angle implementing a grid synchronization algorithm. The gate signals used to control the SiC MOSFETs are obtained from the current control loop. The high switching frequency has been selected as the best compromise between power density and efficiency. Moreover, a suitable switching frequency can lead to a reduction of the passives composing the AC grid filter and the DC bus link. The LCL structure of the filter has been selected since it provides a higher attenuation of switching harmonics with lower passive element values, obtaining a smaller filter volume in comparison with other solutions. The technical specification of the filter parameters, DC bus link and grid operating conditions considered in the following analysis are listed in Table.7.4.

Dual Active Bridge The DAB is the DC/DC isolated bidirectional converter of the BBC. The DAB topology has been selected because of its high efficiency in a wide range of

Parameter		Value
RMS voltage grid V_{AC}		230 V
Grid frequency f_{AC}		50 Hz
Filter parameters	L_C	1.5 µH
	C_{AC}	10 µF
	L_S	325 µH
DC Capacitor C_{DC}		4 mF
Switching frequency f_{sw}		100 kHz

Table 7.4: Technical specification of the filter parameters and grid operating conditions.

operating range [128]. It features a symmetrical structure, characterized by two full bridges connected via a high frequency transformer used to provide the galvanic isolation. The first H-Bridge produces a square-wave voltage with a 50% of duty cycle in the primary side of the transformer. The second H-Bridge performs the AC to DC conversion and implements the current control loop necessary to provide the appropriate current charging profile to the battery. The leakage inductance L_{lk} plays a key role in the effectiveness of the power conversion. Even the DAB is realized with SiC power MOSFETs. Among the several modulation strategies suggested in literature, a Single-Phase Shift Modulation has been used to control the power exchanged between the BBC and the main grid.

The phase shift (ϕ) is defined positive when the power flows from the grid to battery, and negative when the power flows in the opposite direction. The relation between the phase shift and the delivered power is given according to [129] in (7.6) where $-90° < \phi < 90°$, V_1 and V_2 are the transformerś voltages, n is the transformer turn ratio, f_s is the switching frequency and L is the leakage inductance. Hence, for a specific active power P, the phase shift ϕ that must be imposed between the input-output voltages is given by (7.7)

$$P = \frac{nV_1V_2\phi(\pi - |\phi|)}{2\pi^2 f_{sw} L} \tag{7.6}$$

$$\phi = \frac{\pi}{2}\left[1 - \sqrt{1 - \frac{8f_{sw}L\,|P|}{nV_1V_2}}\right] sgn(P) \tag{7.7}$$

The design specifications of the DAB of the analyzed BBC are listed in Table.7.5.

High Frequency Transformer The high frequency transformer is responsible for the power transfer and for the galvanic isolation [130]. Different core geometries and materials are widespread, and the selection of the most appropriate solutions depends on the kind of application. It is well known that high frequency reduces the core dimensions, and exploiting the ferrite materials involves negligible eddy currents losses. The design method is based on the "core geometry method" [131, 132]. For this bidirectional converter the EE core geometry has been chosen with N87 material. This choice is related to the high

Parameter		Value
Nominal input Voltage	V_{DC}	400 V
Nominal output voltage	V_O	400 V
Minimal output voltage	$V_{O,min}$	150 V
Output Power	P_{Out}	5 kW
Duty Duty Cycle	D	50%
Switching frequency	f_{sw}	100 kHz

Table 7.5: DAB design specifications.

switching frequency ($f_{sw} = 100kHz$) and high-power density to which the transformer is subjected. The transformer characteristics are listed in Table 3.

Parameter		Value
Nominal input Voltage	V_{pri}	400 V
Maximum Input Voltage	$V_{pri,max}$	480 V
Minimum Input Voltage	$V_{pri,min}$	360 V
Input current	I_{pri}	22 A
Nominal output Voltage	V_{sec}	400 V
Output current	I_{sec}	17.5 A
Switching frequency	f_{sw}	100 kHz
Regulation	α	0.15%
Max operating flux density	B_m	$0.16T$
Duty Cycle	D	50%
Maximum temperature rise	T_r	70 °C

Table 7.6: High frequency transformer parameters.

Converter modelling, and simulation Modelling of the BBC, with its closed control loop have been performed in Matlab Simulink®in order to simulate its behaviour and evaluate its performances under different working conditions. The converter model includes the parasitic elements that affects each power conversion stage. The MOSFETs parameters have been taken into account as well as the dead-time between each leg switches. The closed loop control block diagram for the AC/DC PFC converter is shown in Fig.7.34.

Using the Park's transformation (appendix A), the regulation is implemented using the i_d and i_q currents to control, respectively, the active and reactive power. Moreover, this control structure allows to regulate the DC voltage and the power factor. During G2V mode the AFE with power factor correction works as AC to DC converter, and it charge the battery, maintaining constant DC voltage and unitary PF. In V2G mode it discharges the battery and acts as DC/AC inverter, maintaining constant voltage on the bus-dc and

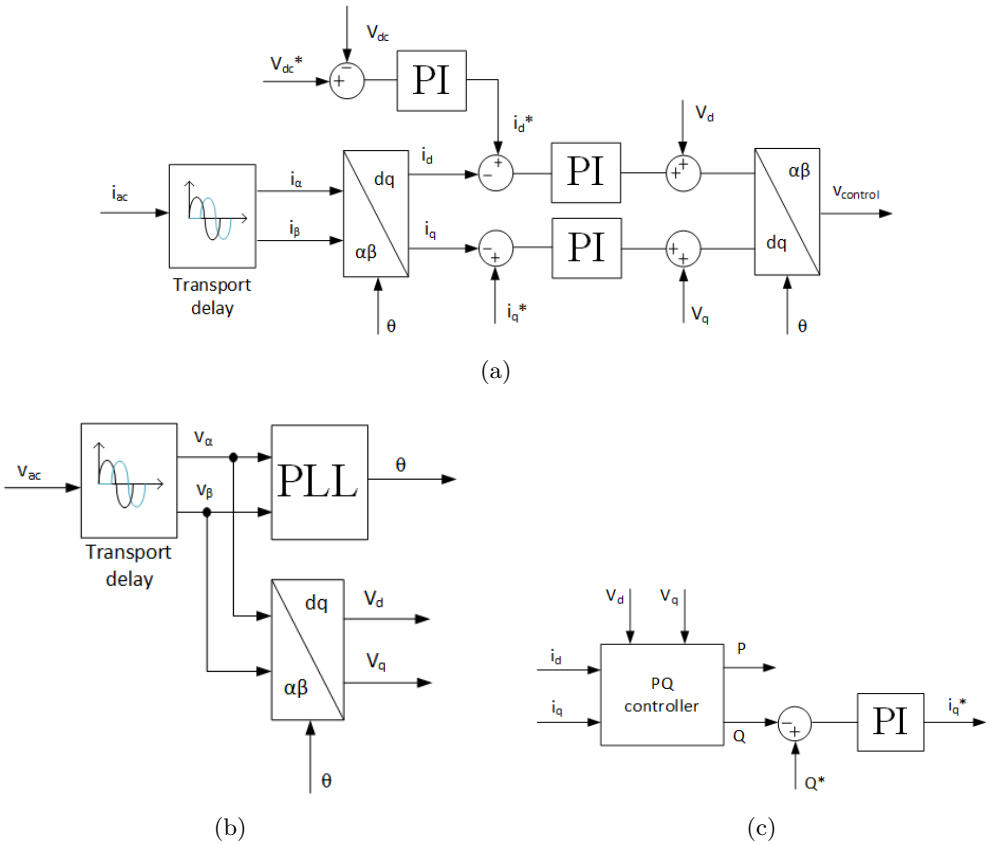


Figure 7.34: AFE PFC closed loop control block diagram

managing the power factor to compensate the amount of reactive power required by the grid. The control loop block diagram for the DAB is shown in Fig.7.35.

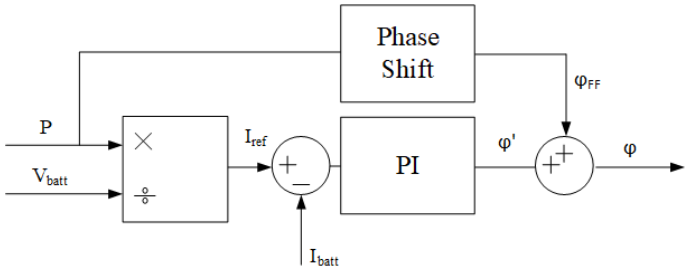


Figure 7.35: Phase Shift control loop block diagram

The required power from the converter will acts on the phase shift, and by varying this reference it will be possible to reverse the power flow. The simulation waveforms during the G2V mode are shown below. Fig.7.36, shows the first stage waveforms, that are the grid voltage vac and current iac with unitary power factor, and the ripple of the DC

voltage. The THD for the AC current is close to 7%. Voltage and current on the primary side of the transformer are shown in Fig.7.37. The current waveform depends on the phase shift between the two transformer-ends voltages. The secondary side quantities are pretty similar, as the turn ratio n has been chosen equal to one. The leakage inductance L affect the power delivered in the DAB converter. Therefore, the voltage vL waveform is strictly related to the power direction.

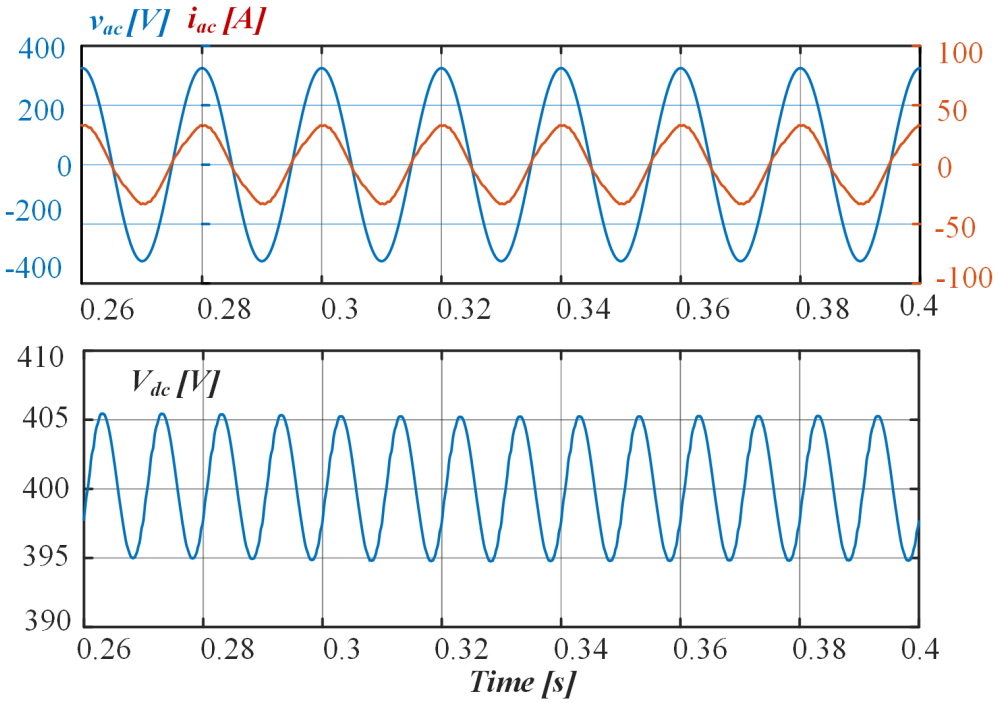


Figure 7.36: Voltage and current of the AC grid and Ripple on the DC side

The DC output waveforms are shown in Fig.7.38 in which the ripple of the voltage V_o and current I_o has been highlighted. During V2G mode the power flows from the battery to the grid to satisfy the power demand. In this case the reference power is modified and it acts on the phase shift, as described before. Transition from G2V to V2G mode, during the t^* instant, requires current inversion as illustrated in fig.7. In this case, the PF has been maintained unitary, that means no reactive power demand.

This inversion affects partially the total harmonic distortion of the ac grid current, with value close to 10%. The main simulation results are summarized in Tab.7.7.

In Fig.7.40 you can see the efficiency of the entire power conversion system related to the output power, performed for some simulations results.

Battery Charger Prototype and Experimental Results The prototype of the converter has been designed and realized in order to test the performance and efficiency of

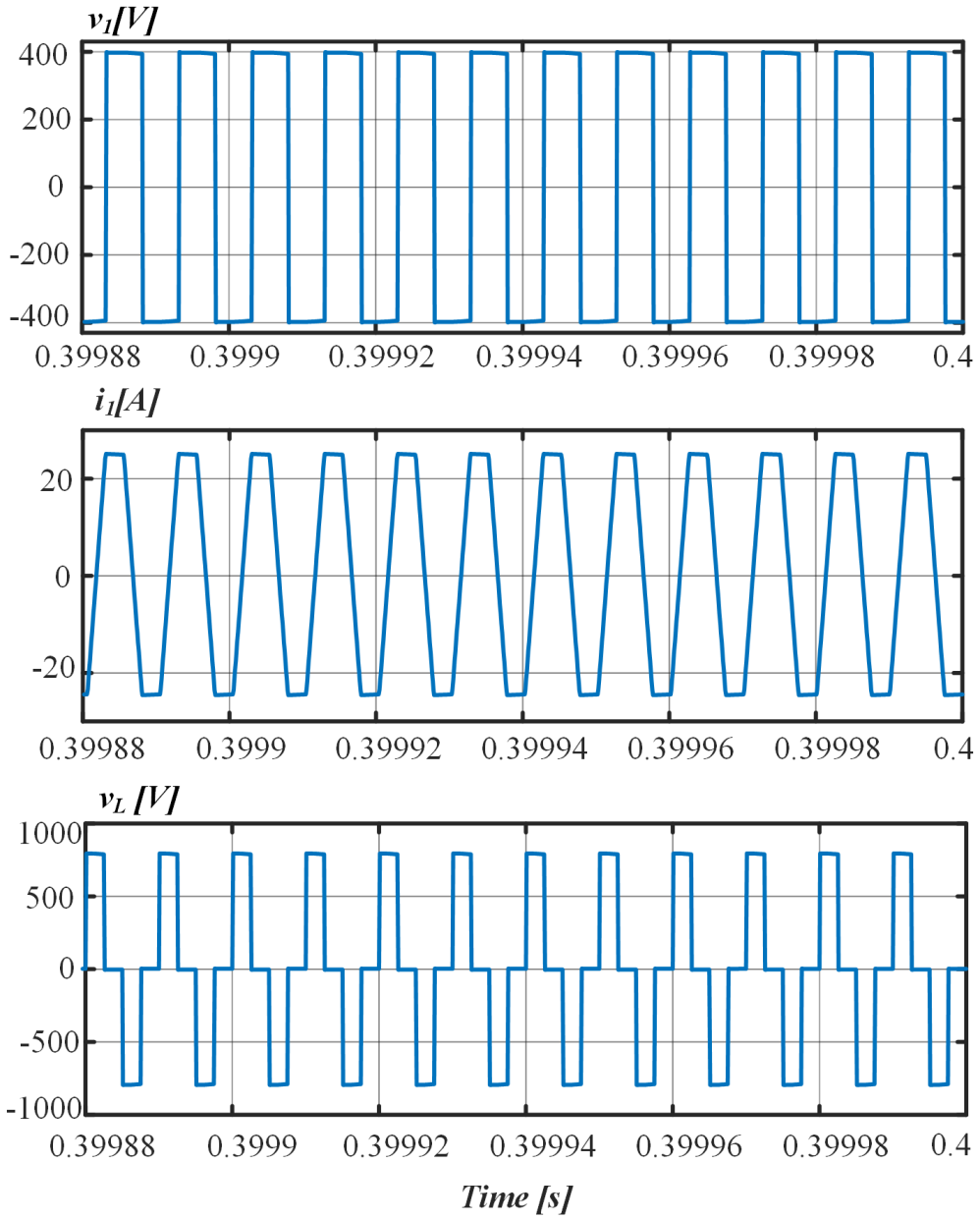


Figure 7.37: Voltage and current on the primary side of the transformer, and inductance voltage.

this bidirectional battery charger. SiC MOSFETs have been used with voltage rating of 1200 V and current of 45 A. Modern microcontroller STM32G474[8] has been employed to

[8]STMicroelectronics - STM32G4 Series of mixed-signal MCUs with DSP and FPU instructions.

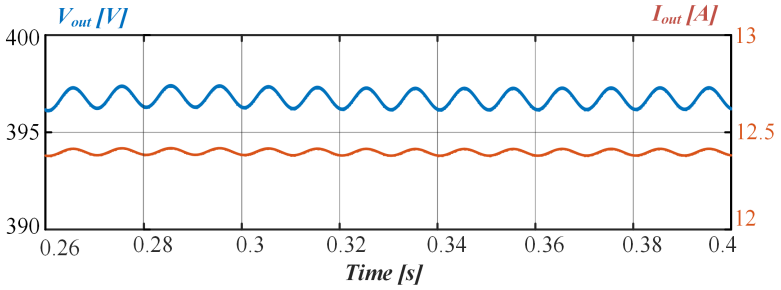


Figure 7.38: Ripple on the DC output Voltage and Current

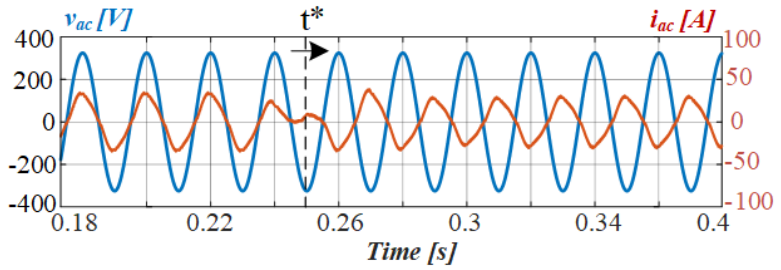


Figure 7.39: AC voltage and current from G2V to V2G mode

generate the digital control signals that are sent to the Gate via optical fiber. The microcontroller exploits the advanced internal timer, in master-slave mode, to obtain the phase shift modulation and manage the dead-time in the leg switches. This allows to realize

Parameter		**Value**
RMS grid voltage	$V_{AC_{rms}}$	230 V
RMS grid current	$I_{pri,max}$	22.6 A
Average Bus DC Voltage	V_{DC}	403 V
Average output voltage	V_O	397 V
Average output current	I_O	12.4 A
Input Apparent Power	S	5.2 kV A
Input Active Power	P_{AC}	5.2 W
Bus DC Power	P_{DC}	5.03 W
Output Power Po	P_O	4.91 W
Power Factor	PF	0.999
AFE efficiency	$\eta_{AFE} = P_{DC}/P_{AC}$	96.7%
DAB efficiency	$\eta_{DAB} = P_O/P_{DC}$	94.42%
Total efficiency	$\eta = P_O/P_{AC}$	94.26%

Table 7.7: Simulation results.

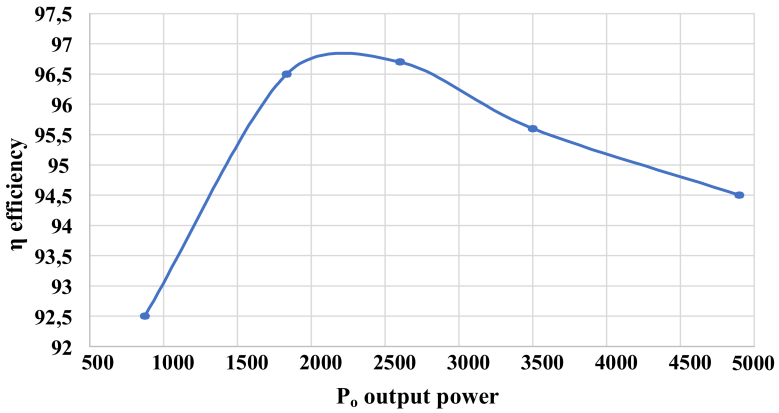


Figure 7.40: Efficiency

more compact and robust solutions for the entire experimental system. The experimental converter has been realized, as shown in Fig.7.41, and preliminary tests have been carried out with low power levels. This BBC is actually under test.

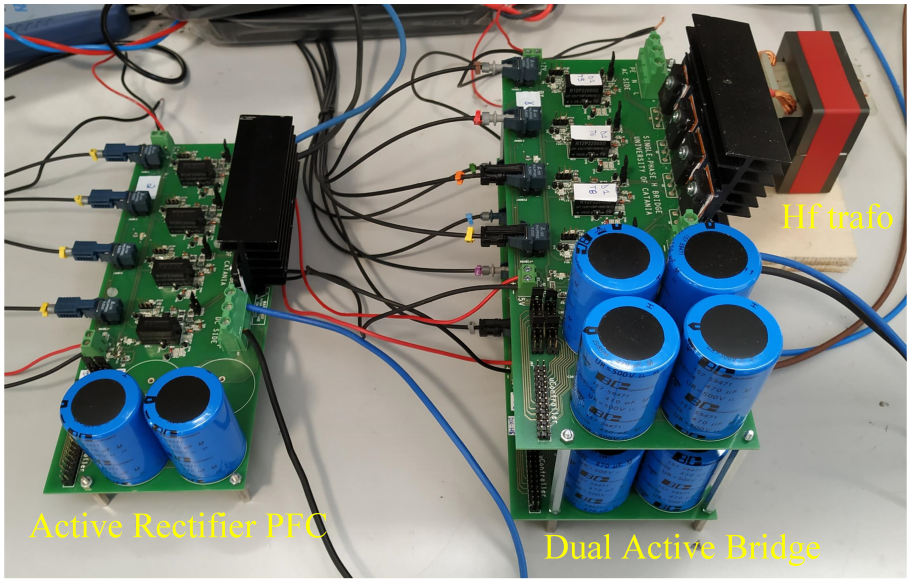


Figure 7.41: Experimental prototype of the BBC

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Appendix A

Notes on the generalized theory

In general, rotating electrical machines can be seen as the set of an electromagnetic system (described by means of equations of voltage) and a mechanical system (described in terms of equations of torque). They are studied considering the mutual interactions between the winding of stator and rotor, viewed as circuits ohmic-inductive: such interactions are variable with time and with the relative position between rotor and stator. Also, the machine is modeled by referring to a three-phase system Real, constituted by a set of three coplanar axes abc phase-shifted by 120°. This approach can be generalized to all rotating machines, both in direct current and in alternating current (synchronous and asynchronous machines). Throughout the history and development of electric machines several researchers (from Park in the first half of the 900') have tried to construct a new method of simplifying the equations of electrical machines. The new approach exploits simply a change of the reference system: it goes, that is, from the real system of the machine to a fictitious system (in which the machine is abstract) realized by means of a set of three axes *qdo* arranged in the space and orthogonal to each other. In particular, the *axes q* (quadrature) and *axes d* (direct) lie on the plane determined by the three-abc, and rotate in the counterclockwise direction around the *axis 0*. In 1965 researchers Krause and Thomas showed that one single transformation of this type can be applied , in general, to all the electrical machines, specifying, case by case, the relative speed of rotation between the two sets of axes. For this character of "general", this treatment is called the theory of arbitrary references; its beauty is that it has its own validity mathematics and a precise geometric meaning. Algebraically, the transformation can be expressed in matrix form as in eq. (A.1) or, in compact form, as in eq. (A.2)

$$\begin{bmatrix} f_{qx} \\ f_{dx} \\ f_{0x} \end{bmatrix} = \frac{2}{3} \begin{bmatrix} cos\gamma_x & cos\left(\gamma_x - \frac{2}{3}\pi\right) & cos\left(\gamma_x + \frac{2}{3}\pi\right) \\ sin\gamma_x & sin\left(\gamma_x - \frac{2}{3}\pi\right) & sin\left(\gamma_x + \frac{2}{3}\pi\right) \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \begin{bmatrix} f_{ax} \\ f_{bx} \\ f_{cx} \end{bmatrix} \tag{A.1}$$

$$f_{qd0x} = K_x f_{abc_x} \tag{A.2}$$

where are indicated with f_{abc_x} the vector of the components along the axes of the generic *abc* magnitude f speed rotary ω_x and with f_{abc_x} the vector of the components

along the axes of the generic $qd0$ magnitude f rotating speed ω, while the angle γ_x is expressed in eq. (A.3)

$$\gamma_x = \theta_x - \theta = \theta_x(0) + \int_0^t \omega_x(t)dt - \theta(0) - \int_0^t \omega(t)dt \tag{A.3}$$

where they are indicated with θ_x and θ, respectively, the angles generated during the rotation of triple abc_x and the triad $qd0_x$ in time t. The subscript "$_x$" in the sizes remembers precisely the "generality" of this transformation. It is possible to define an inverse transformation, using the inverse matrix K_x in eq. (A.4) or in compact form, similar to the direct transformation in eq. (A.5)

$$\begin{bmatrix} f_{ax} \\ f_{bx} \\ f_{cx} \end{bmatrix} = \begin{bmatrix} cos\gamma_x & sin\gamma_x & 1 \\ cos\left(\gamma_x - \frac{2}{3}\pi\right) & sin\left(\gamma_x - \frac{2}{3}\pi\right) & 1 \\ cos\left(\gamma_x + \frac{2}{3}\pi\right) & sin\left(\gamma_x + \frac{2}{3}\pi\right) & 1 \end{bmatrix} \begin{bmatrix} f_{qx} \\ f_{dx} \\ f_{0x} \end{bmatrix} \tag{A.4}$$

$$f_{abc_x} = K_x^{-1} f_{qd0_x} \tag{A.5}$$

By having this theory a mathematical meaning autonomous carriers f can represent either any size. Finally, in fig. A.1 shows the geometric representation of this transformation, ie the graphical relationship between the triads of $axesabc$ and $qd0$ (the axis 0 is not graphically represented, as emerging from the plane of the figure).

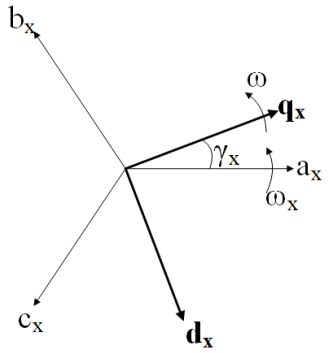


Figure A.1: Geometric representation of the theory of arbitrary references

A.1 Application to three-phase electrical systems

Until this point the theory of the references arbitrary was presented as a simple change of reference system: this step in itself does not represent a step forward in the simplification of the study of the electrical systems. Firstly it is essential to consider that, in case of electrical three-phase balanced (magnitudes mutually out of phase by 120°) and symmetrical (sizes equal in magnitude), the component vector along the *axis 0* is canceled. In fact, from

eq. (A.1) take eq. (A.6), If the system is symmetrical and balanced three-phase abc, namely in eq. (A.7) the eq. (A.6) becomes eq. (A.8).

$$f_{0x} = \frac{1}{2}\left(f_{ax} + f_{bx} + f_{cx}\right) \tag{A.6}$$

$$f_{ax} + f_{bx} + f_{cx} = 0 \tag{A.7}$$

$$f_{0x} = 0 \tag{A.8}$$

This result represents a first great advantage in the application of the general theory: a three-phase abc symmetrical and balanced may be reduced to a system of two mutually perpendicular axes. So far, moreover, with f it denotes a generic vector quantity; specifically, this discussion can be applied to all the operational variables of an electric power system (voltages, currents, magnetic fluxes, powers, etc.). Below, consider the voltage vector. It has been said can un a general transformation can be detailed by specifying, in each case, the relative speed between the two systems, or, similarly, defining the angle γ_x contained in eq. (A.1). In particular, with reference to the description of the control systems and measuring system model GD, it is useful to consider two specific transformations:

- Transformation abc / dq stationary;
- Transformation abc / dq synchronized with the pulse of your network, or simply synchronous.

In case of transformation stationary, the relative speed of rotation between the two reference systems is zero and, consequently, they cancel the integrals in eq. (A.3). If, in addition, are considered coincident axes a e q (very used in practice) you can get the angle γ_x is zero. Then, considering the voltage vectors and eliminating the component called along the *axis* 0, the transformation eq. (A.1) in this case becomes eq. (A.9)

$$\begin{bmatrix} v_q \\ v_d \end{bmatrix} = \frac{2}{3}\begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & -\frac{\sqrt{3}}{2} & \frac{\sqrt{3}}{2} \end{bmatrix}\begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} \tag{A.9}$$

In synchronous processing instead it is considered fixed in the system qd ($\omega = 0$) while the system abc rotates with constant speed $\omega_x = \omega_e$. Consequently, the angle to be included in the transformation matrix K_x is (eq. (A.10))

$$\gamma_x \equiv \theta_e = \omega_e \int_0^t dt = \omega_e t \tag{A.10}$$

Then, in the case synchronous, (considering the voltages and eliminating the component along 0) transformation eq. (A.1) becomes (eq. (A.11))

$$\begin{bmatrix} v_q \\ v_d \end{bmatrix} = \frac{2}{3}\begin{bmatrix} cos\omega_e t & cos\left(\omega_e t - \frac{2}{3}\pi\right) & cos\left(\omega_e t + \frac{2}{3}\pi\right) \\ sin\omega_e t & sin\left(\omega_e t - \frac{2}{3}\pi\right) & sin\left(\omega_e t + \frac{2}{3}\pi\right) \end{bmatrix}\begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} \tag{A.11}$$

Making explicit expressions (eq. (A.9)) and (eq. (A.11)) can make further considerations. Therefore, consider a generic set of three voltages symmetrical and balanced pulse amplitude V and $\omega_e = 2\pi f_e$ obtain eq. (A.12))

$$\begin{aligned} v_a &= V cos\omega_e t \\ v_b &= V cos\Big(\omega_e t - \tfrac{2}{3}\pi\Big) \\ v_c &= V cos\Big(\omega_e t + \tfrac{2}{3}\pi\Big) \end{aligned} \tag{A.12}$$

fig. A.2a shows the voltage eq. (A.12) with $230Vrms$ amplitude and frequency $50Hz$. Applying the transformation stationary (eq. (A.9)) to abc 3-phase terms eq. (A.12) are obtained in eq. (A.16) and from which, by applying trigonometric formulas obtain eq. (A.14).

$$\begin{aligned} v_q &= \tfrac{2}{3}V\Big\{cos\omega_e t - \tfrac{1}{2}\Big[cos\Big(\omega_e t - \tfrac{2}{3}\pi\Big) + cos\Big(\omega_e t - \tfrac{2}{3}\pi\Big)\Big]\Big\} \\ v_d &= \tfrac{2}{3}\tfrac{\sqrt{3}}{2}V\Big[-cos\Big(\omega_e t - \tfrac{2}{3}\pi\Big) + cos\Big(\omega_e t + \tfrac{2}{3}\pi\Big)\Big] \end{aligned} \tag{A.13}$$

$$\begin{aligned} v_q &= V cos\omega_e t \\ v_d &= -V sin\omega_e t \end{aligned} \tag{A.14}$$

The result in eq. (A.14) shows that by a transformation stationary magnitudes are obtained that have equal amplitude and frequency of the magnitudes abc of origin, and offset by 90° with the component along the q advance. The voltages qd expressed in eq. (A.14) are shown in fig. A.2b. Similarly, by applying the transformation synchronous (eq. (A.11)) the triple (eq. (A.12)) is obtained (eq. (A.15))

$$\begin{aligned} v_q &= \tfrac{2}{3}V\Big[cos^2\omega_e t + cos^2\Big(\omega_e t - \tfrac{2}{3}\pi\Big) + cos^2\Big(\omega_e t + \tfrac{2}{3}\pi\Big)\Big] \\ v_d &= \tfrac{2}{3}V\Big[cos\omega_e t sin\omega_e t + cos\Big(\omega_e t - \tfrac{2}{3}\pi\Big)sin\Big(\omega_e t - \tfrac{2}{3}\pi\Big) + +cos\Big(\omega_e t + \tfrac{2}{3}\pi\Big)sin\Big(\omega_e t + \tfrac{2}{3}\pi\Big)\Big] \end{aligned} \tag{A.15}$$

from which, by applying trigonometric formulas by Werner obtain (eq. (A.16)),

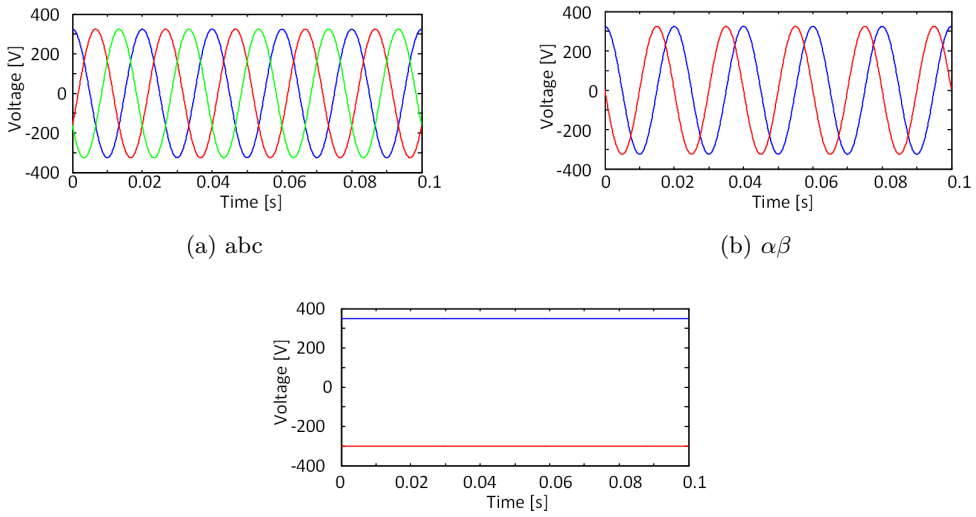
$$\begin{aligned} v_q &= \tfrac{1}{3}V\Big[cos2\omega_e t + cos2\Big(\omega_e t - \tfrac{2}{3}\pi\Big) + cos2\Big(\omega_e t + \tfrac{2}{3}\pi\Big) + 3\Big] \\ v_d &= \tfrac{1}{3}V\Big[sin2\omega_e t + sin2\Big(\omega_e t - \tfrac{2}{3}\pi\Big) + sin2\Big(\omega_e t + \tfrac{2}{3}\pi\Big)\Big] \end{aligned} \tag{A.16}$$

Finally, since the abc terms of origin symmetrical and balanced, the eq. (A.16) becomes eq. (A.17)

$$\begin{aligned} v_q &= V \\ v_d &= 0 \end{aligned} \tag{A.17}$$

The result (eq. (A.17)) shows that by a transformation synchronous with the pulsation of the magnitudes of the network are obtained continuous signals, that is to say constant over time. As obtained allows, ultimately, to transform sinusoidal quantities (variables) in continuous quantities (constants), to great advantage of control techniques that are based on the use of PI regulators (such devices, in fact, work well when the reference to be reached It is constant and not if it varies over time). For this reason, as seen in the

previous chapters, it is necessary that the PLL generates the phase ϑ of the magnitudes of the network, and then use it in the transformations (synchronous) that allow to obtain continuous signals in the feedback loop in the control system. Finally, the voltages expressed in qd (eq. (A.17)) are shown in fig. A.2c.



(a) abc

(b) $\alpha\beta$

(c) dq

Figure A.2: Clarke - Parke example.

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