A 0.3-V 8.5-μA Bulk-Driven OTA

Andrea Ballo, Alfio Dario Grasso, Salvatore Pennisi, and Giovanni Susinni

***Abstract*— A bulk-driven operational transconductance amplifier (OTA) suitable for ultralow-power and ultralow-voltage applications is described. The amplifier exploits local positive feedback in the first stage to increase its transconductance. The OTA entails a single Miller capacitor for frequency compensation, thus saving area occupation and improving frequency performance. As a distinctive feature of the proposed solution, the OTA is stable for capacitive loads higher than 5 pF. Implemented in a 65-nm standard CMOS technology, the proposed solution occupies an area of $10.6 \cdot 10^{-3}$ mm^2 and is powered from 0.3 V, with a total quiescent current equal to 8.5 μA. Experimental measurements show a gain–bandwidth (GBW) product of 1.65 MHz (0.81 MHz) with a phase margin (PM) equal to 70° (71°) when driving a 50-pF (150-pF) load, featuring the best figures of merit compared to other multistage sub-1-V OTAs in the literature.**

***Index Terms*— Bulk-driven, CMOS analog integrated circuits, low-voltage, operational transconductance amplifier (OTA).**

I. Introduction

A major trend in the current electronics industry is the extension of battery life in portable devices through the adoption of ultralow-power design techniques. This has reinforced interest in the development of low-voltage, low-current design approaches. By limiting power consumption is in fact possible to reduce the size of the battery (and consequently the overall volume of the device), thus ensuring the same device lifetime. This latter aspect is especially critical for implanted biomedical devices, where a reduced system volume is desirable to limit invasiveness [1].

Considering CMOS technology, the most widely adopted methodology for enabling analog circuits with low-voltage and low-current capabilities is subthreshold biasing, also known as weak inversion biasing. For example, through this approach, excellent operational transconductance amplifier (OTA) topologies have been implemented [2], [3], [4], [5]. These solutions allow supply voltages from around 1–0.5 V, but with limited input common-mode swing.

When operations below 0.5 V are requested, with rail-to-rail input capabilities, the bulk driving (body driving) technique, even in combination with the subthreshold one, has been proven to be the best solution [6], [7], [8], [9], [10], [11], [12], [13], [14], [15], [16], [17], [18], [19], [20].

To enable bulk driving, the MOSFET gate must be biased to form a conduction channel inversion layer, and the drain current is modulated by varying the bulk voltage through the body effect. In fact, bulk-driven stages allow minimum supply with wide input ranges, including rail-to-rail, and are particularly effective under very low-voltage supply, where the forward biasing of the body-source junction cannot exceed 0.4 V, thus limiting the forward body current in the range of a few picoamperes. However, compared with conventional gate-driven circuits, body-driven counterparts are characterized by lower voltage gain and/or gain–bandwidth (GBW) product, because of the limited value of bulk transconductance, g_{mb}, which is only about 10%–20% of the gate transconductance, g_m [21].

To overcome some of these limitations usually found in a conventional body-driven OTA, we present in this brief, a novel three-stage OTA. The main features of the proposed circuit can be summarized as follows.

1) It exploits local positive feedback within the first stage to improve its equivalent transconductance.
2) Three cascaded gain stages are adopted to further increase the dc gain, and unlike previous solutions, a single Miller capacitor is successfully exploited to implement frequency compensation, thus reducing the overall area occupation and maximizing GBW under a given standby current.
3) Class AB operation of the last stage increases slew rate (SR) performance and current driving capability.
4) A better common-mode rejection ratio (CMRR) with respect to a previous similar high-performance solution [10] is also inherently achieved by the proposed topology.

The OTA is designed and fabricated using a standard 65-nm CMOS technology. It can operate under a 0.3-V supply and provides a dc gain around 40 dB. Compared with other sub-1-V experimental solutions in the literature, the proposed one offers significant improvements, especially when considering area occupancy and GBW, reflected in the best figures of merit achieved by a body-driven OTA.

Some preliminary results of the proposed OTA have already been presented by the authors in a national conference [22]. In this work, the theoretical analysis is extended to include the effects for high capacitive loads. Moreover, extensive simulations, including corner and Monte Carlo analysis, and additional experimental results are provided.

II. Proposed Amplifier

A. Topology, Operating Point, and Large Signal Operation

The simplified schematic of the proposed OTA is depicted in Fig. 1. The circuit relies on a bulk-driven nontailed differential pair M1–M2, whose gate voltage, V_A, is set by M13 and current generator I_B [10]. Note that transistors M1 and M2 are thick oxide transistors, showing a higher value of the body effect parameter. Transistors M3 and M4 with resistors R_A and R_B implement the load of the differential pair. The body and drain terminals of M3 and M4 are cross-coupled as discussed in [23] for a gate-driven OTA. The provided positive feedback increases the differential input stage transconductance, as will appear clear in the following. The bias current of M1–M2 is accurately set by the current mirror ratio $(W/L)_{1,2}/(W/L)_{13}$ (where W/L is the MOS transistor aspect ratio), provided that the bulk voltage of M1, V_{CM}, is equal to the common-mode input voltage $(v_{IN+} + v_{IN-})/2$.

Considering that no current flows through R_A and R_B at dc, the drains of M3–M4 are at the same potential of their gates, i.e., they act as diode-connected transistors. Therefore, transistors M6 and M8

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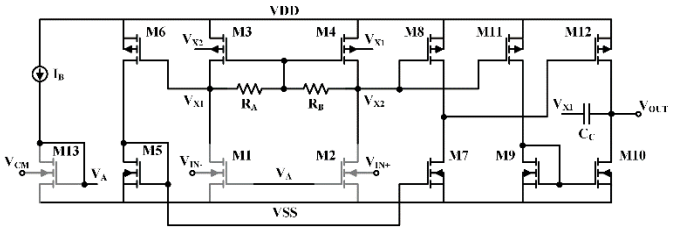


Fig. 1. Simplified schematic of the proposed OTA.

have the same source–gate voltage of M3 and M4, to which we refer to as $V_{\rm SG}$. Since the threshold voltage of a pMOS is expressed by

$$V_T = V_{T0} - \gamma\left(\sqrt{2\varphi_F + V_{\rm SB}} - \sqrt{2\varphi_F}\right) \tag{1}$$

where V_{T0} is the zero-bias threshold, φ_F is the Fermi potential, γ is the body effect parameter, and $V_{\rm SB}$ is the source-bulk voltage, hence, neglecting the channel length modulation and assuming operation in saturation, and the dc current ratio $I_{D6,8}/I_{D3,4}$ is

$$\frac{I_{D6,8}}{I_{D3,4}} = \frac{(W/L)_{6,8}}{(W/L)_{3,4}}\left[1 - \frac{\gamma\left(\sqrt{2\varphi_F + V_{\rm SG}} - \sqrt{2\varphi_F}\right)}{V_{\rm SG} + V_{T0}}\right]^2 \tag{2}$$

where $V_{\rm SB} = V_{\rm SG}$ was set for M3 and M4, due to the topological symmetry. As a result, the current mirror ratio in (2) is lower than that of a conventional current mirror, in which the factor in the square brackets equals 1. In other words, if $(W/L)_{6,8} = (W/L)_{3,4}$ is set, $I_{D6,8} < I_{D3,4}$ is obtained.

As far as I_{D11} is concerned, it stands in a current mirror ratio with I_{D8} and sets the quiescent current in the output stage (M12) through the current mirror M9–M10. Class-AB operation of the last stage is ensured by M11 and M12 for sinking and sourcing output current, respectively.

B. Small-Signal Analysis

Similar to what was demonstrated in [10], the first stage exhibits a differential output behavior, even though the input voltage is applied only to the bulk of M1 (or equivalently to the bulk of M2). In addition, the differential-mode transconductance of the first stage is enhanced by the positive feedback of the bulk-drain cross-connection of transistors M3 and M4. This can be demonstrated in the same way as was done in [23], which analyzed a gate-driven cross-coupled input stage. The (unbalanced) differential gain of the first stage, $A_{0,1}$, is hence given by the equivalent transconductance multiplied by the equivalent output resistance and results to be

$$\begin{aligned} A_{0,1} &= \frac{v_{x1}}{v_{id}} = -\frac{1}{2}G_{\rm mb}R_{A,B}//r_{o1} \\ &= -\frac{1}{2}\frac{g_{\rm mb1,2}}{1 - g_{\rm mb3,4}R_{A,B}//r_{o1}}R_{A,B}//r_{o1} \end{aligned} \tag{3}$$

where $g_{\rm mb1,2}$ and $g_{\rm mb3,4}$ are the bulk transconductance of transistors M1–M2 and M3–M4, respectively, and r_{o1} is the parallel of $r_{d1,2}$ and $r_{d3,4}$. Care must be taken during the design phase, so that the denominator of (3) is always positive in all the process corners and temperature values. In conclusion, the gain increase is achieved by setting the denominator of (3) less than 1, but close to 1.

The overall OTA differential gain is given by

$$A_0 \approx G_{\rm mb}g_{m6,8}g_{m12}\left(R_{A,B}//r_{o1}\right)r_{o2}r_{o3} \tag{4}$$

where r_{o2} and r_{o3} are the output resistances of the second stage, equal to $r_{d7}//r_{d8}$ and of the third stage (the main output), equal to $r_{d10}//r_{d12}$, respectively.

One of the main limitations of [10], of which this solution is an improved version, was the low CMRR, expressed by $1/2\ g_{m3,4}R_{A,B}$, and that resulted in the range of a few decibels. In the proposed topology, CMRR is enhanced due to both the increased input-stage differential gain given by (3) and the differential to single ended conversion operated by current mirror M5–M7, not present in [10]. In fact, under perfect symmetry conditions (i.e., with the same common-mode currents generated by M6 and M8 and a unity current gain of M5–M7), the common-mode gain ideally nullifies. This condition requires that the drain voltages of M6 and M8 (and of course of M5 and M7) must be equal, yielding

$$V_{\rm GS5} = V_{\rm DD} - V_{\rm SG12}. \tag{5}$$

Such a condition nullifies systematic offset as well. Unfortunately, (5) is hardly met due to different pMOS and nMOS threshold voltage constraints and variations with process and temperature; therefore, a nonnegligible common-mode gain will still be present in an actual implementation.

Among the possible frequency compensation strategies, single Miller approach is exploited [24]. In particular, the frequency compensation is achieved through the Miller capacitor C_C connected between the output and the drain of M3. This is the first time that this type of compensation is successfully exploited in a body-driven OTA.

Denoting by c_{o2} the parasitic capacitance at the output of the second stage and by C_L the loading capacitance (not shown in Fig. 1), small-signal analysis reveals that the open-loop transfer function can be approximated as

$$\begin{aligned} A(s) &= A_0\frac{\left(1+\frac{s}{z_1}\right)\left(1+\frac{s}{z_2}\right)\left(1-\frac{s}{z_3}\right)}{\left(1+\frac{s}{p_1}\right)\left(1+a_1s+a_2s^2\right)\left(1+\frac{s}{p_4}\right)} \\ &\approx A_0\frac{\left(1+\frac{s}{z_1}\right)}{\left(1+\frac{s}{p_1}\right)\left(1+a_1s+a_2s^2\right)} \end{aligned} \tag{6}$$

where A_0 is the same as in (4), and the other parameters are given in the following:

$$p_1 \approx \frac{1}{g_{m6,8}g_{m12}\left(R//r_{o1}\right)r_{o2}r_{o3}C_C + r_{o3}C_L} \tag{7}$$

$$a_1 \approx \frac{C_L\left(C_CR_{A,B} + 2c_{o2}r_{o2}\right)}{2} \tag{8}$$

$$a_2 \approx \frac{C_CC_Lc_{o2}R_{A,B}r_{o2}}{2} \tag{9}$$

$$z_1 \approx \frac{g_{m3,4}}{2C_C} \tag{10}$$

$$z_2 \approx \frac{g_{m8}g_{m12}}{c_{o2}\left(g_{m10} - g_{m3,4}\right)} \tag{11}$$

$$z_3 \approx \frac{g_{m10} - g_{m3,4}}{c_{X2}} \tag{12}$$

$$p_4 \approx \frac{g_{m3,4}}{2c_{X2}}. \tag{13}$$

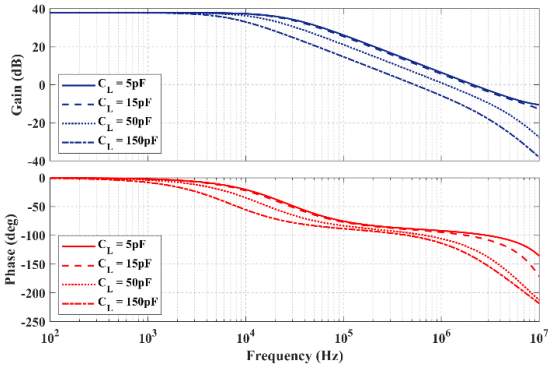
Note that the two last zeros and pole (all real) can be neglected because they depend on parasitic capacitances much lower than C_L and C_C, and hence, their values are at a frequency much higher than the GBW product, which, from (4) and (7), is expressed by

$$\text{GBW} = A_0p_1 = \frac{G_{\rm mb}}{C_C + \frac{C_L}{g_{m6,8}g_{m12}(R//r_{o1})r_{o2}}}. \tag{14}$$

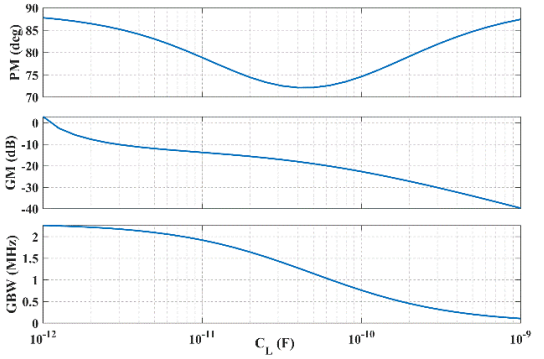
It should be observed that (14) reduces to the usual expression $G_{\rm mb}/C_C$ for $C_L \ll g_{m6,8}g_{m12}(R//r_{o2})r_{o2}$. However, for $C_L \gg g_{m6,8}g_{m12}(R//r_{o2})r_{o2}$, the GBW reduces with increasing values

TABLE I
TRANSISTOR ASPECT RATIOS AND CIRCUIT PARAMETERS

Par.	Value	Par.	Value	Par.	Value	Par.	Value
V_{DD}	0.3 V	$(W/L)_6$, $(W/L)_8$	9/0.18	C_L	50 pF	g_{m10}	78.9 µS
I_B	1.6 µA	$(W/L)_9$	2.1/0.18	$g_{m1,2}$	25.9 µS	g_{m12}	74.7 µS
V_B	150 mV	$(W/L)_{10}$	12.6/0.18	$g_{mb1,2}$	7.1 µS	r_{o1}	304 kΩ
$(W/L)_1$, $(W/L)_2$	4.2/0.3	$(W/L)_{11}$	9/0.18	$g_{mb3,4}$	3 µS	r_{o2}	845 kΩ
$(W/L)_{13}$	4.2/0.3	$(W/L)_{12}$	13.5/0.18	$g_{m3,4}$	7.3 µS	r_{o3}	110 kΩ
$(W/L)_3$, $(W/L)_4$	9/0.18	R_A, R_B	200 kΩ	g_{m7}	14.8 µS	c_{o1}	45 fF
$(W/L)_5$, $(W/L)_7$	0.45/0.18	C_C	470 fF	$g_{m6,8}$	16.3 µS	c_{o2}	62 fF



(a)



(b)

Fig. 2. Simulated (a) ac response at different load capacitor values and (b) PM, GM, and GBW product versus load capacitor.

of C_L. Again, the positive feedback enhancing $G_{\rm mb}$ is found beneficial also to improve GBW.

The evaluation of the phase margin (PM), yields

$$\mathrm{PM} = \tan^{-1}\left(\frac{1 - a_2\omega_{\rm GBW}^2}{a_1\omega_{\rm GBW}}\right) + \tan^{-1}\left(\frac{\omega_{\rm GBW}}{z_1}\right). \qquad (15)$$

III. DESIGN AND SIMULATION RESULTS

The OTA in Fig. 1 was designed using a standard 65-nm CMOS technology provided by STMicroelectronics. The above equations were also considered during the design steps. Table I shows the main transistor aspect ratios and circuit parameters. The supply voltage, $V_{\rm DD}$, is 0.3 V ($V_{\rm SS}$ = 0 V) and the total current consumption is 8.5 μA. It is seen that $g_{\rm mb3,4}R_{\rm A,B}//r_{o1}$ is about 0.36 providing a 1.56 boost in the transconductance, as anticipated by (3).

Assuming a load capacitance equal to 50 pF, the required value of C_C to get a PM of 70° is equal to only 470 fF.

Fig. 2(a) shows the simulated bode plot of the open-loop gain at various capacitive loads. As predicted by (14), GBW does not depend on C_L for $C_L \ll g_{m6,8}g_{m12}(R//r_{o2})r_{o2} \approx 58$ pF. This result is confirmed by Fig. 2(b), where the PM, gain margin (GM), and GBW are simulated versus C_L. As a distinctive feature of the proposed solution, the OTA exhibits a PM higher than 72° for any capacity load. However, stability is reduced for low value of C_L due to reduced GM, which is caused by the reduction of the damping factor of complex and conjugate poles. Consequently, the amplifier is stable for capacitive loads greater than about 5 pF.

The simulation of the input-referred noise shows a value of the white noise equal to 250 nV/$\sqrt{\rm Hz}$ with a corner frequency value of about 10 μV/$\sqrt{\rm Hz}$.

The robustness of the OTA against process and temperature variations has been assessed through extensive corner analysis. The results are summarized in Tables II for the various transistor corners and at −10 °C, 27 °C, and 85 °C, assuming C_L = 50 pF. The amplifier is apparently stable in all cases.

Additional analyses were executed considering a ±10% variation of the power supply, confirming the robustness of the OTA.

Finally, 1000 Monte Carlo simulations have been executed, and the results are summarized in Table III, showing a relative standard deviation lower than 20% in all cases.

TABLE II
CORNER ANALYSIS RESULTS

T=-10°C

Parameter	TT	SS	SF	FS	FF
Power (µW)	2.3	1.9	2	2.2	2.7
DC Gain (dB)	38.1	35.8	39	33.1	39.6
GBW (MHz)	1.06	0.69	1.01	0.68	1.4
Phase Margin (deg)	73.5	77.1	71.6	79.7	72.7
Gain Margin (dB)	-21.3	-23.5	-19.1	-27.1	-20.2
Pos. Slew Rate (V/µs)	0.44	0.27	0.98	0.22	0.86
Neg. Slew Rate (V/µs)	0.28	0.18	0.26	0.24	0.45

T=-27°C

Parameter	TT	SS	SF	FS	FF
Power (µW)	2.8	2.4	2.5	2.8	3.3
DC Gain (dB)	38.1	36.7	37.3	34.5	38.8
GBW (MHz)	1.28	0.97	1.15	0.96	1.52
Phase Margin (deg)	72.8	73.9	72.8	76.2	73.7
Gain Margin (dB)	-20.4	-21.5	-19.5	-24.6	-20
Pos. Slew Rate (V/µs)	0.61	0.41	0.98	0.34	0.86
Neg. Slew Rate (V/µs)	0.36	0.26	0.29	0.33	0.45

T=-85°C

Parameter	TT	SS	SF	FS	FF
Power (µW)	3.7	3.2	2.2	3.6	4.3
DC Gain (dB)	35.3	35.3	30.9	34.1	35
GBW (MHz)	1.32	1.16	0.99	1.19	1.41
Phase Margin (deg)	75.7	74.3	79.3	75.7	77.9
Gain Margin (dB)	-21.1	-21	-23.2	-23.1	-21.5
Pos. Slew Rate (V/µs)	0.83	0.62	1.11	0.53	1.06
Neg. Slew Rate (V/µs)	0.4	0.34	0.29	0.42	0.44

TABLE III
CORNER AND MONTE CARLO (1000 ITERATIONS) ANALYSIS RESULTS FOR $T = 27$ °C (TT CORNER)

Parameter	µ	σ
Power (µW)	2.8	0.2
DC Gain (dB)	38	0.5
GBW (MHz)	1.26	0.1
Phase Margin (deg)	73	0.5
Gain Margin(dB)	-20.5	0.7
Positive Slew Rate (V/µs)	0.62	0.11
Negative Slew Rate (V/µs)	0.35	0.04

IV. EXPERIMENTAL RESULTS

Fig. 3 depicts the layout of the OTA superimposed to the chip microphotograph. The occupied area is $10.6 \cdot 10^{-3}$ mm^2.

Fig. 4(a) and (b) shows the measured open-loop frequency response for C_L = 50 pF and C_L = 150 pF, respectively, of one of the fabricated prototypes. The dc gain is around 40 dB and GBW is

TABLE IV

SUMMARY OF MEASURED PERFORMANCE METRICS AND COMPARISON WITH OTHER MULTISTAGE EXPERIMENTALLY TESTED SUB-1-V OTAS

Ref.	[4]	[10]	[21]	[11]	[12]	[13]	This work*	
Year	2016	2016	2017	2018	2020	2020	2022	
Tech. (nm)	180	180	350	180	180	65	65	
Op. mode**	GD	BD	GD	BD	BD	BD	BD	
# stages	2	3	2	2	3	3	3	
Area ($mm^2 \times 10^{-3}$)	36	19.8	14.0	8.2	9.8	2.0	1.06	
Supply voltage(V)	0.5	0.7	0.7	0.3	0.3	0.25	0.3	
C_L (pF)	40	20	10	20	30	15	50	150
DC gain (dB)	77	57	65	63	98.1	70	38	
I_{BIAS} (µA)	0.14	36	27	0.056	0.043	0.104	8.5	
GBW (MHz)	0.004	3	1	0.0028	0.0031	0.0095	1.65	0.81
PM (°)	56	60	60	61	54	88	70.3	71.3
SR (V/µs)	0.002	2.8	0.25	0.0071	0.0091	0.002	0.18	0.12
CMRR (dB)	55	19	45	72	60	62.5	39.8	
PSRR (dB)	52	52	50	62	61	38	44.7	
$IFOM_S$ (MHz·pF/µA)(1)	1.14	1.67	0.37	1.00	2.15	1.37	9.71	14.29
$IFOM_L$ (V/µs·pF/µA) (2)	0.57	1.56	0.09	2.54	6.30	0.29	1.06	2.12
$IFOM_{AS}$ (MHz·pF/µA·mm^2) (3)	31.8	84.2	26.5	122	219	685	9156.5	13485
$IFOM_{AL}$ (V/µs·pF/µA· mm^2) (4)	15.9	78.6	6.61	309.2	642.9	144.2	998.9	1997.8

*Average values over six samples.

**GD: gate-driven; BD: bulk-driven

$$^{(1)}\ IFOM_S = \frac{GBW}{I_{bias}} C_L \quad ^{(2)}\ IFOM_L = \frac{SR}{I_{bias}} C_L \quad ^{(3)}\ IFOM_S = \frac{GBW}{I_{bias} \cdot Area} C_L \quad ^{(4)}\ IFOM_L = \frac{SR}{I_{bias} \cdot Area} C_L$$

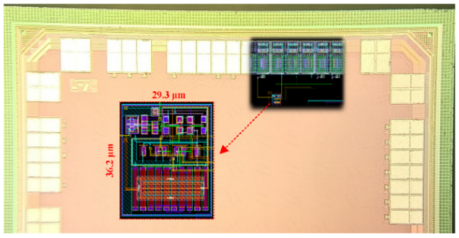


Fig. 3. OTA layout and chip microphotograph.

1.65 MHz for $C_L = 50$ pF and 0.77 MHz for $C_L = 150$ pF and with a PM of nearly 66° for $C_L = 50$ pF and 70° for $C_L = 150$ pF.

The measured response of the same prototype to a 40-mV_{pp} step is illustrated in Fig. 5(a) and (b) for $C_L = 50$ pF and $C_L = 150$ pF, respectively. Positive/negative SR and 1%-settling time are, respectively, equal to 0.25/−0.11 V/μs and 0.31/0.7 μs for $C_L = 50$ pF. The same parameters for $C_L = 150$ pF are equal to 0.17/−0.07 V/μs and 0.62/1.26 μs. The maximum input current when a 300-mV_{pp} step is applied is equal to about 600 nA.

The experimental characterization of the OTA for lower capacitive loads was not possible due to the loading effect of the package, test PCB, and probes, which accounts for a parasitic load almost equal to 50 pF.

Six different samples have been experimentally characterized, and the mean values of the main amplifier performance metrics are summarized in the last column of Table IV, which compares the proposed solution with other recent multistage sub-1-V OTAs. The proposed solution has the lowest area consumption, operates under one of the lowest supply voltages, and can drive the largest load capacitor with one of the best GBW achieved.

The traditional figures of merit, whose expressions are reported at the bottom of Table IV, are adopted to compare the different amplifiers. It can be noted that other solutions exhibit a higher value of $IFOM_L$ than the proposed OTA (namely, [10], [11], [12] for $C_L = 50$ pF and [11], [12] for $C_L = 150$ pF), whereas $IFOM_S$ is higher

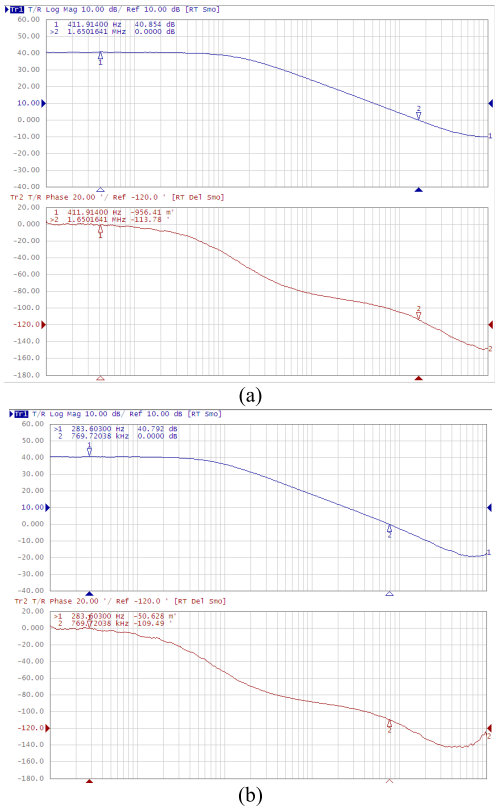


Fig. 4. Measured bode diagram of the OTA loop gain with (a) $C_L = 50$ pF and (b) $C_L = 150$ pF.

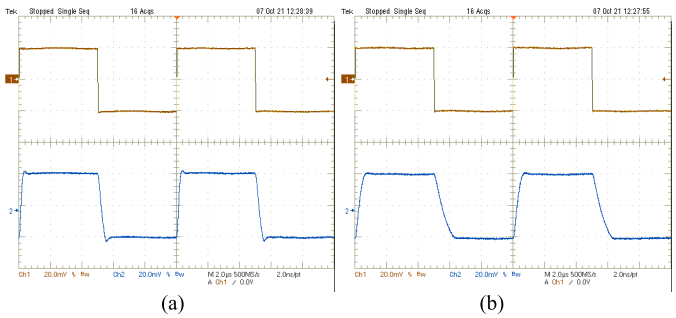


Fig. 5. Measured step response in unity gain configuration with (a) $C_L = 50$ pF and (b) $C_L = 150$ pF.

than the other solutions by 4.5× and 6.6× for C_L equal to 50 and 150 pF, respectively.

Moreover, when $IFOM_{AS}$ and $IFOM_{AL}$ are considered, the proposed OTA exhibits an improvement equal to about 13× and 1.5× for $C_L = 50$ pF and 20× and 3× for $C_L = 150$ pF, when compared to the other solutions. As a main drawback, the lowest dc gain is displayed by the proposed OTA.

V. CONCLUSION

A bulk-driven three-stage OTA exploiting positive feedback and a single Miller capacitor has been proposed and experimentally validated. The solution can work under a 0.3-V supply and exhibits class AB operation, amenable to drive a 50-pF load with an SR of 0.18 V/μs and a GBW of 1.65 MHz. The proposed OTA is a good candidate for area-constrained ultralow-voltage, ultralow-power applications, such as wireless sensor nodes and implantable biomedical devices. The adoption (apart from M1–M2 and M13) of transistors of the digital core of the design kit has led to a dc

gain equal to 38 dB, due to the reduced intrinsic output resistance offered by these devices. However, additional circuit techniques relying on local positive feedback can be adopted to increase the gain as those proposed in [14], [15], and [16]. Moreover, the lack of a tail current generator for the first stage leads to reduced values of power supply rejection ratio (PSRR) and CMRR, which, nevertheless, still offer acceptable values. The proposed OTA can be exploited in all the applications requiring sub-0.5-V supply and rail-to-rail input operation, like IoT nodes directly powered by single silicon solar cells.

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