Hybrid Cascode Frequency Compensation for Four-Stage OTAs Driving a Wide Range of C_L

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***Abstract*— Feedback amplifiers consisting of multiple gain stages are used to establish highly accurate buffered/amplified signals that can drive a wide range of capacitive load (CL). This article models, analyzes, and presents the measurement results of a high-gain four-stage operational transconductance amplifier (OTA) that is able to handle a wide range of CL up to infinity. In addition to local compensation capacitors and nulling resistors in the intermediate stages, two high-speed feedback loops made by parallel Miller capacitors and current buffers provide Miller compensation and the consequent pole-splitting in the lower CL range. The dominant pole is made dependent on the CL for the higher CL range, enabling the maintenance of the stability conditions up to infinite CL. The proposed amplifier was integrated into a 65-nm CMOS technology, consuming 140-μA static current under a 1.2-V supply and an active area of 0.0086 mm^2. A dc gain greater than 100 dB was also perceived with a unity-gain frequency (UGF) of 4.09, 2.01, and 0.27 MHz for 4.7, 10, and 100-nF load capacitors, respectively. The average slew rate (SR) is 0.59 V/μs, when the OTA is formed as a buffer targeting the CLs higher than 4.7-nF.**

***Index Terms*— Capacitive load (CL), frequency compensation, miller effect, multistage, operational transconductance amplifiers (OTA), slew-rate (SR), stability, unity-gain frequency (UGF).**

I. Introduction

THE continuous trend toward the scaling of MOS transistors has been followed by reducing the voltage supply (V_{DD}) to guarantee a safe operation under very low power constraints. Meanwhile, short-channel MOS devices suffer from reduced intrinsic gain [1], and traditional gain-boosting solutions like cascading have been progressively abandoned in low-voltage nano-scale bulk CMOS technologies [2]. Although FinFET technologies (i.e., technology nodes lower than 16 nm) exhibit sufficient intrinsic gain, the majority of commercial analog products are still fabricated with conventional higher than 32 nm bulk technologies. Enlarging the gain of the amplifiers in scaled bulk CMOS (down to 32 nm) can be therefore accomplished by resorting to the multiple gain stages cascaded. Efficient implementation of multistage amplifiers has not been, however, straightforward and thus the focus of extensive research over the last decades [3], [4], [5]. Within this framework, one of the commonly used applications of the high-gain operational transconductance amplifiers (OTAs) was to provide a reliable amplified signal for the capacitive loads (CLs) reaching tens of nanofarad. Some principal blocks that call for such specifications are active-matrix liquid crystal displays (LCDs), low-dropout regulators (LDOs), active filters, analog-to-digital converters, and line drivers [6], [7], [8], [9], [10], [11].

Maintaining the loop stability is the main challenge of the feedback OTAs supporting a wide C_L range [2], [5], [12]. Each stage adds a high-impendence node and, consequently, a dominant pole in the transfer function which potentially depends on the loading conditions, so keeping the OTA stable over a broad C_L range entails a carefully designed compensation network. The size of the CL is highly variable in some applications, preventing the optimization of the transistor sizes irrespective of C_L. In the case of a headphone driver, e.g., the external load is dependent on the type of cable connected to the output and its size may vary between a few picofarads to several nanofarads [13]. The C_L variations may not be aggressive in those designs used for LCD drivers, but a general-purpose amplifier is highly desirable to prevent multiple design cycles by supporting a wide range of static CLs. Single- or two-stage feedback OTAs handling a wide C_L range can be conveniently designed and stabilized using the commonly used architectures [14], [15], [16], [17]. Indeed, at least three stages are needed to overcome the gain requirement of several customary applications in recent technologies. It soon became apparent that two compensation capacitors, both of which are dependent on C_L, are required to stabilize a three-stage amplifier using classical nested Miller compensation (NMC) [4], [18]. [19], [20], [21]. As such, the bandwidth is severely limited and ends up with inferior power and area efficiencies due to improper placement of poles/zeros setting aside the loading conditions of the amplifier. Sophisticated design strategies for three-stage amplifiers thus tend to eliminate the second capacitor and enrich the so-called single-Miller capacitor (SMC) compensation method with auxiliary current buffers, local *RC* networks, and feedforward stages, so additional left-half-plane (LHP) zeros are generated and nondominant poles can be moved to higher frequencies for the minimum area and power consumption [22], [23], [24], [25].

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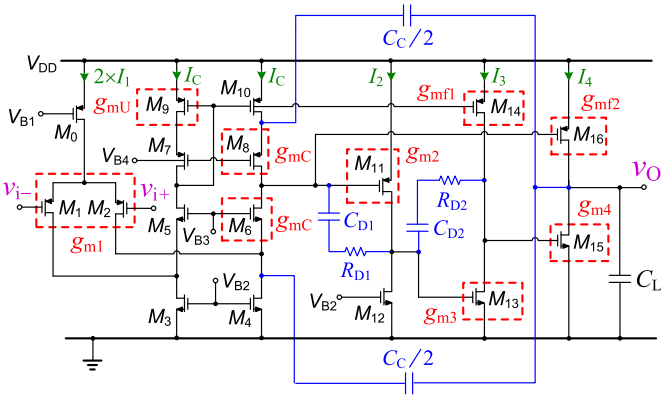

Fig. 1. Schematic of the proposed OTA.

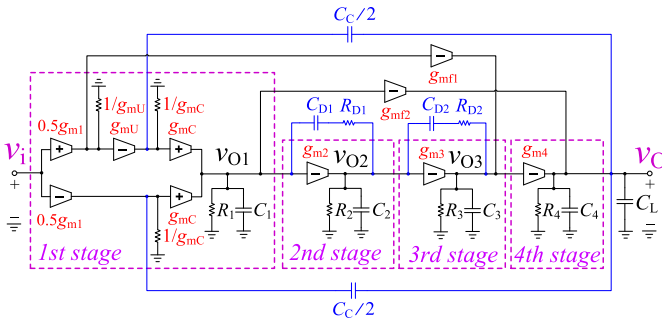

Fig. 2. Block diagram of the OTA in Fig. 1.

Capacitor-free compensation strategies have been also reported at the cost of inferior power efficiency relative to the capacitor-based solutions [26], [27]. Among the possible ways to realize a stable three-stage OTA, hybrid-cascode frequency compensation [28], [29] was originally developed from the idea of Miller compensation employing current buffers [23], [24], and proved to be very efficient especially when combined to the local *RC* network for achieving a wide C_L drivability range [2]. According to the original strategy, the Miller capacitor is split into equal fractions, and each fraction is applied to build up a unilateral feedback pathway to the first stage through a current buffer. The original compensation loop is thus divided into parallel loops to detect the output signal with a higher feedback factor, thus boosting the overall efficiencies in terms of area and power. The additional feedback is carefully incorporated into the circuit topology without sacrificing area or power and by exploiting the original resources of the amplifier only [2]. In the case of three-stage OTAs, experimental results thus reflected substantial improvements from the CL range, size of C_C, silicon footprint, and power aspects [2]. As intrinsic gain and channel length of transistors continue to scale down, four-stage amplification is becoming more essential to maintain both dynamic range and the gain requirements in nano-scale technologies. By contrast, the frequency compensation of four-stage amplifiers appears to be much more complicated especially when a wide C_L range is demanded [30], [31], [32], [33].

In this work, we extend the idea of hybrid-cascode frequency compensation to four-stage OTAs by combining it with local compensation capacitors and resistors so that acceptable stability margins can be maintained over a wide C_L range (from 4.7-nF to infinity, as confirmed by the experimental results). The remainder of this contribution is structured as follows. Section II analyzes the topology, block diagram, and small- and large-signal conditions of the new amplifier. Section III is devoted to the design procedures and the prerequisite stability analysis. In Section IV, we show the simulation and experimental results and compare the performance metrics with the relevant art. Finally, Section V concludes the article.

II. Proposed Topology

A. Circuit Schematic

Fig. 1 presents a possible implementation of the proposed four-stage OTA, where $v_i = v_{i+} - v_{i-}$ is the input voltage and v_O is the output. The input stage g_{m1} is made by M_0–M_{10} with M_0 to power up the input devices. The current mirror devices M_9–M_{10} perform the differential to single-ended conversion. The complementary MOS devices M_{11}–M_{12}, M_{13}–M_{14}, and M_{15}–M_{16} constitute the second, third, and fourth inverting stages between the supply rails where g_{m2}, g_{m3}, and g_{m4} are their equivalent transconductances, respectively. Transistors M_{14} and M_{16} implement the feedforward stages with transconductances g_{mf1} and g_{mf2}, which assist in improving the large-signal operation by forming class-AB third and fourth stages topologies. The quiescent current of the output branch is decided by the second stage current since M_{11} and M_{16} share the same source-gate voltage. To establish a more stable quiescent current for the output stage, either M_{15} or M_{16} can be biased via a low impedance node in the form of a class-A configuration. Such approach is not, however, effective in terms of dynamic load drivability and static power consumption. The biasing voltages V_{B1}–V_{B4} are accompanied by a biasing circuitry not illustrated for the sake of conciseness. It is worth noting that the circuit topology is very simple and entails the same number of transistors of a three stage OTA since the second, third, and fourth stages are all inverting.

The main elements of the frequency compensation network are the series R_{D1}, C_{D1}, and R_{D2}, C_{D2} around the second and the third stages, respectively, besides the Miller $C_C/2$ capacitors between v_O and the source of M_6 and M_8 that implement the embedded g_{mC} transconductances without any power overhead. These devices with a relatively light $1/g_{mC}$ input impedance close the parallel feedback pathways from v_O to the input, moving a right-half-plane (RHP) zero to very high frequencies by minimizing a feedforward current to flow to the output via either $C_C/2$ [34]. The hybrid nature of the compensation network also allows designers to achieve a balanced time response during the falls and rises of v_O, unlike the classical solution which possibly connects C_C to the source of M_6 or M_8.

B. Small-Signal Analysis

Fig. 2 depicts the amplifier diagram of the proposed four-stage OTA, where identical symbols as in Fig. 1 are utilized to represent similar elements. It contains a front-end differential stage followed by inverting second, third, and fourth stages,

all of which are modeled by a transconductance g_{mi}, output resistor R_i, and output capacitor C_i ($i = 1, 2, 3, 4$). The feedforward stages g_{mf1} and g_{mf2} have negligible effect on the small-signal operation, but are intended for improving the large-signal operation [2], [24]. The compensation network contains C_C broken into equal fractions, and each fraction forms a feedback loop consistent with the earlier descriptions. It will be shown later that the new arrangement pushes to a higher frequency the magnitude of the nondominant poles and lowers their quality factor, Q, when compared to a single feedback loop potentially closed by C_C. One-way g_{mC} current buffers are placed in series with the Miller capacitors to represent the contribution of M_6 or M_8 in Fig. 1. The small input impedance of the current buffers extends the bandwidth of the compensation loop by relaxing the C_C loading on v_O. As for the series C_{D1}, R_{D1} and C_{D2}, R_{D2}, they enhance the stability of the inner gain-stages while contributing to the overall stability not by introducing a low-frequency zero only but also by reducing the Q-factor of the poles as will be analyzed later.

A voltage-gain transfer function based on the amplifier diagram in Fig. 2 is a prerequisite to exploring the different aspects of the proposed OTA in the presence of C_L variations. The exact transfer function is excessively complex, containing several terms related to the stages' output impedances, their equivalent transconductors, and compensation elements. Many terms can be simplified upon $R_i \gg R_{D1}$, $R_{D2} \gg 1$, $g_{mi}R_j \gg 1$, and $C_L \gg C_C$, C_{D1}, $C_{D2} \gg C_i$ for $i, j = 1, 2, 3, 4$, the output impedances are subsequently dominated by C_L, g_{mi} and compensation elements. Under these circumstances, the methodology described in [34] can be used to approximate v_O/v_i as

$$A_V(s) = \frac{v_O}{v_i} \approx \frac{A_0\left(1+\frac{s}{z_1}\right)\left(1+\frac{s}{z_2}\right)}{\left(1+\frac{s}{p_{-3dB}}\right)\left(1+\frac{s}{Q\omega_0}+\frac{s^2}{\omega_0^2}\right)} \tag{1}$$

where

$$A_0 \approx g_{m1}g_{m2}g_{m3}g_{m4}R_1R_2R_3R_4 \tag{2}$$

and

$$p_{-3dB} = -\frac{1}{g_{m2}g_{m3}g_{m4}R_1R_2R_3R_4C_C + R_4C_L} \tag{3}$$

denote the dc gain and the main pole, respectively. The transfer function contains two nondominant poles, whose Q-factor and natural frequency ω_0 are given as

$$\omega_0 = \sqrt{\frac{2g_{mC}g_{m2}g_{m3}g_{m4}(R_{D1}C_{D1}+R_{D2}C_{D2})}{(g_{m2}+g_{m3})C_{D1}C_{D2}C_L}} \tag{4}$$

$$\begin{aligned} Q &= \frac{1}{R_{D1}R_{D2} + \frac{g_{m2}+g_{m3}}{g_{m2}g_{m3}g_{m4}}\left(1+\frac{C_L}{C_C}\right)} \\ &\quad \times \sqrt{\frac{(g_{m2}+g_{m3})(R_{D1}C_{D1}+R_{D2}C_{D2})C_L}{2g_{mC}g_{m2}g_{m3}g_{m4}C_{D1}C_{D2}}} \\ &\approx C_C\sqrt{\frac{g_{m2}g_{m3}g_{m4}(R_{D1}C_{D1}+R_{D2}C_{D2})}{2g_{mC}(g_{m2}+g_{m3})C_{D1}C_{D2}C_L}}. \end{aligned} \tag{5}$$

These latter equations show that as follows.

1) Increasing C_L lowers the Q factor, thus leading up to two real poles when the OTA should drive an ultralarge load capacitor.
2) The coefficient "2" appearing in the Q factor and ω_0 expressions stems from the parallel loops implemented by dual $C_C/2$. Not only ω_0 is pushed to higher frequencies by this coefficient, but the Q factor is also reduced, both of which are in favor of stability.
3) The Q factor is governed by R_{D1} and R_{D2} rather than the output resistors R_2 and R_3. This means that reducing the compensating resistors assist in improving the gain margin (GM) by dropping the Q factor without sacrificing the dc gain. Too low R_{D1} or R_{D2} are accompanied by compromised stability as they excessively lower ω_0 and, in turn, the phase margin (PM) of the exterior loop. Therefore, these resistors should be tuned to optimally position the nondominant poles relative to the time and frequency requirements of the application.

The derived transfer function also involves the LHP z_1 and the RHPz_2 located at high frequencies, in which their magnitude is

$$z_1 = \frac{R_{D1}C_{D1}+R_{D2}C_{D2}}{R_{D1}R_{D2}C_{D1}C_{D2}} = \frac{1}{R_{D1}C_{D1}} + \frac{1}{R_{D2}C_{D2}} \tag{6}$$

$$z_2 = -\frac{2g_{mC}g_{m2}g_{m3}g_{m4}R_{D1}R_{D2}}{(g_{m2}+g_{m3})C_C}. \tag{7}$$

The LHP zero depends on all C_{D1}, C_{D2}, and R_{D1} and R_{D2}, and should be positioned to nullify partially the negative phase shift caused by the nondominant poles. As for the RHP zero, it is proportional to the compensating resistors, Miller capacitor and the g_m factors, and should be located well after the gain-bandwidth (GBW) product for its contribution not to reduce the stability margins. From (2) and (3) the GBW is expressed by

$$\text{GBW} = A_0 \cdot |p_{-3\text{dB}}| = \frac{g_{m1}}{C_C + C_L/g_{m2}g_{m3}g_{m4}R_1R_2R_3}. \tag{8}$$

As for $C_L \ll g_{m2}g_{m3}g_{m4}R_1R_2R_3C_C$, the above expression is simplified to the maximum g_{m1}/C_C, reducing gradually to $g_{m1}g_{m2}g_{m3}g_{m4}R_1R_2R_3/C_L$ under the heavy capacitive loading conditions. Depending on the size of C_C, the classical g_{m1}/C_C relation thus holds only in the lower range of C_L (say up to a few nanofarad). This means that the role of C_C is substituted by C_L when the amplifier should handle a very large load capacitors load. Endorsed by measurement results, scaling of the GBW via C_L can be exploited to optimize the stability conditions and to widen the upper C_L limit up to infinity. The movement of the poles/zeros is sketched in Fig. 3 by enlarging C_L, indicating that increasing the CL converts to real poles the original complex and conjugate poles and pushes the first pole toward the origin.

The transconductances of M_6 and M_8 were assumed to be identical in the foregoing analysis. While perfect matching can never be met using different types of M_6 and M_8 in Fig. 1, we anticipate that small mismatches between their g_{mC} trivially alter the positioning of the poles and zeros [2].

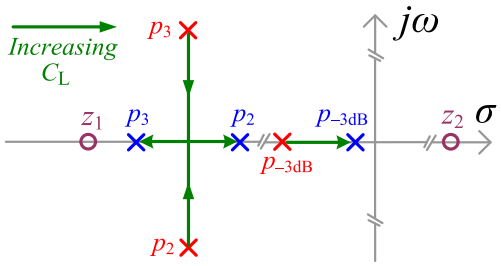

Fig. 3. Pole-zero map of the proposed OTA against C_L.

C. Large-Signal Analysis

The large-signal step response is generally described by slew rate (SR) instead of the small-signal GBW, GM, and PM parameters. Referred to as the maximum rate of deviation, the SR is defined by the available current that can charge or discharge the parasitic and load capacitors connected to the gain stage outputs. By denoting $I_{A1} \approx I_C$, $I_{A2} \approx I_2$, $I_{A3} \approx I_3$, and $I_{A4} \approx I_4$ as the upper limit of the currents that can be fed to the loading of the first stage $C_{L1} \approx C_{D1} + C_C/2 + C_C/2 = C_{D1} + C_C$, second stage $C_{L2} \approx C_{D1} + C_{D2}$, third stage $C_{L3} \approx C_{D2}$, and the final stage $C_{L4} \approx C_C + C_L$ in Fig. 1, further by assuming that the parasitics are negligible when compared to the load and compensation capacitors, the SR will be the minimum among the following contributors:

$$\begin{aligned} \mathrm{SR} &\approx \min(\mathrm{SR}_1, \mathrm{SR}_2, \mathrm{SR}_3, \mathrm{SR}_4) \\ &= \min\left(\frac{I_{A1}}{C_{L1}}, \frac{I_{A2}}{C_{L2}}, \frac{I_{A3}}{C_{L3}}, \frac{I_{A4}}{C_{L4}}\right). \end{aligned} \tag{9}$$

The above relation is nominally restricted by SR_1 and SR_4 for small and heavy CLs, respectively. As for M_{16} in Fig. 1, it manages to improve the SR by forming an output push–pull stage capable of boosting the output current I_{A4} under the undesired output transitions. The use of SR boosters can help drive ultralarge CLs more effectively [30].

The above SR analysis models the average trend of the realistic *SR* only. Completely symmetrical positive/negative SR (SR+/SR−) never happens in practice, as different type of devices with potentially unequal gate inputs switch on/off and affect the charging/discharging rates of the capacitive loading in different stages.

III. Stability Analysis and Design Procedures

A. Analysis of Stability

Let us apply the key expressions derived in Section II to characterize PM and GM in terms of C_L. Using the GM definition as the starting point, it can be derived from (1) as

$$\mathrm{GM} = -20\log\left(\frac{\sqrt{\left[1+\left(\frac{\mathrm{PX}}{z_1}\right)^2\right]\left[1+\left(\frac{\mathrm{PX}}{z_2}\right)^2\right]}}{\frac{\mathrm{PX}}{\mathrm{GBW}}\sqrt{\left(1-\frac{\mathrm{PX}^2}{\omega_0^2}\right)^2+\left(\frac{\mathrm{PX}}{Q\omega_0}\right)^2}}\right) \tag{10}$$

where PX is the phase crossover frequency derived as follows:

$$\tan^{-1}\left[\frac{\mathrm{PX}}{\omega_0 Q\left(1-\mathrm{PX}^2/\omega_0^2\right)}\right] - \tan^{-1}\left(\frac{\mathrm{PX}}{z_1}\right) + \tan^{-1}\left(\frac{\mathrm{PX}}{z_2}\right) = 90^\circ. \tag{11}$$

A solution for the above relationship is

$$\mathrm{PX} = \omega_0 \sqrt{\frac{\left(\frac{1}{R_{D1}C_{D1}}+\frac{1}{R_{D2}C_{D2}}\right)C_C}{\left(\frac{1}{R_{D1}C_{D1}}+\frac{1}{R_{D2}C_{D2}}\right)C_C - 2g_{mC}}}. \tag{12}$$

For the usual R_{D1}, R_{D2}, and g_{mC}, provided that

$$\left(\frac{1}{R_{D1}C_{D1}}+\frac{1}{R_{D2}C_{D2}}\right)C_C \gg 2g_{mC} \tag{13}$$

the former will be reduced to $PX \approx \omega_0$, so the GM can be written as

$$\begin{aligned} &\mathrm{GM} \\ &\approx 20\log\left(\frac{\omega_0}{\mathrm{GBWQ}}\right) - 10\log\left[1+\left(\frac{\omega_0}{z_1}\right)^2\right] \\ &\quad - 10\log\left[1+\left(\frac{\omega_0}{z_2}\right)^2\right] = \\ &\approx 20\log\left[\frac{2g_{mC}}{g_{m1}}\left(1+\frac{C_L}{g_{m2}g_{m3}g_{m4}R_1R_2R_3C_C}\right)\right] \\ &\quad -10\log\left[1+\frac{2g_{mC}g_{m2}g_{m3}g_{m4}(R_{D1}R_{D2}C_{D1}C_{D2})^2}{(g_{m2}+g_{m3})(R_{D1}C_{D1}+R_{D2}C_{D2})C_{D1}C_{D2}C_L}\right] \\ &\quad -10\log\left[1+\frac{(g_{m2}+g_{m3})(R_{D1}C_{D1}+R_{D2}C_{D2})C_C^2}{2g_{mC}g_{m2}g_{m3}g_{m4}(R_{D1}R_{D2})^2C_{D1}C_{D2}C_L}\right]. \end{aligned} \tag{14}$$

As deduced from (14), the stability will not be compromised by GM at large C_L values, for the trend is rising when C_L approaches infinity

$$\lim_{C_L\to\infty} \mathrm{GM} = 20\log\left(\frac{2g_{mC}}{g_{m1}g_{m2}g_{m3}g_{m4}R_1R_2R_3C_C}C_L\right) \tag{15}$$

with refer to PM definition, it can be formulated as

$$\mathrm{PM} \approx 90^\circ - \tan^{-1}\left[\frac{\mathrm{GBW}}{\omega_0 Q\left(1-\mathrm{GBW}^2/\omega_0^2\right)}\right] + \tan^{-1}\left(\frac{\mathrm{GBW}}{z_1}\right) - \tan^{-1}\left(\frac{\mathrm{GBW}}{|z_2|}\right). \tag{16}$$

Substituting from (4) to (7) and after some algebra, the above relation can be expanded to (17), as shown at the bottom of the next page.

Tending C_L to infinity, we get

$$\lim_{C_L\to\infty} \mathrm{PM} = 90^\circ - \tan^{-1}\left[\frac{g_{m1}(g_{m2}+g_{m3})R_1R_2R_3C_{D1}C_{D2}}{(R_{D1}C_{D1}+R_{D2}C_{D2})C_C}\right]. \tag{18}$$

In view of (18), it becomes evident that proper sizing of C_{D1}, C_{D2}, R_{D1}, and R_{D2} leads up to adequately high PM in very heavy CLs. In this sense, while zeros are nearly unaffected by the load, increasing C_L influences the GBW and

asymptotically the GBW decrease compensates the reduction in the high-frequency poles, which finally become real and separate (one pole remains asymptotically constant while the other falls with C_L at the same rate as GBW).The lower limit of C_L would not be limited by PM for a carefully sized compensation network, since tending C_L to zero ends up to

$$\lim_{C_L\to\infty} \mathrm{PM} = 90^\circ + \tan^{-1}\left[\frac{g_{m1}R_{D1}R_{D2}C_{D1}C_{D2}}{(R_{D1}C_{D1}+R_{D2}C_{D2})C_C}\right] - \tan^{-1}\left[\frac{g_{m1}(g_{m2}+g_{m3})}{2g_{mC}g_{m2}g_{m3}g_{m4}R_{D1}R_{D2}}\right]. \quad (19)$$

Decreasing C_L raises ω_0 as is apparent from (4), yielding a higher PM when its effect outperforms the GBW increase in (17). Instead of the PM, the GM dictates the stability conditions under the light CLs, as reducing C_L is accompanied by compromised stability in the internal Miller loop which causes a peaking in the frequency response [35]. Minimum GM usually happens at maximum Q factor ($Q_{\max}$) in the minimum load capacitor ($C_{L\min}$), which would be equivalent to $Q_{\max} = \omega_0/\mathrm{GBW}$ if the contribution of the zeros in (14) was neglected. Regarding this scenario, a maximum $Q_{\max}$ may be set in (5) to evaluate $C_{L\min}$ as

$$C_{L,\min} \approx \frac{g_{m2}g_{m3}g_{m4}(R_{D1}C_{D1}+R_{D2}C_{D2})C_C^2}{2g_{mC}(g_{m2}+g_{m3})C_{D1}C_{D2}Q_{\max}^2}. \quad (20)$$

The minimum C_L is dependent on R_{D1} and R_{D2} rather than the output resistors and can be lowered either by increasing g_{mC} of the cascode devices or by reducing R_{D1} and R_{D2}, the former being at the cost of increased power consumption while the latter comes at the price of compromised PM at higher C_L due to a large z_1 frequency (6).

B. Design Guidelines

The transfer function along with the derived equations for PM and GM were used to develop an iterative design procedure based on targeted bandwidth and stability margins over a prescribed C_L range. For this purpose, the parasitics were extracted and updated with the help of computer simulation at the beginning of each sizing sequence. Starting from the transconductance values, a primitive g_{m1} value needs to be calculated following the design specifications that take into account the input-referred noise, matching, and, most importantly, the g_m/I_D ratio based on the power, area, and speed envelopes [36]. A maximum GBW, i.e., $\mathrm{GBW}_{\max} = g_{m1}/C_C$ can be evaluated afterward through a maximum GBW limited by $C_{L,\min}$ when the feedback factor is set to unity, since the final PM and GM would be large enough to support such approximation. With the $\mathrm{GBW}_{\max}$ acquired, an initial C_C can be achieved from g_{m1}. The transconductor g_{mC} can be subsequently achieved from g_{m1}, by observing that critical stability margins happen at $C_{L,\min}$, so careful placement of poles and zeros is a prerequisite here. Pertinently, the minimum GM can be estimated from (14) as

$$\mathrm{GM}_{\min} \approx 20\log\left(\frac{2g_{mC}}{g_{m1}}\right) - 10\log\left[1+\left(\frac{\omega_{0,\max}}{z_1}\right)^2\right] - 10\log\left[1+\left(\frac{\omega_{0,\max}}{z_2}\right)^2\right] \quad (21)$$

where $\omega_{0,\max}$ is the maximum pole-pair frequency measured from (4) for $C_{L,\min}$. The g_{mC}/g_{m1} ratio must be selected carefully for $\mathrm{GM}_{\min}$ not to become negative in any process-voltage-temperature (PVT) corners. Setting $g_{mC} = \alpha g_{m1}$ and picking, e.g., $\alpha = 4$ gives 18 dB by the first term, a fairly sufficient margin to counteract the adverse contributions of the second and the third terms caused by the zeros. Sizing g_{m2}, g_{m3}, and g_{m4} is the next step and should rely on the designated operating regions and the relevant power/area trade-offs.

The resistors R_{D1} and R_{D2} are then sized based on the proper location of the zeros. Placing the first zero right after the maximum GBW frequency, i.e., $\gamma \times \mathrm{GBW}_{\max}$ which happens at $C_{L,\min}$, we get

$$z_1 = \gamma\cdot\mathrm{GBW}_{\max} \Rightarrow \frac{1}{R_{D1}C_{D1}} + \frac{1}{R_{D2}C_{D2}} = \gamma\cdot\mathrm{GBW}_{\max}. \quad (22)$$

The second RHP zero, z_2, should be positioned well beyond $\mathrm{GBW}_{\max}$ simultaneously. Choosing $|z_2| > 10\ \mathrm{GBW}_{\max}$ would be a safe margin for the phase contribution of z_2 not to disturb the frequency response, consequently

$$z_2 > 10\cdot\mathrm{GBW}_{\max} \Rightarrow R_{D1}R_{D2} > 5\frac{g_{m2}+g_{m3}}{\alpha g_{m2}g_{m3}g_{m4}}. \quad (23)$$

The sizing of C_{D1} and C_{D2} is relied on $R_{D1}C_{D1}+R_{D2}C_{D2}$, the term that contributes directly to the absolute PM and its limits derived in (18) and (19). Larger C_{D1} and C_{D2} improve the PM but also add to the silicon footprint and vice-versa. After setting C_{D1} and C_{D2}, the next step is to modify the initial g_{m1} and the consequent C_C and g_{mC}. To estimate the required C_C, we set $\omega_{0,\max}$ equal to $\beta\cdot\mathrm{GBW}_{\max}$ and choose β between

$$\mathrm{PM} = 90^\circ - \tan^{-1}\left\{\frac{g_{m1}(g_{m2}+g_{m3})R_1R_2R_3C_{D1}C_{D2}C_L}{C_C\left[\begin{array}{c}(g_{m2}g_{m3}g_{m4}R_1R_2R_3C_C+C_L)(R_{D1}C_{D1}+R_{D2}C_{D2}) \\ -\frac{g_{m2}g_{m3}g_{m4}(g_{m2}+g_{m3})(g_{m1}R_1R_2R_3)^2C_{D1}C_{D2}C_L}{2g_{mC}(g_{m2}g_{m3}g_{m4}R_1R_2R_3C_C+C_L)}\end{array}\right]}\right\} + \tan^{-1}\left(\frac{g_{m1}g_{m2}g_{m3}g_{m4}R_{D1}R_{D2}R_1R_2R_3C_{D1}C_{D2}}{(g_{m2}g_{m3}g_{m4}R_1R_2R_3C_C+C_L)(R_{D1}C_{D1}+R_{D2}C_{D2})}\right) - \tan^{-1}\left(\frac{g_{m1}(g_{m2}+g_{m3})R_1R_2R_3C_C}{2g_{mC}g_{m2}g_{m3}g_{m4}R_{D1}R_{D2}R_1R_2R_3C_C+2g_{mC}R_{D1}R_{D2}C_L}\right) \quad (17)$$

2 and 3 to allow for sufficient GM and PM. Combining (8) with (4), we get

$$C_C = \beta g_{m1}\sqrt{\frac{(g_{m2}+g_{m3})C_{D1}C_{D2}C_{L,\min}}{2g_{mC}g_{m2}g_{m3}g_{m4}(R_{D1}C_{D1}+R_{D2}C_{D2})}}. \quad (24)$$

Substituting $g_{mC} = \alpha g_{m1}$ from the former assumptions, C_C will befound by

$$C_C = \frac{\beta}{\alpha}\sqrt{\frac{g_{mC}(g_{m2}+g_{m3})C_{D1}C_{D2}C_{L,\min}}{2g_{m2}g_{m3}g_{m4}(R_{D1}C_{D1}+R_{D2}C_{D2})}}. \quad (25)$$

Combining (22) and (24), the coefficients α, β, and γ need to be adjusted such that a sufficiently high $\mathrm{GM_{min}}$ is resulted from the following equation:

$$\mathrm{GM_{min}} \approx 20\log(2\alpha) - 10\log\left\{\left[1+\left(\frac{\beta}{\gamma}\right)^2\right]\left[1+\left(\frac{\beta}{10}\right)^2\right]\right\}. \quad (26)$$

The above procedure should be reiterated and enriched by simulations as the initial assessments of the parasitics and some design parameters are not accurate. Simulation of the zeros and poles under the component and process variations would be also necessary in the final phase. A prototype of the proposed OTA was realized by taking into account the described design rules, using an algorithm that optimizes the device sizes for lesser power consumption and area.Measurement and simulation results are discussed in Section IV.

IV. Results

A. Simulation Results

The operation of the proposed amplifier was analyzed through the simulation results in a 65-nm standard CMOS process under a 1.2-V voltage supply. Optimizations were conducted according to the design guidelines in Section III to reach a stable operation with maximum bandwidth over a 5–100 nF C_L range. The final configuration consumes 140 μA current in a total area of 0.0086 mm^2. Table I outlines the transistor sizes and the small-signal parameters. Notably, the value of g_{mC} was set to $4g_{m1}$ in line wirh the design guidelines described in the previous section. Table II presents the operation details for $C_L = 5$ nF. The GBW product was adjusted to 5 MHz in this case, while the minimum GM is derived as 9 dB thanks to $\alpha = 4$ as discussed earlier.

Fig. 4(a) shows the loop-gain frequency responses at various load capacitors. The main pole depends on the Miller capacitors for small C_L values, becoming a function of the load capacitor for heavy C_Ls. Fig. 4(b) presents the step response of the amplifier in buffer configuration to the falling and rising edges of a 400-mV input. The supply current drawn by the output stage lies in the almost zero to some mA range depending on the step size and C_L, while the bias current of the output stage indicates a tolerance of ±12% and ±8% across the 0.2–0.6 V output voltage and 1.2−1.5 V supply voltage ranges, respectively.

The OTA is found to be stable with adequately high stability margins over the designative C_L range from 5 nF to infinity,

TABLE I
Transistor Sizes, Small-Signal Parameters, and Passive Components Values

Stage #	Transistor	W/L	Param.	Value
1	M_0	64.1 µ / 0.5 µ	g_{m1}	81µA/V
	$M_1 - M_2$	8.5 µ / 0.3 µ	g_{mC}	340µA/V
	$M_3 - M_4$	52.3 µ / 1.7 µ		
	$M_5 - M_6$	6.3 µ / 0.2 µ		
	$M_7 - M_8$	36.3 µ / 0.2 µ		
	$M_9 - M_{10}$	2.9 µ / 0.3 µ		
2	M_{11}	2.3 µ / 0.4 µ	g_{m2}	56µA/V
	M_{12}	20.0 µ/1.7 µ		
3	M_{13}	12.8 µ / 1.7 µ	g_{m3}	114µA/V
	M_{14}	4.4 µ / 0.5 µ	g_{mf1}	95µA/V
4	M_{15}	9.6 µ / 0.2 µ	g_{m4}	1.2mA/V
	M_{16}	40.8 µ / 0.2 µ	g_{mf2}	1.6 mA/V
Comp. network	C_{D1}			0.4 pF
	R_{D1}			700 kΩ
	C_{D2}			0.6 pF
	R_{D2}			500 kΩ
	C_C			2.0 pF

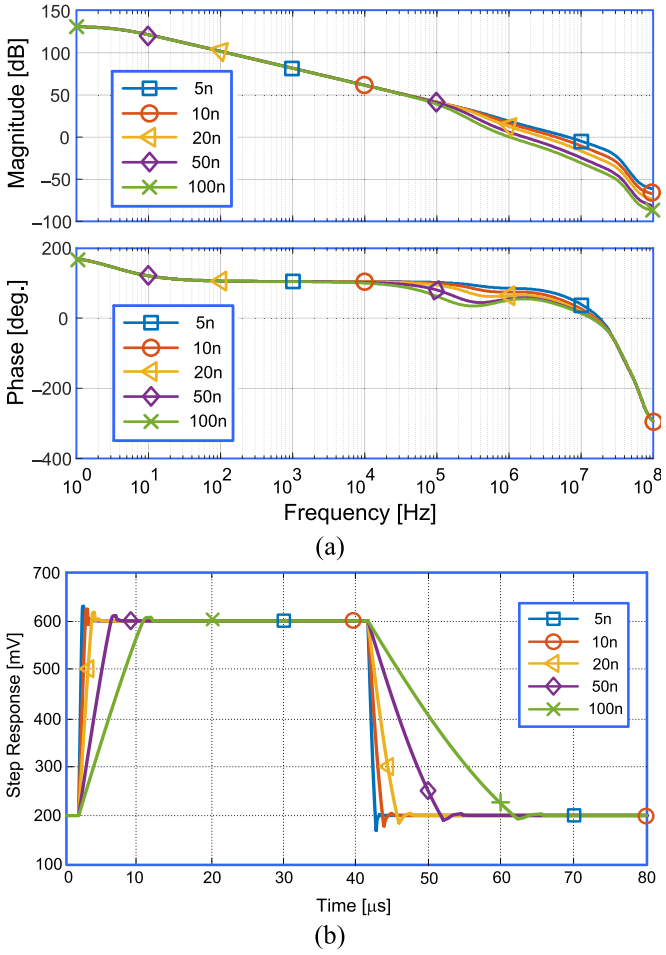

Fig. 4. Simulated performance for different C_L values. (a) Open-loop frequency response. (b) Unity-gain Settling response ×10.

becoming gradually unstable for lighter CL due to insufficient GM. The stability is typically limited by GM rather than PM in lighter C_Ls. Nevertheless, it is possible to configure the compensation network for the proposed OTA such that it drives

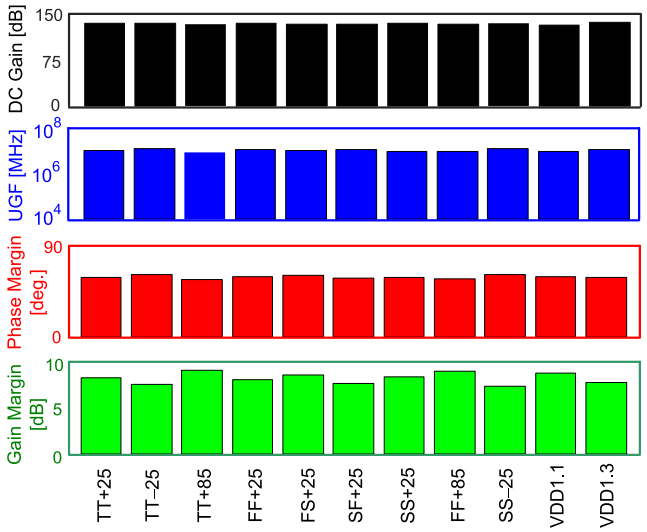

Fig. 5. Performance comparison in different process corners for $C_L = 5$ nF.

TABLE II
DESIGN PARAMETERS FOR THE NOMINAL $C_L = 5$ nF

Voltage Supply [V]	1.20
Quiescent Current [µA]	140
DC Gain [dB]	130
UGF [MHz]	5.15
PM [deg.]	58.11
GM [dB]	8.86

the more common on-chip loads. For instance, reducing the original C_C, R_{D1}, and R_{D2} into 0.7 pF, 68 kΩ, and 12 kΩ extends the lower C_L limit to as low as 5 pF consistent with the results from (20). The maximum C_L limit, however, drops to around 250 pF because of the additional phase lag caused by the second term in (18) which negates the PM.

B. Corner and Monte-Carlo Analysis

Corner and Monte-Carlo simulations were executed to investigate the immunity of the design against local and systematic variations. Fig. 5 illustrates the loop-gain parameters in the minimum C_L of 5 nF, which takes into account the realistic deviations of the voltage supply (±5%) and temperature (–25 °C to 85 °C) across the TT = typical, SS = slow *n*MOS, slow *p*MOS, FF = Fast *n*MOS, and Fast *p*MOS process corners. Table III lists the worst and the best cases of each parameter. The design was found to be stable in different process, voltage, and temperature corners, and the GBW and dc gain distributions were acceptable.

Monte-Carlo simulation results (1000 runs) are summarized in Table IV for the nominal CL of $C_L = 5$ nF. The mean values are slightly different from the simulated design parameters set. The standard deviation is contained for each parameter with a maximum coefficient of deviation (σ/μ), registered for the unity-gain frequency (UGF), approximately equal to 3.5%.

C. Measurement Results and Comparisons

The proposed OTA with the chip micrograph shown in Fig. 6 was designed in a standard 65-nm CMOS. The experimental setup, not depicted for its standard arrangement, includes double power suppliers besides a waveform generator and the characterization is performed on seven samples with bond-wire. An oscilloscope, Tektronix TDS5054B, was utilized to examine the transient output and input responses. To measure the frequency response, an E5061B LF-RF network analyzer (ENA) from Keysight Technologies was also employed. Fig. 7 illustrates the measured open-loop gain frequency responses for C_L ranging between 4.7 and 100 nF. Above 100 dB dc gain was measured with the UGF frequency of about 4.09 and 0.27 MHz and a PM of 72° and 87° at 4.7 and 100 nF loads, respectively, owing to the UGF being scaled by C_L, as predicted by (8).

The measured UGF turns out to be less than about 21% as compared to their nominal values, which is surely attributed to the internal parasitics as well as the layout-dependent effects. For instance, metal-oxide-metal (MOM) and high sheet-resistance capacitors and resistors were used in the compensation network, respectively. Such components, however, suffer from high process excursions, especially for the MOM case, being about 25%–30% of variations, but have been

TABLE III
BEST AND WORST PARAMETERS OVER CORNERS

Parameter	Value	Corner
Min. *UGF*	4.47 MHz	TT (+85°C)
Min. *PM*	56.04 °	TT (+85°C)
Min. *GM*	7.91 dB	SS (−25°C)
Min. DC Gain	127.90 dB	VDD = 1.1 V
Max. *UGF*	6.15 MHz	SS (−25°C)
Max. *PM*	60.94 °	SS (−25°C)
Max. *GM*	9.74 dB	TT (+85°C)
Max. DC Gain	131.9 dB	VDD = 1.3 V

TABLE IV
SUMMARY OF MONTE-CARLO ANALYSIS (1000 RUNS @ $C_L = 5$ nF)

Parameter	μ	σ
UGF [MHz]	5.164	0.18
PM [deg.]	58.19	0.90
GM [dB]	10.04	0.24
I_{DD} [µA]	134.6	3.80
SR [mV/µs]	429.3	1.46

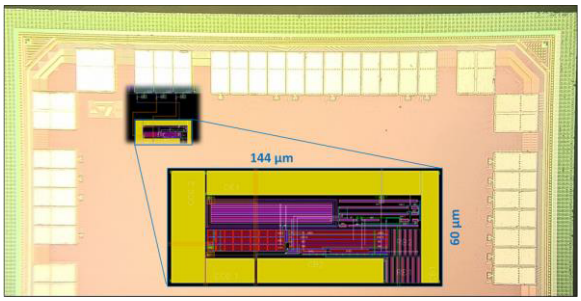

Fig. 6. Chip microphotograph.

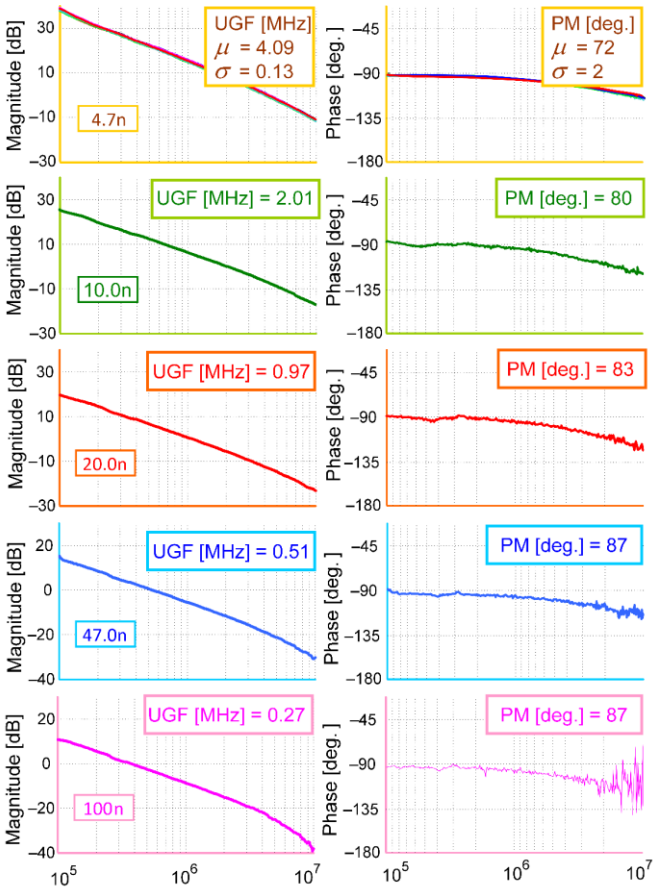

Fig. 7. Measured loop-gain frequency response at different C_L.

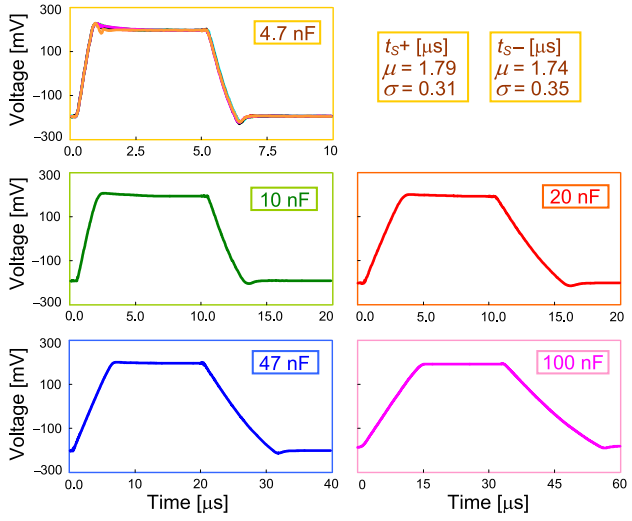

Fig. 8. Measured loop-gain frequency response at different C_L.

exploited for more compactness and lower equivalent series resistance (ESR).

Fig. 8 exhibits the step response of the unity-gain OTA subject to an input step size of 400 mV. As for $C_L = 4.7$ nF, the mean(μ) positive and negative 1% settling times are 1.79 and 1.74 μs with a standard deviation (σ) of 0.31 and 0.35 μs, respectively.

TABLE V
COMPARISON WITH THREE-STAGE OTAS

	[9] 2013	[37] 2016	[25] 2018	[26] 2020	This work
Tech. [nm]	350	350	350	130	**65**
#stages	3				**4**
Area [mm^2]	0.016	0.003	0.0025	0.006	**0.0086**
I_{DD}[μA]	72	24.9	6.36	185	**138.2**
A_0 [dB]	>100	>100	113	71.25	**132**[a]
C_L[nF]	1–15	5–15	5–100	4.45–50	**4.7–100**
C_T [pF]	2.6	1	0.5	0	**3**
$C_{L,max}/C_{L,min}$	15	3	20	11.24	**20**
UGF [MHz]	3.37–0.95	2.85–2.38	2.88–0.43	5.41–0.46	**4.1–0.27**
SR[V/μs]	0.59–0.22	0.76–0.3	0.36–0.045	0.49–0.04	**0.53–0.03**[a]
PM [deg.]	83–52	78–47	46–59	69–90	**72–87**
1% t_s [μs]	1.28–4.49	0.63–0.93	2.05–7.7	0.57–4.62	**1.77–16**
IFOM_S[(1)]	198	1'433.7	6'761	124.3	**195.37**
IFOM_L[(2)]	45.8	180.7	707.6	10.81	**25.99**
IFOM_{SA}[(3)]	12'370	482.7	2'704'403	20'721	**22'717**
IFOM_{LA}[(4)]	2'865	60.8	283'019	1'801	**3'022**

[a]:minimum value

TABLE VI
COMPARISON WITH FOUR-STAGE OTAS

	[38] 2008	[39][b] 2014	[32] 2015	[30] 2020	This work
Tech. [nm]	120	65	350	130	**65**
Area [mm^2]	0.017	--	0.014	0.007	**0.0086**
I_{DD}[μA]	1400	80	52	146	**138.2**
A_0 [dB]	108	91	173[a]	107	**132**[a]
C_L[nF]	0.5	1	0.33–1	0.4–10	**4.7–100**
C_T [pF]	17.6	1	9.7	3.1	**3**
UGF [MHz]	40.2	19.06	2.98	2.75–1.18	**4.1–0.27**
SR [V/μs]	17.52	1.45	1.18	0.92–0.14	**0.53–0.03**[a]
PM [deg.]	62	59	55	48–61	**72–87**
1% t_s [μs]	0.14	0.33	0.46	0.33–9.75	**1.77–16**
IFOM_S[(1)]	14.36	238.25	57.31	97	**195.37**
IFOM_L[(2)]	6.26	18.13	22.69	11.51	**25.99**
IFOM_{SA}[(3)]	845	--	4'093	13'855	**22'717**
IFOM_{LA}[(4)]	368	--	1'621	1'644	**3'022**

[a]:minimum value
[b]:simulated results

The positive/negative SR+/SR− were measured as 0.65/0.53 and 0.05/0.03 V/μs for 4.7 and 100 nF CLs, respectively. Altogether, the step responses demonstrate very close agreement with the simulation results. A longer settling time was, however, appreciated owing to the aforementioned internal parasitics and layout dependent effect as well as the loading of the bond wires and the experiment setup.

The figures of merit, $\text{IFOM}_S = \text{GBW} \times C_{L,\text{max}}/I_{DD}$ and $\text{IFOM}_L = \text{SR} \times C_{L,\text{max}}/I_{\text{DD}}$, were employed to quantify the small-signal and large-signal characteristics in the upper limit of C_L, whereas $\text{IFOM}_{\text{SA}} = \text{IFOM}_S/\text{Area}$ and $\text{IFOM}_{\text{LA}} = \text{IFOM}_L/\text{Area}$ were added to include the active area [2]. Tables V and VI compare the performance metrics of the proposed amplifier with some of the state-of-the-art three- and four-stage OTAs based on the above FOMs. The minimum among SR+/SR− is reported for each C_L and is used later to find the large-signal FOMs.

The proposed four-stage OTA does not outperform all the other solutions among the three-stage OTAs driving a wide C_L range, which is mainly due to the increased number of gain stages and a more complicated compensation network.

However, among the fabricated and tested four-stage amplifiers, it outperforms all the topologies presented in Table VI when taking into consideration the active area, consuming current, range of stability, as well as the large- and small-signal operations. The proposed OTA can drive the widest C_L range up to 100 nF for analogous current consumption and compensation capacitor sizes.

V. Conclusion

The principle of hybrid-cascode frequency compensation was applied to a four-stage feedback amplifier, thus leading up to improved performance metrics with respect to the prior art. Other than the local Miller compensations used for the stability of inner gain stages, two Miller capacitors with current buffers are applied according to the idea. A reliable operation and a wide range of the CLs spanning from 4.7-nF up to infinity were achieved by shaping the frequency response such that stability is ensured initially by the Miller and, gradually, by the load capacitor in lower and higher CLs, respectively. The proposed amplifier was fabricated in a 65-nm CMOS, consuming 168 μW power while occupying an active area of 0.0086 mm^2. Experimental results indicate a gain factor higher than 100 dB, and a PM of at least 72° for the CLs beyond 4.7-nF.

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