Actual Reasons Involving Turn-Off Losses Improvement With Increasing Load and Gate Resistance in MOSFETs Enhanced With Kelvin Source

Santi Agatino Rizzo, *Member, IEEE*, and Nunzio Salerno, *Senior Member, IEEE*

***Abstract*—This article explains the actual reasons behind the improvement in terms of turn-OFF energy losses (Eoff) reduction, obtained using Kelvin pin (4-lead, 4L) MOSFETs instead of 3L ones. Eoff increases by increasing gate resistance and load, but the experimental results reveal that the increment is less in 4L than in 3L MOSFETs. Analyzing the turn-OFF waveforms and adopting circuit analysis, the article first proves that the common argument about the undesired effect of the parasitic source inductance in 3L MOSFETs is misleading. Then, the reasons behind the aforesaid improvement in 4L MOSFETs with increasing gate resistance and load are described by means of the derived analytical expressions. Finally, the analysis of the equations has provided helpful information at the design stage, also accounting for the different device technologies. In particular, the improvement obtained using 4L MOSFETs reduces as the driving loop parasitic inductance increases and evanesces if its value becomes comparable with the power loop parasitic inductance.**

***Index Terms*—Circuit analysis, energy efficiency, packaging, power MOSFET, semiconductor device modeling.**

I. Introduction

THE design of efficient power converters is highly desirable to obtain environmental-friendly electric systems and reduce operating costs [1], [2], [3]. Power density increment is more and more required in many applications and from consumers [4]. The wide-bandgap (WBG) devices present good features that facilitate the achievement of these targets [5], [6]. Using an additional source, the Kelvin pin, is helpful to obtain a highly efficient and compact converter also adopting Silicon devices, thus benefiting from the technology maturity. On the other hand, the WBG devices can benefit from the use of the Kelvin pin too [7], [8]. Moreover, these advantages deriving from the Kelvin pin have also been proved in other device technologies [9]. The main problem, solved by 4L MOSFET, is the coupling between the driving and power loop due to the source parasitic inductance of the 3L. Some works have proposed to optimize the gate driver to mitigate the effect of this parasitic inductance [10], [11], [12]. In other cases, layout and packaging guidelines have been proposed [13], [14], [15], [16]. However, using the 4L MOSFET is the best state-of-art solution.

The advantages deriving from the use of a MOSFET equipped with a Kelvin pin (4L MOSFET) in comparison with a 3-lead device (3L MOSFET) increase as the current increases, making the former interesting in high currents applications [17]. More specifically, for both kinds of packages, the switching losses increase with increasing current, but the increment is lower in 4L MOSFETs compared to 3L ones as the current increases. The lower switching losses involve lower heating of the device and other components, thus improving the converter lifetime and/or reducing the need for bulky cooling systems. Moreover, 3L MOSFET could suffer undesired self-turn-ON at the turn-OFF [18]. Finally, the parasitic inductance can affect the protection performance under overcurrent/short circuit conditions [19].

Regardless of the technology, these advantages obtained during the commutation are commonly attributed to the decoupling of the driving and power loops [20], [21]. More specifically, in 3L MOSFETs, during the turn-OFF, the decreasing current opposites to the reduction of the gate-source voltage, thus slowing down the switching [22]. This is due to the voltage drop across the source parasitic inductance, which affects the gate-source voltage since this inductance belongs both to the driving and power loops [see Fig. 1(a)] [23]. In 4L MOSFET, this voltage drop does not affect the gate-source voltage since the source parasitic inductance belongs to the power loop only [see Fig. 1(b)]. Similar reasoning is usually adopted to explain the advantages during the turn-ON [24]. Indeed, such an interpretation is valid only for the turn-ON, not for the turn-OFF, as we will prove in the following.

The contributions of this article are listed as follows.

1) It proves, in Section III, that the common explanation (consolidated in academia and industry) about the effect of the source inductance on the turn-OFF of 3L and 4L

Manuscript received 16 August 2022; revised 29 November 2022 and 4 January 2023; accepted 27 January 2023. Date of publication 9 February 2023; date of current version 10 July 2023. This work was supported by "Advanced power-trains and systems for full electric aircrafts - 2017MS9F49" funded by the "Ministero dell'Istruzione dell'Università e della Ricerca" under the call PRIN 2017. *(Corresponding author: Santi Agatino Rizzo.)*

The authors are with the Department of Electrical Electronic and Computer Engineering, University of Catania, 95124 Catania, Italy (e-mail: santi.rizzo@dieei.unict.it; nunzio.salerno@unict.it).

Color versions of one or more figures in this article are available at https://doi.org/10.1109/TIE.2023.3243272.

Digital Object Identifier 10.1109/TIE.2023.3243272

This work is licensed under a Creative Commons Attribution 4.0 License. For more information, see http://creativecommons.org/licenses/by/4.0/

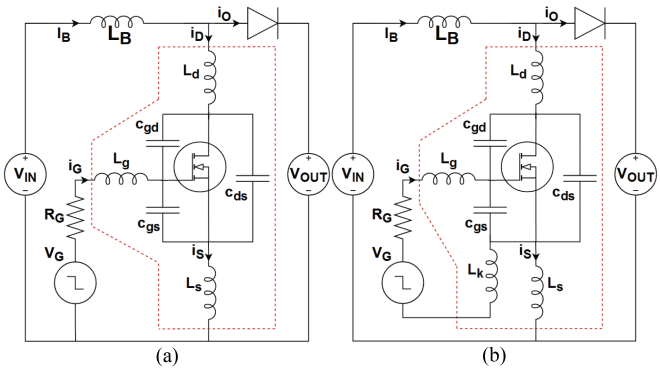

Fig. 1. Ideal boost converter where only the parasitic components of the MOSFET are reported (inside the red dashed line). (a) 3L. (b) 4L.

MOSFETs is misleading. The proof is obtained by comparing the common turn-OFF equations with the experimental turn-OFF waveforms reported in this article and literature.

2) It highlights, in Section IV, the actual reasons why turn-OFF energy losses increase less in 4L than in 3L MOSFETs. with increasing gate resistance and load current (this is the main contribution).
3) It provides, in Section IV, practical information for the layout designer.

The rest of this article is organized as follows. Section II reports: 1) the comparison between 3L and 4L MOSFETs presented so far by Academia and Industry; 2) a test vehicle to compare the switching losses for increasing gate resistance and load current, for confirmation purposes. Section III reports: 1) the well-consolidated phenomenon interpretation in Academia and Industry by recalling the turn-OFF equations usually adopted to support this common interpretation; 2) some test vehicle turn-OFF switching waveforms used for proving that the aforementioned common interpretation is misleading, and results from the literature used with the same purpose. Section IV reports: 1) the correct circuit analysis of 3L MOSFETs, which is also based on the analysis reported in Section III; 2) the circuit analysis of 4L MOSFETs; 3) a comparison of the results of the two circuit analyses to highlight the actual reasons for which the difference between the power losses of 3L and 4L MOSFETs increases with increasing gate resistance and load current. Finally, Section V concludes this article.

II. Comparison Between the Switching Losses of 3L and 4L MOSFETs

A. Academia and Industry Experience

A demonstration board has been prepared in [25] to verify the impact of parasitic inductance on both the commutation times and power losses of 3L and 4L MOSFET. The results revealed that the improvement obtained by 4L MOSFET increases as the load current increases. An experimental comparison of the turn-ON and turn-OFF switching losses in 3L and 4L MOSFETs has been presented in [20]. The results have shown that both switching losses increases as the gate resistance increases but the slope of the losses increment is larger in 3L MOSFET. The improvements obtained using a 4L MOSFET are discussed and analyzed in [26]. Then, a new technique based on an inductive rather than resistive gate driver impedance was proposed to mitigate or even completely compensate for the effects of source inductance in 3L MOSFET. In [17], the experimental results highlighted that the 4L MOSFET performs better than the 3L one in high currents applications, while the higher cost of the former limits their use in low-current applications. A comparison of the double pulse test switching losses of a 3L and 4L SiC MOSFET has been reported in [27]. The comparison has highlighted that the difference between the case temperature of the two devices increases as the load increases as well as the gate resistance increases. The gate-source spikes occurring during the MOSFET commutation have been analyzed in [18] to highlight the advantages enabled by 4L devices in terms of spike reduction.

The turn-ON energy losses measured experimentally for different load conditions in [24] have shown that the energy advantage of the 4L is reduced at low load. This is due to the drain-source voltage waveform of the 3L device, which is more similar to those of the 4L one at a low current. More specifically, the drain-source voltage waveform of the 3L device usually presents a plateau due to the voltage drop across the parasitic inductances during the current rising and due to the clamp imposed by the diode until it conducts. The higher current speed of the 4L MOSFET involves that the plateau should occur at a lower value of the drain-source voltage, and then this voltage takes longer to reach the clamp value. On the other hand, the higher current speed of a 4L MOSFET involves a reduced time necessary for it to reach the load current, thus unclamping the diode earlier. Consequently, the drain-source plateau does not occur, thus reducing turn-ON losses.

The switching loss in the 4L SiC MOSFETs is lower affected by package degradation, and the difference with the 3L ones increases at high currents [28]. When the gate resistance is decreased to increase the turn-ON speed of a 3L MOSFET, in order to reduce the gap with the 4L performance, high turn-ON oscillations occur. In [29], a gate driver able to suppress these oscillations has been proposed. In [30], the results highlighted that the switching energy reduction in 4L MOSFETs increases as the load increases. This advantage also intensifies as the gate resistance increases. Similarly, this [31] has also highlighted that 4L MOSFETs present reduced switching losses, oscillations, and voltage spikes than 3L ones, and the improvement is more significant at high currents.

An Infineon application note [32] has also confirmed that the difference between the switching losses between 3L and 4L MOSFETs increases with increasing load current. Also, an STMicroelectronics application note [33] has underlined that this difference also increases with increasing gate resistance.

B. Experimental Analysis of 3L and 4L MOSFETs E_{off}: Impact of the Load Current and Gate Resistance

The analysis of the literature has revealed that the improvement obtained using 4L MOSFETs increases with increasing load

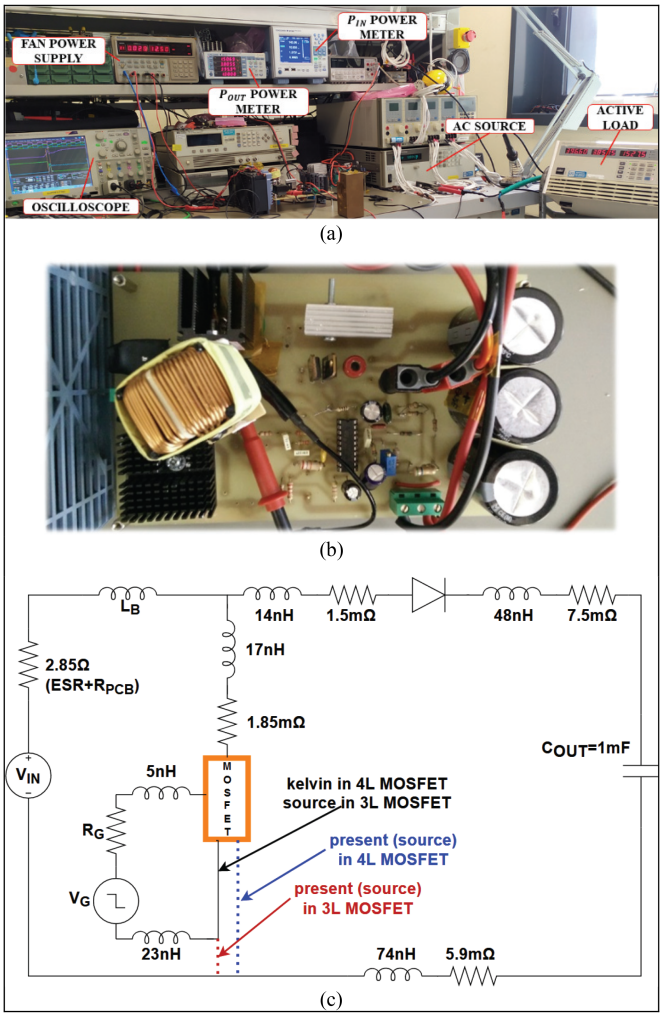

Fig. 2. Experimental setup. (a) Overall view. (b) Boost converter.(c) Point-to-point main parasitic components.

TABLE I
POWER CONVERTER AND DEVICE SPECIFICATIONS

Converter			
V_{IN}	200 V	L_B	0.5 mH
V_o	400 V	V_G	0 V (off) 12 V (on)
MOSFET			
Breakdown	650 V	V_{th}	4 V
Current rating	58 A (@25 °C) 36.5 A (@100 °C)	On-state resistance	37 mΩ (@ 25°C and V_{GS}=10 V & I_{ds}=29 A)

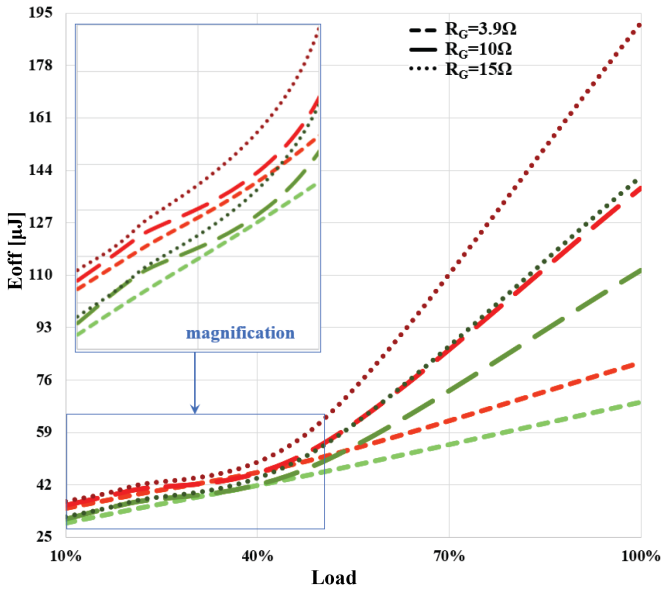

Fig. 3. Turn-OFF energy losses trend with increasing load for 3L (red) and 4L (green) MOSFET for different gate resistance values.

current and gate resistance. In this section, an independent investigation is carried out by evaluating the turn-OFF energy losses for different combinations of load current and gate resistance.

The test vehicle is the boost converter reported in Fig. 2. The test equipment consists of: Agilent ac–dc power supply 6813B; 1 GHz Oscilloscope Tektronix MS05140; Tektronix current probe TCP0030; Tektronix voltage passive probe (1:10); Passive voltage probe LeCroy P6139B (1:100); Flir Thermocamera; Power Meter Yokogawa WT310; Chroma 6314 electronic load. The gate driver is TC4422. Fig. 2(c) reports the point-to-point main parasitic components of the PCB. The parasitic inductors in series with L_B are neglected since they present a negligible inductance compared to the boost inductor. For similar reasons, the parasitic resistors in series with the gate resistor are neglected. The device parasitics (due to bonding wire, terminals, and so on) are inside the MOSFET block. Table I reports quantities related to the converter and the devices [34].

Fig. 3 reports the variation of the energy loss, Eoff, during the turn-OFF versus increasing load for different gate resistances. The results highlight that the losses increase more in 3-L MOSFET than in 4-L with increasing load. Therefore, the improvement, in terms of power loss reduction, obtained using 4-lead MOSFETs actually increases as the load increases. An interesting aspect arising from the results is that the gate resistance modulates this phenomenon. More specifically, the loss difference between the 3L and 4L MOSFETs increases with increasing gate resistance. For example, at full load, the loss difference between 3L and 4L quadruples when passing from $R_G = 3.9$ to $R_G = 15$. The same effect occurs on the turn-ON energy losses, although the reasons are different, as proved by Gaito et al. [24].

III. COMMON MISLEADING INTERPRETATION OF THE IMPACT OF THE SOURCE PARASITIC INDUCTOR ON THE TURN-OFF LOSSES IN 3L MOSFETS

This section first recalls the common explanation about the effect of the source inductance on the turn-OFF of 3L and 4L MOSFETs. It is worth noticing that this explanation is well consolidated in academia and industry as it emerged from the literature analysis, and it has led to a misleading interpretation of the impact of the source parasitic inductor on the turn-OFF losses of 3L and 4L MOSFETs. Some experimental waveforms of the

turn-OFF for different gate resistance values and load conditions, which are analyzed in Section II to obtain Fig. 3 are reported in the following to highlight the incorrectness of the common explanation.

A. Common Reasoning About the Undesired Interaction Between Current and Gate-Source Voltage During 3L MOSFET Turn-Off

In a power converter, there are many parasitic elements due to the PCB and, more in general, due to the interconnection among devices, components, power supply, and so on. Even an ideal design of the converter that eliminates any parasitic element cannot totally avoid the presence of parasitic components that are due to the MOSFET itself. Anyway, the MOSFET parasitic components are sufficient to pinpoint the effect of the source inductance since the difference with an actual case is mainly quantitative instead of qualitative. Fig. 1 shows a significant case where only the parasitic capacitance and inductance of the MOSFET and some PCB parasitic components are added to the circuit of the boost converter. More specifically (also considering Fig. 8) they are as follows:

L_d parasitic inductance from the internal drain terminal (node D) to the lead connection with the PCB, plus the parasitic inductance from that point to node E;
L_s parasitic inductance from the internal source terminal (node S) to the lead connection with the PCB, plus the parasitic inductance from that point to node N;
L_g parasitic inductance from the internal gate terminal (node G) to the lead connection with the PCB, plus the parasitic inductance of the driver edge.

The boost converter has been chosen as the test vehicle because it enables easily setting the MOSFET current when the turn-OFF starts, by a simple tuning of the electric load. In the following analysis, the input and output voltages have been considered constant without losing generality.

When the 3L MOSFET is considered, the gate-source voltage v_{GS}, across the parasitic capacitor c_{gs} can be obtained by applying the Kirchhoff's voltage law (KVL) to the driving loop [see Fig. 1(a)]

$$v_{GS} = V_G - R_G i_G - L_g \frac{di_G}{dt} - L_s \frac{di_S}{dt}. \tag{1}$$

During the turn-OFF, V_G is zero (or negative in SiC MOSFETs) and the decreasing v_{GS} asymptotically tends to this value. The MOSFET current is decreasing, then the derivative of i_S is negative, thus involving a positive quantity in (1), which opposes to the reduction of v_{GS}. Consequently, after a given time τ, from the beginning of turn-OFF, the v_{GS} value is greater than if the current i_S does not affect it (i.e., when L_S is zero)

$$v_{GS,Ls=0}(\tau) < v_{GS,Ls>0}(\tau). \tag{2}$$

By assuming that the turn-OFF switching losses occur while the MOSFET is in the active region, recalling that the MOSFET current is proportional to the gate-source voltage in this region

$$i_S \propto g_m (v_{GS} - V_{TH}) \tag{3}$$

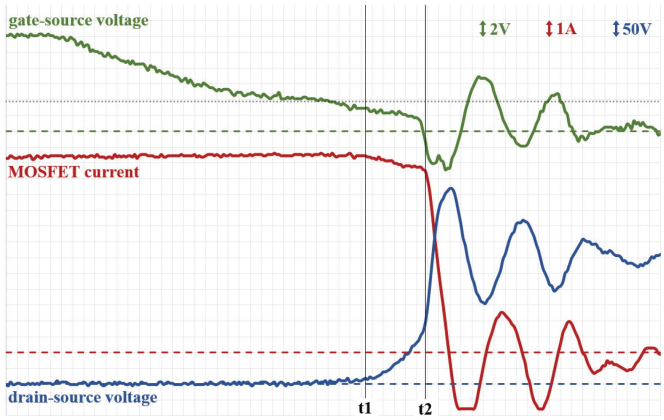

Fig. 4. Waveforms during the turn-OFF of a 3L MOSFET (5 ns/div). The dashed lines are the 0-axis of the waveform with the same color. The gray dotted line indicates the threshold voltage (at 53.7 °C).

and according to the previous considerations about v_{GS} (relation 2), it follows that, at a given time τ, after the start of the turn-OFF, the value of i_S is greater than if i_S itself has no effect on v_{GS} (i.e., when L_S is zero)

$$\begin{matrix}\text{relation 2}\\ \text{relation 3}\end{matrix} \Rightarrow i_{S,Ls=0}(\tau) < i_{S,Ls>0}(\tau). \tag{4}$$

In other terms, the decreasing i_S delays the v_{GS} commutation that, in turn, delays the i_S lowering. Such behavior is undesired because it involves higher turn-OFF switching time and losses. Similar considerations can be obtained when focusing on the i_D.

Instead, when the 4L MOSFET is considered, v_{GS} is obtained by applying the KVL to a different driving loop arising from the different topology [see Fig. 1(b)]:

$$v_{GS} = V_G - R_G i_G - (L_g + L_k) \frac{di_G}{dt}. \tag{5}$$

Equation (5) highlights that, in the case of 4L MOSFET, i_S does not affect v_{GS} regardless of the L_S value.

B. Analysis of the Experimental Results Under Variable Load

In the following, first, the waveforms of a turn-OFF (see Fig. 4) are analyzed to prove that the reasoning described in Section A is misleading. After that, more results are reported and discussed to generalize this conclusion. It is worth noticing that the following analysis does not aim at proving that the parasitic source inductance does not delay the turn-OFF in 3L MOSFET. This inductance actually slows the turn-OFF but the actual reasons are those described in Section IV. Hence, the following analysis aims only at proving that the typical argumentation described in Section III-A is misleading. Of course, understanding the correct mechanism leads to helpful information at the design stage of the converter as it will be shown in Section IV-C.

Fig. 4 reports the waveforms of the 3L MOSFET current (red), gate-source voltage (green), and drain-source voltage (blue) at the maximum load with $R_G = 3.9\ \Omega$. The sample rate is 1ns, while the time-step in the figure is 5 ns/division. The red dashed

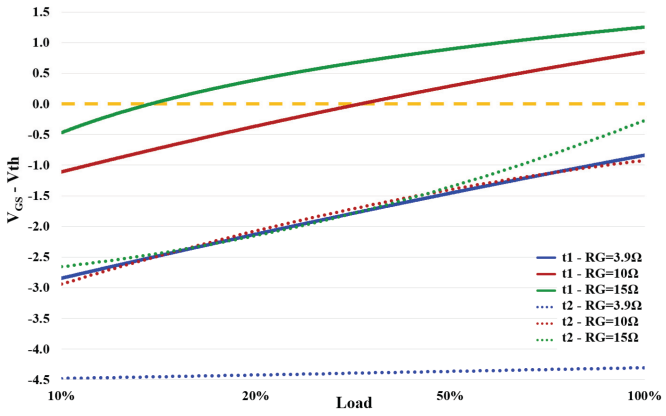

Fig. 5. Difference between the gate-source voltage and the threshold voltage for various values of gate resistance and load conditions, @t1 solid line and @t2 dotted lines. The dashed line represents the 0-axes.

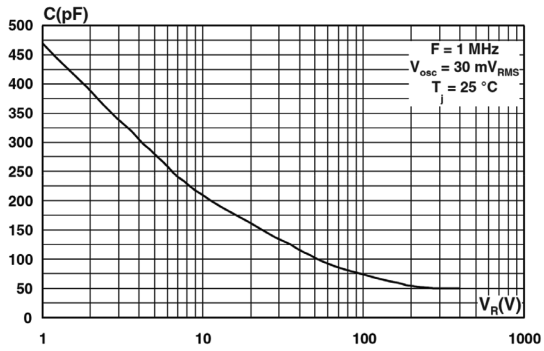

Fig. 6. Diode differential capacitance versus the reverse voltage.

line represents the zero current axis. Similarly, the green and blue dashed lines represent the zero voltage axes for, respectively, the gate-source and drain-source voltage. The gray dotted line represents the voltage threshold of the device at 53.7 °C (device temperature measured by the thermocamera).

The first vertical line indicates the instant t1, when the MOSFET current starts decreasing. Before, the current is constant (indeed it is slightly increasing) while the gate-source voltage is decreasing. Therefore, according to (1), the constant current does not delay the gate-source voltage reduction (indeed the slightly positive derivative implies that the current facilitates the reduction). At t1, the drain-source voltage is slightly higher than during the ON-time (see Fig. 4). Consequently, the MOSFET would be in the active region of the output characteristic if the gate-source voltage was greater than the threshold. On the other hand, as Fig. 4 highlights that the gate-source voltage (2.9 V) is below the threshold (3.8 V at 53.7 °C, which is the temperature measured by the thermocamera), then relation 3 does not hold. Therefore, when the current derivative is negative and, consequently, the current could actually delay the gate-source voltage reduction [according to (1)], the v_{GS} commutation does not delay the current reduction. The second vertical line indicates the instant t2, when the sudden reduction of the MOSFET current starts, i.e., the magnitude of the derivative current is very high, then according to (1) the reduction of v_{GS} should be strongly delayed. It occurs when v_{DS} is about equal to the converter input voltage, which implies that the boost inductor current i_B [see Fig. 1(a)], does not increase more. At t2, the gate-source voltage is widely below the threshold voltage, and then the previous considerations (made for t1) are still valid. In conclusion, the common reasoning about the effect of the parasitic source inductance based on assuming that the falling current delays the gate-source voltage commutation that, in turn, delays the former is misleading. This deduction can be generalized by the following analysis.

The difference between the gate-source voltage and the threshold voltage for different values of gate resistance and load conditions is shown in Fig. 5. Such an approach accounts for the reduction of the threshold voltage with increasing temperature [35]. The temperature increases when R_G and the load increase, involving higher power losses. The difference computed at the instant t2 (dotted lines) is always negative, thus, relation 3 does not hold regardless of the value of R_G and the load condition. Therefore, the v_{GS} commutation does not delay the current reduction. The difference computed at t1 (solid lines) is negative for a typical R_G value (3.9 Ω) regardless of the load condition, hence, the previous considerations are still valid. The difference is positive when R_G is high (15 Ω), especially at a high load. However, it can be demonstrated that the MOSFET current reduction, in t1-t2, is caused by the capacitive behavior of the diode instead of the MOSFET behavior in the active region. In other words, even in this case, the MOSFET current reduction is not due to relation 3. Hence, the common reasoning is misleading even in these cases.

To demonstrate the previous statement, it is sufficient to analyze just the case with the largest positive difference between the gate-source voltage and the threshold voltage ($R_G = 15$ Ω, load = 100%). In the interval t1-t2, the diode (see Fig. 1) is in the reverse region and it behaves similarly to a capacitor whose differential capacitance c_{JD}, is reported in Fig. 6 as a function of the reverse voltage v_R.

Recalling that the voltage across the diode v_{Diode} is

$$v_{\text{Diode}} = v_{DS} - V_{\text{OUT}} = -v_R. \tag{6}$$

It follows that, in the interval t1-t2, the diode current i_o (see Fig. 1) can be expressed as

$$i_o = c_{JD}\left(\frac{dv_{DS}}{dt} - \frac{dV_{\text{OUT}}}{dt}\right) = c_{JD}\frac{dv_{DS}}{dt}. \tag{7}$$

Then, in this interval, the diode current is positive since the drain-source voltage increases. Moreover, the voltage increment rate $\frac{dv_{DS}}{dt}$ is also increasing, as shown in Fig. 7, which refers to the analyzed case (such a typical behavior is shown in Fig. 4 too). Then, the diode current is increasing in the interval t1-t2. According to (6), the reverse voltage is decreasing in this interval and, consequently, according to Fig. 6, c_{JD} is increasing, thus, further supporting the increment of the capacitive current i_o flowing through the diode. This current can be estimated by using (7) and the blue curve in Fig. 7(b). Then, looking at node E in Fig. 8, an estimation of the waveform of the inductor current i_B [see violet curve in Fig. 7(b)] can be obtained by adding,

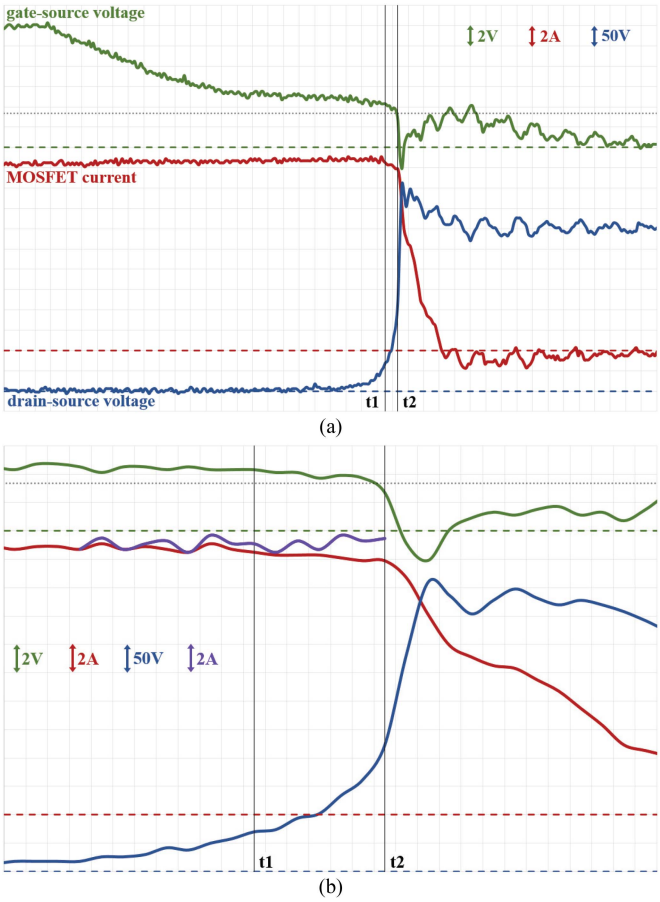

Fig. 7. Turn-off waveforms of the 3L MOSFET at full load when RG = 15: (a) overall turn-OFF (15 ns/div) and (b) zoomed view of t1–t2 interval (2 ns/div). The violet waveform is the estimated inductor current obtained by the sum of the MOSFET current and the estimated (capacitive) current of the diode.

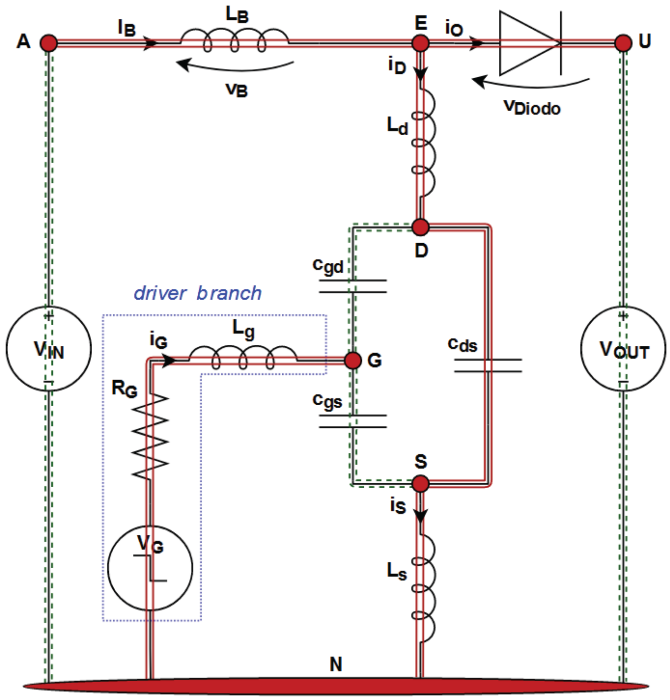

Fig. 8. Boost converter components and main parasitic elements during the OFF-state of a 3L MOSFET.

point-to-point, the estimated current i_0 to the measured MOSFET current i_D (see red line in Fig. 7), Therefore, looking again at node E in Fig. 8, this proves that the increasing capacitive current is the cause of the reduction of the current flowing through the MOSFET and, consequently, the MOSFET current reduction is not due to the v_{GS} reduction. So it confirms once more that the reasoning of Section III-A is misleading. In fact, at t_2, the gate voltage is sufficiently below the threshold to affirm that relation 3 and, consequently, relations 4 and 5 are not valid after t2, when there is a sudden decrease of the MOSFET current. Therefore, the knowledge of the current through the diode and the inductor after t2 is not important for the aim of the proof and, consequently, they have not been estimated.

Furthermore, it is worth noticing that: the MOSFET derivative current is small in the interval t1-t2 [see Fig. 7(b)]; the difference between the MOSFET gate-source voltage and the threshold is only about 1 V in this interval, which is not sufficient to obtain 18 A according to the output characteristic.

The previous discussion can be applied to the switching waveforms reported in the literature. For example, the analysis of the turn-OFF waveforms reported in [21] highlights that at t1 the gate-source voltage is equal to the threshold voltage while at t2 it is lower than the threshold voltage. Hence, the same considerations made referring to Fig. 4 are confirmed. That is, relation 3 does not hold at t1 and later when the current derivative is negative, and, consequently, the current could actually delay the gate-source voltage reduction [see according to (1)] and the v_{GS} commutation does not delay the current reduction. The analysis of the turn-OFF waveforms reported in [23] reveals, once again, that relation 3 does not hold when the current derivative is negative, then the common interpretation is misleading since the discussions about Fig. 4 are valid also in this case. The analysis of the turn-OFF waveforms reported in [28] reveals that at t2 the previous considerations as well as those related to Fig. 4 hold true, while a different behavior arises at t1. In detail, at t1, the gate-source voltage is greater than the threshold. However, comparing the gate-voltage of 3L and 4L MOSFETs in [28], it is evident that they are similar in the interval t1-t2, consequently, the negative current derivative does not have an additional undesired impact on the gate-source voltage decrement in 3L MOSFETs in this interval. Hence, this proves, again, that the common reasoning about the source parasitic inductance impact is misleading.

IV. Formulation of the Actual Reasons Enabling the Turn-Off Losses Reduction in 4L MOSFET

The actual reasons involving the reduction of the turn-OFF losses in 4L MOSFET are analytically investigated in this section. Moreover, the increment of the difference between the turn-OFF losses of 3L and 4L MOSFETs with increasing gate resistance and load conditions is also analytically obtained.

Finally, useful considerations regarding the different technologies are reported based on the obtained equations.

A. Analysis of 3L MOSFETs Turn-Off

Fig. 8 shows a schematic of a boost converter during the switch turn-OFF, when a 3L MOSFET is used. The figure is valid once the v_{GS} is below (or, according to the discussion about Fig. 7, close to) the MOSFET threshold. Some parasitic components of the switch, e.g., parasitic inductances of the bonding wires and leads, and the PCB, e.g., parasitic inductances of the copper/aluminium traces connecting the converter components, are reported.

The total parasitic inductance in the input path (from node N to A-plus from A to E) can be neglected since it is in series with the boost inductor L_B. The total parasitic inductance in the output path (from node E to U-plus from U to N, comprising, for example, the ones due to diode leads) cannot be neglected and should be reported in the circuit. On the other hand, as will be apparent in the following, this parasitic inductance does not affect the specific analysis, thus, it has been omitted.

In the figure, upper letters indicate quantities that do not vary during the analyzed interval, while lower ones indicate variable quantities. The subscripts of the symbols indicating actual components are upper letters, while lower letters are used for the subscript of parasitic components. The input and output capacitors of the converter have been modeled with constant voltage sources since their voltages can be assumed to be almost constant.

The identification of the impact of the drain current, i_D, on its derivative function is the target of the following analysis. To this aim, a reduced sparse tableau approach for circuit analysis has been adopted. In Fig. 8, are reported the nodes (A, E, U, D, G, S and N) and branches of a graph related to the circuit. Each component of the circuit represents a branch of the graph, except for the driver branch, which comprises some circuit components, which are inside the blue-dashed polygon. The twigs of a spanning tree (ST) are colored with double-red-straight lines, while the co-tree branches are colored with double-green-dashed lines.

The following equations are independent of each other since they are obtained by applying the Kirchhoff's current law to the fundamental cut sets (FC).

FC1: driver branch, c_{gs}, c_{gd}

$$i_G = c_{gs}\frac{dv_{GS}}{dt} + c_{gd}\frac{dv_{GD}}{dt}. \tag{8}$$

FC2: L_s, c_{gs}, c_{gd}, V_{IN}, V_{OUT} , and FC3: L_B, V_{IN}, and FC4: diode, V_{OUT}

$$i_S = c_{gs}\frac{dv_{GS}}{dt} + c_{gd}\frac{dv_{GD}}{dt} + I_B - i_o. \tag{9}$$

FC5: L_d, V_{IN}, V_{OUT}, and FC3 and FC4

$$i_D = I_B - i_o. \tag{10}$$

FC6: c_{ds}, c_{gd},V_{IN}, V_{OUT}, and FC3 and FC4

$$c_{ds}\frac{dv_{DS}}{dt} = c_{gd}\frac{dv_{GD}}{dt} + I_B - i_o. \tag{11}$$

Other independent equations are obtained by applying the KVL to the fundamental loops (FL).

FL1: c_{gs}, driver branch, L_s

$$v_{GS} = V_G - R_G i_G - L_g\frac{di_G}{dt} - L_s\frac{di_S}{dt}. \tag{12}$$

FL2: c_{gd}, driver branch, L_s, c_{ds}

$$v_{GD} = V_G - R_G i_G - L_g\frac{di_G}{dt} - L_s\frac{di_S}{dt} - v_{DS}. \tag{13}$$

A well-known equation is obtained by combining them

$$v_{GD} = v_{GS} - v_{DS}. \tag{14}$$

The following equation is obtained by substituting (14) in (11):

$$c_{ds}\frac{dv_{DS}}{dt} = c_{gd}\left(\frac{dv_{GS}}{dt} - \frac{dv_{DS}}{dt}\right) + I_B - i_o \tag{15}$$

which, in turn, can be rewritten as

$$\frac{dv_{GS}}{dt} = \frac{c_{ds}+c_{gd}}{c_{gd}}\frac{dv_{DS}}{dt} + \frac{1}{c_{gd}}(I_B - i_o). \tag{16}$$

The following equation is obtained by substituting (14) and (16) in (8):

$$\begin{aligned} i_G &= (c_{gs}+c_{gd})\frac{dv_{GS}}{dt} - c_{gd}\frac{dv_{DS}}{dt} = \\ &= \frac{(c_{gs}+c_{gd})(c_{ds}+c_{gd})}{c_{gd}}\frac{dv_{DS}}{dt} + \frac{(c_{gs}+c_{gd})}{c_{gd}}(I_B - i_o) \\ &\quad - c_{gd}\frac{dv_{DS}}{dt} \Rightarrow i_G = \frac{c_{gs}c_{ds} + c_{gd}(c_{gs}+c_{ds})}{c_{gd}}\frac{dv_{DS}}{dt} \\ &\quad + \frac{(c_{gs}+c_{gd})}{c_{gd}}(I_B - i_o). \end{aligned} \tag{17}$$

The following equation is obtained by subtracting (8) from (9) and then substituting (17):

$$\begin{aligned} i_S &= \frac{c_{gs}c_{ds} + c_{gd}(c_{gs}+c_{ds})}{c_{gd}}\frac{dv_{DS}}{dt} \\ &\quad + \frac{(c_{gs}+2c_{gd})}{c_{gd}}(I_B - i_o). \end{aligned} \tag{18}$$

Eventually, the unnumbered equation shown at the bottom of the next page is obtained by firstly substituting (10), (17) and (18) in (12), then by explicitly expressing the derivative of the drain current

$$\Rightarrow \frac{di_D}{dt} = \frac{\left\{\begin{array}{c} c_{gd}(V_G - v_{GS}) - R_G(c_{gs}+c_{gd})i_D + \\ -R_G[c_{gs}c_{ds} + c_{gd}(c_{gs}+c_{ds})]\frac{dv_{DS}}{dt} + \\ -(L_g+L_s)[c_{gs}c_{ds} + c_{gd}(c_{gs}+c_{ds})]\frac{d^2v_{DS}}{dt^2} \end{array}\right\}}{(L_g+L_s)(c_{gs}+c_{gd}) + L_s c_{gd}}. \tag{19}$$

This equation highlights the effect of the drain current on its derivative during the subperiod of the turn-OFF in which the current actually varies.

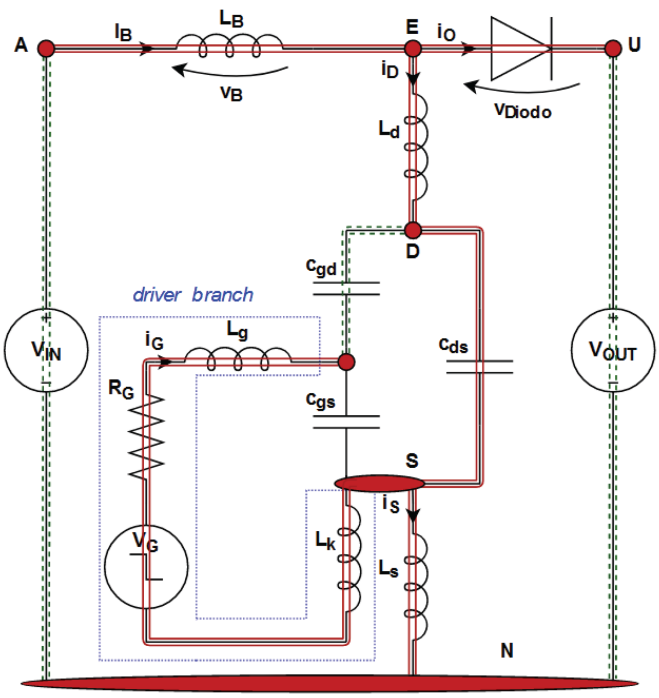

Fig. 9. Boost converter components and main parasitic elements during the OFF-state of a 4L MOSFET.

B. Analysis of 4L MOSFETs Turn-Off

A similar relation can be obtained for a 4L MOSFET. In this perspective, as Fig. 9 reveals, (8), (10), and (11) are still valid because the related FCs (1, 3, 4, 5, 6) are equal to the ones in Fig. 8. Hence, (16) and, consequently, (17) are still valid. Obviously, (14) still holds. On the other hand, FC2 and the related equation are changed as follows.

FC2-4L: L_s, V_{IN}, V_{OUT}, and FC3 and FC4

$$i_S = I_B - i_o. \tag{20}$$

The two FLs considered for the circuit with 3L MOSFET are not valid for the one with 4L MOSFET, as shown in Fig. 9.

Moreover, the driver branch also includes the parasitic Kelvin inductance, L_k. Then, the two FLs and the related equations change as follows in the case of 4L MOSFET, although they are still similar to the ones of 3L MOSFETs [(12) and (13)].

FL1-4L: c_{gs}, driver branch (now includes L_k)

$$v_{GS} = V_G - R_G i_G - (L_g + L_k)\frac{di_G}{dt}. \tag{21}$$

FL2: c_{gd}, driver branch (now includes L_k), c_{ds}

$$v_{GD} = V_G - R_G i_G - (L_g + L_k)\frac{di_G}{dt} - v_{DS}. \tag{22}$$

Equation (23) is obtained by first substituting (10) and (17) in (21), then by explicitly expressing the derivative of the drain current

C. Practical Design Consideration Emerging From the Comparison Between 3L and 4L MOSFETs Turn-Off

During the turn-OFF, the derivative of the drain current i_D is negative. In (19) (3L) and (23) (4L), the contribution of the drain current term is negative since i_D is positive. So, in both cases, an increasing drain current has an empowering effect on its derivative. Moreover, considering that the drain current is equal to the inductor current when the turn-OFF starts, and, in turn, the inductor current is proportional to the load current, i_{LOAD}, then the magnitude of the current derivative, $\frac{di_D}{dt}$, increases with increasing load.

By summarizing, considering that as follows:

1) the greater the derivative, the faster the commutation, the lower the turn-ON switching losses;
2) the coefficient of the drain current in (23) (4L) is greater than the one in (19) (3L);
3) the initial value of the drain current is equal to the boost inductor current I_B, when the turn-OFF begins;
4) the boost inductor current is proportional to i_{LOAD};

then the 4L MOSFET more and more outdoes the 3L one as the load increases.

More practical information for converters design can be obtained by evaluating the magnitude of the increment Δ of the derivative current in 4L MOSFET due to the current itself. By setting

$$L_s \triangleq (1+\alpha)\,L_k. \tag{24}$$

and considering (19) and (23) shown at the bottom of the next page, it follows:

$$\Delta = \left\{ \frac{\frac{1}{(L_g+L_k)(c_{gs}+c_{gd})} + \frac{-1}{(L_g+L_k)(c_{gs}+c_{gd})+\alpha L_k(c_{gs}+2c_{gd})+L_k c_{gd}}}{} \right\} \cdot R_G\,(c_{gs}+c_{gd})\,i_D \tag{25}$$

which can be rewritten as follows (26) shown at the bottom of the next page:

Recalling that $c_{gs} \gg c_{gd}$, the following relation is obtained:

$$\Delta \approx \frac{L_k\,[\alpha c_{gs} + c_{gd}]}{(L_g+L_k)\,c_{gs}\,[L_g+L_k+\alpha L_k]} R_G i_D. \tag{27}$$

$$v_{GS} = V_G - \frac{\left\{ \begin{array}{c} R_G\left[(c_{gs}c_{ds}+c_{gd}(c_{gs}+c_{ds}))\frac{dv_{DS}}{dt} + (c_{gs}+c_{gd})\,i_D\right] + \\ -L_g\left[(c_{gs}c_{ds}+c_{gd}(c_{gs}+c_{ds}))\frac{d^2v_{DS}}{dt^2} + (c_{gs}+c_{gd})\frac{di_D}{dt}\right] + \\ -L_s\left[(c_{gs}c_{ds}+c_{gd}(c_{gs}+c_{ds}))\frac{d^2v_{DS}}{dt^2} + (c_{gs}+2c_{gd})\frac{di_D}{dt}\right] \end{array} \right\}}{c_{gd}}$$

Interesting considerations arise from analyzing (27) in two extreme cases. More specifically, when $L_k \approx L_s \Rightarrow \alpha \approx 0$, it becomes

$$\begin{cases} \Delta \approx \frac{c_{gd}}{4L_k c_{gs}} R_G i_D \text{ when } L_g \approx L_k \\ \Delta \approx \frac{c_{gd}}{L_k c_{gs}} R_G i_D \text{ when } L_g \ll L_k \end{cases} \tag{28}$$

otherwise, when $L_k \ll L_s \Rightarrow \alpha \gg 1$, (27) becomes

$$\begin{cases} \Delta \approx \frac{1}{2L_k} R_G i_D \text{ when } L_g \approx L_k \\ \Delta \approx \frac{1}{L_k} R_G i_D \text{ when } L_g \ll L_k \end{cases} \tag{29}$$

When the device is turned-OFF, the initial value of the drain current is equal to the boost inductor current, which, in turn, is proportional to the load current. Therefore, (25), and its approximated relations (28) and (29), show that the improvement obtained using a 4L MOSFET (that is the difference between the power losses of 3L and 4L MOSFET) increases as the gate resistance increases as well as with increasing the load. This result is compliant with the experimental results in Fig. 3 and the literature, as discussed in Section II.

The analysis performed so far has only considered the MOSFET parasitic inductances. However, the main effect of the other parasitic inductances, e.g., those due to the PCB, can be translated in an increment of inductances L_k and L_s, thus extending the validity of this article and the usability of the obtained equations for providing practical information to the layout designer. In this perspective, the approximated (28) and (29) reveal that the improvement, i.e., Δ, obtained using 4L MOSFETs reduces as the Kelvin parasitic inductance increases. Moreover, in 28 and 29, when $L_g \approx L_k$, the effect of the gate parasitic inductance on Δ cannot be neglected since this inductance is in series with the Kelvin one. In other words, in this case, it empowers the effect of the Kelvin inductance. Therefore, it presents the same effect related to the other parasitic components, e.g., the PCB parasitic inductances. According to this, the previous statement can be generalized: *the improvement obtained using 4L MOSFETs reduces as the parasitic inductance of the driving loop increases*.

Therefore, defining L_{dri} as the parasitic inductance of the driving loop, which is obtained by summing the aforementioned contributions, (27) can be approximately rewritten as

$$\Delta \approx \frac{L_{dri}\left[\alpha c_{gs} + c_{gd}\right]}{L_{dri} c_{gs} L_{dri}\left[1+\alpha\right]} R_G i_D = \frac{\left[\alpha c_{gs} + c_{gd}\right]}{c_{gs} L_{dri}\left[1+\alpha\right]} R_G i_D. \tag{30}$$

This result is useful for the designer since it is suitable to define the following figure of merit:

$$\delta(\alpha) \triangleq \frac{\alpha + \frac{c_{gd}}{c_{gs}}}{\alpha + 1} \frac{1}{L_{dri}} R_G i_D. \tag{31}$$

As said, in (31) the overall (device plus PCB and so on) source and Kelvin parasitic inductances are considered. Therefore, the following remarks based on the discussion of (31) are useful at the design stage.

Eq. (31) highlights that, for a given $R_G \cdot i_D$, the improvement depends on the MOSFET technology (that is, the ratio between the Miller and the gate-source capacitances) when $\alpha \to 0$. This condition, according to (24), occurs when the source inductance is equal to the Kelvin one. Generalizing, accounting for the overall parasitic inductances, the condition $\alpha \to 0$ occurs when the power loop inductance is equal to the one of the driver loop. The Kelvin parasitic inductance is usually small, thus obtaining this condition in a practical application means that the PCB layout should be strongly optimized to reduce the parasitic source inductance. However, it is challenging to obtain a power loop parasitic inductance equal to the driver loop one. Nevertheless, if the designer focuses on the reduction of the power loop inductance only and pays no attention to the driver loop, the $\alpha \to 0$ condition could occur, thus jeopardizing the advantages of the 4L MOSFET.

On the other hand, the impact of the MOSFET technology is negligible when the PCB layout involves power loop parasitic inductance significantly larger than the driver loop one ($\alpha \gg 1$), which is the most common case. Therefore, (31) provides information about the effectiveness of different layout solutions in terms of improvement achievable using a 4L MOSFET. The greater $\delta(\alpha)$ the better the improvement a 4L MOSFET provides. Finally, (31) also highlights that the improvement decreases with increasing driver loop parasitic inductance. Therefore, the designer of the PCB layout must pay more attention to this inductance than those of the power loop and, similarly, the 4L

$$v_{GS} = V_G - \frac{\left\{\begin{array}{c} R_G\left[\left(c_{gs}c_{ds} + c_{gd}\left(c_{gs}+c_{ds}\right)\right)\frac{dv_{DS}}{dt} + \left(c_{gs}+c_{gd}\right) i_D\right] + \\ -\left(L_g+L_k\right)\left[\left(c_{gs}c_{ds} + c_{gd}\left(c_{gs}+c_{ds}\right)\right)\frac{d^2v_{DS}}{dt^2} + \left(c_{gs}+c_{gd}\right)\frac{di_D}{dt}\right] \end{array}\right\}}{c_{gd}} \Rightarrow \frac{di_D}{dt}$$
$$= \frac{\left\{\begin{array}{c} c_{gd}\left(V_G - v_{GS}\right) - R_G\left(c_{gs}+c_{gd}\right) i_D + \\ -R_G\left[c_{gs}c_{ds} + c_{gd}\left(c_{gs}+c_{ds}\right)\right]\frac{dv_{DS}}{dt} + \\ -\left(L_g+L_k\right)\left[c_{gs}c_{ds} + c_{gd}\left(c_{gs}+c_{ds}\right)\right]\frac{d^2v_{DS}}{dt^2} \end{array}\right\}}{\left(L_g+L_k\right)\left(c_{gs}+c_{gd}\right)}. \tag{23}$$

$$\Delta = \frac{L_k\left[\alpha\left(c_{gs}+2c_{gd}\right)+c_{gd}\right]}{\left(L_g+L_k\right)\left[\left(L_g+L_k\right)\left(c_{gs}+c_{gd}\right)+\alpha L_k\left(c_{gs}+2c_{gd}\right)+L_k c_{gd}\right]} R_G i_D. \tag{26}$$

MOSFETs manufacturers must take more care of the kelvin and gate parasitic inductances than the source one. However, this concern must be even more considered at the PCB design stage since the additional parasitic contribution in the driving loop could be more significant than the one due to the package.

V. Conclusion

As well known, the adoption of an additional source terminal, the Kelvin pin, improves the switching performance of both Silicon- and WBG-based devices, especially at large loads. This article has first proved that the common reasoning about the causes of this improvement during the turn-OFF is misleading. After that, the correct reasons have been evinced by means of analytical circuit analysis. Information useful at the design stage of the converter has been highlighted by using the results of this analysis. The ratio between the Miller and the gate-source capacitances influences the improvement when the PCB design strongly reduces the parasitic source inductance or, more precisely, when similar parasitic inductance in both the driver and power loops are obtained ($\alpha \to 0$). In fact, in this case, the decoupling of the driver and power loop is not sufficient to fully benefit from the additional source terminal. Moreover, another important aspect that emerged from the study is that the improvement using 4L MOSFET could become ineffective in the presence of large parasitic inductance in the driving loop. Therefore, the layout designer has to reduce this contribution. However, it is worth noticing that these considerations account for the turn-OFF only. A proper design must also consider the behavior during the turn-ON [24].

Finally, this article lays the foundation for an in-depth understanding of the advantages of the Kelvin pin as well as the aspects that can hinder them in various applications. Starting from this point, the research could focus on extending this article to wide-bandgap devices as well as to applications where the devices are placed in parallel or in power modules adopting multi-die switches. Moreover, interesting future work is the identification of the equations describing the device voltage waveforms during the switching, and to esteem the turn-OFF switching losses by combining them with the equations obtained for the current.

References

[1] H. Chen, K. Sabi, H. Kim, T. Harada, R. Erickson, and D. Maksimovic, "A 98.7% efficient composite converter architecture with application-tailored efficiency characteristic," *IEEE Trans. Power Electron.*, vol. 31, no. 1, pp. 101–110, Jan. 2016.

[2] W.-Y. Choi and J.-S. Lai, "High-efficiency grid-connected photovoltaic module integrated converter system with high-speed communication interfaces for small-scale distribution power generation," *Sol. Energy*, vol. 84, no. 4, pp. 636–649, 2010.

[3] A. K. Mishra and B. Singh, "High gain single ended primary inductor converter with ripple free input current for solar powered water pumping system utilizing cost-effective maximum power point tracking technique," *IEEE Trans. Ind. Appl.*, vol. 55, no. 6, pp. 6332–6343, Nov./Dec. 2019.

[4] G. Z. Abdelmessih, J. M. Alonso, M. A. Dalla Costa, Y.-J. Chen, and W.-T. Tsai, "Fully integrated buck and boost converter as a high efficiency, high-power-density off-line LED driver," *IEEE Trans. Power Electron.*, vol. 35, no. 11, pp. 12238–12251, Nov. 2020.

[5] B. Whitaker et al., "A high-density, high-efficiency, isolated on-board vehicle battery charger utilizing silicon carbide power devices," *IEEE Trans. Power Electron.*, vol. 29, no. 5, pp. 2606–2617, May 2014.

[6] M. H. Ahmed, M. A. de Rooij, and J. Wang, "High-power density, 900-W LLC converters for servers using GaN FETs: Toward greater efficiency and power density in 48V to 6/12V converters," *IEEE Power Electron. Mag.*, vol. 6, no. 1, pp. 40–47, Mar. 2019.

[7] D. Koch, J. Weimer, M. Weiser, J. Hueckelheim, and I. Kallfass, "Gate driver concept for parallel operation of low-voltage high-current GaN power transistors for mild-hybrid applications," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2021, pp. 1755–1760.

[8] Y. Wang, D. Zhao, X. Ma, B. Chen, and C. Chen, "Accurate model and switching characteristics of SIC MOSFET power modules with Kelvin source package," in *Proc. IEEE 11th Int. Conf. Power Electron., Mach. Drives*, 2022, pp. 680–684.

[9] V. Crisafulli, "A new package with Kelvin source connection for increasing power density in power electronics design," in *Proc. IEEE 17th Eur. Conf. Power Electron. Appl.*, 2015, pp. 1–8.

[10] F. Merienne, J. Roudet, and J. L. Schanen, "Switching disturbance due to source inductance for a power MOSFET: Analysis and solutions," in *Proc. IEEE 27th Annu. Power Electron. Specialists Conf.*, 1996, vol. 2, pp. 1743–1747.

[11] B. Wittig, O. Muehlfeld, and F. W. Fuchs, "Adaption of MOSFETs current slope by systematic adjustment of common source stray inductance and gate resistance," in *Proc. IEEE 14th Eur. Conf. Power Electron. Appl.*, 2011, pp. 1–10.

[12] M. Ebli and M. Pfost, "A gate driver approach using inductive feedback to decrease the turn-on losses of power transistors," in *Proc. IEEE Int. Exhib. Conf. Power Electron., Intell. Motion, Renewable Energy Energy Manage.*, 2018, pp. 1–6.

[13] Y. Xiao, H. Shah, T. P. Chow, and R. J. Gutmann, "Analytical modeling and experimental evaluation of interconnect parasitic inductance on MOSFET switching characteristics," in *Proc. IEEE 19th Annu. Appl. Power Electron. Conf. Expo.*, 2004, vol. 1, pp. 516–521.

[14] Z. Chen, D. Boroyevich, and R. Burgos, "Experimental parametric study of the parasitic inductance influence on MOSFET switching characteristics," in *Proc. Int. Power Electron. Conf. - ECCE Asia*, 2010, pp. 164–169.

[15] K. K.-M. Siu, M. K.-H. Cheung, and F. P. Stückler, "Performance analysis of package parasitic inductances for fast switching MOSFET in converter," in *Proc. IEEE Int. Power Electron. Appl. Conf. Expo.*, 2014, pp. 314–319.

[16] Y. Sugihara, K. Nanamori, M. Yamamoto, and Y. Kanazawa, "Parasitic inductance design considerations to suppress gate voltage oscillation of fast switching power semiconductor devices," in *Proc. IEEE Int. Power Electron. Conf.*, 2018, pp. 2789–2795.

[17] M. Cacciato et al., "High frequency operation of superjunction MOSFET enhanced with Kelvin source pin," in *Proc. AEIT Int. Conf. Elect. Electron. Technol. Automot.*, 2020, pp. 1–6.

[18] J. Smutka, V. Scarpa, J. Svetlik, and J. Hajek, "Improvement of dynamic characteristics of discrete 1200V SiC MOSFETs through Kelvin source connection," in *Proc. IEEE Int. Exhib. Conf. Power Electron., Intell. Motion, Renewable Energy Energy Manage.*, 2020.

[19] F. Yang, Z. Wang, Z. Liang, and F. Wang, "Electrical performance advancement in SiC power module package design with Kelvin drain connection and low parasitic inductance," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 7, no. 1, pp. 84–98, Mar. 2019.

[20] C. G. Stella, M. Laudani, A. Gaito, and M. Nania, "Advantage of the use of an added driver source lead in discrete power MOSFETs," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2014, pp. 2574–2581.

[21] R. Jagannathan, H. Hoenes, and T. Duggal, "Impacts of package, layout and freewheeling diode on switching characteristics of super junction MOSFET in automotive DC-DC applications," in *Proc. IEEE Int. Conf. Power Electron., Drives Energy Syst.*, 2016.

[22] Z. Zhang, J. Fu, Y.-F. Liu, and P. C. Sen, "Switching loss analysis considering parasitic loop inductance with current source drivers for buck converters," *IEEE Trans. Power Electron.*, vol. 26, no. 7, pp. 1815–1819, Jul. 2011.

[23] Z. Wang, J. Zhang, X. Wu, and K. Sheng, "Analysis of stray inductance's influence on SiC MOSFET switching performance," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2014, pp. 2838–2843.

[24] F. Giorgio, S. A. Rizzo, N. Salerno, G. Scarcella, A. Scuto, and G. Sorrentino, "Understanding the Kelvin pin mitigation of the MOSFET turn-on losses by fast-switching and neutralization of the clamp diode," in *Proc. IEEE 47th Annu. Conf. Ind. Electron. Soc.*, 2021, pp. 1–6.

[25] A. Gaito, R. Scollo, G. Panebianco, and A. Raciti, "Impact of the source-path parasitic inductance on the MOSFET commutations," in *Proc. Appl. Power Electron. Conf.*, 2012, pp. 1367–1373.

[26] B. Zojer, "A new gate drive technique for superjunction MOSFETs to compensate the effects of common source inductance," in *Proc. IEEE Appl. Power Electron. Conf.*, 2018, pp. 2763–2768.

[27] Y. Hu, J. Shao, T. S. Ong, J. Rice, and J. Solovey, "Comparative study of packaging effects of SiC MOSFETs on their performances in a 10 kW boost converter," in *Proc. IEEE Int. Exhib. Conf. Power Electron., Intell. Motion, Renewable Energy Energy Manage.*, 2020, pp. 1–5.
[28] F. Yang, S. Pu, B. Akin, S. W. Butler, and G. Wang, "Package degradation's impact on SiC MOSFETs loss: A comparison of Kelvin and non-Kelvin designs," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2021, pp. 2258–2264.
[29] H. Zhao, J. Chen, Y. Li, and F. Lin, "A novel gate drive circuit for suppressing turn-on oscillation of non-Kelvin packaged SiC MOSFET," *Energies*, vol. 14, no. 9, 2021, Art. no. 2449.
[30] M. Cacciato et al., "Analysis of the different impact of the external gate resistance in 3-lead and 4-lead superjunction MOSFETs," in *Proc. AEIT Int. Annu. Conf.*, 2021, pp. 1–6.
[31] Y. Li, Y. Zhang, Y. Gao, S. Du, and J. Liu, "Switching characteristic analysis and application assessment of SiC MOSFET with common source inductance and Kelvin source connection," *IEEE Trans. Power Electron.*, vol. 37, no. 7, pp. 7941–7951, Jul. 2022.
[32] Infineon application note. "CoolMOS C7 650V switch in a Kelvin source configuration," Accessed: Apr. 1, 2023. [Online]. Available: https://www.infineon.com/dgdl/Infineon+-+Application+Note+-+TO-247-4pin+-+650V+CoolMOS+C7+Switch+in+a+Kelvin+Source+Configuration.pdf?fileId=db3a30433e5a5024013e6a9908a26410
[33] STMicroelectronics application note. "Advantage of the use of an added driver source lead in discrete power MOSFETs," Accessed: Apr. 1, 2023. [Online]. Available: https://www.st.com/resource/en/application_note/an4407-advantage-of-the-use-of-an-added-driver-source-lead-in-discrete-power-mosfets-stmicroelectronics.pdf
[34] N-channel 650 V, 0.037 Ohm typ., 58 A MDmesh M5 Power MOSFET in a TO247-4 package, Accessed: Apr. 1, 2023. [Online]. Available: https://www.st.com/en/power-transistors/stw69n65m5-4.html
[35] Y. Tsividis, *Operation and Modeling of the MOS Transistor*. New York, NY, USA: McGraw-Hill, 1987.

Santi Agatino Rizzo (Member, IEEE) received the master's degree (with hons.) in electronic engineering and the Ph.D. degree in electrical engineering from the University of Catania, Catania, Italy, in 2006 and 2010, respectively.

He is currently an Assistant Professor in Electrotechnics with the University of Catania. His research interests include the circuit analysis and modeling applied to power electronics and power systems, numerical methods for electromagnetic fields computation, and application of stochastic optimization and machine learning techniques in the field of electrical and electronic engineering. He is a Member of IES.

Nunzio Salerno (Senior Member, IEEE) was born in Catania, Italy, in 1966. He received the M.Sc. degree in electronic engineering and the Ph.D. degree in electrical engineering from the University of Catania, Catania, Italy, in 1992 and 1997, respectively.

He is currently an Associate Professor of Electrical Engineering with the University of Catania. He authored more than 100 papers. His research interests include the FEM analysis and optimization of electromagnetic devices.

Open Access provided by 'Università degli Studi di Catania' within the CRUI CARE Agreement