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Ph.D. Thesis

Fully Integrated Data and Power Transfer Systems with Galvanic Isolation

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Summary

This thesis sums up main activities which I have been carried out at the *Radio-Frequency Advanced Design Center* (RF-ADC), a joint research center between STMicroelectronics and the University of Catania, during my three years of Ph.D. studies.

My principal activity was focused on the design of galvanically isolated integrated systems as a part of a research project at the RF-ADC by exploiting STMicroelectronics technology platforms providing on-chip galvanic isolation. This technology was previously addressed to the implementation of isolated data transfer and it is currently used for mass production. In this context, the principal purpose of my work was the investigation on a fully integrated dc-dc power converter with half-duplex data communications providing on-chip galvanic isolation in silicon technologies. This research is mainly interested in increasing the level of integration for the next generation of power converters with data transfer and several other applications requiring galvanic isolation. Autonomous sensors and/or control circuits, typically require a few tens of Mbps for data communication and an output power from tens to hundreds of mW. In this context, fully integrated interfaces can provide several advantages, including higher reliability, lower PCB area, lower system complexity and lower costs, especially if only silicon technology is exploited. The state of the art of isolators concerning data transfer and power devices are presented in Chap. 1.

Integrated dc-dc power converter with on-chip galvanic isolation involves several challenges due to both inherent technology limitations and the highly non-linear interactions between building blocks. It requires customized design

strategies to properly adopt the integrated approach. Therefore, this thesis focuses on fully integrated systems, with the aim of filling this gap by implementing both data and power transfer in silicon technology. This is a complex task that requires accurate evaluation of on-chip and off-chip parasitics, modelling of integrated passive devices, and customized active and passive circuit co-design. In particular, my principal design activities was focused on both dc-dc isolated power converters at different output power levels and data/power transfer systems for autonomous sensors. They are the object of Chapter 2, Appendix A and Chapter 3, respectively. These systems have been integrated in the aforementioned technology and successfully characterized. To the best of the author's knowledge, this is also the first reported system of this kind which do not require post-processing steps, therefore demonstrating the feasibility of power with/without data transfer on silicon technologies and thus promising new and highly-integrated devices to become available.

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Chapter I

Introduction

This chapter introduces the object of this dissertation that is a fully integrated half-duplex data and power transfer system with on-chip galvanic isolation. Starting from the state of the art of low-power isolated applications, the aim, the technology platform and the main outcome of this work will be discussed.

1.1 Low-power isolated interfaces

Galvanic isolation is becoming a crucial requisite in the growing field of applications involving measurements and digital control in order to guarantee safety and reliability for both data communication and power supply, especially in harsh operative environments. Indeed, the isolation protects sensitive circuit components and human interface on the control side from dangerous voltage levels present on the sense side, where more robust components such as sensors and actuators reside. Moreover, thanks to the galvanic isolation common-noises or ground loops that affect data acquisition accuracy can be eliminated. To this end, channel isolators with integrated dc-to-dc power converters are typically adopted within on board discrete or system-in-package implementations. Recently significant efforts have been done to improve the level of integration of such isolated systems, thus lowering costs and reducing package and application board sizes. We will briefly present the need for these low-power isolated interfaces in autonomous sensors, and more generally the safety reasons which make isolation mandatory by many system-level standards. Lastly, the state of the art of low-power isolated interfaces will be discussed, along with the relative component-level regulations.

1.2 Applications

Wireline Networks

Although RF communication is very popular for consumer applications, when it comes to safety-critical applications wireline networks are the solution of choice. Wireline networks based on TIA-485 standard, commonly known as RS-485, are the most used for transmitting data over long distances in noisy environments with communication distances up to 1.2 km and data-rates up to 10 Mbps [1], [2]. However, the most widespread application of wireline networks are maybe found in the automotive environment: modern high-end vehicles can house up to 120 electronic controller units, indeed, which need to share sensor data or drive actuators. The complexity of in-vehicle communication networks led car manufacturers to define several communication standards, e.g. Local Interconnect Networks, Controller Area Networks (CAN) and Flexray, with the CAN bus as the most successful one, actually gaining popularity even in automation and remote control applications [3],[4]. Both in a large industrial plant or in the small environment of a car, wireline networks are often subject to very high disturbances like electro-magnetic interferences (EMI), voltage surges and ground shifts. A common issue of these networks is avoiding ground loops, as described in Fig. 1.1. Wireline communication requires a low-impedance ground connection between network nodes, which forms a ground loop with the local ground reference of each transceiver. It is unlikely that systems with very far ground references maintain the same potential, and therefore ground potential differences (GDPs) are commonly found in wireline installations. Due to the low-impedance path offered by the ground conductor, even small GPDs can produce high current flowing in the ground loops, which corrupts the signal integrity and can be harmful for both sensitive circuitry and human operators. By providing isolation at the transceiver interface all the systems connected to the bus can be referenced to a single ground, therefore preventing any ground loops. Moreover, any electromagnetic (EM) noise coupled to the cable can cause both GPDs and instantaneous voltage surges in the range of hundreds or even

thousands of volts. Typical surges are due to high-current switching loads (e.g. electric motors), or unpredictable events such as electrostatic (ESD) discharges and lightning strikes. These surges can irreparably damage grounded transceiver interfaces, whereas isolation allows the transceiver ground to follow the surge and hence improves the robustness of the network [5]. Low power wireline transceivers for CAN bus and TIA-485 networks operate at 5-V with current consumption around 70 mA in normal operating conditions [6], [7]. Therefore, an isolated power supply providing around 300 mW output power at 5-V is highly desirable to simplify wireline network's design.

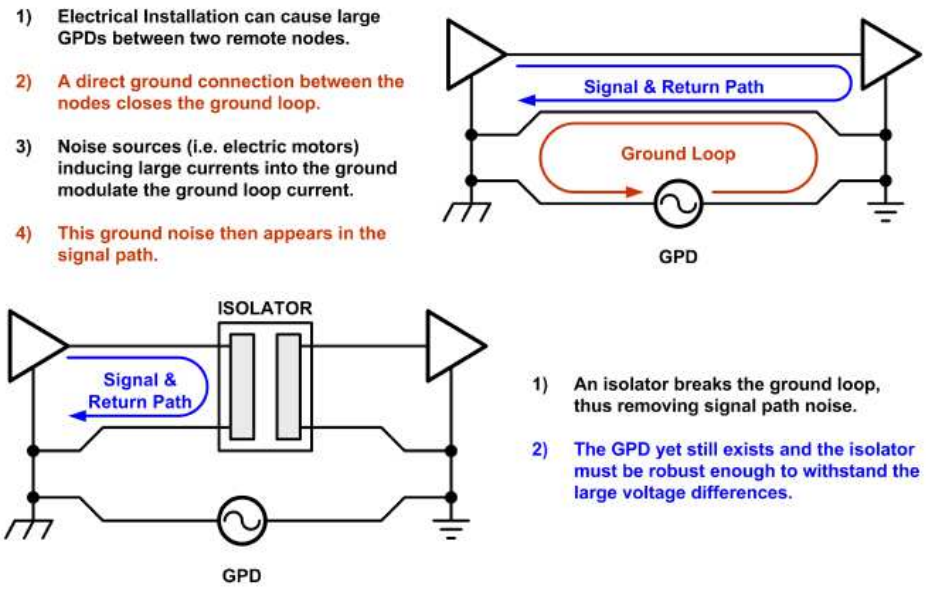

Figure 1.1 Ground loops problem in wireline communication systems [72]

Current-monitoring

Recently, applications such as power line monitoring, system protection etc., are required to meet various stringent insulation and safety standards. For example, domestic power line meters measure currents up to 100 A in AC line voltages of 100 V_{RMS} ~ 240 V_{RMS}. Usually, the current is measured at the output of an isolated sensor such as a current transformer (CT) or a Rogowski coil, or directly across a non-isolated sensor such as a shunt resistor. In the latter case the measurement rides on top of the high voltages and the required isolation is typically gained by using optocouplers connected to the digital outputs. Generally, these systems guarantee a galvanic isolation rating up to 6 kV while providing a CMTI up to 50 $kV/\mu s$. However, they often use an external isolating devices (CT, Rogowski coil, optcouplers), then a fully integrated system able to transfer both bidirectional data and power with on-chip galvanic isolation represent an ambitious solution showing several advantages in term of costs and complexity. By taking the advantage of this solution the inputs of an ADC can sense the current and transfer the corresponding digital word across the isolation barrier to the low-voltage side while the ADC receiving the isolated power.

Safety reason and system regulations

There are a variety of reasons for requiring galvanic isolation in electrical systems. The most obvious and most critical is the protection of human operators from potentially lethal shocks or the application where a sensor may accidentally encounter high voltage, and the system it is driving must be protect. Shocks hazards can come from the mains power that the equipment is plugged into, or from high voltages generate within an enclosure. The protection of an isolation barrier works in both directions, and may be needed in either, or even in both. For example, when a patients is monitored, the protection in both directions is required: the patient must be protected from accidental electric shock, but if the patient's heart should stop, the ECG machine must be protected from the very high voltages (>7.5 kV) applied to the patient by the defibrillator which will be used to

attempt to restart it. As shown in Table 1.1, electrocution due to ventricular fibrillation can be triggered even by relatively low current values. Other mishaps that can represent serious life threats and are directly related to electrical shocks are burns, either directly from sparks or indirectly from increased fire risks, and the involuntary muscle reaction as a consequence of the electric shock.

Table 1.1 Thresholds and limits for continuous 60 Hz current and their effects [8]

Physiological effect	Reaction	Threshold for continuous 15- to 100-Hz current (mA)	Limit used by UL for continuous 60-Hz sinusoidal current (mA)
Involuntary muscular reaction	Perception level, tingling sensation	0.5	0.51
Inability to let go (tetanized muscle)	Painful shock, freezing current, "can't let go"	10	5.0
Ventricular fibrillation	Heart rhythm affected, death may occur	35	20

Notes:
1. Ordinarily, a limit of 0.75 mA applies to stationary or fixed, cord-connected products with equipment-grounding conductors.
2. Data in column 3 is described in IEC Publication 479.
3. Table adapted from **Reference 1**.

Consequently, several safety standard regarding commercial products have been developed to guarantee suitable end-user protection through isolation. They limit voltage and currents which may be in contact with human operators, either in static or transient conditions, and define system specifications, patterns of test-cases, and physical restrictions to be passed by end-products, depending on the applications and for realistic operating conditions. Some examples of commonly used regional and international standards are reported in Table 1.2. Regional regulations are defined by national bodies, such as Verband Deutscher Elektringenieure (VDE), Underwriters Laboratories (UL), and Canadian Standards Association (CSA), for Germany, United States, and Canada, respectively. These agencies also provide system-level testing and certification of products. Their regulations often follow the guidelines of international agencies such as the International Electro technical Commission (IEC) and the European Norms (EN), although there can be substantial differences between each regional version [9].

Table 1.2 System-level standards involving isolation by market and region [9]

	Household	Industrial	Information Technology	Measurement and Control	Medical	Telecom
International	IEC 60065	IEC 60204	IEC 60950	IEC 61010-1	IEC 60601	IEC 60950
Germany	VDE 860		EN 60950	VDE 410/0411	VDE 0750	VDE 0804
USA	UL 60065	UL 508, UL 60947	UL 60950	UL 61010	UL 60601	UL 60950
Canada		CSA. 14-10	CSA 60950	CSA 61010	CSA 601	CSA 60950

The main concept behind these regulations is that three levels of protection are commonly defined, that are *basic*, *double*, and *reinforced* insulation [10]. Basic insulation is ascribed to a system which provides isolation while protecting the end user from potentially lethal shocks, as long as the isolation barrier is intact. Double insulation is often mandatory for end-user products. It requires a second insulation system to guarantee basic protection even if the first insulation system fails, thus providing redundant protection. The simple way to obtain double insulation is by cascading two basic-insulation systems, thus increasing costs and complexity and limiting the performance of the system. As a result, reinforced insulation has been introduced, and it is the most used isolation level, being defined as a single insulation system which guarantees electrical-shock protection equivalent to double insulation. For a given application, system designers must choose the insulation characteristics of each component to meet system-level standards.

1.3 State-of-the-art of isolators

Optocouplers and discrete transformers have traditionally been used to guarantee isolation for data transfer and their low-power supplies. Recently, research efforts have been addressed towards the development of reliable and low-cost integrated implementation able to replace these traditional approaches. Typically, data transfer with galvanic isolation have been achieved by using RF links [11], capacitive coupling [12] or integrated coreless transformers [13], [14]. These devices are commonly referred to as “digital isolators” or simply “isolators”. As far as power transfer is concerned, discrete transformers are still the solution of choice even for the aforementioned

low-power applications (<<1W). However, data and power currently exploit different channels to be transferred through an isolation barrier, thus increasing size area and costs.

Optocouplers

Optocouplers exploit the light to transfer electrical signals, normally in the near-infrared region. The typical internal structure of an optocoupler is described in Fig. 1.2(a), while an x-ray scan of a device is shown in Fig. 1.2 (b). Two separate metal frames include a light source and a photodetector, respectively. A GaAs light emitting diode (LED) and a phototransistor are commonly used to generate and detect the light. The dice are coated with the molding compound which provides isolation from external light, galvanic isolation, and the mechanical substrate for the metal frames. The spacing between the two dice depends on the isolation rating of the device, being typically greater than 400-μm for high-end products. The highest isolation and speed performance is achieved including more than one dielectric material within the package, for example silicon lens can be used to increase isolation and sensitivity of the photodetector [15], but they also increase costs and complexity of the package.

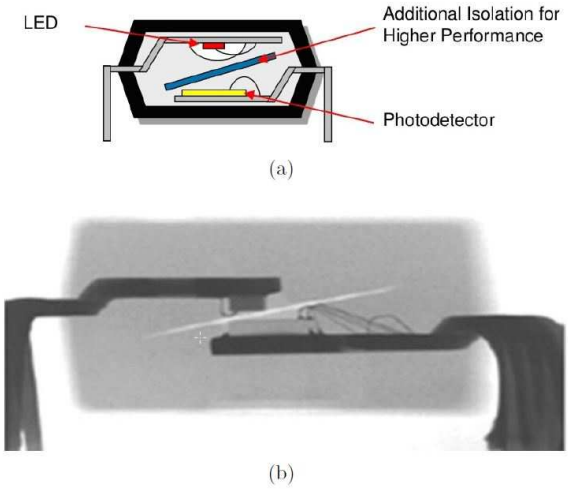

Figure 1.2 (a) Typical optocoupler structure. (b) X-ray cross section of a device

Optocouplers have been historically used to implement both analog and digital data-transfer links since they exhibit several cost and size advantages over the only alternative available in the past, i.e. bulky discrete pulse-transformer. However, they are rarely used because they are slow, power hungry, difficult to integrate with other function, and due to intrinsic time variability of their performance. Fig. 1.3 shows the common equivalent circuit of an optocoupler.

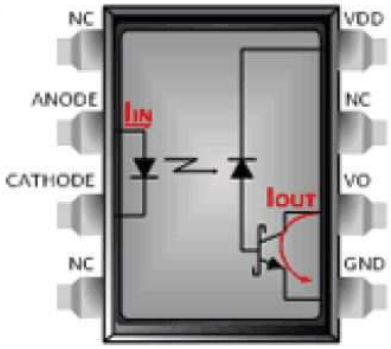

Figure 1.3 Optocoupler equivalent circuit [16]

It is characterised by the current transfer ratio (CTR) that is the ratio of the output current of the phototransistor I_{OUT} versus the input current of the LED I_{IN}. Biasing currents define the bandwidth of the link and hence are proportional to the data rate. State-of-the-art high-speed optocouplers draw more than 30 mA for a 40-Mbps link. Being related to the phototransistor current gain β, the CTR depends on both biasing currents and temperature and changes widely between each sample. These dependencies are accentuated by the great temperature sensitivity of GaAs and the impact of aging on the LED brightness. This last aspect is particularly important since the LED aging is accelerated with higher current levels, therefore a trade-off exists between performance and lifetime of the device [16].

Capacitive isolators

Capacitive isolators rely upon high-voltage capacitors able to sustain the required voltage while providing galvanic isolation. Although advanced or exotic technologies have been proposed [17], [18], the most diffused and integrated approach adopt the inter-metal dielectric (IMD) commonly used in silicon manufacturing technology, that is silicon di-oxide (SiO_2), to achieve isolation. Fig. 1.4 shows a typical single-channel capacitive isolator system. Internally isolator consist of two chips: a transmitter and a receiver. The actual isolation barrier is provided through the high-voltage capacitors located on the receiver chip. The right diagram in Fig. 1.4 shows the cross section of a high-voltage capacitor. Bond wires leaving the transmitter chip attach to the aluminium top plate of the capacitor on the receiver side. The bottom plate, also aluminium, connects to the receiver logic. Between the plates is the interleaved dielectric, a 16-μm thick level of silicon dioxide (SiO_2). The transmitter adopts radio-frequency (RF) amplitude modulation, usually on-off keying (OOK), to transfer the data across the insulation barrier. The receiver performs filtering of the input signal to reject interferers and common-mode disturbances, and amplitude demodulation to recover base-band data. By working at very high frequency (VHF), this approach enables low values for the isolation capacitors and simplifies the filtering.

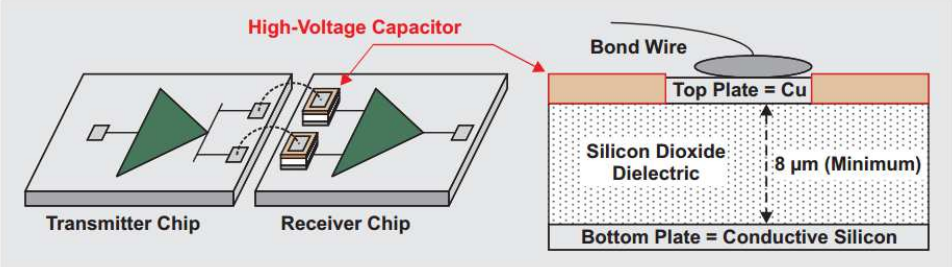

Figure 1.4 Typical capacitive isolator system

The benefits of using SiO_2 as inter-level dielectric are twofold. First, it is one of the most robust isolation materials with the least aging effects and,

therefore, extends the life time expectancy of capacitive isolators well beyond those of competing technologies. Second, SiO_2 can be processed using standard semiconductor manufacturing, thus contributing to significant lower production costs. Fig. 1.5 depicts a micrograph of the isolator before packaging [19]. Moreover, capacitive isolators offer higher level of integration than optocouplers and their high impedance entails very low current consumption.

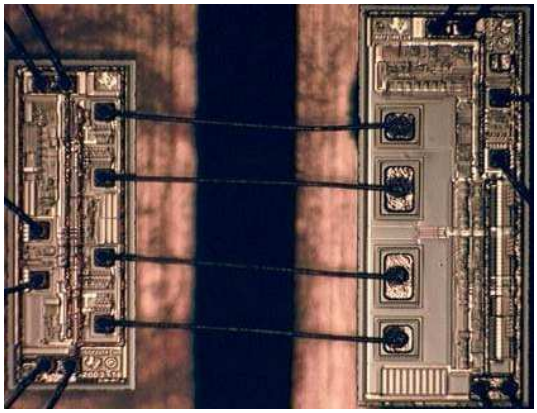

Figure 1.5 Photo of the system before packaging [19]

Clearly, the fully integrated insulation approach is the key factor in providing these advantages: silicon di-oxide is known as one of the best dielectric insulator with reported dc dielectric strength around $850\ V/\mu m$ for pure samples, which is much higher than organic-based compounds [20].

Unfortunately, capacitive isolators suffer by high sensitivity to common-mode transients (CMTs) and electric fields. Indeed, the two isolated interfaces having two different grounds can be affected by grounds shift that cause common-mode currents to flow through isolation capacitors causing hazardous voltages and/or data corruption. A key parameters of isolators is their ability to reject fast common-mode transients, commonly indicated by common-mode rejection (CMR) or the common-mode transient immunity (CMTI) measured in kV/μs. It is measured by applying sharp voltage pulses between the two isolated ground references of the device, and defined as the maximum voltage slew-rate that the isolator is able to withstand without affecting its data transfer

performance. Typical values for CMTI are lower than 25 kV/µs for optocouplers, whereas capacitive isolators can achieve CMTI up to 100 kV/µs thanks to differential signalling even if a complex additional circuitry is required.

Magnetic Isolators

Magnetic isolators, and particular the inductive ones[1] exploit a changing magnetic field between two coils to communicate across an isolation barrier and they are the most diffused integrated approach in semiconductors manufactures. As in a capacitive isolators, two chips include a transmitter and a receiver, whereas the dielectric of the planar transformer is exploited to guarantee galvanic isolation, as depicted in Fig. 1.6. In 2001 Analog Devices introduced the first magnetic isolator with the iCoupler technology [21]. The planar transformer has been fabricated by using two stacked spiral coils which are isolated by a thin-film dielectric, as shown in Fig. 1.7 (a). The iCoupler technology adopts a 20-25 μm-thick polyimide (PI) layer to perform isolation, depending on the isolation rating.

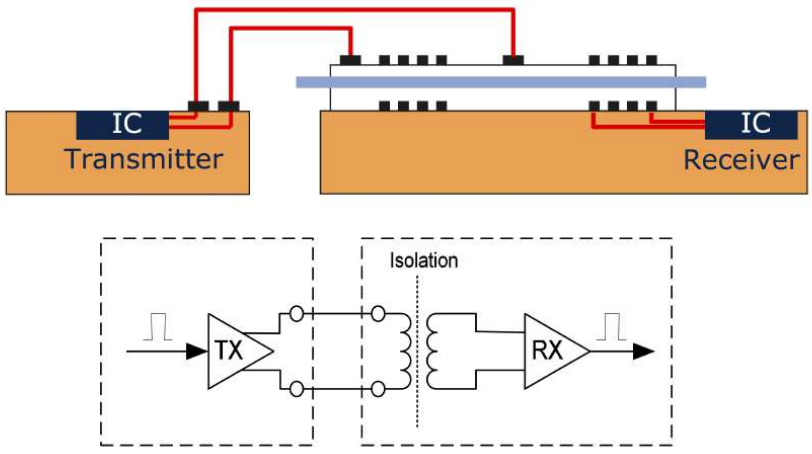

Figure 1.6 Integrated inductive isolator architecture

[1] Other magnetic isolation techniques include Hall-effect and giant magneto resistance links, which can be only used for data transfer applications. Besides, isolation in these technique is often achieved at the package level, similarly to optocouplers.

A 6-μm thick electroplated Au layer is used for the top transformer spiral, whereas the IC top metal layer is used for the bottom one. A photo of a four-channel isolator before packaging is shown in Fig. 1.7 (b). Differently from capacitor-based isolators, transformer-based isolators are more suited for data and power transfer. Indeed, the capacitive coupling between transformer's windings is a parasitic effect, which is further reduced when high dielectric thickness is used, thus increasing both CMTI and isolation rating. Several systems able to transfer both data and power in packages (SiPs) are currently available in the aforementioned technology, with output power levels from tens to few hundreds of milliwatts and data transfer channels in a multi-die SiP, depending on the output power and complexity of the device [22].

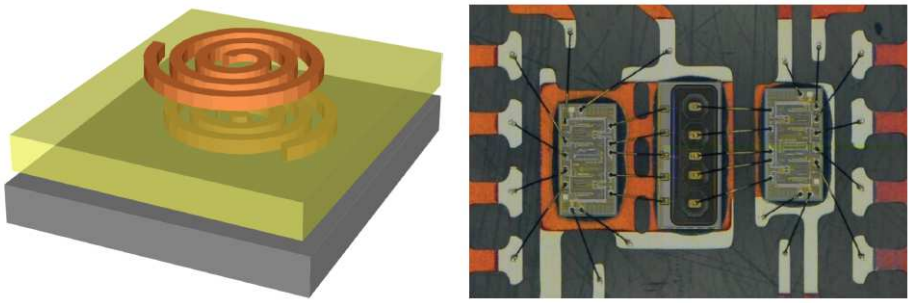

Figure 1.7 (a) Planar isolation transformer. (b) Photo of an inductive isolated system before packaging [21]

The micrograph of one of these systems is shown in Fig. 1.8 (a). It is worth nothing that the data and the power transfer exploit different channel, thus requiring different transformer. Moreover, for power transfer applications both power transformer's coils require thick Au metals to achieve good efficiencies, thus increasing manufacturing costs. Recently, a lot of products exploiting on-chip galvanic isolation have become available for the application discussed in Section 1.2, e.g. general purpose isolators [23], [24], [25], fully integrated isolated

data and power transfer [26], isolated analog-to-digital converters [27], digital isolators [28] and so on.

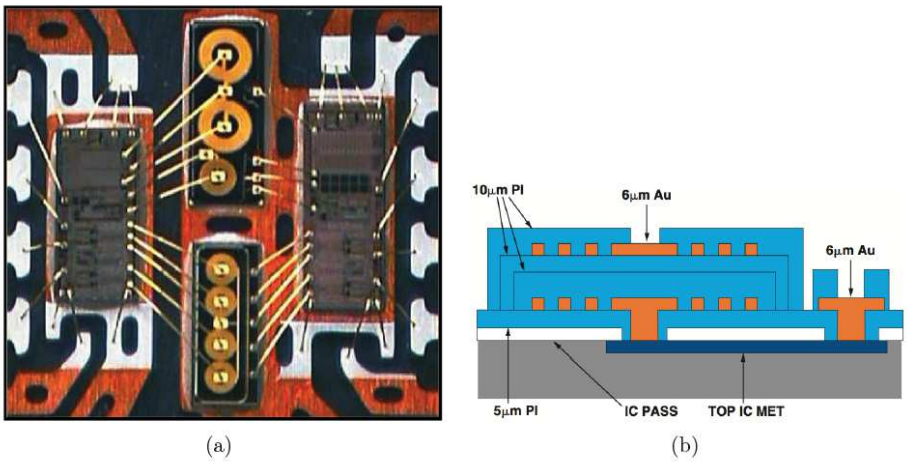

Figure 1.8 (a) Data/power SiP before packaging. (b) Cross-section of isoPower transformer

To enable cost-effect integration, the main challenge of the isolated dc-dc power converter with data transfer is achieving a good trade-off between efficiency and power density while providing a high data rate with a good CMTI performance.

Component regulations

Component regulations are the counterpart of system regulations defining the components specifications needed to guarantee a certain level of protection within a system. Generally adopted component-level standards are the following:

- UL 1577
- IEC 61010-1[2]
- IEC/DIN/EN 60747-5

[2] Safety standard for measurement, control and lab equipment", also defines component requirements.

- VDE 0884-10

Two main class of component standards can be recognized: UL 1577 and IEC 61010-1 focus on voltage breakdown, whereas norms such as VDE 0884-10 and IEC 60747-5 are based on partial discharge tests [29].The first class consists in breakdown-voltage tests to characterize the robustness of the device to over-voltage conditions. Breakdown is achieved when a substantial leakage current can be detected across the isolation barrier. For example, UL 1577 defines the isolation withstand voltage V_{ISO} that is the RMS value that can be sustained for one minute. Lot-samples are tested to establish the voltage rating of the component, with common required values of $1\ kV_{RMS}$, $2.5\ kV_{RMS}$, $3.5\ kV_{RMS}$ and $5\ kV_{RMS}$.This test is destructive: the device must survive for only one-minute, but may fail for longer duration and this over-voltage condition should not be applied anymore. Each device must also pass a one-second non-destructive test at $1.2 \cdot V_{\mathrm{ISO}}$ during production. These tests do not characterize the ability of the device to withstand periodic or continuous voltage stress. On the other hand, standards like VDE 0884-10 and IEC 60747-5 look for partial discharge across the isolator, which may degrade the lifetime or the insulation rating of the barrier if a second test is performed [30]. For example, both IEC 60747-5 and VDE 0884-10 require the devices to be tested with the waveforms defined in Fig. 1.9. Here VIOTM is the peak transient voltage that the device can sustain, and it is equivalent to UL 1577 isolation withstand voltage V_{ISO} for sinusoidal voltage stress. After the transient voltage the device is tested for partial discharge for a certain voltage that is proportional to the maximum peak repetitive voltage V_{IORM}, or the working voltage V_{IOWM} for RMS or dc rating. Method A and method B1 differ for voltage values and measuring times and are used for lot-samples and production tests, respectively.

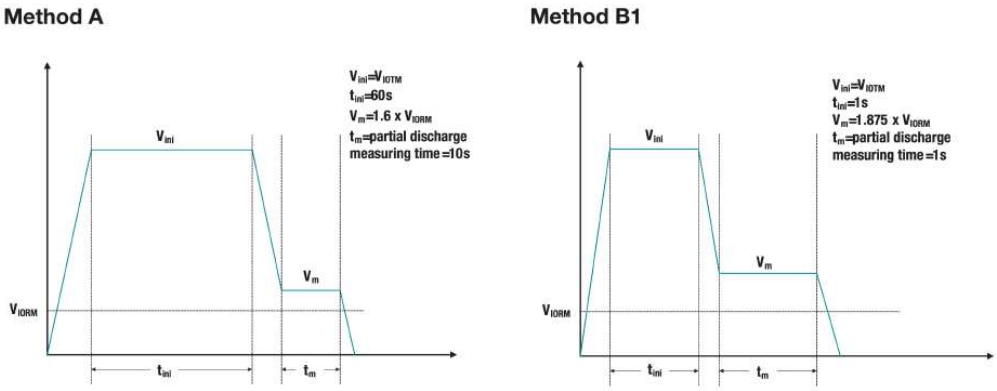

Figure 1.9 Simplified IEC 60747-5 and VDE 0884-10 test profiles [30]

Most regulations were developed when only optical isolators were available and are tailored to their physical structure, where the insulator thickness (a.k.a. *distance through insulator* or DTI) is very high. This is the case for UL 1577 and IEC 60747-5, which only apply to optical isolators. Recently VDE 0884-10 has been developed to expressly take into account the availability of highly integrated semiconductor isolators with micro-scale isolation barriers, either using magnetic or capacitive transfer approach. It certifies reinforced insulation as well as IEC 60747-5-5, but it also includes a 10-kV surge test, which is performed with the waveform in Fig. 1.10, where V_{SURGE} (a.k.a. V_{IOSM}) is the maximum surge isolation voltage [31]. A new standard releases either at component or system level are planning to take into account these new thin-film semiconductor devices [30, 9]. It is also worth noting that many component standards and system-level regulations as well, often pose specific requirements on the clearance (i.e. distance through air) and creep age (i.e. distance along the surface) of the isolator's package, as defined in Fig. 1.11, and its fabrication materials.

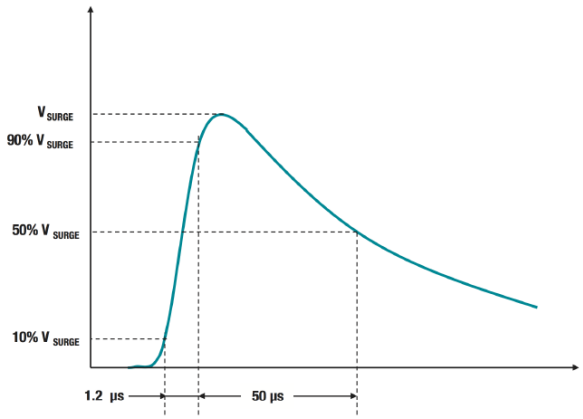

Figure 1.10 Simplified VDE 0884-10 surge test profile [30]

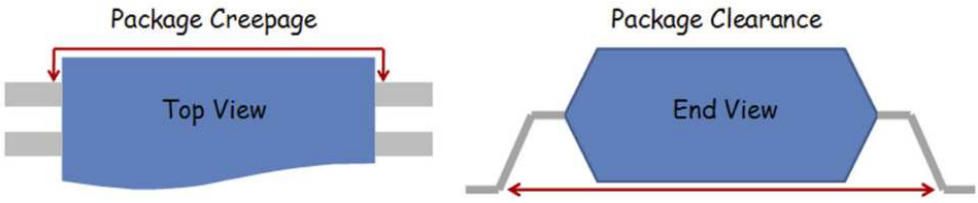

Figure 1.11 Definition of clearance and creepage [31]

1.4 Isolator's market

Usually highly-specialized companies provide a quantitative estimate of market because their revenues is a quite complex task. Through a unique combination of information, analytics and expertize it is possible to elaborate detailed reports about specific business markets, macroeconomic areas, global trends and so on. Besides these reports, the few isolator's market data available for free on the internet can also prove useful to understand the amount of isolator's business and hence the importance of innovation in this field. IHS is one of a global information company with world-class experts in the pivotal areas shaping today's business landscape. In [32], released on 2013, December, a compound annual growth rate (CAGR) up to 10-20 % from 2013 to 2018 is

expected for optocouplers, which have been the mainstream isolator technology. Particularly, the gate driver market is expected to experience high-growth, according to this report. Optocouplers market is estimated around $ 1.3 billion, with $ 543 million from high performance optocouplers, in spite of their drawbacks when compared with the already discussed integrated isolators.

Another report from IHS, released on 2014, May, contains the graph in Fig. 1.12 that is referred to the worldwide isolation market. It is available at [33], where a growth of 8 % between 2012 and 2013 is reported, thus confirming $ 1.33 billion of market revenues in 2013. One of the key point for this growth is the automotive market: while being only 10 % of total optical isolation market in 2013, a Hybrid & Electric Vehicles (HEV) growth of 7 % was observed in 2012/2013 and it is expected to rise up to 18 % in 2014.

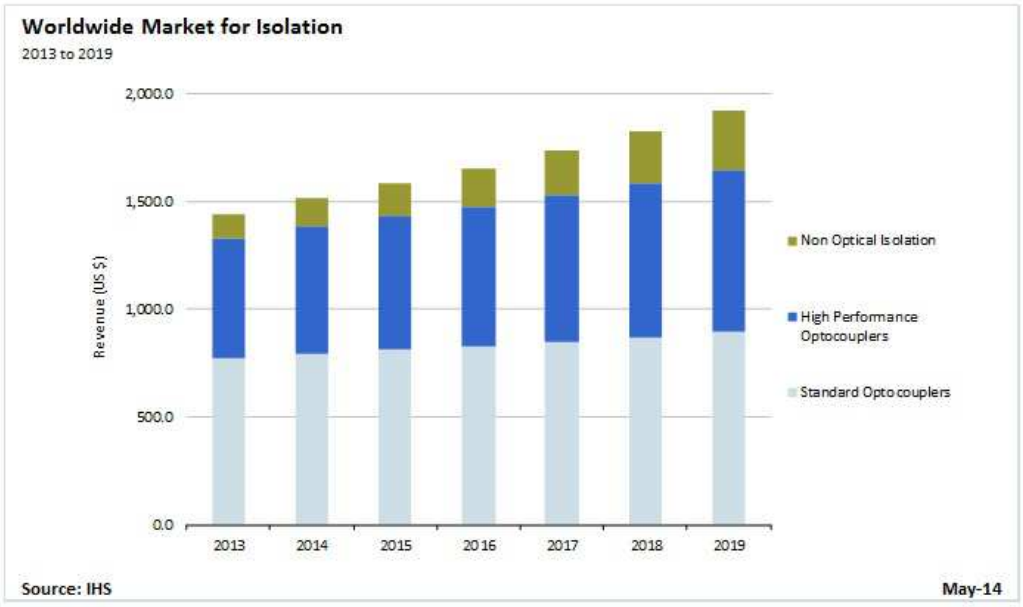

Figure 1.12 Forecasts for worldwide isolation market [33]

According to the report, a CAGR of 12 % is expected between 2013 and 2019 for optocouplers and solid-state relays in this market. For a comparison, industrial market is expected to grow by 12 % between 2014 and 2019 instead, that is a CAGR around 4.7 %. Fig. 1.12 and [33] also put a glance on non-optical

isolators. IHS states that many manufacturers such as Analog Devices Inc., Texas Instruments and Silicon Laboratories have released products or hold patents in this area. Non-optical isolators show increasing success in new and high growth markets such as PV inverters, smart meters and especially HEV due to higher performance and reliability. It is worth nothing again that this is a market where high-performance devices are required, with relatively higher value with respect to industrial applications. Optocouplers companies like Avago, Toshiba and Renesas are trying to compete by introducing new high performance optocouplers but most of their sales occur in the traditional and more stable industrial markets and hence their growth may be lower compared to non-optical isolator companies.

Finally, it is worth nothing that the growing interest and high value of the Galvanic Isolated ADC market. According to a report from IHS on the Galvanic Isolated ADC market [34], the ADC (analog to digital conversion) market was worth $ 163 million or 12 % of the total isolation market. ADC Isolation is also forecast to grow faster than the whole isolation market. As unit shipments, under 2 % of the isolation market is in ADC, but these products have a much higher price, estimated at an average $ 1.03 in 2013 (158 million units in 2013). Avago was the no. 1 supplier of ADC isolation in 2013, mostly based on standard optocouplers, and other suppliers include Fairchild, Renesas, Sharp and Toshiba but also ADI, with the already discussed iCoupler technology, was mentioned. It is worth noting that ADI reports that more than 1 billion digital isolated channels were sold between iCoupler introduction and 2013 [34].

Although the reliability of these almost exponentially growing extrapolated data as well as the quality of market analysis and financial advisors are quite subjective, it is clear that an actual growth of isolated converters took place between 2012 and 2014. More solid reasons for this growth are the increasing policy support of governs and their commitment towards the reduction of global pollution and CO_2, as already pointed out in [35]. To this end a system that provides an isolated dc-dc power converter while allowing a data transfer is preferred.

1.5 Aim of this thesis

As discussed in the previous section, a wide range of application can advantage of fully integrated system performing on-chip galvanic isolation. Applications such as industrial process control, power supply regulation and point-to-point communication can be described by the general block diagram shown in Fig. 1.13. Here, two tied interfaces are often separated by long distances, so galvanic isolation is typically required to break up grounds loop, protect the system from high-voltages transients, and reduce signal distortion, as well as for physical safety. Data transfer are performed across the galvanic isolation barrier to carry out the communication between the two interfaces, whereas isolated power supply for the second domain should be derived from the first one.

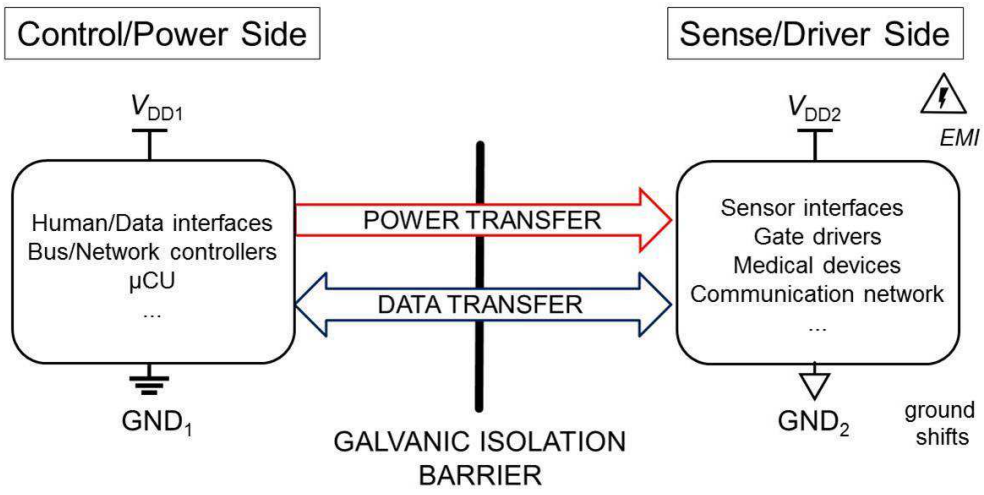

Figure 1.13 Typical low-power applications requiring isolated data and power transfer

By taking advantage of research in semiconductor technologies, some of these applications can be addressed with a fully integrated approach, thus providing on-chip galvanic isolation, while avoiding any discrete or post-processed components. The market for these applications presents solid growth opportunities for next decades, however most players focus on data and

power transfers by exploiting different channel. Moreover, several data transfer applications have already been successfully faced in silicon technology, whereas, further to the power transfer, the most advanced implementations still involve post-processing steps including deposition of both thin-film dielectric and thick metal layers. Then the implementation of fully integrated system able to transfer both data and power by exploiting a single inductive channel is an ambitious result being a key competitive advantage to gain market share in the expected growth scenario.

In this work, we focus on circuit and system design techniques to achieve fully integrated data and power transfer with currently available silicon technologies. Technology aspects regarding the implementation of on-chip galvanic isolation are not covered, since the whole technology platform was supplied by STMicroelectronics. Due to the huge, inherent complexity of developing an isolator, we only focus on the key electrical aspects of the circuit design that are the amount of output power and robustness of data transfer, thus carrying out the maximum efficiency and the minimum bit error rate (BER), respectively, for a given technology. In this section the basic architecture of the developed systems is presented as well as the adopted technology platform and the main results achieved

1.5.1 Architecture of system

At present the most promising approach for fully integrated dc-dc isolated power converter with data transfer uses architecture exploiting the magnetic coupling. This approach is based on transformer-loaded oscillator that performs the dc-ac power conversion, a planar integrated transformer which guaranteed the galvanic isolation, a rectifier to provide the ac-dc power conversion and data blocks which are able to perform the bi-directional data communication. The key element of these systems is the power oscillator including the integrated isolation transformer which affects the power efficiency performance while driving the choice of the system architecture. In particular, the adopted oscillator is based on

current-reuse technique and output power combining, then a three coils-transformers has been implemented. It consists of four inductors for the two primary coils which are arranged through two symmetric interleaved configurations, one for each stacked secondary coil. The thick oxide between the primary and secondary coils guaranteed the galvanic isolation rating up to 5 kV. Since only thin metal layers are available in standard silicon technologies, these windings show very high series resistances, which involves very high operation (VHF) frequencies as well as resonance to improve their poor quality factor (Q-factor) [36].

Following these considerations a novel architecture has been conceived for the proposed system and a simplified diagram block is shown in Fig. 1.14.

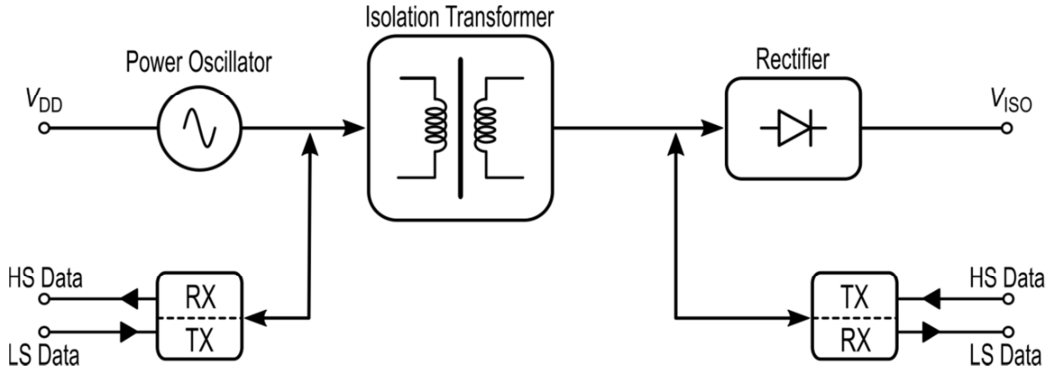

Figure 1.14 Novel architecture for isolated data and power transfer system

Here, the data and power transfer exploit a single inductive channel to be transferred across the isolation barrier [26]. The dc-dc power converter is a transformer-loaded power oscillator, whose resonant network includes the isolation transformer and the rectifier input impedance. It converts the power supply P_{DD} into ac power P_{AC} for the isolation transformer and hence the rectifier input. A full-bridge rectifier has been chosen as the simplest balanced topology to perform the ac-dc power conversion, thus converting the ac power at the transformer output into dc available output power P_{OUT} for the load, with output voltage V_{ISO}. Each block suffers from power losses which can be expressed by a power efficiency, i.e. η_{OSC}, η_{TR} and η_{RECT} for the oscillator core, the isolation

transformer and the power rectifier, respectively. Their product can be used to express the whole power efficiency of the dc-dc power converter, $\eta_{DC/DC}$ or simply η. As discussed before, the system is also able to perform half-duplex bi-directional data communication. It is performed by using a simple amplitude shift keying (ASK) modulation in order to preserve the peak of the RF control signal. In particular, high-speed (HS) data communication (from isolated sense side to control side) is implemented by means of impedance mismatch at secondary coils of the integrated transformer, while the low-speed (LS) data transmit (from control side to isolated sense side) is implemented by switching a series resistances, thus modulating the oscillation signal of the power oscillator.

Main advantages of this architecture include the use of a single isolation transformer for both isolated power and bidirectional data transfer, thus lowering costs and reducing package and application board sizes.

On the other hand, this architecture is inherently characterised by highly non-linear interactions between each block, which complicate the design. For example, transformer efficiency is highly dependent on the interaction with the driving stage, providing the ac input power, and the cascaded stage, which performs the ac/dc conversion. Moreover, the oscillator is inherently subject to parasitic and input supply variations and do not provide voltage regulation. Finally, the data maximum data rate is not far by the carrier frequency, thus complicating the operations of demodulation.

1.5.2 Technology platform

The technology adopted in this work is a 0.35-μm SOI-BCD technology that features both 3.3-V and 5-V CMOS transistors, a 5-V VHF npn BJT, lateral pnp BJTs and several MOS devices providing high-voltage capabilities through drain-extension techniques [37]. Three Al metal layers with 0.45/0.55/0.9-μm thickness, respectively, and a 3.7-μm thick top Cu layer are available for routing. The process was enriched for this work by a thick-oxide module [38] that was

previously developed and characterized for galvanic-isolated data transfer, similar to other state-of-the-art integrated isolators [39], [40], [41]. This module has been recently used for mass-production of several devices providing on-chip galvanic isolation [42], [23]. The tick oxide layer is placed between the two top metal layers, as shown in the simplified back end of line (BEOL) cross-section of Fig. 1.15. Depending on the galvanic isolation rating the tick oxide can have different thickness.

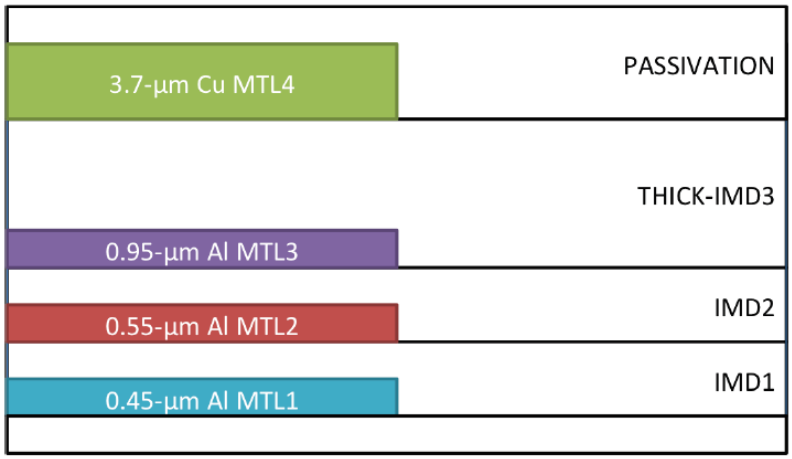

Figure 1.15 Simplified cross-section of the available back end of line with thick

This technology powered by STMicroelectronics was chosen thanks to its compatibility with the thick-oxide module fabrication process and by the high resistivity of the available SOI substrate that is mandatory to achieve high efficiency for power transformers. Is worth noting that, the galvanic isolation rating of this adopted technology has been certified up to 5 kV.

1.5.3 Main results

For the first time a fully integrated CMOS system, able to transfer both data and power on the same isolation transformer was demonstrated. It can be adopted in an interesting real-life application requiring isolated data and power transfer which was addressed during this work as a part of a research project at the

RF-ADC, a joint research center between the University of Catania and STMicroelectronics. As outcome, during my permanence at RF-ADC two full integrated system were designed and characterised in the available technology by different design teams, showing measured performance that are competitive with the state of the art.

They are:

- a highly integrated data and power transfer system, with relatively low output power, for autonomous sensors applications [26].
- medium power CMOS dc-dc converter, with output power of 200 mW for power supplies of general purpose circuitry [43].

General purpose circuitry, such as wireline transceivers and signal processing blocks that require lower output power can benefit of these innovative integrate systems, thus lowering costs while using the widespread CMOS devices demonstrated in [43], and as will be disclosed in Appendix A. Autonomous current sensor interfaces require quite low output power, e.g. around 10-25 mW even if leading to use of multiple isolation transformer, thus increasing costs and complexity. The proposed architecture in [26] enabling both data and power transfer by means of a single inductive channel, shows a competitive advantage with respect to the state of the art even if it does not include any circuitry to improve the CMTI. Lastly, in order to overcome this limits a different system architecture can be implemented. It would be able to deliver a regulated output power up to 100 mW, while providing a half-duplex data communication having maximum data rate up to $50\ Mbit/s$ and CMTI up to $50\ kV/\mu s$.

Chapter II

Fully integrated galvanically isolated power transfer systems

This chapter takes on the detail descriptions and the design of a fully integrated dc-dc converter with galvanic isolation in order of several kilovolts, i.e., 5-kV. The converter was designed to produce about 30 mW output power, P_{OUT}, at 3-V output voltage, V_{OUT}, from a 3-V power supply, V_{DD}. To enable a wide range of low-power applications requiring an isolation barrier, the reduction of cost, complexity and size is a crucial target to be reached. An upper bound of 5 mm^2 for the whole area and a novel architecture for dc-ac power converter were chosen as a reasonable specification for the isolated power transfer system. Indeed, the design was customized to the maximization of power efficiency being a crucial aspect for autonomous low-power isolated sensors.

2.1 System description

A simplified schematic of the fully integrated isolated dc-dc converter is shown in Fig. 2.1. The integrated transformer, T_{ISO}, is the core of the system since it provides on-chip galvanic isolation and power transfer. In the proposed implementation it is integrated into the chip A with a novel power oscillator circuit exploiting the current-reuse technique, whereas a second die includes a well-known full-bridge rectifier for ac-dc power conversion, and the turn's ratio of the integrated transformer is used to obtain the required step-up voltage conversation ratio. The power transfer system was fabricated in 0.35-μm BCD-SOI technology providing on-chip galvanic isolation, as described in Section 1.5.2.

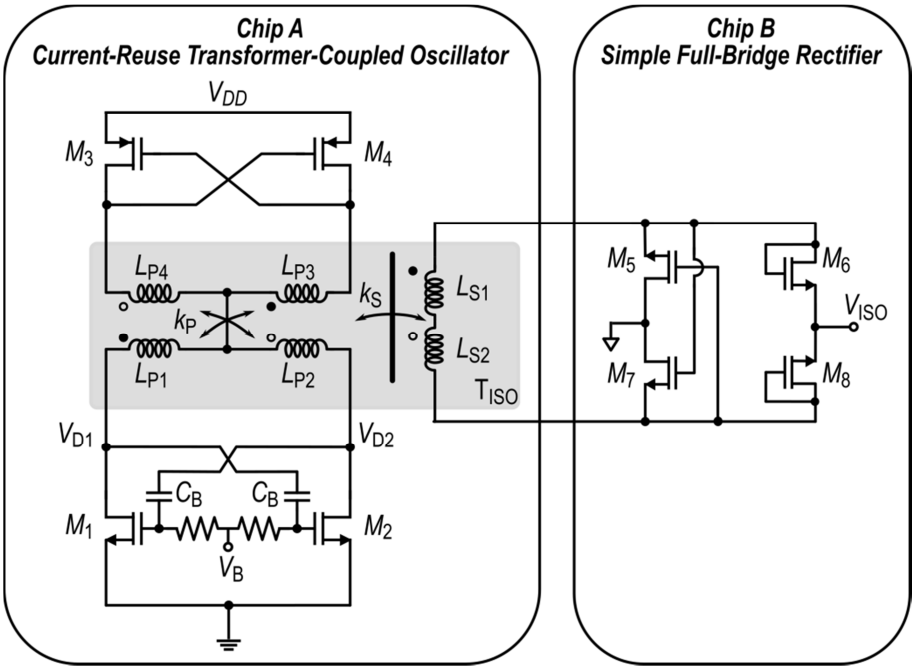

Figure 2.1Schematic of the fully integrated data and power transfer system

2.2 Design issues

The description fulfilled in this section is helpful to better understand the role of each block including in the power transfer link and the impact of each block parameters on the efficiency of other blocks. For a given output power, the main goal of the design is to maximize the system power efficiency while guaranteeing both small silicon area and proper CMTs rejection, which are crucial specifications in galvanically isolated power transfer systems.

Rectifier is the simplest block providing the ac-dc conversion and showing a well-defined and direct relationship between its sizes, in particular M_{NMOS} (i.e., $M_{5,6,7,8}$) and both power efficiency η_{RECT} and input capacitance C_{RECT}.

The transformer gives the main contribution to the whole area of the integrated dc-dc converter (i.e., more than 50 % of the overall silicon area). It also greatly affects the overall power conversion efficiency, thus requiring the maximization of quality factors and magnetic coupling factors. They both depend

on the geometrical parameters and the available back-end-of-line (BEOL). Indeed, to maximize the transfer efficiency the operating frequency has to be kept as close to the resonant frequency f_{RF} due to the secondary coil and the input rectifier capacitance.

The oscillator core is the most complex and important block in the power transfer chain. Its non-linear behaviour needs high tank inductance and minimum external capacitance for a given transistor's width to work with high efficiency. To this aim, the equivalent parallel losses resistance seen at primary side, $R_P \cong \omega \cdot Q \cdot L_P \cdot (1 + k_P) \cdot (1 + k_S^2)$ have to be maximized. By taking advantage of stand-alone block performance and their relationships, an optimized system design can be achieved. Moreover, these considerations confirm that no significant result can be reached by designing each system block as a stand-alone circuit. Instead, optimum performance can be obtained by adopting an iterative co-design procedure between the dc-dc converter building blocks. Eventually, a proper design strategy is mandatory to perform this co-design due to the large number of free design variables.

2.3 Efficiency analysis and block design of the isolated dc-dc power converter

The design of this isolated dc-dc power converter poses several challenges since it is characterized by non-linear interactions between each building stage, thus involving system optimization if the output power have to be delivered with high efficiency. In order to achieve high power efficiency while adopting scaled technologies, transformer-loaded oscillators exploiting a current-reuse technique have recently gained attention. In this section each block of the power transfer system will be descripted examining how its efficiency depends on the design parameters of the converter, as well as on the loading effect of the other blocks, to better understand main issues and trade-offs between each building block designed. The overall power system efficiency, η, is obviously the product of the

efficiency of each building block when operated into the whole system. Specifically, the power flow from the power supply, P_{DD}, to the dc power delivered to the load, P_{OUT}, involves losses in the active devices, in the integrated transformer, and in the rectifier, as detailed in the flow diagram depicted in Fig. 2.2. The total power at the transformer input coils is called P_{TX} while P_{OUT_AC} is the ac power at its output.

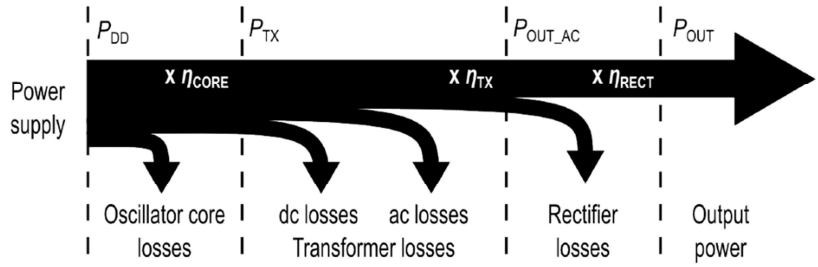

Figure 2.2 Power transfer flow diagram

The rectifier efficiency, η_{RECT}, is defined as P_{OUT}/P_{OUT_AC}, whereas the efficiency of the integrated transformer, η_{TISO}, is defined as P_{OUT_AC}/P_{TX}. We also define the active core efficiency, η_{CORE}, as P_{TX}/P_{DD}, hence:

$$\eta_{RECT} = \frac{P_{OUT}}{P_{OUT\_AC}} \tag{1.1}$$

$$\eta_{TISO} = \frac{P_{OUT\_AC}}{P_{TX}} \tag{1.2}$$

$$\eta_{CORE} = \frac{P_{TX}}{P_{DD}} \tag{1.3}$$

$$\eta = \eta_{RECT} \cdot \eta_{TX} \cdot \eta_{CORE} \tag{1.4}$$

Starting out by the rectifier we analyse the design of each block of the proposed dc-dc power converter with galvanic isolation.

2.3.1 Rectifier

The rectifier provides the ac-dc power conversion, thus receiving the P_{OUT_AC} from the isolation transformer it produces the dc output power (P_{OUT}). The SOI-BCD technology platform adopted does not include Schottky diodes, hence a simple CMOS full-bridge rectifier was used (see Fig. 2.1). The main parameters of this block are the conversion efficiency η_{RECT} and its input impedance, which can be represented as a *RC* parallel circuit, $R_{RECT}//C_{RECT}$. Indeed, the η_{RECT} depends on both the transistors' multiplicity (M_{NMOS}) and the dc output power P_{OUT}. The design was focused on the maximization of the conversion efficiency η_{RECT} at the required output power, P_{OUT}, by setting the multiplicity M_{NMOS} (i.e., $M_{5,6,7,8}$). The frequency response of the rectifier highlights a degradation of its conversion efficiency at increasing frequencies, thus an upper limit to the operation frequency (i.e., the oscillation frequency) was set. The Fig. 2.3 (a) shows η_{RECT} as a functions of the output power for M_{NMOS} between 10 and 30 with a 330-MHz input signal and 3-V V_{OUT}. For increasing power levels a higher number of transistors is required to do not compromise the efficiency performance. The input resistance, R_{RECT}, reported in Fig. 2.3 (b) is inversely proportional to P_{OUT} and does not increase with M_{NMOS}, whereas the input capacitance, C_{RECT}, shown in Fig. 2.3 (c) is almost constant with M_{NMOS} and it is independent of P_{OUT}. For the sake of clarity, the simulated η_{RECT} and input impedance, $Z_{RECT}= R_{RECT}//C_{RECT}$, for different values of M_{NMOS} at the target P_{OUT} of 25 mW at $V_{OUT} = 3$ V, are summarized in Table 2.1. It is obvious that for $M_{NMOS} > 20$ a small efficiency improvement can be obtained at the cost of increased rectifier area, input capacitance and, most importantly, routing complexity. We set M_{NMOS} equal to 20 as trade-off between η_{RECT} and C_{RECT}. This choice takes into account the fact that this block can easily provide high efficiency when compared to other blocks in the power chain.

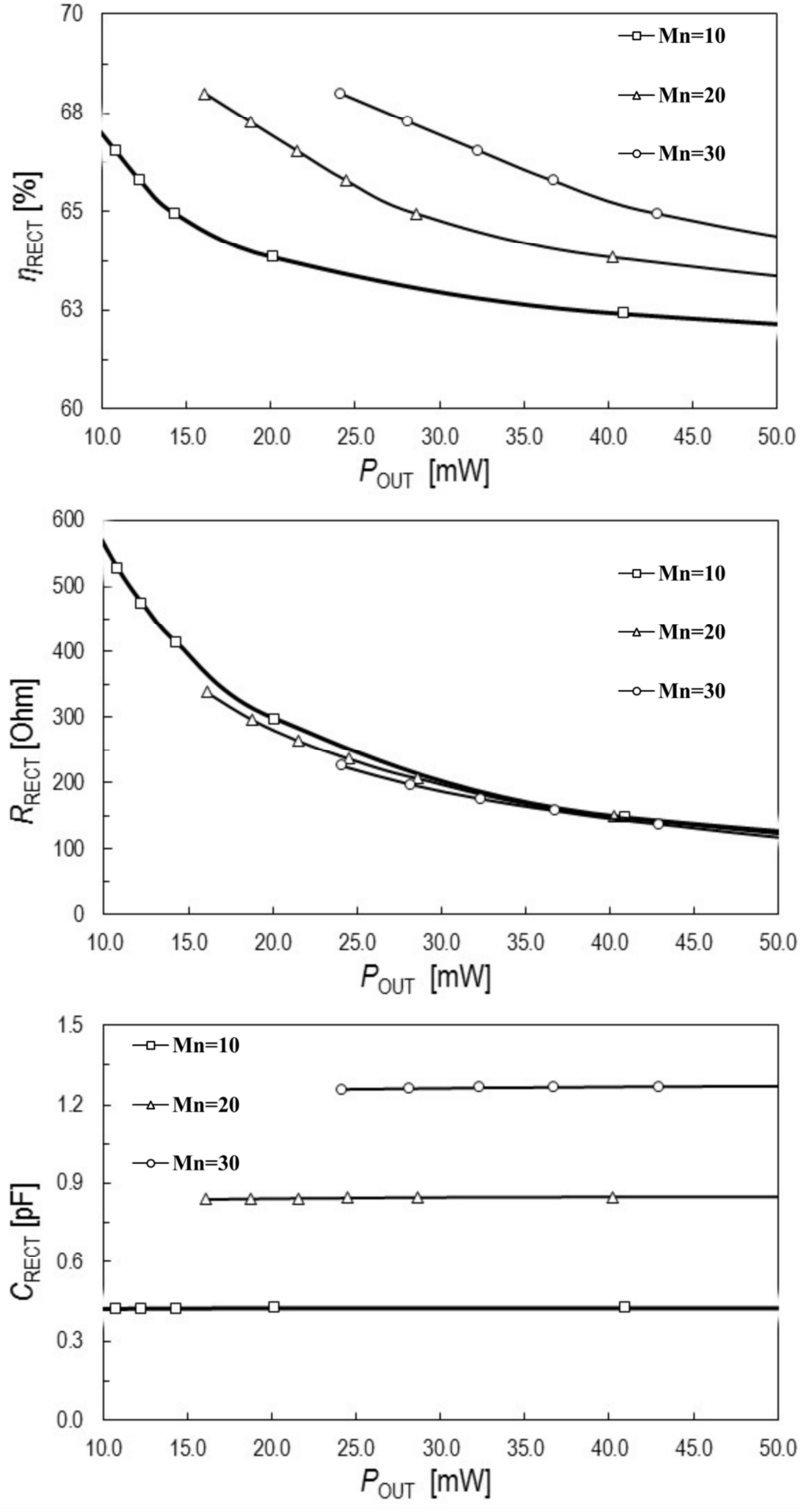

Figure 2.3 Rectifier efficiency as function of output power for different M_{NMOS} (i.e., $M_{5,6,7,8}$)

Table 2.1 Simulated rectifier performance, V_{OUT}= 3 V, P_{OUT}= 25 mW

	M_{NMOS}	η_{RECT} [%]	R_{RECT} [Ohm]	C_{RECT} [pF]
Schematic	10	63.4	248	0.42
	15	64.3	236	0.63
	20	65.7	234	0.84
	25	66.9	224	1.05
	30	67.8	220	1.26
post-layout	20	61	228	1.5

Another important design issue is represented by the rectifier layout: parasitic due to metal connections highly affect efficiency performance and the input capacitance, especially when a high number of transistors have to be connected. Main degradation of both efficiency and bandwidth comes from the resistive parasitic, which were minimized by exploiting all the available metal layers (i.e., metal 1 to metal 4 plus alucap) and optimizing the number of vias. Simulations show that for operating frequencies smaller than 400-MHz the rectifier characteristics are quite constant, and thus it was modelled by an input impedance Z_{RECT} of 228 Ohm//1.5 pF for P_{OUT_AC} = 25 mW at V_{OUT} = 3V.

2.3.2 Oscillator core

The oscillator performs the dc-ac power conversion by exploiting the isolation transformer as resonant load. It is another key block of an isolated power transfer system since it greatly determines the maximum delivered output power and the overall efficiency. One of the most adopted circuit exploits the well-known cross-coupled nMOS topology as shown in Fig. 2.4 (a), which operating in class D improves the power efficiency.

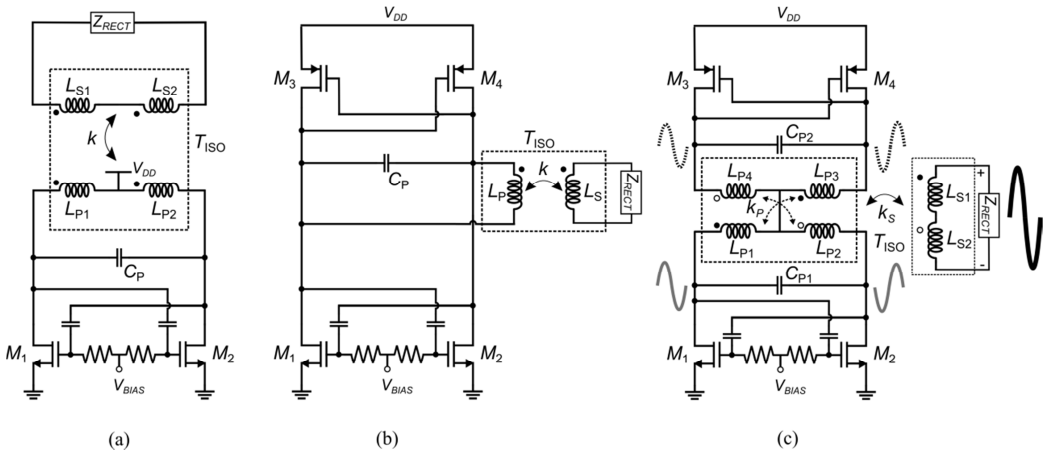

Figure 2.4 Oscillators topologies for isolated power transfer. (a) Class D Oscillator. (b) Complementary cross-coupled oscillator. (c) Current-reuse oscillator

RF class D oscillators have gained attention in highly scaled technologies, for design approaches mainly focused on low power applications [44], thanks to its advantages in term of low phase noise. In fact, this topology makes possible to combine low phase noise, low supply voltage and high efficiency simply by increasing the size of the cross-coupled nMOS switches, thus maximizing the oscillation amplitude. However, this topology requires special devices, such as lateral-diffuses or thick-oxide transistors with higher breakdown voltages, to sustain drain voltages that can reach a pick of approximately $3 \cdot V_{DD}$. When only a standard CMOS technology is available, the complementary cross-coupled architecture shown in Fig. 2.5 (b) is used. This solution allows to reduce the power consumption while avoiding breakdown issues [45], being its oscillation level inherently contained within the supply voltage. For small-signal operation it provides higher small-signal trans-conductance for the same biasing current, thanks to the double cross-coupled pair. However, for large-signal operation this advantage is less important, since very high transistor's width are required to provide ac power with high efficiency and trans-conductance is not a problem. Although the active devices can easily reach the deep triode region to minimize power losses, for power transfer applications the efficiency of this topology is still lower than the class D oscillator, due to lower oscillation level and higher losses in the active devices. Indeed, the differential voltage across the primary coil can

be around V_{DD} at most, which entails higher currents in the coil for a given power level, and during operation two devices are always stacked for each path between power supply and ground, apart from the primary coil, instead of only one. Therefore, novel transformer-loaded topologies are required to improve performance while avoiding breakdown and properly exploiting the characteristics of integrated transformers at the same time. This aspect is particularly important since passive devices are the bottleneck for both power efficiency and power density in standard technology. A novel topology which has been found to satisfy these requirements is shown in Fig. 2.5 (c). It performs three key aspects, i.e. inductively coupled oscillators, current-reuse technique, and output power combining [46]. The circuit is made up of two *LC* complementary CMOS oscillators, i.e., $M_{1,2}$-$L_{P1,2}$ and $M_{3,4}$-$L_{P3,4}$, which share the same supply current and whose tank inductors are magnetically coupled to each other according to the dot-scheme represented in the figure. In particular the inductors $L_{P1,2}$ and $L_{P3,4}$ form the two primary windings of the isolation transformer, T_{ISO}, whereas inductors $L_{S1,2}$ make the second winding. If the magnetic coupling coefficient between the primary windings, k_P, is sufficiently high (typically greater than 0.6) frequency synchronization of the two oscillators is reached [47], [48]. Thanks to the magnetic coupling between the primary coils, the equivalent load inductance of each oscillator is boosted by the factor $(1+k_P)$, while maintaining the same resistive losses. The signal produced at each primary winding is then delivered to the secondary winding of T_{ISO}, where a power combining is performed, thus nearly doubling the overall output power on the rectifier input. The magnetic coupling between primary and secondary coils, k_S, is 0.8. In this configuration thanks to the current-reuse arrangement, which is easily implemented by means of the central-tap of the primary windings, the further improving of the oscillator power efficiency is allowed. In particular, this architecture compared with the complementary cross-coupled topology, has highlighted an increase for both output power and power efficiency higher than 10 % and 40 %, respectively. This comparison was carried out in the same CMOS process, at equal supply voltage and Z_{RECT}, and for the same frequency oscillation. Moreover, the total silicon area was kept constant for both the active core and the isolation

transformer, which is a key constraint in this context. It is worth noting that to maximize the power efficiency at the given output power a co-design procedure between the oscillator core and the transformer is required, thus exploiting this procedure we will design the oscillator core.

2.3.3 Isolation transformer

The implementation of the integrated isolation transformer involves the use of a staked configuration for primary and secondary windings. Indeed, the galvanic isolation is guaranteed by the thick oxide layer between the top metal layers (i.e., metal 4 and metal 3) of the adopted technology platform. As discussed in the previous section, the adopted power oscillator based on current-reuse technique requires an adequate magnetic coupling factor k_P in order to achieve an optimized power combining into the third winding. To this aim a three coils-transformer is implemented, as shown in Fig. 2.5. Specifically, the four inductors of the primary windings, L_{P1}-L_{P4}, are arranged through two symmetric interleaved configurations, $L_{P1/3}$ and $L_{P2/4}$, one for each secondary coupled coils (i.e., L_{S1} and L_{S2}), with a common terminal for the central-tap.

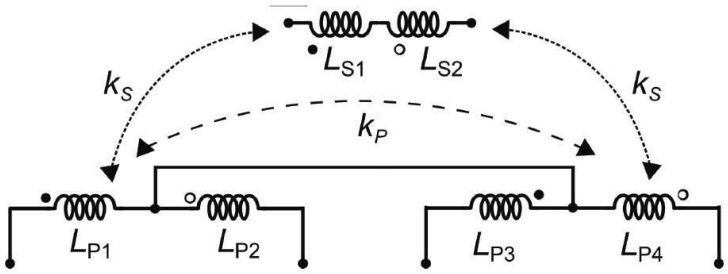

Figure 2.5 Isolation transformer schematic

Thanks to the minimum spacing (1-μm) available on the metal 3 for $L_{P1/3}$ and $L_{P2/4}$ the magnetic coupling is further maximize. Instead the secondary coils, L_{S1} and L_{S2}, are built exploiting the metal 4 and they are staked on the primary coils, as shown in Fig. 2.6. To contact the inductor terminals and the central-tap,

the underpasses are exploited. These are built by using the shunted lowest metal layers in order to minimize their series resistances. The design of this integrated transformer for the proposed dc-dc power converter needs a co-design procedure with the active component (i.e., oscillator core), which will be discusses in next section. As mentioned before, high coupling factor between primary and secondary coils, k_S, is mandatory for an optimized design since a low k-factor combined with the poor Q-factor of integrated transformers would highly affect the overall system efficiency. Consequently, the maximization of the overlap area between primary and secondary windings is crucial to avoid magnetic coupling factor degradation [49]. To this end, it is of utmost importance to equalize the external diameters of the secondary coils L_{S1} (L_{S2}) and the interleaved primary windings $L_{P1\text{-}3}$ ($L_{P2\text{-}4}$), by exploiting a geometrical constrains. Indeed, being such transformer topology rather complex, in interest of speed-up the design flow a novel lumped, geometrically scalable model was developed.

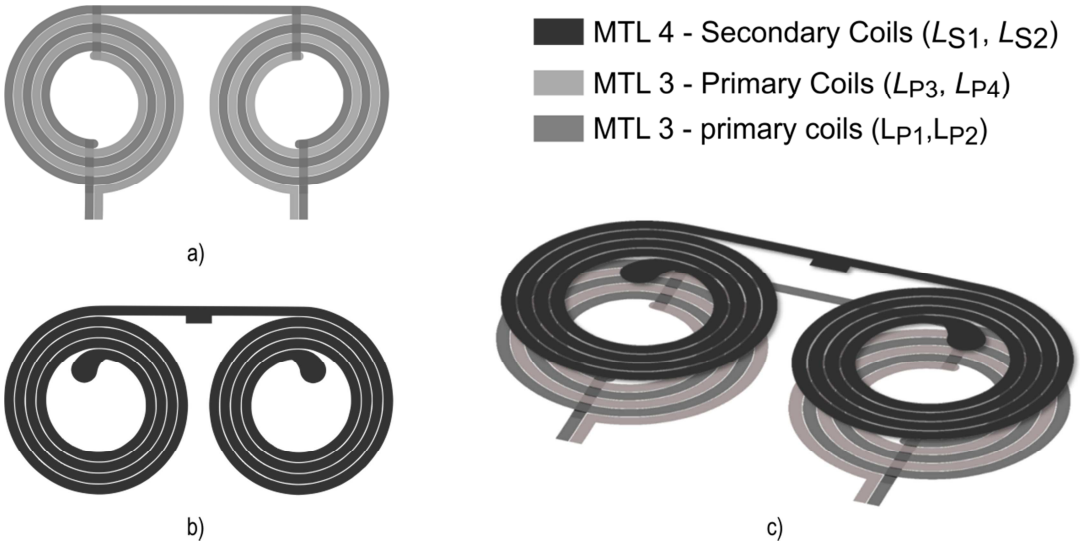

Figure 2.6 Isolation transformer. (a) Primary windings. (b) Secondary windings. (c) 3*D*-view

2.3.3.1 Lumped, geometrically scalable hybrid model

Lumped scalable modelling of integrated transformer has been a research theme since long time, and it is clear that there is no easy way to estimate the key electrical parameters of the transformer starting from geometrical parameters, while providing the required accuracy for power efficiency evaluation in a wide range of design parameters [50]. This accuracy can be obtained by using parametric EM simulations, which however imply high computational effort and long design time. In the proposed design procedure, the integrated transformer was modelled by means of the geometrically scalable lumped model shown in Fig. 2.7. As discussed in the previous section, widely adopted formulae developed for transformer-loaded discrete circuits are not useful for this application due to both complex loss and EM coupling mechanisms on silicon [51]. The displayed network models half structure (i.e., the single-ended configuration) of the transformer and consists of two *T*-like branches, each one for the interleaved spirals, and π-like branch for the staked secondary coil, respectively. In particular, the primary interleaved spirals P_1 (P_2) and P_3 (P_4) are modelled by two *T*-branches (i.e., $L_{P1,2}$ and $L_{P3,4}$) magnetically coupled by means of the magnetic factor k_P, while capacitors C_{OXP} take into account the fringing capacitive coupling.

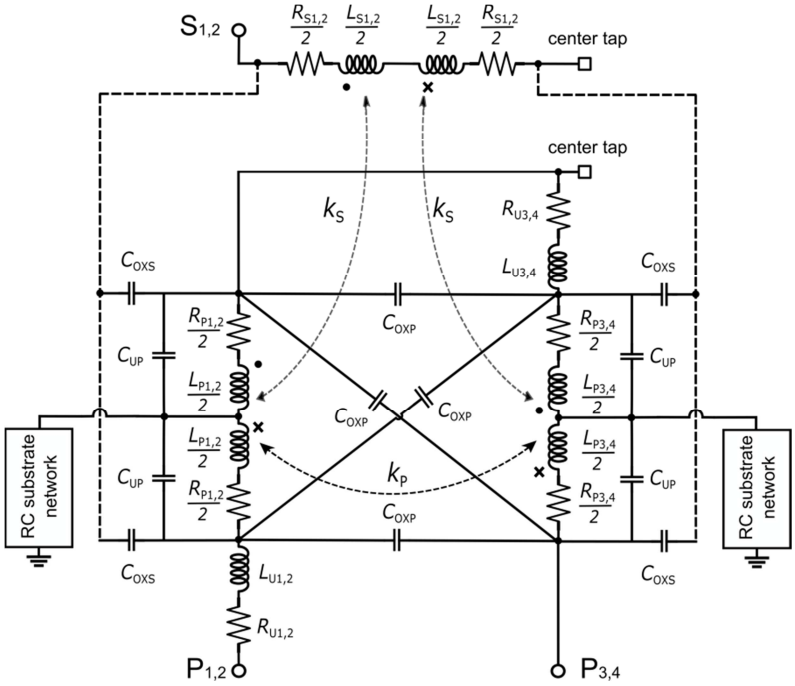

Figure 2.7 Lumped scalable model of the isolation transformer

The primary windings P_1-P_3 (P_2-P_4) are magnetically and capacitive coupled to the secondary spiral S_1 (S_2) through the magnetic coupling factors k_S and capacitors C_{OXS}, respectively. The model also allows for inductive, resistive, and capacitive contribution due the underpass connections. Finally, an *RC* network is used to model the substrate effects [52]. For small transformers the self-resonance frequency (SFR) is essentially due to capacitors C_{OXP} and C_{UP} since the oxide layer between primary and secondary coils is very thick. Of course, at the increasing of the outer diameter (D_{OUT}), primary-to-secondary winding capacitors C_{OXS} become more significant. The scalability of the model is crucial for its employments into the co-design procedure shown in Fig. 2.9. By using the geometrically scaled closed-form expressions [53], scalability is assured for a wide range of the transformer geometrical parameters. A set of integrated inductors was implemented and EM simulated in ADS Momentum. It was found that the following monomial fitting expression introduced in [54] may afford inductance values enough accurate in a wide range of geometrical parameters:

$$L = A \cdot n^b \cdot w^c \cdot D_{OUT}^d \cdot D_{AVG}^e \qquad (1.5)$$

where n, w, D_{OUT} and D_{AVG} are the number of turn, the metal width , the outer diameter and the average diameter of each transformer winding, respectively, while coefficients A, b, c, d and e are fitting parameters extracted from EM simulations. Instead to calculate the underpass inductance, L_{UP}, the well-known expression for a rectangular conductor [55] is used. Capacitor contributions arise from both area (i.e., C_{OXS} and C_{UP}) and perimeter (C_{OXP}) effects and are easily calculated whit the simplified expression for parallel-plate capacitor [49], [52], [56]. Series resistances $R_{P1,2}$ ($R_{S1,2}$) are the most important model's parameters for an accurate estimation of transformer losses. A lots of expressions available in literature were tested and none of them provided the needed accuracy. For this reason, a novel expression was proposed, that is:

$$R = R_{DC} \cdot \left(1 + \frac{\alpha \left(\frac{f}{f_{CRI}} \right)^2}{\beta \left(\frac{f}{SRF} \right)^2} \right) \cdot \frac{t}{t_{EQ}} \qquad (1.6)$$

here the R_{DC} is the dc coil resistance, α and β are the fitting factors, f_{CRI} is the critical frequency as defined in [57], which takes into consideration the crowding effects in comparison with the geometrical coil parameters, while t and t_{EQ} are the physical and the equivalent thickness of the metal layers, respectively, the latter being adopted to model the skin effect phenomena [58]. The equation is further improved thanks to a correction term based on a rough evaluation of the SRF of the coil, which is:

$$SRF \approx \frac{1}{2\pi\sqrt{LC}} \qquad (1.7)$$

where L can be the primary or the secondary inductance in Fig. 2.7 and C is the equivalent capacitance seen by this inductance. This term including the SRF was meant to account for the equivalent resistance reduction that takes place nearby the self-resonance region [59]. Finally, magnetic coupling variations are modelled by means of two monomial expressions for both k_P and k_S, whose were determined by least square fitting to EM simulated date [49].

The suggested model was properly customize for the implemented transformer (see Fig. 2.6), which was chosen to minimize the length of the bonding wires, maximize the overlap between primary and secondary windings and simplify the routing towards the power supply and the active components (i.e., oscillator core). To this end, internal and external diameters were set equal for primary and secondary coils and the number of turns was limited a half-integer number and twice of this for primary and secondary coils, respectively. Metal spacing values (s_P for the primary and s_S for the secondary windings) were the minimum available by the adopted technology for metal 3 and metal 4, respectively. As a outcome, we have three free design parameters for the transformer, i.e. primary coil inner diameter D_{INT_P}, the width, w_P, and the number of primary turns, n_P, being secondary coils parameters extracted by the following constrains:

$$\begin{cases} D_{INT\_P} = D_{INT\_S} = D_{INT} \\ w_S = \dfrac{D_{INT} + (2 \cdot n_P + 1) \cdot w_P + s_P - (2 \cdot n_S - 1) \cdot (w_P + w_S) - D_{INT}}{(2 \cdot n_S + 1)} \\ n_S = n_P + 0.5 \end{cases} \quad (1.8)$$

The coupling factor k for such transformer used in the power transfer system is very high and almost constant (e.g., 0.9) thanks to the high overlap area between primary and secondary windings compared to the oxide thickness (i.e., about three order of magnitude larger). The validity of the developed model is well demonstrated by comparison with respect to EM data of 45 geometrically scaled transformers (D_{INT} from 250 μm to 450 μm, n_P from 2.5 to 4.5, w_P from

15 μm to 75 μm). The error distributions on low-frequency inductance, maximum Q-factor, SRF and magnetic coupling factors, k_P and k_S, are reported in Fig. 2.8. The x-axis reports the magnitude of error, which is defined as the difference between EM simulation and model data. The y-axis reports the percentage of transformers that exceeds the error value at the corresponding x-axis intercept. Although the model was developed for the single-ended structure, the coupling effects are negligible if proper distance between right and left sides of the transformer is guaranteed. This model is crucial to design the integrated isolation transformer exploiting a customize co-design procedure with the active devices (i.e., oscillator core).

2.4 System design

Based on the previous analysis, a co-design procedure was developed, which takes into account the main interactions between the dc-dc converter building blocks. By starting from the definition of main system specifications, i.e., the supply voltage (V_{DD}), the dc isolated output power (P_{OUT}), and the dc output voltage (V_{OUT}), the target is to maximize the dc-ac conversion efficiency, at given power density, which implicates an optimum co-design between power transistors and isolation transformer in the oscillator. Then to optimize the power/efficiency performance of the whole dc-dc isolated converter the maximization of the rectifier efficiency is required. By using the abovementioned isolation transformer model, different feasible design configurations for the whole dc-dc converter were found by properly exploring the design space.

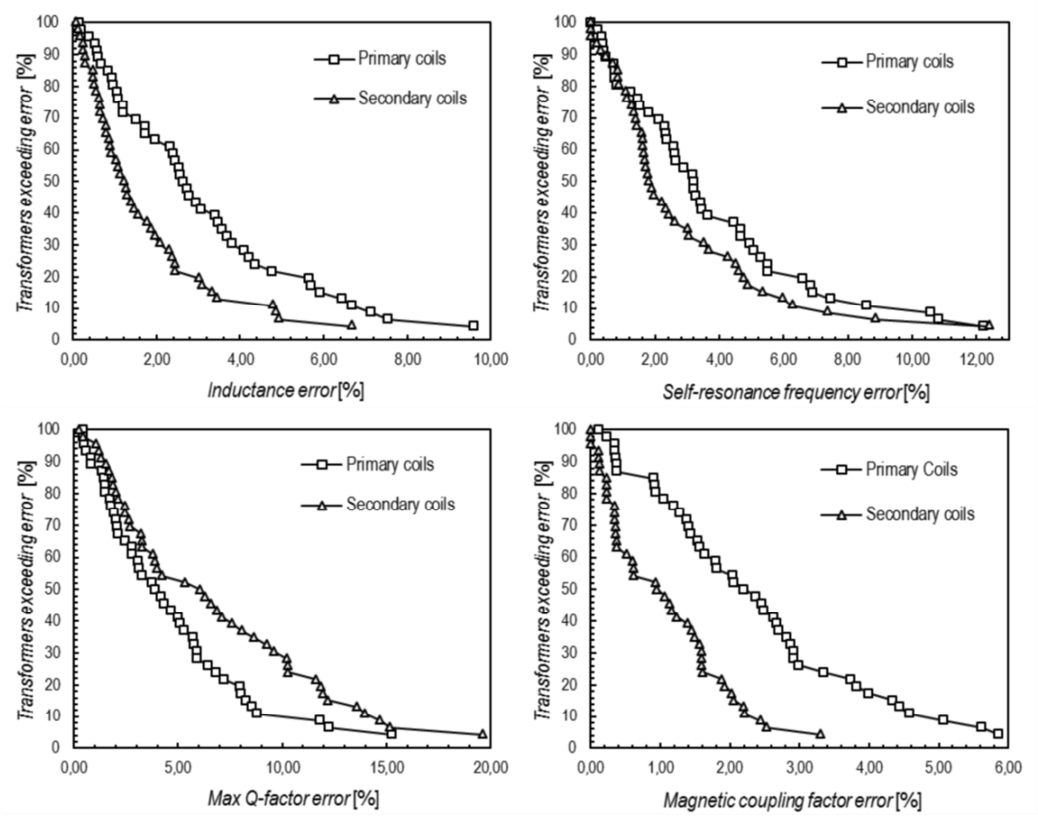

Figure 2.8 Error distributions of the geometrically scalable lumped model

These solutions were refined by iterating the design procedure and using electromagnetic (EM) simulations for the isolation transformer only to check the best results. Lastly, beginning from the best solutions, the system design was completed for integration by also includes main EM and layout parasitic effects.

2.4.1 Co-design procedure and expected results

Firstly, we recall main design parameters of a dc-dc isolated converter. As discussed in the previous section the rectifier design parameter is its multiplicity M_{NMOS}, while only three geometrical parameters characterize the isolation transformer (i.e., D_{INT}, w_P and n_P) thanks the constrains defined in Eq. 1.8. Instead, the oscillator design parameters are the size of the nMOS transistors, W_{NMOS} being $W_{\mathrm{PMOS}}=3\cdot W_{\mathrm{NMOS}}$, the size of the coupling capacitors C_{B} and the biasing voltage V_{B} which are linked to the peak drain voltage by the

voltage $V_{GS,\,MAX}$. The latter can be defined a-priori as the biasing voltage which maximize the g_m/I_D ratio, thus offering the best trade-off between dc losses and trans-conductance for oscillator start-up. The value of C_B is chosen to avoid the gate-oxide breakdown of the transistor while guaranteeing the $V_{GS,MAX}$.

The starting point of the proposed co-design procedure is the definition of main system specifications, i.e., the supply voltage (V_{DD}), the dc isolated output power (P_{OUT}), and the dc output voltage (V_{OUT}) along with the rectifier efficiency (η_{RECT}) and equivalent input impedance (Z_{RECT}), as shown in Fig. 2.9.

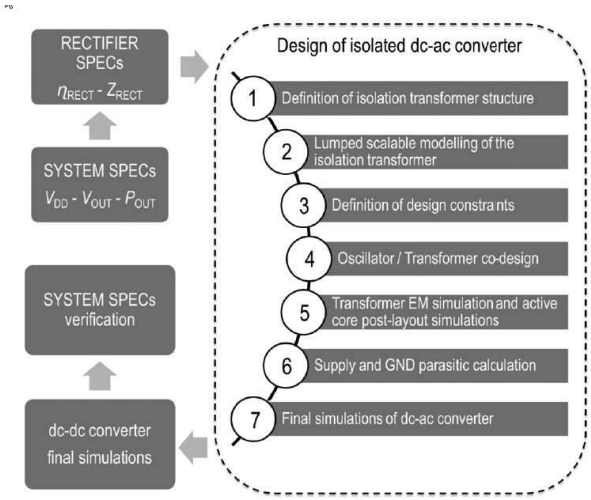

Figure 2.9 Simplified scheme of the design flow

As mentioned before, the key element of the adopted power oscillator topology is the three winding transformer, which performs both oscillator coupling and output power combining. Therefore, the first step of the design procedure is the definition of the transformer physical structure, which has to be compliant with the proposed topology adopted (as shown in Fig. 2.4). Given the transformer structure, 2D EM simulations are exploited to extract a lumped geometrically scalable model as described in previous section. The availability of such model is crucial to enable co-design of the oscillator active core along with the isolation transformer in a simple circuit simulation environment, thus avoiding complex and time-consuming mixed circuit/EM simulations. The co-design is

carried out by optimizing both transistor size and geometrical parameters of the transformer to obtain maximum efficiency at a given output power. Several constrains have to be considered during design optimization, which link the design parameters and/or limit their useful range. Specifically, the required output voltage step-up sets the transformer ratio and the average current in the oscillator imposes a bound to the minimum width of transformer spirals to comply with electro-migration rules. Moreover, the oscillation frequency (f_{OSC}) is kept below the limit imposed by the rectifier (i.e., around 400 MHz) to avoid excessive performance degradation in the ac-dc conversion. By fixing the outer diameter of the isolation transformer, D_{OUT}, a maximum area constrain is adopted, thus mainly determining the overall chip area. The result of the co-design procedure is the definition of both oscillator active core and equivalent transformer load. Of course, an accurate estimation of the dc-ac converter performance requires the adoption of further simulations according to bullets 5 and 6. As analysed in the previous section, the physical layout of the isolation transformer is modelled by means of a 2D EM simulation, while post-layout simulations (PLS) are carried out to extract the *RC* parasitic due to active device connections. The last step is the evaluation of both power supply and ground parasitic, which come from on-chip contributions and bonding wire connections. Finally, simulations of the complete dc-dc isolated converter are carried out to verify the fulfilment of system specs. This design flow requires a few iteration steps to fulfil the required performance. Main impact on system efficiency is ascribed to the integrated transformer and therefore its geometry optimization is crucial. A high magnetic coupling ($k_S > 0.8$) is achieved while the bottleneck is represented by the winding metal losses, which affect the *Q*-factors and hence the equivalent parallel resistance at the primary side, $R_P \cong \omega \cdot Q \cdot L_P \cdot (1 + k_P) \cdot (1 + k_S^2)$ [51]. Indeed, a portion of the ac power is dissipated on R_P instead of being transferred at the transformer secondary side towards the rectifier. The maximization of R_P mainly involves the exploitation of high inductance values, while preventing the oscillation frequency, f_{OSC}, from an excessive reduction. To this aim, additional parallel capacitances (i.e., $C_{P1,2}$ in Fig. 2.4) are avoided, thus exploiting for the *LC* resonance only the

parasitic capacitive contributions due to the active core. On the other hand, the low limit for the capacitive parasitic of the active core is mainly determined by the minimum width (W_{NMOS}) that guarantees the required output power. By taking advantage of the model described in previous section, a transformer-loaded oscillator for the proposed dc-dc power converter was designed, and its design values along with the geometrical parameters of the isolation transformer (T_{ISO}) are summarized in Table 2.2.

Table 2.2 Design parameters of the power oscillator and the isolation transformer

Block	Parameter	Value	Unit
Oscillator Core	$W_{1,2}$	1.08	[mm]
	$W_{3,4}$	3.24	[mm]
	$L_{1,2,3,4}$	0.35	[μm]
	C_B	5	[pF]
	V_B	1.2	[V]
Isolation Transformer	w_P | w_S	38 | 40	[μm]
	s_P | s_S	1 | 5	[μm]
	D_{INT}	370	[μm]
	n_P | n_S	2.5 | 4	turns
	L_P ; L_S	5; 12,5 @ f_{OSC}	[nH]
	Q_P ; Q_S	3.5; 7 @ f_{OSC}	
	k_P ; k_S	0.55; 0.85	

The nominal oscillation frequency has an average value of 330 MHz being a trade-off between the conversion efficiency of the rectifier and the transformer performance. In order to deliver an output power around 30 mW that is compliant with the isolated low-power applications, the transformer ratio, $N = \sqrt{\frac{L_S}{L_P}}$, was set to 2.5. The simulations are carried out at V_{DD} = 3 V achieving an efficiency of the integrated transformer $\eta_{TISO} = 55\ \%$ and an efficiency of the oscillator core $\eta_{CORE} = 30.6\ \%$.

The analysis and the design of this dc-dc isolated power converter is mandatory to develop a system able to transfer both power and bidirectional data exploiting a single inductive channel in order to minimize the silicon area, reduce both costs and complexity, as it will be discussed in the next chapter.

Chapter III

A fully integrated 40-Mbps/23-mW data/power transfer system

An integrated isolator providing both data and power transfer could extremely useful in wide range of applications, especially in low-power design. Being isolated sensor interfaces the main target of such a system, the key parameters are the bit rate from the isolated side, i.e. the downstream data link, the available isolated supply current, I_{OUT}, and the power efficiency. Data rate in a range of tens to hundreds of megabit per second are needed to guarantee sufficient bandwidth and/or oversampling for autonomous sensors. Although low-frequency signals must be measured, this high bandwidth can prove useful when cyclic redundancy check (CRC) codes and data communication protocols are taken into account, or when high signal-to-noise ratio (SNR) is demanded for a ΣΔ modulator, for example. Further to the output current, the cascaded sensor can benefit from scaled technologies to improve speed and costs. This means that a relatively low output voltage is not a problem, whereas the absolute value of available output current plays a key role, being the current consumption directly related to speed and noise performance of mixed-signal circuitry. Thanks to the lower output power levels, the power efficiency is not a bottleneck for these systems [60]. An additional useful feature required to this systems is the availability of a second data link, i.e. from the primary side to the isolated side, thus implementing a half-duplex bidirectional data communication. Such a link can be extremely useful when configuration data stream must be send to the isolated side, thus allowing a system setting or testing for example.

This chapter describes the design and the implementation of a data/power transfer system by exploiting a single isolation transformer. A high data stream

with maximum data rate up to 40 Mbit/s and an output current higher than 10 mA were chosen like main system specifications to be achieved. Taking into account the dropout voltage of a series regulator, the output voltage of the system, V_{OUT}, should be higher than 1.5 V if a supply voltage around 1.2 V is required for the autonomous sensor.

3.1 System description

The simplified block diagram of the proposed data and power transfer system is shown in Fig. 3.1. Differently from the state of the art, this architecture exploits a single isolation transformer for both high efficiency power transfer and bidirectional data communication. Thanks to this innovative aspect a high integration level can be achieved, thus reducing both cost and complexity. The basic idea of this system was also included in a US patent [61].

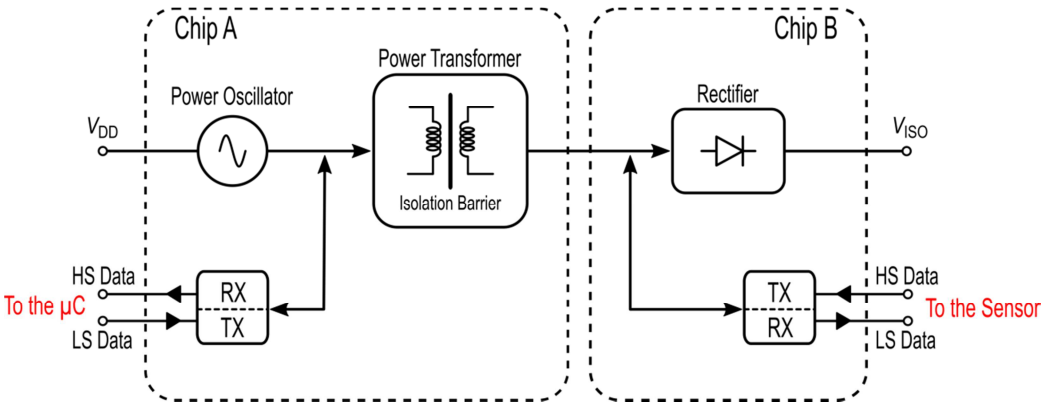

Figure 3.1 Proposed architecture for isolated data/power transfer system

The adopted implementation of the system with a transistor-level of the power link is depicted in Fig. 3.2. It is made up of two dice, A and B which were fabricated in 0.35-μm BCD-SOI technology providing on-chip galvanic isolation. Die A includes a power oscillator, an isolation transformer, a LS ASK modulator, and a HS demodulator, whereas die B houses a full-bridge rectifier, a LS ASK demodulator, and a HS ASK modulator. In addition to the power link described in

the chap 2, this system also includes the RX/TX blocks that perform the half-duplex bidirectional data communication. The isolated output power is delivered from die A to die B across the galvanic isolation barrier thanks to a dedicated power link. In particular, the power oscillator performs the dc-ac power conversion by exploiting a current-reuse technique, thus sharing the same supply current in order to maximize the power efficiency at given output power level. The integrated transformer, T_{ISO}, is a key block of the power chain providing both oscillators coupling and output power combining, while the rectifier provides the ac-dc power conversion. For this system the supply voltage was set to 3 V to comply with typical micro-controller voltages, thus using a 0.35-μm/3-V devices for both the oscillator and the communication circuitry. Instead, for the sake of robustness the rectifier exploits 0.8-μm/5-V devices, since the output voltage at the secondary coils of the isolation transformer is higher than 4 V, as depicted by the simulated waveforms in Fig. 3.3.

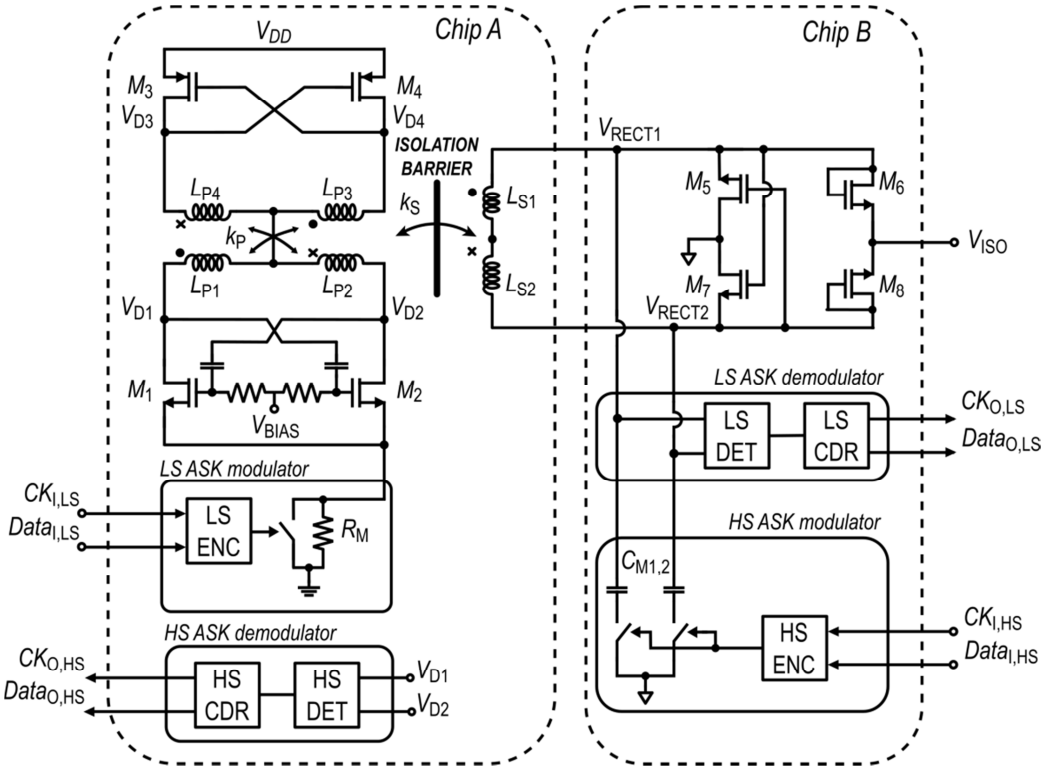

Figure 3.2 Simplified schematic of the isolated data/power transfer system

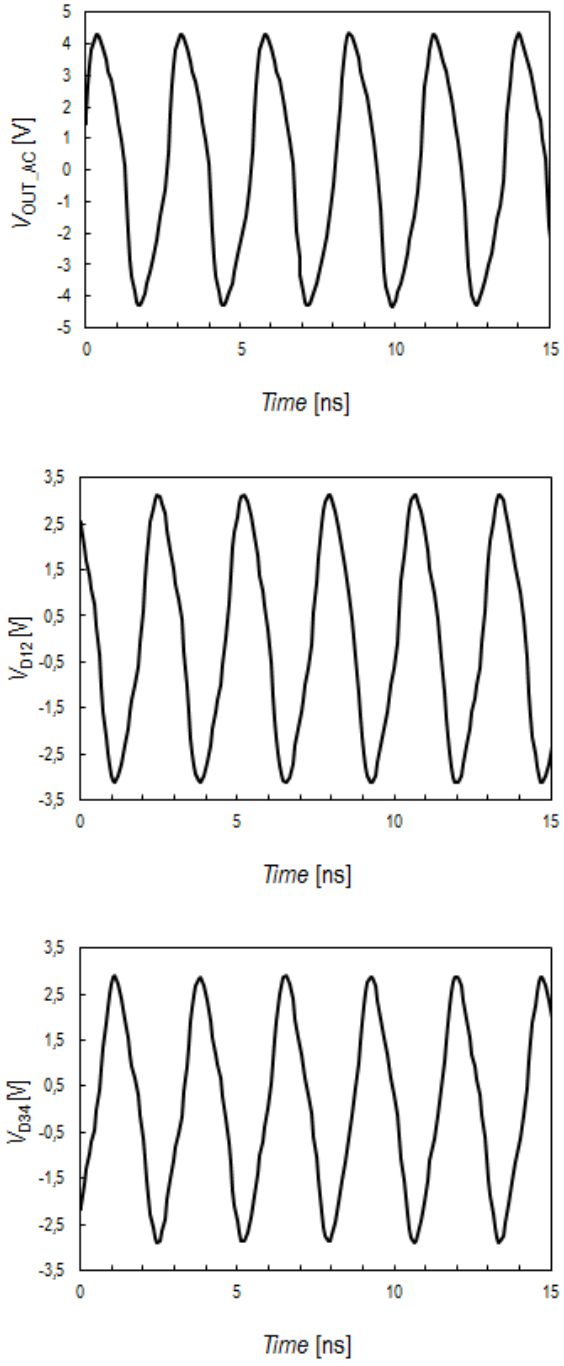

Figure 3.3 Simulated voltage waveforms of the transformer-coupled oscillator

3.2 Data modulation

In order to perform the half-duplex data communication an ASK modulation at the coils of the isolation transformer was performed. It is characterized by the modulation index *h*, which is defined like:

$$h = \frac{A_{MAX} - A_{MIN}}{A_{MAX}} \qquad (1.9)$$

where A_{MAX} and A_{MIN} are the maximum and the minimum amplitudes of the RF power signal. In the following, we denote with HS the signals and circuitry related to the main data communication from isolated die while with LS the signals and circuitry linked to the slower communication, used for example to transfer configuration data.

HS modulation is carried out by means of impedance mismatch at secondary winding of the isolation transformer by exploiting the capacitors $C_{M1,2}$ and the linked switch resistances. On the other hand, the LS data modulation is performed by switching the series resistor, R_S, toward the oscillator ground, thus reducing the current and hence the oscillation levels of the power oscillator. Due to the use of a single isolation transformer for both data and power transfer a lowest h_{HS} is mandatory to preserve the system power efficiency. To this end, the HS data communication adopts a $h_{HS} \cong 5\%$, while a deeper modulation index, i.e., $h_{LS} \cong 25\%$ was chosen at the same time for LS data communication guaranteeing a safe data transfer.

3.2.1 Pulse-with modulation coding

By using the RF power carrier to transfer also data a simply coding was adopted, which allows to easy recover both data and clock signals. To this end two encoding blocks, HS_ENC and LS_ENC, perform pulse-with modulation (PWM) coding of the bit stream before the ASK modulators. Similarly, clock and data recovery of the HS and LS data communication is carried out by two

decoding blocks, HS_CDR and LS_CDR, connected down-line of the respective ASK detectors.

Further to the coding scheme, the length of the bit, T_{BIT}, is kept constant, with the $T_{BIT} = 1/R$ and R is the corresponding HS/LS bit rate, while the bit value is coded by means of the duration of the high level of the envelope, as shown in Fig. 3.4 (a). The HS and LS encoders, are simple digital blocks that use an 8x oversampling clock reference to encode the PWM streams. In particular, this clock reference drives a digital counter whose outputs implement the coding by using logic gates.

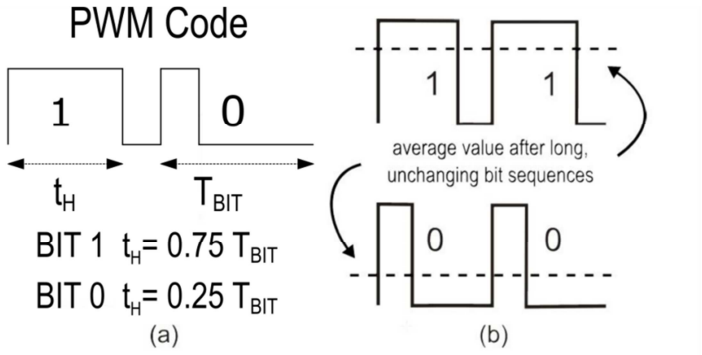

Figure 3.4 PWM coding scheme adopted (a). Degradation of the detector's noise margin due to long sequences of ones or zeroes (b)

Although such a coding scheme has been chosen to the straightforward implementation of clack and data extraction circuitry, it influences the complexity of the ASK detectors. In fact, the bit symbols in PWM have different average value, hence long sequences of one or zeroes shift the average value towards opposite values of the envelop signal, thus reducing the noise margin of the detectors, as shown in Fig. 3.4 (b). High sensitivity and gain are required to achieve very steep rising/falling edges, which is mandatory to minimize the error due to shifts of the average value. System level simulations show that at least the third harmonic of the envelope signal must be preserved to avoid significant performance degradation of the adopted CDR decoding blocks. Consequently, the

design of the ASK detectors becomes one of the central parts of the proposed system.

3.3 High sensitivity and low power ASK detectors

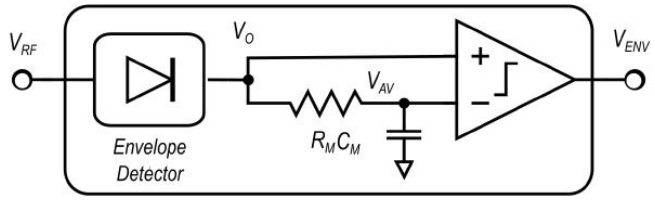

Figure 3.5 Standard architecture of an ASK detector

The common ASK-detector architecture is made up of an envelope detector (ED), followed by a low-pass filter, and a comparator, as depicted in Fig. 3.5. V_{RF} is the RF ASK-modulated input signal. By using the low-pass filter $R_M C_M$ the produced average signal is compared with the actual envelop signal V_O by the comparator, thus providing the rail-to-rail digital signal, V_{ENV}. The comparator is often characterized by a finite gain, offset voltage and limited common-mode input swing, thus affecting the detector sensitivity defined as the minimum envelope variation able to provide a useful V_O. In particular, the envelop detector can be implemented by using passive or active non-linear circuits. A simple topology is based on a diode rectifier as shown in Fig. 3.6 (a) [62]. By only exploiting a passive components it does not require a bias current but suffers from low input impedance and poor sensitivity. Instead common active circuits adopt a common-drain (CD) configuration as depicted in Fig. 3.6 (b) [63]. They are simple and characterized by high input impedance, controlled current consumption, and good input swing but they have a conversion

gain lower than one. Moreover, its output impedance is quite low, thus involving a low signal amplitude and hence a low signal-to-noise ratio [64].

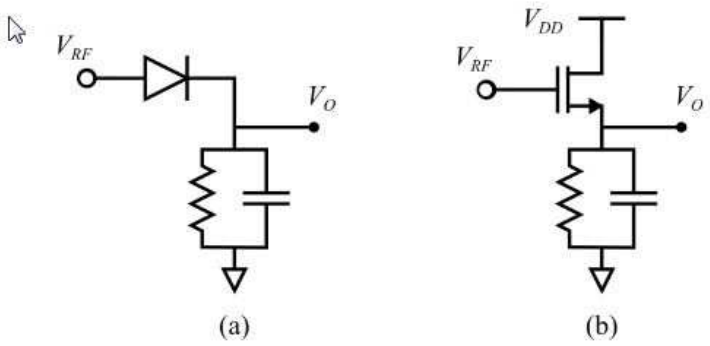

Figure 3.6 Passive (a) and common-drain topologies for the envelope detector (b)

The ASK detector adopted is connected at nMOS oscillator drains of $M_{1,2}$, as shown in Fig. 3.2. To better understand the trade-offs and the design issues Fig. 3.7 shows its typical input signal.

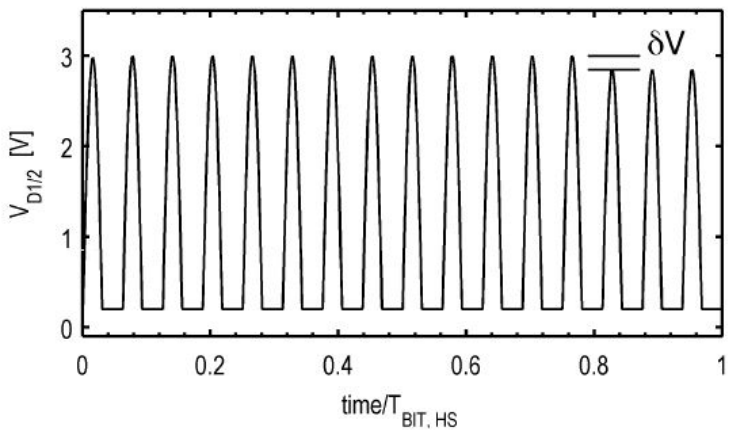

Figure 3.7 Typical (ideal) time domain waveform of the modulated signal at the NMOS oscillator $V_{D1/2}$ (see Fig. 3.2)

Specifically, the Fig. 3.7 shows the typical voltage waveform of the PWM-coded, ASK-modulated signal at the drains of $M_{1,2}$ for one HS bit period, $T_{BIT,HS}$. Ideally, the signal remains quite low for half RF period, to increase the

power efficiency when the transistors $M_{1,2}$ are active and has a sinusoidal shape for the other half RF period, when the oscillator transistors $M_{1,2}$ are switched-off. When the HS data communication is switched-on in order to preserve the power efficiency of the system a very low modulation index h_{HS} is adopted. It determines an envelope signal around 150 mV over 2.8 V_{PP}. Indeed, the RF carrier frequency was set to 330 MHz, hence the maximum bit rate being around $R_{HS,MAX} = 40\ Mbit/s$ is 8x lower. The modulated signal is down-converted by the even order non-linearity of the envelope detector, and hence another main issue is represented by its high-level of uncertain. In the following, we can see the signal's shape in the operating system due to the high variability of rectifier input impedance and oscillator waveforms with respect to parasitic, process variations and output voltage. On the other hand, it is well known that the conversion gain of envelope detectors also depends on the shape of the RF carrier, thus complicating system design. Although CD based detectors may perform well in the proposed system, two novel topologies were instead preferred for the sake of robustness.

3.3.1 Common source ASK detector with adaptive biasing

The most interesting solution of envelope detector characterized by high sensitivity and low power consumption is the common-source (CS) configuration which is shown in Fig. 3.8 (a). For large signal, it produces an addition dc drain current proportional to the even powers of the RF input signal by exploiting the non-linearity of the transistor M_0. This circuit can operate as active envelope detector if the RC load is designed to cut-off the RF frequency while allowing the RF envelope signal. Indeed, this topology having high input and output impedances can perform high conversion gain but its average current consumption is highly affect by supply voltage, temperature (PVT) and process variations. This drawback can produce envelope distortion, high power consumption, and output saturation, since high uncontrolled gain can force the output node to ground when PVT tolerances are considered. Especially for low-*h* ASK modulation it must be

dealt with because A_{MAX} and A_{MIN} are closely spaced and their difference can reach the order of the transistor's threshold voltage tolerance.

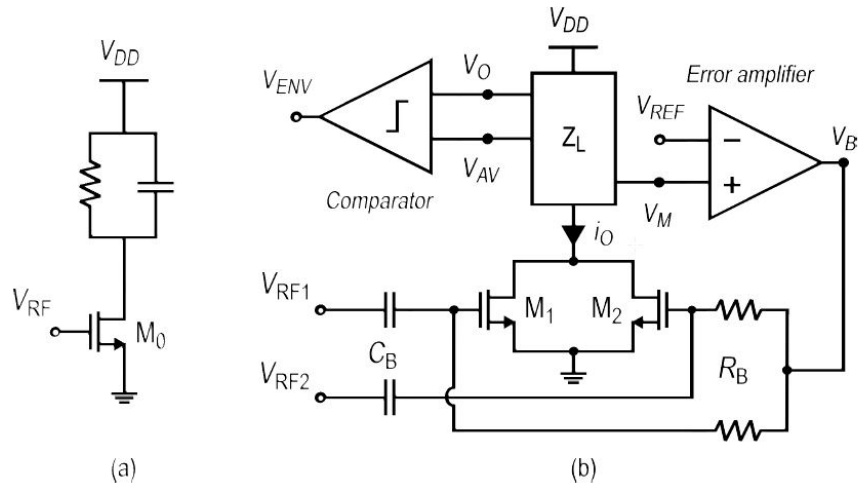

Figure 3.8 (a) Tradition common-source envelope detector. (b) Novel common-source ASK detector with adaptive biasing

Recently, a novel high-sensitivity ASK detector architecture based on common-source configuration has been conceived [65]. Differently from previous topologies it exploits an adaptive biasing technique to avoid the above-mentioned limitation of the SC ED topologies, thus allowing high sensitivity with low power consumption. Its simplified schematic is shown in Fig. 3.8 (b) for a full-wave input stage. The most important feature of this novel topology is the closed-loop able to control the average output voltage of the common source stage and hence its average output current. In particular, the circuit is made up of a CS ED including a feedback loop with an error amplifier and a comparator. The RF differential input, $V_{RF1,2}$, is ac-coupled to the detector through the high-pass filter C_BR_B. The output current of the input pair, i_O, is a non-linear function of both V_{RF} and V_B. It flows into a load network, Z_L, producing three output signals that are the envelope signal, V_O, its average voltage, V_{AV}, and a voltage proportional to the average voltage, V_M. The feedback loop houses the envelope detector and the error amplifier fixing the voltage V_M to the value of the reference voltage V_{REF}

while defining the RF input bias voltage, V_B. Differently from the open-loop CS detector this novel configuration provides several advantages such as:

- High conversion gain which is quite constant for low modulation index
- Controlled power consumption
- Robustness against PVT tolerances

As a consequence, it has been chosen for both HS and LS detectors to satisfy the required sensitivity while guaranteeing system functionality in a wide range of operating conditions.

3.3.2 HS ASK detector

Main issues of the high speed ASK detector are the strong RF harmonics and the low modulation index. To this end, the high output impedance of the CS detectors can be usefully to simplify filtering and amplification of the envelope signal. A simplified schematic of the implemented HS detector is shown in Fig. 3.9.

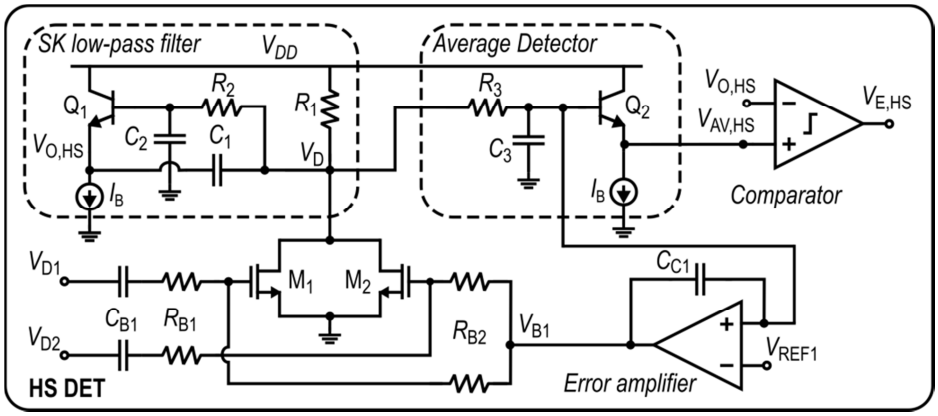

Figure 3.9 Simplified schematic of the HS ASK detector

The differential input ($V_{D1,2}$) is ac-coupled by using the capacitors C_{B1} while halving through a resistive partition made up of $R_{B1\text{-}2}$. In order to implement a wide-band current-to-voltage conversion at the drains of $M_{1,2}$ a simple load

resistor was adopted. However, due to the high RF components at this node, a current-mode Sallen-Key low-pass filter including resistors $R_{1,2}$, capacitors $C_{1,2}$ and the bipolar transistor Q_1, was used. This filter performs a second-order transfer-function having a 90 MHz cut-off frequency in order to filter the RF components, while preserving the envelope signal components. Current-mode signal processing is enabled by the high output impedance of the input stage. The detector is completed by a replica path comprising C_3, R_3 along with a Q_2 which performs the average value of the envelope signal $V_{AV,HS}$ for the HS comparator. It consists of two resistively-loaded differential pairs followed by a differential-to-single-ended converter. The first stage takes advantage of a bipolar input pair to minimize the voltage offset. At the output of the SK filter the signal swing is low enough to avoid IP2 issues for the first stages, whereas its envelope component is high enough to overcome the input-referred voltage offset. The simple low-pass characteristic of the two amplification stages easily provides a few dB of attenuation which is required to completely suppress the RF signal before the differential-to-single-ended converter. Therefore, it compares $V_{AV,HS}$ with the output of the low-pass filter, $V_{O,HS}$, to achieve the rail-to-rail envelope signal $V_{E,HS}$ required for the digital decoder. Therefore, the average signal at the base of Q_2 is also the input of the error amplifier whose output sets the bias voltage V_{B1} of the input pair, thus closing the adaptive biasing loop. In fact, thanks to the error amplifier the voltage across R_1 is set at value of the reference voltage V_{REF1}, thus well controlling the average current in $M_{1,2}$ to ensure the PVT accuracy for the system. The design parameters and the main simulated performances are summarized in the following Table 3.1.

Table 3.1 Summarized design parameters and simulated performance of the HS ASK detector

Parameters	*Values*	*Unit*
R_1	18	[$k\Omega$]
$R_{2,3}$	41	[$k\Omega$]
$R_{B1,2}$	7	[$k\Omega$]
C_1	40	[fF]
C_2	20	[fF]
$C_{3,C}$	7,5	[pF]
C_B	1	[pF]
I_B	25	[μA]
$W_{1,2}$	16	[μm]
$L_{1,2}$	0,75	[μm]
G_C @ hHS=5%	4	[dB]
I_{DD}	250	[μA]
Silicon Area	0,054	[mm^2]

3.3.3 LS ASK detector

Differently from the HS detector, the LS one has to manage much lower envelope frequencies, which were conceived in the Mbps range. In particular, the upstream data rate is picked out of about 1 Mbps, thus easy filtering the RF components. On the other hand, different issues such as current consumption, lower supply voltage, (i.e., the isolated output voltage V_{OUT}) and size of the compensation capacitor are come up. In fact, due to the low power efficiency system a very low current consumption of the LS ASK detector is required. To this end, it would be easy increase the load resistance of the input pair but due to the low-voltage available and the small area, a totally different topology, as shown in Fig. 3.10, was adopted.

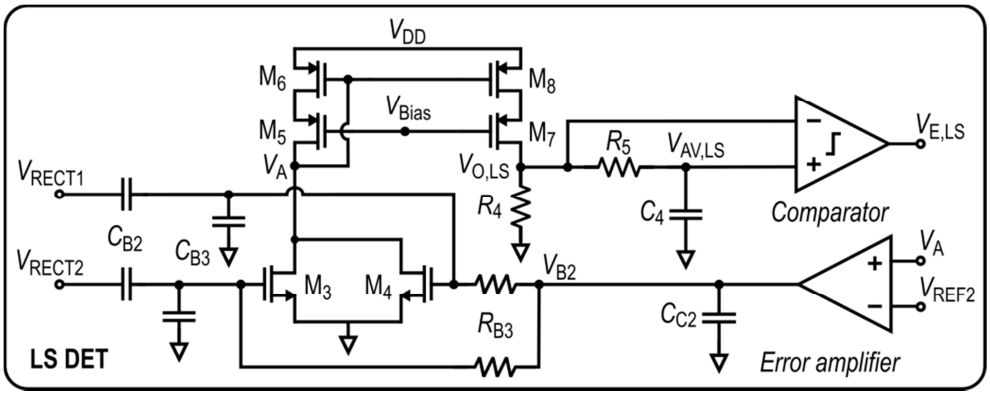

Figure 3.10 Simplified schematic of the LS ASK detector

The voltage at the rectifier input can be much higher than the supply voltage, e.g. 4 V_{PK} due to the voltage droop on the rectifying devices, hence a capacitive partition was chosen to reduce the input voltage while allowing the ac-coupling. It is made up of capacitors $C_{B2,3}$ and performs a 4x partition while minimizing the resistive loading at the input stage. To deal with the low output voltage without compromising the output node dynamic, a low-voltage mirror cascade topology was adopted. It consists of the transistors $M_{5\text{-}8}$ and provides copy and mirror of the output current $i_{O,LS}$ while performing a 5x current gain. With the aim of achieve the current-to-voltage conversion at the output node, $V_{O,LS}$, a high resistive load, R_4, was adopted. The low-pass filter R_5C_4 is used to recover the average voltage, $V_{AV,LS}$, for the LS comparator, whereas the feedback signal for the error amplifier, $V_{M,LS}$, was taken at the low-impedance gate of M_6 to bypass time-constant C_4R_5 and make possible dominant-pole compensation. Indeed, it is evident that the pole of the average detector $C_4 R_5$ is outside the loop gain path, thus increasing the robustness of the topology and its area efficiency with respect to the HS detector. Main design parameters of the LS detector are reported in Table 3.2.

Table 3.2 Summarized design parameters and simulated performance of the LS ASK detector

Parameters	*Values*	*Unit*
R_1	18	[$k\Omega$]
$R_{2,3}$	41	[$k\Omega$
$R_{B1,2}$	7	[$k\Omega$]
C_1	40	[fF]
C_2	20	[fF]
$C_{3,C}$	7,5	[pF]
C_B	1	[pF]
I_B	25	[μA]
$W_{1,2}$	16	[μm]
$L_{1,2}$	0,75	[μm]
G_C @ h_{HS}=5%	4	[dB]
I_{DD}	250	[μA]
Silicon Area	0,054	[mm^2]

3.4 Measurements results

This section reports the measured results of the proposed isolated dc-dc power converter with half-duplex bidirectional data communication. Firstly, the complete system was assembled on an evaluation board, as shown in Fig. 3.11. Here the secondary coils of the isolation transformer are directly connected to the rectifier input pads thanks to two bonding wires.

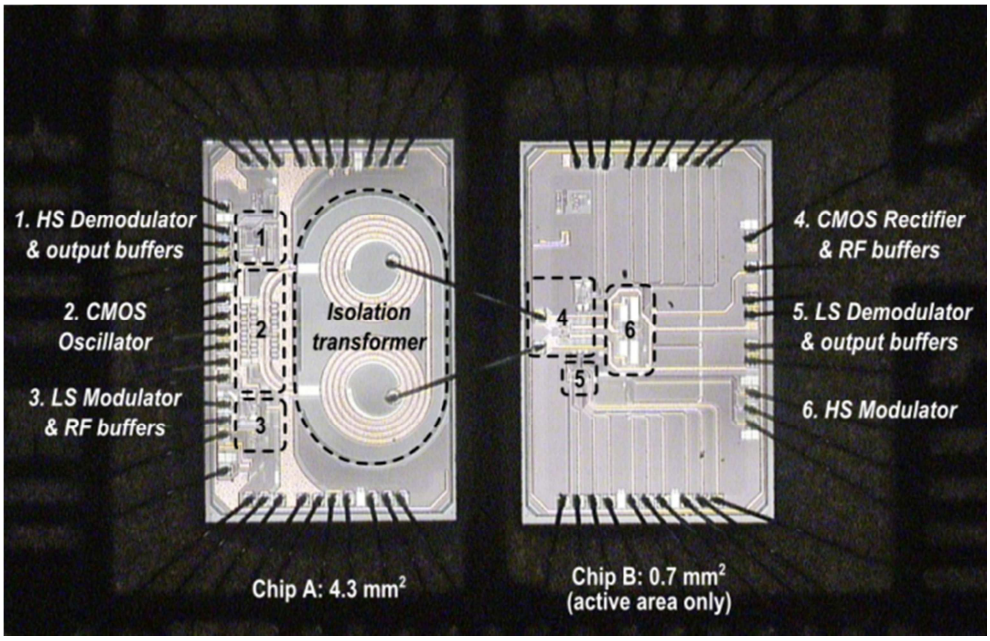

Figure 3.11 Micrograph of the overall system assembled on board

The rectifier die (chip B) has the same size of the chip A being pad-limited due to the high number of the internal signals, which were taken off-chip for monitoring and configuration. The experimental characterization of the system was carried out at different supply and output voltages showing sufficient output current to power up a wide range of isolated sensors. At first, the converter was characterized at increasing dc output voltage, V_{OUT}, by means of a semiconductor parameter analyser, for supply voltages of 3 V ± 5 % and 3.3 V ± 5 %. Then, the performance of the bidirectional data transfer was assessed by bit error rate (BER) measurements.

3.4.1 DC-DC power converter

Figs. 3.12 and 3.13 depict the measurements of the available output power, P_{OUT}, and power efficiency, η, as a function of the output voltage, V_{OUT}, with and without data communication at different supply voltages. It is apparent that the output power does not significantly change with respect to V_{OUT}. At nominal supply voltage V_{DD}= 3V, the maximum output power P_{OUT} of 23.7 mW

at V_{OUT}= 2V was achieved without data link. In all measurement range the output power changes by less than 4 mW. Its value reduces by less than 5 mW if the HS data link is switched-on, thanks to a HS modulation index (h_{HS}) as low as 5 %. Instead, when the LS data link is active, the output power lowers by around 9 mW, mainly due to the higher LS modulation index (h_{LS}=26 %) adopted.

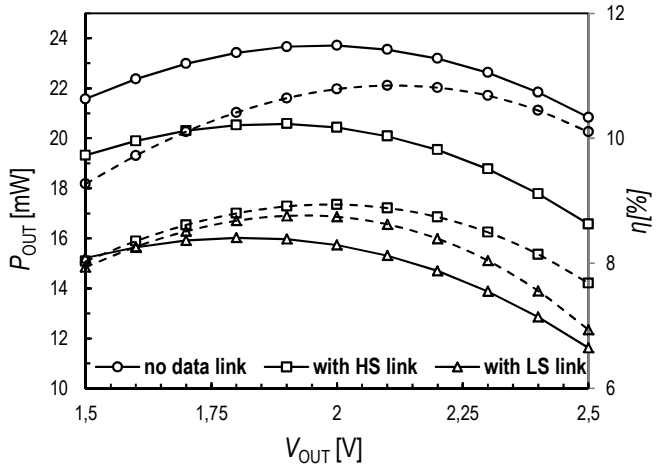

Figure 3.12 Output power, P_{OUT}, and power efficiency, η, as a function of the output voltage V_{OUT} @ supply voltage V_{DD}= 3V

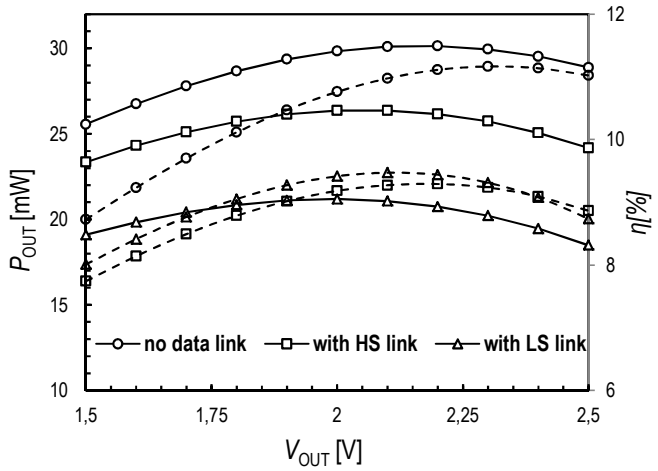

Figure 3.13 Output power, P_{OUT}, and power efficiency, η, as a function of the output voltage V_{OUT} @ supply voltage V_{DD}= 3.3V

At V_{DD}= 3.3V the maximum available output power of 30 mW without data communication was achieved, which is around 26 % higher than the maximum P_{OUT} at the nominal power supply (V_{DD}= 3V). Measurements have confirmed that at V_{OUT} of 3V the proposed system is able to deliver a dc available output power compliant with a wide range of isolated sensors.

3.4.2 Data measurements setup

Due to the lack of proper instrumentation for BER measurements, a customized arrangement was fined-tune to estimate the BER of the two implemented data links. This is typically measured in term of highest bit-rate that the system is able to process while providing a BER lower than 10^{-3}. Fig. 3.14 illustrates the physical setup for BER measurements. When the HS or the LS data link is active, the system requires two correlated signals, here shown as $Data_{IN}$ and CK_{IN}, representing the input data and the respective clock signal for synchronous communication. They were generated by using the in-phase and in-quadrature baseband signals of an Agilent E4438C ESG vector signal generator (VSG), i.e. I_{OUT} and Q_{OUT} respectively. Each data communication is performed by the HS/LS_ENC which use a PWM coding requiring two 8x oversampling references clocks, CK_{REF}. They were provided by Agilent 81160A and an Agilent N5171B signal generators. Finally, a digital sampling oscilloscope, Agilent MSO9104A, was connected to the demodulated data and clock recovery outputs of the HS/LS CDR block, here shown as $Data_{OUT}$ and CK_{OUT}, through a digital input active probe. It also acquires the input signals $Data_{IN}$ and CK_{IN}. All the measurement instruments were connected to a PC with Labview for automated measurement through a GPIB bus and a GPIB to Ethernet adapter. Input and output voltages for the two chips were forced and measured during measurements, respectively, with an HP 4156C semiconductor parameter analyser. A customized LabView software was adopted to provide the BER measurements. The simplified flow-chart diagram of the measurements system software is shown in Fig. 3.15. Due to the limited speed of the GPIB as well as limited memory buffers of both

Ethernet adapter and oscilloscope, BER measurements were performed in discrete steps. Firstly, a random bit vector, B, is generated and split in smaller vectors, whose size M depends on the bit rate, and on the oscilloscope memory buffer, as well as on is sampling frequency.

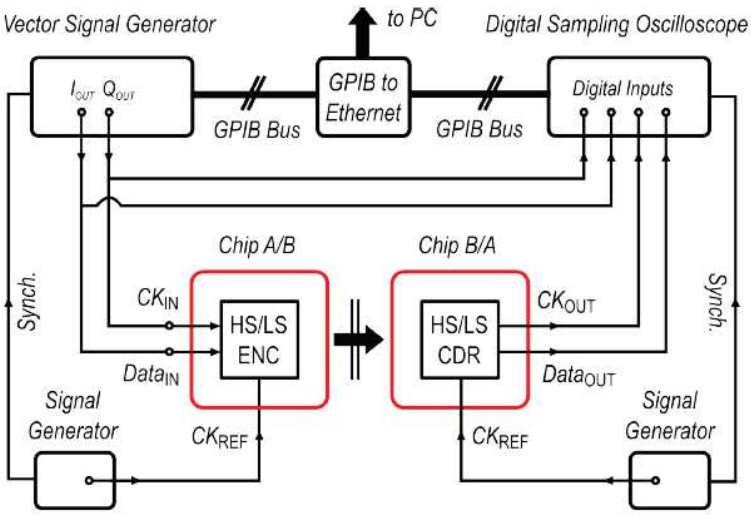

Figure 3.14 Simplified description of the BER measurement setup

Then the vector signal generator is programmed to provide $Data_{IN}$ and CK_{IN} signals to the first chip and the oscilloscope start sampling the digital inputs. After the memory buffer of the oscilloscope is filled data are transferred to LabView for a post-processing where $Data_{IN/OUT}$ signals are sampled in correspondence of the respective $CK_{IN/OUT}$ signals to recover two digital bitstream. Finally the input and output bit-streams are compared: bit errors are counted and stored and the measurement starts again until enough bits or errors are counted. Tests were generally performed to measure at least 10^5 bits.

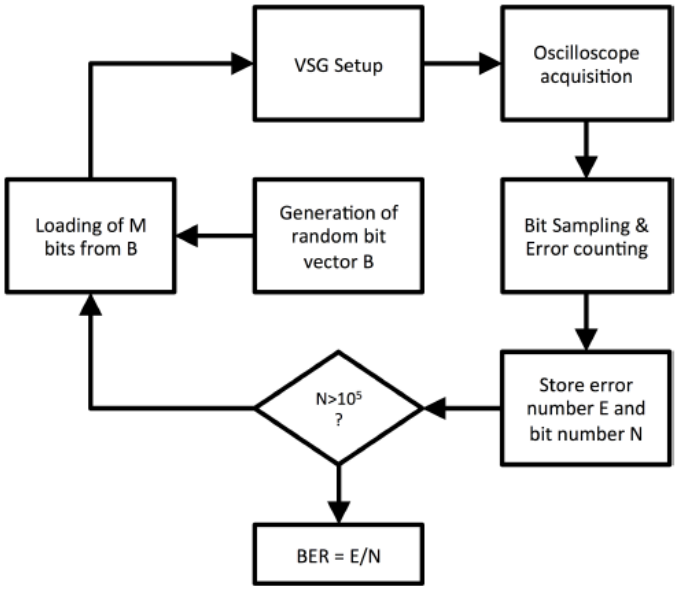

Figure 3.15 Simplified flow-chart diagram of the BER measurement system

3.4.3 High-Speed data communication

BER measurements for minimum, nominal and maximum R_{HS} bit-rate and their key measured waveforms are shown in Fig.3.16, Fig. 3.17 and Fig. 3.18. Both input and output clock and data signal are shown as well as the envelope signal at the comparator output, $V_{E,HS}$ and the analog detector's output signals, $V_{O,HS}$ and $V_{AV,HS}$. The output signal of the drain node is also depicted. It was measured by using an RF output buffer and it is plotted normalized with respect to its peak value to make the ASK modulation noticeable. The time axis is normalized to the bit-rate to easily recognize each bit period. The lower limit for BER around $3.63 * 10^{-3}$ was measured at $R_{HS} \approx 1\, Mbit/s$. The relatively low bit-rate, comparable with the low cut-off frequency of $Z_{\mathrm{L,HS}}$ in this case, gives enough time to the average value of $V_{AV,HS}$ and output voltage $V_{O,HS}$ to converge. The RF signals in the figure appear distorted due to aliasing, since the sampling frequency of the oscilloscope had to be kept low enough to capture a wide acquisition time.

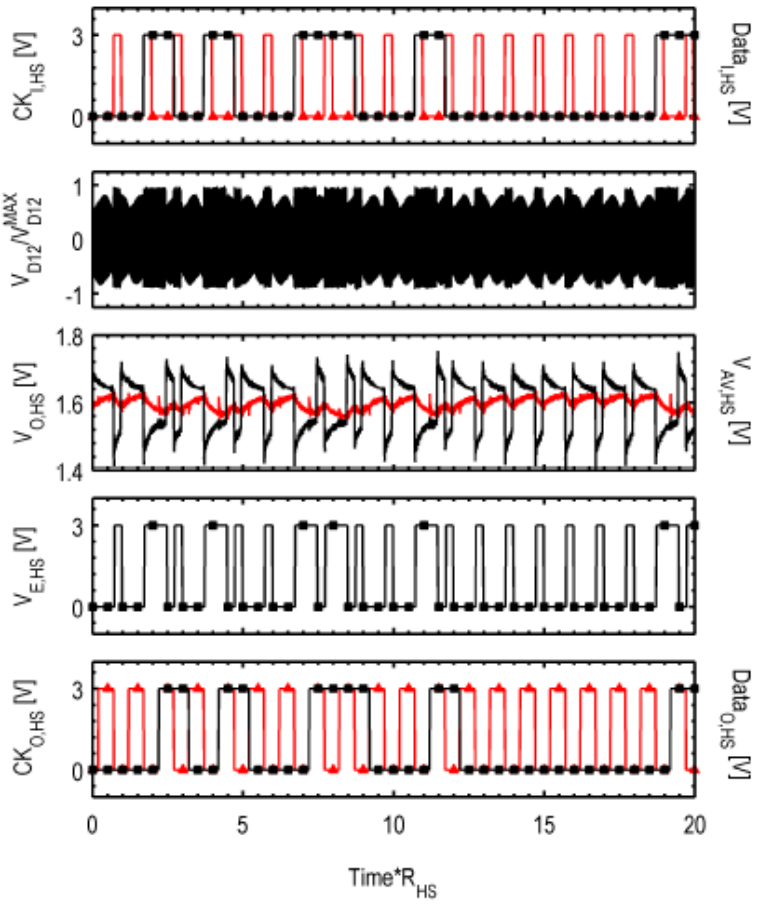

Figure 3.16 Measured HS data link waveforms at 2.5 Mbps

Due to the non-idealities in the oscillator's waveforms the output swing for the nominal 20 Mbit/s bit-rate of 250 mV is slightly higher than the ideal form shown in Fig. 3.7.

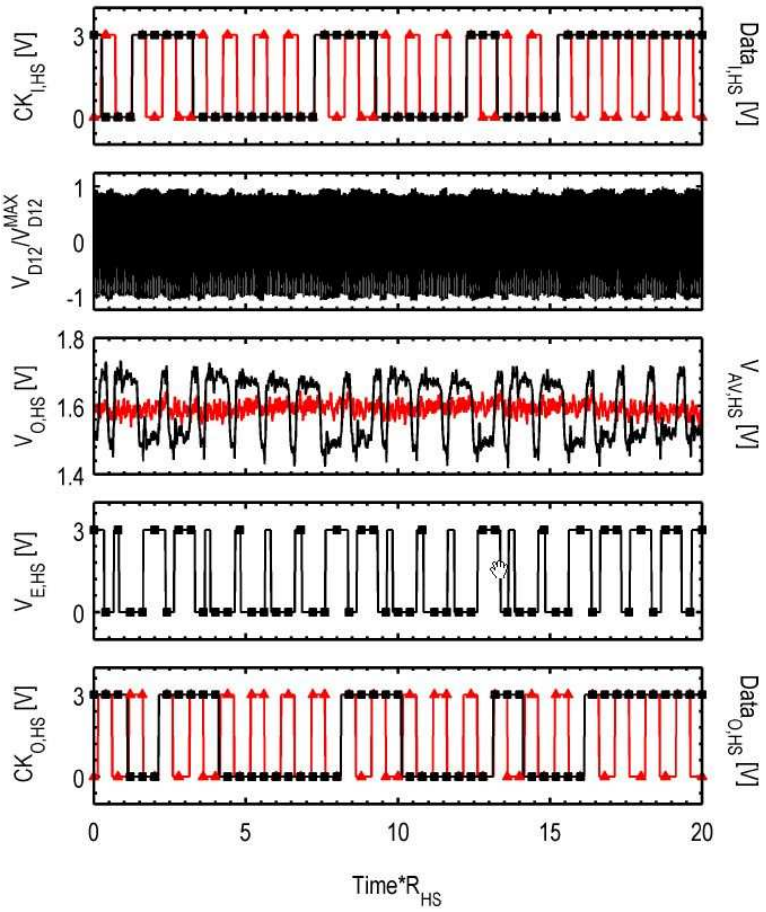

Figure 3.17 Measured HS data link waveforms at nominal bit-rate equal to 20 Mbps

The maximum bit-rate R_{HS} is actually limited to 40 Mbit/s due to limit of the adopted instrumentation to provide an oversampling clock references synchronized with the V_{SG}, although noise margin at this bit-rate is quite low, as shown in Fig. 3.18. It can be noticed also in the PWM waveform, where some zero-coded bits are so short that the relatively low sampling frequency of the oscilloscope is not able to capture them.

In conclusion, measurements with bit-rate from 2.5 Mbit/s to 40 Mbit/s were carried out guaranteeing a BER < 10^{-5}, thus confirming the robustness of the proposed approach even with long sequences of equal bits (0" or "1"), being this the worst case in the PWM coding, due to the reduction of the detector noise margin.

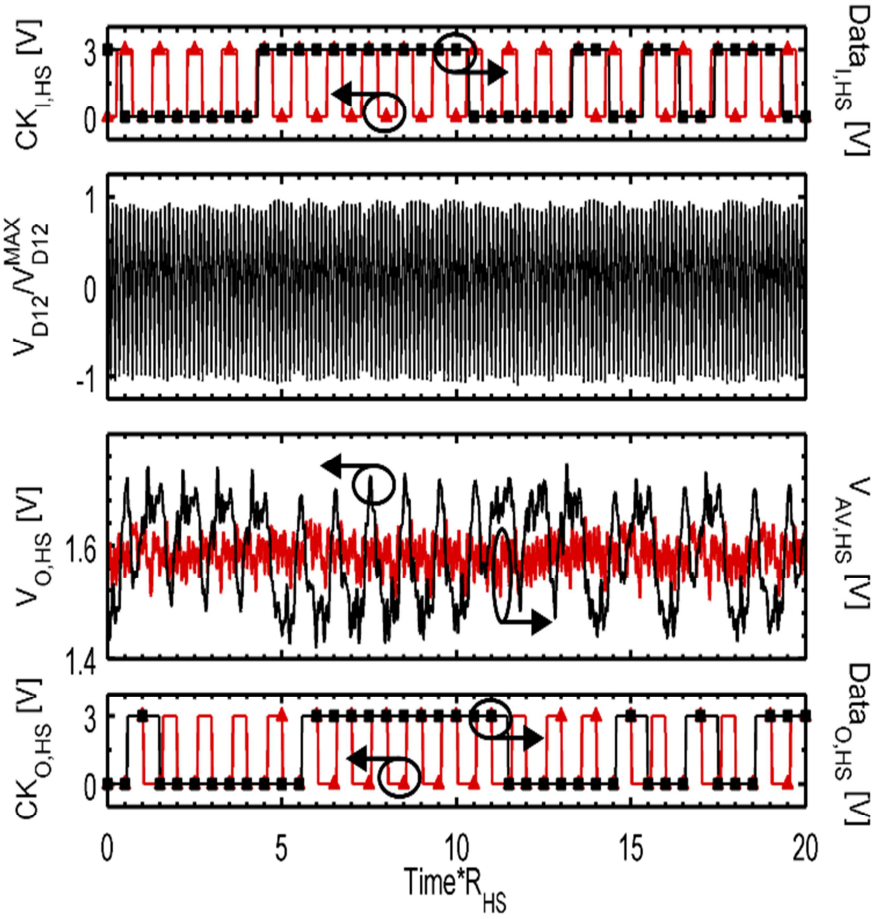

Figure 3.18 Measured HS data link waveforms at maximum bit-rate equal to 40 Mbps

3.4.4 Low-Speed data communication

For the LS data communication measurements at different bit-rate were performed to evaluate the bit-rate limits of this data link by monitoring the BER. Fig. 3.19, Fig. 3.20 and Fig. 3.21 depict the key measured data link waveforms for minimum, nominal and maximum R_{LS} bit rate. The latter was estimate in 3 Mbit/s since the BER is around $2.89 * 10^{-3}$ at $R_{LS} = 6\ Mbit/s$.

Lower limit for R_{LS} is 150 kbps, thus being this value comparable with the loop bandwidth, the error amplifier works in slew-rate at the beginning of each bit. It is almost fast enough to compensate for the envelope signal, although $V_{O,LS}$

and $V_{AV,LS}$ never cross each other because of the single-pole loop-gain transfer function, which shows no overshoot or ringing when the slew-rate condition has ended.

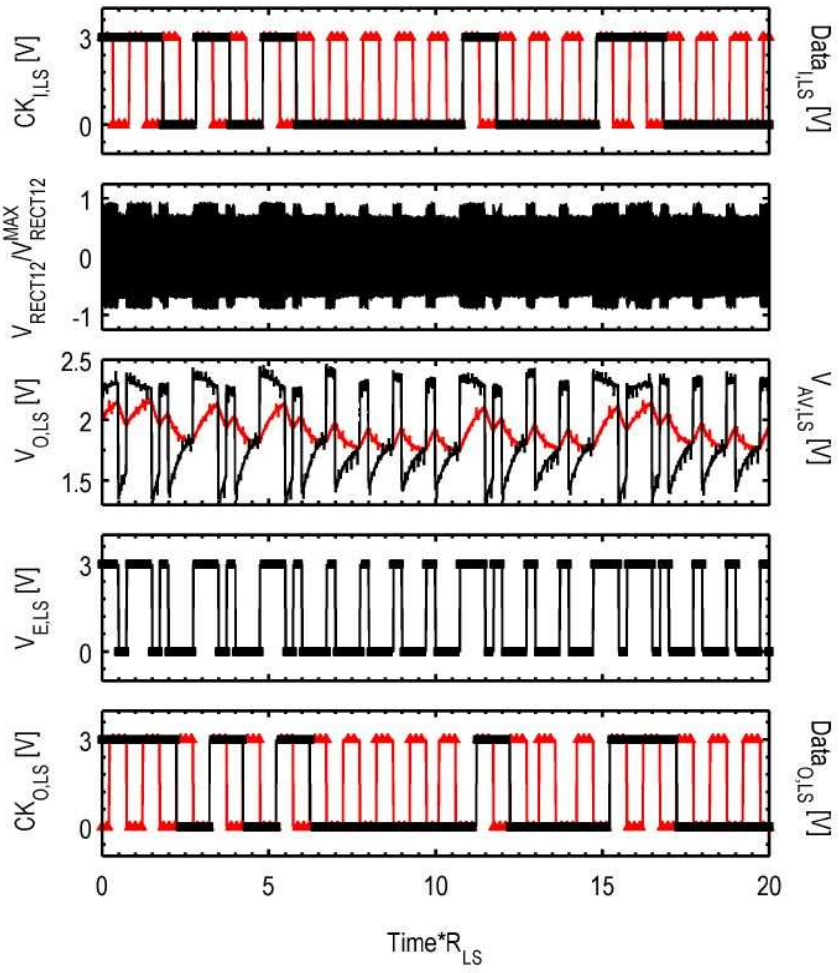

Figure 3.19 Measured LS data link waveforms at minimum bit-rate equal to 150 kbps

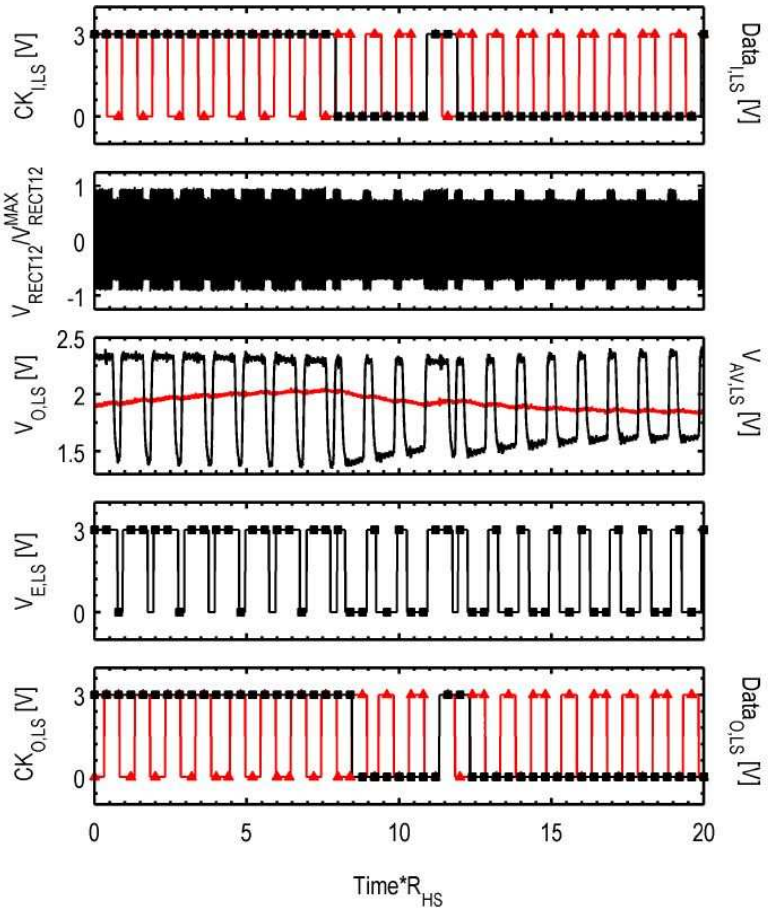

Figure 3.20 Measured LS data link waveforms at nominal bit-rate equal to 1 Mbps

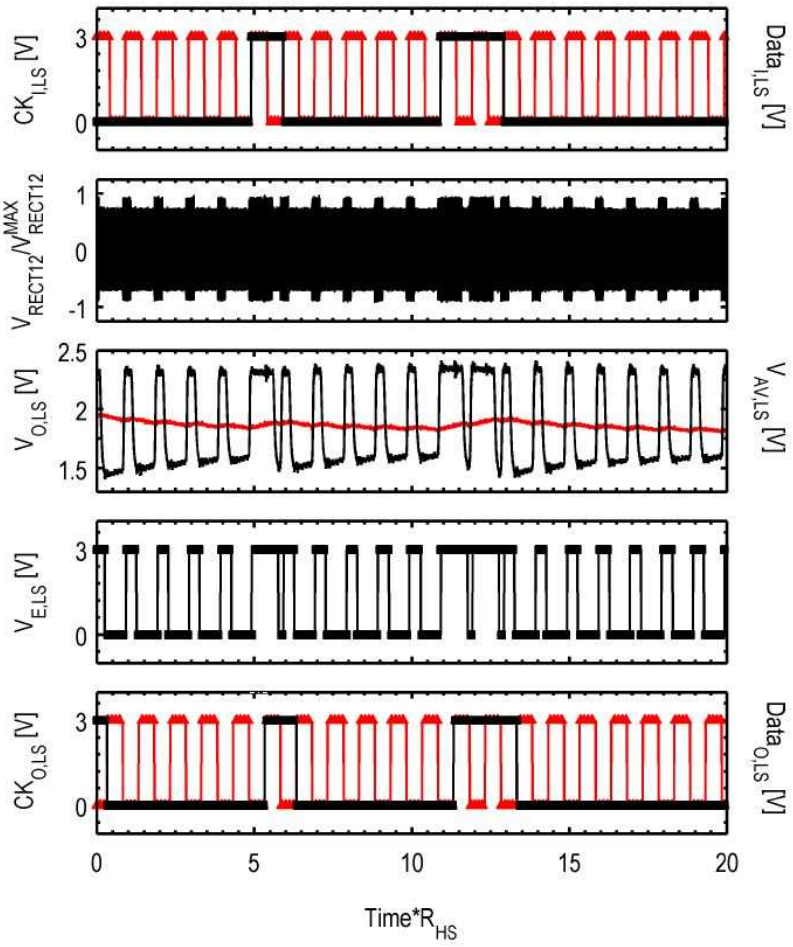

Figure 3.21 Measured LS data link waveforms at maximum bit-rate equal to 3 Mbps

Chapter IV

Common-mode transient immunity

A fully integrated CMOS system able to transfer both data and power by exploiting a single isolation transformer was demonstrated and disclosed in the previous chapter. The design of this isolated system has highlighted critical issues due to the non-linear interactions between each building stage and the very low ratio of carrier frequency to maximum data-rate, thus involving a challenging system optimization. Besides, a crucial requirement associated with these isolated systems is the robustness to common-mode noise. Indeed, CMTI in the order of several tens of kV/μs are mandatory. Unfortunately, the implemented system [26] is not able to guarantee such stringent CMTI specifications. Typically, isolated systems highly suffer from ground shifts since the parasitic capacitive coupling of the galvanic isolation barrier produces common-mode currents, I_{CM}, and consequently hazardous over-voltages and/or data transmission degradation in terms of BER. The current I_{CM} is made up of a strong dc component proportional to the product between the maximum voltage slew-rate, dV/dt and the parasitic capacitances, C, $I_{CM} = C \cdot dV/dt$ and it is also characterised by an important high-frequency component. State-of-the-art approaches to reject the common-mode noise are based on common-mode feedback circuitries [66], [67], which exploit an additional circuit to draw the injected current as shown in Fig. 4.1.

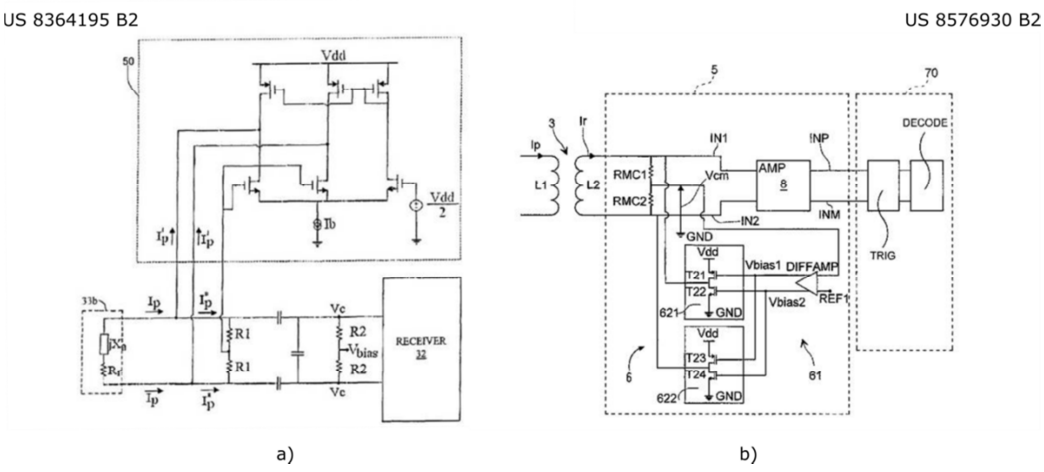

Figure 4.1 Common-mode feedback approach for CMTI

Fig. 4.1 (b) shows a solution using a class-B additional circuit to draw the common-mode noise current. By taking advantage of this approach, a low static consumption can be achieved preserving the system power efficiency but due to its limited frequency bandwidth, this solution is not compliant with high CMTI performance. Then, these approaches are well-suited to isolated systems with very low parasitic capacitances. An alternative technique exploits a multi-resonant passive filtering network to reject the common-mode noise, while transferring a data signal across the isolation barrier [68]. Fig. 4.2 shows the resonant coupler that can include N number of stages, where N is an integer greater than or equal to one. Each one of them can be configured as a pass-band tuned filter to remove spurious noise through filtering, while achieving CMTI up to 150 $kV/\mu s$ as demonstrated in [69]. It is worth noting that the isolated network is fabricated on a dielectric substrate, such as laminate, flex or crystalline materials, which is not suitable to a fully-integrated approach. Besides, the bass-band filter does not discriminate the useful differential signals from the common-mode noise signals, thus involving a dependency of the CMT rejection from the data rate. In fact, by using a high number of stages, N, a very narrow pass-band filter is achieved, while limiting the maximum data rate.

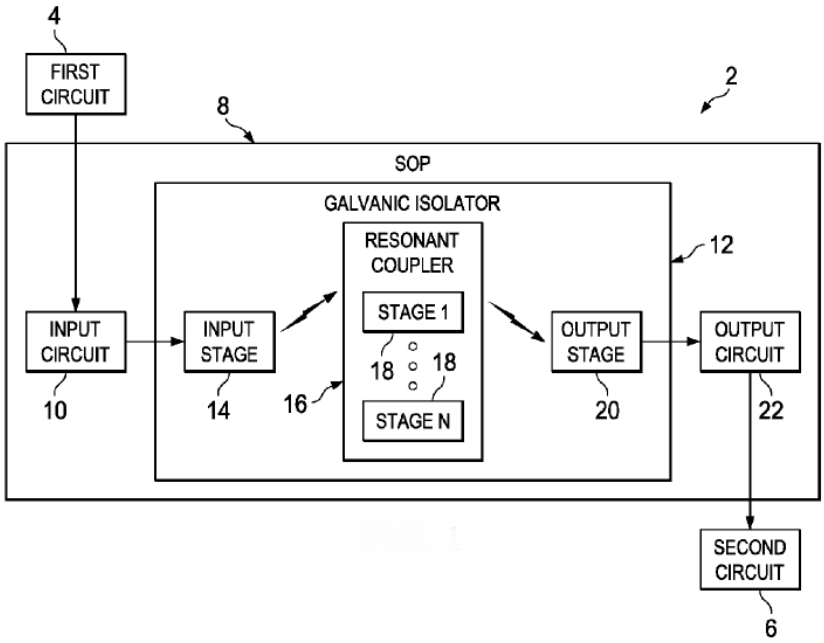

Figure 4.2 Multi-resonant approach for CMTI [68]

Differently from the state of the art, a novel CMT circuit rejection has been conceived, which is depicted in Fig. 4.3.

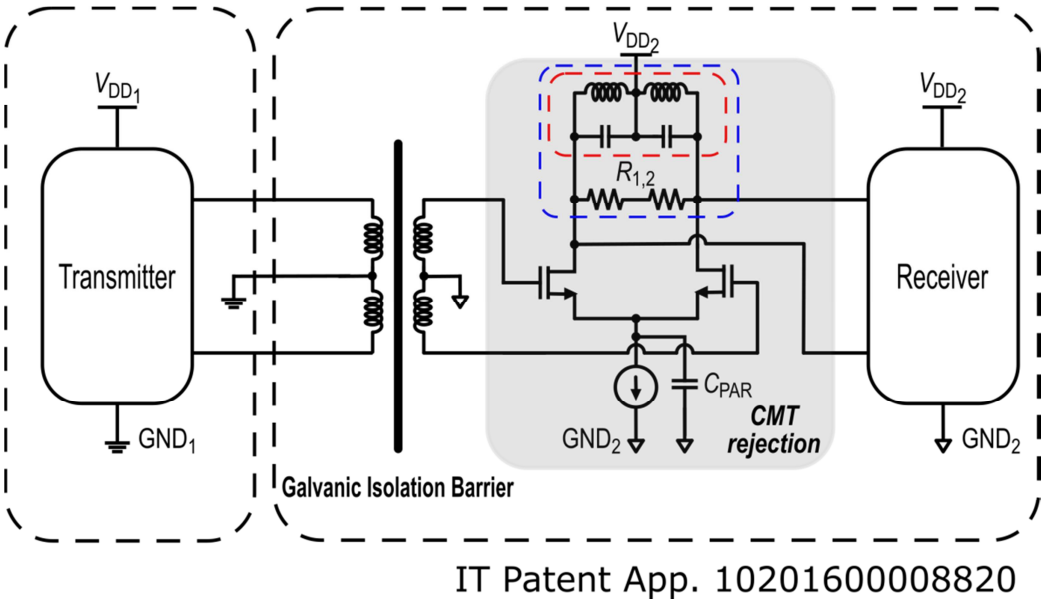

Figure 4.3 Standard data transfer link adopting the CMT rejection circuit [71]

In order to draw both dc and low-frequency components of the injected common-mode noise current, I_{CM}, a very low impedance paths are easily achieved by connecting both center-taps of the isolation transformer to the corresponding ground. Additionally, with the aim of better rejecting the residual high-frequency common-mode spurious, an LC differential amplifier driven by the secondary windings, was adopted. In particular, even if the high-Q LC filter is tuned at the data carrier frequency, differential resistors $R_{1,2}$ are used to properly expand the bandwidth for the differential signals, thus allowing high speed data communication while achieving high CMTI performance, as shown in Fig. 4.4. Otherwise from [69], the proposed CMT rejection circuit is able to perform very selective common-mode filtering while guaranteeing a constant CMTI performance with respect to increasing data rate.

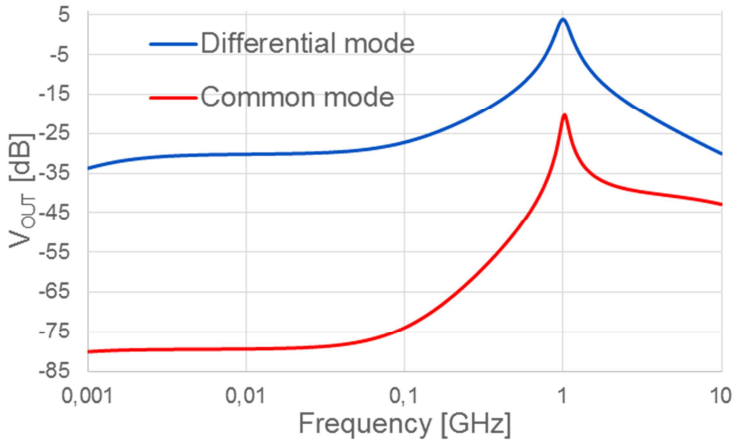

Figure 4.4 Frequency response of CMT rejection circuit

With aim of improving the CMTI performance of the implemented system in [26], the proposed CMT rejection circuit along with properly expedients could be adopted:

- adopting a oscillator operated in class D along with a stacked configuration for the isolation transformer, in order to achieve a higher robustness with respect to the current-reuse topology, thus performing a better resilience to the common-mode noise;

- connecting the center-taps of the isolation transformer to the corresponding grounds, thus achieving low-impedance paths able to draw both dc and low-frequency components of I_{CM};
- increasing the rectifier input impedance, Z_{RECT}, by the ac-coupling the rectifier to the secondary coils of the isolation transformer. By taking advantages of higher Z_{RECT}, the power efficiency of the oscillator can be greatly improved while avoiding its switching-off in presence of CMTs. In fact, in this system which exploit a single isolation transformer to transfer both data and power, the power oscillator has to remain active to guarantee communication;
- exploiting the CMT circuit rejection [71] to better reject the residual high-frequency common-mode spurious.

Fig. 4.5 shows the system disclosed in [26] with the aforementioned solution and the CMT rejection circuit.

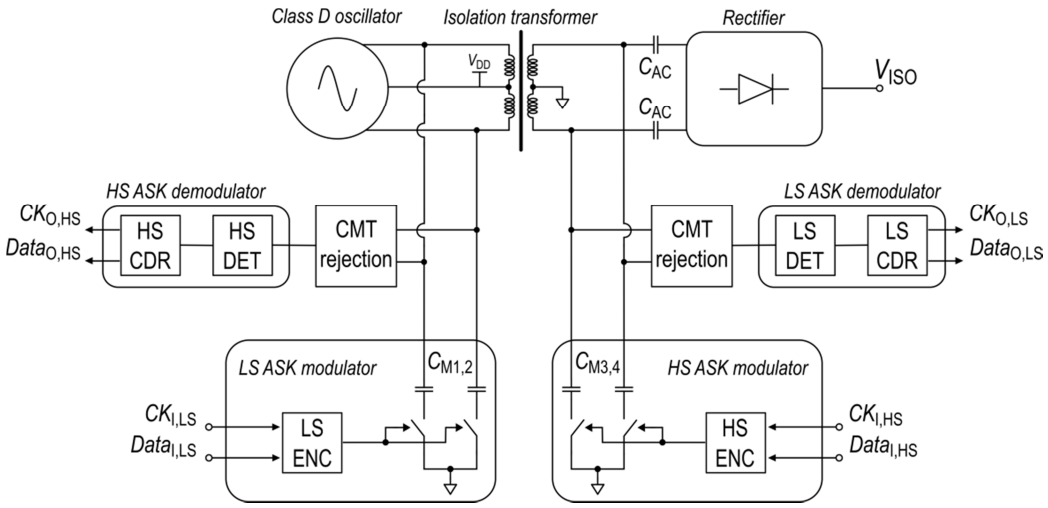

Figure 4.5 Architecture of fully integrated galvanically isolated system providing both data/power transfer on a single isolation transformer while guaranteeing a good CMTI performance

Simulations are carried out to evaluate the robustness of this system in presence of CMTI. During CMTI testing, a pulsed transient is applied across the

isolated ground planes and the input of the rectifier are monitored. The key characteristic of this transient is its slew-rate. Firstly, the system disclosed in [26] was simulated applying a transient pulse with a slope of $\pm 10\ kV/\mu s$ to the ground of the chip A. Fig. 4.6 shows the ASK-modulated signal at the secondary windings of the isolation transformer. Unfortunately, according to the applied transient, the power oscillator turns-off, compromising both power and especially data communication.

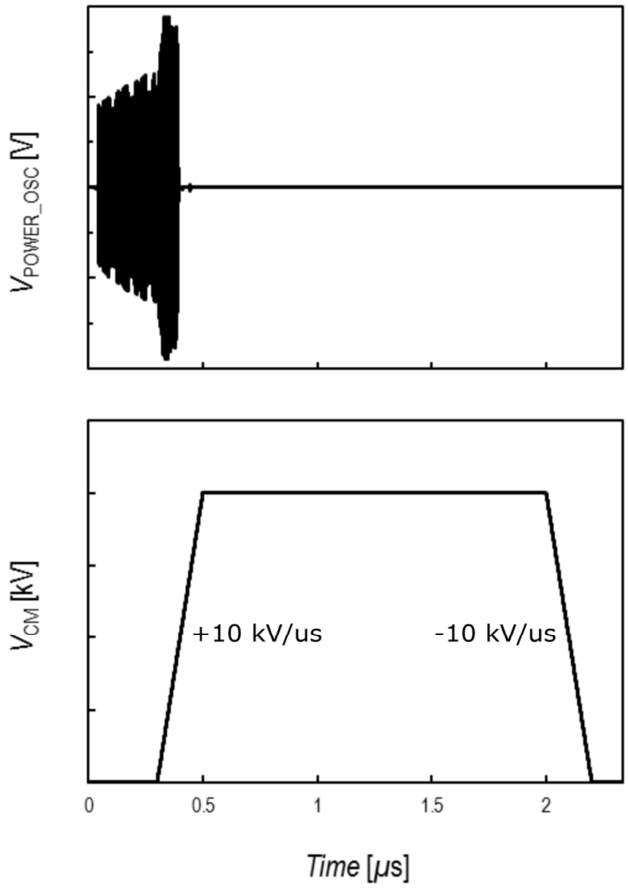

Figure 4.6 System [26] is simulated in presence of $\pm 10\ kV/\mu s$ CMTs

Instead, the simulation results of the system sketched in Fig. 4.5, are shown in Fig. 4.7. It is evident that the power oscillator remains on, thus guaranteeing both power and data transfers. Besides, to better reject the residual high-frequency components, the CMT rejection circuit [71] could be adopted.

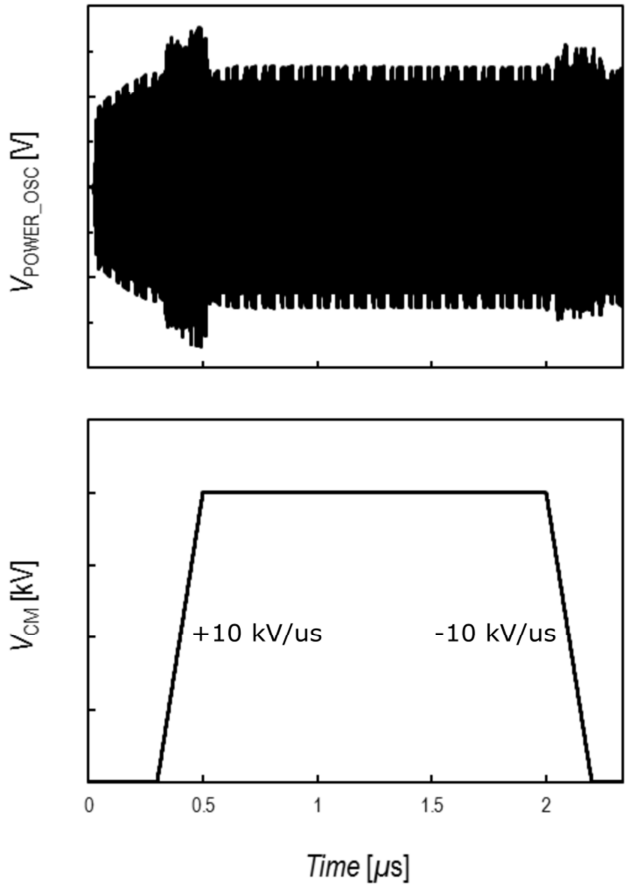

Figure 4.7 The system of Fig. 4.5 is simulated in presence of $\pm$ 10 $kV/\mu s$ CMTs

It is worth noting that exploiting the above-mentioned solutions, a fully integrated isolated system able to guarantee a good CMTI performance, still maintaining the advantages of exploiting a single insolation transformer for both power and data transmission is achievable.

Conclusion

This chapter sums up main results and outcomes of this work, while highlighting novel challenges for future developments of isolated systems.

Power transfer system

In Chap. 2, the analysis and design of a fully integrated dc-dc power converter with on-chip galvanic isolation is disclosed. A depth analysis, concerning both power efficiency and the interactions between building blocks, leads to the development of a co-design procedure. To this aim, a lumped, geometrically scalable model for integrated isolation transformers has been introduced housing a novel empirical expression for the series resistance of both primary and secondary windings. The co-design procedure fully takes advantage of the integrated approach. By taking into account system specifications, the aforementioned transformer model helps to manage the interactions between building blocks, thus maximizing power transfer efficiency.

Differently from the state of the art, a highly integrated dc-dc power converter providing on-chip galvanic isolation by exploiting only two dice was demonstrated. This result could have a great impact on lowering cost and complexity of isolated systems. In fact, commercial products (e.g., iCoupler Analog Devices) adopt post-processed transformers with polyimide dielectrics and 6-μm thick Au metals for the coils, implemented as a third, single die in a system in package configuration.

Besides these main achievements, this isolated dc-dc power converter has been crucial to develop both the data and power transfer system reported in Chap. 3 and the 200-mW P_{OUT} dc-dc converter described in Appendix A.

A fully integrated data and power transfer system

In Chap.3 the design and characterization of the data and power transfer system with on-chip galvanic isolation. For the first time, starting from the isolated dc-dc power converter designed and disclosed in Chap.2, an isolated system able to transfer both power and half-duplex data communication by using only a single integrated isolation transformer was demonstrated [26]. The implementation of such a system involved several circuit and system-level issues, which were properly addressed at design time.

A data stream with data rate up to 40 Mbit/s and an output current higher than 10 mA were measured. This performance is compliant with a wide range of autonomous isolated sensors Moreover, a data stream with data rate up to 3 Mbit/s that can be extremely useful for system setting or testing, was achieved. In order to provide the aforementioned half-duplex data communication, two novel common-source based ASK detectors with adaptive biasing were introduced. Despite the very low ratio of carrier frequency to maximum data-rate and the many drawbacks of the adopted PWM coding, these circuitries have worked very well during all measurement conditions. In addition, with aim of preserving the whole power efficiency during the HS data communication, a modulation index as low as 5 % was adopted.

To the best of the author's knowledge this is the first reported system able to integrate all those function by using only two silicon chips, and hence it could represent a serious breakthrough in the field of fully integrated interfaces for low-power sensor applications.

It is worth noting that a crucial requirement associated with these isolated systems is the robustness to common-mode noise in the order of several tens

of kV/μs. Unfortunately, this system is not able to guarantee such stringent CMTI specifications, but its performance can be improved by exploiting the expedients disclosed in Chap. 4.

Open issues

Some open questions remain to be addressed to increase performance and reliability of the isolated data and power transfer systems:

- CMTI performance can be improved with level up to $50\,kV/\mu s$ in order to increase both the reliability of these isolated systems with a single isolation transformer for both power and data.
- Higher output power levels require output regulation by means of an isolated feedback link, thus increasing efficiency performance and functionality of the system.

These open issues could be taken into account together, thus achieving an innovative highly integrated isolated dc-dc converter with bi-directional data communication. Two different 5-kV isolated links can be implemented, as included in a US patent [73]. In particular, one link can be used to deliver the regulated output voltage up to 100 mW, while the second one can be exploited to implement the control loop of output power while allowing a bidirectional half duplex data communication up to $50\,Mbit/s$. Besides, the resilience to common-mode noise of this system could be improved by using the CMT rejection circuit [71], thus achieving a CMTI up to $50\,kV/\mu s$ independently of the data rate.

Conclusion

Main results of this work demonstrate that by exploiting proper architectures and design techniques, power transfer with on-chip galvanic isolation, as well as data and power transfer using a single isolation transformer,

are both feasible with current silicon technology. The power efficiency performance is mainly limited by the technology BEOL and can be increased by improving the quality of coil's metals. In fact, the metal thickness defines the resistivity and maximum current of transformer coils, thus affecting the minimum coil's metal width for a given power target. Higher thickness could be exploited to reduce either transformer area, which is proportional to both costs and parasitic capacitance and affects power density, or power losses, thus increasing peak performance and resilience to CMTs.

By taking advantage of simple expedients discussed in Chap. 4 the CMTI performance of the system [26] can be improved, thus demonstrating that the data and power can be transferred by using a single isolation transformer.

Appendix A

DC-DC isolated power converter

This appendix focuses on a dc-dc power converter fabricated in 0.8-μm CMOS technology with on-chip galvanic isolation. By taking advantages of the design steps discussed in Chap. 2, an highly integrated galvanically isolated power transfer system for isolated interfaces, such as wireline transceiver and signal processing blocks, was designed and demonstrated [43].

In particular, the isolated dc-dc converter is able to deliver an output power up to 200 mW, P_{OUT}, at 8-V output voltage, V_{OUT}, from a 5-V power supply, V_{DD}. An upper bound of 6 mm^2 for the whole area and a fully CMOS architecture for dc-ac power converter were chosen. Furthermore, the design was tailored to the maximization of power efficiency, which is another key aspect for these isolated systems, thus achieving an efficiency better than 27 % at maximum output power of 200 mW.

According to the simplified block diagram shown in Fig. 6.1, the system houses a power oscillator, an isolation transformer (chip 1) and a rectifier (chip 2).

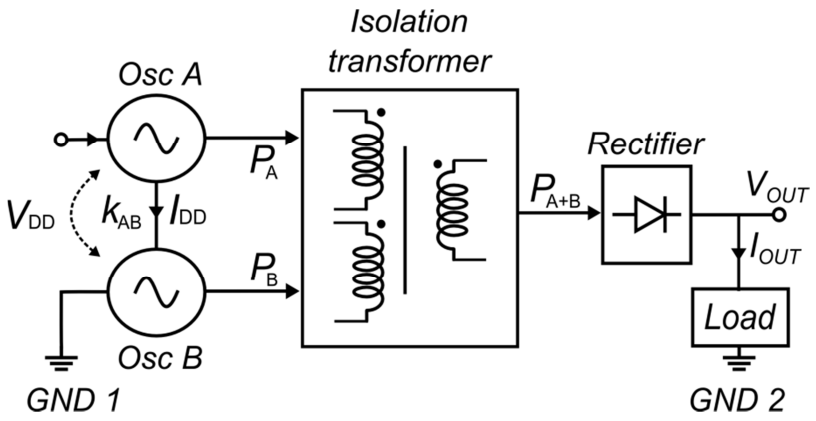

Figure 6.1 Simplified diagram block of the isolated dc-dc power converter demonstrated in [43]

As for the isolated converter disclosed in Chap. 2, the power oscillator is made up of two complementary oscillators sharing the same current, the isolation transformer provides both galvanic isolation and power combining, whereas the rectifier performing the ac-dc power conversion is implemented by using Schottky diodes in simple full-bridge arrangement. Fig. 6.2 shows the simplified schematic of the fully integrated dc-dc power converter. In particular, the power oscillator is made up of two LC complementary oscillators (i.e., $M_{1,2} - L_{P1,2} - C_{P1}$ and $M_{3,4} - L_{P3,4} - C_{P2}$) that share the same current and whose tank inductors are magnetically coupled to each other, according to the dot-scheme. Inductors $L_{P1,2}$ and $L_{P3,4}$ form the two primary windings of the isolation transformer, T_{ISO}, whereas inductors $L_{S1,2}$ are the secondary coils. The signal produced at each primary winding is then delivered to the secondary winding of T_{ISO}, where a power combining is performed, thus nearly doubling the overall output power on the equivalent rectifier impedance, Z_{RECT}. The current-reuse arrangement improving the power efficiency of the overall oscillator, is easily implemented by means of the center-tap of the primary windings of T_{ISO}. The rectifier sets an upper limit to the operation frequency due to the degradation of ac-dc conversion efficiency at increasing frequencies.

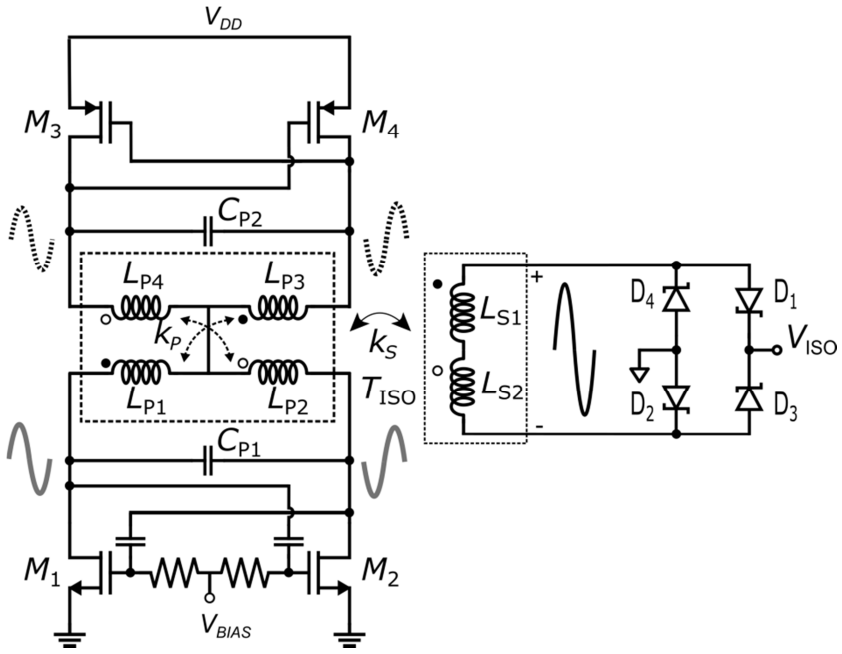

Figure 6.2 Simplified schematic of the fully integrated dc-dc power converter providing a P_{OUT} up to 200 mW

For isolated power transfer applications, rectifier efficiency values better than 80 % are mandatory. This performance can be attained by using high-frequency diodes in simple bridge rectifier topology. Differently from the isolated converter described in Chap 2, this technology platform houses a Schottky diode, thus allowing a full-bridge rectifier to be implemented with almost flat power efficiency performance up 300 MHz. Therefore, this frequency was considered the upper limit for the system operation frequency. As far as co-design is concerned, the performance of MOS transistors and isolation transformer of the power oscillator are linked together by several design parameters. Among these, the most important are transistor sizes, inductance values of primary and secondary windings ($L_{P1,2}$, $L_{P3,4}$, and $L_{S1,2}$), and the geometrical parameters of the isolation transformer (i.e., width, internal diameter, etc.). These parameters were set by means of an optimization procedure based on circuit simulations with scalable modelling of the transformer, as already discussed in Chap. 2. By taking advantages of this optimization procedure, the transformer-coupled power

oscillator and the isolation transformer were designed and Table 6.1 summarized their adopted design parameters.

Table 6.1 Design parameters of the oscillator and the isolation transformer

Block	Parameter	Value	Unit
Oscillator Core	$W_{1,2}$	6.05	[mm]
	$W_{3,4}$	4.9	[mm]
	$L_{1,2,3,4}$	0.8	[μm]
Isolation Transformer	L_P ; L_S	6.5; 6.5 @ f_{OSC}	[nH]
	k_P ; k_S	0.85; 0.6	
	k_P ; k_S	0.85; 0.55	
	f_{OSC}	240	[MHz]
	V_{DD}	5	[V]

At 5-V supply voltage, nominal oscillation frequency was about 240 MHz. Moreover, a transformer ratio, $N = \sqrt{L_S/L_P}$, of about 2 was adopted in order to boost the output voltage at the secondary coil after power combining. Simulated differential output waveforms for both n-MOS and p-MOS oscillators along with the output voltage at the secondary winding, V_{OUT_AC}, are depicted in Fig. 6.3. Simulations are carried out with equivalent output impedance of $130\ \Omega/1pF$. An ac power of 330 mW is delivered to the secondary side of the isolation transformer with an efficiency of 39 %. The simulated efficiency of T_{ISO} within the overall system is around 54 %.

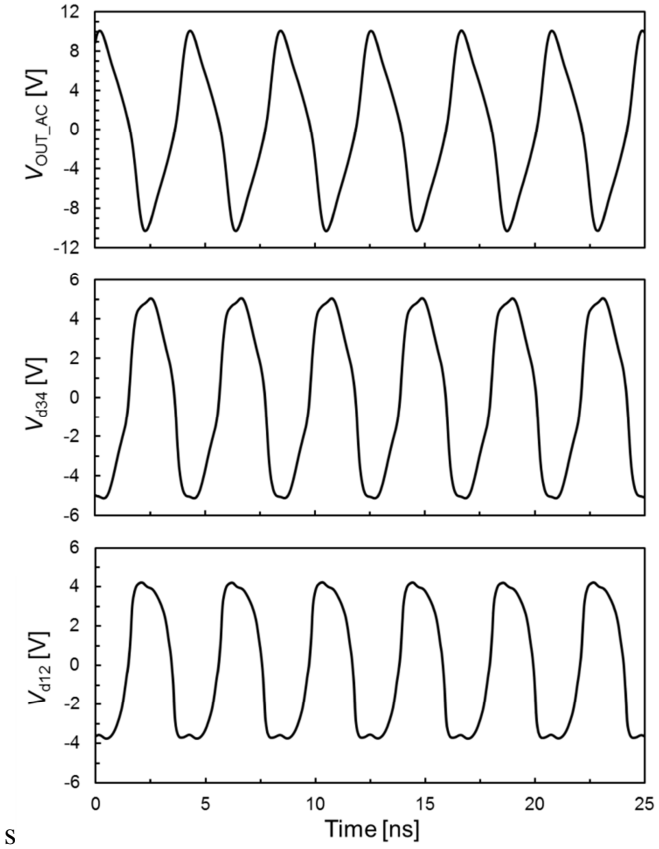

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Figure 6.3 Simulated voltage waveforms of the transformer-coupled oscillator

As before discussed, the four inductors ($L_{P1} - L_{P4}$) forming the primary coils of T_{ISO}, are arranged by means of two symmetric interleaved configurations, one for each secondary coupled windings (i.e., L_{S1} and L_{S2}), with a common terminal for the center tap. With aim of reducing the underpass series resistance, metal 2 is shunted to metal 1. The interleaved configuration guarantees high magnetic coupling thanks to the very close spacing (1-μm) available on the metal 3, while allowing inherently symmetric coils to be designed. The secondary coils, L_{S1} and L_{S2}, are stacked on the primary coils using the top metallization and connected to build the secondary winding. To achieve higher magnetic coupling factor, k_S, between primary and secondary windings, which affects the overall system efficiency, it is of utmost importance to equalize the external diameters of the secondary coils and the interleaved primary spirals, thus maximizing the overlap

area between primary and secondary windings. The physical implementation adopted for the isolation transformer is shown in Fig. 6.4.

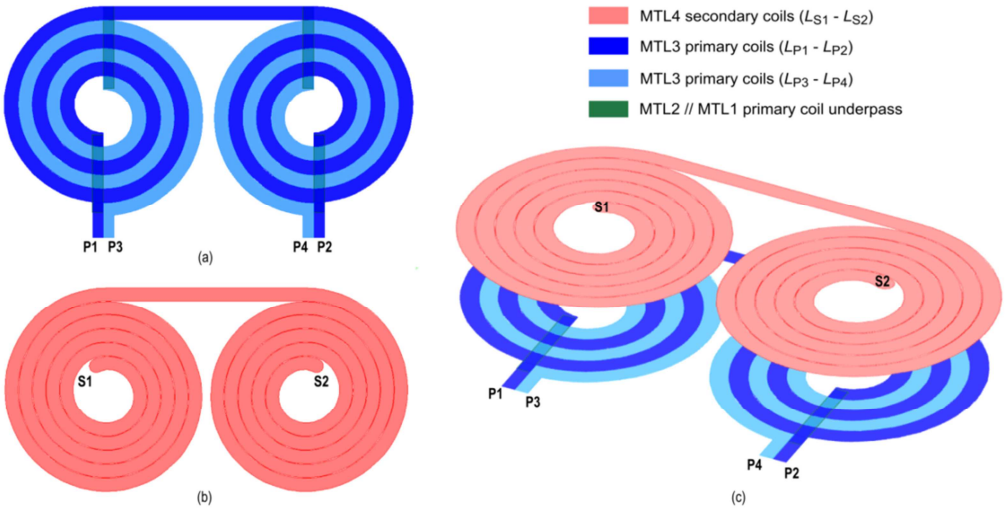

Figure 6.4 Isolation transformer. (a) Primary winding. (b) Secondary winding (c) 3*D*-view

Starting of the scalable model topology disclosed in Section 2.3.3.1, a customized model has been developed and verified by using EM simulated data of 24 geometrically scaled isolation transformers drawn according to the configuration of Fig. 5.4 (primary: n_P from 2.5 to 3.5, w_P from 70 μm to 130 μm, D_{INT} from 350 μm to 550 μm; secondary: n_S from 5 to 7, w_S from 70 μm to 130 μm, D_{INT} from 350 μm to 450 μm).

Fig. 6.5 depicts the error distributions on low-frequency inductance, maximum Q-factor, SRF and magnetic coupling factors, k_P and k_S, for 24 transformers. These results confirmed the soundness of the model that was hence profitable exploited to design the transformer for the proposed power transfer system. Although the model was developed for the single-ended structure, the coupling effects are negligible if proper distance between right and left transformer sides is adopted.

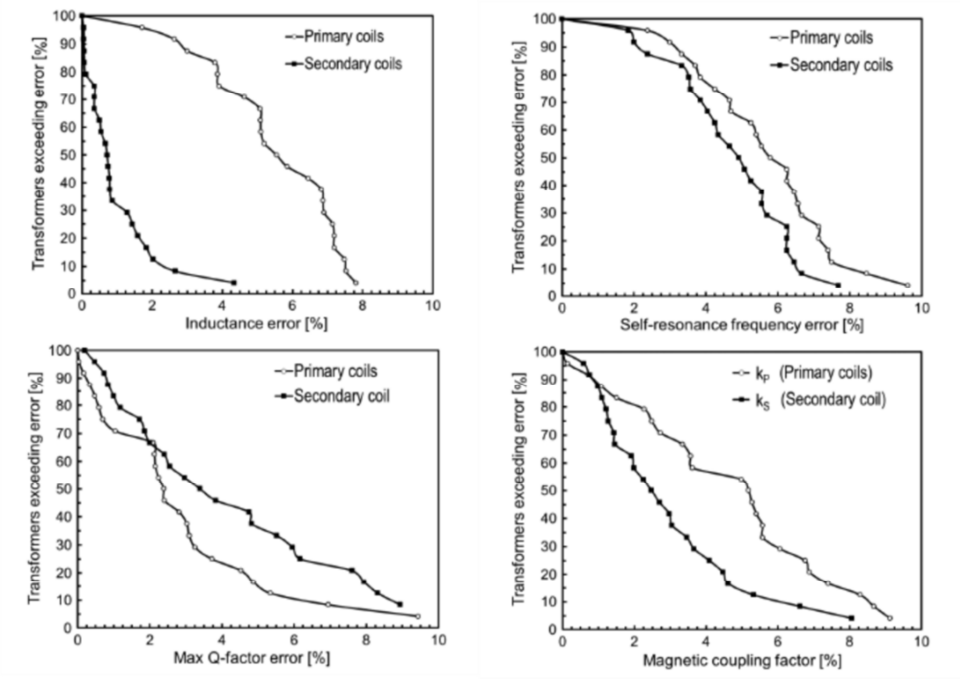

Figure 6.5 Error distributions of the lumped scalable model of the isolation transformer calculated with respect to EM simulations

The adopted geometrical parameters are summarized in Table 6.2. Finally, Fig. 6.6 compares (single-ended) performance of the adopted isolation transformer (corresponding to the geometrical parameters of Table 6.2) estimated by the developed lumped model, simulated with a 2D EM tool, and measured on-wafer.

Table 6.2 Isolation transformer geometrical parameters

Block	Parameter	Primary coils	Secondary coils
Isolation Transformer	Numbers of turns (n)	2.5	5
	Width (w) [μm]	110	106
	Spacing (s) [μm]	112	5
	Inner diameter (D_{INT}) [μm]	460	431
	Outer diameter(D_{OUT}) [μm]	1680	1640

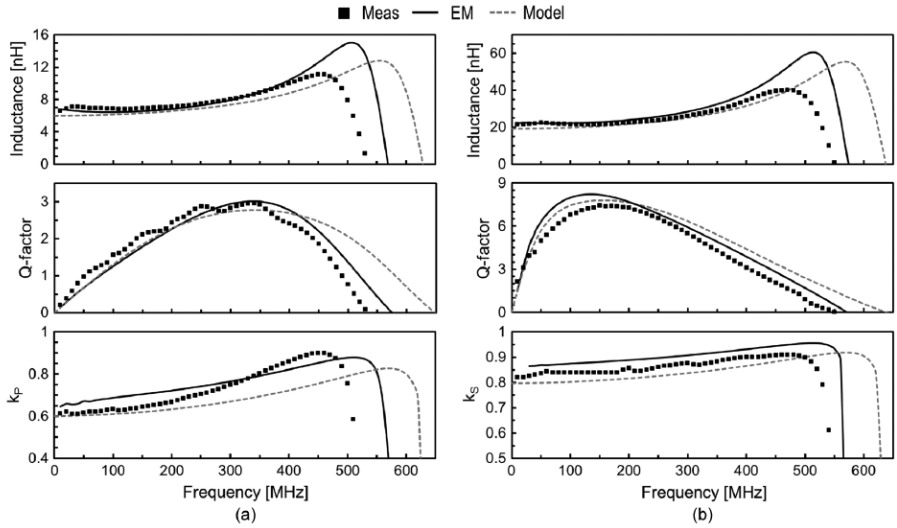

Figure 6.6 Isolation transformer (half structure) performance. (a) Primary coil. (b) Secondary coil

Main discrepancies with measured performance are related to the SRF and are mainly due to inaccuracy in the parasitic de-embedding [70]. It is worth noting the excellent agreement between the model and measured/simulated curves in the useful range of frequencies (i.e., below the SRF). Fig. 6.7 shows the micrograph of the implemented power oscillator chip, whose die size is 3.6 mm x 2.7 mm that is mainly due to the isolation transformer area of 5.7 mm^2. The CMOS active core is placed at the bottom of the die. Large ground/power supply planes in the top metal layer were adopted to reduce on-chip parasitic inductances, while off-chip parasitics were minimized by using multiple bonding wires. In order to demonstrate a complete power transfer system based on the proposed power oscillator topology, a previously integrated rectifier designed for higher output power/voltage levels was exploited.

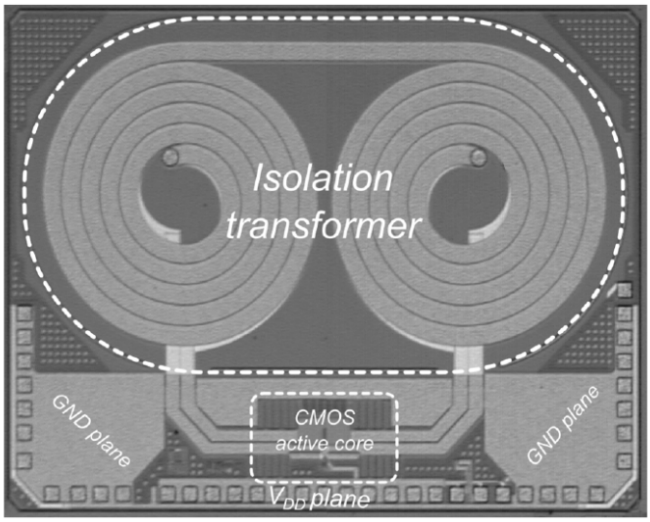

Figure 6.7 Micrograph of the transformer-coupled CMOS oscillator

Fig. 6.8 shows a die photo of the rectifier adopting the traditional full-bridge topology with Schottky diodes. It has an actual size of 950 μm x 725 μm while including a 200 pF output filter capacitor.

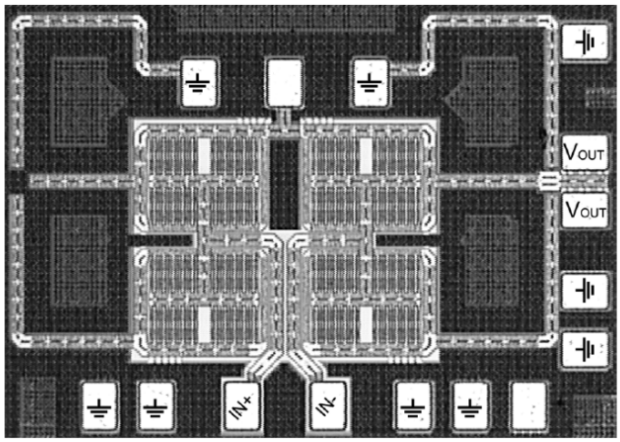

Figure 6.8 Micrograph of the full-bridge diode rectifier

All measurements were performed at 5-V power supply and room temperature. First, the performance of the dc-ac conversion was evaluated by mounting the power oscillator die on a FR4 board along with an equivalent output load performed by a resistance, R_L, in parallel to a capacitance, C_L. The dc-ac

performance was extensively measured in terms of transferred power, P_{OUT_AC}, and efficiency, η_{DC-AC}, evaluated as a function of the load impedance. Fig. 6.9 reports the measured output power and efficiency at the secondary winding as a function of load resistance R_L without C_L. The oscillation frequency, f_{OSC}, was around 250 MHz. An output power of 290 mW and a maximum efficiency of 36 % were achieved with an R_L of about 130 Ω.

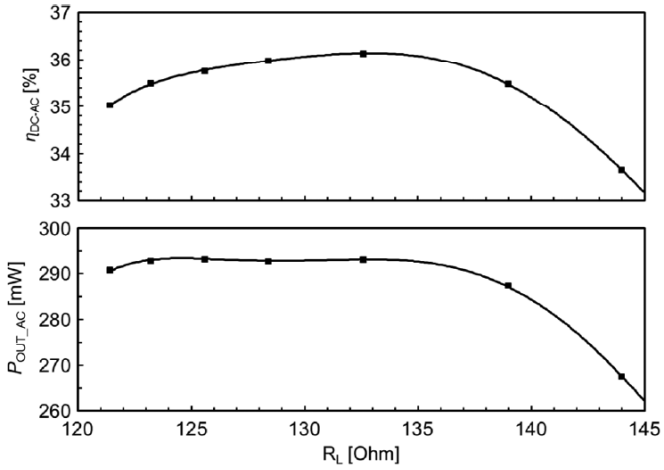

Figure 6.9 Measured output power and efficiency at the transformer secondary winding as a function of load resistance R_L (C_L = 0, f_{OSC} = 250 MHz)

The loading effects of capacitance C_L were evaluated with the optimum load resistance. Fig. 6.10 shows the delivered output power, the power efficiency, and the oscillation frequency as a function of C_L, with R_L of 130 Ω. Output power and efficiency achieve a maximum of 300 mW and 36.5 %, respectively, corresponding to an oscillation frequency of about 230 MHz with a C_L of around 1 pF. For load capacitances higher than 2 pF, the oscillation frequency decreases and both output power and efficiency exhibit a significant degradation.

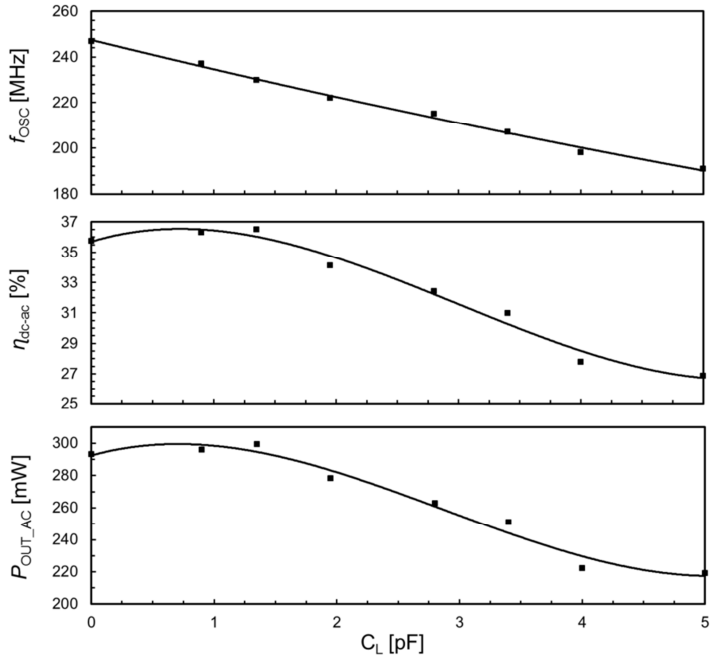

Figure 6.10 Measured output power, efficiency, and oscillation frequency at the transformer secondary winding as a function of load capacitance C_L with R_L = 130 Ohm

These measurements confirm that there is an optimum load capacitance that can be achieved by properly setting the area of the Schottky diodes in the rectifier. Fig. 6.11 shows the output voltage, V_{OUT_AC}, measured at the secondary winding of the isolation transformer with the optimum load (i.e., $R_L = 130\ \Omega$ and $C_L = 1$ pF). The voltage waveform was captured with a high-impedance active probe. Thanks to the power combining, differential oscillation amplitude as high as 10 V was achieved.

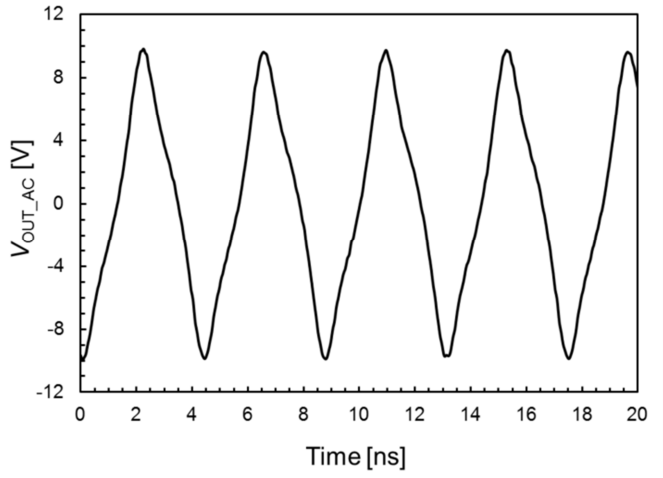

Figure 6.11 Measured output voltage at the transformer secondary winding

With aim of performing a full characterization of the dc-dc conversion, the complete system consisting of the oscillator and the rectifier was assembled on board, as shown in Fig. 6.12.

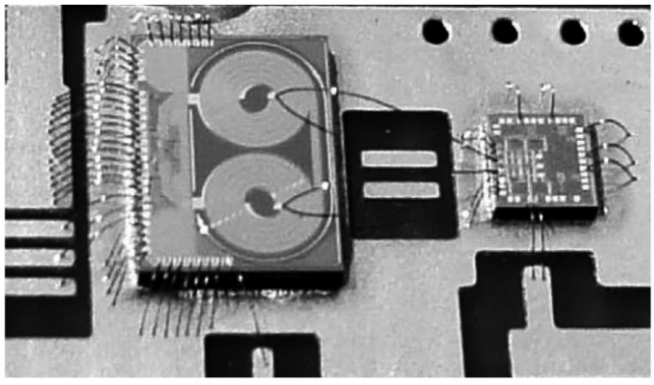

Figure 6.12 Micrograph of the overall power transfer assembled on board

The dc-dc converter performance that is measured with the dc output voltage, V_{OUT}, that sweeps from 5 V to 12 V, by means of a semiconductor parameter analyser, is shown in in Fig. 6.13. The overall system is able to deliver a dc output power of 200 mW with power efficiency better than 27 % at a V_{OUT} of 8-V. Of course, this performance is affected by the available rectifier that is not

optimized for this dc-ac converter. Actually, with a proper design of the rectifier, it is expected that the dc-dc converter achieves an output power and efficiency of about 250 mW and 30 %, respectively.

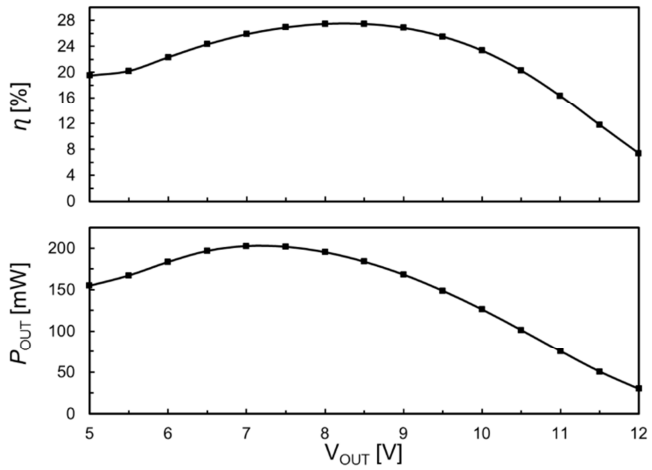

Figure 6.13 Measured dc output power and efficiency versus dc output voltage

Measured performance of the dc-dc converter is summarized and compared with the state of the art in Table 6.3. Both works was obtained thanks to the current-reuse transformer-coupled oscillator topology and a proper design approach.

Table 6.3 Summarized performance with state-of-the-art comparison

Parameters	**[6]**	**[7]**	**This Work**
Oscillator topology	n-MOS	Cross-coupled	Current-reuse Transformer-coupled
P_{OUT}	500 mW	225 mW	200 mW
η	33 %	25 %	27 %
V_{OUT}	5 V	5 V	8 V
V_{DD}	5 V	5 V	5 V
f_{OSC}	170 MHz	160 MHz	240 MHz
Voltage gain	1	3	1.6
Isolation rating	5 kV	5 kV	5 kV
Chip number	3	3	2
Isolation technology	Post-processed polyimide transformer, 6-μm Au MTLs		On-chip SiO_2 transformer, 0.9-μm Al / 3.7-μm Cu MTLs
Silicon technology	0.6-μm HV-CMOS, Schottky diodes		0.8-μm CMOS, Schottky diodes

Appendix B

Publications

Patents

- E. Ragonese, V. Fiore, N. Spina, **P. Lombardo**, G. Palmisano, "Power oscillator apparatus with transformer-based power combining for galvanically-isolated bidirectional data communication and power transfer", US patent US9306614 B2, granted 05 April 2016.

- E. Ragonese, N. Spina, **P. Lombardo**, N. Greco, A. Parisi, G. Palmisano, "Galvanically isolated DC-DC converter with bidirectional data transmission," US Patent App. 15178822, filed 10 June 2016.

- E. Ragonese, N. Spina, **P. Lombardo**, N. Greco, A. Parisi, G. Palmisano, "A galvanic isolation circuit, corresponding system and method," IT Patent App. 10201600008820, filed 30 Aug. 2016.

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- **P. Lombardo** (Speaker), V. Fiore, E. Ragonese, G. Palmisano, "A fully-integrated half-duplex data/power transfer system with up to 40Mbps data rate, 23mW output power and on-chip 5kV galvanic isolation," *IEEE International Solid-State Circuits Conference (ISSCC)*, San Francisco, USA, Feb. 2016, pp. 300-301.

Peer-reviewed journals

- N. Spina, V. Fiore, **P. Lombardo**, E. Ragonese, and G. Palmisano, "Current-reuse transformer coupled oscillators with output power combining for galvanically isolated power transfer systems," *IEEE Trans. Circuits Syst. I: Regular Papers*, vol. 62, pp. 2940-2948, Dec. 2015.

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"Life is always

triumph of the improbable and

the miracle of the unexpected"

"Henri-Marie de Lubac"

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