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NUNZIO GRECO

Fully integrated dc-dc converters with basic and double galvanic isolation

Ph.D. Thesis

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Summary

This dissertation summarizes the main activities that I have been carried out at the *Radio Frequency Advanced Design Center (RF-ADC)*, a joint research group between the university of Catania and STMicroelectronics Catania, during three years of Ph.D. studies.

The increasing demand of low-profile power converters in modern electronic devices has pushed research towards integrated systems able to replace expensive and bulky solutions based on discrete components. Consequently, galvanically isolated interfaces are becoming an interesting research topic for both industry and academia, since integrated systems performing power and/or data transfer through a galvanic isolation barrier are largely demanded in a wide range of applications, which are growing rapidly during the last few years.

Galvanic isolation can be required for several reasons, e.g. to ensure the

proper function of a system, to preserve sensitive circuits from damages or to guarantee safety of human beings. In this context increasing levels of galvanic isolation have been defined by regional and international bodies. The main applications and different degrees of galvanic isolation will be discussed in Chapter 1, along with an overview of the state-of-the-art of semiconductor isolators. The technology platform adopted for this work will be introduced as well. It is provided by STMicroelectronics, and its peculiar back-end allows to implement on-chip passives providing 5-kV of galvanic isolation. Besides, it is used for the production of commercially available integrated data isolators.

A fully integrated power transfer system with on-chip basic galvanic isolation will be presented in Chapter 2. Specifically, it is a 300-mW step-up dc-dc converter for gate driver's power supply applications, exploiting a CMOS-based circuit topology. Indeed, the design of galvanically isolated power transfer systems is not a trivial task due to the highly non-linear interactions between building blocks. It requires an accurate evaluation of on-chip and off-chip parasitics, modeling of passive devices along with a customized co-design procedure to pursue maximization of performance. To this aim, a novel lumped, scalable modelling for three-winding integrated transformers with tapped primary coils has been developed.

The analysis and design of a 100-mW dc-dc converter with double galvanic isolation will be the object of Chapter 3. Currently, only data isolators performing on-chip double isolation are available in the state-of-the-art, whereas power transfer is still hindered by low efficiencies of series-connected integrated isolation transformers. A novel circuit architecture will be pro-

posed, achieving an efficient power transfer across a double isolation barrier thanks to a resonant mode operation between system's blocks. Finally, an innovative PWM control loop performing output power/voltage regulation will be presented. At the authors' best knowledge this is the very first fully integrated and double isolated dc-dc converter with integrated output voltage regulation, among previously published works.

Besides the main topic, during the first year of my Ph.D. studies I was involved in another research activity that was carried out at the RF-ADC. I actively contributed to the design of an RF-powered transceiver for wireless sensor networks (WSNs) applications, which exploits a sample and hold operation on the received carrier. Specifically, thanks to a PLL working alternatively in closed and open loop condition, the system recovers downlink data and generates the uplink carrier for data transmission, respectively, while exploiting the same antenna for the receiving and transmitting phases. The description and characterization of this system is discussed in [1].

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CHAPTER 1

Integrated Systems with Galvanic Isolation

1.1 Introduction to galvanic isolation

Galvanic isolation is a principle used to separate electrically two domains while allowing at the same time an exchange of energy and/or informations between them. It eliminates any direct path connections, thus preventing unwanted dc and ac current flows in both directions.

Galvanic isolation can be adopted for several reasons. It is a simple solution for breaking ground loops, but also it guarantees safety in case of electrical shocks. Common applications include industrial automation systems, motor drives, medical equipment, solar inverters, power supplies and hybrid electric vehicles (HEVs). A real scenario is shown in Fig. 1.1, where

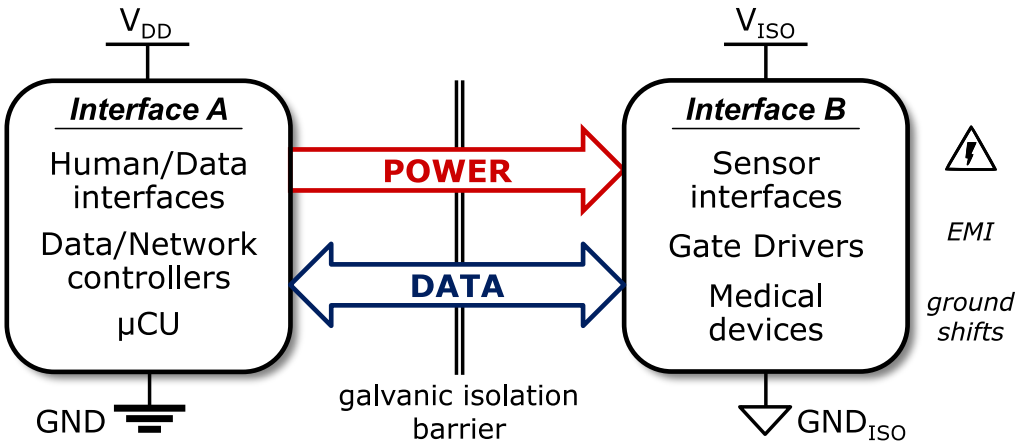


Figure 1.1: Typical applications requiring galvanic isolation.

two interfaces (A and B), which can have different ground potentials (i.e., GND and GND_{ISO}), exchange power and/or data through a galvanic isolation barrier. However, while data communication can take place in both directions, energy is usually transferred only from interface A to B, thus providing an auxiliary power supply to the circuits on the isolated side.

Typically, interface A is called user interface or low-voltage side (e.g., human/data interfaces, data/network controllers, micro-controller, etc.), whereas interface B is the isolated interface or high-voltage side (e.g., sensor interfaces, gate drivers, medical devices, etc.). The latter usually operates in harsh, noisy or high-power environments subjected to lighting strikes and hazardous voltages that can endanger the user interface. Therefore, galvanic isolation assures safety of human operators and protects from damages expensive and sensitive circuits within the user interface, while preserving the proper system operation in presence of ground shifts.

The wide range of applications have made galvanic isolators (or simply isolators) an interesting research topic in the course of the last decades. As

far as low-power applications are concerned, the research is pushing towards low-cost miniaturized systems based on micro-scale isolation barriers, either using inductive or capacitive transfer techniques, to replace traditional isolators based on expensive and bulky solutions (i.e., optocouplers for data transmission and discrete transformers for power transfer).

This chapter introduces the main topic of this dissertation that are fully-integrated dc-dc converter with basic and double galvanic isolation. The different degrees of isolation and the new safety standards specifically developed for such highly-integrated semiconductor isolators are discussed in the next section. Then, some example of low-power applications exploiting galvanic isolators are reported in section 1.3. The various isolation approaches for power and data transfer along with the state-of-the-art are presented in section 1.4. Finally, the main outcomes of this work are summarized in section 1.5.

1.2 Safety standards and degree of isolation

Whenever galvanic isolation is used to enable the system to function properly, but not necessarily to serve as a barrier against shock, it is called functional isolation. If human beings or costly and sensitive circuits are involved, a functional isolation is not sufficient to guarantee safety and protection against electrical shocks during long-term system operation.

Safety reasons are the most important motivations for using galvanic isolation, since dealing with high voltage capability of measurement instrumentations or medical appliances, users can be subjected to lethal electric shocks

or burns. Also, overvoltages arising from lighting strikes during a storm and high-power switching devices can threaten health of human operators. Every year electricity causes thousands of injuries and hundreds of deaths [2], then it should not be underestimated. A severe electrical shock can cause ventricular fibrillation and cardiac arrest. Shocks and burns of varying degrees of severity are the most common injuries, while others can result from an electric current that acts as a trigger initiating a chain reaction of mishaps, including involuntary muscle reaction.

Table 1.1: Thresholds for continuous ac current and their effects.

Physiological effect	**Reaction**	**Threshold for continuous 15 to 100-Hz current (mA)**
Involuntary muscular reaction	Perception level, tingling sensation	0.5
Inability to let go	Painful shock, freezing current	10
Ventricular fibrillation	Heart rhythm affected, death may occur	35

The effects of current flow through a human body are a function of the magnitude of the current, the human body's resistance, and the duration of time. As shown in Table 1.1 from [3], even low currents can cause injury, and 100 milliamps flowing through the body for only two seconds can cause death. Coupling high currents with extra-low voltages can also cause severe injuries.

Safety standards limit voltage, current, and transient levels through the various isolation techniques. They have been developed both at the component and system level, thus providing general rules for specifications and testing of isolators and electrical systems employing isolation.

Over time, national and international standards were developed. Some

Table 1.2: System-level standards relevant to applications requiring isolation by market and region.

	Household	**Industrial**	**Information technology**	**Measurement and control**	**Medical**	**Telecom**
International	IEC 60065	IEC 60204	IEC 60950	IEC 61010-1	IEC 60601	IEC 60950
Germany	VDE 860		EN 60950	VDE 410/0411	VDE 0750	VDE 0804
USA	UL 60065	UL 508, UL 60947	UL 60950	UL 61010	UL 60601	UL 60950
Canada		CSA 14-10	CSA 60950	CSA 61010	CSA 601	CSA 60950

examples of commonly used system standards are reported in Table 1.2. System-level national regulations are defined by regional bodies, such as Verband Deutscher Elektringenieure (VDE), Underwriters Laboratories (UL), and Canadian Standards Association (CSA), for Germany, United States, and Canada, respectively. Whereas international agencies such as the International Electrotechnical Commission (IEC) and the European Norms (EN), define the international standards. However, certification requirements can vary across the different regions of the world even when the same safety standards are referenced [4], though national and international bodies are working to simplify the certification process, reducing the complexity caused by the high number of standards.

System standards define the different isolation characteristic of the whole system, thus giving a corresponding safety level. The most important concept behind these system-level standards is the classification of the isolation degree in an electrical system, i.e. functional, basic, double and reinforced [5], [6], whose incremental differences are briefly summarized in Fig. 1.2. As discussed at the beginning, a functional isolation does not protect the user but only guarantees the proper function of the system. On the other hand, a basic isolation provides an adequate protection against electrical shocks, thanks

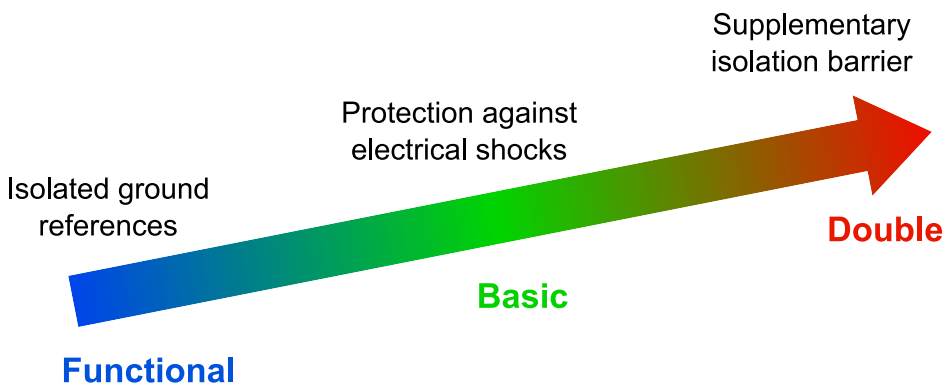


Figure 1.2: Isolation levels and main additional features.

to insulation barrier able to withstand voltage differences of several kilovolts. A higher level of safety is required when human beings are involved, which is achieved by adding a supplementary insulation barrier for redundancy. This level is called double isolation. Indeed, such additional barrier continues to provide isolation in even if the first one fails, thus improving the protection of the user from potentially lethal shocks. The straightforward way to achieve double insulation is by cascading two basic-insulation systems, but this increases costs and complexity, while limiting the performance of the system. To make systems compact and save cost, it is desirable to have only one level of isolation that has the required electrical strength, reliability and shock protection of two levels of basic isolation. Therefore, an additional degree of isolation has been standardized, which is called reinforced isolation. Double isolation is a widespread approach to achieve reinforced isolation [7], which is the higher level of isolation available in commercial products.

For a given application, system designers must choose the insulation characteristics of each component to meet system-level standards. In this approach isolation specifications are defined down to the single device by ad-

ditional component-level standards. These certify that a digital isolator component meets particular safety requirements, though they do not guarantee the isolation level of the overall system. Commonly adopted component-level standards are:

- IEC 60747: Semiconductor Devices—Part 1: General
- UL 1577: Standard for Optical Isolators
- VDE 0884-10: Semiconductor Devices—Magnetic and Capacitive Coupler for Safe Isolation

The IEC 60747 and UL 1577 standards were specifically written for optical communication across an insulation barrier, thus defining isolation specifications and testing paramenter of optocoupler devices. In the last decade modern digital isolators based on micro-scale magnetic and capacitive isolation barriers have been developed, overcoming the opto-isolator technology in terms of cost and performance. Then, the VDE 0884-10 standard has been released in 2006[1], which is specifically addressed to highly integrated transformer-based and capacitive isolators.

These standards describe several parameters and testing methodologies to classify the isolation characteristic of the component. Some of the most important parameters will be reported hereinafter.

The maximum transient isolation voltage (V_{IOTM}) and the maximum repetitive voltage (V_{IORM}) are parameters defined by the standards IEC 60747-5-5 and VDE 0884-10. V_{IOTM} is defined as the peak transient voltage that

[1] A more recent version has been recently released in 2017.

the isolator can handle without breaking down and measures the ability of an isolator to handle high voltages across the isolation barrier for very short periods of time. On the other hand, V_{IORM} is defined as the maximum repetitive peak voltage that the isolator can withstand and tests the ability of an isolator to handle high voltage across its barrier throughout its lifetime. These two parameters are measured together and a failure of the device during the testing phase is checked by means of a partial discharge test, which looks for localized discharges inside the insulation indicating the degradation of the such layer due to tiny imperfections[2] [8]. Two testing methodologies are defined by the VDE 0884-10 standard, which are Method A and Method B1. The Method A is a destructive test. It must be passed by a family of devices to obtain the certification by the aforementioned standard. This method combines transient overvoltage and partial discharge tests as illustrated in Fig. 1.3. Being a destructive test, the isolator is stressed at V_{ini}=V_{IOTM} for a t_{ini} as long as 60 seconds. A following partial discharge test is carried out at a V_{m} of 1.6 times V_{IORM} for a t_{m} of 10 seconds. Since high values of t_{ini} and t_{m} are used, safety level of devices could be compromised. Consequently, all devices subjected to this test (even those that pass it) are thrown away.

On the other hand, the Method B1 is used during production manufacturing. Every device must pass this test before being released to the market. As shown in Fig. 1.4, during the process, the isolator is stressed at V_{IOTM} for only one second, with a following partial discharge test at 1.875 times V_{IORM} for one more second. Indeed, such low values of t_{ini} and t_{m} are chosen to do

[2]On the contrary, standards such as the UL 1577 test a weaker condition, which allows a partial discharge in the insulation layer.

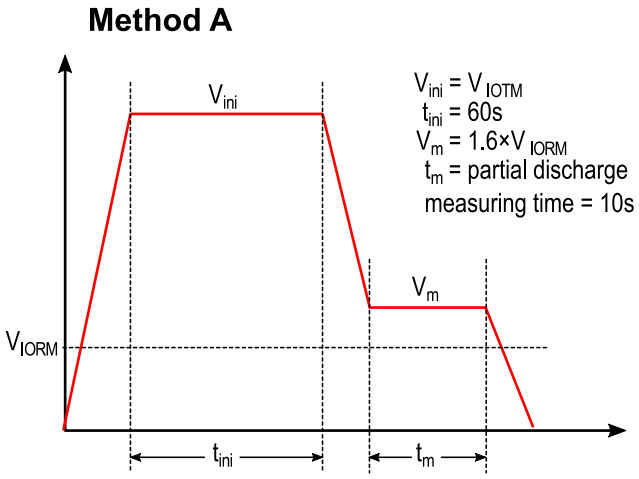


Figure 1.3: Simplified Method A test profile.

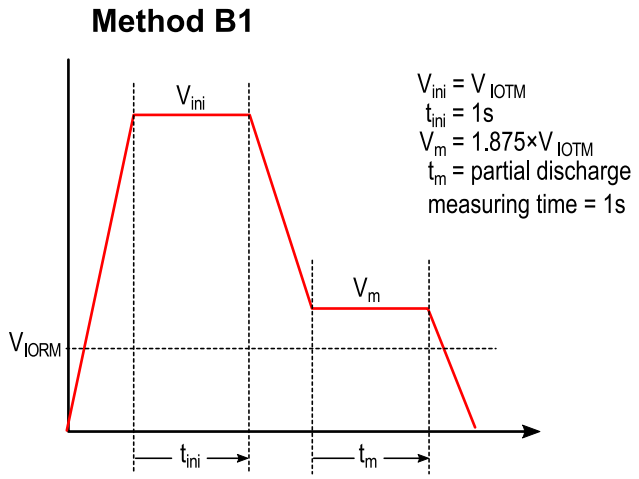


Figure 1.4: Simplified Method B1 test profile.

not deteriorate the isolation capability of devices.

Another specification defined by IEC 60747-5-5 and VDE 0884-10 is the maximum surge isolation voltage (V_{IOSM}) that quantifies the ability of the isolator to withstand very high voltage impulses of a certain transient profile, which can arise from indirect lightning strikes or faults. The adopted surge test profile is shown in Fig. 1.5.

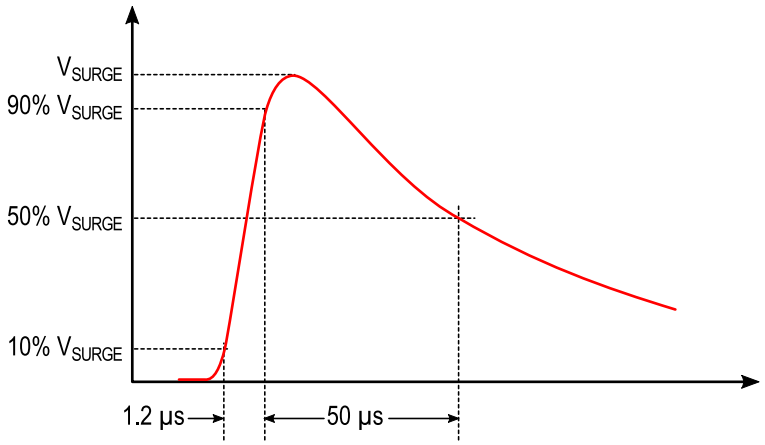


Figure 1.5: Simplified surge test profile.

To claim a certaing V_{IOSM} an isolator must pass the surge test at a peak voltage of 1.3 times V_{IOSM} for basic isolation, and 1.6 times V_{IOSM} for reinforced isolation. However, an isolator can be called reinforced at the component level, only if it passes the surge test with a V_{SURGE} greater than 10 kV, though higher surge pulses are commonly used during test production of reinforced isolators.

The distance through insulator (DTI) is a further specification that was introduced before high-quality insulation layers were available. It defines the smallest distance between the two voltage domains in the isolator, internal to the isolation package. In optocouplers a high DTI (e.g. usually hundreds of micrometers) was a measure of higher quality but with the new isolation materials and the introduction of highly-integrated magnetic and capacitive isolators, high performance can be obtained even with DTI of several micrometers.

It is also worth noting that many component standards and system-level regulations as well, often pose specific requirements on the clearance (i.e.

distance through air) and creepage (i.e. distance along the surface) of the isolator's package [5], as defined in Fig. 1.6, and its fabrication materials.

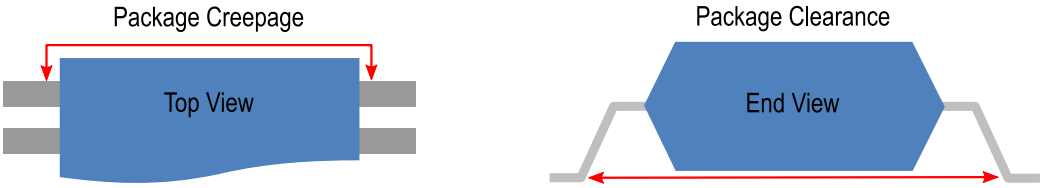


Figure 1.6: Definition of clearance and creepage.

1.3 Applications

Galvanic isolators for power and data transfer are widely used in many applications. Often they are a fundamental component of the system, enabling its proper function. In other cases their use is made mandatory by regional and international agencies for safety purpose. This section briefly shows some common low power applications of galvanic isolators, focusing on those requiring an auxiliary power supply for the isolated interface.

1.3.1 Wireline networks

Wireline networks are widely used in applications such as industrial process control, power supply regulation and point-to-point communications between computers [9]. Typically, data communication is supported by various types of physical networks, such as RS-232, RS-485, and the Controller Area Network (CAN). These networks are characterized by the long distances between the interconnected systems, which can reach up to 4000 meters for the RS-485 networks [10]. Since each node has its own power supply, a

ground potential difference (GPD) can exist between them. Indeed, when long distances of the ground wires are involved, it is most unlikely that interconnected systems have the same ground reference. Therefore a ground current will flow between them, generating a GPD. Galvanic isolators are exploited to break ground loops, thus avoiding ground currents that can cause signal distortion and data loss. In addition they improve the safety of the system, by protecting each node from possible damages caused by high-voltage transient.

As shown in Fig. 1.7(a), when two devices (A and B) are connected to different ground potentials and a third ground wire is used to exchange power or informations between them, they form a ground loop. These multiple ground paths act as a large loop antenna, which can induce currents into the system by picking up noise from the environment [11]. Such noise can can come from different sources, such as the 50 Hz/60 Hz magnetic field of the ac power distribution, motor switching or other events that cause a rapid change in the local ground potentials. For instance, when a local ground shift occurs in B, it will be superimposed to the signal received from A. Consequently, such unexpected overvoltage will cause severe damage to the system B. As shown in Fig. 1.7(b), galvanic isolators overcome this problem by breaking the ground loop. When both power and data are transferred from A to B, all signals and power supply lines must be isolated. Therefore an isolated dc-dc converter is used to provide isolation on the supply power of each node, while achieving a single ground reference for the whole system.

Typically, low power wireline transceivers for RS-232, RS-485 and CAN bus networks operate with a supply voltage from 3.3 to 5 V and a current

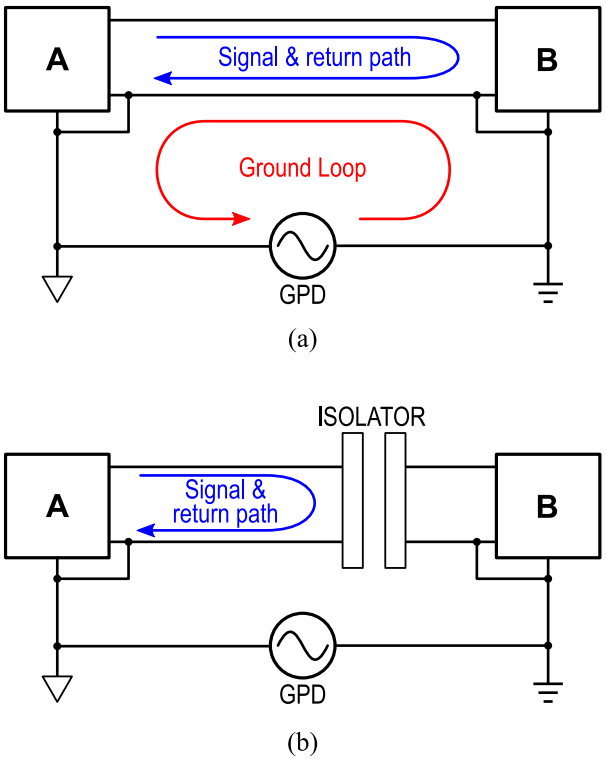


Figure 1.7: Ground loop in wireline networks. Without (a) and with (b) a galvanic isolator.

consumption up to tens of milliamps [12]–[14]. Therefore, an isolated power supply providing around few tens of milliwatts of output power, working with supply voltages from 3.3 to 5 V is highly desirable to simplify wireline network's design.

1.3.2 Current monitoring

The measurement of current flow is required in a wide range of applications, such as hybrid electrical vehicles (HEVs), electrical vehicles (EVs) and power line monitoring.

The number of EVs and HEVs is growing very fast during the last years.

This growing is encouraged by government organizations such as the EVI (a multi-government policy forum), which is working to reach 20 million EVs across the worlds in 2020 [15]. In this scenario an accurate energy monitoring is considered of utmost importance to estimate state of health (SOH) and state of charge (SOC) of the battery in the vehicle. Typically, to monitor the SOH and SOC, several voltage, current and temperature sensors are involved. Moreover, to ensure safety, automotive specifications call for twice the isolation required for simple functioning, thus automotive ICs must be manufactured to provide this level of protection, known as reinforced isolation [16]. On the other hand, domestic power line monitoring is regulated by international agencies, which have made galvanic isolation a fundamental safety-requirement for every device in order to be introduced to the market. Therefore, after these considerations, a high demand of galvanically-isolated current-monitoring systems is expected in the next decades.

Various methods can be used to measure the current flow in a conductor [17], e.g. Rogowski coil or current transformer, but the simplest one is based on the shunt resistor. A simplified architecture of a current monitoring system based on this approach is shown in Fig. 1.8. Typically, a resistor R_{shunt} of few hundreds micro-ohms is exploited to measure current flows up to hundreds of amps. The value of the current I_{shunt} that flows through R_{shunt} is obtained indirectly, measuring the voltage across the resistor and exploiting the Ohm's law.

An analog-to-digital converter (ADC) is typically exploited on the high-voltage side to send digital data information across the galvanic isolation barrier. Therefore, an isolated dc-dc converter of only few milliwatts is re-

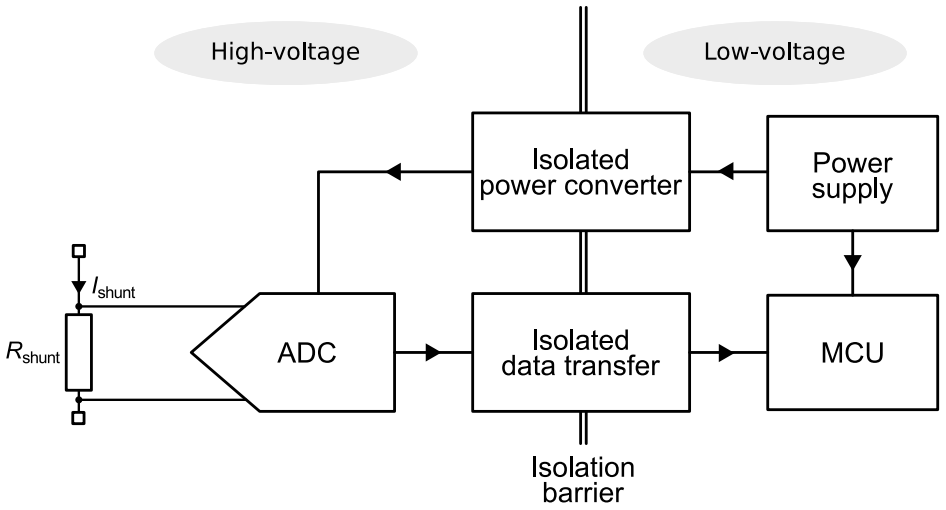


Figure 1.8: Simplified current-monitoring system architecture based on the shunted-resistor technique.

quired to provide supply power to the ADC and other circuits on the isolated side. Moreover, a digital data isolator, whose data communication speed depends on the particular application, is exploited to transmit the digital data towards the micro-controller unit (MCU) on the low-voltage side.

1.3.3 Gate drivers

The increasing of environmental pollution of the last decades has led to a global effort to reduce carbon emission. To this purpose, renewable energy sources, such as photovoltaic plants and wind turbines, are preferred over coal-fired energy plants, while EVs and HEVs are becoming more popular on the roads. All these clean alternatives entail power conversion systems that can handle power from hundreds of watts to several kilowatts. A high-efficiency performance is highly desired at such high power levels. Therefore, a minimum value has been made mandatory in the world's largest industrial

regions including Europe, U.S., Japan and China [18]. Moreover, a galvanic isolation barrier between low-power control circuits and high-voltage ones is required to ensure safety and protect sensitive control circuits.

Modern power conversion systems rely on switched-mode power electronics (SMPE) to achieve high-efficiency power conditioning and control. Typically they exploit power MOSFET and IGBT-based inverters, which transform a rectified input voltage into a variable frequency voltage that drives a motor. A commonly adopted solution is represented by the half-bridge bridge topology, which is based on two N-type power switches [19]. As shown in Fig. 1.9, it requires additional gate driver circuits that minimize conduction loss and switching time of the power switching devices, while avoiding destructive conditions that occur when both devices, Q_1 and Q_2, are conducting at the same time.

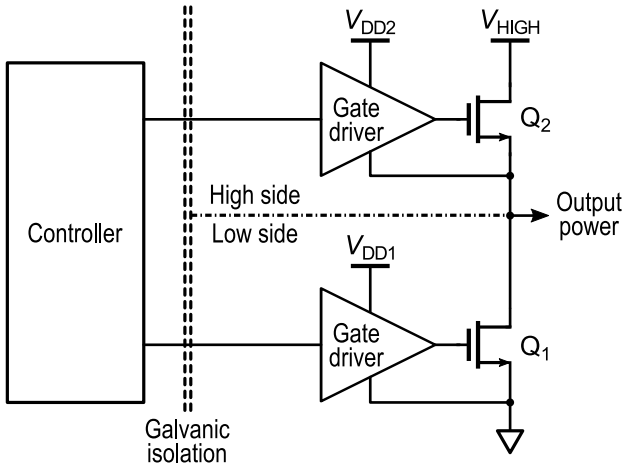


Figure 1.9: Simplified half-bridge circuit.

The gate drivers on the low-side and high-side must be supplied by the voltages V_{DD1} and V_{DD2}, respectively. Indeed, to drive properly the power switch Q_2, the gate driver on the high-side must have a supply voltage V_{DD2}

very close to V_{HIGH}, which typically is several hundreds of volts. To simplify this task, traditional solutions for high-side power supplies rely on the bootstrap capacitor technique, which poses limitations on the start-up, the duty cycle, and the maximum off time for the high-side switches of the converter. Besides , it does not completely eliminate the risk for latch-up even in the low-side gate-driver, which arises when the output node of the power switch goes below ground during inductive spikes or free-wheeling diode conduction. These limitations and the risk of latch-up can be eliminated by providing to each gate driver an auxiliary galvanically-isolated supply voltage, while connecting each gate driver's ground to the source of the corresponding power switch. As a result, galvanic isolation is provided not only between controller and gate drivers but also between the low-side and high-side.

The minimum power supply required by a gate driver can be expressed as

$$P_{\mathrm{GD}} = P_{\mathrm{DR}} + P_{\mathrm{G}} \tag{1.1}$$

where, P_{DR} is the power consumption of the driver and P_{G} is the power required to periodically turn on and off the power switch. Usually, P_{DR} is few milliwatts and it is negligible with respect to P_{G}. For power MOSFETs or IGBTs the input impedance is capacitive, hence P_{G} can be estimated as the power required to charge and discharge its gate capacitance C_{G} at the switching frequency f_{SW}, thus

$$P_{\mathrm{G}} = C_{\mathrm{G}} \cdot \Delta V_{\mathrm{G}}^2 \cdot f_{\mathrm{SW}} = Q_{\mathrm{G}} \cdot \Delta V_{\mathrm{G}} \cdot f_{\mathrm{SW}} \tag{1.2}$$

where, ΔV_{G} and Q_{G} are the voltage swing provided to the gate and the charge required to turn on the device, respectively.

State-of-the-art gate-driver integrated circuits can handle peak currents of few amps while switching at $f_{\mathrm{SW}} < 1$ MHz. Main applications are 600/1200V inverters, UPS equipment, solar inverters, and motor drivers in hybrid and electric vehicles [20], [21]. Common IGBTs can require a gate charge of about hundred nano-coulombs and a voltage swing higher than 6 V [22]. According to such specification a galvanically-isolated dc-dc converter with an output power of few hundreds of milliwatts with an output voltage higher that 6 V can be exploited as auxiliary power supply for isolated gate drivers.

1.4 State-of-the-art

Recently, the miniaturization of galvanic isolators has gained a lot of attention among the academic and industrial environments, thus becoming an interesting research topic. As a result, the bulky and costly traditional solutions based on optocouplers and/or discrete transformers are going to be replaced in the near future by highly-integrated low-cost semiconductor isolators.

In the last years, several data transfer systems with galvanic isolation, realized with silicon technologies, have been proposed. They exploit different techniques to perform galvanic isolation, such as RF links [23], capacitive [24] and magnetic coupling [25], [26]. As far as the power transfer is concerned, several solutions addressed to low power applications have been proposed as well. However, in this case galvanic isolation is mainly performed by

magnetic coupling. Consequently, the miniaturization of the inductive components (e.g. the isolation transformer) has become the main concern of such systems. Various approaches have been proposed to improve the integration level, such as post-processing devices and magnetic layers. However, some require uncommon processes and technologies [27], which increase the complexity and cost of the system. Recently, highly integrated (i.e., made up of only two chips) dc-dc converters with basic 5-kV galvanic isolation were also demonstrated for power levels ranging from about 20 mW to 1 W [28]–[30]. They exploit on-chip transformers, which guarantee a high galvanic isolation rating thanks to the excellent field strength of silicon dioxide.

This section shows the advance made in galvanic isolators throughout the past years, focusing on the most recent approaches to implement micro-scale galvanic isolation barriers.

1.4.1 Optocouplers

Optocouplers are used to transfer electrical signals between two isolated circuits exploiting light near the infrared region. They have been the default choice to implement data transfer with galvanic isolation since the end of 1970s, when they were introduced. Although they are still part of the isolators market, in the last decade they are being supplanted by more reliable and cost-effective solutions.

The typical internal structure of an optocoupler is shown in Fig. 1.10(a), while an x-ray scan of a device [31] is shown in Fig. 1.10(b). The structure basically consists of two metal frames that house an infrared light emitting

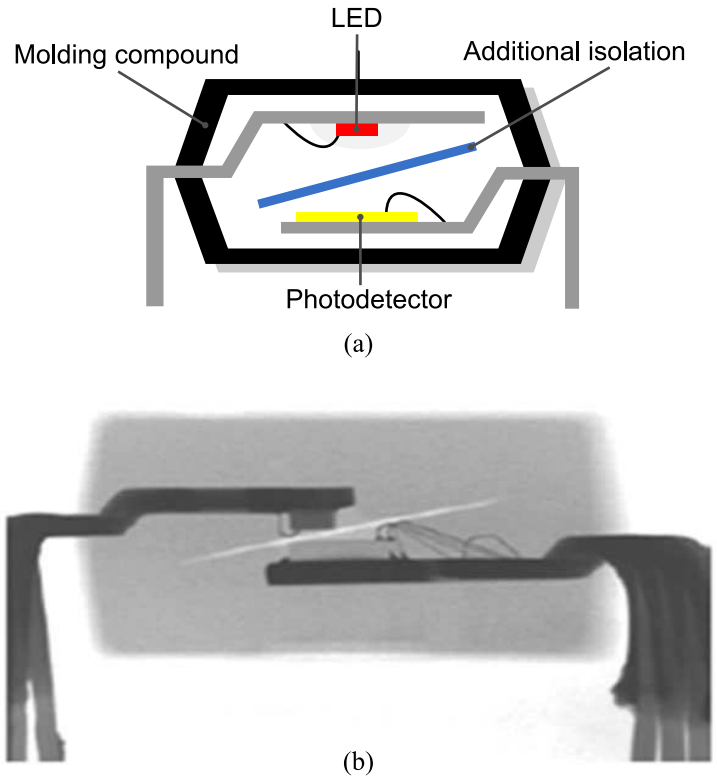


Figure 1.10: (a) Typical optocoupler structure and (b) X-ray cross-section.

diode (LED) and a photo-sensitive device that detects the light beam (photodetector), respectively. These are enclosed in a plastic package that is coated with a molding compound, which determines the isolation breakdown voltage of the device but also shields it from external light sources and mechanical stresses. The LED and photodetector are separated by a physical gap that depends on the isolation rating of the device, being typically greater than 400 μm for high-end products. This gap can contain one or more additional transparent isolation layers to improve isolation performance while reducing input-output coupling capacitance [32] . However, increasing the complexity of package makes manufacturing more difficult, thus rising the cost of a device.

Optocouplers can be used to transfer either analog or digital signals and present several advantages with respect to the old and bulky pulse transformers in terms of cost and size. A simplified schematic of a photo-transistor optocoupler is shown in Fig. 1.11. The main parameters that characterize

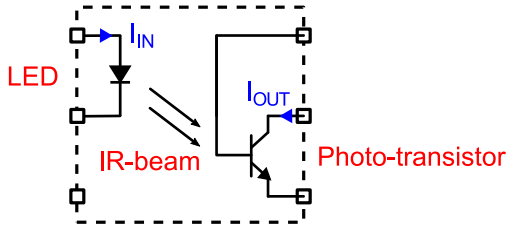


Figure 1.11: Simplified schematic of an optocoupler device.

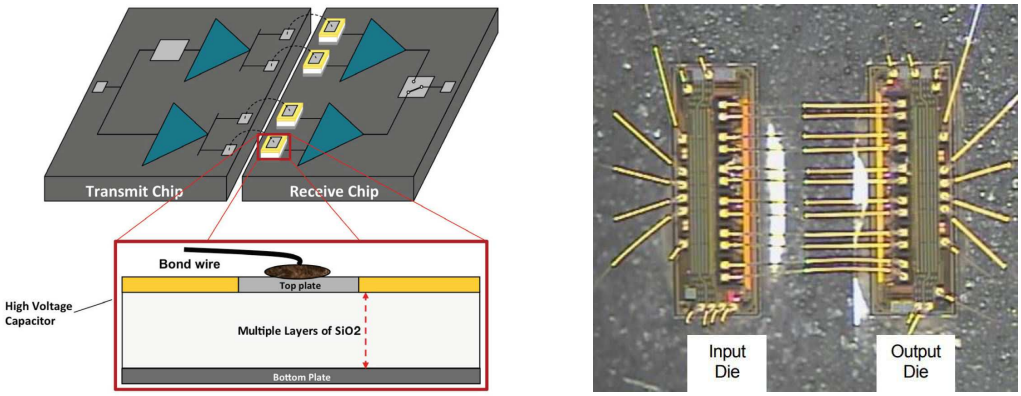
an optocoupler are the bandwidth and the current transfer ratio (CTR). The bandwidth depends on the biasing current of the photo-transistor and determines the speed of the data link. In state-of-the-art for a biasing current of ten milliamps, the maximum data rates can reach about ten megabits/s. On the other hand, CTR is the ratio between the output current, I_{OUT}, of the photo-transistor and the input current, I_{IN}, required to turn-on the LED. Since the CTR depends on the photo-transistor current gain β, it is affected by variability due to biasing current, temperature and process variations. These dependencies are accentuated by the aging degradation of the LED brightness, which is accelerated by the high working current level of the device. This leads to a trade-off between performance and lifetime of optocouplers, which makes more complex their design.

1.4.2 Capacitive isolators

Capacitive isolation exploits high-voltage capacitors as galvanic barriers. Although advanced technologies for the implementation of high-performance isolation capacitors have been proposed [33], the most diffused isolation approach in CMOS silicon technology exploits the inter-metal dielectric (IMD), i.e. silicon dioxide (SiO_2), to realize low-cost isolation capacitors that enable the mass production of fully integrated digital isolators.

Using silicon dioxide layers presents several advantages with respect to other technologies. Indeed, SiO_2 is known as one of the best dielectric insulator with a dielectric strength as high as 850 V/μm [33]. Consequently, high isolation performance can be achieved using relatively thin SiO_2 layers. Moreover, SiO_2 has been widely used by semiconductor foundries for decades, thus very high quality silicon dioxide layers with low defects per area can be easily realized. Since SiO_2 layers are available in most silicon back-ends, a high integration level (e.g. only two chips) can also be achieved, combining both CMOS devices and isolation barriers on a single die.

Capacitive isolation is widely used to implement digital data isolators. A typical arrangement of a state-of-the-art capacitive isolator [34] along with the cross-section of the high-voltage capacitor is shown in Fig 1.12(a). Two chips, i.e. a transmitter and a receiver, are attached on the top of the two respective metal frames. In this case, the receiver houses the high-voltage capacitors, which provide galvanic isolation. These are realized using standard metal layers for the top and bottom plates and several layers of thin-film SiO_2. The working principle is based on the amplitude modulation of a differ-



(a) (b)

Figure 1.12: (a) Typical capacitive isolator system with simplified cross-section of the high-voltage capacitor. (b) Photo of a six-channel capacitive digital isolator.

ential RF signal transmitted through the capacitors. Indeed, the differential approach increases the robustness against common mode disturbances, such as external RF interference. A photo of a capacitive digital isolator [32] is shown in Fig. 1.12(b). Thanks to the little area occupied by each isolated link, up to six data channels have been implemented within two chips. A great advantage of capacitive digital isolators is the low power consumption, typically only few milliamps in the state-of-the-art. In addition, a high common mode transient immunity[3] (CMTI) performance can also be achieved. These features make capacitive isolators a more reliable solution compared to optocouplers.

The state-of-the-art of capacitive digital isolators includes also systems with reinforced isolation [7], which can be implemented simply by series-connecting more isolation capacitors, thus increasing the overall breakdown

[3]The common mode transient immunity measures the ability of an isolator to withstand rapid voltage shifts, in the order of several kV/μs, between the grounds of the two interfaces.

voltage of the isolation barrier. Fig. 1.13 shows the photo of a multi-chip implementation of an isolated $\Delta\Sigma$ modulator [35], where two isolation barriers (i.e., double isolation) have been used to achieve the reinforced isolation level.

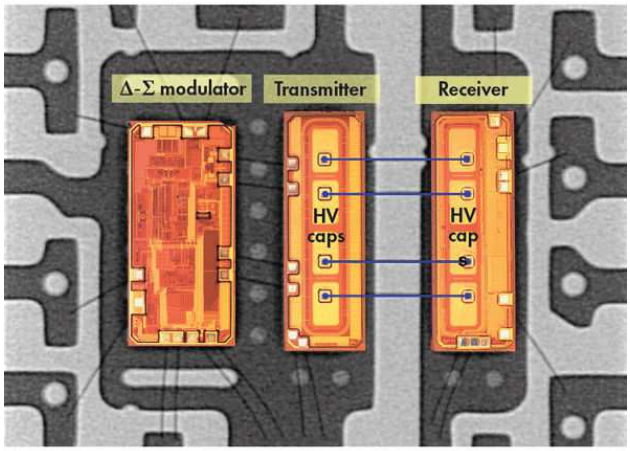


Figure 1.13: Photo of a $\Delta\Sigma$ modulator with reinforced galvanic isolation.

As far as power transfer is concerned, capacitive isolation presents several limitations. Fig. 1.14 shows how the ac input power is transferred through the capacitive isolation barrier, capacitors C_{ISO}, towards the parallel RC load impedance, $R_{\mathrm{L}}//C_{\mathrm{L}}$. Indeed, the ac output voltage, V_{OUT}, will be lower than

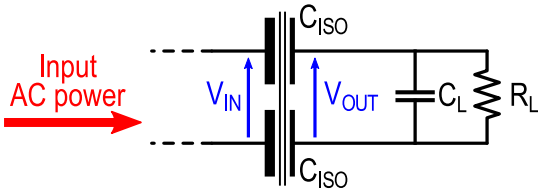


Figure 1.14: Voltage partition in capacitive power transfer.

the input one, V_{IN}, due to the capacitive partition between C_{ISO} and C_{L}. This voltage partition causes a reduction of the ac power that is transferred to R_{L},

thus leading to a low efficiency for the isolation barrier. Such problem can be overcome increasing the value of C_{ISO}, but this is often in contrast with the silicon area specification, since high-voltage isolation capacitors usually have very low specific capacitance.

Furthermore, on-chip isolation capacitors exhibit heavy parasitics, which determines the power loss of the isolation barrier. Typically, as shown in Fig. 1.15 the IMD that separates the bottom and top metal plates is much

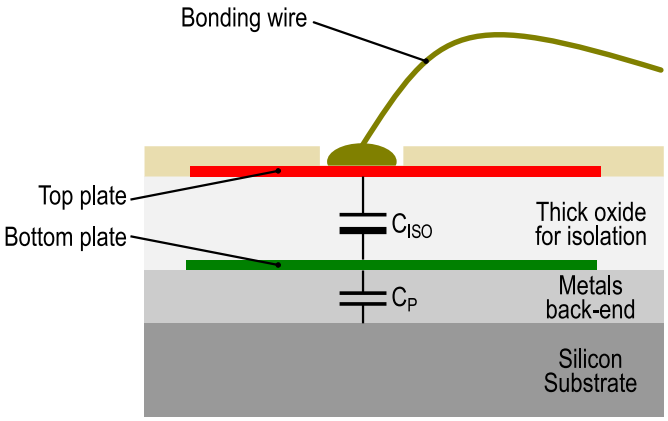


Figure 1.15: Bottom plate parasitic (C_{P}) of on-chip isolation capacitor (C_{ISO}).

thicker than the distance of the bottom plate from the silicon substrate. Therefore, differently from on-chip low-voltage capacitors, they have a ratio $C_{\mathrm{P}}/C_{\mathrm{ISO}}$ greater than one, which must be carefully considered during the design of the capacitive power transfer system.

Recently, a dc-dc converter based on integrated capacitive isolation has been proposed [36]. It achieves power and efficiency up to 62 mW and 50.7%, respectively, thanks to the subharmonic resonant approach, which avoids power efficiency degradation due to the bottom plate parasitics. However, the isolation rating of the system is only 1 kV, which is lower than the state-

of-the-art, and the value of the bottom plate parasitic is about the same of the isolation capacitor. Moreover, the system is not fully-integrated since resonances require an external high-Q inductor.

1.4.3 Magnetic isolators

Nowadays, highly integrated magnetic isolators based on inductive coupling are widely diffused. This is mainly due to possibility to implement both power and data transfer by means of transformers. A typical data transfer architecture is depicted in Fig. 1.16. As well as for capacitive isolators, it basically consists of a transmitter and a receiver, which exchange data information through a planar isolation transformer by using either ASK modulated RF signals or voltage pulses. The transformer can be housed in a standalone chip or can be placed within the transmitter or receiver die, thus achieving the highest level of integration (i.e., only two chips).

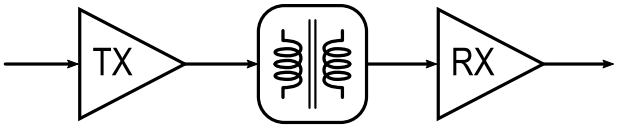


Figure 1.16: Typical architecture of a transformer coupled magnetic isolator.

The first highly integrated magnetic isolators were introduced by the company Analog Devices in 2001 with the iCoupler technology [37]. The iCoupler technology adopts micro-transformers realized with post processing steps to implement a multi-chip System in Package (SiP) solution. A cross-section of the iCoupler technology is shown in Fig. 1.17(a). Galvanic isolation up to 5-kVrms is performed by a 20-25 μm thick polyimide layer, which separates the two windings of the micro-transformer. The top coil of the transformer

exploits a 4 μm-thick electroplated Au layer, while the bottom spiral is realized on a standard IC top metal layer. A photo of a four-channel digital isolator realized with the iCoupler technology is shown in Fig. 1.17(b). State-

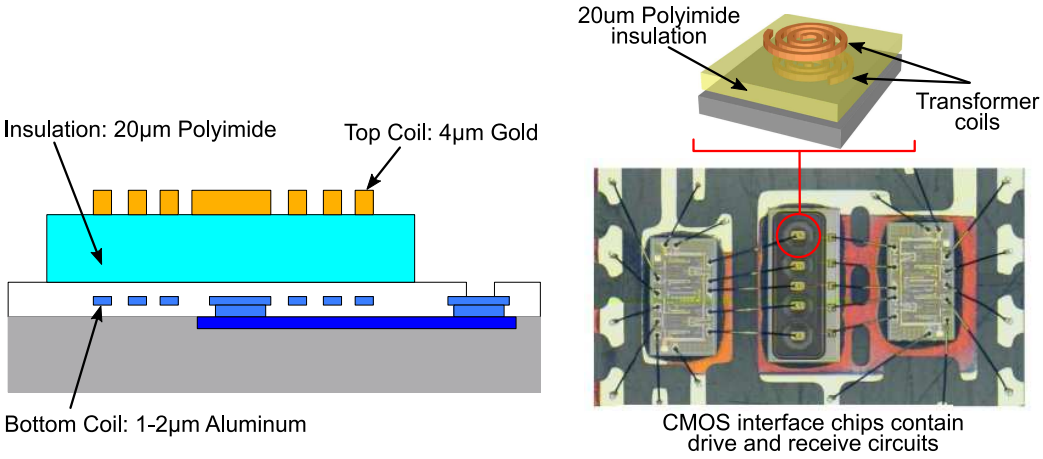


Figure 1.17: iCoupler technology. (a) Cross-section. (b) Photo of a four-channel digital isolator before packaging.

of-the-art transformer-based digital isolators have maximum data-rate up to 150 Mbs. Thanks to a lower parasitic capacitance between the two interfaces they also exhibit a better CMTI performance than capacitive isolators, though magnetic isolators require a more advanced technology.

The main advantage of magnetic isolators is surely the power transfer capability. Typical state-of-the-art system architecture for isolated power transfer is shown in Fig. 1.18. It consists of three main blocks. Firstly, a dc-ac conversion of the input power is made, then it is transferred through a transformer. Galvanic isolation barrier is provided by such transformer, which is typically realized on-chip or by post-processing steps. Finally, an ac-dc converter, i.e. a rectifier, converts back the ac power to the dc isolated

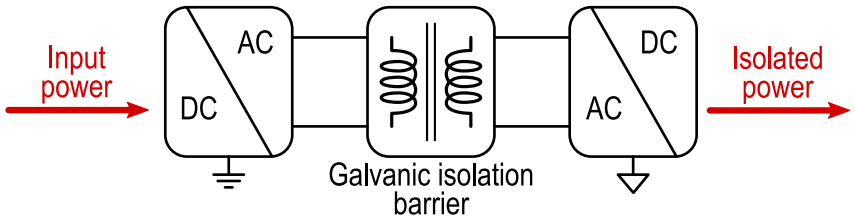


Figure 1.18: Typical state-of-the-art architecture of an isolated power transfer systems.

output power.

The first multi-chip SiP dc-dc converter with galvanic isolation was also proposed by Analog Devices in [38]. It adopts a micro-transformer realized with the isoPower technology, whose cross-section is shown in Fig. 1.19(a). It

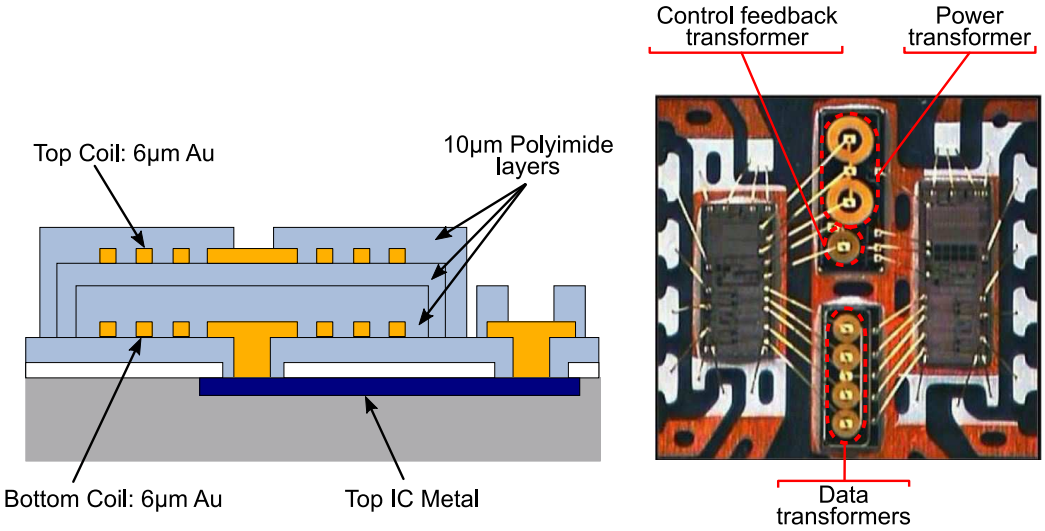


Figure 1.19: (a) Cross-section of the isoPower technology. (b) Photo of an isolated dc-dc converter with 4 isolated data links before packaging.

is worth noting that for power transfer applications both power transformer's coils require thick Au metals to achieve good efficiencies, thus increasing manufacturing costs. An interesting photo of an isolated dc-dc converter, is

shown in Fig. 1.19(b), which combines power and data transfer capability by adding isolated data channels within the same multi-chip SiP solution. Many products of this kind are already available on the market [39]. They have power levels ranging from tens to hundreds of milliwatts. Recently, an isolated $\Delta\Sigma$ converter with integrated power and data transfer, addressed to current monitoring applications, was proposed in [40], [41]. It provides about 10 mW of isolated dc power and 3 data channel for current/voltage readout. Differently from other approaches, it uses the same transformer for both data and control feedback signals, thus reducing the overall costs of the system.

One of the most important specification for an integrated dc-dc converter is the power density, i.e., the ratio between the output power and the overall area of the system. Indeed, micro-transformers realized with post-processing techniques do not lend themselves to high power density levels, since more than two chips are typically required to implement an isolated system. However, a different method for the realization of on-chip isolation transformers was introduced by STMicroelectronics in [42], [43]. Nowadays, only digital data isolators exploiting this technology are commercially available [20], but the power transfer feasibility was demonstrated by several fully-integrated systems with power levels ranging from 20 mW to 1 W [28]–[30].

The key of this technology is the possibility to implement both active devices and isolation transformers within the same die, thanks to a standard 0.35 μm-BCD process enriched with a thich-oxide module in the back-end-of-line (BEOL) that provides a 5-kV isolation rating between the two top metal layers. The scanning electron microscope (SEM) cross-section of the four metals back-end along with the photo of a 200-mW two-chips dc-dc

converter assembled on board [29] are shown in Fig. 1.20(a) and Fig. 1.20(b), respectively.

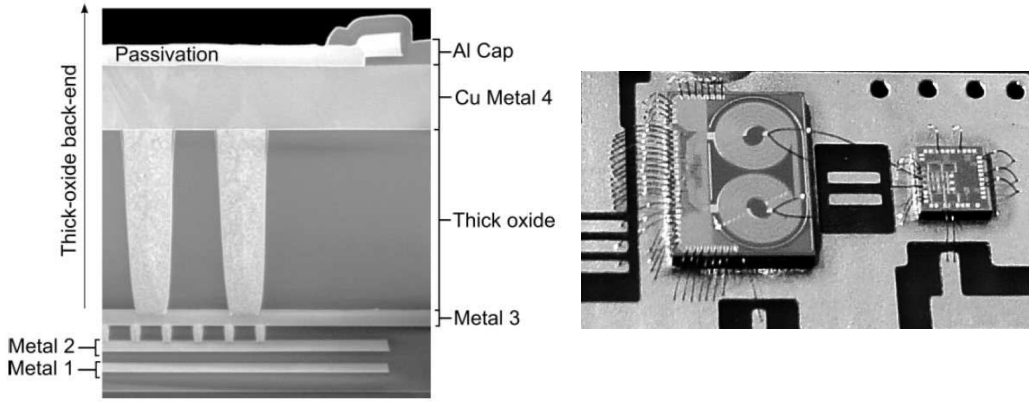


Figure 1.20: (a) SEM cross-section of the 0.35-μm BCD process metal stack with thick-oxide option. (b) Photo of a 200-mW isolated power transfer system assembled on board.

Indeed, the isolation transformer is implemented in the top metal layers, i.e., 0.9-μm Al metal 3 and 3.7-μm thick-Cu metal 4, leaving bottom metal layers for the underpass. Although this process exploits a weaker back-end with respect to the two 6-μm thick Au layers of the isoPower technology, competitive power efficiencies from 10% to 30% were obtained, along with the highest level of integration[4], i.e., only two chips. These systems benefit from all of the advantages of SiO_2-based isolators, thus representing a fully-integrated low-cost solution that reduce the complexity of the system.

In the last years research of magnetic isolators is pursuing the adoption of thin-film magnetic layers for the realization of high-quality micro-transformer. Indeed, such technology would lead to better performance, espe-

[4]The finite conductivity of the silicon substrate does not allow to implement an isolated system on a single die.

cially for integrated dc-dc converters, while improving EMI performance [44]. However, at the moment it is not as cost-effective as the standard techniques mentioned above.

1.5 Thesis overview

As mentioned in this chapter, a wide range of low-power applications would benefit from fully-integrated devices providing on-chip galvanic isolation. Both power and data communication are highly desired, however, isolated dc-dc converters present many design challenges while data isolators are already largely diffused. Indeed, implementing efficient fully-integrated dc-dc converters with galvanic isolation without exploiting any discrete or post-processing components is not a trivial task. To this purpose, during my permanence at the RF-ADC, a joint research group between the University of Catania and STMicroelectronics, my research activity was mainly focused on fully-integrated and isolated dc-dc converters for relatively low-power applications.

It is worth noting that this work is only focused on circuit and system design techniques to achieve fully integrated power transfer with currently available silicon technologies. Therefore, technology aspects regarding the implementation of on-chip galvanic isolation are not covered, since the whole technology platform was supplied and tested by STMicroelectronics.

In this section the adopted technology platform will be firstly presented. Then, the objectives of this work of will be pointed out highlighting the main results.

1.5.1 Technology platform

The technology platform is the same adopted in [28]–[30]. It is a 0.35-μm SOI-BCD technology that features both 3.3 V and 5 V CMOS transistors and several lateral-diffused MOS (LDMOS) devices for high-voltage capabilities. For the sake of clarity a simplified cross-section of the BEOL is shown in Fig. 1.21. Three Al metal layers with 0.45/0.55/0.9 μm thickness, respectively, and a 3.7-μm thick top Cu layer are available for routing. The process was enriched with a thick-oxide module of several μm of thickness, which has been tested by the technology provider for a 5-kV isolation rating [42]. Actually, it is used for the mass-production of several data isolators for gate drivers applications, providing on-chip galvanic isolation [20].

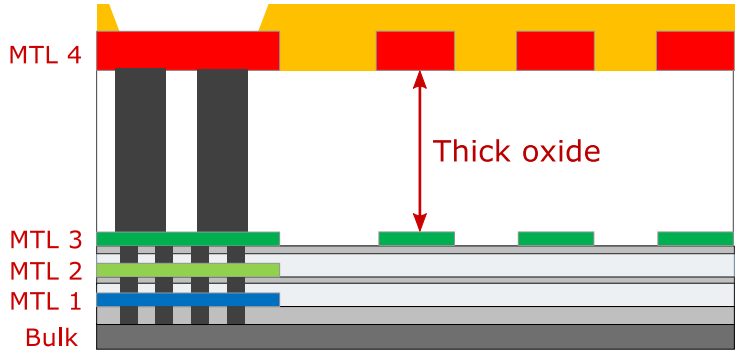


Figure 1.21: Simplified cross-section of the BCD back-end enriched with the thick oxide layer for galvanic isolation.

As shown in the cross-section of Fig. 1.21, the thick oxide is located between the third and fourth metal layers, thus all integrated passive components for galvanic isolation are implemented exploiting these metals. Bottom metals instead, are mainly required by transformer underpasses. It is worth noting that an SOI technology is not required for this work, as long as a

substrate with a low conductivity is available to implement on-chip passive devices.

1.5.2 Main results

The great advantage of the adopted technology is definitely the possibility to realize on-chip passive components (i.e., capacitors and transformers) with 5-kV of galvanic isolation. This allows to achieve the highest level of integration for galvanic isolators, thus the minimum number of chips. The main outcomes of this work are basically two fully-integrated dc-dc converters with different target of applications. They are briefly described hereinafter.

The first system is mainly addressed to gate driver applications. It is a 300-mW step-up dc-dc converter, providing a 10-V output voltage from a 5-V supply voltage [45]. The main objective of this system was to improve power density performance of [29], thus reducing the silicon area while increasing the output power level. Its basic architecture can be divided in three main blocks, as depicted in state-of-the-art of Fig. 1.18. A dc-ac converter (i.e., a VHF oscillator), an integrated three-windings transformer providing 5-kV of galvanic isolation and an ac-dc converter (i.e., a rectifier). This work introduces a novel hybrid-coupling approach for current-reuse oscillators, enabling a more compact implementation of the transformer and increasing the power density of the system.

Secondly, a 100-mW dc-dc converter with double galvanic isolation has been designed. As discussed in Section 1.4, only capacitive data isolators with integrated double isolation are currently available in state-of-the-art [7],

while power transfer is still hindered by the low efficiency of series-connected micro-scale isolation barriers. Therefore, the objective was to implement the very first fully-integrated power transfer system with two barriers of isolation providing 5-kV of galvanic isolation each. With a 3.3-V isolated output voltage from a 3.3-V supply, such system is addressed to many medical and sensor applications, especially those where human beings are directly involved. Indeed, this level of safety is mandatory and regulated by regional and international system standards. Furthermore, double isolation can be also used to achieve the highest level of isolation for semiconductor devices, i.e. reinforced isolation, which is certified by the standard [46]. A novel system architecture for the power link was introduced in [47] and presented in [48]. It is based on a resonant mode operation between the oscillator and the double isolation network. Moreover, output voltage/power regulation is provided by a novel control feedback loop, whose working principle was also applied to another galvanically isolated dc-dc converter with data communication [49].

These two systems are the main topics of the following chapters.

CHAPTER 2

A 300-mW fully-integrated power transfer system with basic galvanic isolation

2.1 Introduction

This chapter deals with the design and characterization of a fully-integrated power transfer system with basic galvanic isolation. It was targeted to produce an output power of 300 mW from a 5-V supply voltage. A step-up gain is also performed, thus achieving an output voltage of about 10 V. These specifications enable a wide range of low-power applications, e.g. gate drivers.

The system has many aspects that differentiate it from common dc-dc converters. It basically consists of a power oscillator and a rectifier, which

perform the dc-ac and ac-dc conversion, respectively, while a 5-kV isolation rating is provided by means of the on-chip air core transformer between the two blocks. Thanks to the available isolation technology, no post-processing steps are required such as in [38] and [50], thus achieving the highest level of integration (i.e., only two chips) and lower costs.

The converter uses an innovative power oscillator topology [29], which can be implemented in a standard 0.8-μm CMOS technology. It includes a novel hybrid-coupling approach that leads to a great improvement of system performance in terms of power density, by simply adding two capacitors and changing the transformer structure.

The chapter is organized as follows. Section 2.2 introduces the proposed dc-dc converter by focusing on the differences between standard CMOS power oscillators topologies. Section 2.3 deals with the modeling of the isolation transformer, a key block of the whole system. In Section 2.4 the adopted design procedure is described. Finally, experimental results for both dc-ac and dc-dc power conversions are reported in Section 2.5

2.2 System Description

The schematic of the galvanically isolated dc-dc converter is shown in Fig. 2.1. It consists of a power oscillator with on-chip isolation transformer (chip A) and a rectifier (chip B). The overall system is fully integrated in a standard CMOS technology provided by STMicroelectronics. A basic 5-kV galvanic isolation rating is provided by the three-winding isolation transformer, thanks to a thick oxide layer between top metal layers, i.e., a 0.9-μm

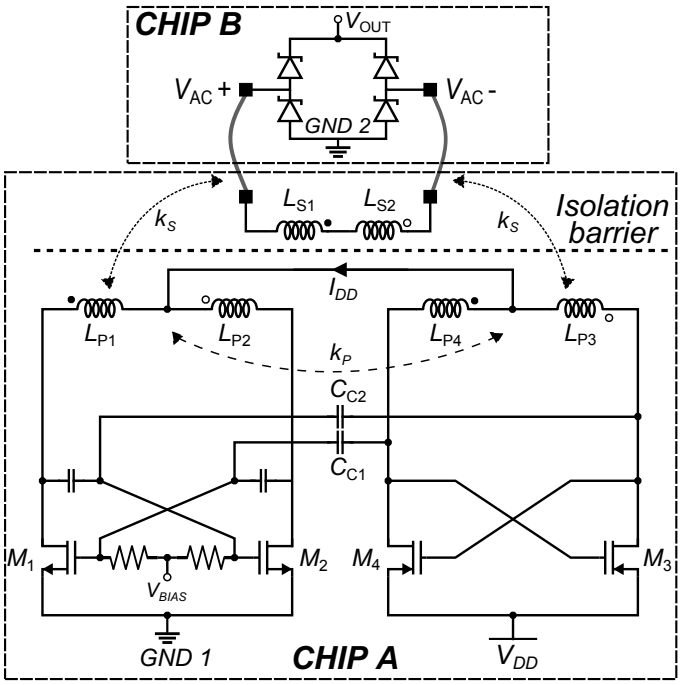


Figure 2.1: Schematic of the galvanically isolated dc-dc converter based on hybrid-coupled oscillators

Al metal 3 and a 3.7-μm Cu metal 4, which are used for the primary (L_{P}) and secondary (L_{S}) windings, respectively. The transformer is fully-integrated in the silicon process back-end without requiring additional post processing steps that would increase complexity and cost of the system.

The second chip houses a rectifier that performs efficient ac-dc conversion. It is based on high-voltage Schottky diodes with high-frequency operation capability. A classical full-bridge topology for the rectifier is crucial to achieve high efficiency while simplifying the design.

The system exploits an enhanced version of complementary cross-coupled oscillator topology, which takes advantage of current-reuse and power combining techniques, by means of the three-winding transformer, to achieve high power density and efficiency. As apparent, the same biasing current

flows through the pMOS and nMOS cross-coupled pairs, whereas the power signals produced by each oscillator are constructively combined together at the secondary winding of the transformer, $L_{S1,2}$.

Usually, transformer-based isolated power transfer systems exploit the well-known cross-coupled nMOS oscillator to achieve both high power and efficiency [51], owing to the high oscillation amplitude that can be easily reached [30], [38], [50]. However, such topology requires special devices, such as lateral-diffused or thick-oxide transistors, to sustain drain voltages that are typically two times higher than the voltage supply.

When only a standard CMOS technology is available, the complementary cross-coupled topology in Fig. 2.2(a) is the traditional solution for reducing power consumption while avoiding breakdown issues [52]. Fig. 2.2(b) shows a recent CMOS oscillator topology based on the current-reuse technique and output power combining [29], [53]. In this topology, the transformer guarantees frequency synchronization between oscillators by means of the primary-winding magnetic coupling, thus setting a lower bound for k_{PP} [54]. To this end, the isolation transformer in [29] exploits an interleaved configuration for primary windings. This choice limits both the power level and the power density, due to the poor performance of interleaved spirals (i.e., low Q-factor, low inductance density, and hence large transformer area). Specifically, despite the considerable efficiency improvement, the power density increment with respect to the traditional complementary topology is as low as 10%, which prevents adopting the transformer-coupled solution for high power levels due to the excessive silicon area involved.

The proposed converter solves this drawback thanks to a novel oscilla-

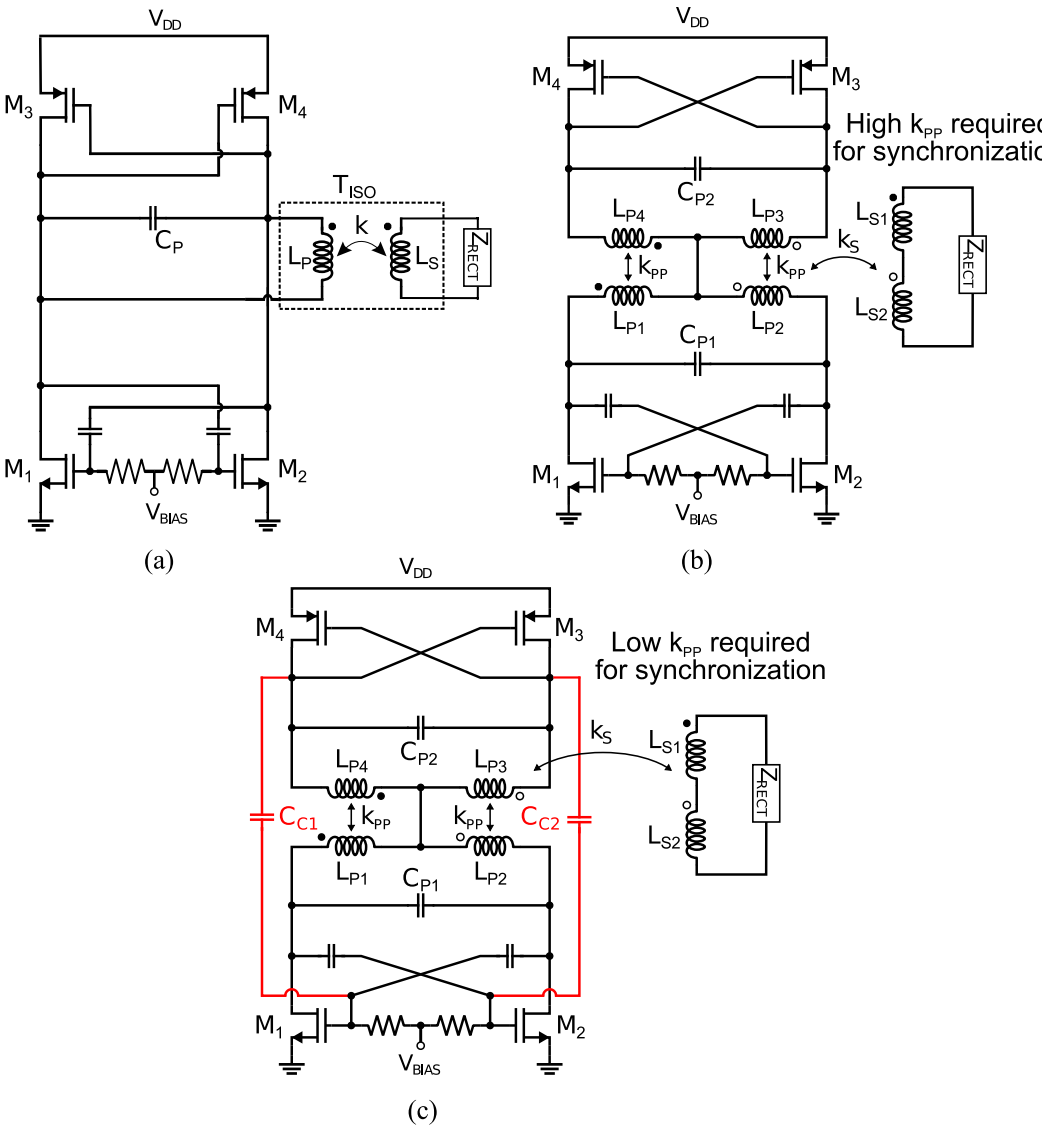


Figure 2.2: Transformer-loaded CMOS oscillators with the rectifier impedance Z_{RECT} . (a) Complementary cross-coupled oscillator. (b) Current-reuse transformer-coupled oscillator [29]. (c) Current-reuse hybrid-coupled oscillators.

tor coupling approach that enables an area-efficient three-winding isolation transformer with tapped primary coils. The circuit is shown in Fig. 2.2(c) for comparison purposes. Two capacitors $C_{\mathrm{C1,2}}$ are connected between the

oscillators to provide additional coupling. These capacitive links, along with the intrinsic magnetic coupling of the primary windings, k_{PP}, implement a hybrid coupling between nMOS and pMOS oscillators. For this topology, high magnetic coupling k_{PP} between primaries is not required to guarantee frequency synchronization, thus giving more freedom in the transformer structure that making possible to increase output power and power density. As a result, with the hybrid coupling approach (Fig. 2.2(c)), a magnetic coupling, k_{PP}, as low as 0.3 is enough to guarantee synchronization, while the inductive coupling in Fig. 2.2(b) would require a k_{PP} higher than 0.6.

Indeed, in such fully-integrated power converters, the most critical block to design is the isolation transformer. It requires an extensive use of electromagnetic (EM) simulations, but also it takes most of the silicon area of the converter, thus greatly contributing to the overall power efficiency and power density performance. Moreover, the non-linear interaction between dc-ac converter (i.e., oscillator and transformer) and ac-dc converter (i.e., rectifier) makes difficult pursuing the optimum design of the dc-dc converter. Therefore, an iterative co-design procedure between blocks is mandatory to maximize the overall dc-dc conversion performance, especially when on-chip transformer with low quality factors are involved. Once the circuit-level schematic of the system along with the transformer structure have been defined, an accurate scalable model of the transformer becomes crucial to streamline the design process. Then next section presents a lumped scalable modelling for three-winding isolation transformers with tapped primary coils that has been developed to this purpose.

2.3 Modeling of the isolation transformer

Modeling of on-chip transformers has always been an important research area in microelectronics. Actually, there is no easy way to estimate accurately the key electrical parameters (i.e., inductance, Q-factor, magnetic coupling and resonance frequency) of a transformer from its geometrical parameters. Indeed, an accurate evaluation of the power losses is crucial, since they determine the Q-factor of the transformer, thus its power efficiency in the dc-dc converter. The complex frequency-dependent phenomena, i.e., skin and current crowding effects, require EM simulations to be estimated with an adequate accuracy. As a result, developing a geometrically scalable modelling for the power transformer drastically reduces both computational resources and time required for an optimum design of this block, while enabling the co-design procedure that is detailed in the next Section.

The proposed power transfer system exploits a three-winding isolation transformer with tapped primary coils that is shown in Fig. 2.3. As apparent, it has a more complex structure compared to a typical stacked transformer used in class-D oscillators. It is implemented exploiting the four available metal layers in the adopted BCD technology that was presented in Sec. 1.5. The four inductors of the primary windings, $L_{\mathrm{P1-4}}$, are arranged by means of two tapped spirals, one for each secondary coupled coil, L_{S1} and L_{S2}, with a common terminal for the center tap. Underpasses are built in the bottom metal layers (i.e., metal 2 shunted to metal 1) and are only used to contact the inductor terminals and for the center tap. The secondary coils L_{S1} and L_{S2} are stacked on the primary coils using the top metallization and series

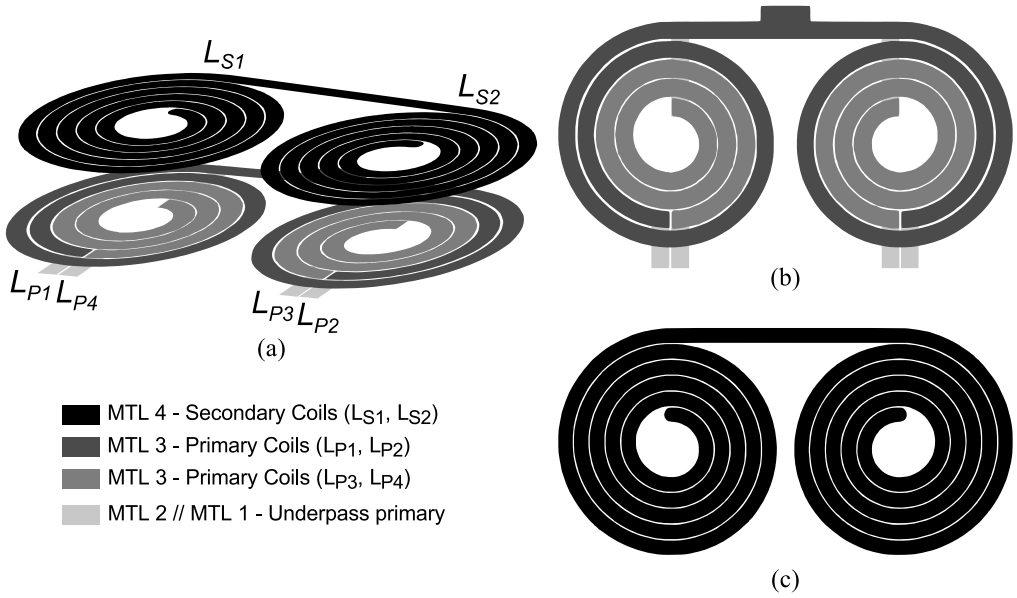


Figure 2.3: Three-winding tapped isolation transformer. (a) Three-dimensional view of the transformer. (b) Primary winding. (c) Secondary winding.

connected to build the secondary winding.

2.3.1 Geometrical constraints of the transformer

Due to the symmetry of the differential configuration, only half-structure has been modeled. Moreover, as reported hereinafter, the peculiar transformer configuration sets several constraints to its geometry, which simplifies the extraction of the model. For the sake of clarity, a detailed layout view of the single-ended transformer (half-structure) along with the main geometrical parameter (i.e., metal widths and spiral diameters) is shown in Fig. 2.4.

Firstly, the minimum value of metal width is bounded by the oscillator average current to comply with electromigration rules. On the other hand, the maximum width is limited by the silicon area and self-resonance frequency

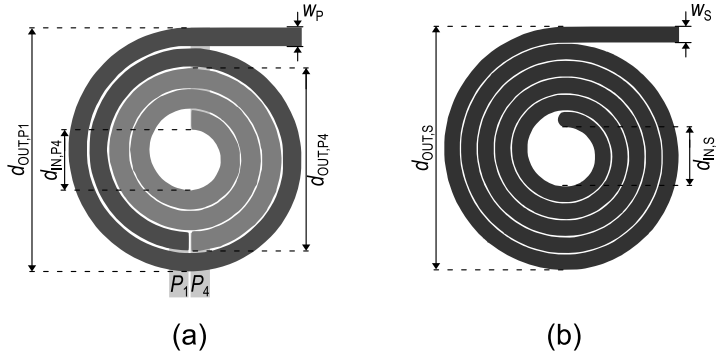


Figure 2.4: Single-ended layout views of the three-winding isolation transformer (a) tapped primary windings and (b) secondary winding.

constraint. Therefore, a metal width in range 50 to 150 μm were exploited for the model extraction, whereas the minimum spacing was set for primary and secondary coils (i.e., 1 and 5 μm, respectively) to improve the inductance density and thus minimizing the transformer area.

Primary inductance balance is important to pursue the power/efficiency performance optimization of coupled oscillators. Indeed, similar primary winding inductances allow comparable impedance for the nMOS and pMOS oscillators to be achieved. This condition makes easier power distribution equalization between coupled oscillators, which is crucial to maximize its performance. Therefore, only balanced tapped primary windings were considered for the model. Differently from the interleaved implementation [29], the tapped structure is not inherently symmetric, and hence, primary winding inductance balancing is not trivial. This drawback has to be overcome by a proper sizing of primary coil geometrical parameters, $L_{\mathrm{P1-4}}$. Specifically, inductances $L_{\mathrm{P1,2}}$ and $L_{\mathrm{P3,4}}$ were balanced by using the monomial expression by Mohan [55], reported in (2.1)

$$L = \alpha_0 \cdot d_{\mathrm{OUT}}^{\alpha 1} \cdot w^{\alpha 2} \cdot \left(\frac{d_{\mathrm{OUT}} + d_{\mathrm{IN}}}{2} \right)^{\alpha 3} \cdot n^{\alpha 4} \tag{2.1}$$

where L is the value of inductance, α_{0-4} are customized coefficients computed by least square fitting EM simulated data, and w, n, d_{OUT} and d_{IN} are the width, number of turns, outer and internal diameter of the coil, respectively.

Another geometrical constrain fix a relationship between the number of turns of primary coils, $n_{\mathrm{P1,2}}$ and $n_{\mathrm{P3,4}}$. Actually, to ease primary inductance balancing the number of turns of outer primary coils, $n_{\mathrm{P1,2}}$, was set a unit lower than $n_{\mathrm{P3,4}}$

$$n_{\mathrm{P1,2}} = n_{\mathrm{P3,4}} - 1. \tag{2.2}$$

Then, given the metal width ($w_{\mathrm{P}} = w_{\mathrm{P1,2}} = w_{\mathrm{P3,4}}$), the metal spacing ($s_{\mathrm{P}} = s_{\mathrm{P1,2}} = s_{\mathrm{P3,4}}$), and the number of turns ($n_{\mathrm{P1,2}}$, $n_{\mathrm{P3,4}}$) of primary coils, the value of the inner diameter of the inner primary winding ($d_{\mathrm{IN,P3,4}}$) that equals the inductance values $L_{\mathrm{P1,2}}$ and $L_{\mathrm{P3,4}}$ is numerically found by exploiting (2.1) along with the following geometrical links:

$$d_{\mathrm{OUT}} = d_{\mathrm{IN}} + (2n_{\mathrm{P}} + 1)w_{\mathrm{P}} + (2n_{\mathrm{P}} - 1)s_{\mathrm{P}}, \tag{2.3}$$

$$d_{\mathrm{IN,P1,2}} = d_{\mathrm{OUT,P3,4}} - w_{\mathrm{P}} + s_{\mathrm{P}}. \tag{2.4}$$

Finally, a high magnetic coupling factor between primary and secondary coils, k_{S1} and k_{S2}, is crucial for high-efficiency power transfer. It was maximized by equalizing the outer and inner diameters of the two secondary

structures and the two primary windings while complying with the geometrical bound (2.4):

$$d_{\mathrm{IN,S}} = d_{\mathrm{IN,P3,4}}, \tag{2.5}$$

$$d_{\mathrm{OUT,S}} = d_{\mathrm{OUT,P1,2}}. \tag{2.6}$$

2.3.2 Lumped scalable model

The lumped scalable model of the three-winding transformer with tapped primary coils (half-structure) is shown in Fig. 2.5. It exploits a π-like topology for both primary and secondary coils and uses scalable expressions for inductances, parasitic capacitances, and resistive losses. The inductors $L_{\mathrm{P1,2}}$ and $L_{\mathrm{P3,4}}$ of the two primary branches are magnetically coupled by the factor k_{PP}, whereas the coefficients k_{S1} and k_{S2} represent the magnetic couplings between each $L_{\mathrm{P1,2}}$ and $L_{\mathrm{P3,4}}$ with the secondary coil $L_{\mathrm{S1,2}}$.

The low-frequency value of inductances are computed from geometric parameters of spirals by means of the monomial expressions (2.1) [55], whereas the magnetic coupling factors are calculated using the following monomial expressions [56]

$$k_{\mathrm{PP}} = x_0 \cdot w_{\mathrm{P}}^{x1} \cdot d_{\mathrm{IN,P1,2}}^{x2} \cdot n_{\mathrm{P1,2}}^{x3} \cdot n_{\mathrm{P3,4}}^{x4} \tag{2.7}$$

$$k_{\mathrm{S1}} = y_0 \cdot d_{\mathrm{IN,P1,2}}^{y1} \cdot d_{\mathrm{IN,S}}^{y2} \cdot d_{\mathrm{OUT,S}}^{y3} \cdot n_{\mathrm{P1,2}}^{y4} \cdot n_{\mathrm{S}}^{y5} \tag{2.8}$$

$$k_{\mathrm{S2}} = z_0 \cdot d_{\mathrm{IN,P3,4}}^{z1} \cdot d_{\mathrm{IN,S}}^{z2} \cdot d_{\mathrm{OUT,S}}^{z3} \cdot n_{\mathrm{P3,4}}^{z4} \cdot n_{\mathrm{S}}^{z5} \tag{2.9}$$

where, coefficients x_{0-4}, y_{0-5} and z_{0-5} are computed by least square fitting

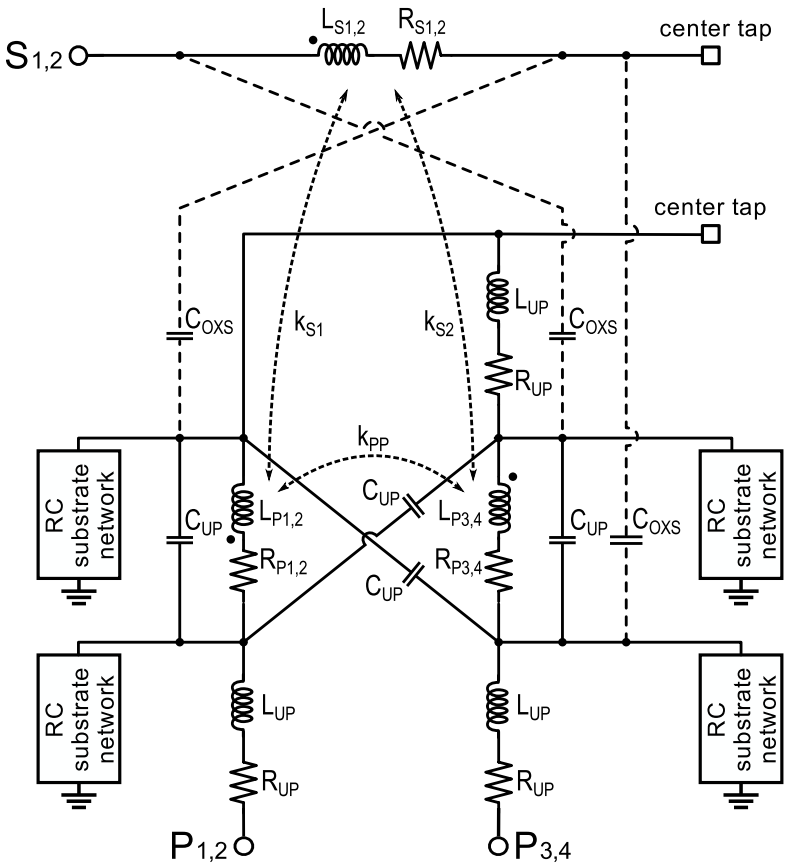


Figure 2.5: Scalable model (half-structure) of the three-winding transformer with tapped primary coils

EM simulated data.

The capacitances due to underpasses (C_{UP}) and oxide between primary and secondary coils (C_{OXS}) are calculated using the simplified expression for parallel plate capacitors, whereas fringing capacitances are neglected, since their value is an order of magnitude lower. It is worth noting that the lack of symmetry leads to a not uniform distribution of the capacitance C_{OXS} and C_{UP}, which must be included in the model.

Inductive and resistive effects due to the three underpasses are taken into account by the model with L_{UP} and R_{UP}, respectively, whose value are cal-

culated by means of the well-known expressions for rectangular conductors. On the other hand, spiral resistive losses (i.e., $R_{\mathrm{P1,2}}$, $R_{\mathrm{P3,4}}$ and $R_{\mathrm{S1,2}}$) are modeled by the expression:

$$R = R_{\mathrm{DC}} \cdot \left[1 + a\sqrt{f} + b \left(\frac{f}{f_{\mathrm{CRI}}} \right)^2 \right] \tag{2.10}$$

where, R_{DC} is the low-frequency resistance of the coil and f_{CRI} is the critical frequency calculated as in [57]. The equation takes into account the increment of resistance due to skin and crowding effects according to the fitting coefficients a and b, respectively, which are computed from the geometrical parameters of the coils by means of linear customized expressions. Finally, typical RC networks are included to model substrate effects [58].

The proposed model was properly customized for the power transfer system specifications, considering the constraints described before. A comparison in the frequency-domain between the developed model and EM simulations of the main electrical parameters (i.e., inductance, Q-factor and magnetic coupling) are shown in Fig. 2.6 and Fig. 2.7, for two three-winding transformers with different geometrical parameters. As apparent, a high degree of accuracy has been achieved. All the EM simulations were carried out using Momentum, a tool for planar EM simulations included in the Advanced Design System (ADS) environment.

The overall accuracy is demonstrated by the error distribution between computed electrical parameters and EM simulations of several geometrically scaled isolation transformers (w_{P} from 50 to 150 μm, d_{IN} from 150 to 450 μm and a number of turns n_{S} of secondary windings from 4 to 6). The y-axis

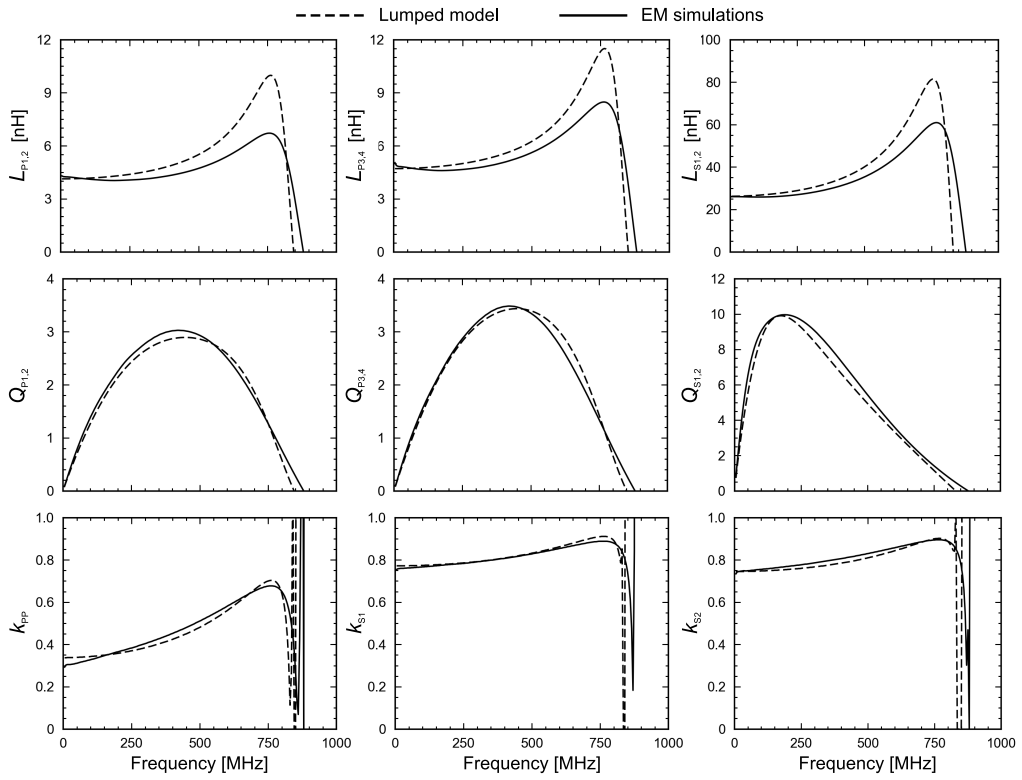


Figure 2.6: Comparison between the developed model and EM simulations of the main electrical parameters of the three-winding transformer ($w_{\mathrm{P}} = 130\ \mu m, d_{\mathrm{IN,P1,2}} = 342\ \mu m, n_{\mathrm{S}} = 6, n_{\mathrm{P3,4}} = 2.5$).

of the graphs in Fig. 2.8. shows the percentage of transformers that exceed the error value at the corresponding x-axis intercept. Maximum errors for inductance, Q-factor peak, self-resonance frequency (SRF), and magnetic coupling factors, k, are smaller than 8%. This accuracy confirms that the proposed lumped model of the three-winding transformer can well be used for the co-design of the hybrid-coupled current-reuse oscillator in power transfer systems with galvanic isolation.

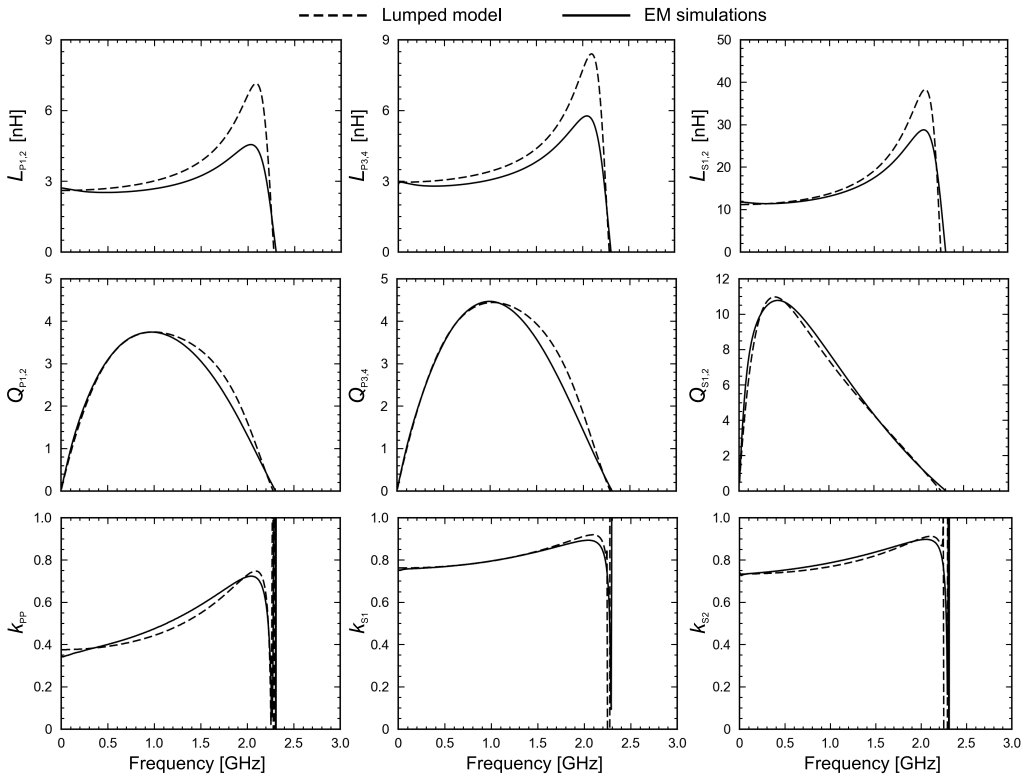


Figure 2.7: Comparison between the developed model and EM simulations of the main electrical parameters of the three-winding transformer ($w_{\mathrm{P}} = 70\ \mu m, d_{\mathrm{IN,P1,2}} = 203\ \mu m, n_{\mathrm{S}} = 5, n_{\mathrm{P3,4}} = 2.5$).

2.4 System design

The design of a power transfer systems with galvanic isolation is not a straightforward process. The interactions between non-linear blocks, i.e. the power oscillator and the rectifier, must be carefully analysed to pursue system optimization in terms of output power, P_{ISO}, and efficiency, η.

To better understand how the losses of each block affect the output power, P_{ISO}, Fig. 2.9 shows a simplified analysis of power losses throughout the dc-dc converter. Since the losses due to the power oscillator cores are subtracted from the power supply P_{DD}, only P_{TX} is transferred through the isolation

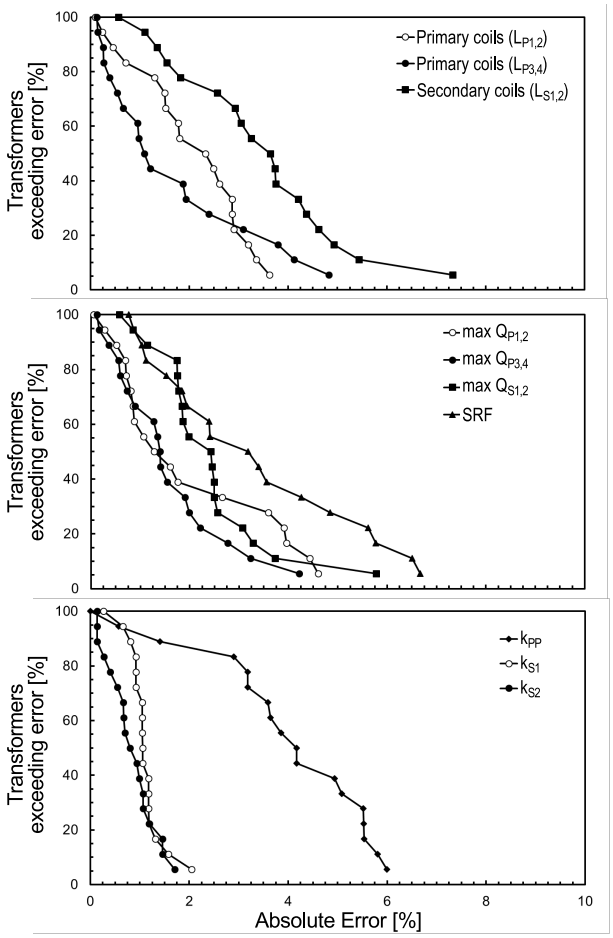


Figure 2.8: Error distributions for the model of the three-winding tapped transformer calculated with respect to EM simulations.

transformer. The power $P_{\mathrm{OUT\_AC}}$ represents the overall ac power coming from the transformer-loaded oscillator towards the input of the rectifier. An important specification for system design is the dc-ac conversion efficiency, defined as $\eta_{\mathrm{DC-AC}} = P_{\mathrm{OUT\_AC}}/P_{\mathrm{DD}}$. Finally, the power $P_{\mathrm{OUT\_AC}}$ is subjected to ac-dc conversion losses, thus the output power of the system is P_{ISO} with the overall efficiency $\eta = P_{\mathrm{ISO}}/P_{\mathrm{DD}}$. The performance optimization requires maximization of the rectifier efficiency, as well as co-design between active (i.e., the oscillator core) and passive (i.e., the transformer) components to

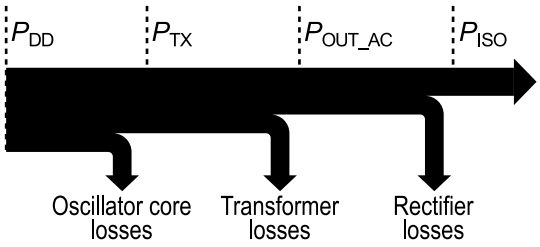


Figure 2.9: Analysis of the power losses throughout the dc-dc converter.

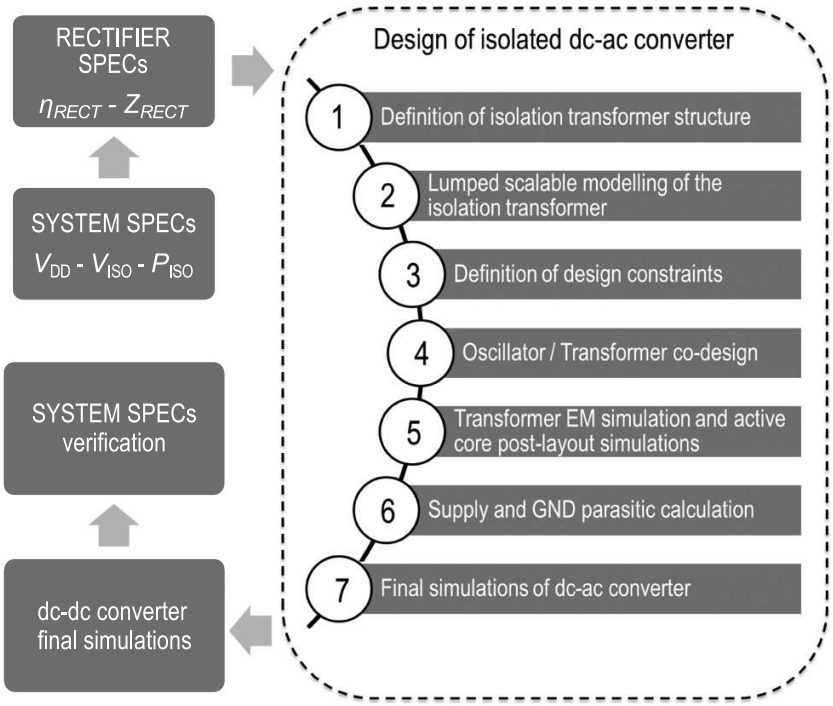


Figure 2.10: Simplified scheme of the design procedure.

maximize $\eta_{\mathrm{DC-AC}}$.

The system design has been been carried out following the procedure introduced in [29]. For the sake of completness, it is reported in Fig. 2.10.

The dc-dc converter was designed to produce a 10-V output voltage, V_{ISO}, from a 5-V power supply, V_{DD}, by exploiting the turn's ratio of the isolation transformer. A dc output power, P_{ISO}, of about 300 mW was addressed,

which enables a wide range of applications (e.g., gate drivers).

The rectifier sets an upper limit to the operation frequency (i.e., the oscillation frequency) due to the degradation of ac-dc conversion efficiency at high frequency. Given the output power and voltage specifications, the rectifier efficiency, η_{RECT}, highly depends on the overall size of the Schottky diodes. The size of each diode is defined by the number M of elementary cells in parallel that in the adopted technology have an active area of 100 $\mu\mathrm{m}^2$ each. Higher size means higher efficiency but also higher input capacitance for the rectifier that can negatively affect the power oscillator. Being Z_{RECT}=$R_{\mathrm{RECT}}//C_{\mathrm{RECT}}$ the input impedance of the rectifier, the size of the Schottky diodes is chosen considering the trade-off between η_{RECT} and C_{RECT}. At the target specifications of 10 V output voltage and 300 mW output power, it leads to $M = 40$, whereas expected values for η_{RECT} and Z_{RECT} were 75% and 200 $\Omega//5$ pF, respectively. Since the rectifier characteristics were quite constant for frequencies lower than 400 MHz, it allows input impedance to be well modelled by Z_{RECT} until this frequency.

The key element of the adopted oscillator topology is the three-winding transformer, which performs both oscillator coupling and output power combining. Once the transformer structure has been defined, the lumped scalable modelling of the transformer developed in the previous section is crucial to maximize system performance, while reducing the amount of computational resources required by complex and time-consuming EM simulations. The availability of such model enables a co-design procedure between the oscillator and the transformer [30]. This allows an accurate estimation of the key electrical performance of the dc-dc converter, i.e., efficiency, output power

Table 2.1: Design parameters of the hybrid-coupled oscillators.

$W_{1,2}/L_{1,2}$	$W_{3,4}/L_{3,4}$	L_{P1-4}	$L_{S1,2}$	k_{S1}	k_{S2}	k_{PP}	$C_{C1,2}$	f_{OSC}	V_{DD}
[mm/μm]		[nH]					[pF]	[MHz]	[V]
10.4/0.8	7.9/0.8	5	20	0.78	0.72	0.32	10	230	5

and power density.

As in traditional transformer-loaded oscillators, the equivalent parallel resistance at the primary side, $R_P = \omega \cdot Q \cdot L_P \cdot (1 + k_P) \cdot (1 + k_S^2)$, has to be maximized to improve the transfer efficiency. This involves high inductance values while preventing an excessive reduction of the the oscillation frequency f_{OSC}. To this aim, parallel capacitances (i.e., $C_{P1,2}$ in Fig. 2.2(c)) are avoided, thus implementing the LC resonance only by means of active core parasitic capacitances, whose lower bound is mainly determined by the minimum transistor size (W/L) for the required power.

The last steps require post-layout simulations (PLS) to extract the RC parasitics due to active device connections. Also, an evaluation of both on-chip and off-chip inductive parasitics, which come from supply planes and bonding wire connections, respectively, is carried out. Finally, simulations of the complete dc-dc isolated converter are performed to verify the fulfillment of system specs.

This design flow requires a few iteration steps to obtain the desired performance. Table 2.1 summarizes the design values for the proposed power oscillator, whereas in Table 2.2 and Fig. 2.11 are shown the final geometrical parameters and measured electrical performance of the three-winding transformer, respectively. At 5-V supply voltage, the nominal oscillation

frequency was 230 MHz. A transformer ratio of 2 was implemented, which increases the output voltage at the secondary winding after power combining up to 10 V. The two 10-pF capacitors $C_{C1,2}$ along with a magnetic coupling k_{PP} as low as 0.32 guarantee the synchronization between the pMOS and nMOS cross-coupled pairs.

Table 2.2: Geometrical parameters of the transformer.

Parameters	**Outer Primary (P1-P2)**	**Inner Primary (P3-P4)**	**Secondary (S1-S2)**
Number of turns (n)	1.5	2.5	5
Width (w) [μm]	115	115	91
Spacing (s) [μm]	1	1	5
Internal diameter (d_{IN}) [μm]	912	332	332
Outer diameter (d_{OUT}) [μm]	1374	1026	1374

2.5 Experimental results

The micrographs of the power oscillator and the rectifier are shown in Fig. 2.12 5(a) and (b), respectively, along with corresponding silicon areas, whereas the complete dc-dc converter assembled on board is shown in Fig. 2.13.

All measurements were performed at 5-V power supply. First, the dc-ac converter was measured by mounting the power oscillator die on an FR4 board along with an equivalent load resistance R_L in parallel to a capacitance C_L representing the rectifier input impedance. Fig. 2.14 reports the measured output power P_{OUT_AC}, the efficiency η_{DC-AC}, and the oscillation frequency f_{OSC} as a function of C_L, with R_L of 200 Ω (i.e., the equivalent rectifier input

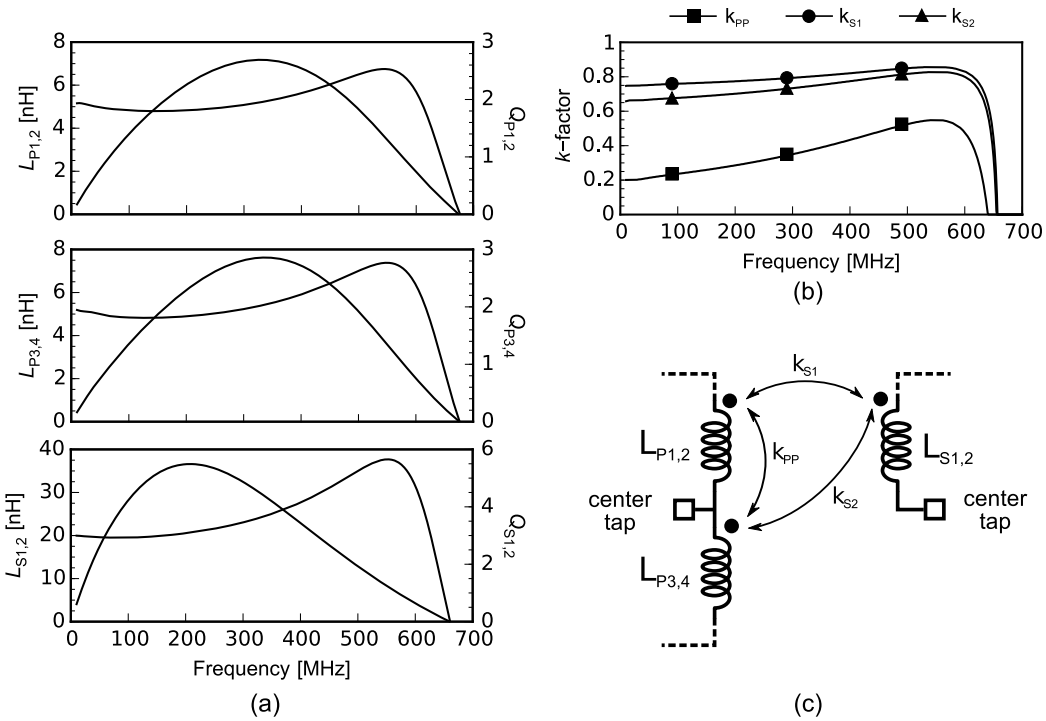


Figure 2.11: Electric performance of the transformer. (a) Inductance and Q-factor. (b) Magnetic coupling factors. (c) Simplified scheme of the transformer (half structure)

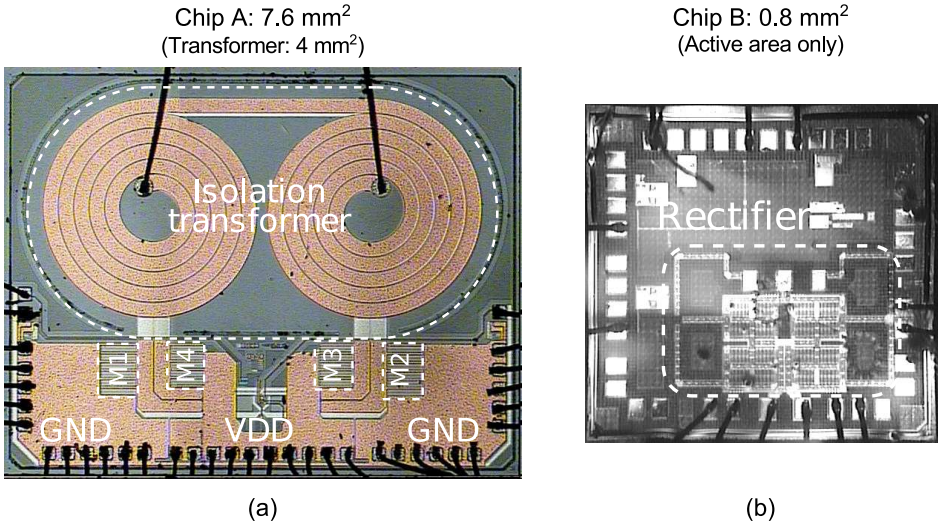


Figure 2.12: Micrographs of (a) power oscillator and (b) rectifier.

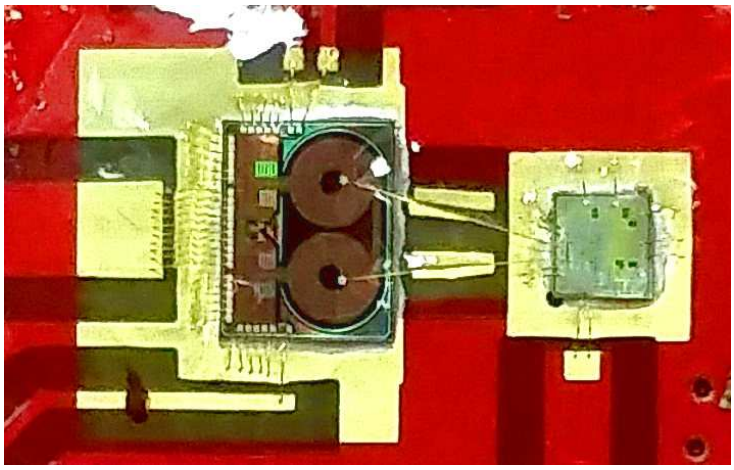


Figure 2.13: Complete dc-dc converter assembled on board.

resistance). An output power higher than 400 mW with an efficiency of about 33% was measured for a C_{L} close to the C_{RECT}. The oscillation frequency is around 225 MHz. It reduces to 190 MHz for a C_{L} as high as 10 pF without appreciably affecting the whole system performance.

Fig. 2.15 shows the waveform of output voltage $V_{\mathrm{OUT\_AC}}$ measured for different values of equivalent rectifier capacitance C_{L} at $R_{\mathrm{L}} = 200\ \Omega$. The x-axis has been normalized to the oscillation period $T_{\mathrm{OSC}} = 1/f_{\mathrm{OSC}}$. As apparent, the maximum oscillation amplitude is as high as 13 V for values of C_{L} around C_{RECT}.

The measured performance of the overall dc-dc converter is shown in Fig. 2.16, where the output dc voltage V_{ISO} was varied from 7 to 11 V by using a semiconductor parameter analyzer. A 300-mW output power P_{ISO} with power efficiency η higher than 24% is achieved.

Table 2.3 compares the performance of the proposed converter with the state of the art of transformer-based step-up dc-dc converters with galvanic isolation. The work in [50] adopts a traditional nMOS cross-coupled topol-

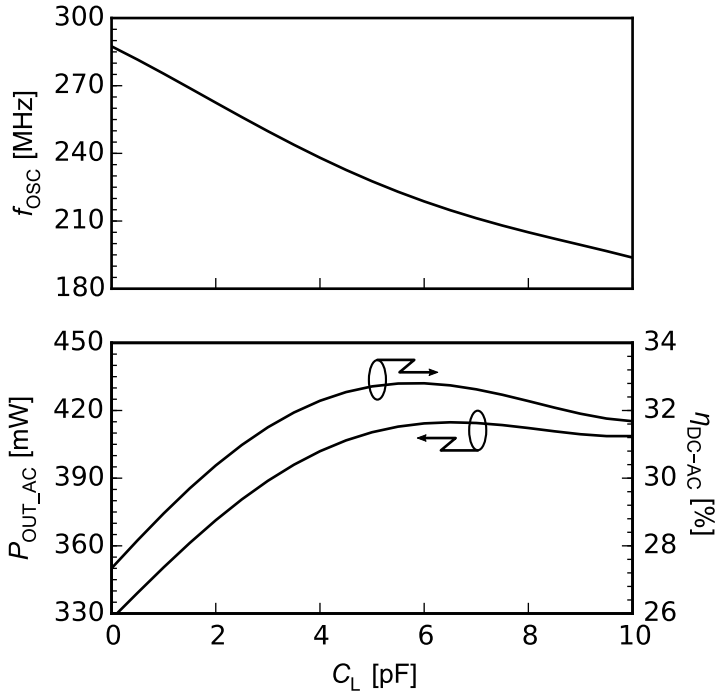


Figure 2.14: Measured output power $P_{\mathrm{OUT\_AC}}$, power efficiency $\eta_{\mathrm{DC-AC}}$, and oscillation frequency f_{OSC} as a function of C_{L} for $R_{\mathrm{L}} = 200\Omega$.

ogy owing to the availability of an HV-CMOS technology. The 5-kV isolation transformer is implemented as a post-processed device in a stand-alone third chip and takes advantage of very thick Au metals, thus achieving a 225-mW output power and an efficiency of 25%. This performance is similar in terms of efficiency to the one of the proposed converter that uses a two-chip implementation and a weaker back end of line without post-processing. A previous work [29] carried out by my research group using the same technology platform (i.e. on-chip SiO_2 transformer and 0.8-μm CMOS devices) exhibits a better efficiency but with a much lower power density. Indeed, the proposed hybrid coupling approach, which reduces the need for a high magnetic coupling factor, combined with the tapped implementation for the

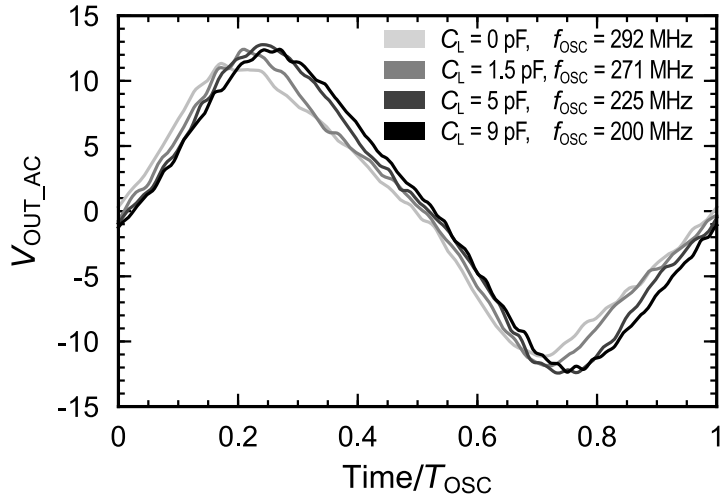


Figure 2.15: Measured ac output voltage $V_{\mathrm{OUT\_AC}}$ for different value of C_{L} ($R_{\mathrm{L}} = 200\Omega$).

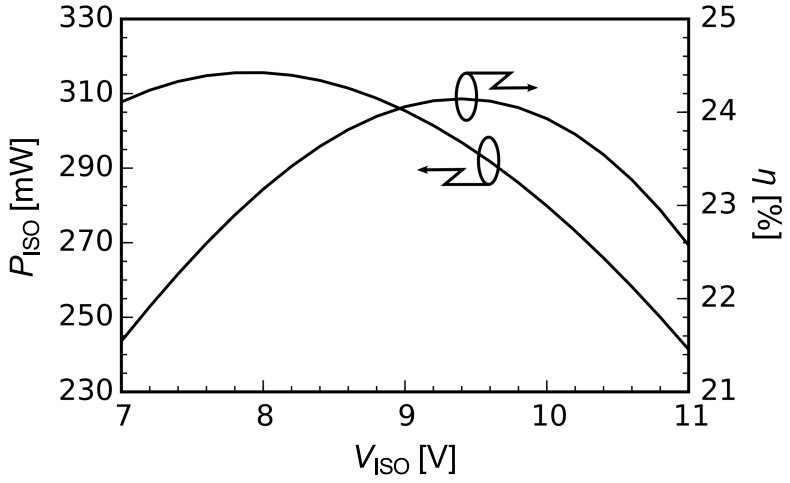


Figure 2.16: Measured dc output power P_{ISO} and efficiency η versus V_{ISO}.

isolation transformer, greatly increases silicon-area efficiency. As a result, output power and power density grow up to 300 mW and 36 mW/mm^2, which are 50% and almost two times higher than those in [29], respectively.

Table 2.3: Comparison with the state-of-the-art step-up dc-dc converters with transformer-based galvanic isolation

	[50]	[29]	This work
Topology	n-MOS cross-coupled	Current-reuse transformer-coupled	Current-reuse hybrid-coupled
P_{ISO} [mW]	225	200	300
η [%]	25	27	24
V_{DD}/V_{ISO} [V]	5/15	5/8	5/10
f_{OSC} [MHz]	160	240	225
Isolation [kV]	5	5	5
Chip no.	3	2	2
Power density [mW/mm^2]	n.a.	19	36
Isolation technology	Post-processed polyimide transformer, 6-μm Au MTLs	On-chip SiO_2 transformer, 0.9-μm Al/3.7-μm Cu MTLs	
Silicon technology	0.6-um HV-CMOS, Schottky diodes	0.8-μm CMOS, Schottky diodes	

The power efficiency of 24% is competitive with the state of the art.

CHAPTER 3

A 100-mW fully-integrated dc-dc converter with double galvanic isolation

3.1 Introduction

This chapter presents the very first fully-integrated dc-dc converter with double galvanic isolation. It is implemented using only two chip, thus achieving the highest level of integration. A 3.3-V output voltage from a 3.3-V supply voltage was targeted to enable a large range of low-power applications, e.g. sensor interfaces requiring up to 100 mW of isolated output power.

As introduced in the first chapter, increasing degrees of isolation can be implemented for a semiconductor isolator. A functional isolation enables the proper function of system by separating the ground references between the

two interfaces. Then, a basic isolation provides protection against electrical shocks in the order of a few kilovolts. Finally, a double galvanic isolation is used to improve the safety by adding a supplementary isolation barrier that provides redundancy in case one of the barriers fails, while inherently increasing the overall galvanic isolation level. The latter can be useful in many cases, especially when human operators or sensitive circuits are involved. Typically, the double isolation is the widespread approach to achieve the highest level of isolation, namely reinforced isolation, which is certified by *VDE 0884-10* standard by means of a specific 10-kV surge test [46].

As far as double isolation is concerned, only fully-integrated data isolators are commercially available [7], whereas power transfer is still hindered by the very poor power efficiency due to the high loss associated with the two isolation barriers connected in series. On the other hand, achieving reinforced isolation by means of a single thicker isolation barrier is not trivial due to second order breakdown effects and mechanical stress.

A double isolation barrier could be implemented exploiting either two series-connected isolation capacitors or transformers. However, thick-oxide capacitors alone are not suitable for power transfer due to both bottom plate parasitics and capacitive partition with the input of the ac-dc conversion stage (rectifier), whereas on-chip isolation transformers allow power transfer but typically exhibit a low efficiency (i.e., around 50%), thus resulting in a poor power transfer system when two transformers are connected in series. On the other hand, implementing a double isolation barrier using both isolation components enables a resonant mode operation, which can be exploited to improve the dc-dc converter performance. To this aim, the

proposed converter uses a novel architecture based on LC resonant isolation networks, which considerably improve the efficiency of the power transfer with respect to traditional schemes (i.e., series connected transformers or capacitors). Output power regulation is also provided by means of a PWM based control link that sets the output voltage.

The chapter is organized as follows. Section 3.2 presents the system overview. Section 3.3 and 3.4 describe the power and control links giving the main circuit design guidelines. A detailed description of the integrated isolation components is reported in Section 3.5. Finally, experimental results are provided and discussed in Section 3.6.

3.2 System Description

The simplified block diagram of the proposed dc-dc converter is depicted in Fig. 3.1. It consists of two dice, namely Chip A and Chip B, both fabricated in a 0.35 μm BCD technology by STMicrolectronics. A thick oxide layer is included in the back-end of line (BEOL) [42]. It features a 5-kV galvanic isolation between top metal layers, which is exploited to implement the isolation barriers.

The core of the system is the very high frequency (VHF) power link that is made up of a power oscillator and a rectifier, which perform dc-ac and ac-dc conversion, respectively. A double isolation is achieved by means of an LC resonant barrier specifically implemented by thick oxide capacitors $C_{\mathrm{ISO,P}}$ and transformer $T_{\mathrm{ISO,P}}$ [47] on Chip A and Chip B, respectively.

The output voltage V_{ISO} is regulated by means of a RF feedback loop,

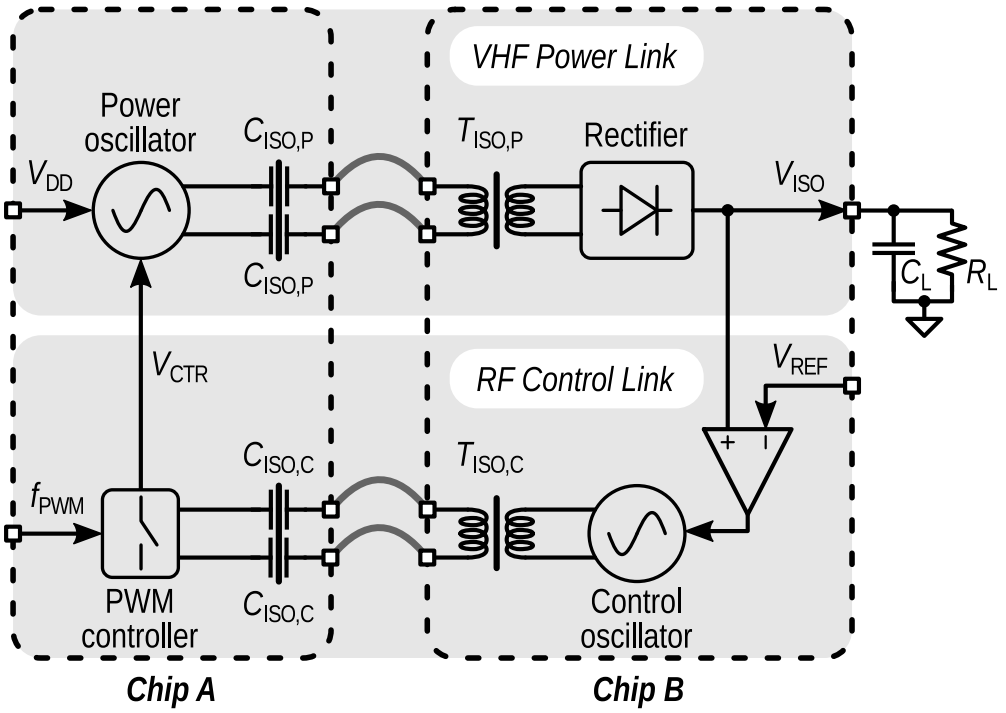


Figure 3.1: Simplified block diagram of the system.

according to the pulse width modulated (PWM) control scheme proposed in [59] and implemented in [49]. Specifically, as shown in Fig. 3.1, V_{ISO} is compared with a voltage reference V_{REF} and hence the error signal sets the oscillation amplitude of the control oscillator. Of course double galvanic isolation is guaranteed also for the control feedback loop. The RF oscillation signal is transmitted towards the PWM controller through the two galvanic barriers performed by the transformer $T_{\mathrm{ISO,C}}$ and capacitors $C_{\mathrm{ISO,C}}$. Finally, the controller drives the power oscillator by means of the control voltage V_{CTR}, whose duty cycle is inversely proportional to the output voltage error, $V_{\mathrm{ISO}} - V_{\mathrm{REF}}$.

The converter was designed to provide up to 100 mW output power, P_{ISO}, to the external load $R_{\mathrm{L}}//C_{\mathrm{L}}$. A nominal output voltage, V_{ISO}, of 3.3 V,

from a 3.3 V supply voltage, V_{DD}, was targeted. These specifications are suitable for many applications, which include low-voltage sensor interfaces. The following Sections will be focused on the transistor-level design of the power and control links with a detailed description of the integrated isolation networks.

3.3 Power Link

The architecture of the power link presents several differences with respect to the ones commonly adopted for basic isolation [28], [30], [38], [45], [47], [60]. As shown in Fig. 3.2, double isolation is performed by means of a hybrid coupling based on the thick-oxide capacitors, $C_{\mathrm{ISO,P}}$, and the transformer, $T_{\mathrm{ISO,P}}$. This approach inherently enables the resonant mode operation for the isolation network, thus increasing efficiency compared with series-connected isolation components (i.e., two transformers).

Unfortunately, thick-oxide capacitors $C_{\mathrm{ISO,P}}$ exhibit heavy parasitic capacitances (C_{P} in Fig. 3.2) that greatly limit their use in a typical power link based on a transformer-loaded oscillator. To overcome this drawback, a novel circuit architecture is proposed, which includes the parasitic capacitances into the resonant tank of an inductive-loaded oscillator, thus neutralizing the power partitioning between $C_{\mathrm{ISO,P}}$ and C_{P}.

The power oscillator exploits lateral-diffused MOS (LDMOS) transistors, $M_{1,2}$, as active core and is operated in D-class [30], [51]. Thanks to the oscillator topology and the high voltage/current capability of LDMOS transistors, a voltage oscillation amplitude, $V_{\mathrm{OSC,P}}$, of about two times V_{DD} is achieved.

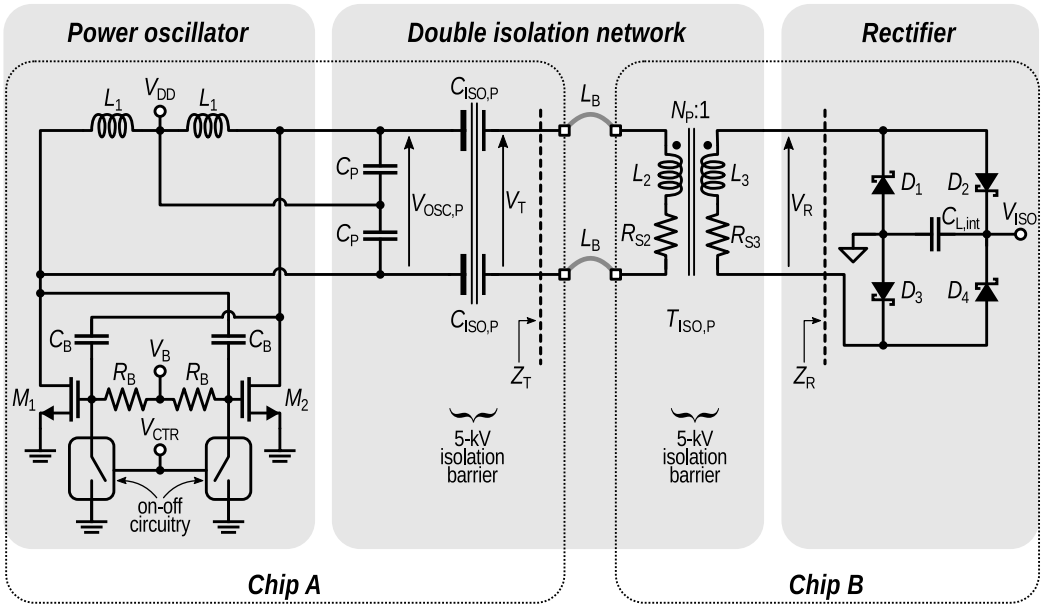


Figure 3.2: Schematic of the power link.

On the other hand, capacitors C_{B} keep the gate-source voltage of $M_{1,2}$ below the maximum allowable value, since they perform a voltage partition with the gate-source capacitances that avoids gate-oxide breakdown. The resonant tank benefits of a high-Q differential inductor, L_1, built on the top Cu metal. Since capacitance C_{P} is much higher than $C_{\mathrm{ISO,P}}$, the power oscillation frequency, $f_{\mathrm{OSC,P}}$, is set by C_{P} regardless Z_{T}, thus simplifying the design with respect to the commonly adopted transformer-loaded oscillator [30],[49]. Specifically, the inductor-loaded power oscillator allows double isolation network to be properly designed without affecting the oscillation frequency that becomes an independent design parameter. A proper step-down conversion of the oscillation signal (i.e., from V_{T} to V_{R}) is required to produce the nominal output voltage at 3.3 V. Finally, the ac-dc conversion is performed by means of a Schottky diode full-bridge rectifier. To control the output power

an on-off circuitry was implemented. It allows the cross-coupled pair $M_{1,2}$ to be on-off switched by means of the control terminal V_{CTR}. Therefore, the amount of power delivered to the load can be varied without losing efficiency by feeding a pulse width modulated (PWM) signal to V_{CTR}.

Starting from the converter requirements on power supply V_{DD}, isolated output power P_{ISO}, and isolated output voltage V_{ISO}, a design procedure has been developed, which is summarized in Fig. 3.3.

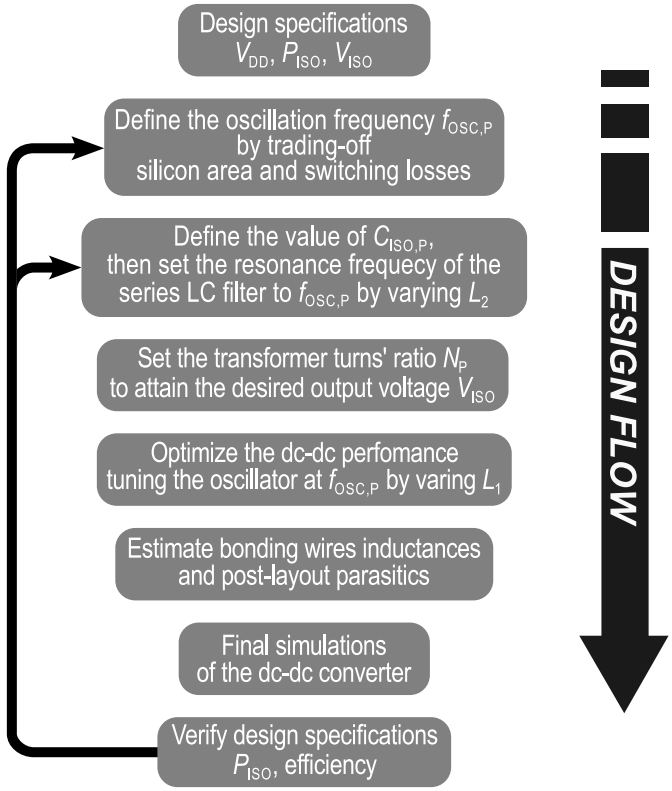


Figure 3.3: Proposed design procedure for the power link.

The first step consists in setting the power link operating frequency, $f_{\mathrm{OSC,P}}$. As mentioned before, it is almost independent from the isolation network thanks to the oscillator arrangement. Indeed, a high $f_{\mathrm{OSC,P}}$ would

reduce the silicon area required by the isolation network, however it increases power losses of both switching transistors and rectifier. Therefore, as a trade-off between area and losses, an oscillation frequency, $f_{\mathrm{OSC,P}}$, around 400 MHz was set. The rectifier performance is optimized accordingly and hence its input impedance, Z_{R}, is estimated for the next design steps, i.e., the design of double isolation network. Specifically, a linear approximation of Z_{R} at the first harmonic was considered by using a large-signal periodic steady-state analysis (i.e., $Z_{\mathrm{R}} = R_{\mathrm{R}}//C_{\mathrm{R}}$).

In the second step, the resonance frequency of the series LC network (i.e., capacitors $C_{\mathrm{ISO,P}}$ and the primary winding of isolation transformer, L_2) is set to the operating frequency, $f_{\mathrm{OSC,P}}$. Since the area consumption is mainly ascribed to thick-oxide capacitors, due to their very low specific capacitance, the value of $C_{\mathrm{ISO,P}}$ has been traded-off between silicon area and the Q-factor of the network, $Q_{\mathrm{ISO,P}}$, whereas L_2 is simply calculated, as follows:

$$L_2 \approx \frac{\mathrm{Im}[Z_{\mathrm{TR}}]}{2\pi} = \frac{(2\pi f_{\mathrm{OSC,P}})^2}{C_{\mathrm{ISO,P}}/2}. \tag{3.1}$$

Indeed, thanks to the resonance of the series LC network, the oscillation voltage $V_{\mathrm{OSC,P}}$ experiences a step-up gain that produces a voltage, V_{T}, at the top plates of capacitors $C_{\mathrm{ISO,P}}$, which is $Q_{\mathrm{ISO,P}}$ times higher than $V_{\mathrm{OSC,P}}$. However, maximizing $Q_{\mathrm{ISO,P}}$ improves the isolation network power transfer at the cost of its bandwidth, which has to be sufficiently wide to comply with process variations. The Q-factor of the series LC isolation network,

neglecting parasitic resistances of $C_{\mathrm{ISO,P}}$ and L_2, can be approximated as

$$Q_{\mathrm{ISO,P}} \approx \frac{1}{\mathrm{Re}[Z_{\mathrm{T}}]}\sqrt{\frac{L_2}{C_{\mathrm{ISO,P}}/2}}, \tag{3.2}$$

being Z_{T} the impedance seen at top plates of $C_{\mathrm{ISO,P}}$, as indicated in Fig. 3.2. According to (3.2), a low Q-factor calls for a high $C_{\mathrm{ISO,P}}$, but this would lead to excessive silicon area consumption.

The design of the isolation network is finalized in the third step, where transformer turns' ratio, N_{P}, is calculated considering the overall voltage gain throughout the power link. Indeed, to attain the desired output voltage level, the power isolation transformer, $T_{\mathrm{ISO,P}}$, accomplishes the required step-down conversion of the oscillation voltage V_{T}. An approximated expression for the dc-dc converter voltage gain has been developed. Assuming a high magnetic coupling between transformer windings and an ideal full-bridge rectifier, the voltage gain from V_{DD} to V_{ISO} can be expressed as

$$\frac{V_{\mathrm{ISO}}}{V_{\mathrm{DD}}} \approx 2 \cdot Q_{\mathrm{ISO,P}} \cdot \frac{L_2}{L_2 + 2L_{\mathrm{B}}} \cdot \frac{1}{N_{\mathrm{P}}} \cdot \frac{|Z_{\mathrm{R}}|}{|Z_{\mathrm{R}} + R_{\mathrm{S3}}|} \cdot \frac{2}{\pi}, \tag{3.3}$$

where L_{B} and R_{S3} are the inductance of the bonding wires and the dc series resistance of L_3, respectively, whereas $N_{\mathrm{P}} = \sqrt{L_2/L_3}$ is the transformer turns' ratio. As apparent from (3.3), the power signal experiences a voltage attenuation due to both L_{B} and R_{S3}, which cause a reduction of the power efficiency. However, these attenuations have been mitigated during the design of transformer $T_{\mathrm{ISO,P}}$, by setting L_2 much higher than L_{B} and minimizing R_{S3}.

Being $V_{\mathrm{ISO}} = V_{\mathrm{DD}} = 3.3\ V$, a unitary voltage gain was fixed. Hence, performing a trade-off among power efficiency, bandwidth and silicon area, for a $C_{\mathrm{ISO,P}}$ of about 3 pF, an inductance L_2 around 100 nH and a transformer turns' ratio N_{P} of about 2.6 are obtained. The resulting value for $Q_{\mathrm{ISO,P}}$ is 2. It is worth noting that in this calculation the approximated equation (3.1) has been used. Therefore, the final value of L_2 will be lower than 100 nH. It will be corrected afterwards by means of circuit simulations, where these second-order terms are taken into account.

Once the double isolation network has been defined, the VHF oscillator optimization is carried out. Thus, the cross coupled pair $M_{1,2}$ is properly sized to deliver the output power P_{ISO}, whereas L_1 is tuned to set the oscillation frequency equal to $f_{\mathrm{OSC,P}}$.

An accurate evaluation of post-layout and off-chip parasitics is of utmost importance to finalize the power link design. As far as the power oscillator is concerned, post-layout parasitic capacitances can shift the oscillation frequency away from the center-band of the series LC network, thus reducing the isolation network gain. On the other hand, a limited number of bonding wire connections for the supply planes leads to a reduction of the effective supply voltage, caused by the high switching frequency and current level of the LDMOS pair. Therefore, taking into account parasitics is essential to reduce their effects, while avoiding an excessive degradation of the overall dc-dc converter performance.

The last steps of the adopted design procedure include final simulations followed by a verification of system requirements. A few iterations are required to find the right operation frequency $f_{\mathrm{OSC,P}}$ and the value of $C_{\mathrm{ISO,P}}$

that respect the limits imposed on silicon area consumption and guarantee a sufficient bandwidth for isolation network to make the design robust against the expected process variations.

Finally, in Fig. 3.4 are depicted the simulated voltage waveforms $V_{\mathrm{OSC,P}}$, V_{T} and V_{R} of the power link, whereas in Table 3.1 and Table 3.2 are shown the final values of design parameters of the power link and the simulated breakdown power losses, respectively. Simulations have been carried out with Cadence Virtuoso and Eldo Platform, specifically by using the steady state analysis performed by Eldo RF. As apparent, most of the power losses are due to the oscillator, but thanks to the proposed approach the two isolation barriers contribute only for the 25% of the overall power loss. This result shows that the double isolation barrier exhibits a power efficiency comparable to a single one.

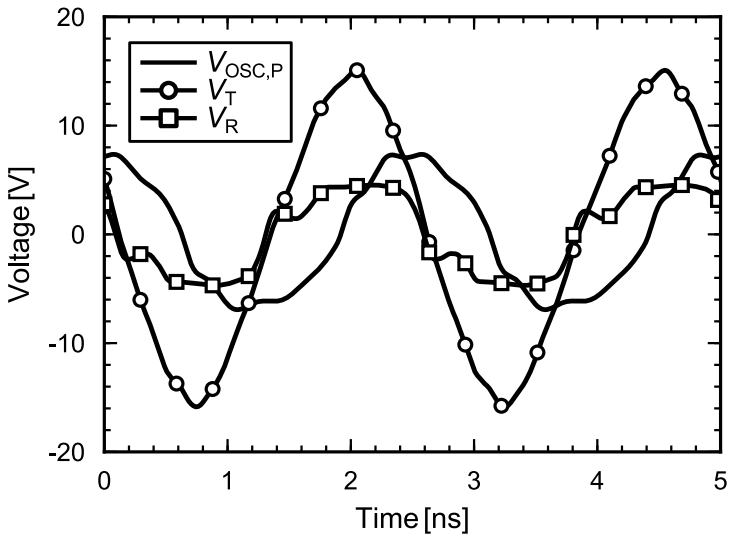


Figure 3.4: Simulated differential voltage waveforms $V_{\mathrm{OSC,P}}$, V_{T}, V_{R} of the power link ($P_{\mathrm{ISO}} = 100\ mW$, $V_{\mathrm{ISO}} = 3.3\ V$ and $V_{\mathrm{DD}} = 3.3\ V$).

Table 3.1: Design parameters of the power link.

$W_{1,2}$ [mm]	L_1	L_2	L_3	C_P	$C_{ISO,P}$	$f_{OSC,P}$ [MHz]	V_{DD} [V]
	[nH]			[pF]			
2	5	85	15	15	3	400	3.3

Table 3.2: Simulated breakdown power losses of the power link ($P_{ISO} = 100\ mW$, $V_{ISO} = V_{DD} = 3.3\ V$).

Block	**Power loss [%]**
Oscillator	65
Isolation capacitors	10
Isolation transformer	15
Rectifier	10

3.4 Control Link

A simplified schematic of the control loop is sketched in Fig. 3.5. An error amplifier compares the output voltage,V_{ISO}, with the reference voltage, V_{REF}, then its output voltage drives M_3, which controls the biasing current $I_{OSC,C}$ of the transformer-loaded control oscillator. The differential oscillation voltage between the drains of M_4 and M_5 experiences a step-up gain followed by an attenuation, which are performed by the transformer turns' ratio N_C, and the capacitive partition between $C_{ISO,C}$ and its bottom plate capacitances, respectively. Finally, the RF voltage, $V_{OSC,C}$ is converted into the control signal V_{CTR} by means of the PWM controller, whose schematic is shown in Fig. 3.6. Specifically, the peak detector generates a voltage V_{PD} that is inversely proportional to the peak of the oscillation voltage, $V_{OSC,C}$. V_{PD} is processed by the SC integrator, which produces a voltage descending ramp that is compared with the voltage reference, V_{COMP}. When this ramp goes

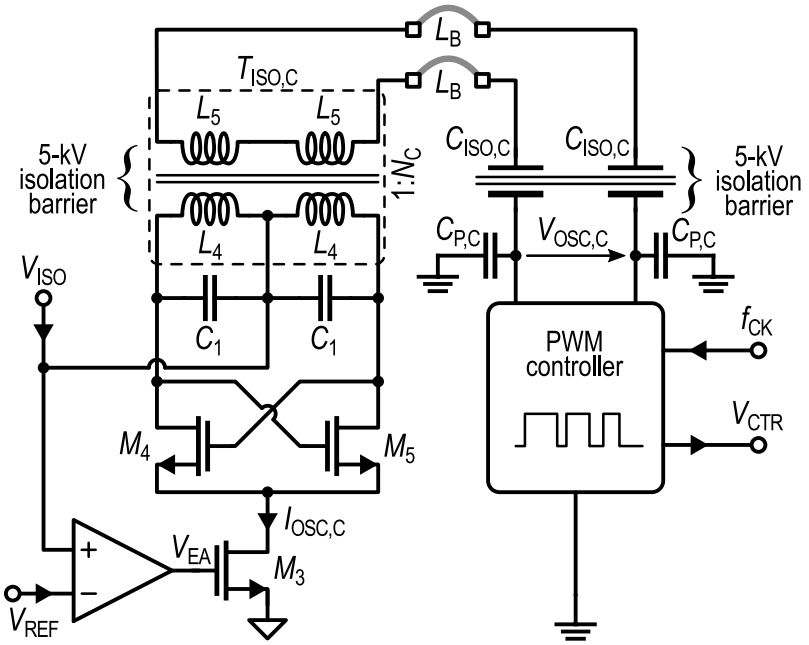


Figure 3.5: Simplified schematic of the control link.

below V_{COMP}, the comparator resets the output of the D Flip Flop, the capacitor C_{F} is discharged and the output of the SC integrator is restored to V_{GND}. Also, the SC integrator is periodically restored through ϕ_0 either at the beginning of each period or when V_{CTR} is low.

Indeed, the voltage reference V_{COMP} along with the ground voltage of the SC integrator, V_{GND}, have been designed to comply with the dynamic range V_{PD}. As apparent, given V_{GND} and V_{COMP}, a higher value of V_{PD} would generate a lower duty cycle for V_{CTR}. The duty cycle, DC, produced by the PWM controller as function of V_{PD} is reported in (3.4)

$$DC = \frac{1}{32}\frac{C_{\mathrm{F}}}{C_{\mathrm{I}}}\frac{V_{\mathrm{COMP}} - V_{\mathrm{GND}}}{V_{\mathrm{PD}} - V_{\mathrm{GND}}} \tag{3.4}$$

The clock signal, f_{CK}, sets the timing of the PWM controller. It is

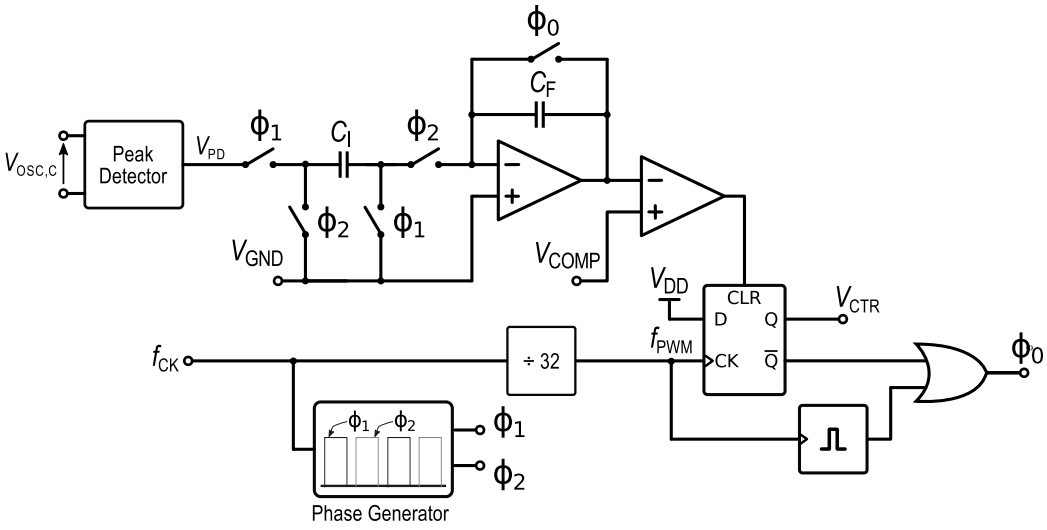


Figure 3.6: Schematic of the PWM controller of the control link.

exploited to generate the two non-overlapped phases (i.e., ϕ_1 and ϕ_2) for the SC integrator and the frequency f_{PWM} of the PWM signal, V_{CTR}. Differently from conventional continuous-time control loops, the proposed approach based on SC integrator and external clock reference allows the PWM control frequency to be set according to the application requirements, such as output ripple frequency content.

To reduce the size of passive isolation components (i.e., $C_{\mathrm{ISO,C}}$ and $T_{\mathrm{ISO,C}}$), the control link is operated at an oscillation frequency $f_{\mathrm{OSC,C}}$ as high as 1 GHz, fixed by the resonant load of the oscillator L_4-C_1. Since the control oscillator is supplied by the isolated output voltage, V_{ISO}, its biasing current, $I_{\mathrm{OSC,C}}$, has to be kept as low as possible, to avoid excessive degradation of the overall power converter efficiency, especially at maximum P_{ISO}. On the other hand, the amplitude of $V_{\mathrm{OSC,C}}$ has to be large enough to overcome the attenuation due to bottom plate capacitances of $C_{\mathrm{ISO,C}}$. Thus, the maximum biasing current $I_{\mathrm{OSC,C}}$, which is used at the minimum P_{ISO} (i.e., at minimum

PWM duty cycle) is about 1 mA, while it is reduced to about 300 μA at maximum P_{ISO} (i.e., at maximum PWM duty cycle) to maximize the overall dc-dc converter efficiency, η.

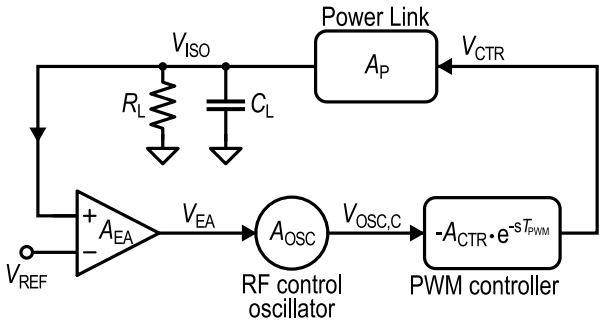


Figure 3.7: Simplified block diagram of the control loop for stability analisys.

The control loop stability analysis was carried out considering a single pole approximation for each block of the system. By referring to the simplified model in Fig 3.7, the open-loop gain, T_{O}, can be written as

$$T_{\mathrm{O}} = A_{\mathrm{EA}} \cdot A_{\mathrm{OSC}} \cdot A_{\mathrm{CTR}} \cdot A_{\mathrm{P}} \tag{3.5}$$

where A_{EA} is the error amplifier gain and A_{OSC}, A_{CTR} and A_{P} are the gains of the RF control oscillator, PWM controller and power link, respectively, which are given by

$$A_{\mathrm{OSC}} = \frac{dV_{\mathrm{OSC}}}{dV_{\mathrm{EA}}} = g_{\mathrm{m3}} \frac{2}{\pi} R_{\mathrm{P}} k_{\mathrm{C}} N_{\mathrm{C}} \frac{C_{\mathrm{ISO,C}}}{C_{\mathrm{ISO,C}} + C_{\mathrm{P,C}}} \tag{3.6}$$

$$A_{\mathrm{CTR}} = \frac{dDC}{dV_{\mathrm{OSC}}} = |A_{\mathrm{PD}}| \frac{32(C_{\mathrm{F}}/C_{\mathrm{I}})DC^2}{V_{\mathrm{GND}} - V_{\mathrm{COMP}}} \tag{3.7}$$

$$A_{\mathrm{P}} = \frac{dV_{\mathrm{ISO}}}{dDC} = \frac{1}{2}\sqrt{\frac{R_{\mathrm{L}} P_{\mathrm{ISO,max}}}{DC}} \tag{3.8}$$

being g_{m3} the transconductance of M_3, R_P, k_C and N_C the equivalent loss resistance at the primary winding $T_{ISO,C}$, the magnetic coupling factor and the turns' ratio of $T_{ISO,C}$, respectively, $C_{ISO,C}$ and $C_{P,C}$ the isolation capacitor and its bottom plate parasitic, respectively, A_{PD} the gain of the peak detector, DC the duty cycle of V_{CTR}, and $P_{ISO,max}$ the maximum power delivered to R_L, which can be considered constant in a first-order approximation.

An expression of the loop-gain, $T(s)$, in the frequency domain has been evaluated neglecting high-frequency poles. Thus, considering only the two main low-frequency contributions, which are the pole of the power link load (i.e., R_L-C_L) and the delay introduced by the PWM controller, whose maximum value is $T_{PWM} = 1/f_{PWM}$, the loop gain can be written as

$$T(s) = T_O \cdot \frac{e^{-sT_{PWM}}}{1 + sR_L C_L} \tag{3.9}$$

The worst case for system stability (i.e., the maximum value of T_O) is given for a unitary DC. In this case, a 30-dB open-loop gain, T_O, has been evaluated. Therefore, a dominant-pole compensation can be easily carried out increasing the 300-pF on-chip load capacitance $C_{L,int}$ with the external capacitor in parallel, C_L. Finally, the overall value of the compensation capacitor, C_L, can be calculated from

$$C_L = \frac{T_O T_{PWM}}{R_L \left(\frac{\pi}{2} - PM\right)} \tag{3.10}$$

where PM is the phase margin of the system in radians. As a result, to guarantee system stability with 100-kHz PMW control signal, a few-microfarads

$C_{\mathrm{L}} \gg C_{\mathrm{L,int}}$ is required. Such values provide adequate performance in terms of both output voltage ripple and transient responses.

Thanks to the generality of the proposed control loop, it can be adopted in various power systems with galvanic isolation regardless the degree of isolation (i.e., basic, double or reinforced). A different example of application is demonstrated in [49], where the control loop has been adapted to a fully integrated and galvanically isolated dc-dc converter with data communication. Specifically, the RF oscillator has been exploited to transfer both data and control signal on the same channel. This greatly reduces the overall cost of the system since a single isolation transformer performs two functions. It is possible because the information impressed by the control signal to the peak of the oscillation varies slowly, thanks to the low-frequency dominant pole at the output of the power link. Therefore, a communication channel with 50 Mbps of data rate can be superimposed to the RF oscillation amplitude. Of course, data and control signals can be easily filtered thanks to their largely spaced frequency contents.

3.5 Double isolation networks

The isolation networks for both power and control links have been implemented by exploiting all the available four metal layers. Of course the 5-kV galvanic isolation rating is guaranteed thanks to the thick oxide that separates the two top metal layers (i.e., 0.9-μm thin-Al metal 3 and 3.7-μm thick-Cu metal 4), and it has been assessed by the technology provider using various passive structures [42], [43]. Both isolation networks have been

designed ad-hoc and optimized by means of extensive electromagnetic (EM) simulations and compact modelling [29], [30], [58], [61]. All the EM simulations have been carried out using Momentum, a planar EM simulator within the Advanced Design System (ADS) environment.

As far as the power link is concerned, the simplified cross-section of the substrate and the equivalent electric circuit of the double isolation network are sketched in Fig. 3.8. Inductor L_1 is built on the thick-Cu metal layer

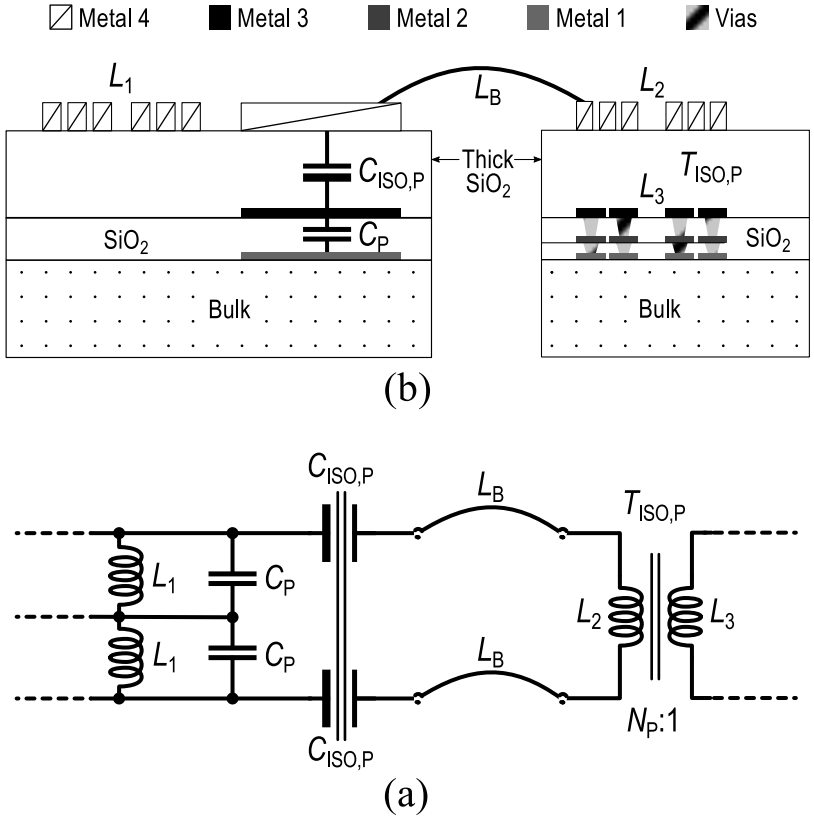


Figure 3.8: (a) Simplified cross-section of the double isolation network of the power link and (b) its equivalent circuit model.

to attain a high Q-factor. The first level of isolation is provided by capacitors $C_{\mathrm{ISO,P}}$ that are built between the third and fourth metal layers. It is

worth noting that the thick inter-metal oxide layer leads to a significantly low specific capacitance, while the bottom plate parasitic is very large due to the few micrometers distance from the substrate. Moreover, bottom plate parasitic of capacitor $C_{\mathrm{ISO,P}}$ has a very low quality factor, thus causing a detrimental power loss and a consequent degradation of the power transfer efficiency. To overcome such problem, the novel circuit architecture presented in Section 3.3 has been adopted for the power link. In this implementation, capacitors $C_{\mathrm{ISO,P}}$ have been shielded from substrate exploiting a metal 1 plane (see Fig. 3.8), thus inherently creating the additional high-Q capacitors C_{P}, which are included in the oscillator resonator along with L_1. Many advantages come from replacing bottom plate capacitors with capacitors C_{P}, which also become crucial for the system. Firstly, the Q-factor of C_{P} is considerably improved, thanks to the high quality of the inter-metal oxide layer, thus reducing the power losses. Moreover, the bottom plate of capacitors C_{P} can be cancelled out by means of a simple connection to V_{DD} through the center tap of the differential inductor L_1, increasing the quality of the resonator. Finally, the capacitance value of C_{P} is well-controlled, since it depends on the oxide thickness of technology back-end.

Fig. 3.9 shows the measured capacitance and Q-factor of a 1-pF isolation capacitor (e.g., C_{ISO}) shielded with a metal 1 plane to form the additional capacitor (e.g., C_{P}). A $C_{\mathrm{ISO,P}}$ of about 3 pF in the power converter leads to a $C_{\mathrm{P}} \approx 15$ pF. Along with the 10-nH differential inductor L_1, they define the power oscillator resonator. It is worth noting that the high value of capacitors C_{P} reduces the effect of the non-linear variations of active device capacitance, thus improving $f_{\mathrm{OSC,P}}$ estimation, especially if large-signal

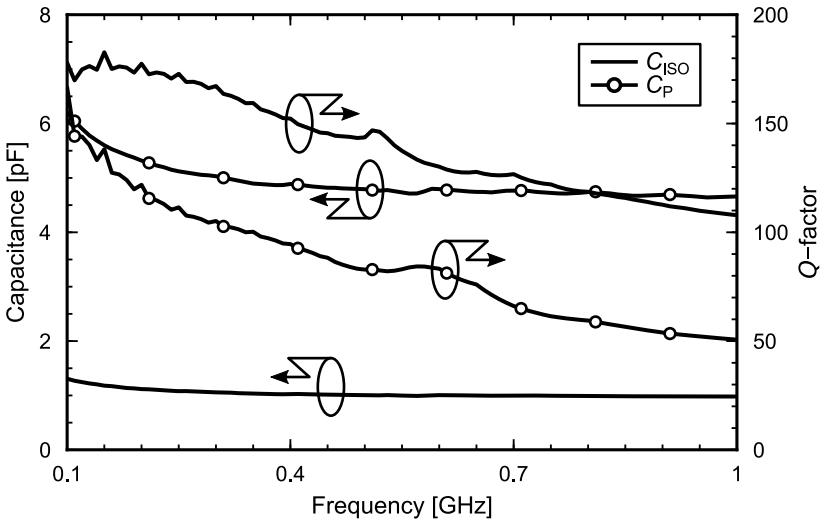


Figure 3.9: Capacitance and quality factor of a 1-pF metal3-metal4 capacitor, (C_{ISO}) shielded with a metal 1 layer (C_{P}).

LDMOS capacitance modeling is not available [62].

The second level of isolation of the power link is provided by the transformer $T_{\mathrm{ISO,P}}$, which is shown in Fig. 3.10 along with its measured electrical performance. It is built on a second die (i.e., Chip B), and its terminals are connected to the top plates of the isolation capacitors $C_{\mathrm{ISO,P}}$ by means of two bonding wires. The primary winding L_2 is implemented on metal 4, whereas the secondary winding L_3 is realized shunting metal layers 1 to 3 to minimize the dc series resistance, as required by (3.3). An L_2 and L_3 of about 85 nH and 15 nH, respectively, have been implemented. Differently from isolation transformers adopted in typical fully integrated power transfer systems with basic isolation [30], [38], [49] the transformer $T_{\mathrm{ISO,P}}$ takes advantage of a single-ended configuration since there is no need of a center tap. This leads to a better quality factor of the coils and a magnetic coupling

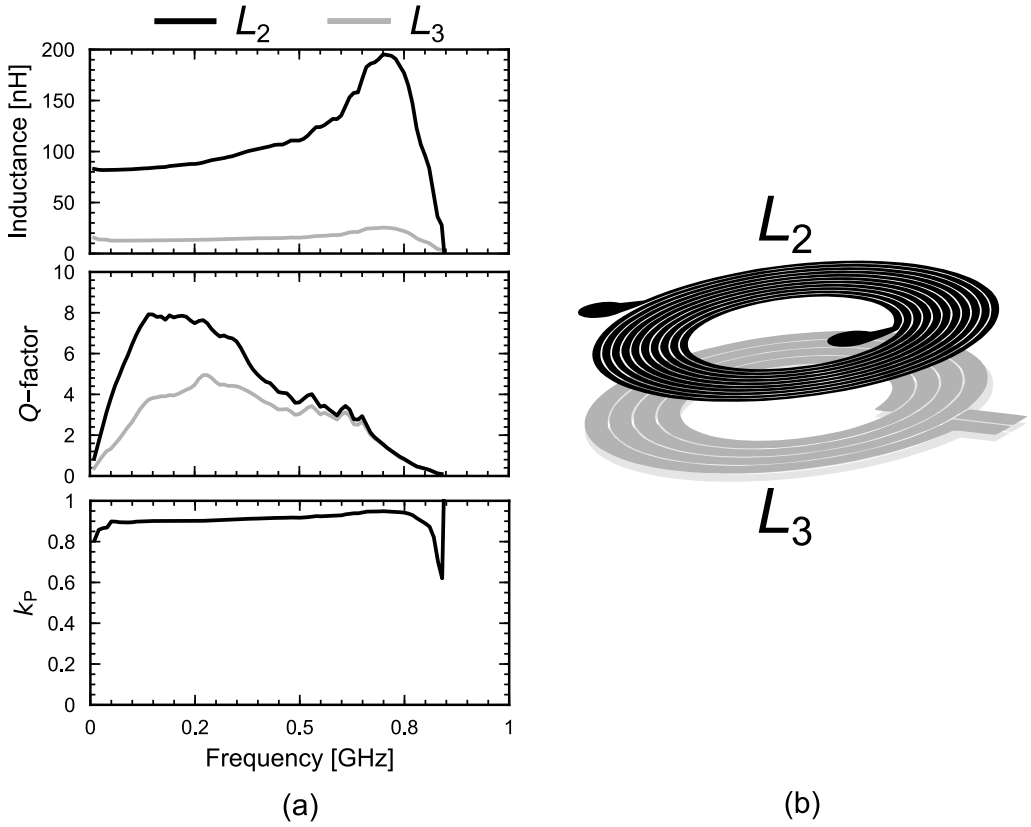


Figure 3.10: Isolation transformer, $T_{\mathrm{ISO,P}}$, of the power link. (a) Electrical performance and (b) 3D view.

factor, k_{P}, as high as 0.92, thus increasing the power transformer efficiency.

As shown in Fig. 3.8, the double isolation network of the feedback control loop consists of the transformer $T_{\mathrm{ISO,C}}$ and capacitors $C_{\mathrm{ISO,C}}$. Differently from the power link, only a small amount of power need to be transmitted through the barriers, so the design of isolation components has been carried out minimizing the component sizes. A 3D-view of the differential transformer $T_{\mathrm{ISO,C}}$ along with its measured single-ended electrical performance are shown in Fig. 3.11. To improve electromagnetic immunity (EMI) of the control link the transformer coils exploit an S-shape implementation. The

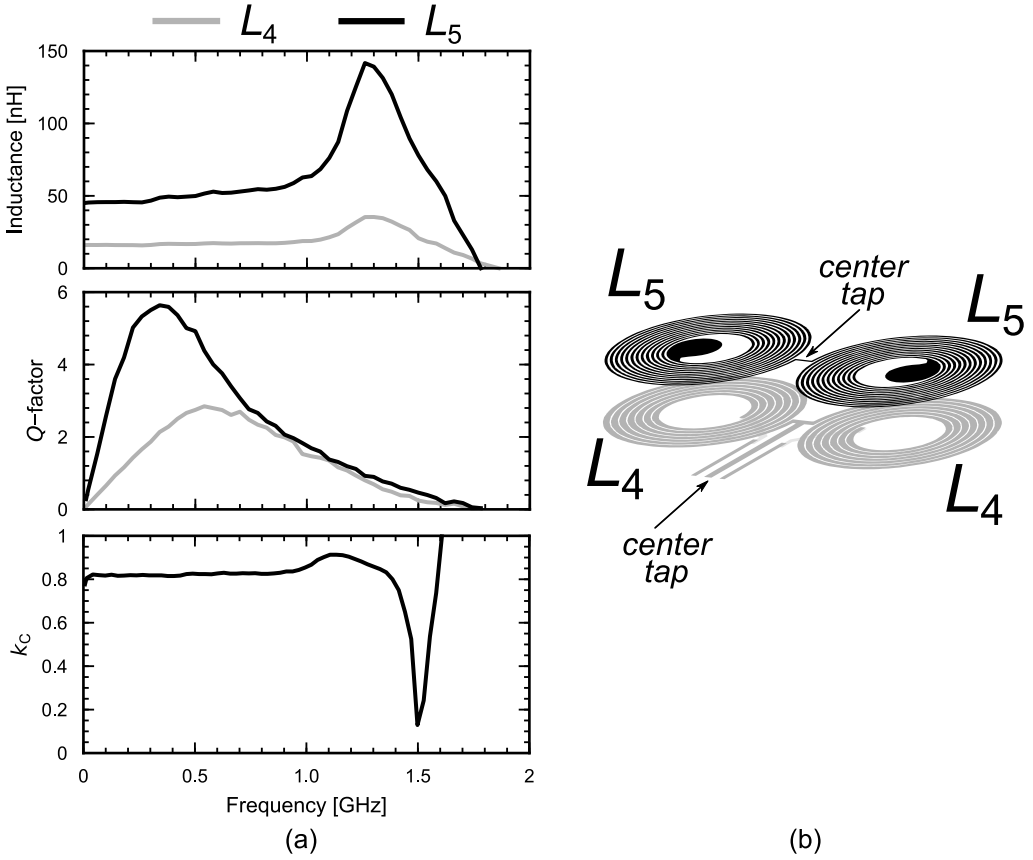


Figure 3.11: Isolation transformer, $T_{\mathrm{ISO,C}}$, of the control link. (a) Sigle-ended electrical performance half-structure and (b) 3D view.

primary and secondary windings L_4 and L_5 are implemented on third and fourth metallization layers, respectively. Primary coil has been designed to maximize the ωQL factor at 1 GHz to increase the control oscillation voltage amplitude [63], while keeping as low as possible its current consumption, $I_{\mathrm{OSC,C}}$. To this aim, an inductance an inductance L_4 of 16 nH has been implemented by means of 7-turns differential coils. To further step-up the control voltage signal, the secondary coil has an inductance L_5 of 45-nH by exploiting a number of turns of 12.5 along with minimum width metals. It is worth noting that to guarantee a high coupling factor, k_{C}, internal and exter-

nal diameters are kept equal for both primary and secondary windings [56]. The isolation capacitors, $C_{\mathrm{ISO,C}}$, are built between the two top metal layers shielded by a metal 1 plane, as done for $C_{\mathrm{ISO,P}}$. In this case, such arrangement allows controlling bottom plate parasitic value that is responsible of the control voltage attenuation. Actually, bottom plate capacitances degrade the transferred signal of a factor around one-fifth, which can be easily compensated by increasing the gain of the PWM controller or the RF control oscillator. A $C_{\mathrm{ISO,C}}$ of 300 fF has been implemented to transmit the control signal, while preserving the silicon area.

For the sake of completeness, Table 3.3 summarizes the geometrical parameters of the inductive components implemented in the power and control links of the dc-dc converter.

Table 3.3: Geometrical parameters of integrated inductors of the dc-dc converter.

Inductor	**No. of turns**	**Width [μm]**	**Spacing [μm]**	**Internal diameter [μm]**
L_1	3.5	40	5	200
L_2	10.5	16	5	450
L_3	4	50	1	450
L_4	7	15	1	160
L_5	12.5	5	5	160

3.6 Experimental results

The micrograph photo of the double-isolated dc-dc converter is shown in Fig. 3.12, along with the main blocks labelled for both dice. They measure

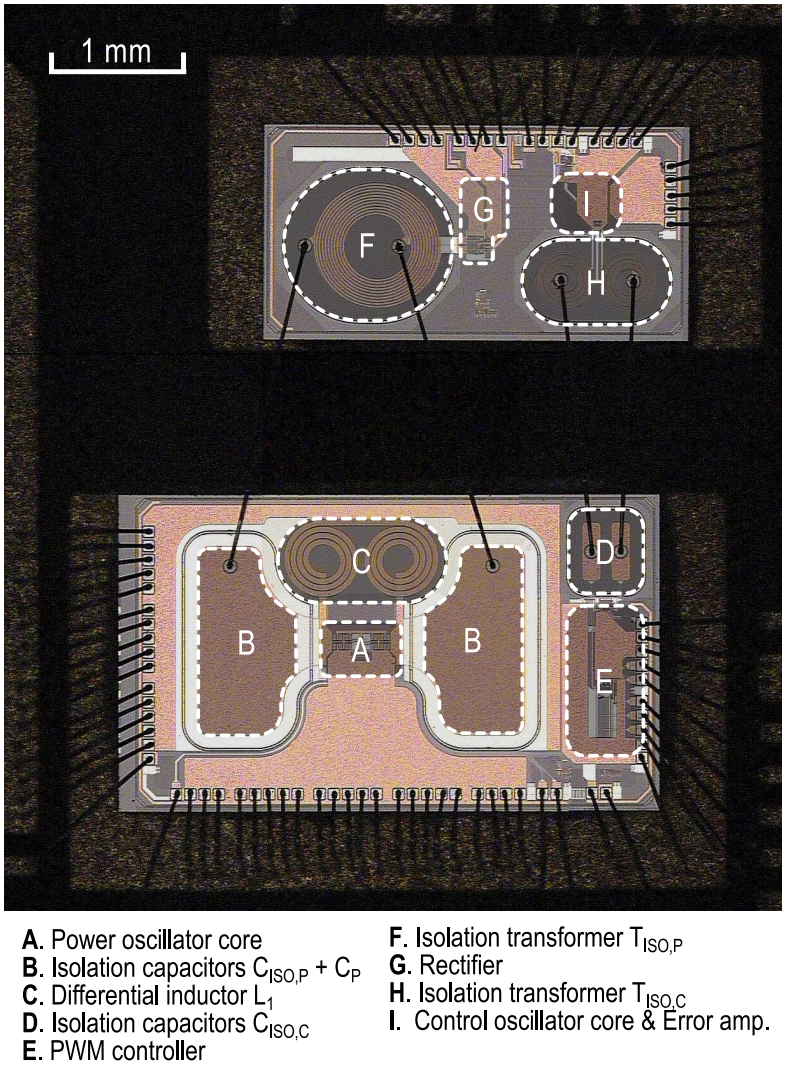


Figure 3.12: Micrograph photo of the dc-dc converter with main blocks labelled.

3.7 mm $\times$ 2.2 mm and 2.95 mm $\times$ 1.5 mm, respectively, whereas passive components required by double galvanic isolation networks (i.e., $T_{\mathrm{ISO,P}}$, $T_{\mathrm{ISO,C}}$, $C_{\mathrm{ISO,P}}$ and $C_{\mathrm{ISO,C}}$) take about one third of the overall silicon area. As apparent, large metal planes and multiple bonding wire connections for both ground and V_{DD} were employed to minimize on-chip and off-chip parasitic

inductances, respectively. Moreover, a proper floorplan was adopted to minimize the cross-talk between the power and control links, taking place on chip and through the bonding wires, as in [49].

Experimental characterization was performed at room temperature and 3.3-V supply voltage, V_{DD}. Firstly, the performance of the dc–ac power conversion was evaluated by mounting the standalone dc-ac converter (i.e., power link oscillator and double isolation network) on a testing board. A discrete passive network was used to account for the rectifier input impedance Z_{R}, which is composed of a resistance (R_{R}) in parallel to a capacitance (C_{R}). The output voltage at the transformer secondary winding was captured by means of a high impedance active probe. Fig. 3.13 reports the ac output power, $P_{\mathrm{OUT,AC}}$, dc-ac conversion efficiency, $\eta_{\mathrm{DC-AC}}$, and oscillation frequency, $f_{\mathrm{OSC,P}}$, measured at the secondary winding of $T_{\mathrm{ISO,P}}$, for different values of R_{R} and C_{R}. The oscillation frequency $f_{\mathrm{OSC,P}}$ varies by less than 10% around its nominal value, as expected.

The complete dc-dc converter was tested at different output power levels, while the output voltage, V_{ISO}, was regulated to 3.3-V by means of the integrated control link. An external 3.2-MHz clock frequency was used as reference to generate the internal 100-kHz PWM signal. The measurement in Fig. 3.14 compares the efficiency, η, versus the output power, P_{ISO}, performance of the complete dc-dc converter with the standalone power link (i.e., without integrated output voltage control [48]). The system delivers up to 100-mW output power with a power efficiency of 16.8%. It is worth noting that at maximum P_{ISO} the losses of power and efficiency due to the integrated double isolated control link are of 10 mW and 0.4 percentage points,

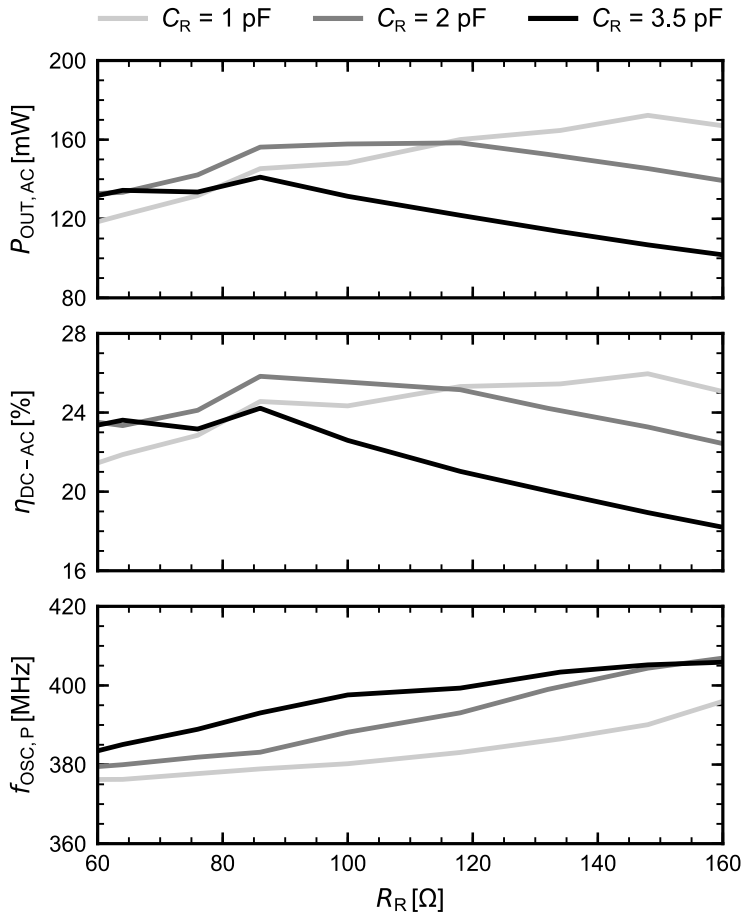


Figure 3.13: Measured ac output power, $P_{\mathrm{OUT,AC}}$, dc-ac conversion efficiency, $\eta_{\mathrm{DC-AC}}$, and oscillation frequency $f_{\mathrm{OSC,P}}$ of the dc-ac converter as a function of rectifier input impedance Z_{R}.

respectively. For higher output power level, η is quite constant with respect to P_{ISO}, thus confirming that output voltage regulation is achieved without significantly affecting the performance of the power link.

Fig. 3.15 shows the transient response of the output voltage V_{ISO} to a step from 2.8 to 3.3 V of the reference voltage, V_{REF}, which corresponds to a variation of P_{ISO} from 65 to 90 mW on a load resistance of about 120 Ω. Two values of the output capacitance, C_{L}, have been used to verify the trade-

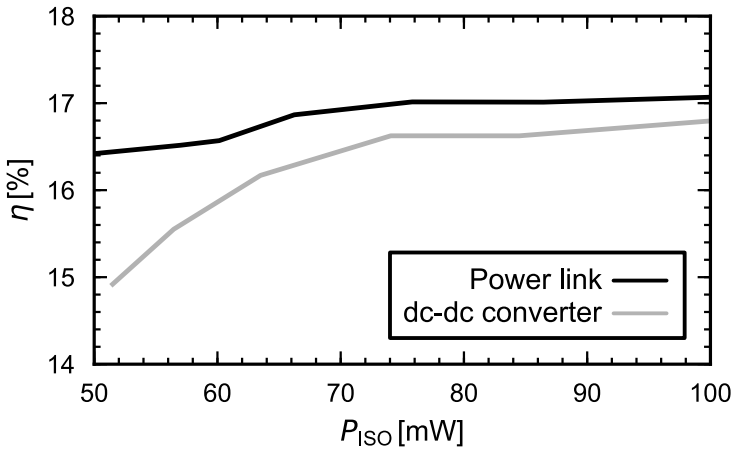


Figure 3.14: Measured power efficiency, η, versus output power, P_{ISO}, with external and on-chip power regulation ($V_{\mathrm{ISO}} = 3.3$ V)

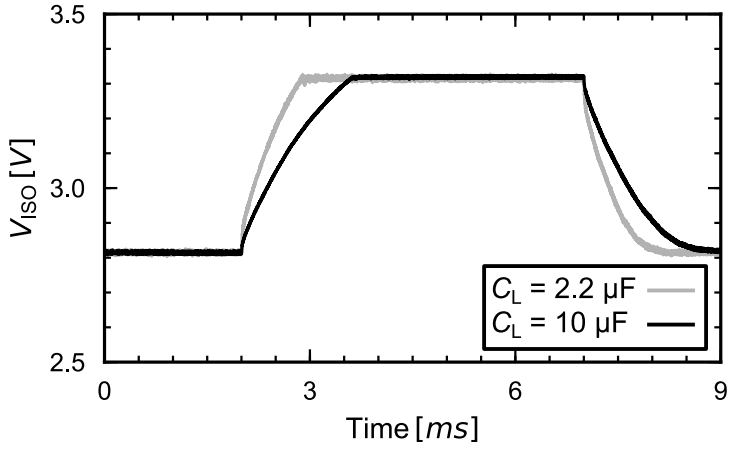


Figure 3.15: V_{ISO} transient response to a step of the reference voltage, V_{REF} from 2.8 to 3.3-V for two values of C_{L} ($R_{\mathrm{L}} = 120\ \Omega$).

off between speed and output ripple, while guaranteeing the stability of the control loop.

Fig. 3.16 shows the start-up transient of the output voltage V_{ISO} for two different values of output capacitance, C_{L}. A V_{REF} of 3.3 V and R_{L} of 160 Ω were imposed, which set the steady-state output power to 68 mW and the

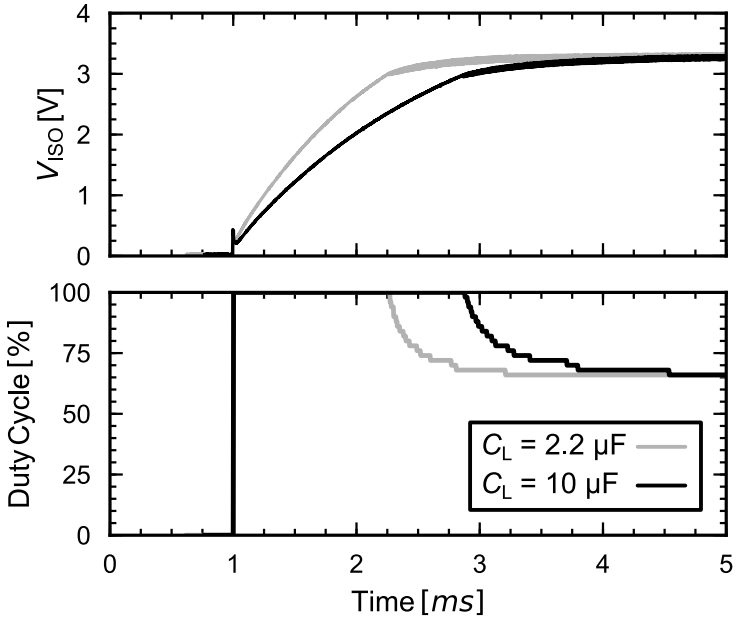


Figure 3.16: V_{ISO} start up transient and corresponding duty cycle of the PWM control signal V_{CTR} ($V_{\mathrm{REF}} = 3.3$ V, $f_{\mathrm{PWM}} = 100$ kHz, $P_{\mathrm{ISO}} = 68$ mW).

duty cycle of the PWM control signal to about 65%. After a delay of about 2 and 3.5 ms, for a C_{L} of 2.2 and 10 μF, respectively, V_{ISO} reaches its steady-state value of 3.3 V.

Finally, Table 3.4 reports a performance comparison with the state of the art of fully integrated dc-dc converters with galvanic isolation. The comparison is carried out only with dc-dc converters with basic isolation since, at the authors' knowledge, no integrated double-isolated dc-dc converters with on-chip output voltage regulation were published yet. Among the dc-dc converters for low-voltage applications, the proposed converter achieves 100 mW of regulated output power with a remarkable power efficiency of 16.8%, outperforming available converters in terms of isolation. On-chip double isolation is achieved on both power and control links thanks to a breakthrough

Table 3.4: Summarized performance and comparison with the state-of-the-art of dc-dc converters with galvanic isolation.

	[28]	[41]	[49]	**This work**
V_{DD}	3.3 V	3.3 V	3.3 V	3.3 V
V_{ISO}	2 V	3.3 V	3.3 V	3.3 V
P_{ISO}	24 mW	10 mW	93 mW	100 mW
η	10.8%	22%	19%	16.8%
$f_{OSC,P}$	330 MHz	200 MHz	350 MHz	400 MHz
Control scheme/ frequency	n.a.[(1)]	Bang-bang/ 1700 kHz	PWM/ 100 kHz	PWM/ 100 kHz
Isolation rating	5 kV (BASIC)	5 kVrms (BASIC)	6 kV (BASIC)	2×5kV (DOUBLE)
Silicon technology	0.35-μm CMOS	0.35-μm DMOS, Schottky diode	0.35-μm BCD	0.35-μm BCD, Schottky diode
Isolation technology	On-chip transformer	Post-processed transformer	On-chip transformer	On-chip capacitors and transformer
Chip no.	2	3	2	2

[(1)]Output voltage is not controlled

converter architecture along with oscillation frequencies as high as 400-MHz and 1 GHz, respectively.

Conclusion

A higher integration level is greatly demanded by the next generation of power converters and different degrees of galvanic isolation are required by certain applications, to ensure circuit protection and human safety. In Chapter 1, an overview of the available state-of-the-art solutions for both isolated data and power transfer has been presented. In this context, dc-dc converters fully integrated in silicon technology represent the maximum achievable level of miniaturization for such power converters, while enabling a considerable cost reduction. This thesis deals with the analysis and design of two dc-dc converters for low power applications, which include integrated basic and double galvanic isolation, respectively.

In Chapter 2 a 300-mW step-up dc-dc converter for gate driver applications has been presented. Galvanic isolation up to 5 kV is performed by the integrated three-windings transformer thanks to the thick oxide layer of the

technology back-end. A novel hybrid-coupling approach for current-reuse oscillators was introduced, which allows to use an area-saving configuration for the transformer. As a result, the power density of the converter was greatly improved with respect to [47], while achieving a competitive power efficiency of 24%.

The strong non-linear interactions between the building blocks of the system and the complex three-windings structure of the transformer require an iterative co-design procedure to achieve the maximum performance in terms of output power, efficiency and power density. To this purpose, a novel lumped and geometrically scalable modelling for three-windings transformers with tapped primary coils has been developed. It has been compared with various EM-simulated structures obtaining an error smaller than 8% for the main electrical parameters.

According to possible real-life applications of this work, additional features would be greatly appreciated. A control loop should be included to regulate output power/voltage, while protection circuitry as short-circuit detection would be needed to improve robustness and reliability. These features have been investigated for a long time, hence various solutions are already available in state-of-the-art and can be easily adopted in this work.

As far as Chapter 3 is concerned, a 100-mW dc-dc converter with double galvanic isolation, addressed to low voltage sensor applications, has been demonstrated. A novel circuit architecture based on the resonant mode operation between the power oscillator and double isolation network has presented, including a simplified design procedure for the power link. The double isolation network exploits integrated transformer and capacitors, thus per-

forming a double 5-kV on-chip galvanic isolation barrier. Power losses due to large bottom plate parasitic capacitances of the isolation capacitors were greatly reduced by including them in the resonant tank of the power oscillator. This allows the converter to achieve a power transfer efficiency of about 17%, which is better than common solutions exploiting series-connected isolation components, i.e. two isolation transformers.

The analysis and design of a novel PWM control loop for the output power/voltage regulation has been presented. Of course, the double 5-kV galvanic isolation is guaranteed also for the feedback loop by using only integrated components. Differently from common PWM control circuits, the duty cycle of PWM control signal is extracted from the peak of an RF signal. This allows such circuit architecture to be used also in a different scenario [49], where data communication is superimposed to the control signal, thus exploiting a single channel to transmit both.

At the authors' knowledge, this is the very first fully-integrated and double-isolated dc-dc converter with on-chip output voltage regulation, which also achieves the highest level of integration thanks to the two-chips implementation.

Additional improvements can be done to make this system more appealing. A short circuit protection would be useful, whereas integrated data communication is highly demanded, especially in medical and sensor applications. Two possible implementations to include data communication could take advantage the approaches proposed in [28] and [49], exploiting either the power or control link, respectively. However, a huge cost-reduction could be achieved by including all power, control and data on a single channel.

APPENDIX A

Publications

Patents

- E. Ragonese, N. Greco and G. Palmisano, "A method of transmitting power and data across a galvanic isolation barrier, corresponding system and apparatus," U.S. Patent *15 138 702*, April, 26, 2016.
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