Fully Integrated Galvanic Isolation Interface in GaN Technology

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***Abstract*— This paper presents for the first time a fully integrated galvanic isolation interface in a GaN technology. It is based on planar micro-antennas and chip-to-chip communication with an on-off keying-modulated RF carrier. This approach can achieve high isolation rating and high common-mode transient immunity by properly setting the distance between chips. The interface provides the isolation channel for a main driver/power switch and the one for the control feedback of the dc-dc converter providing the isolated power supply. Driver and power control channels adopt an RF carrier of 2 GHz and 1.2 GHz, which are modulated by a pulse width modulated signal of 2 MHz and 0.5 MHz, respectively. The interface includes a continuously operating offset compensation approach, which overcomes not only the strong variations due to the large process tolerances of the GaN technology, but also offset drifts due to temperature variations. An accurate pulse width modulated signal with a large duty cycle variation in both channels was achieved. The isolation interface adopts a 6-V power supply, which delivers a quiescent current of 6.3 mA and 7.5 mA to the driver and power control channels, respectively, assuming a signal with a duty cycle of 50%.**

***Index Terms*— Galvanic isolation, GaN technology, micro-antennas, RF oscillator, OOK modulation, RF rectifier, gate driver, switching power converters.**

I. Introduction

GALLIUM Nitride (GaN) High Electron Mobility Transistors (HEMTs) are very promising devices for both switching and RF power applications, thanks to the inherent material properties, such as the wide bandgap and the high mobility, of the two-dimensional electron gas (2DEG) generated at GaN/AlGaN interface [1], [2]. These characteristics allow transistors with higher breakdown, faster switching speed, and lower on-resistance than silicon ones.

In recent years, the GaN technology has been improved to push up power conversion efficiency so that GaN HEMTs are becoming more and more common discrete devices [3], [4].

Manuscript received 2 March 2023; revised 29 May 2023 and 24 June 2023; accepted 14 July 2023. The research activity has been supported by the Electronic Components and Systems for European Leadership (ECSEL) European Project "Gallium Nitride for Advanced Power Applications" (GaN4AP), ECSEL Joint Undertaking (JU) No.101007310. This article was recommended by Associate Editor Y. Tang. *(Corresponding author: Giuseppe Palmisano.)*

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Color versions of one or more figures in this article are available at https://doi.org/10.1109/TCSI.2023.3296200.

Digital Object Identifier 10.1109/TCSI.2023.3296200

Moreover, to enhance performance of GaN power switches a fully integrated circuit (IC) approach has been attempted through the implementation on the same substrate of low-power and high-power GaN transistors, thus overcoming the performance limitations due to parasitic inductances between driver and power switch [5], [6], [7]. This solution minimizes losses and allows higher switching speed, efficiency, and compactness to be achieved. However, the current GaN technology presents several limitations mainly due to the absence of low-power p-channel transistors and wide electrical parameter spread [8], [9], [10], [11].

An important requirement of many switching power systems is galvanic isolation, which makes a wide range of application areas (e.g., medical, smart-home systems, electric vehicles, industrial instrumentations, etc.) compliant with safety and reliability standards [12], [13], [14]. Many isolator solutions based on optocouplers, discrete/integrated transformers and capacitors, etc., have been presented in literature for data transfer up to several tens of Mb/s [15], [16], [17]. Among them, integrated transformers are also able to transfer power with galvanic isolation from few tens of mW up to 1 Watt [18], [19]. They are employed to reduce cost while improving reliability and power density although with a lower power efficiency with respect to discrete implementations.

In this scenario, research efforts have been addressed to the design with all-GaN approaches of integrated basic cells, gate drivers, and power switch systems, including the control circuitry [20], [21], [22], [23], [24], [25], [26], [27], [28], [29], [30], [31]. However, high-performance integrated galvanic isolation is still a prerogative of silicon implementations since it usually needs a high complexity in terms of analog/digital circuitry, which cannot be easily managed by a GaN technology, given its component limitations and the high fabrication tolerances.

On the other hand, the high switching frequency allowed by GaN transistors leads to a high common-mode transient immunity (CMTI), which is in the order of 200 kV/μs. This requirement, along with the introduction of a reinforced galvanic isolation standard at 10 kV, can well be faced with the package-scale isolation approach [32], [33]. Indeed, this approach can be exploited using RF-coupled planar micro-antennas to implement a highly isolated data communication interface [34], [35], [36], [37]. These works show interesting performance, but they are all in CMOS/BCD technologies while no GaN fully integrated implementations are available. On the other hand, the planar micro-antenna approach in the

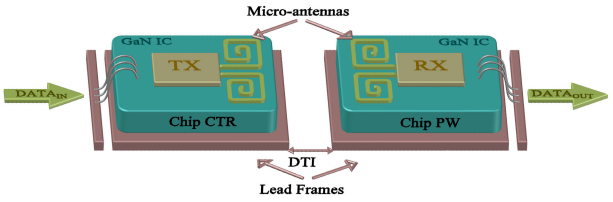

Fig. 1. Simplified representation of the on-package system implementation.

GaN technology is very interesting. Indeed, it allows integration of the galvanic isolation interface with the driver/power circuit, thus achieving a high-performance power switching system with high rating of galvanic isolation and high CMTI.

This paper presents for the first time a fully integrated galvanic isolation interface in GaN technology, which is based on the planar micro-antenna approach and includes two isolation channels, *i.e.,* a driver channel and a power supply control channel. Main design challenges concerned the management of a mixed analog/digital integrated circuit, while overcoming typical GaN technology limitations.

To this purpose, the isolation interface adopts an innovative strategy for offset compensation and noise immunity. Specifically, a dynamic offset compensation was used to face the detrimental effects of the high process tolerances of GaN transistors and the offset drift due to temperature variations. Dynamic offset compensation and noise immunity approaches make the circuit robust against large bias variations and disturbances.

The overall system is made up of two chips, a controller chip (chip CTR) and a power chip (chip PW), as shown in Fig. 1. They should be assembled side-by-side in the package lead frames at a proper distance through insulation (DTI) to guarantee the desired galvanic isolation performance. Chip-to-chip wireless communication with magnetically coupled planar micro-antennas and modulated RF carrier are used for data communication through the isolation interface. Besides a high galvanic isolation rating, the distance between the two chips also guarantees high CMTI.

The paper is organized as follows. Section II deals with the system architecture and the fabrication technology. Section III presents the main system building blocks, such as the micro-antennas, the oscillator, the receiver with the offset compensation strategy, and the signal generator with the pulse width modulation (PWM). Section IV describes measurements and Section V draws conclusions.

II. System Solution

The isolation interface consists of two channels, namely the driver control channel and the power supply control channel. The former is used to drive a power switch through a driver stage to implement a dc-ac switching power converter, the latter performs the feedback path of a dc-dc power converter (i.e., a flyback dc-dc converter) that provides the isolated power supply for the power chip. The simplified block diagram in Fig. 2 shows the isolation interface with a couple of driver/power switches, which together perform a complete system. Indeed, the objective of this work is not a stand-alone isolation interface to be used with an external driver/power

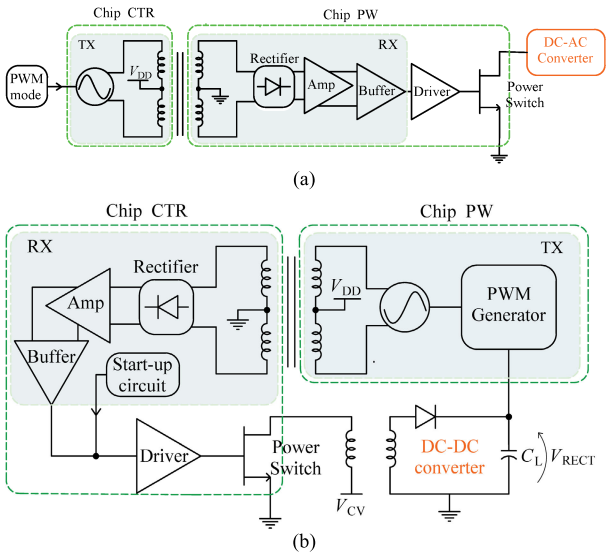

Fig. 2. Example of system application. (a) Driver control channel and (b) power supply control channel.

switch as in traditional implementations. In these last cases, the isolation interface can adopt any technology since it is not constrained to the power technology. The perspective of this proposal is instead to embed the isolation interface with a driver/power switch to achieve a fully GaN high-performance integrated power switching system with a two-chip solution.

Each channel of the isolation interface in Fig. 2 adopts an RF front-end that is composed of a transmitter (TX) and receiver (RX). As mentioned before, the distance (DTI) between chips imposes the isolation rating. The simulated curves in Fig. 3 show the dependence of the micro-antenna insertion loss, *IL*, and the signal amplitude at the receiver input, $A_{\mathrm{IN\_RX}}$, as a function of this distance in the driver channel. In this design, we set 250 μm between chip CTR and chip PW to achieve an isolation rating as high as 12.5 kV assuming a typical molding compound for the package assembly with a dielectric strength around 50 V/μm. With this distance, *IL* and $A_{\mathrm{IN\_RX}}$ are about 58 dB and 250 mV, respectively. As far as CMTI is concerned, the simulation in Fig. 4 shows the response of the micro-antennas of the driver channel to a common-mode transient generated by applying an impulse, V_{CM}, with a slope of 250 kV/μs to the ground of chip CTR. A current impulse, I_{CM}, of 5 mA flows in the metal spirals of the micro-antennas towards the power supply lines and produces a disturbance on the common-mode input voltage of the receiver, $V_{\mathrm{CM\_RX}}$. However, thanks to the connection of the antenna center taps to low-impedance nodes (*i.e.*, ground or V_{DD}), this current does not affect either the TX oscillation or the receiver input signal. Indeed, the RX differential input signal, $V_{\mathrm{IN\_RX}}$, and the output signal, $V_{\mathrm{OUT\_PWM}}$, are not appreciably disturbed by the common-mode transient. As final consideration, the galvanic isolation rating and CMTI performance can be correctly evaluated with a package assembly and considering the specific application.

A. Channel Description

Several challenges were faced to satisfy data transfer requirements through the galvanic isolation barrier and achieve

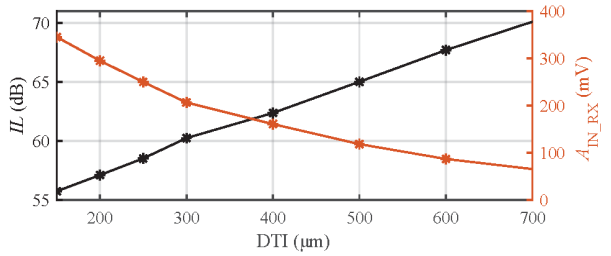

Fig. 3. Micro-antenna insertion loss and receiver input signal amplitude versus the distance between chips.

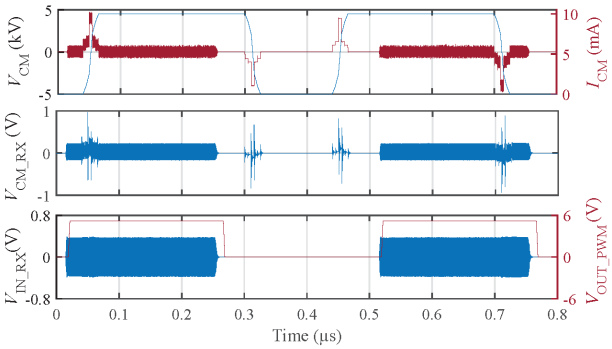

Fig. 4. Simulation of the driver channel with a 250-kV/μs common-mode transient.

an effective integrated implementation in terms of robustness, power consumption, and area occupation, despite the limitations of the GaN technology. As well-known, these limitations come mainly from the absence of a p-channel transistor, the high absolute tolerances of threshold voltages, and the high mismatch between transistor pairs, which have a big impact on the performance of both analog and digital integrated circuits.

Both channels of the proposed galvanic isolation interface share the same data transfer circuitry that is made up of a transmitter (TX), a receiver (RX), and two magnetically coupled coplanar micro-antennas. The TX is performed by an LC oscillator, whose parallel tank exploits a micro-antenna as inductive component. The oscillator provides the RF carrier that is on-off keying (OOK)-modulated by the PWM signal and transmitted through the isolation barrier.

Due to the distance between TX and RX antennas, the RF signal arrives to the RX input with a strong attenuation and hence it must be properly amplified to be recovered. The first circuit of the RX is a rectifier that provides a 6-dB conversion gain. It is followed by a gain stage to further increase the signal level.

The last building block of the RX is a buffer that performs a differential-to-single-ended signal conversion and drives the power section (see Fig. 2). Since the output of the rectifier delivers a low frequency signal whose duty cycle must be accurately preserved, the limitations on the signal amplification due to the offset voltage cannot be overcome with a simple ac coupling. Specifically, an offset compensation approach was used, which also embeds a threshold voltage to guarantee high noise immunity. Besides the TX and RX front-end, the power supply control link includes additional circuits for the generation of the PWM control signal and the start-up of the dc-dc converter. Indeed, the output capacitance, C_L, of the dc-dc converter (see Fig. 2(b)) is initially charged thanks to the start-up circuit that drives the power section with

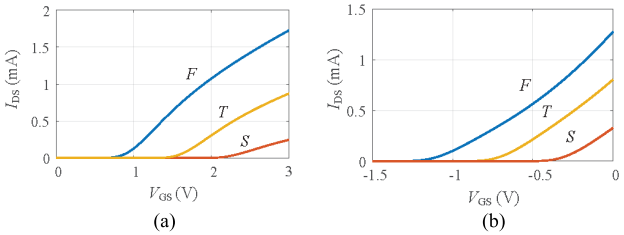

Fig. 5. Drain current versus gate-source voltage for fast (F), typical (T), and slow (S) conditions, for (a) enhancement (W/L = 5/1, V_{DS} = 6 V) and (b) depletion (W/L = 5/0.5, V_{DS} = 6 V) devices.

a locally generated PWM signal until the converter output voltage, V_{RECT}, is high enough to turn on the circuitry of chip PW. Starting from this time, the PWM generator delivers to the RF oscillator a PWM signal whose duty cycle is strictly related to V_{RECT}. This signal is transmitted by the RF front-end from chip PW to chip CTR and then recovered by the RX and delivered to the dc-dc converter.

B. Fabrication Technology

The two chips were implemented in a 0.5-μm GaN on Si technology that includes enhancement (E) and depletion (D) n-channel transistors, capacitors, and resistances. A 650-V power transistor is also available, which allows future integration of the galvanic isolation interface with the power sections.

The technology provides three metal layers for interconnections and inductive component design.

As already mentioned, GaN technology parameters are affected by large spreads. Fig. 5 shows simulations of the I_{DS}- V_{GS} transfer characteristics for both types of transistors under different process corners. Specifically, it shows that the enhancement (depletion) threshold voltage, whose nominal value is about 1.6 V (−0.7 V), becomes 0.9 V (−1,2 V) and 2.3 V (−0.3 V) for fast and slow models, respectively, which means a variation of around 44%. Moreover, also the mismatch between transistors is much higher than the CMOS counterpart. These high process tolerances greatly impact bias point accuracy and power consumption.

III. Main Building Blocks

A. Micro-Antennas

The performance of the micro-antennas is a key aspect of the galvanic isolation interface. Most important parameters are the quality factor (Q) and the magnetic coupling coefficient (k). The former is important to achieve a high oscillation amplitude in the TX local oscillator without an excessive current consumption and to reduce losses in the RX resonant input network. The latter is instead responsible of the coupling loss between TX and RX antennas, which greatly impacts the overall performance of the communication channel.

A rectangular U shape differential configuration was adopted for the micro-antennas as shown in Fig. 6. Proper aspect ratio (*i.e.*, ratio of the longer to shorter side), metal width, and turn ratio between antennas were set to achieve a good trade-off between contrasting requirements such as the coupling factor (k), the quality factor (Q), the self-resonant frequency (SRF), and the chip size [36], [37].

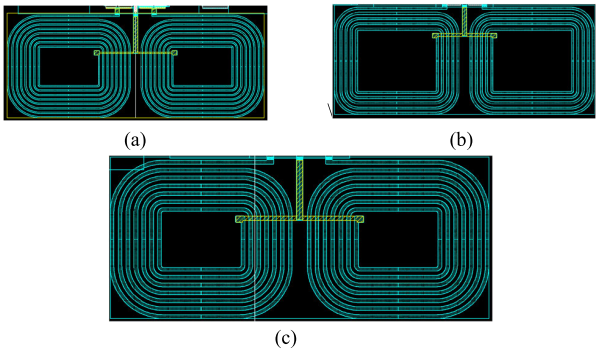

Fig. 6. Layout of the micro-antennas of (a) TX and (b) RX driver channel and (c) TX/RX power supply control channel.

TABLE I
GEOMETRICAL PARAMETERS OF THE MICRO-ANTENNAS

Antenna		n	W [µm]	S [µm]	d_{OUT_MAX} [µm]	d_{OUT_MIN} [µm]
Driver channel	L_{TX}	5	6	8	336	280
	L_{RX}	9	4	8	336	290
Power channel	L_{TX}	7	7	8	346	300
	L_{RX}	7	7	8	346	300

TABLE II
MEASURED PERFORMANCE PARAMETERS OF THE MICRO-ANTENNAS

Parameters	Driver channel		Power channel	Units
	L_{TX}	L_{RX}	L_{TX}/ L_{RX}	
Operative frequency, f_{RF}	2	2	1.2	GHz
Low frequency inductance	20	41.7	26.7	nH
Inductance @ f_{RF}	22.5	47.5	28.8	nH
Q-factor @ f_{RF}	7.6	5.1	7.6	
Self-resonant frequency	6	3.8	4.7	GHz

To this end, the GaN technology takes advantage of a high substrate resistivity and low parasitic capacitances, which allow better Q and SRF to be achieved. The differential configuration with the central tap in both TX and RX is imposed by the CMTI. Indeed, the central tap guarantees a low-impedance path towards the power supply or ground to the common-mode disturbances. Of course, the crosstalk between TX and RX antennas of adjacent channels was carefully considered.

The adopted geometrical parameters are summarized in Table I for each micro-antenna. Besides the number of spirals (n), the metal width (W), and the spacing (S), there are the external longer (d_{OUT_MAX}) and shorter (d_{OUT_MIN}) side of the half inductance. A turn ratio of 1.6 was set in the driver channel to increase the RX input voltage, thus compensating for a lower RF signal due to the higher carrier frequency in this channel. This was accomplished using a smaller metal width for the RX antenna, while maintaining the same overall outer size for each couple of antennas to avoid degradation of the magnetic coupling between them.

Main performance parameters of the micro-antennas are summarized in Table II, which were obtained from s-parameter on-wafer measurements.

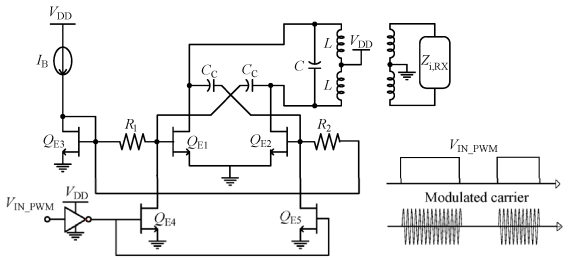

Fig. 7. Schematic of the class D oscillator for the isolation channels.

B. Oscillator

The RF oscillator is a key building block of the isolation channel since it mainly impacts the accuracy of the PWM signal through the communication channel as well as the power consumption of the isolation interface. Indeed, maximum rate, pulse distortion and delay of the PWM signal are greatly related to the oscillator turn on/off times.

Moreover, for a given DTI and hence antenna coupling loss, the oscillation amplitude sets the signal amplitude at the RX input, which to some extent impacts the RX complexity and robustness. Thanks to the GaN technology that exhibits high breakdown voltage, the D-class oscillator in Fig. 7 was adopted [38], which provides an oscillation amplitude as high as 12 V in both channels with a supply voltage, V_{DD}, of 6 V.

On the other hand, the oscillation frequency, f_{RF}, was set to about 2 GHz and 1.2 GHz for the driver and power supply channel, respectively, to reduce crosstalk. However, the main contribution to the crosstalk attenuation in this design comes from the distance between micro-antennas since the selectivity of the resonator at the receiver input is low due to the low Q and hence the relatively wide band.

With these oscillation frequencies, the tank capacitor, C, is still dominant on the parasitic capacitances due to transistors and interconnections. On the other hand, the receiver input impedance does not affect the oscillator tank due to the low coupling coefficient between micro-antennas. Although an optimum design in terms of power consumption would suggest in principle a tank resonance exploiting only the parasitic capacitances, this approach has the drawback of increasing the dependence of the oscillation frequency on the process tolerances.

The coupling capacitors, C_C, besides providing the positive feedback for the oscillator also perform a voltage partition with the gate-source capacitances of the transistor pair, $Q_{E1,2}$, which reduces the gate peak voltage and hence avoids breakdown.

Finally, the OOK modulation of the RF carrier generated by the oscillator is performed using a couple of switches implemented by the transistors, $Q_{E4,5}$, which are driven by the PWM signal and turn on/off the oscillator.

C. Receiver (RX)

A simplified block diagram of the receiver chain is shown in Fig. 8. It is composed of a rectifier, a gain stage with dynamic offset compensation, a buffer, and a phase generator. The receivers of the two isolation channels only differ for the

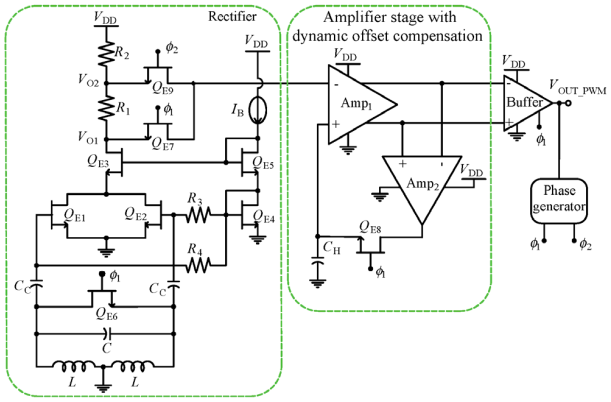

Fig. 8. Receiver (RX) circuit diagram.

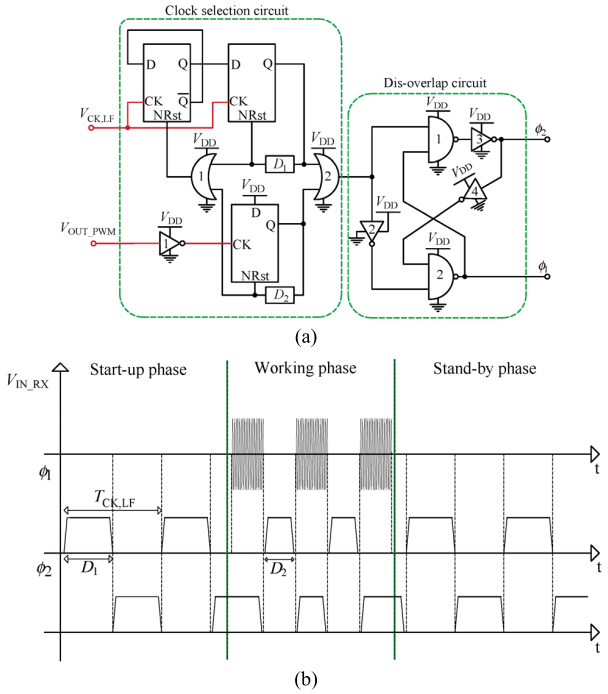

Fig. 9. (a) Phase generator. (b) RF signal and clock phases.

parameter values of the resonant input networks being the RF carrier different for the two channels.

The rectifier exploits a common-source topology [39] based on $Q_{E1,2}$ in series with a common-gate transistor, Q_{E3}, and a resistive load, $R_{1,2}$. It achieves a first gain contribution that avoids the need for RF amplification. Transistors Q_{E1-3} and $Q_{E4,5}$ form a cascode current mirror that defines the rectifier bias current. The antenna is ac-coupled to the receiver input thanks to the capacitors, C_C, and the resistances, $R_{3,4}$. The RX inductor central tap is connected to ground to increase rejection to common-mode disturbances.

The amplifier, Amp_1, increases the signal level whereas the final buffer provides a differential-to-single-ended conversion to drive the power section. The buffer was oversized to also drive the external probe capacitance without excessively impacting the PWM signal. In all the open and closed-loop amplifiers, in which a bias sink current is required, a current generator based on a depletion transistor with degeneration resistance [40] was used instead of the more traditional current mirror, being the latter affected by higher fabrication tolerances.

The receiver requires an offset compensation approach to overcome the offset voltage due to process tolerances, which hinders signal amplification. Moreover, a hysteresis technique is also needed to guarantee robustness against disturbances. To these purposes, the receiver adopts an effective offset compensation strategy that also embeds the hysteresis functionality.

The compensation circuit is made up of the feedback loop that includes Amp_1, Amp_2, and the hold capacitor, C_H. It also uses the switches, Q_{E6-9}, and the clock phases, ϕ_1 and ϕ_2, as shown in Fig. 8. Compensation is performed during phase ϕ_1 by closing switches Q_{E6-8} and charging C_H to the value of V_{O1}. During the next phase ϕ_2, the inverting input of Amp_1 is connected to V_{O2}, which is a ΔV_T higher than V_{O1}, thus forcing the buffer output low when the PWM signal is low or absent. In this way, a kind of hysteresis functionality is performed by exploiting ΔV_T (i.e., the voltage drop across resistance R_1), which hence defines the hysteresis level. In this design, the value of ΔV_T was set to 200 mV to guarantee good noise immunity, whereas the value of the PWM signal at the rectifier output is around 500 mV. When the PWM signal at the receiver input is high, it produces a negative voltage at the rectifier output, which overcomes the hysteresis threshold and switches high the buffer output.

Phases ϕ_1 and ϕ_2 of the compensation circuit exploit two clock signals that are dynamically selected to allow operation in all the operating conditions of the receiver, which are start-up, working, and stand-by conditions.

The phase generator is shown in Fig. 9(a). It is made up of a clock selection circuit and a dis-overlap circuit. The former is composed of three D-Flip Flops, two NOR gates, and two delay blocks, $D_{1,2}$. The latter is the well-known dis-overlap topology. A low frequency clock, V_{CK_LF}, is internally generated by a ring oscillator. It drives the two upper Flip Flops that along with delay D_1 provide a large time slot for the offset compensation during start-up/stand-by conditions. This large time slot is also useful to overcome the slew-rate limitation of the compensation loop in the start-up transient. If during the low value of clock V_{CK_LF} a PWM signal is received (*i.e.*, the working condition starts), the clock of the phase generator is switched to the second clock that is performed by the PWM signal itself. In the working condition, offset compensation is carried out when the PWM signal is low thus preserving the receiver functionality. The time slot for compensation, in this case, is set by a small delay, D_2. It accounts for the minimum time value imposed by the maximum duty cycle and for worst case conditions due to process and temperature variations. In this design, a PWM signal of 2 MHz and 90% of maximum duty cycle was considered, which leads to a minimum time available for offset compensation of 50 ns. Delay D_2 can be set small since there are no slew rate limitations during the working condition. Indeed, capacitor C_H that also provides loop-gain frequency compensation, is already charged to the nominal value during the start-up and only small charge variations are

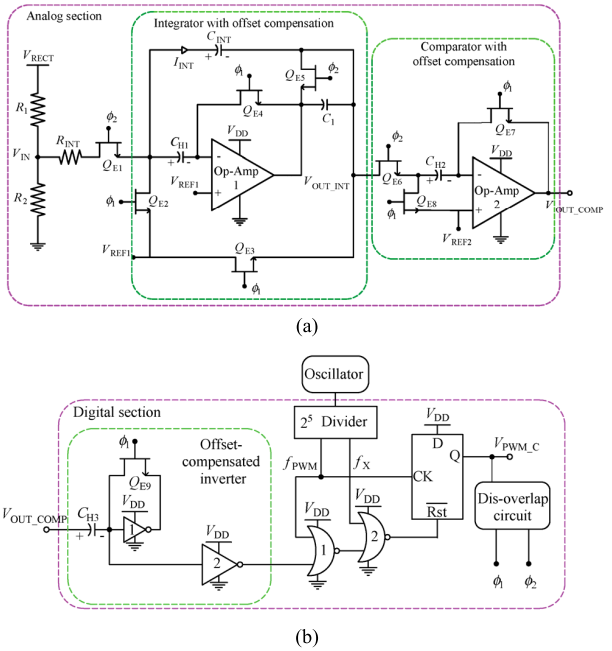

Fig. 10. PWM generator. (a) Analog and (b) digital section.

required during the working condition. The nominal values of D_1 and D_2 were set to 400 ns and 20 ns, respectively.

In case a stand-by condition arises, the phase generator is again switched to the internal clock, V_{CK_LF}. Fig. 9(b) shows the RF signal at the receiver input, V_{IN_RX}, and clock phases ϕ_1 and ϕ_2 during start-up, working, and stand-by conditions. To preserve accuracy, a dis-overlap between clock phases was guaranteed. Moreover, phase ϕ_1 of switch Q_{E8} was slightly delayed with respect to phase ϕ_1 of Q_{E6} to avoid overlap between offset compensation and input signal. The proposed compensation strategy is very effective. Indeed, it overcomes not only the offset voltage due to process tolerances, but also the offset drift caused by temperature variations during the operating conditions.

D. PWM Generator

The PWM generator for the power supply control channel is shown in Fig. 10. The circuit produces a PWM signal, V_{PWM_C}, whose duty cycle is directly related to the rectified voltage, V_{RECT}, at the output of the dc-dc converter (see Fig. 2(b)). The purpose of the duty cycle control is to keep constant the converter output voltage at the desired value. Specifically, if voltage V_{RECT} goes high (low) due to a variation of the load power, the PWM generator will decrease (increase) the signal duty cycle, thus varying the dc-dc converter output power and hence maintaining constant the steady-state value of V_{RECT}. Under nominal conditions, the duty cycle of V_{PWM_C} is set around 50%.

The PWM generator is composed of an analog section and a digital control section, which are shown in Fig 10(a) and (b), respectively. The analog section mainly consists of an offset-compensated switched-capacitor (SC) integrator and comparator. Indeed, offset compensation is mandatory for the accuracy of the analog processing, since the mismatch of GaN transistor pairs is larger and can greatly impact circuit operation. Offset compensation is performed with the SC approach, by using the hold capacitors, C_{H1} and C_{H2}, for the integrator and comparator in the analog side, respectively, and C_{H3} for inverter 1 in the digital side. Offset compensation also needs typical dis-overlapped clock phases, ϕ_1 and ϕ_2, which are performed using the PWM signal as main clock signal to guarantee synchronous operation. Specifically, offset compensation and integration capacitor reset are both performed during phase ϕ_1, which corresponds to V_{PWM_C} low, whereas the main operations of integration and comparison are carried out during phase ϕ_2 with V_{PWM_C} high. The integrator input signal, V_{IN}, is determined by a voltage partition of V_{RECT} using R_1 and R_2. It is applied to the input resistance, R_{INT}, that along with the feedback capacitor, C_{INT}, defines the integrator time constant.

Fig. 10(b) shows the digital section. It incorporates a 2^5 divider, a D-Flip Flop, a dis-overlap circuit, two NOR gates, and the offset-compensated inverter. The divider provides a reference clock frequency, f_{PWM}, for the PWM signal that goes high with the rising edge of this clock. The duty cycle of V_{PWM_C} is generated as follows. The voltage difference between V_{IN} and V_{REF1} across resistance R_{INT} produces a current, I_{INT}, which flows into C_{INT}, thus generating a voltage ramp at the integrator output, V_{OUT_INT}, whose expression is given by

$$V_{OUT\_INT} \approx -\frac{I_{INT}}{C_{INT}} \cdot t + V_{REF1} \approx \frac{V_{REF1} - V_{IN}}{R_{INT} C_{INT}} \cdot t + V_{REF1} \quad (1)$$

As soon as V_{OUT_INT} goes below the comparator reference voltage, V_{REF2}, the comparator switches high and reset the Flip Flop, thus determining the duty cycle of V_{PWM_C}.

Specifically, the ramp slope at the integrator output is related to the value of V_{RECT} and determines the duty cycle, D, of V_{PWM_C}, which is given by

$$D = \frac{t_{on}}{T} \approx \frac{1}{T} (V_{REF2} - V_{REF1}) \frac{R_{INT} C_{INT}}{V_{REF1} - V_{IN}} \quad (2)$$

where t_{on} is derived from (1), as the time at which V_{OUT_INT} is equal to V_{REF2}.

In case of ramp slope too high or too low, the duty cycle is imposed by the digital circuit that sets its maximum and minimum value to around 94% and 5%, respectively.

Finally, the selected control approach is among well-known solutions for dc-dc power converters. It has the advantage of simplicity and inherently exploits the galvanic isolation based on micro-antennas and PWM signal transmission. The drawback lies in the non-linear response as apparent in (2). However, the key aspect of the proposal relies in its implementation tailored for the GaN technology, rather than in the specific control approach. This implementation exploits an analog/digital design strategy in which the accuracy is achieved thanks to both offset-compensated analog circuits and digitally defined minimum/maximum duty cycles. The proposed implementation strategy can easily be arranged for different control approaches.

IV. Experimental Results

The two chips of the galvanic isolation interface were assembled chip-on-board at 250 μm as shown in the photograph in Fig. 11. Driver and power supply control channels

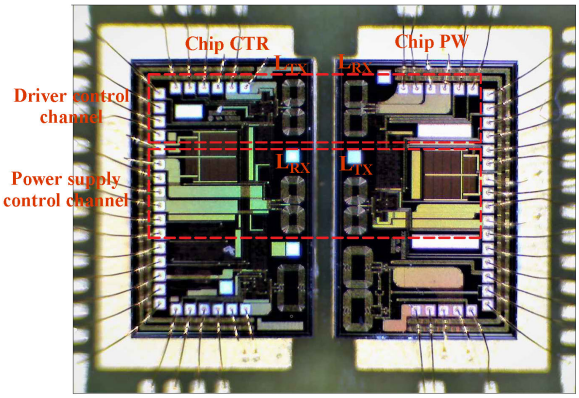

Fig. 11. Photograph of the chip-on-board assembly of the galvanic isolation interface.

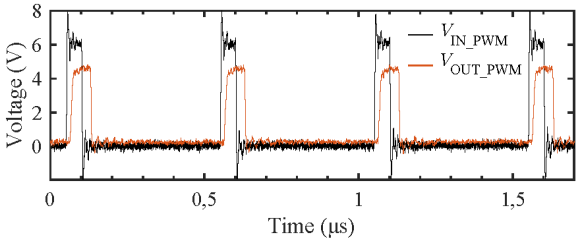

Fig. 12. 2-MHz and 10% PWM signal in the driver channel.

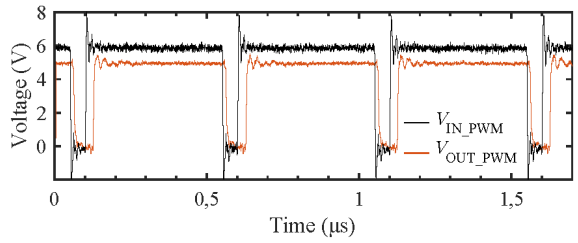

Fig. 13. 2-MHz and 90% PWM signal in the driver channel.

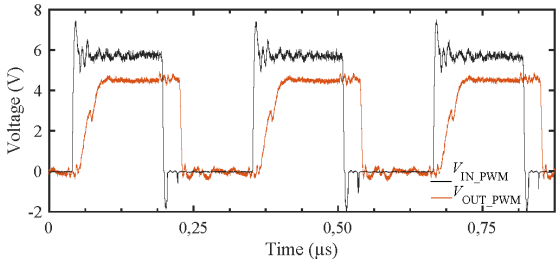

Fig. 14. 4-MHz and 50% PWM signal in the driver channel.

are highlighted by dashed lines. A third channel is shown on the bottom side, which exploits a different approach for the micro-antennas that is not presented in this paper.

The chips are pad limited since various test buffers were included along the signal path of the two isolation channels to allow an exhaustive experimental characterization to be carried out. The two chips have the same overall area of 3.8 mm x 2.3 mm, although the effective circuit area is much lower, and a wide part of the chip is occupied by interconnections to the pads and the third channel in the bottom side.

A power supply of 6 V was used in both channels. Considering a PWM signal duty cycle of 50%, the TX and RX current consumptions are 4.3 mA and 2 mA for the driver channel and 4.5 mA and 3 mA for the power supply control channel, respectively. These currents also include the consumption of

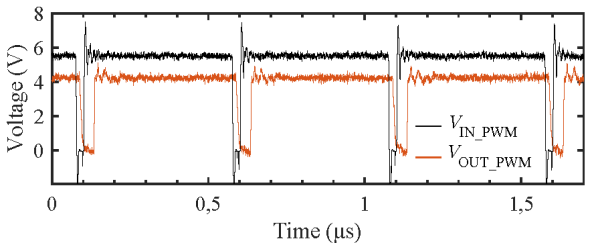

Fig. 15. 2-MHz and 95% PWM signal in the driver channel.

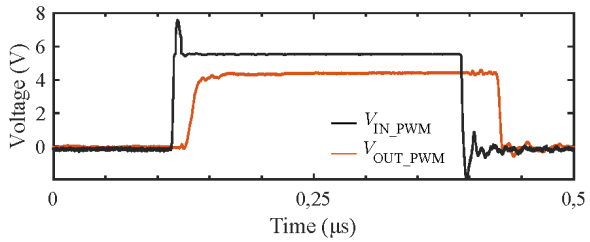

Fig. 16. Details on delay and duty cycle distortion of the 2-MHz 50% PWM signal in the driver channel.

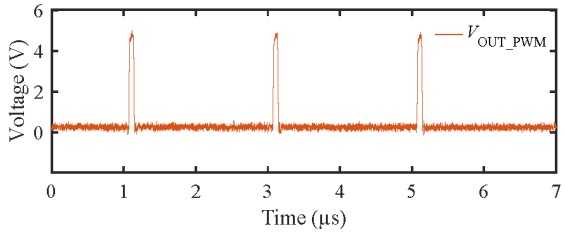

Fig. 17. 0.5-MHz and 6% PWM signal in the power channel.

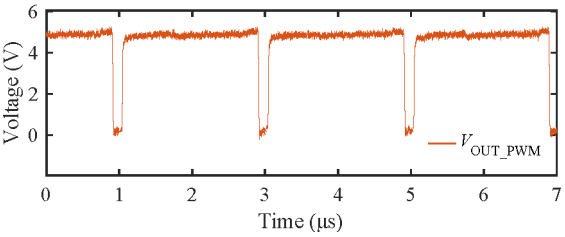

Fig. 18. 0.5-MHz and 94% PWM signal in the power channel.

the test buffers, which is around 1 mA in both channels. The measured oscillation amplitude and frequency for the two TX oscillators closely agree with the expected values mentioned above. The 2-MHz PWM signal at the input and output of the driver channel is shown in Figs. 12 and 13 for duty cycles of 10% and 90%, respectively, whereas a 4-MHz PWM signal is shown in Fig. 14 to demonstrate the maximum frequency capability of the driver channel. The slower rise time at 4 MHz is due to the large load capacitance of the measurement set-up on the output of the test buffer.

Fig. 15 shows a measurement of the driver channel with the maximum allowable duty cycle of 95%. This measure demonstrates that the proposed offset compensation strategy can correctly operate even with a time window as low as 25 ns (*i.e.,* equal to 5% of the PWM period).

Fig. 16 highlights the delay and duty cycle distortion on a 2-MHz 50% duty cycle PWM signal, due to the processing chain of driver channel. Delay and pulse distortion are 30 ns and 18 ns, respectively, and are mainly due to the oscillator, which exhibits different values of turn on/off times. However, the pulse distortion can be greatly improved by properly

TABLE III
SUMMARIZED PERFORMANCE AND COMPARISON WITH THE STATE OF THE ART

Parameters	**[32]**	**[41]**	**[42]**	**[43]**	**[44]**	**This work**
Application	General purpose	Gate drivers	Gate drivers	General purpose	General purpose	Gate drivers
No of isolation channels	4	2	2	2	1	2
Max data/PWM rate	1 Mbit/s	1 MHz	1 MHz	80 Mbit/s	1 Mbit/s	4 MHz[3] 0.5 MHz[4]
Propagation delay [ns]	42	44	28	15.5	11	30[3]
Isolation technology	Face-to-face stacked antennas	Polyimide transformers	On-chip SiO_2 capacitors	On-chip SiO_2 lateral	Polyimide transformer	Planar micro-antennas
Isolation level	(7 kV_{RMS})	(5.7 V_{RMS})	(8 kV_{PK})	(5 kV_P)	(20 kV_{PK})	(>10 kV_{PK})[5]
CMTI [kV/µs]	n.a.	150	100	650	200	> 250[5]
Supply voltage [V]	3.3 V	5	3 / 5.5	5 V	1.7-5.5 V	6 V
Current per channel [mA]	1.65	n.a.	n.a.	1.9[1]	2.8[2]	6.3[3]/7.5[4]
Technology	0.25-µm SOI BiCMOS	n.a.	n.a.	0.25-µm CMOS	0.18-µm CMOS	0.5-µm GaN
Area per channel [mm^2]	n.a.	n.a.	n.a.	0.95	n.a	2.9
No. of dice	2	2	3	2	2	2

[1] At 1 Mbit/s. [2] V_{DD} = 5 V. [3] Driver channel. [4] Power supply control channel. [5] Expected.

delaying the falling edge of the PWM input signal that drives the oscillator.

Fig. 17 and 18 show minimum (6%) and maximum (94%) duty cycles of the PWM signal at the output of the power supply control channel. The signal frequency is 0.5 MHz.

As mentioned in the previous section, the boundary values of the duty cycle and the frequency of the PWM signal in the power supply control channel are set by the digital circuitry of the PWM generator in Fig. 10(b).

Finally, Table III summarizes the measured main performance parameters of the galvanic isolation interface. For completeness, Table III also reports the performance of some typical state-of-the-art solutions of galvanic isolation in silicon technologies since no integrated implementations are available in the GaN technology.

The performance of the proposed galvanic isolation interface is similar to the best silicon works, although a fair comparison between silicon and GaN solutions is not possible, especially when mixed analog/digital integrated circuits are involved as in this work. However, as mentioned before, the objective of this work is not a stand-alone isolation interface as in traditional implementations with silicon technologies. The measured results demonstrate that the proposed GaN isolation interface is suitable for a monolithic implementation with a driver/power switch. This means that a fully GaN integrated power switching system can be pursued, which embeds the galvanic isolation in both driver and power supply control channels.

V. CONCLUSION

An integrated galvanic isolation interface in a 0.5-μm GaN technology has been presented, which is based on chip-to-chip communication and RF coupling between planar micro-antennas. The isolation interface implements two isolation channels, one to drive the power section of a dc-ac converter and the other to perform the feedback control path of a dc-dc converter that provides the isolated power supply. An innovative offset compensation strategy has been also discussed, which guarantees accurate biasing and robust operation. Measurements have been presented that well validate the galvanic isolation interface and demonstrate that a high-performance fully GaN integrated power switching system with galvanic isolation is feasible.

ACKNOWLEDGMENT

The authors would like to thank Alessandro Castorina, Mariantonietta Rizzo, and Egidio de Giorgio of STMicroelectronics, Catania, Italy, for their support in measurements and layout, respectively.

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Open Access funding provided by 'Università degli Studi di Catania' within the CRUI CARE Agreement