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# 0.9-V CMOS cascode amplifier with body-driven gain boosting

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SUMMARY

The body-driven variant of the gain-boosting technique is here exploited to design a CMOS transconductance amplifier with minimum supply below 1 V. When compared with the conventional gain-boosting technique, the proposed body-driven approach reduces the minimum supply requirement by two thresholds in a rail-to-rail amplifier exploiting two complementary input stage topologies. Simulations using a 130-nm process show that a 0.9-V power supply is adequate for a single-stage rail-to-rail amplifier providing a 56-dB gain, which is 18 dB higher than that achieved by the same architecture but using the traditional cascoding approach. The main drawbacks are that the solution requires a twin-tub process and an additional bias section. Copyright © 2008 John Wiley & Sons, Ltd.

KEY WORDS: low voltage; low power; gain boosting; body driven; bulk driven

## 1. INTRODUCTION

The maximum achievable voltage gain of a simple single-stage amplifier implemented in deep submicron CMOS technologies is becoming unsatisfactorily low because of the progressive reduction in the transistor small-signal output resistance [1]. Although it is a good practice in analog applications to set the channel length of critical transistors not lower than 2–4 times $L_{\min}$ (i.e. the minimum allowed by the technology), greater channel lengths cannot be easily adopted without losing the speed advantages offered by the advanced technology. Therefore, increasing the channel length in order to boost the transistor output resistance is not a viable solution. A possible remedy to the gain reduction is the adoption of multistage amplifier topologies (cascading approach) [2–7]. By using simple low-voltage gain stages, the minimum supply requirement is preserved and voltage gain is increased. Unfortunately, an amplifier with more than two gain stages requires invariantly some kind of (nested) Miller frequency compensation technique that limits the maximum achievable bandwidth. An efficient technique to increase the voltage gain without severely impairing

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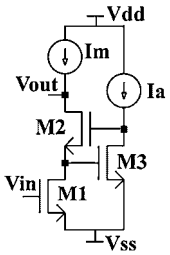


Figure 1. Simplified schematic of a standard gain-boosted amplifier.

bandwidth is cascoding. However, the simple cascoding scheme cannot be tolerated in a low-voltage context, so that several low-voltage approaches have been devised. In addition, to increase the gain of a single-stage amplifier even further (up to three or four equivalent simple gain stages) gain boosting can also be employed. In a gain-boosted amplifier, since Miller compensation is avoided, we do not incur in the frequency limitations exhibited by the cascading approach.

The well-known standard way to implement a gain-boosted amplifier is depicted in Figure 1, where M1 is the common-source amplifier, M2 is the cascode transistor and M3 is the auxiliary gain-boosting stage [8]. Current generators $I_{\mathrm{m}}$ and $I_{\mathrm{a}}$ are used for biasing purposes. In particular, $I_{\mathrm{m}}$ must be implemented through a cascoded approach to avoid decreasing gain. The auxiliary amplifier can be dimensioned through optimized design approaches [9–11]. It does not need to be excessively fast, even though a pole-zero doublet at high frequency may limit settling time [12, 13].

The minimum supply requirement of the circuit can be easily evaluated by inspection of Figure 1, following the $V_{\mathrm{SS}}$-to-$V_{\mathrm{DD}}$ path from M3, M2 and $I_{\mathrm{a}}$. To keep all the transistors in saturation, assuming $I_{\mathrm{a}}$ implemented by a single transistor, we need two gate-source voltages plus one saturation voltage, or equivalently $2V_T+3V_{DSsat}$. Of course, some headroom must be left to preserve signal swing; hence, supply lower than 1 V can be hardly adopted even assuming thresholds as low as 0.3 V. Straightforward small-signal analysis shows that the auxiliary loop gain provided by M3 is $g_{m3}r_{o3}$, where $g_{m3}$ is the transconductance of transistor M3 and $r_{o3}$ is the total resistance at the drain of M3. Therefore, the voltage gain $v_{\mathrm{out}}/v_{\mathrm{in}}$ is equal to $-g_{m1}g_{m2}g_{m3}r_{d1}r_{d2}r_{o3}$.

To achieve very low-voltage operation, the utilization of the MOS body terminal has been investigated until recently [14–22]. In this context, a gain-boosted approach that exploits the body of the auxiliary gain-boosting transistor as input terminal was proposed independently in [23, 24]. Compared with the standard approach, it decreases the supply demand of about one threshold in the simple structure. In a rail-to-rail amplifier topology, which is usually made up of two complementary sections, two thresholds are then saved. The solution requires a triple-well technology to allow the independent control of the body of n- and p-channel MOS devices. As a result, amplifiers with gain in the range of 50–60 dB, under power supplies below 1 V, become in principle possible nowadays with deep submicron technologies.

## 2. BODY-DRIVEN GAIN BOOSTING

The simplified schematic of a body-driven gain-boosted stage is illustrated in Figure 2. It is similar to the one in Figure 1, the main difference is that now transistor M3 is driven by the body terminal,



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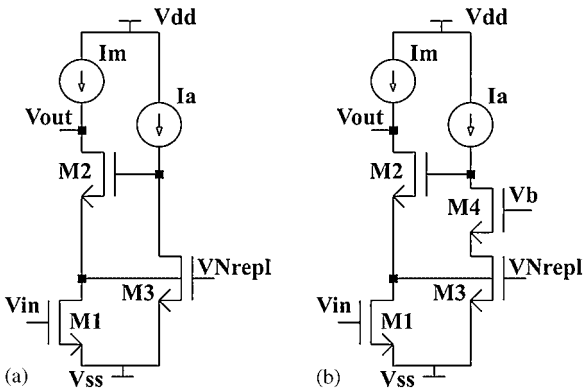


Figure 2. Simplified schematics of the proposed body-driven gain-boosted topology: (a) simple and (b) cascoded.

whereas its gate voltage is kept to a constant value, $V_{\mathrm{Nrepl}}$. It is worth noting that the bias voltage $V_{\mathrm{Nrepl}}$ plays a key role for the practical implementation, as will be discussed shortly.

The minimum supply voltage keeping all transistors in saturation is $V_T + 3V_{\mathrm{DS,sat}}$, thus saving a threshold compared with the conventional gain-boosting approach in Figure 1.

In this case the small-signal gain is $-g_{m1}g_{m2}g_{mb3}r_{d1}r_{d2}r_{o3}$, where $g_{mb3}$ is the source-bulk transconductance of M3, which is typically smaller than the gate-source transconductance by about one order of magnitude. Additionally, one can also cascode transistor M4, as in Figure 2(b). This increases the supply demand by one saturation voltage, because current generator $I_{\mathrm{a}}$ must also be implemented by means of a cascode structure, but the loop gain is increased by an additional gain stage. In this case the small-signal gain is $-g_{m1}g_{m2}g_{mb3}g_{m4}r_{d1}r_{d2}r_{d3}r_{o4}$.

If we assume the standard expression for the threshold voltage, as a first approximation, the required $V_{\mathrm{Nrepl}}$, once $I_{\mathrm{a}}$, $V_{SB3}$ and $(\mathrm{W/L})_3$ are chosen, is expressed in terms of the Fermi potential, $\phi_F$, and zero-bias threshold, $V_{T0}$, as

$$V_{\mathrm{Nrepl}} = \sqrt{\frac{I_{\mathrm{a}}}{K_n(W/L)_3}} + V_{T0} + \gamma\left(\sqrt{2\phi_F - v_{\mathrm{BS}}} - \sqrt{2\phi_F}\right) \tag{1}$$

where, as usual, $K_n$ is the MOS transconductance factor.

This voltage must be chosen properly, so as to avoid that the bulk-source junction of M3 becomes forward biased (at this purpose, a source-bulk voltage lower than 0.4 V can be considered as a safe bound to limit the junction current). Moreover, it must be avoided that transistor M1 enters the triode region. In conclusion, a bulk-source voltage of about 100 mV can be sufficient to keep M1 in saturation, while causing a negligible current flowing in the bulk-source junction.

A possible biasing circuit providing voltage $V_{\mathrm{Nrepl}}$ is depicted in Figure 3. It implements a replica circuit embedded in a negative feedback loop acting as described below. Transistors M22, M18, M19 and M23 are, respectively, a replica of M1, M3, M4 and M2 in Figure 2. As already mentioned, cascoding transistor M19 is used to further increase the loop gain, this requires cascoding also in the p-channel side (M20–M21). Transistor M21 is a bias current generator that provides a replica of $I_{\mathrm{a}}$ in Figure 2. Transistors M15–M17 form a differential amplifier that sets the gate voltage of M23 to the analog ground, $(V_{\mathrm{DD}} + V_{\mathrm{SS}})/2$, while forcing the current into M18–M19 to equal $I_{\mathrm{a}}$.



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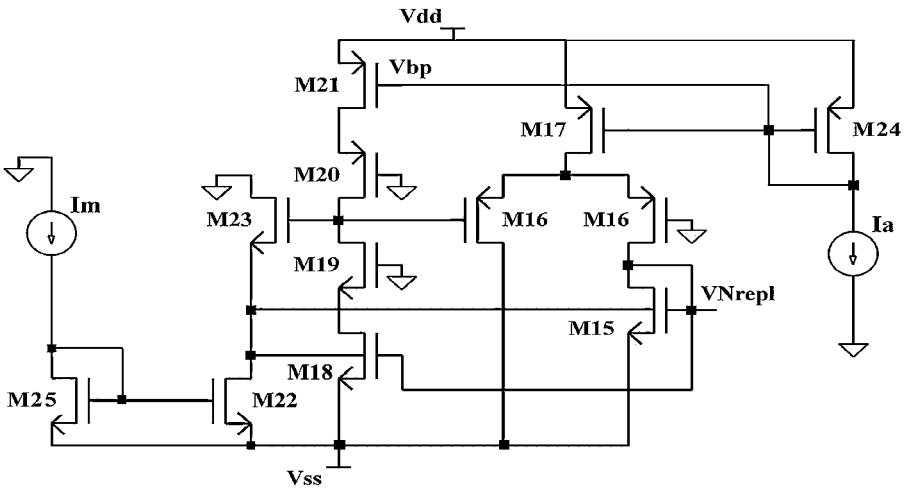


Figure 3. Circuit for the generation of the required bias voltage $V_{\mathrm{Nrepl}}$ for auxiliary gain-boosting amplifier in Figure 2(b).

Note the mirror action of M15–M18 and that both transistors have the same body voltage. The circuit forces the body of M18 to $V_{\mathrm{GND}}-V_{\mathrm{GS},23}$, which is slightly higher than the saturation voltage of M22, in order to have a margin before entering the triode region. In principle, the gate of M16 can be set to a different voltage to set in turn a different bias point for the body of M18.

It should be finally observed that the supply requirements of the chosen bias circuit is $2V_T + 4V_{\mathrm{DS,sat}}$ (caused by transistors M22, M23, M16 and M17), which is more than that required by the basic body-driven gain-boosting circuit. However, this does not constitute a real problem in the design of a complete OTA because a complementary input stage OTA topology is mandatory to obtain rail-to-rail operation under very low supply. Otherwise, non-complementary solutions would provide strongly limited (if not useless at all) common-mode input ranges.

## 3. DESIGN OF A RAIL-TO-RAIL BOY-DRIVEN GAIN-BOOSTED AMPLIFIER

Figure 4 shows the schematic of the proposed transconductance amplifier. The circuit exploits a folded cascode architecture and uses two complementary input sections (M6–M7 and M8–M9, plus bias current generators M5 and M10) to provide input rail-to-rail operations. Of course, the differential output nature of the OTA requires a common-mode feedback circuit (not shown in the figure), it can be accomplished with one of several well-known techniques, including the switched-capacitor approach, suitable for very low-voltage supplies. Additional strategies, like either pseudo-differential approaches or common-mode control via the body terminal [16–21], can be exploited to eliminate the tail current generator and decrease supply demand.

The common-mode feedback loop (CMFB) has been implemented by means of a standard switched-capacitor loop employing transmission gates and MIM capacitors. The use of transmission gates is possible since the supply voltage is higher than $2V_T$. Cascode transistors M7 and M8



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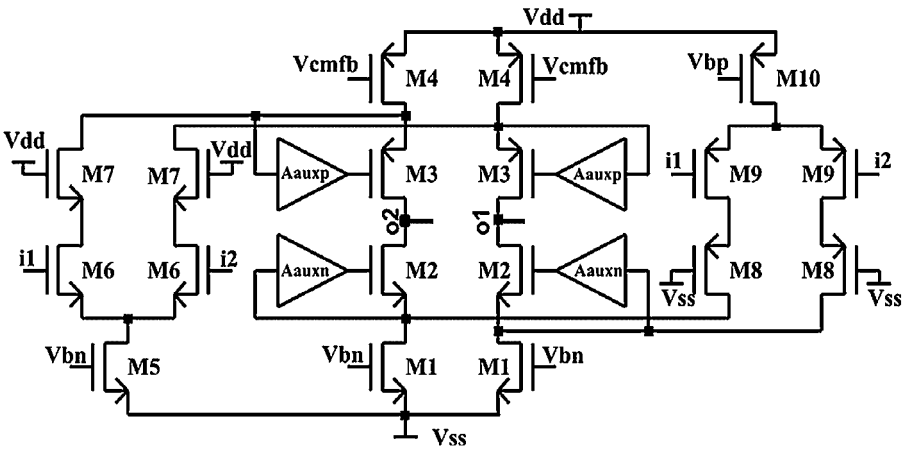


Figure 4. Gain-boosted OTA (CMFB section not shown).

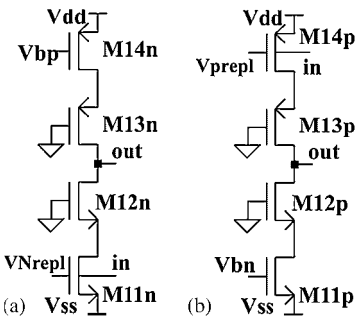


Figure 5. Implementation of blocks Aauxn (a) and Aauxp (b) in Figure 4.

increase the gain of the stage, their gate voltages can be set to $V_{DD}$ and $V_{SS}$, respectively, ensuring that all transistors work in saturation.

Using deep submicron technologies, the cascode structure alone is no longer sufficient to provide even moderate gains (e.g. about 60 dB). Therefore, we exploit the proposed body-driven gain-boosting approach to increase dc gain while preserving low supply capability and without strongly affecting bandwidth.

The auxiliary gain-boosting amplifiers are labelled with $A_{auxn}$ and $A_{auxp}$ in Figure 4. Their implementation is detailed in Figure 5, in which the input terminal is the body of M11n and M14p, respectively. Note that the gates of M12 and M13 are tied to the analog ground $(V_{DD}+V_{SS})/2$. The reference voltage $V_{Nrepl}$ is generated by the replica loop section already discussed in Figure 3. In particular, M18, M19 and M22 are matched with M1, M2 and M3, respectively. M21 supplies a replica of current $I_m$.

A complementary topology as that in Figure 3 (not shown) is used for the generation of the appropriate biasing voltage $V_{Prepl}$ for the auxiliary amplifier $A_{auxp}$.



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In conclusion, the minimum supply voltage of the amplifier in Figure 4 is $2V_T+4V_{\mathrm{DS,sat}}$, that is the same as that required by a simple cascoded architecture (i.e. the amplifier in Figure 4 with the gates of M2 and M3 kept to a constant value). In contrast, the minimum supply of the conventional gain-boosted amplifier (employing the structure in Figure 1) is $4V_T+4V_{\mathrm{DS,sat}}$.

It should be recognized that the proposed solution requires additional area and current consumption for the biasing section. However, a single bias circuit is usually necessary for more than one amplifier used as a VLSI cell. Hence, apart form the requirement of a triple-well technology, the main drawback of the proposed solution is the noise increase. Specifically, the input-referred noise voltage power density is expressed as

$$S_{V,\mathrm{in}}=\overline{v_{n,\mathrm{in}}^2}=\frac{g_{m1}^2S_{V1}+g_{m9}^2S_{V9}+g_{m4}^2S_{V4}+g_{m6}^2S_{V6}}{(g_{m9}+g_{m6})^2}+\frac{S_{V,An}}{(g_{m9}+g_{m6})^2r_{o1}^2}+\frac{S_{V,Ap}}{(g_{m9}+g_{m6})^2r_{o4}^2} \tag{2}$$

where $S_{Vi}=4kT(2/3g_{mi})$ is the gate-referred noise power spectral density of the $i$th transistor and the input-referred noise of the auxiliary amplifiers is

$$S_{V,An}=S_{V,11n}\left(\frac{g_{m11n}}{g_{mb11n}}\right)^2+S_{V,14n}\left(\frac{g_{m14n}}{g_{mb11n}}\right)^2 \tag{3a}$$

$$S_{V,An}=S_{V,14p}\left(\frac{g_{m14p}}{g_{mb14p}}\right)^2+S_{V,11p}\left(\frac{g_{m11p}}{g_{mb14p}}\right)^2 \tag{3b}$$

Of course, the last two terms in (2) take into account the contribution of the auxiliary gain-boosting amplifiers. This contribution is absent in the standard cascode, while in the conventional gain-boosting approach the transconductances $g_{mb11,n}$ and $g_{mb14,p}$ must be replaced by the gate-source transconductances. Since the ratio $g_{mi}/g_{mbi}$ is usually about equal to 10, this explains the worst noise performance of the body-driven gain-boosting approach.

For what concerns the frequency response, the amplifier's behaviour is the same as a standard gain-boosting topology, except for the transconductance of the auxiliary stage, which is a body transconductance. Therefore, the dominant pole, the second pole and the zero have the same expression as for instance given in [9–11]. The parasitic BJT transistor due to body driving [19] is negligible because of the low $V_{\mathrm{DS}}$ and $V_{\mathrm{BS}}$ of the body-input devices.

An alternative implementation is to use two body-driven fully differential amplifiers as auxiliary gain stages: one $n$-type and the other $p$-type. These two stages may be implemented by a folded cascode or a telescopic cascode structure. This may reduce offset, but would require two additional CMFB loops and complicates the circuit biasing. Besides, a perfectly symmetrical layout is straightforward when using our topology.

## 4. SIMULATION RESULTS

The proposed amplifier in Figure 4 was simulated using the process parameters of a 130-nm CMOS technology with thresholds around 0.25 V, respectively. The saturation voltage $V_{\mathrm{DS,sat}}$ was



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Table I. Design parameters of the proposed amplifier.

| Component | Value |
|---|---|
| M1 M5 | 20/0.26 |
| M2 M6 M7 | 5/0.13 |
| M3 M8 M9 | 15/0.13 |
| M4 M10 | 60/0.26 |
| M11n,p M12n,p | 1.5/0.13 |
| M13n,p M14n,p | 9/0.26 |
| $I_{M1} = I_{M4} = I_{M5} = I_{M10}$ | 100 μA |
| $C_C$ | 350 fF |

approximately set to 50 mV. This allowed us to accommodate a 0.9-V supply while maintaining all transistors in saturation for a $\pm V_T$ output swing. Transistors aspect ratios and other component parameters are summarized in Table I. Observe that minimum channel length was intentionally chosen for active devices whereas $2L_{min}$ was chosen for active load devices in order to provide a slight increase in the output resistance and reduce the channel length modulation effects (causing systematic offset). The quiescent current of the main amplifier was 500 μA (the current consumption of the biasing networks was set to 150 μA). To estimate the frequency behaviour of the amplifier, a load capacitor of 350 fF was assumed, which also provides dominant-pole compensation.

Standard cascoded and gain-boosted versions of the amplifier were designed and simulated for comparison. The same total current consumption, output linear range and load capacitance were assumed. In particular, the first assumption allows a larger standby current in the input-stage OTA and in turn a higher transconductance, $g_{m\_in}$ (and hence unity-gain frequency, $g_{m\_in}/C_L$) to be achieved in the standard cascode and gain-boosting versions. Observe also that while the cascoded topology required the same 0.9-V supply, the conventional gain-boosted amplifier required a 1.2-V supply. The ratio of bandwidth to power consumption is the same in the gate-driven and in the body-driven gain-boosting stages and may be better in the body-driven gain boosting if the two biasing loops are used to bias more than one amplifier. This gain is due to the lower supply voltage.

The loop gain frequency response (magnitude) of the three amplifiers is shown in Figure 6. It has to be noted that the typical gain per stage in the adopted technology is lower than 20 dB. The DC gain, unity-gain frequency, phase margin and gain margin of the designed amplifier with the associated standard deviations obtained through Monte Carlo simulations (accounting for devices mismatching) are, respectively, 56 dB (1.6 dB), 570 MHz (10 MHz), 65° (1.1°) and 31 dB (1.0 dB). As expected, the obtained gain is almost equivalent to that of three stages. As can be seen from the data collected in Table II, the proposed circuit provides a gain improvement of 18 dB over the simple cascoded version, with a 30% reduction in the unity-gain frequency. The conventional gain-boosted approach provided a 63-dB DC gain and a unity-gain frequency of 790 MHz.

The transient response of the three amplifiers in unity-gain configuration is shown in Figure 7, for a 1.2 $V_{pp}$ differential input signal. Settling time at 5% of the final value is 2.3 ns for the proposed circuit, whereas the standard and gain-boosted ones give 1.6 and 2.1 ns, respectively. As expected, noise increases from the standard cascode and gain-boosted to the body-driven gain-boosted amplifier. Table II summarizes the input-referred white noise contributes of the three amplifiers.



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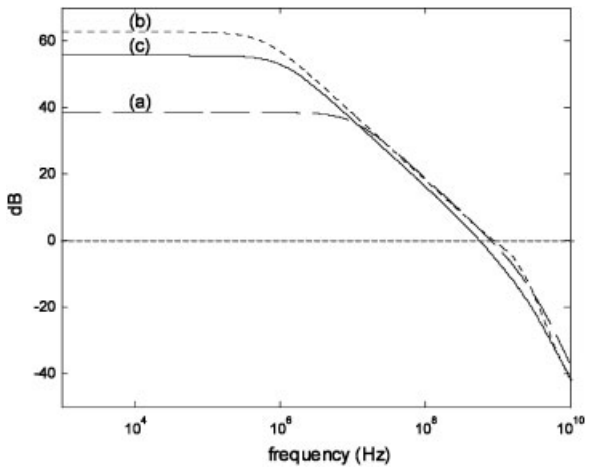


Figure 6. Loop gain frequency response of the three amplifiers: (a) standard; (b) gain-boosted; and (c) body-driven gain-boosted cascoded.

Table II. Performance comparison of the amplifier using standard cascoding approach, standard gain boosting and body-driven gain boosting.

| Parameter | Unit | Standard cascoded | Standard gain boosted | This work |
|---|---|---|---|---|
| Supply* | V | 0.9 | 1.2 | 0.9 |
| $I_{TOT}^{\dagger}$ | μA | 650 | 650 | 650 |
| Load capac. | fF | 350 | 350 | 350 |
| Gain | dB | 38 | 63 | 56 |
| $f_U$ | MHz | 820 | 790 | 570 |
| Phase margin | Deg | 66 | 72 | 65 |
| Gain margin | dB | 23 | 15 | 31 |
| Slew rate | V/μs | 900 | 750 | 700 |
| Settling time | ns | 1.6 | 2.1 | 2.3 |
| CMRR@dc | dB | 64 | 94 | 81 |
| PSRR@dc | dB | 63 | 101 | 82 |
| Input noise | $nV/\sqrt{Hz}$ | 10 | 12 | 32 |

*Providing an output swing of $\pm V_T$.

†Part of this current (150 μA) is used by the proposed circuit in the bias section.

## 5. CONCLUSIONS

In this paper we have presented and discussed the design of a rail-to-rail CMOS transconductance amplifier powered form a single 0.9-V supply. The amplifier exploits a single-stage cascoded topology that is based on a body-driven gain-boosting approach. By using the body terminal of the auxiliary gain-boosting transistor as feedback input terminal supply requirements are reduced. As a consequence, the approach can be advantageously adopted in the design of sub-1V CMOS amplifiers while compensating for the reduction in gain of deep submicron CMOS technologies.



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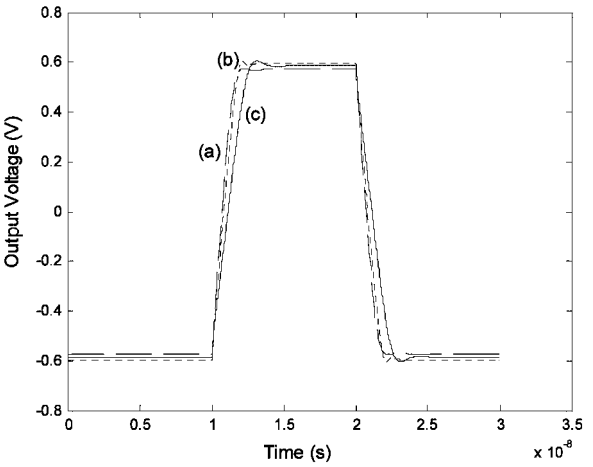


Figure 7. Step response in unity gain of the three amplifiers: (a) standard; (b) gain-boosted; and (c) body-driven gain-boosted cascoded.

An implementation example was given and simulations showing the viability of the proposed approach were also provided. The main drawback, when compared with the standard cascode architecture, is the reduction of about 30% in the unity-gain frequency and noise increase.

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