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A CLOSED LOOP POWER MANAGER FOR TRANSMISSION POWER CONTROL IN WIRELESS NETWORK-ON-CHIP ARCHITECTURES

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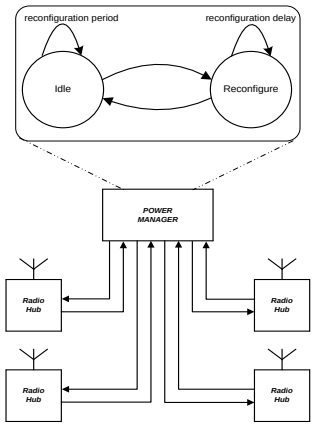
Graphical abstract



Abstract

In wireless Network-on-Chip (WiNoC), radio frequency (RF) transceivers account for a significant power consumption, particularly its transmitter, out of its total communication energy. Current WiNoC architectures employ constant maximum transmitting power for communicating radio hubs regardless of physical location of the receiver radio hubs. This paper proposes a closed loop transmitting power control mechanism that, using bit error rate (BER) report obtained at receiver's side, dynamically calibrates the transmitting power level needed for communication between the source and destination radio hubs to guarantee transmission reliability. Our proposed strategy achieves a significant total system energy reduction by about 40% with an average performance degradation of 3%.

Keywords: WiNoC, BER, RF transceiver, closed loop transmitting power control, dynamic power calibration

Abstrak

Dalam rangkaian-atas-cip tanpa wayar (WiNoC), sistem penghantar-terima radio frekuensi (RF) terutamanya pada bahagian pemancar, menggunakan sebahagian besar daripada jumlah keseluruhan tenaga. Senibina WiNoC terkini menggunakan kuasa pemancaran maksimum yang sama untuk komunikasi hab radio tanpa mengambil kira lokasi fizikal hab radio penerima. Kertas kajian ini mencadangkan satu mekanisma kawalan kuasa penghantaran gelung tertutup yang menggunakan maklumat kadar ralat bit (BER) yang diperolehi pada penerima, untuk menentukur tahap kuasa pemancaran yang diperlukan. Tahap kuasa pemancaran ini digunakan untuk komunikasi antara hab radio pemancar dan hab radio penerima bagi menjamin kebolehpercayaan sistem. Strategi yang kami cadangkan mampu mencapai pengurangan jumlah tenaga sistem sebanyak sekitar 40% dengan penurunan prestasi pada purata 3%.

Kata kunci: WiNoC, BER, sistem komunikasi radio frekuensi (RF), kawalan penghantaran kuasa gelung tertutup, penentukuran dinamik kuasa

1.0 INTRODUCTION

As the number of possible cores integrated in a chip increases, the role played by the on-chip communication system becomes more and more important. The Network-on-Chip (NoC) has been considered as one of the best candidates to replace bus-interconnects system. It integrates large number of cores on a single die. However, as the number of cores in the network size increases, the multi-hop communication nature of NoC-based systems results in increased communication latency. Even with improved integration density and device speed, the electrical interconnects become the bottleneck in terms of delay and power-consumption [5]. To mitigate this problem, a few emerging NoC derivatives have been introduced such as 3D-NoC, nanophotonic communication and RF-based interconnect or also known as wireless network-on-chip (WiNoC). RF interconnects replace metal wires in traditional wire-based NoC. On-chip RF modules such as antenna and transceivers also increase area and power overhead. As far as power issue of WiNoC is concerned, the major contribution of WiNoC power consumption is due to the radio transmitter front-end connected to the antenna. For instance, it has been shown that the transmitter is responsible for about 65% and 74% of the overall transceiver power consumption in two WiNOC architectures in [1] and [9] respectively.

Previous works in the context of WiNoCs are based on fixed transmitting power regardless of the physical location of destination nodes that is able to guarantee a certain reliability level (in terms of bit error rate, BER) in the worst case scenario. Mineo *et al.* [6] proposed a configurable transmitter with transmission power based on physical location of the receiver. It has been shown that such transmitters allow significant power saving with a negligible impact in terms of area and delay. On the other hand, it has to be configured offline by means of an extensive characterization phase which requires either time consuming field solver simulations or direct measurement of real context. This offline configuration presents several drawbacks as follows.

1) Determining radiating fields in CMOS substrates requires robust and accurate field solvers, and many commercial field solvers have not been rigorously tested or verified in on-chip integration level [4].
2) Metal structures near the antenna can affect the magnitude of received signal and several design guidelines have been proposed in order to alleviate this phenomenon [8].

Thus, in order to design a robust communication infrastructure, the analysis should take into account interference such as process variability which characterizes ultra-deep sub-micron technology nodes.

In this paper, we propose a novel mechanism for reducing the energy consumption of transmitters in WiNoC architectures. Different from the previous work in [6], the proposed technique does not require offline characterization but it uses an online closed-loop control mechanism which operates as follows. Each receiver periodically informs the controller about the rate of bit error detected in packets received from transmitters. Based on this information, the controller reconfigures transmitting power by increasing or decreasing it. Overall, given a certain reliability requirement expressed by means of a maximum allowable BER (a reference BER), the proposed controller allows dynamic tuning of transmitting power for each transmitter and receiver communicating pair to meet the reliability requirement with minimum energy consumption.

2.0 RELATED WORKS

The communication latency among the cores becomes the bottleneck in NoC-based system due to multi-hop nature of the system. Several wireless NoC architectures that propose introduction of radio frequency (RF) transceivers as a communication medium have been introduced [12], [13]. This is motivated by already recognized antenna designs that operate in high frequency at deep submicron level [2], [4]. Some guidelines on designing RF modules that operate in sub-terahertz frequencies have been discussed [5]. Hybrid architecture of electrical link and wireless link NoC has been introduced [3]. Cluster-based WiNoC architectures connect each RF module to a group of neighboring processing cores [3], [7]. A proposed architecture applies small world property that integrates traditional NoC topologies communicating with different topologies via radio hubs considering long range communication [9].

In selecting a signal modulation scheme, WiNoC often selects a noncoherent on-off keying (OOK) based transceiver. In our design, a specific amplitude shift keying (ASK-OOK) modulation technique is chosen due to its simple implementation and low-power consumption features.

Traditional transmitters in WiNoC use fixed transmitting power regardless of the physical location of the receiver. Maximum transmission power is utilized to meet the reliability requirement of maximum bit error rate constraint. Mineo *et al.* [6] proposed a reconfigurable transmitter that selects transmitting power based on the physical location of the receiver. The design drives power amplifier (PA) to configure real output power based on power level provided by variable gain amplifier (VGA) module at runtime.

Dynamic power tuning has been an established technique in the context of radio communication such as mobile phones and wireless sensor network. In wireless sensor network, dynamic communication power management strategies are aimed at reducing transceivers power consumption and/or nodes sensing. These strategies include sleep-mode module, low-power management and battery management at sensing nodes. Examples of wake-up receiver power management scheme in wireless sensor network have been implemented by Lin *et al.* [17] and Lu *et al*. [18].

Dynamic power tuning in WSN is different with NoC due to its much larger propagation time and transmission time. In NoC, certain strategies such as sleep-mode and battery management at sensing nodes cannot be applied.

In the context of WiNoC, dynamic power management requires specific controller and implementation policy in semiconductor ambience. The main problem of this scheme is that such optimal transmitting power must be characterized offline by using time-consuming field solver simulator. For this reason, this paper presents a power manager that applies a closed-loop control mechanism which dynamically reconfigures the transmitting power based on several input parameters. We implemented our design on two WiNoC architectures; McWiNoC [7] and iWise [3]. These architectures adopt cluster-based WiNoC architectures.

3.0 RESULTS AND DISCUSSION

In this section, we introduce the basic theory on how to compute the required transmitting power in order to guarantee a certain BER. Firstly, the Friis transmission equation [11] is introduced to compute the fraction of transmitting power that reaches the receiving antenna. Consequently, the required transmitting power that determines a given BER for the OOK modulation scheme is derived.

3.1 Friis Transmission Equation

The required transmitting power depends on many factors such as the type of modulation, transceiver noise figure and attenuation introduced by wireless medium. Let us consider a transmitting power P_t and a relative angle of (θ_t, ϕ_t) with respect to the receiving antenna, and a receiving antenna located at distance R, and P_r represents the power received at the terminal of the of the receiver antenna. The attenuation gain G_a that reaches the terminal of P_r, can be computed with the Friis transmission equation using scattering parameters S_{11}, S_{12} and S_{22} as:

$$G_a = \frac{P_r}{P_t} = \frac{|S_{12}|}{(1-|S_{11}|)(1-|S_{22}|)} \quad (1)$$

In practical cases, the scattering parameters should be evaluated by using field solver simulation tools [15] or by direct measurement from realized prototypes.

3.2 Signal Strength Requirements

Eqn. (1) estimates the signal attenuation due to the wireless medium. Since the reliability of the ASK-OOK modulation is related to the energy per bit, E_b, spent to reach the receiver's antenna, we can determine the power required by the transmitter for each value of the attenuation G_a.

$$BER = Q\left(\sqrt{\frac{E_b}{N_0}}\right) \quad (2)$$

where N_0 is the transceiver noise spectral density and the Q function is the tail probability of the standard normal distribution. Since $E_b = P_r/R_b$, where R_b is the data rate, we can compute the required transmitting power for a given data rate and BER requirement for a given transceiver's thermal noise as:

$$P_r = E_b.R_b = [Q^{-1}(BER)]^2 N_0 R_b \quad (3)$$

where Q^{-1} is the inverse of the Q function. Based on the above considerations, the minimum transmitting power to reach a certain receiver guaranteeing a maximum BER can be computed as:

$$P_t(dB) = P_r(dB) - G_a(dB) \quad (4)$$

where P_r(dB) is given by Eqn. (3) while G_a(dB) is computed by using a field solver with the Friis formula when power is expressed in dB and converted to dBm.

3.3 Efficient Transmission

An effective energy transmission of an antenna is measured by voltage standing wave ratio (VSWR) based on G_a, known as return loss. The quality of transmission defined by VSWR at each antenna transceiver considering G_a is given by:

$$VSWR = \frac{1+|\Gamma|}{1-|\Gamma|} \quad (5)$$

where Γ is a reflection coefficient, also known as return loss. A high value of VSWR is associated with low return loss parameter. It shows that a high percentage of power is radiated or received at the front-end transceiver while small percentage is reflected because of impedance mismatch and vice versa.

4.0 CLOSED LOOP TRANSMITTER POWER CONTROL

In realizing the proposed power management control, we consider the implementation on homogeneous multicore system with application specific integrated circuit design. The importance of power reconfiguration in generic NoC system, particularly WiNoC platform as opposed to fixed distance NoC is discussed as follow.

Firstly, computation and communication loads vary over time depending on extrinsic factors such as power saving mode specification and online data streaming that require extra run-time computation and communication efforts. Furthermore, power consumption overhead centered on circuit area leads to high energy density and thermal hotspot formation. Secondly, intrinsic factors also affect computational and communication loads such as application specific algorithm. Various packet error rates at receiver terminal in WiNoC platform is not trivial to overcome for on-chip wireless communication.

Thus far, there is no known WiNoC prototype has yet been fabricated and marketed, thus researchers have limited knowledge on noise signal for short and medium range on-chip RF transmission. Significant signal-to-noise ratio effect may be observed when high transmission power is applied for communicating radio hubs. But there are other considerations for depreciating signal integrity in WiNoC communication such as multipath fading, inter-channel interference require practical observation on real platform.

For all the above mentioned reasons, we believe dynamic power reconfiguration on fixed location NoC offers improvement in energy consumption while satisfying system throughput constraint as opposed to one-off power reconfiguration scheme. In this section, we present a scheme that eliminates attenuation gain characterization for the estimation of scattering parameters between two radio hubs. The scheme applies a closed loop self-calibrating mechanism at runtime for transmitted power at each transmitter based on packet granularity.

4.1 Architecture

The main idea in the proposed architecture is to introduce power reconfigurability to the transceiver based on bit error rate information. It has been proven that source and destination transceivers power profiles are characterized by different attenuation gain, G_a. Equipped with good error detection module at the receiver module, the architecture is assumed to be able to provide accurate statistical bit error information to the power management scheme.

The core architecture of the centralized self-calibration approach is the variable gain amplifier controller (VGA controller). The VGA controller features a dynamic reconfigurable lookup table that stores code word representing one of the power steps for communication between source and destination radio hub. The power step is a 3-bit word-code associated with 7 steps that drives the power amplifier (PA) for actual transmission power. Based on the packet header destination, the <*source*,*destination*> table entry drives power amplifier to the associated power level. Our centralized scheme introduces a power configurable module based on BER notification generated at destination radio hub. Another core architecture that we propose is the power manager module that collects BER information from each radio hub during RS that adapts the power requirement of both source and destination radio hubs that guarantee reliability and finally distributes the decision for self-calibration transmission power at radio hub level.

4.2 Adaptive Mechanism and Power Manager

Figure 1 shows the finite state machine implementing the power manager. Centralized power manager adopts two modes of operation. In Reconfiguration Period (RP), WiNoC platform collects BER statistics of packets at receivers. The power manager is idle during this period. As soon as reconfigurable counter at each receiver notifies the end of RP, WiNoC platform is stalled. It enters Reconfiguration State (RS). During this stage, BER information collected during RP is transmitted to the manager for power reconfiguration. The statistical bit error rate of each radio hub is compared with reference BER. Based on power management strategy, the look up table in VGA controller of each radio hub is updated with new code word that represents the power step.

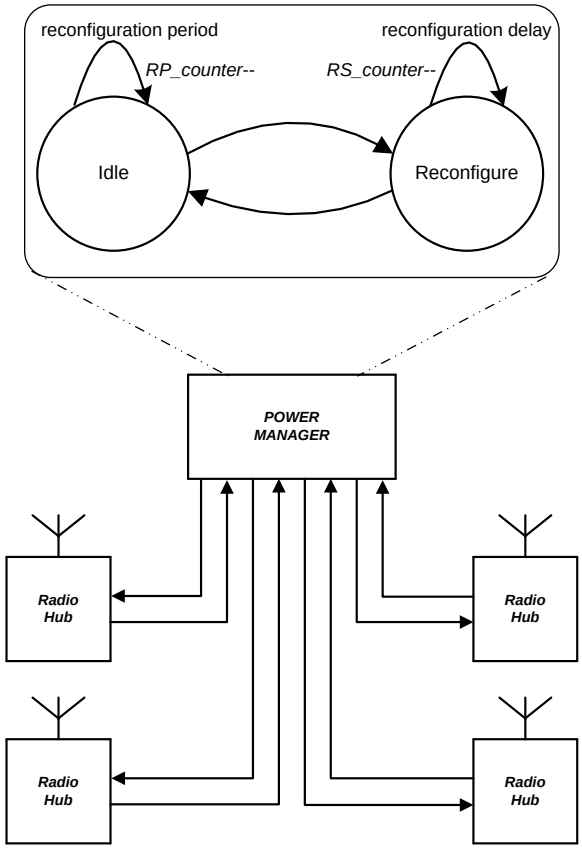


Figure 1 Possible centralized architecture for 2 by 2 WiNoC radio hubs

The management strategy can be formalized as in Algorithm 1. The algorithm can be described as follows. A source radio hub, *i* transmits packets with initial maximum power step to a destination radio hub, *j*. Radio hub *j* counts the number of packets it receives from transmitter *i* using module *PC[T]*, determined by a predefined RP. *PC[T]* is decremented each time *j* receives a packet from *i*.

For any specific RP, we assume there is a unique error detection module attached to each radio hub, providing accurate packet error information. Signal *ber_estimated(i,j)* determines estimated BER after a complete execution of *PC[T]*. When RP ends and no error is reported at radio hub *i*, signal *ber_estimated(i,j)* is not asserted. The universal adaptive power manager assumes the transmitted power of the pair <*i,j*> is oversupplied. Hence, the word code for *i*-th entry is

decremented in the lookup table. WiNoC operation is stalled during RP, allowing power manager to reconfigure the table.

As soon as the platform enters period RS, each radio hub concurrently notifies universal power manager of current estimated BER. The universal power manager obtains estimated BER value input from radio hub *i* during communication with radio hub *j*. It then compares the BER value with desired BER value, *reference_ber*. The *reference_ber* value is predetermined before RP commences to guarantee reliability. If the signal *estimated_ber(i,j)* is greater than the user defined *reference_ber*, then power manager increments the transmitting power needed for reliable communication between the pair. The same mechanism applies if *estimated_ber(i,j)* is less than *reference_ber* in which the transmitting power is decremented.

Figure 2 shows the block diagram of two communicating radio hubs on WiNoC platform. The receiver terminal maintains the statistical error report of packets received during period RP using error control module. As RP ends, the error control module of the receiver terminal notifies the power manager input ports with signal CONTROL_OUT that is a 3-tuple field ($addr_{rx}$, $addr_{tx}$, *estimated_ber*), where $addr_{rx}$ is the receiver radio hub address that reports the error, $addr_{tx}$ is the address of the transmitting radio hub that produces packet error rate and *estimated_ber* is the estimated bit error rate detected by the receiver.

During RS, the power manager receives the statistical error reports concurrently from all reporting radio hubs. The module compares the *estimated_ber* value of respective radio hub with the predefined *reference_ber*. The output signal CONTROL_IN from power manager is exclusively fed into each transmitting radio hub that needs to be regulated, $addr_{tx}$ to update its transmitting power step in VGA controller lookup table via signal command *cmd*. The operation is a 3-bit code-word protocol indicating one of the conditions for optimal transmitting power: increase, decrease or no change. Detail explanation of VGA controller operation is discussed in the following subsection. As RP period commences again, the VGA controller drives the power amplifier for actual wireless transmission power [1], [3]. The amplifier module is an established technique that translates bit representation power steps into actual voltage level on WiNoC radio hub.

4.3 Variable Gain Controller

The VGA controller consists of a dynamic lookup table that regulates transmitting power from source *i* to destination *j* as shown in Figure 2. During the period RS, if *UPDATE* is high, input *DST ADDR* updates *j*-th table entry of code word (power level) that tunes the transmitting power level in order to meet the network BER requirement. If *UPDOWN* is high, the power level pointed by *DST ADDR* is increased and vice versa. During period RP (*UPDATE* is low), the output power level pointed by *DST ADDR* is used to drive PA to actual transmission power.

4.4 Access Control Mechanism

This mechanism regulates communication control granted by destination *j* to notify source *i* in modifying transmitting power steps to the desired level.

The adaptive manager relays the control decision to radio hub *i* to increase, decrease or retain its transmission power level. The point to multipoint control occurs in less than 10 clock cycles. The strategy transmits command via a 3-tuple packet protocol. Packet *CONTROL OUT* contains address of current radio hub, $addr_{rx}$, address of transmitting radio hub that needs to be regulated, $addr_{tx}$, and estimated BER, *estimated_ber(i,j)*. The received packet, *CONTROL IN* consists of address of transmitting radio hub that needs to be regulated, $addr_{tx}$, and command of control operation (increase or decrease), *cmd*.

5.0 EXPERIMENTS, RESULTS AND DISCUSSION

5.1 Experimental Setup

We implement the proposed technique in an extended version of Noxim [10] supporting wireless communications. It has been applied on two well-known WiNoC architectures: McWiNoC [7] and iWise [3]. We apply VGA controller with 8 power steps and vary the number of radio hubs to prove scalability of the proposed design. We implement a 4 radio hub network size and followed by 8 radio hubs. Hence, the number of look-up table entries in VGA controller changes proportionally with the network size. The proposed design has been modeled in VHDL and synthesized using Synopsys Design Compiler and mapped on 28 nm CMOS standard cell-library from TSMC operating at 1 GHz. The area overhead of our module on WiNoC platform is obtained using the compiler tool, whereas Synopsys Power Compiler generates the power consumption of the proposed power manager. Both analyses are shown in Table 1.

We compare the level of energy saving and performance improvement by applying the design on McWiNoC and iWise architectures. Benchmarking has been done with SPLASH-2 application files.

We consider the proposed transceiver utilizes seven adjustable output power steps in the VGA controller as proposed by Daly *et al.* [1] and DiTomaso *et al.* [3]. The transmitting power steps are ranged equally between 8 µW (-21 dBm) and 794 µW (-1 dBm). When expressed in terms of energy per bit, each power step corresponds to 0.42 pJ/bit and 1.4 pJ/bit. The attenuation map has been obtained from the Ansoft HFSS (High Frequency Structural Simulator) [16] modeled with zigzag antenna. The energy saving analysis has been carried out using RP represented in unit packet(s), considering a packet is transmitted

when each RP cycle executes. The latency analysis stated in the following experiments defines the number of extra cycles needed when executing our proposed scheme as opposed to the baseline iWise and McWiNoC architectures without the power manager implementation.

5.2 Experimental Results

Referring to Figure 2 and Table 1, the proposed VGA controller, that is the only overhead in our proposed design as compared to an extant work [14], accounts for less than 0.1% both in terms of area and power. We do not take into account power manager contribution in power consumption since the module operates during reconfiguration phase (when all system operations are stalled). Power manager occupies a small fraction of time to operate during RS period as compared to time taken by WiNoC platform during period RP, when the power manager is idle.

In terms of energy saving and latency, our experimental results are compared with the baseline architectures of McWiNoC and iWise64 that utilize constant power for communication with all radio hubs on their platforms.

As the reconfiguration period increases, the energy saving of WiNoC platform decreases. This is due to the communication response between power manager and the radio hubs. This fact is supported by the experimental results conducted on McWinoC-16 architecture which consists of 4 radio hubs (Figure 3). More than 50% total energy consumption is observed for RP 1000 due to high response activity among the radio hubs and power manager. However, the energy saving is consistent from RP 2000 until RP 4000 at about 40%.

Similar trend is observed when we implemented the design on McWiNoC-64 and iWise-64 architectures with 8 radio hubs each (Figure 4). It can be observed, on average, the implementation of the proposed design on McWiNoC results in more than 40% energy saving. On the other hand, around 5% energy saving reduction is observed for iWise-64 between RP 1000 and RP 4000. Even though the number of radio hubs in iWise and McWiNoC is identical, the frequency of intra cluster radio hub communication for iWise is four times more than the frequency of inter cluster communication for McWiNoC due to the nature of iWise architectural design. Hence, an effective and responsive power management becomes less efficient as RP value increases.

As soon as the platform enters reconfiguration phase, network operation is stalled, causing performance degradation. Figure 5 shows the effect of varying reconfiguration period on communication latency. As shown in the figure, the latency is inversely proportional to RP. A high RP value results in higher energy saving with a tradeoff of performance degradation and vice versa. However, overall, both architectures do not suffer more than 3% performance degradation.

The above analysis has been carried out considering a reconfiguration time of 10 clock cycles. We take for an example, the measurement of energy saving and latency when we set RP value to 2000 on iWise architecture, verified with SPLASH-2 benchmark (Figure 6 and Figure 7).

Algorithm 1 Proposed closed loop transmitting power control mechanism

Input: *i*, *ber_estimated(i,j)*, *reference_ber*

```
1:  if PC[i] = 0 then
2:      if ber_estimated(i,j) > reference_ber then
3:          SendCmdPLInc(i.j)
4:          PC[i] ← RP_counter
5:      else
6:          SendCmdPLDec(i,j)
7:          PC[i] ← RP_counter
8:      end if
9:  else
10:     PC[i] ← PC[i] – 1
11: end if
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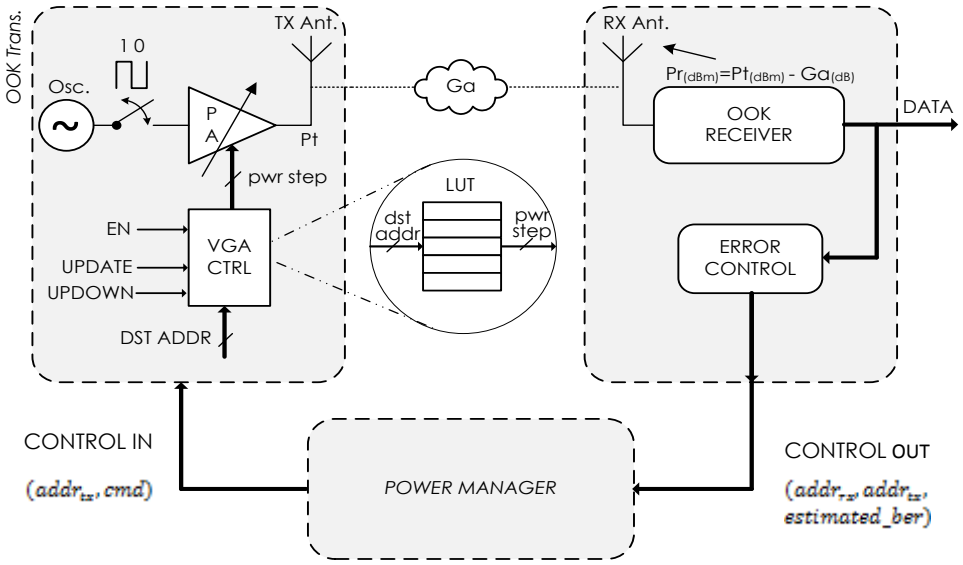

Figure 2 Block diagram of the architecture implementing the proposed WiNoC scheme

Table 1 Area and power overheads of the proposed design [14]

	Area / %	Power / %
Transceivers	80.1	90.7
Router	19.8	9.2
VGA Ctrl	0.1	0.1

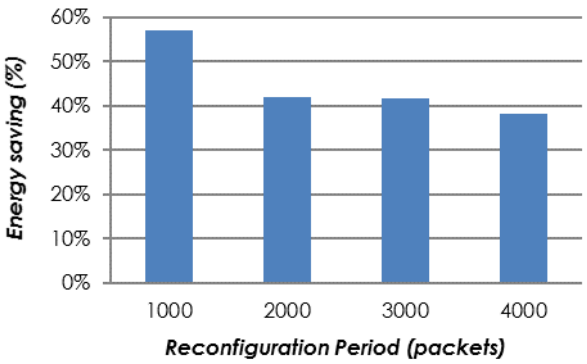

Figure 3 Energy saving for different reconfiguration period on McWiNoC-16

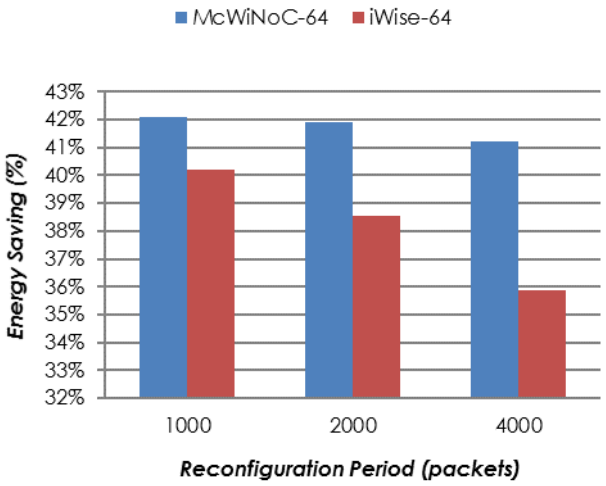

Figure 4 Energy saving for different reconfiguration period on two WiNoC architectures, namely McWiNoC-64 and iWise64, implementing 16 radio hubs with 64 cores with SPLASH-2 benchmark

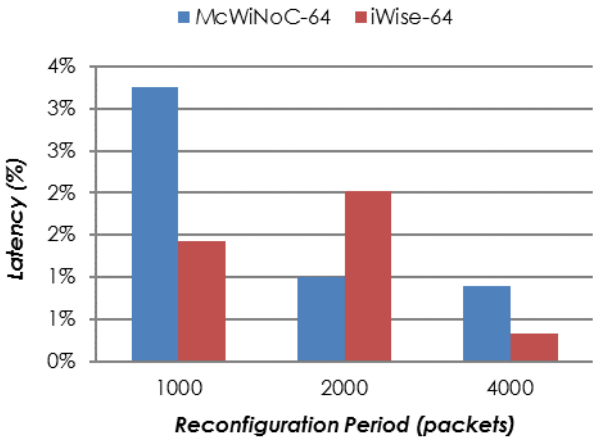

Figure 5 Percentage delay for different reconfiguration period on McWiNoC-64 and iWise-64 with SPLASH-2 benchmark

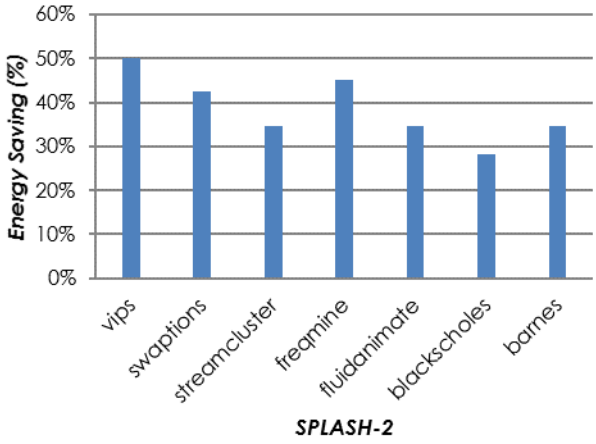

Figure 6 Detailed energy saving impact on iWise-64 architecture with SPLASH-2 benchmark applying reconfiguration period of 2000

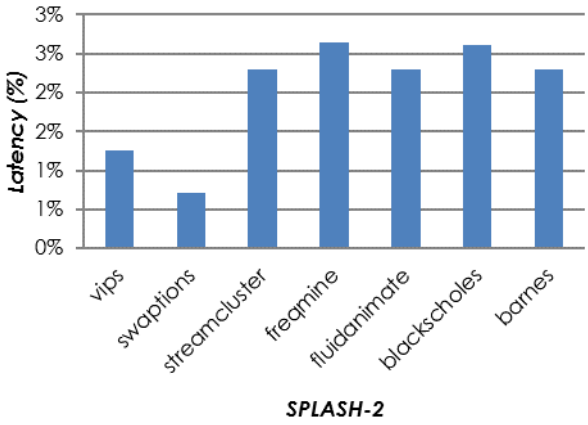

Figure 7 Detailed communication latency impact on iWise-64 architecture with SPLASH-2 benchmark applying reconfiguration period of 2000

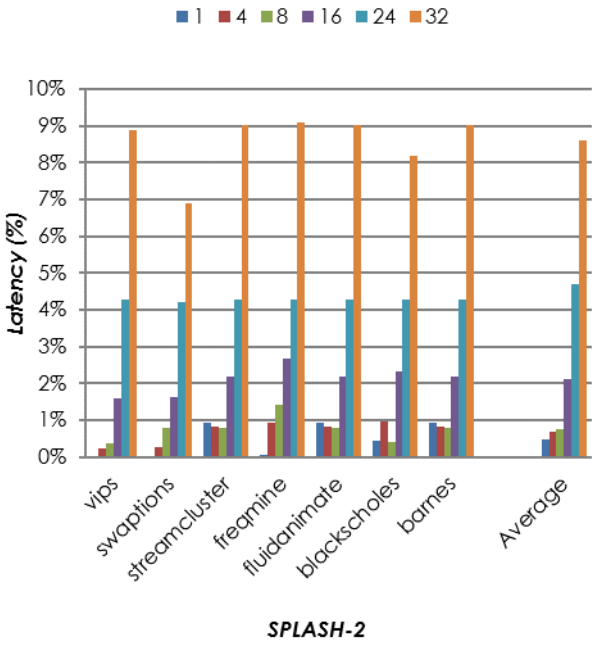

Figure 8 Percentage latency impact on iWise-64 architecture with SPLASH-2 benchmark for different reconfiguration stage (penalty) applying reconfiguration period of 2000

Based on these figures, low RP values increase system's responsiveness towards power management strategy. The more persistent power management strategy is employed, the more frequent bit error rate is detected, causing higher probability and frequency of changing transmitting power step. Communication latency is maintained at average level of 3% due to packet retransmission scheme.

Varying the period for reconfiguration phase affects system performance. Figure 8 shows the performance effect on iWise architecture when the RS value is varied. As the reconfiguration phase is greater than 16 clock cycles, system latency increases about double the previous latency value. Communication latency varies from about 4% to more than 8% when reconfiguration phase is manipulated to 24 and 32 clock cycles, respectively. The iWise architecture works well under 3% performance degradation for the reconfiguration phase of 16 clock cycles and below.

The latency maintains at 2% for RS value of 16 cycles and below. This means that to achieve optimized delay metric below the percentage, a power manager is assigned to a maximum of 16 radio hubs, considering 1 RS cycle represents a transmitting power management command to a radio hub. However, as RS increases from 24 to 32 cycles, the platform becomes less efficient due to increased power management burden that can be handled by the manager. Similar trend applies to McWiNoC architecture in which the communication latency rises sharply as reconfiguration stage goes beyond 16 clock cycle threshold [14].

6.0 CONCLUSION

We have proposed a closed-loop control power manager for reducing the energy consumption in WiNoC architectures by about 40%. Based on the observation that the minimum transmitting power to guarantee a certain BER strongly depends on the physical location of the transceivers, we have proposed a mechanism for on-line reconfiguration of transceivers using minimum transmitting power suitable for a certain transmitter-receiver pair communication. The proposed power manager dynamically regulates transmitting power of a source radio hub to a destination radio hub. The proposed technique can be generally applied to any WiNoC architecture. Specifically for this paper, our design has been applied on two WiNoC architectures, namely McWiNoC and iWise. In assessing the energy saving and performance, we verified our design with SPLASH-2 benchmark files. Based on our experimental results, it has been shown that the technique is effective in achieving total communication energy saving (about 40%) with considerably low performance degradation (about 3%). It has been also shown that our proposed design utilizes a small fraction of both area and power overheads (about 0.1%) out of total transceiver properties.

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