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Research Article

Design of a Traffic-Aware Governor for Green Routers

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Today the reduction of energy consumption in telecommunications networks is one of the main goals to be pursued by manufacturers and researchers. In this context, the paper focuses on routers that achieve energy saving by applying the frequency scaling approach. The target is to propose an analytical model to support designers in choosing the main configuration parameters of the Router Governor in order to meet Quality of Service (QoS) requirements while maximizing energy saving gain. More specifically, the model is used to evaluate the input traffic impacts on the choice of the active router clock frequencies and on the overall green router performance. A case study based on the open NetFPGA reference router is considered to show how the proposed model can be easily applied to a real case scenario.

1. Introduction

In the last decade, new requirements are appearing in telecommunications network design and management deriving from the fact that the global Internet, with its energy consumption of about 8% of the global production, is becoming one of the most important energy consumers in the world [1]. Today's most telecommunications networks are provisioned for worst-case or busy-hour load, and this load typically exceeds their long-term utilization by a wide margin; moreover, as shown in [2], current network nodes have a power consumption that is practically constant and does not depend on the actual traffic load they face. The implication of these factors is that most of the energy consumed in networks today is wasted [3]. A nonmarginal side effect of high-energy dissipation is the increment of the temperature of the places where network devices reside, with a consequent further waste of energy used by cooling machines to maintain the temperature of the local environment constant.

For this reason, addressing energy efficiency in the Internet is receiving considerable attention in the literature today [4–10] and many research projects are working on this topic (see, e.g., [11–13]). The novel approach for networking means that, besides typical performance parameters as, for example, throughput, latency, and packet loss probability, amount of consumed energy starts to be one of the most important factors of network design and operation.

For the above reasons, some novel hardware devices, the so-called "green routers", are expected in the near future to allow different power states [14] according to the input traffic. A lot of work was done in the past, focusing on the definition of power management techniques, like, for example, the static techniques described in [6–8], and the adaptive policy proposed in [9]. Two approaches have been proposed to reduce energy consumption in network components [5]. The first is based on putting network components in sleeping state during idle intervals, reducing energy consumed in the absence of traffic. The second one is based on adapting the rate of network operations to the offered workload. Rate adaptation in particular is usually achieved by scaling the processing power according to the data rate the router has to manage; at this purpose, the clock frequency driving the router processes can be modified according to the input data rate [10]. The energy aware techniques to be used in a green router depends on a number of factors, including the role of the router in the network, the profile of incoming traffic, and the hardware complexity. Other aspects that have to be considered are the related costs with respect to the energy we can potentially save, and the Quality of Service (QoS) we want to guarantee to the users [15]. The user notices also that different techniques and architectures have been proposed in the literature in order to provide frequency scaling capabilities to networking devices, like, for example, [16, 17].

With all this in mind, the paper focuses on routers that achieve energy saving by applying the frequency scaling approach [17]. The target is to extend the proposed model of a green router introduced by the same authors in [18, 19] to support designers in choosing system parameters in order to meet QoS requirements while maximizing energy saving gain. The paper starts from the observation that each modification of the operating clock frequency causes some QoS degradation in terms of packet loss, delay, or energy waste, according to the particular implementation of the router. For this reason, the best tradeoff between energy saving and QoS performance could be achieved by using a set of clock frequencies that is a timely chosen subset of all the clock frequencies supported by the router CPU. However, the choice of the particular subset, that is, both the number of frequencies and which frequencies among all the available ones, is strongly related to the input traffic, and specifically its mean value, its variance, and its autocorrelation. For example, it is not befitting to use clock frequencies that manage bit rate values close to the mean value of the input traffic bit rate. Moreover, it is better to avoid frequencies that are very close to each other if the traffic is low correlated. With the aim of choosing the set of frequencies and deciding the best clock frequency at runtime, a Router Governor is introduced. An additional parameter, in the following referred to as δ, is introduced to control the frequency change rate, with the aim of matching the given QoS requirements. Starting from the Router Governor architecture defined in [18, 19], defined to support only two clock frequencies, a general Router Governor is proposed to work in routers with any number of clock frequencies. A new multidimensional discrete-time Markov model is presented to capture the behavior of the proposed Governor. Since, as mentioned so far, each frequency switch is characterized by a given cost, the model is used to evaluate how the input traffic impacts the choice of the active clock frequencies and on the overall green router performance. A case study based on the open NetFPGA Open Router [20] is considered to show how the proposed model can be easily applied to a real case scenario. More specifically, the paper uses the green NetFPGA Reference Router proposed by the same authors in [18, 19] that leverages on the facility of the NetFPGA platform to reduce the clock rate by changing the value of an ad-hoc hardware register. Loss probability and energy saving gain are considered as QoS metrics.

The paper is structured as follows. Section 2 introduces the reference router architecture and the proposed policy. Section 3 describes the Markov model of the considered system. Section 4 derives of the main performance parameters. All the results of our analysis are shown in Section 5, which describes the proposed case study. Finally, Section 6 ends the paper with authors' conclusions and future directions.

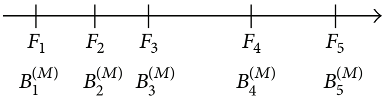


Figure 1: Set of clock frequencies implemented by the router, and relative maximum supported bitrates.

2. A Traffic-Aware Governor for Green Routers

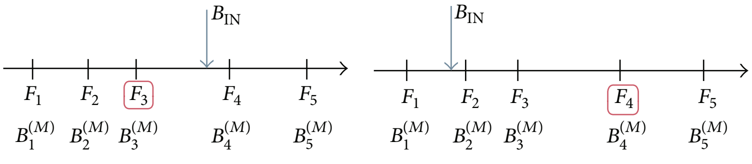
In this section we describe the system which is the focus of this paper. It is a Governor for green routers that implement frequency scaling [19] to save energy when the input traffic load is low. Frequency scaling, a capability available in many routers today, is the possibility of changing the core clock frequency in a set of values to dynamically scale the energy consumption of the device. The base problem of this approach is that if on the one hand the device power consumption is reduced using lower clock frequencies with respect to the highest one, on the other hand such a decision can deteriorate the router performance. For example, in the green implementation of the NetFPGA Reference Router [18], clock frequency switches cause a temporary block of the router, and therefore all the incoming packets during these intervals are lost. Other routers, although with different hardware architecture and implementation, behave at the same way: at each clock frequency variation they present a QoS degradation, in terms of either loss probability, delay, and/or energy consumption peaks.

Starting from the above considerations, the approach proposed in this paper, which aims at finding the best tradeoff between energy efficiency and QoS, is very general since it can be used to limit such a router QoS degradation by only changing the particular target QoS parameter (e.g., loss probability, mean delay, or energy consumption during the switching periods).

In order to manage frequency switches maintaining QoS acceptable while decreasing energy consumption, we introduce a Router Governor, that is, an entity which implements a router management policy to change the clock frequency of the router CPU. In the following, QoS is defined by the following parameters: packet loss, mean delay, and energy waste during frequency switching intervals.

Let us note that other traditional QoS parameters characterizing the router, like, for example, packet loss probability for output queue overflow and queuing delay, are not considered here because they are not altered by the presence of our Router Governor.

Let $\overline{\Phi}$ be the set of clock frequencies supported by the router CPU, and let F_i be the generic ith CPU clock frequency. For the sake of simplicity, we sort frequencies in such a way that $F_i < F_{i+1}$. Let us indicate the maximum bit rate that can be supported with no loss when the CPU is working at the frequency F_i as $B_i^{(M)}$. These values are sketched in Figure 1.



(a) Example for Rule 1

(b) Example for Rule 2

Figure 2: Set of clock frequency implemented by the router, and relative maximum supported bitrates.

An important observation that is at the basis of our approach is that the greater the cardinality of $\overline{\Phi}$, that is, the greater the number of available frequencies, the higher the ability to follow the input traffic behavior with the most appropriate clock frequency, and consequently the higher the energy saving gain. However, a high number of clock frequencies could cause too frequent switches and therefore QoS degradation. For this reason, the best tradeoff between energy saving and QoS performance can be achieved by using an appropriate set Φ of clock frequencies that is a subset of $\overline{\Phi}$. In addition, we have to take into account that the choice of the particular subset Φ has to depend on the input traffic, that is, its mean value, its variance, and its autocorrelation. In fact, if the input bit rate, due to its first- and second-order statistics, too frequently crosses the value $B_i^{(M)}$ associated with the clock frequency F_i, this clock frequency should not be used.

Once the set of active frequencies Φ is decided, the Router Governor has to work controlling that the QoS requirements are respected. To achieve this goal, indicating the generic ith clock frequency in the set Φ as F_i, we define the Router Governor policy as follows.

Rule 1. If the clock frequency was previously set to F_i (see Figure 2(a), where $i = 3$) and the current input bit rate B_{IN} is greater than $B_i^{(M)}$ ($B_3^{(M)}$ in Figure 2(a)), then the clock frequency is switched to the minimum clock frequency belonging to Φ that does not cause losses (F_4 in Figure 2(a)).

Rule 2. If the clock frequency was previously set to F_i (see Figure 2(b) where $i = 4$) and the current input bit rate B_{IN} is lower than $B_{i-1}^{(M)}$ (e.g., lower than $B_3^{(M)}$ in Figure 2(b)), then it can be switched down to a value F_k less than F_i, but not less than the minimum clock frequency belonging to Φ that does not cause losses (i.e., F_2 in Figure 2(b)). However, since a frequency switch causes a QoS degradation, this is done with a probability $p_G(B_{\mathrm{IN}}, i, k)$ which is adaptive to the current input bit rate B_{IN}: the greater the distance between B_{IN} and the maximum bit rate that can be supported by the new clock frequency, the lower the risk of a new frequency switch. To this purpose, referring to the example illustrated in Figure 2(b), the switching probability is defined as follows:

(i) the new clock frequency is set to F_2 with a probability:

$$p_G(B_{\mathrm{IN}}, 4, 2) = \delta \frac{B_2^{(M)} - B_{\mathrm{IN}}}{B_4^{(M)} - B_{\mathrm{IN}}}, \tag{1}$$

(ii) if the result of the previous draw was negative, and so the clock frequency was not set to F_2, the new clock frequency is set to F_3 with a probability:

$$p_G(B_{\mathrm{IN}}, 4, 3) = \delta \frac{B_3^{(M)} - B_{\mathrm{IN}}}{B_4^{(M)} - B_{\mathrm{IN}}}, \tag{2}$$

(iii) if the previous draw is negative again, that is, the clock frequency is not set to F_3, the clock frequency remains F_4.

Generally speaking, if the current clock frequency is F_i and the input bit rate B_{IN} is lower than $B_{i-1}^{(M)}$, the clock frequency can be changed in the set $\{F_j, \dots, F_i\}$, where F_j is the minimum clock frequency of Φ not causing loss. More specifically, the clock frequency is set to F_k, with $k \in [j, i]$, with a probability:

$$p_G(B_{\mathrm{IN}}, i, k) = \left[\prod_{h=j}^{k-1} \left(1 - \delta \frac{B_h^{(M)} - B_{\mathrm{IN}}}{B_i^{(M)} - B_{\mathrm{IN}}}\right)\right] \cdot \begin{cases} \delta \dfrac{B_k^{(M)} - B_{\mathrm{IN}}}{B_i^{(M)} - B_{\mathrm{IN}}} & \text{if } k < i \\ 1 & \text{if } k = i. \end{cases} \tag{3}$$

The term $\delta \in [0, 1]$ allows the designer to make clock frequency switches more or less rare. It is easy to argue that its value plays a very important role in the router performance. The design of the clock frequency subset Φ and the parameter δ will be assisted by the analytical model that will be described in Section 3. In order to follow variations of traffic statistics in a long-term time scale, they can be modified runtime according to continuous measurements done by the Router Governor.

3. Markov Model

In this section we define a discrete-time model of the system described so far in order to capture the behavior of the clock frequency process. Since it depends on the input traffic bit rate according to the Router Governor policy, we define the Markov model state as $S^{(\Sigma)}(n) = (S^{(C)}(n), S^{(I)}(n), S^{(S)}(n))$, where

(i) $S^{(C)}(n) \in \mathfrak{I}^{(C)}$ is the clock frequency process at the generic slot n;

(ii) $S^{(I)}(n) \in \mathfrak{I}^{(I)}$ represents the quantized input traffic bit rate at the generic slot n;

(iii) $S^{(S)}(n) \in \mathfrak{I}^{(S)} = \{0, 1\}$ is the indicator variable of a switch at the generic slot n: $S^{(S)}(n) = 1$ if, in the slot n, the router is switching its clock frequency.

The set of states $\mathfrak{I}^{(C)}$ contains the *active frequencies*, that is, all the clock frequencies belonging to the set Φ. The set $\mathfrak{I}^{(I)}$ contains the considered quantized input traffic values.

Let us define the slot duration as the interval between two consecutive observations of the input bit rate; it will be indicated as Δ. In order to define the model time diagram, let us consider two generic states: $\underline{s}_{\Sigma 1} = (s_{C1}, s_{I1}, s_{S1})$ in the slot n and $\underline{s}_{\Sigma 2} = (s_{C2}, s_{I2}, s_{S2})$ in the slot $n + 1$. We assume the following event sequence.

(1) The first action at the beginning of the slot $n + 1$ is the evaluation of the new value of the input traffic bit rate. This value is obtained by sampling the bit rate values and smoothing the obtained sequence with an EWMA filter with a time constant equal to the time slot Δ.

(2) Then, according to the new value of the input traffic bit rate, the Governor decides the clock frequency for the new slot. Let us recall that, as said so far, a clock frequency modification determines that the router enters in the switching interval, during which some performance degradation occurs; all the clock frequency switching slots will be characterized by the state variable $S^{(S)}(n) = 1$. Let $\overline{T}_F$ be the duration of this period.

(3) Then, at the end of the slot $n + 1$, the system state variables are observed.

Now we can define the generic element of the state transition probability matrix as follows:

$$\begin{aligned} Q^{(\Sigma)}_{[s_{\Sigma 1}, s_{\Sigma 2}]} &= \text{Prob}\left\{S^{(\Sigma)}(n+1) = s_{\Sigma 2} \mid S^{(\Sigma)}(n) = s_{\Sigma 1}\right\} \\ &= Q^{(I)}_{[s_{I1}, s_{I2}]} \cdot \eta^{(C)}_{[s_{C1}, s_{C2}]}(s_{I2}) \cdot Q^{(S)}_{[s_{S1}, s_{S2}]}(s_{C1}, s_{C2}), \end{aligned} \tag{4}$$

where

(i) $Q^{(S)}_{[s_{S1}, s_{S2}]}(s_{C1}, s_{C2})$ is the transition probability of the clock frequency switch indicator variable. It is defined as follows:

$$Q^{(S)}_{[s_{S1}, s_{S2}]}(s_{C1}, s_{C2}) = \begin{cases} 1 & \text{if } (s_{C2} \neq s_{C1}, s_{S1} = 0, s_{S2} = 1) \\ 1 & \text{if } (s_{C2} = s_{C1}, s_{S1} = 0, s_{S2} = 0) \\ \dfrac{\Delta}{\overline{T}_F} & \text{if } (s_{S1} = 1, s_{S2} = 0) \\ 1 - \dfrac{\Delta}{\overline{T}_F} & \text{if } (s_{S1} = 1, s_{S2} = 1) \\ 0 & \text{otherwise,} \end{cases} \tag{5}$$

where the term $\Delta/\overline{T}_F$ is the probability that the router leaves the switching period. The first two probabilities are set to 1 because they represent the probability of changing the state variable $S^{(S)}(n)$ from 0 to 1 when a clock frequency switch occurs, and the probability of maintaining $S^{(S)}(n)$ equal to 0 when the router works normally.

(ii) $\eta^{(C)}_{[s_{C1}, s_{C2}]}(s_{I2})$ gives the probability of a clock frequency switch depending on the clock frequency switching law used by the Governor to decide the clock frequency according to the input traffic bit rate. It is set to 0 when, according to the clock frequency switching law, it is not possible that the Governor sets the value of s_{C2} when the input traffic value is s_{I2} and the current clock frequency is s_{C1}. Following the Governor policy illustrated in Section 2, it is defined as follows:

$$\eta^{(C)}_{[s_{C1}, s_{C2}]}(s_{I2}) = \begin{cases} 1 & \text{if } s_{I2} > B^{(M)}_{s_{C1}},\ B^{(M)}_{s_{C2}} = s_{I2} \\ 1 & \text{if } s_{I2} = B^{(M)}_{s_{C1}},\ s_{C2} = s_{C1} \\ p_G(s_{I2}, s_{C1}, s_{C2}) & \text{if } s_{I2} < B^{(M)}_{s_{C1}},\ s_{I2} \leq B^{(M)}_{s_{C2}} \leq B^{(M)}_{s_{C1}} \\ 0 & \text{otherwise.} \end{cases} \tag{6}$$

The term $p_G(s_{I2}, s_{C1}, s_{C2})$ is the frequency clock switching probability defined as in (3). As said in Section 2, it is adaptive with the current value of the input bit rate;

(iii) $Q^{(I)}$ is the state transition probability matrix for the quantized input traffic. It is an input of the problem, because it characterizes the traffic crossing the router.

Now, from the matrix $Q^{(\Sigma)}$ we can derive the system steady-state probability array $\underline{\pi}^{(\Sigma)}$ by solving the following system:

$$\begin{aligned} \pi^{(\Sigma)} Q^{(\Sigma)} &= \pi^{(\Sigma)}, \\ \pi^{(\Sigma)} \cdot \underline{1}^T &= 1, \end{aligned} \tag{7}$$

where $\underline{1}^T$ is a column array with all the elements equal to one. Its generic element, $\pi^{(\Sigma)}_{[\underline{s}_\Sigma]}$, is the steady-state probability of the state $\underline{s}_\Sigma = (s_C, s_I, s_S)$.

4. Performance Parameter Derivation

Let us now derive the main QoS parameters, with the aim of both evaluating router performance and supporting Router Governor design.

First let us calculate the mean power consumed by the router when the Governor applies the proposed policy:

$$P_{\text{MEAN}} = \sum_{\forall s_C \in \mathfrak{I}^{(C)}} \sum_{\forall s_I \in \mathfrak{I}^{(I)}} \Psi(s_C, s_I) \cdot \sum_{\forall s_S \in \mathfrak{I}^{(S)}} \pi^{(\Sigma)}_{[s_C, s_I, s_S]}, \tag{8}$$

where the term $\Psi(s_C, s_I)$ in (8) is a model input and represents the power consumed when the router is loaded with an input traffic bit rate of s_I and the clock frequency is s_C.

Now let us calculate the QoS parameters that can be degraded during clock frequency switching periods, according to the switching technique applied by the green router. The following three relevant cases will be considered.

(1) If the router remains frozen during the switching period and all the traffic arrived in that period is lost, as, for example, in the green NetFPGA reference router case [18, 19], the QoS parameter to be considered is the probability of loss occurring during the switching periods. It is defined as

$$P_{\text{Loss}} = \lim_{m \to +\infty} \frac{L(m)}{V(m)} = \frac{\overline{L}}{\overline{V}} = \frac{\sum_{s_C \in \mathfrak{F}^{(C)}} \sum_{s_I \in \mathfrak{F}^{(I)}} s_I \pi^{(\Sigma)}_{[s_C, s_I, 1]}}{\sum_{\underline{s}_\Sigma \in \mathfrak{F}^{(\Sigma)}} s_I \pi^{(\Sigma)}_{[\underline{s}_\Sigma]}}, \tag{9}$$

where $L(m)$ and $V(m)$ are the cumulative number of lost and arrived bits in m consecutive slots, respectively. The term $\overline{V}$ is the mean value of arrived bits per slot, while the term $\overline{L}$ represents the mean value of bits lost per slot.

(2) If the router remains frozen during the switching period and all the traffic arrived in that period is buffered, the QoS parameter to be considered is the mean delay suffered by the traffic arrived during the switching periods. It can be represented by the mean number of packets that arrive during a switching period:

$$\overline{D} = \frac{\overline{T}_F}{\Delta} \left[\sum_{\forall s_C \in \mathfrak{F}^{(C)}} \sum_{\forall s_I \in \mathfrak{F}^{(I)}} s_I \cdot \pi^{(\Sigma)}_{[s_C, s_I, 1]} \right], \tag{10}$$

where the term in squared brackets represents the mean traffic loading the router during a switching period, while $\overline{T}_F/\Delta$ represents the mean duration of the switching period expressed in slots.

(3) If a clock frequency switch causes a peak of energy consumption [21], the QoS parameter to be considered is the total mean power consumption, $P^{(\text{switch})}_{\text{MEAN}}$, defined as the sum of the mean value of the consumed power not considering the switching events, P_{MEAN}, and the mean power caused by the switches. Indicating the power consumed during a switch period as P_{switch}, and taking into account that a switch lasts for $\overline{T}_F/\Delta$ slots, the overall mean power can be calculated as follows:

$$P^{(\text{switch})}_{\text{MEAN}} = P_{\text{MEAN}} + \frac{P_{\text{switch}}}{\overline{T}_F/\Delta} \sum_{\forall s_C \in \mathfrak{F}^{(C)}} \sum_{\forall s_I \in \mathfrak{F}^{(I)}} \pi^{(\Sigma)}_{[s_C, s_I, 1]}. \tag{11}$$

The term P_{switch} is an input of the problem, while P_{MEAN} has been derived in (8).

Another important parameter that can be derived by the mean consumed power calculated as in (11) is the power saving percentage achieved by using the proposed Governor policy. Depending on whether we consider the power consumed during switches or not, it can be calculated as follows:

$$\rho = \frac{\left(P_{\text{MAX}} - P_{\text{MEAN}}\right)}{P_{\text{MAX}}} \cdot 100\%, \qquad \rho = \frac{\left(P_{\text{MAX}} - P^{(\text{switch})}_{\text{MEAN}}\right)}{P_{\text{MAX}}} \cdot 100\%, \tag{12}$$

where P_{MAX} is the power consumed if no saving policy is applied.

5. Model Application to the Governor Design

In this section we will apply the proposed analytical model to a case study to show how the model can be used in the Router Governor design. More specifically, as discussed so far, the goal is to design the clock frequency subset Φ and the δ probability term to be used in (3). Applying such a switching probability, the greater the value of the δ parameter, the more accurate is the Router Governor in the following input traffic bit rate variations, so obtaining higher power saving, but consequently increasing the loss probability.

The considered case study is constituted by a router like the NetFPGA reference router [22]. In this case the QoS parameter that is degraded by clock frequency switches is the loss probability, as discussed in the first of the cases listed in Section 4. The duration of the switching period depends on the specific implementation of the frequency scaling capability. In this case study we consider a switching period of about 2 μs: during this time interval the board is not able to process packets and this causes packet losses.

The proposed model is used to solve an optimization problem, finding the subset Φ of active clock frequencies and the probability term δ which maximize the power saving gain ρ, subject to the constraint $P_{\text{Loss}} \leq P^{(T)}_{\text{Loss}}$, where $P^{(T)}_{\text{Loss}}$ is the upper bound for the switching loss probability that can be tolerated, hereinafter also called target loss probability.

To this aim we started from a set of measurements achieved for the 2-frequency NetFPGA platform presented by the same authors in a previous work [18, 19], here extended to the following eight clock frequencies:F_1 = 15.625 MHz, F_2 = 31.25 MHz, F_3 = 46.875 MHz, F_4 = 62.5 MHz, F_5 = 78.125 MHz, F_6 = 93.75 MHz, F_7 = 109.375 MHz, and F_8 = 125 MHz. This set of frequencies constitutes the set $\overline{\Phi}$ presented in Section 2.

Table 1: Nonnull elements of the input traffic transition probability matrix.

Inferior pseudodiagonal		Main diagonal		Superior pseudodiagonal	
Pos	Value	Pos	Value	Pos	Value
		(1, 1)	$9.9990e-001$	(1, 2)	$1.0000e-004$
(2, 1)	$3.1569e-005$	(2, 2)	$9.9993e-001$	(2, 3)	$3.5098e-005$
(3, 2)	$6.7811e-006$	(3, 3)	$9.9994e-001$	(3, 4)	$4.8774e-005$
(4, 3)	$4.1255e-005$	(4, 4)	$9.9995e-001$	(4, 5)	$6.3636e-006$
(5, 4)	$1.9848e-005$	(5, 5)	$9.9994e-001$	(5, 6)	$3.8975e-005$
(6, 5)	$3.8314e-005$	(6, 6)	$9.9992e-001$	(6, 7)	$3.8609e-005$
(7, 6)	$1.3970e-005$	(7, 7)	$9.9990e-001$	(7, 8)	$8.6030e-005$
(8, 7)	$1.4286e-004$	(8, 8)	$9.9986e-001$		

As demonstrated in [18], the consumed power can be modeled as follows:

$$\Psi\left(f_C, B_{\mathrm{IN}}\right) = P_C\left(f_C\right) + KP_E\left(f_C\right) + N_I\left(B_{\mathrm{IN}}\right)\cdot E_p\left(f_C\right) + \\ + R_I\left(B_{\mathrm{IN}}\right)\cdot E_r\left(f_C\right) + R_O E_t\left(f_C\right), \tag{13}$$

where f_C is the CPU clock frequency while B_{IN} is the bit rate of the router input traffic. The term $P_C(f_C)$ is the constant baseline power consumption of the NetFPGA card (without any Ethernet ports connected); $P_E(f_C)$ is the power consumed by each Ethernet port (without any traffic flowing); $E_p(f_C)$ is the energy required to process each packet (parsing, routing lookup, etc.); $E_r(f_C)$ is the energy required to receive, process, and store a byte on the ingress Ethernet interface; $E_t(f_C)$ is the energy required to store, process, and send a byte on the egress Ethernet interface; K is the number of Ethernet ports connected (1 to 4); $N_I(B_{\mathrm{IN}})$ is the input traffic bit rate to the NetFPGA card in packets-per-second (pps); $R_I(B_{\mathrm{IN}})$ is the input rate to the NetFPGA card in bytes-per-second; $R_O(B_{\mathrm{IN}})$ is the output rate from the NetFPGA card in bytes-per-second.

Results achieved by applying the power model in (13) to the considered set of eight frequencies are shown in Figure 3. Further measurements on the power consumption relative to the running of the Router Governor procedures have shown that it is negligible with respect to the power consumption of the board. For this reason it has not been considered here.

In order to achieve the input traffic model, we have quantized a traffic trace measured at the ingress of the DIEEI lab router in eight different bit rate levels, ranging from 0.25 Gbit/s to 3.75 Gbit/s with steps of 0.5 Gbit/s. First- and second-order statistics of that trace, in terms of probability density function (pdf) and autocorrelation function (acf), are represented in Figure 4. Then, solving an inverse eigenvalue problem [23, 24], we derived the input traffic Markov model characterized with the same statistical functions as in Figure 4. The traffic model is constituted by the transition probability matrix $Q^{(I)}$ and the bit rate array $\Gamma^{(I)}$. The matrix $Q^{(I)}$ is a tridiagonal matrix whose nonnull elements are listed in Table 1. The bit rate array is $\Gamma^{(I)} = [0.25, 0.75, 1.25, 1.75, 2.25, 2.75, 3.25, 3.75]$ Gbit/s. The considered traffic has a mean value of 2.66 Gbit/s and a standard deviation of 0.946 Gbit/s.

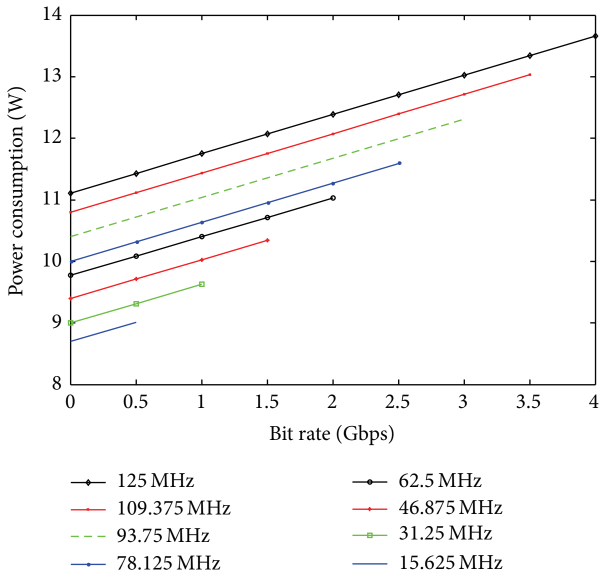
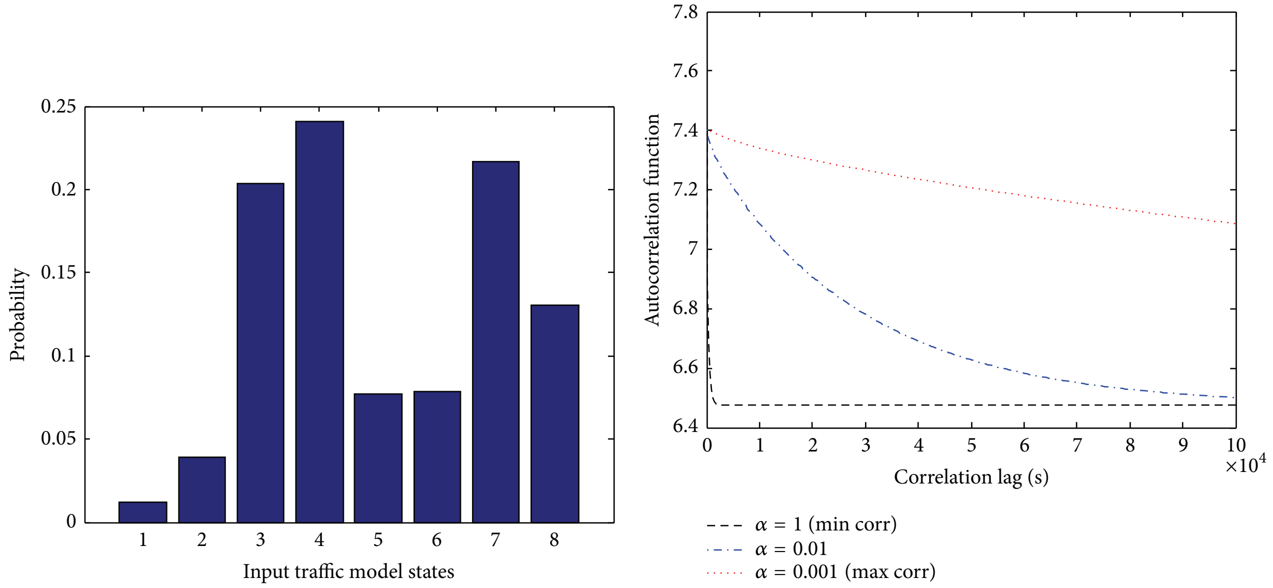


Figure 3: Power consumption model for a router with 8 clock frequencies.

From the traffic model $(Q^{(I)}, \Gamma^{(I)})$ we have derived a set of ten different models, obtained as follows.

(i) $T_i = (Q_i^{(I)}, \Gamma^{(I)})$, with $1 \le i \le 5$, characterized by a transition probability matrix $Q_i^{(I)}$ derived from $Q^{(I)}$ by multiplying the terms of the two pseudodiagonals by a coefficient $\alpha_i \in \{10^4, 10^2, 10^0, 10^{-2}, 10^{-4}, 10^{-6}\}$. The terms of the main diagonals are then calculated such that the sum of each row is equal to one. In this way the traffic modeled by T_1 and T_2 result less correlated than the measured traffic, the traffic modeled by T_3 coincides with the real traffic, while the other models represent more correlated traffic.

(ii) $T_i = (Q_i^{(I)}, \overline{\Gamma}^{(I)})$, with $6 \le i \le 10$, characterized by the same five transition probability matrices of the previous case, that is, $Q_i^{(I)} = Q_{i-5}^{(I)}$, but with a bit rate array $\overline{\Gamma}^{(I)}$ achieved by mirroring the array $\Gamma^{(I)}$ of the



(a) Probability density function

(b) Autocorrelation function

FIGURE 4: Input traffic first- and second-order statistics.

previous case. By so doing the new pdf is the mirror of the one shown in Figure 4(a), and the new mean value is equal to 1.33 Gbit/s.

Using the analytical system model defined in previous section, we have analyzed the loss probability and the power consumption of the router architecture discussed so far. More in details, we have considered 127 different frequency sets Φ, achieved by choosing from the whole set $\overline{\Phi}$ all the possible subsets containing the highest frequency; that is, F_8 = 125 MHz. In other words, the subsets we have considered are $\{F_1, F_8\}, \{F_2, F_8\}, \{F_3, F_8\}, \ldots, \{F_1, F_2, F_8\}, \{F_1, F_3, F_8\}, \{F_1, F_4, F_8\}, \ldots, \{F_1, F_2, F_3, F_4, F_5, F_6, F_7, F_8\}$.

We have solved the optimization problem stated at the beginning of this section, for each of the considered ten traffic models, and versus the target loss probability $P_{\text{Loss}}^{(T)}$. The results are shown in Figure 5, where each point corresponds to the configuration (δ, Φ) that provides the highest power saving for each target loss probability and traffic model.

The reader can notice that, when the value of $P_{\text{Loss}}^{(T)}$ increases, the power saving for all the curves tends to an asymptotic value which mainly depends on the mean value of the input traffic. Therefore this result highlights that the maximum achievable power saving is influenced by the mean value of the input traffic bit rate. Moreover, in the same figure we can also notice that the higher the autocorrelation of the traffic, the higher the power saving for a given target loss probability. It is caused by the fact that, when the traffic autocorrelation is higher, the Router Governor can follow the traffic profile with more rare switches of the clock frequency.

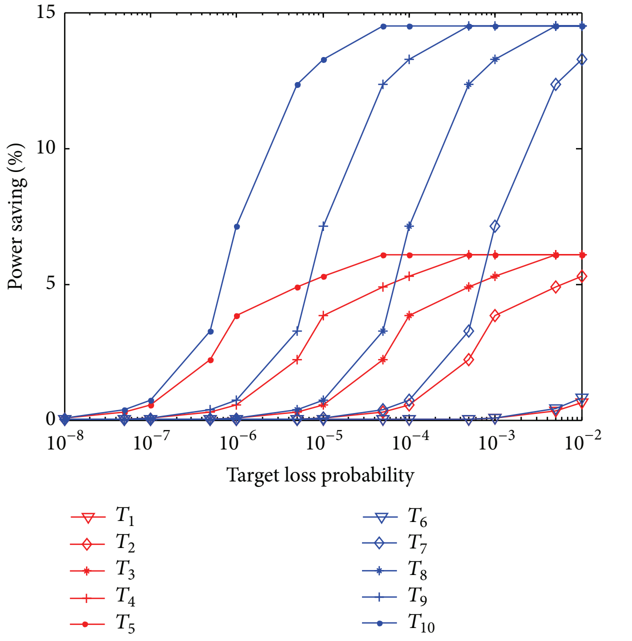
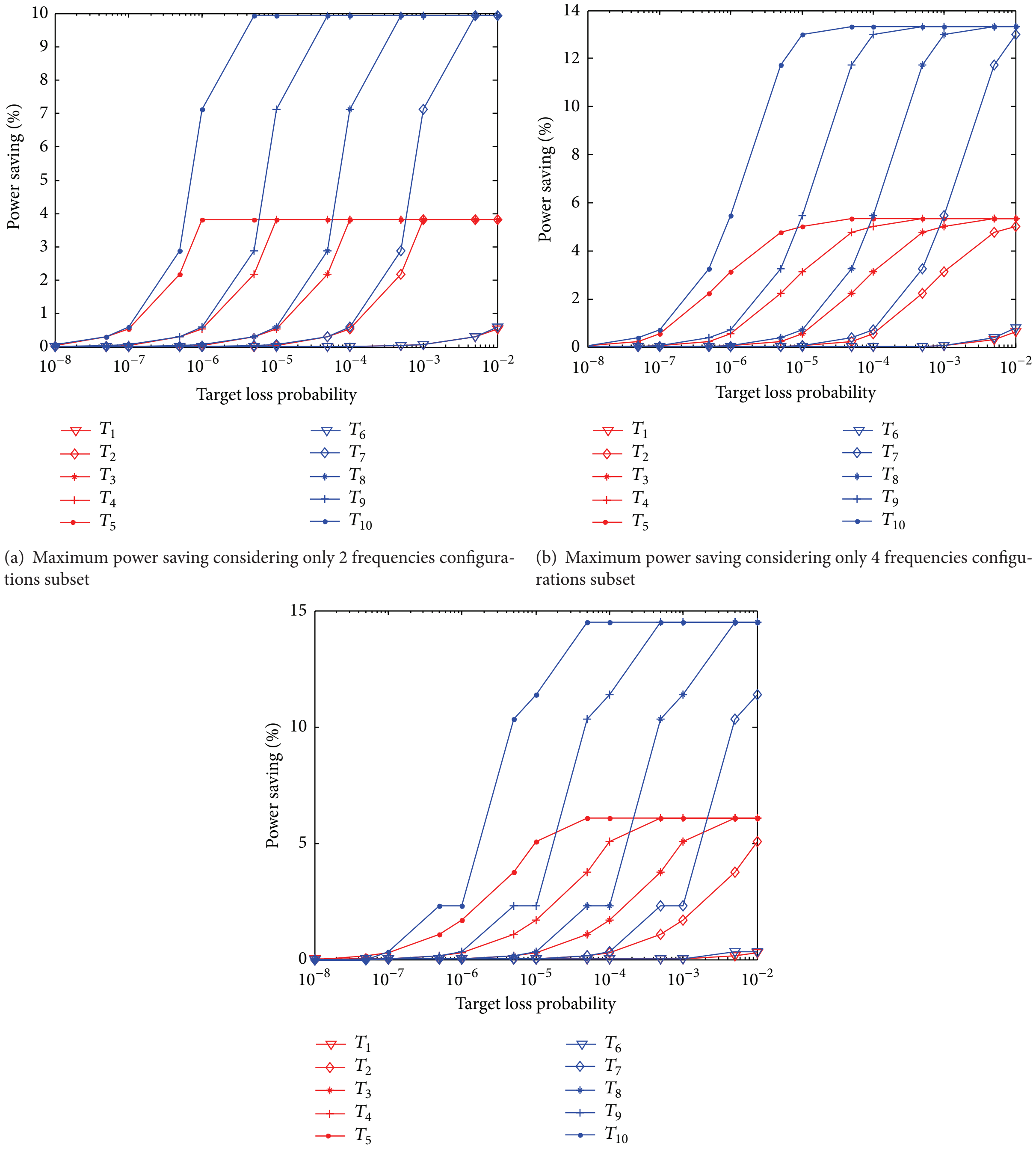


FIGURE 5: Maximum power saving due to the Router Governor given a maximum loss probability.

Now, in order to evaluate the impact that the used frequencies have on the router performance (target loss probability and power consumption), we have solved the optimization problem considering a constant number of frequencies, leaving the system free to choose the best value of δ and the best set Φ with a number of frequencies equal to the considered one. Figures 6(a), 6(b), and 6(c) show the results for the cases of two, four, and eight frequencies, respectively. We can notice again that the maximum achievable power saving is higher using a higher number of frequencies; this is, because in this case the router processor is able to follow the input traffic more accurately.



(a) Maximum power saving considering only 2 frequencies configurations subset

(b) Maximum power saving considering only 4 frequencies configurations subset

(c) Maximum power saving considering only 8 frequencies configurations subset

FIGURE 6: Power saving versus target loss probability resulted by optimization problem fixing the number of frequencies.

To better investigate the behavior of the Router Governor varying the frequency set and the δ parameter, Figures 7, 8, and 9 show a detailed view of a subset of the cases already represented in Figures 5 and 6. In particular, we consider the cases corresponding to a loss probability target of 10^{-6}. Figure 7 shows the results of the most general optimization problem, solved over the 127 frequency sets described so far. Instead, Figures 8 and 9 present results achieved for the two optimization problems characterized by two and four frequencies, respectively. Such figures explore the frequency configurations and the δ parameter value selected by the optimization algorithm, also showing the power gain of each case. Looking at the above figures we can observe that the Router Governor changes the subset of used frequencies according to both the mean and the autocorrelation of the input traffic.

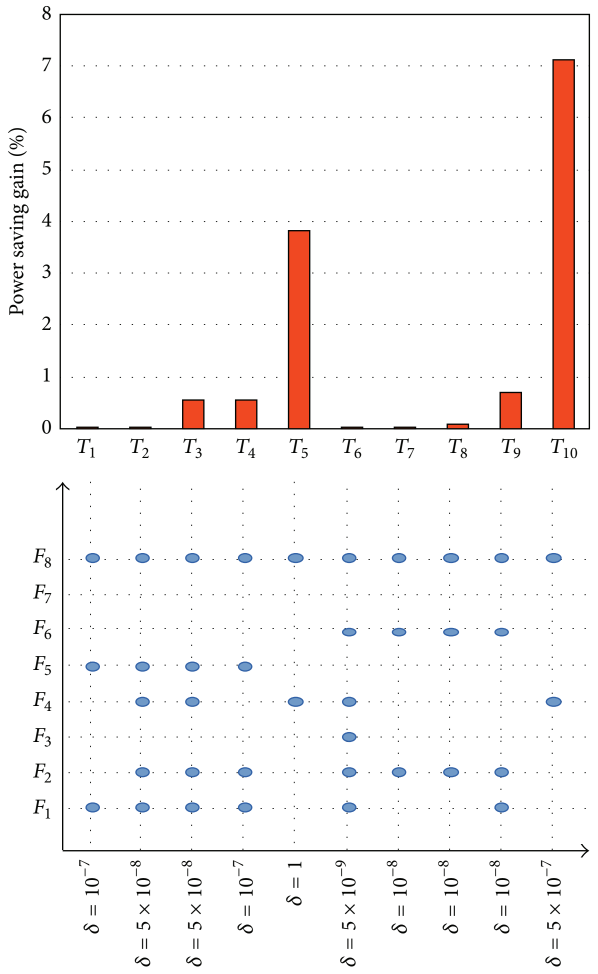


Figure 7: Power saving and selected configuration (δ, Φ) corresponding to a target loss probability of 10^{-6}.

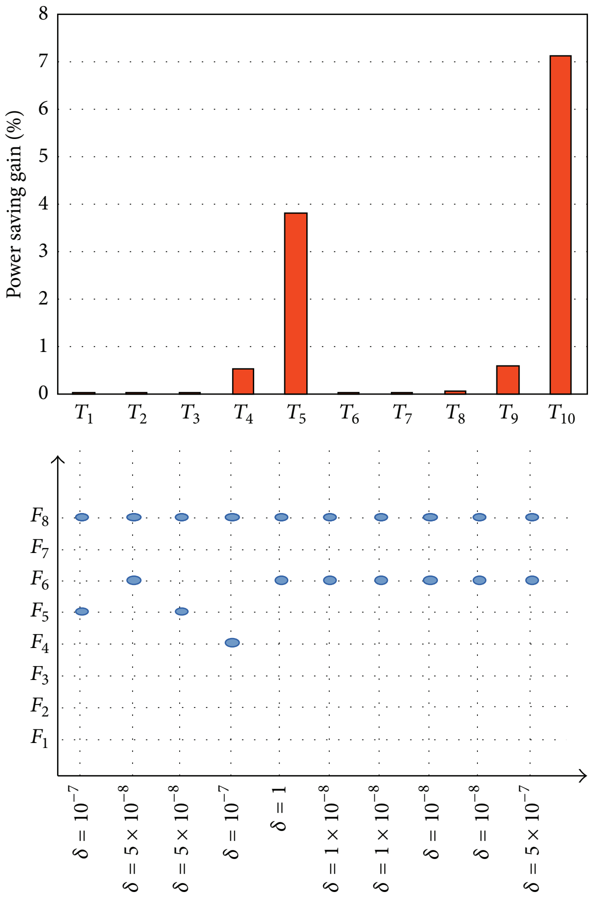


Figure 8: Power saving and selected configuration (δ, Φ) corresponding to a target loss probability of 10^{-6}—2-frequency subset.

To better understand the results of the optimization algorithm, we need to further analyze those figures, and doing that, we have to take into account that for cases T_1 and T_6, the traffic is uncorrelated and so the achievable power consumption is very low (see Figures 5 and 6). So, the Router Governor selects a low value of δ to avoid too frequent clock frequency switches. As far as the other cases are concerned, when the traffic autocorrelation increases the number of frequencies can be augmented: in fact, if the Router Governor sets the clock frequency to a value that supports the current input traffic and such frequency remains unchanged for a given amount of time, both the loss probability and the power consumption will be positively influenced.

In Figure 7 the reader can notice that for T_2 and T_3 the optimization problem has selected five frequencies and δ is equal to $5 \cdot 10^{-8}$, whereas for the T_4 case four frequencies have been selected, but the clock frequency is more free to follow the input traffic variations, since δ is equal to 10^{-7}. Instead, in the T_5 case, where the autocorrelation of the input traffic is very high, the algorithm selects only two frequencies but, since $\delta = 1$, leaves the system completely free to change between them every time the input traffic varies.

Regarding Figure 8, same considerations can be formulated, but here we can found a much more evident result for cases T_2, T_3, and T_4: in fact, the higher the autocorrelation of the traffic, the lower the frequencies we can use and therefore the higher the power saving the system can achieve. Also in the same figure, we can notice, for the T_5 case, that the system is free to change the clock frequency following the input traffic (δ is equal to 1). In Figure 9 the optimization algorithm selects four frequencies for each case: for both the cases T_2 and T_3 the δ parameter is equal to $5 \cdot 10^{-8}$, whereas for T_4 and T_5 lower frequencies are selected and the δ parameter leaves the Governor freer to change the clock frequency more often, increasing the power saving and maintaining the same loss probability.

Finally, in order to evaluate the impact of δ on the performance, we have solved the optimization problem for all the 127 sets described so far, but for two given values of δ, that is, 10^{-4} and 10^{-6}. The relative results are in Figures 10(a) and 10(b), respectively. First of all, it is easy to notice that the higher the value of δ, the higher the power saving, since the Router Governor can follow the input traffic more accurately: in fact, we can achieve a higher power saving using a δ equal to 10^{-4} rather than 10^{-6}.

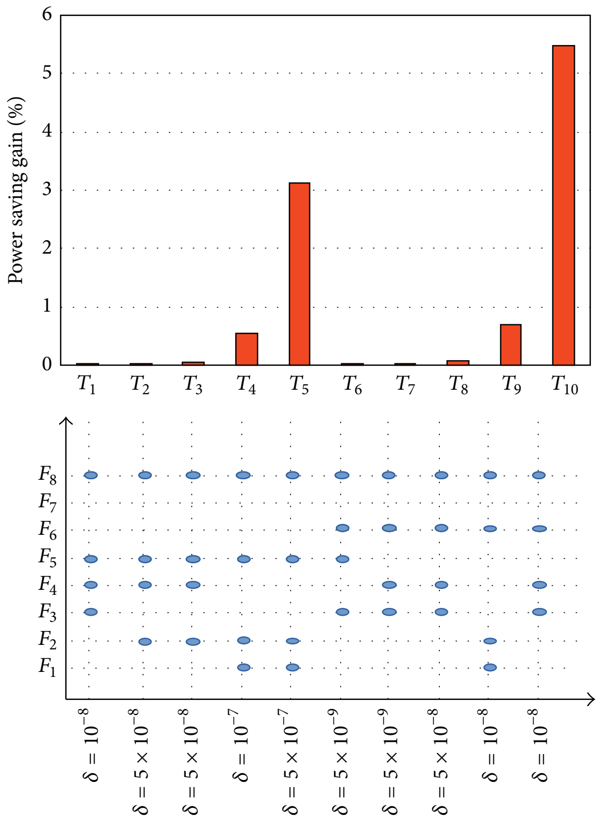
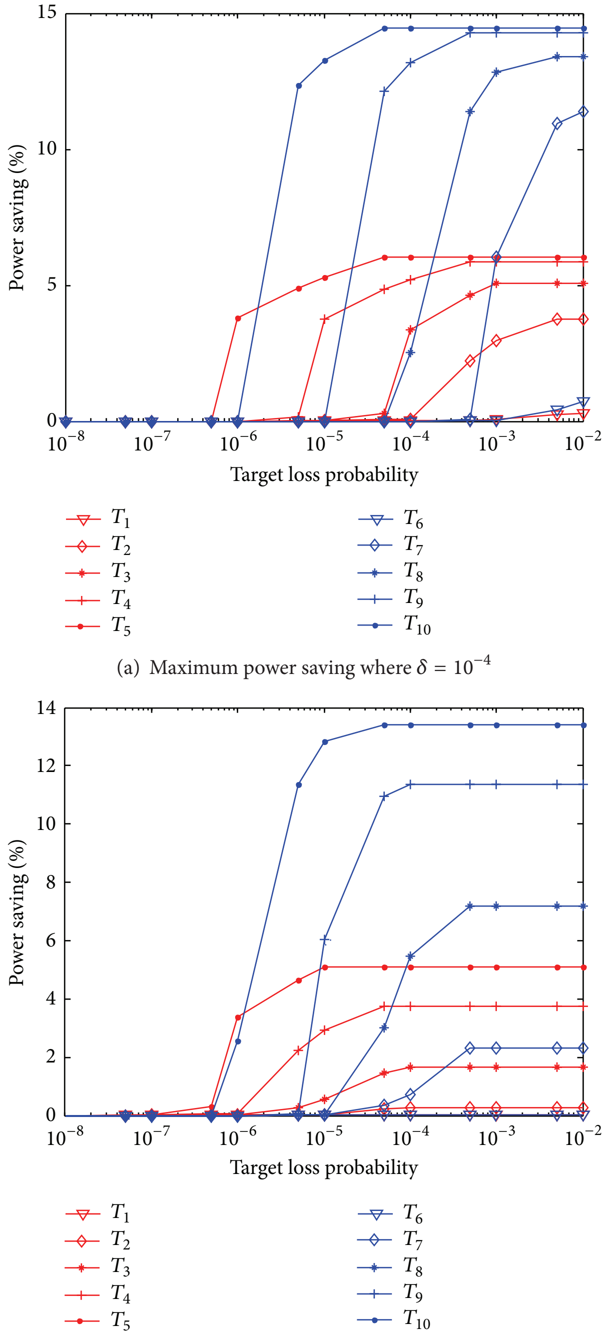


Figure 9: Power saving and selected configuration (δ, Φ) corresponding to a target loss probability of 10^{-6}—4-frequency subset.

It is worth noting that the designed Router Governor can have a strong impact on both power saving and loss probability. In fact, as stated so far, the main important contribution provided by the Governor to the system is to find the best tradeoff between power saving and loss probability. In order to better highlight this matter, in Figures 11 and 12 we have presented power saving and loss probability versus the δ parameter. Reminding that low values of δ lead the system to rarely change the frequency whereas high values of δ lead the system to change the frequency often, accurately following the input traffic. For example, when δ is equal to 1 the system switches the frequency always to the lowest possible one and it corresponds to have high values of power saving, but at the same time high values of loss probability that assumes basically intolerable values (that are very close to 1).

Let us note that all the above figures have been presented to evaluate the impact of the traffic behavior, the parameter δ and the set Φ on the power consumption, and the system performance, but the same figures can also be used by the system designer to choose suitable values of those parameters according to the input traffic, looking for the best tradeoff between power saving and loss probability.



(a) Maximum power saving where $\delta = 10^{-4}$

(b) Maximum power saving where $\delta = 10^{-6}$

Figure 10: Power saving versus target loss probability resulted by optimization problem fixing δ parameter.

6. Conclusions

In this paper, we have proposed an analytical model to be used to design a Governor for green routers using frequency scaling to save energy. The design aims at limiting the performance worsening due to frequent clock frequency switches. More specifically, the model is used to evaluate the input traffic impacts on the choice of the active router clock

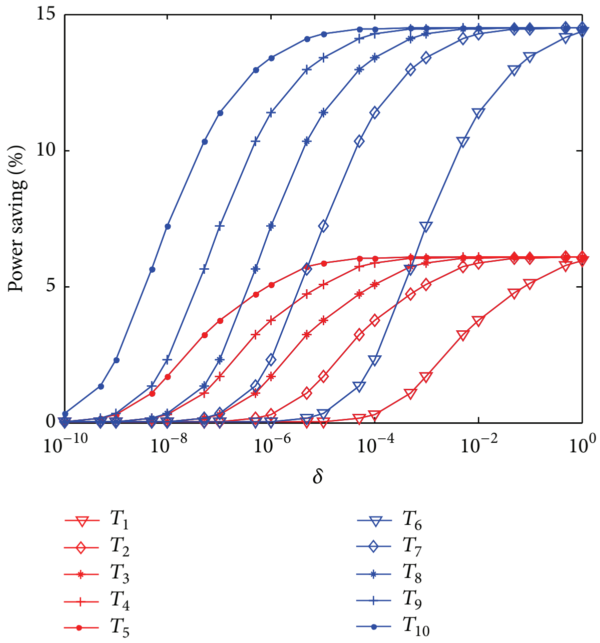


Figure 11: Power saving versus δ parameter.

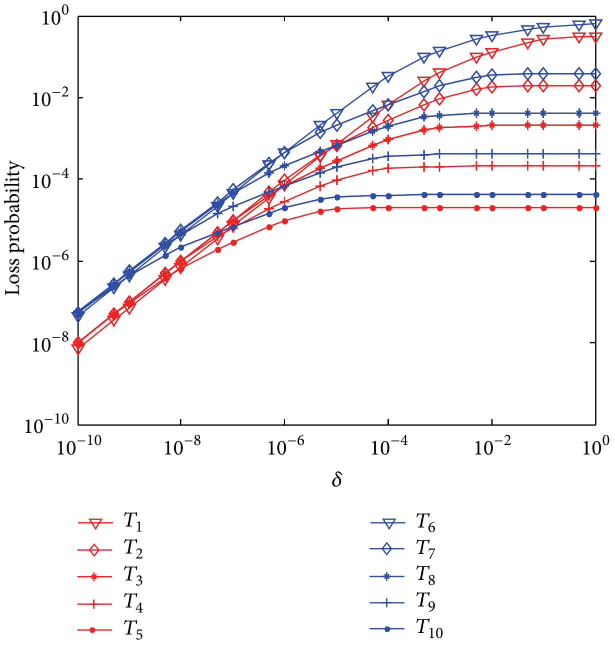


Figure 12: Loss probability versus δ parameter.

frequencies and on the overall green router performance. A case study based on the open NetFPGA reference router is considered to show how the proposed model can be easily applied to a real case scenario.

The model allows the manufacturers to evaluate the power saving gain which is possible to obtain when the proposed Router Governor is used. The future directions that we will pursue are related to an extension of the model to capture the behavior of both input and output queues. In addition, we are working to use the achieved results to design a traffic shaper that is able to modify the autocorrelation of the input traffic to maximize the achieved power saving.

Conflict of Interests

The authors declare that there is no conflict of interests regarding the publication of this paper.

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