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Riccardo Caponetto[1], Giovanni Dongola[1], Guido Maione[2] and A Pisano[3]

Abstract

In this paper an integrated circuit (IC) design of the fractional order proportional-integral-derivative (PID) controller is proposed. The development of the IC device is realized in Cadence environment, using the switched capacitors (SC) technology in order to reduce the area on the silicon wafer and to improve the electrical controllability. In order to obtain transfer functions that describe the fractional order of the differ-integral operator it is necessary to use interpolation methods, in particular, the choice in this work has fallen on the Oustaloup interpolation. This procedure is aimed at implementing a series of pole-zero blocks that approximate the non-integer order. The realized approach is able to guarantee a good approximation of the fractional order PID and simultaneously propose a detailed circuit analysis of the influence of the non-idealities, in particular the phenomenon of warping. This takes into account the distortion introduced by the s-domain to the z-domain transition, acting on the positions of poles and zeros, especially those at a higher frequency. Time and frequency domain result tests confirm the feasibility and reliability of the SC implementation.

Keywords

Digital filters, fractional order controller, integrated circuit, sampling rates, switched capacitors technology

1. Introduction

Proportional-integral-derivative (PID) controllers are commonly used in many industrial divisions – for example, chemical, petrochemical, pulp and paper, oil and gas, food and beverages, municipal water and sewerage facilities, etc. Thus any minimal innovation can lead to relevant improvements in the area of automatic control systems. For this reason, the fractional order PID (FO-PID), (Podlubny, 1999), represents an significant research topic and an wide application area of industrial control (Oustaloup, 1983; Dorcak et al., 2000). Therefore the implementation of these regulators in integrated technology is very attractive. The authors proposed a hardware implementation of FO-PID in an analog environment (Caponetto and Dongola, 2008).

The goal of this paper is the development on chip of the digital structure of the FO-PID. The basic building block for the implementation of such systems is the fractional order integrator. The fractional order derivative operator is obtained by applying a derivative action of integer order to the complementary fractional order integration. Thus the hardware structure of the FO-PID is obtained according to the configuration shown in Figure 1.

In order to define transfer functions that describe fractional order integration it is mandatory to use interpolation methods, in particular in this paper the Oustaloup interpolation (Oustaloup, 1981; Oustaloup et al., 2000) has been applied. This procedure is aimed at implementing a series of pole-zero blocks that approximate the non-integer order integrator in a defined working bandwidth.

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At the beginning, a fractional order differ-integrator circuital version with operational amplifiers (OA) and RC blocks was implemented. Successively, in order to carry out the design in integrated technology, it was necessary to replace each resistance with the switched capacitor (SC) technique (Caponetto et al., 2008, 2009), which simulates the resistance using capacitors whose charge and discharge phases are controlled through switches that commutate at the same frequency, but with a half period phase shift. The studies made on the circuital solutions for the realization of the non-integer order differ-integrator have produced good results during the simulation in PSpice environment, but this was not enough to move to the on-chip realization. In fact it is necessary to take into account size, rules and characteristics of the technology adopted.

The authors proposed a first study on an on-chip circuital implementation of the fractional order differ-integrator in Caponetto et al. (2010) where they suggested a different circuital topology. The idea was to divide the circuit realized in the previous work (Caponetto et al., 2008, 2009) in two sub-blocks in cascade, the first one realize half of the pole-zero pairs,

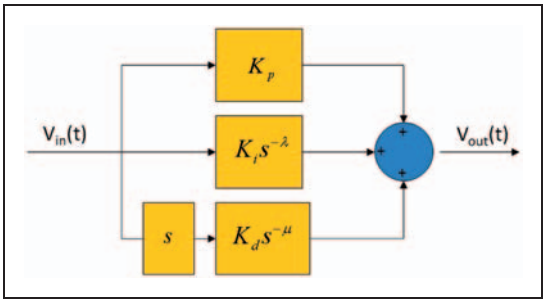

Figure 1. Structure for realizing the fractional order proportional-integral-derivative.

Table 1. Structure for realizing the fractional order differ-integrator.

Realized Differ-integral Order	Blocks used					
	d/dt	−0,1	−0,2	−0,3	−0,4	−0,5
−1			x	x		x
−0.9					x	x
−0.8				x		x
−0.7				x	x	
−0.6			x		x	
−0.5						x
−0.4					x	
−0.3				x		
−0.2			x			
−0.1		x				
0.1	x				x	x
0.2	x			x		x
0.3	x			x	x	
0.4	x		x		x	
0.5	x					x
0.6	x				x	
0.7	x			x		
0.8	x		x			
0.9	x	x				
1	x					

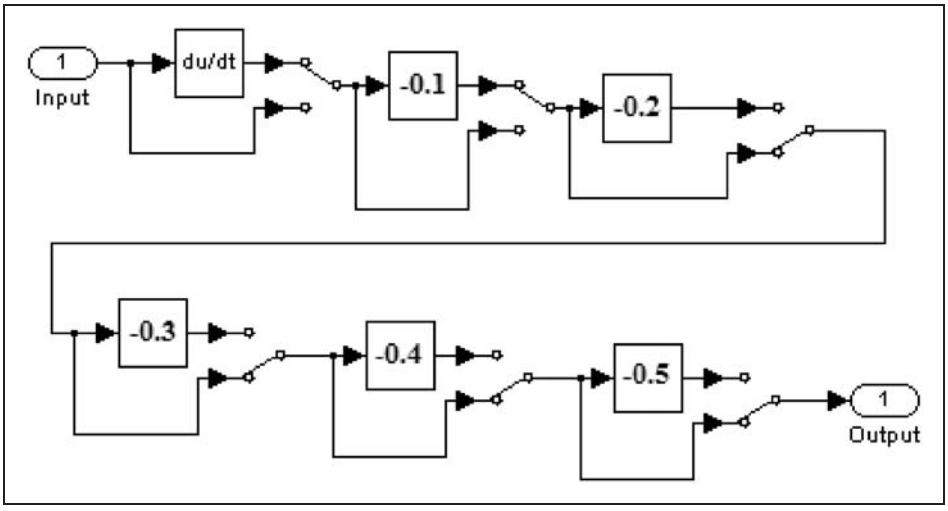

Figure 2. Structure for realizing the fractional order differ-integrator.

while the second one realize the second half of the Oustaloup interpolation. The two sub-blocks had different switching frequencies in order to limit the capacitive spread and reduce the warping effect. In fact, in this work the authors made a detailed analysis of the influence of the non-idealities in order to obtain a design fit for IC implementation. Anyway a similar circuital topology, even if it perfectly realizes a single differ-integral operator, does not allow to implement the FO-PID on chip.

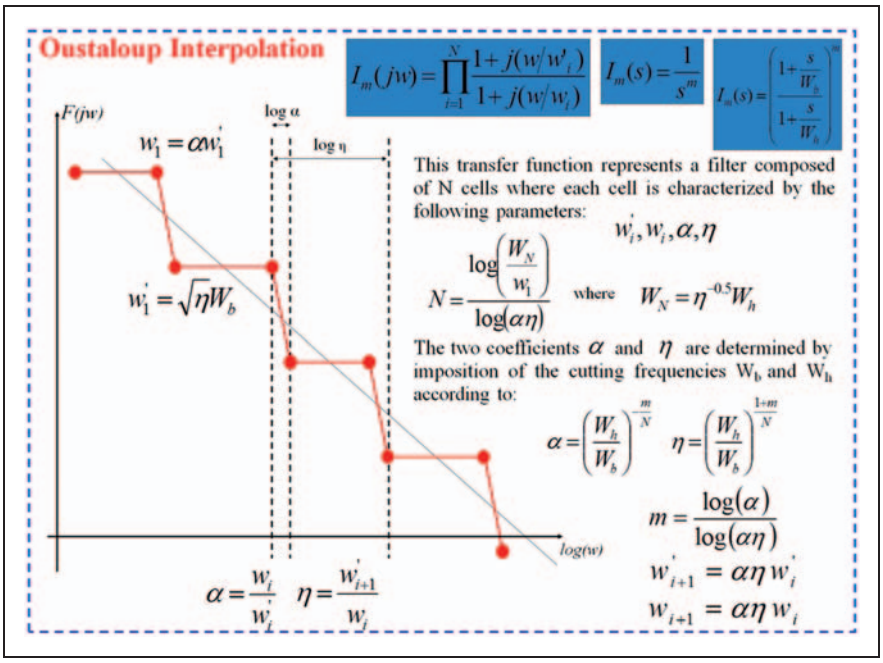

Figure 3. Oustaloup interpolation for fractional order integrator.

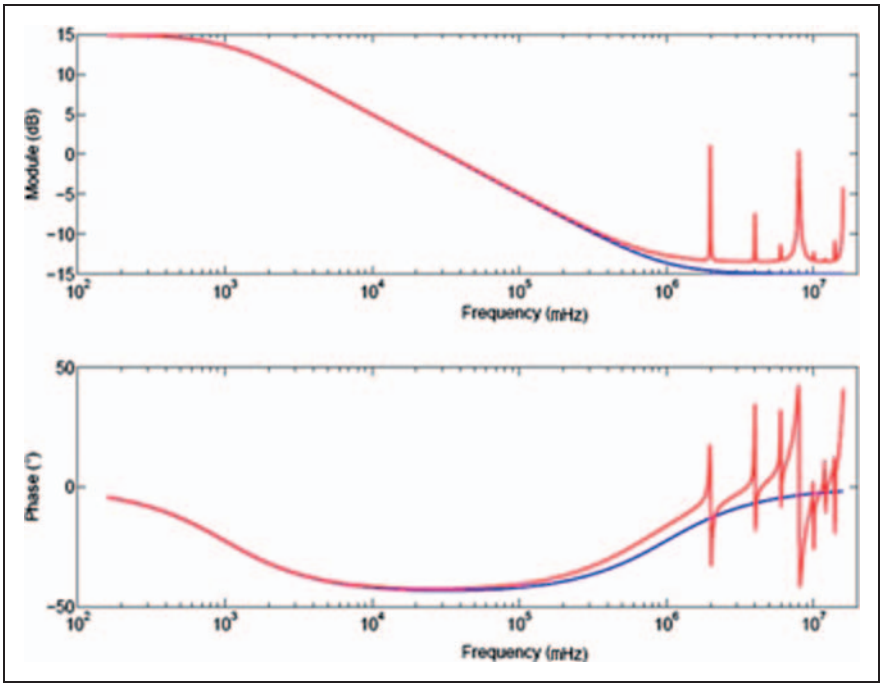

Figure 4. Bode Diagrams: ideal (in blue), real (in red) for an integrator with order equal to 0.5.

In this paper the authors propose the implementation on chip of the FO-PID using the structure shown in Figure 1, where the fractional order differ-integrator is realized in Cadence environment according to the configuration presented in Figure 2. Control purposes require an easy change of the order of the system: unfortunately this feature cannot be achieved by direct manipulation of the circuit, whose parameters have been obtained for a specific value of the integration order. A good solution is given by the structure in Figure 2. Each order (from –1 to 1 in steps of 0.1) is obtained by the activation, through a suitable switching configuration, of a cascade structure (see Table 1).

2. Circuital parameters calculus for Oustaloup interpolation

The fractional order integrator is the basic block for the realization of a non-integer order differ-integrator. In particular, it was shown that by providing a derivative operator of the integer order $n=1$ and various fractional order integrator with order $m=0.1$, 0.2, 0.3, 0.4, 0.5, any differ-integrator with a non-integer order q ($-1 \leq q \leq 1$) can be implemented, suitably combining these building blocks.

Furthermore, a working bandwidth for the differ-integrator should be defined first of all (Caponetto et al., 2008, 2009). The bandwidth selected in this paper is (10 Hz, 100 Hz). Thus the Oustaloup interpolation is defined in a bandwidth that starts a decade before and ends a decade after the one of interest, i.e. in the frequencies range equal to (1 Hz, 1 kHz).

An algorithm that automatically calculates the Matlab transfer function of the Oustaloup interpolation, the circuit parameters, the pre-warping poles and zeros and the capacitive spread was developed. The operations performed by this script are listed below.

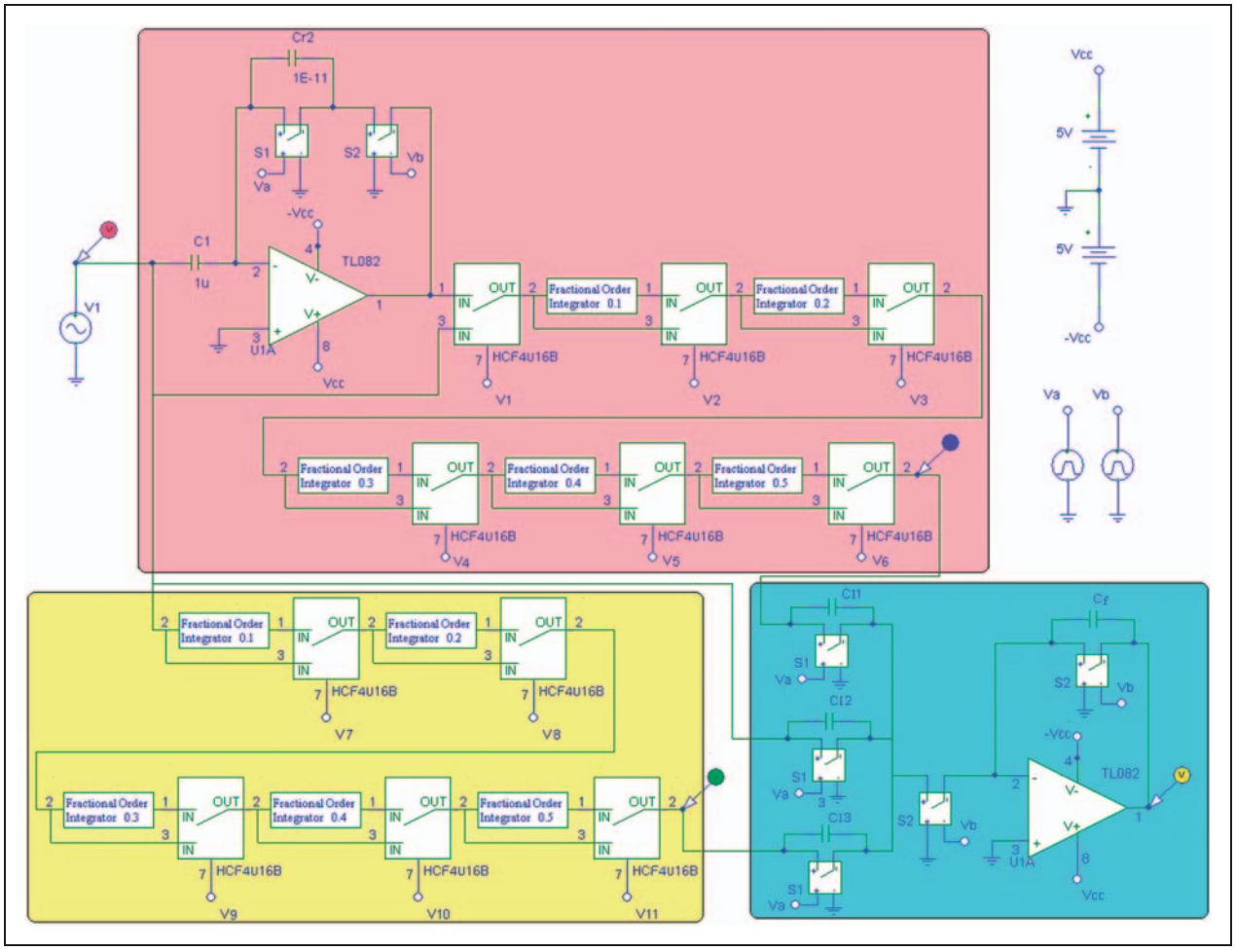

Figure 5. Schematic of the fractional order proportional-integral-derivative.

2.1. Matlab algorithm

The developed Matlab algorithm requires as inputs:

- The differ-integral order $\boldsymbol{m}$ to be realized.
- The gain at the center of the selected bandwidth.
- The lower ($\boldsymbol{W_b}$) and the higher ($\boldsymbol{W_h}$) frequencies of the working bandwidth.
- The switching frequency $\boldsymbol{f_s}$.

The gain in dB at the center frequency of the bandwidth is fixed equal to zero, while the switching frequency must be chosen according to the Shannon theorem:

$$f_s \geq 2BW \tag{1}$$

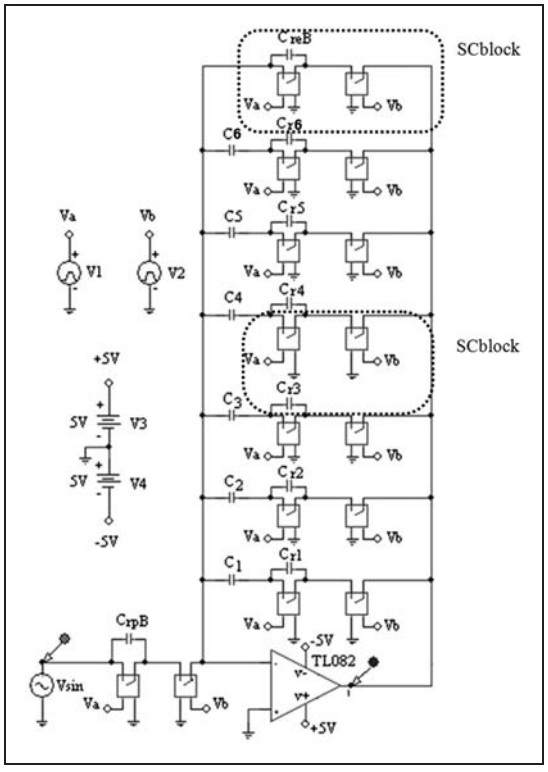

Figure 6. Schematic of the fractional order integrator.

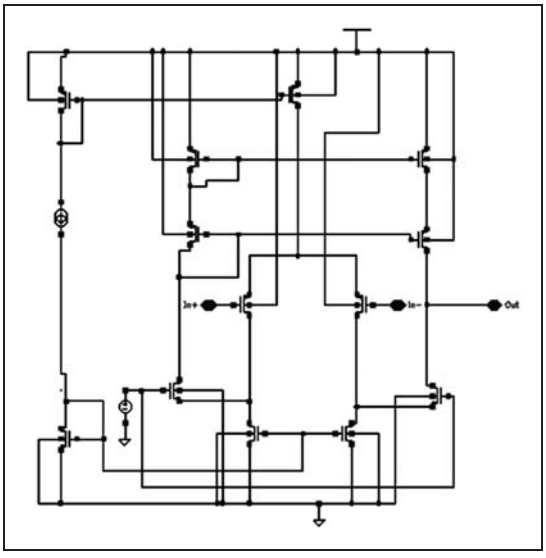

Figure 8. Folded cascade amplifier in Cadence environment.

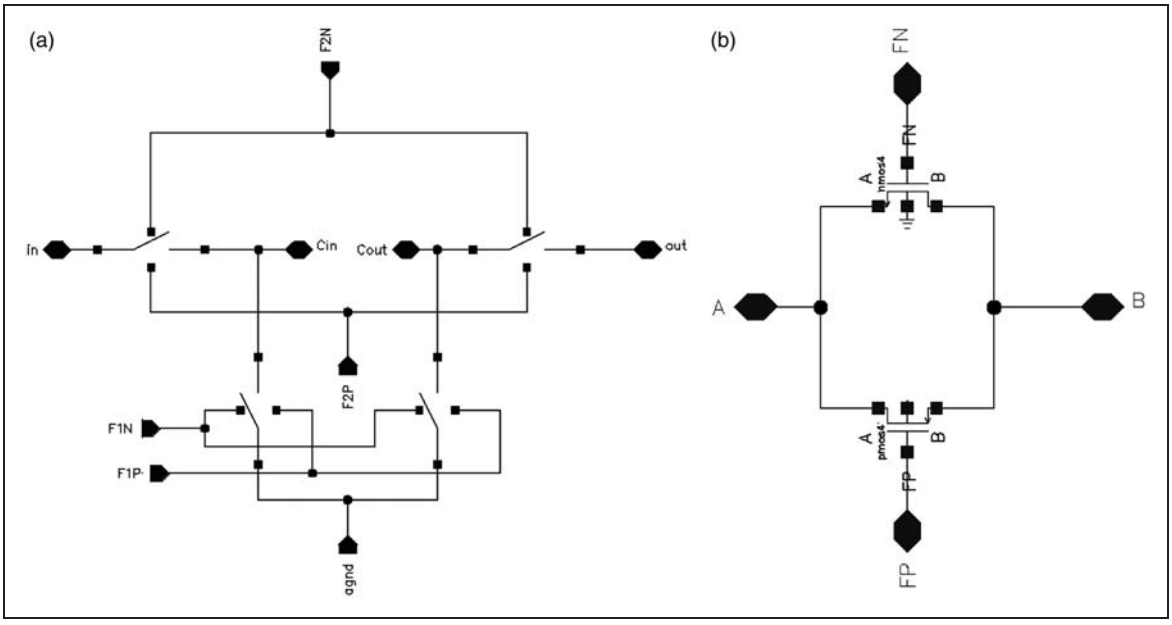

Figure 7. Schematic in Cadence of SCblock (a) and switch (b).

where BW is the maximum bandwidth of the signal. The algorithm imposes two pole-zero pairs per decade, so that, the number N of cells turns out to be 6, since the decades in the range (1 Hz, 1 kHz) are 3 as shown in Figure 3.

As a first step the DC gain is calculated, taking into account the slope of the Bode module diagram $\boldsymbol{m}$ and the first pole $\boldsymbol{w_1}$ of the Oustaloup interpolation. Then the parameters $\boldsymbol{\alpha}$ and $\boldsymbol{\eta}$, the transfer function and the circuit parameters according to the formulas described in the previous works (Caponetto et al., 2008, 2009) are calculated. This strategy allows to determine the minimum capacity inside the whole circuit, assign it the smallest capacity that can be reached in the applied technology (200fF), and therefore calculate all the remaining capacities normalized to it. It is thus possible to derive the minimum and maximum value of the capacitors and then evaluate the obtained capacitive spread.

The second part of the algorithm is related to the calculus of transfer functions in the z-domain and the estimation of the warping, evaluated comparing the ideal Bode plots with the Bode of the real circuit (Figure 4). The warping effect is evident at frequencies close to the switching one.

Thus the calculus of the pre-distorted poles and zeros in accordance with the pre-warping law is carried out in (Caponetto et al., 2010); the capacitor values that allow such couples of the pre-distorted pole-zero to be obtained and the resulting new capacitive spread are recalculated.

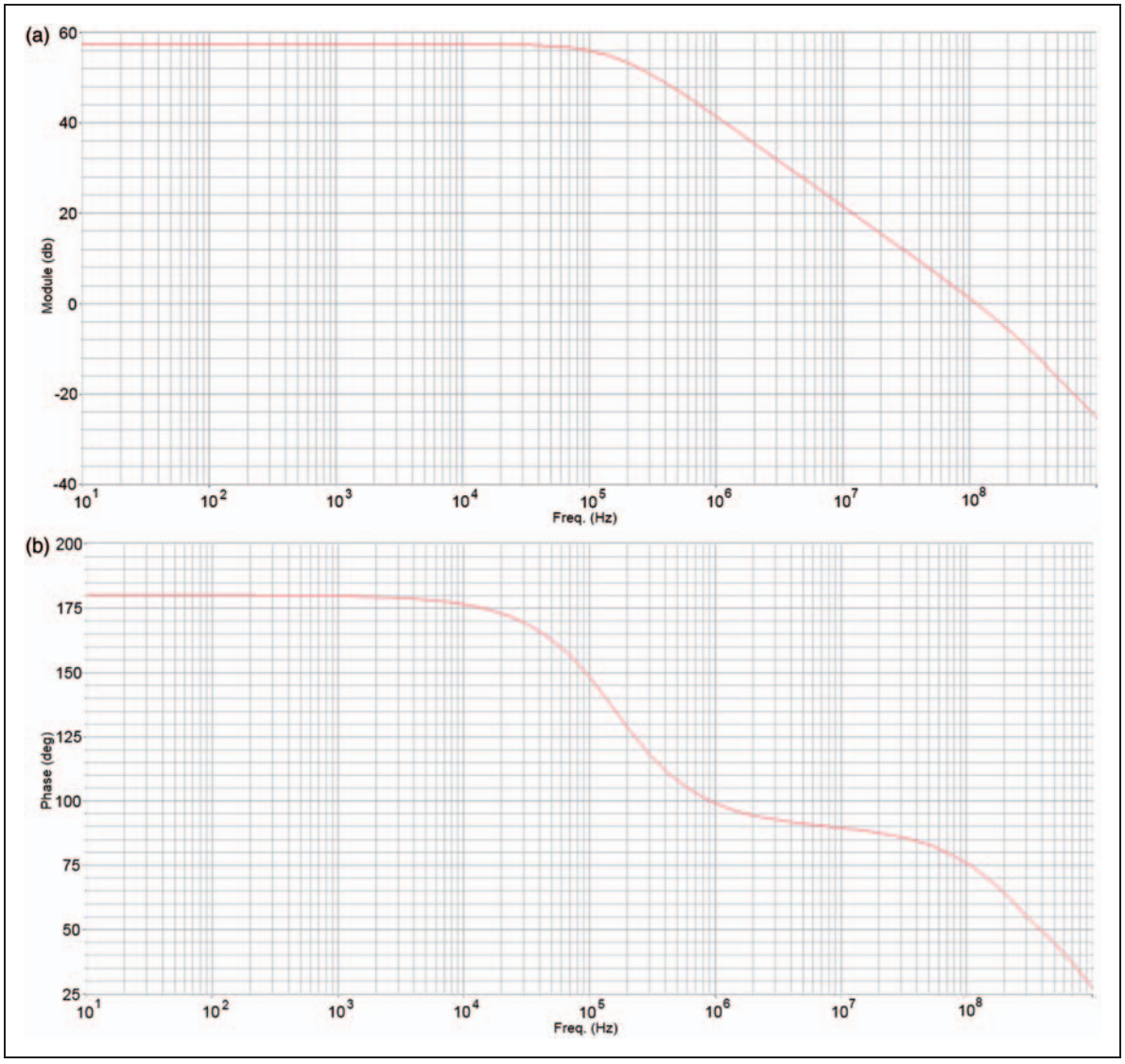

Figure 9. Gain-bandwidth performances of the folded cascade amplifier in module (a) and in phase (b).

In the next section all the structures developed in the switched capacitor technology realizing the fractional differ-integral operator are described.

3. Cadence environment implementation

The SC technique for designing filters is a recent development and is highly suitable for the realization of complete filters on a silicon chip. Switched capacitor filters, realized using metal oxide semiconductor (MOS) technology, use periodically operated switches with capacitors and operational amplifiers (OA). They are essentially based on active RC filter configurations, where the resistors are replaced through the use of switched capacitors.

The capacitors used in the switched capacitors technology, in order to obtain a fine accuracy, are realized between two layers of poly-silicon. With these capacitors the minimal dimensions which can be obtained are 20 * 20 μm^2 with values of capacities about $0.2 \div 0.3$ pF. The capacities of greater value are realized, connecting in parallel the capacities of the smaller value. This procedure allows there to be greater tolerances to inaccuracies.

The switches are realized using a parallel configuration of n-MOS and p-MOS in triode configuration in order to avoid the clock-feedthrough and to increase the dynamics of the signals (Caponetto et al., 2010).

Cadence is a design environment for full-custom analog, digital and mixed integrated circuits. In this work the technology used for the IC design is the 0.35 μm CMOS.

3.1. The fractional order PID

In order to realize the FO-PID, the structure presented in Figure 1 is implemented in Cadence environment, where the fractional order differ-integrator is realized according to the configuration shown in Figure 2 and explained in Table 1. According to the selection of the switches via the voltages from V1 to V11 it is possible to define any integrative or derivative order, included among –1 and 1; for the integrative and derivative actions of the FO-PID, see Figure 5.

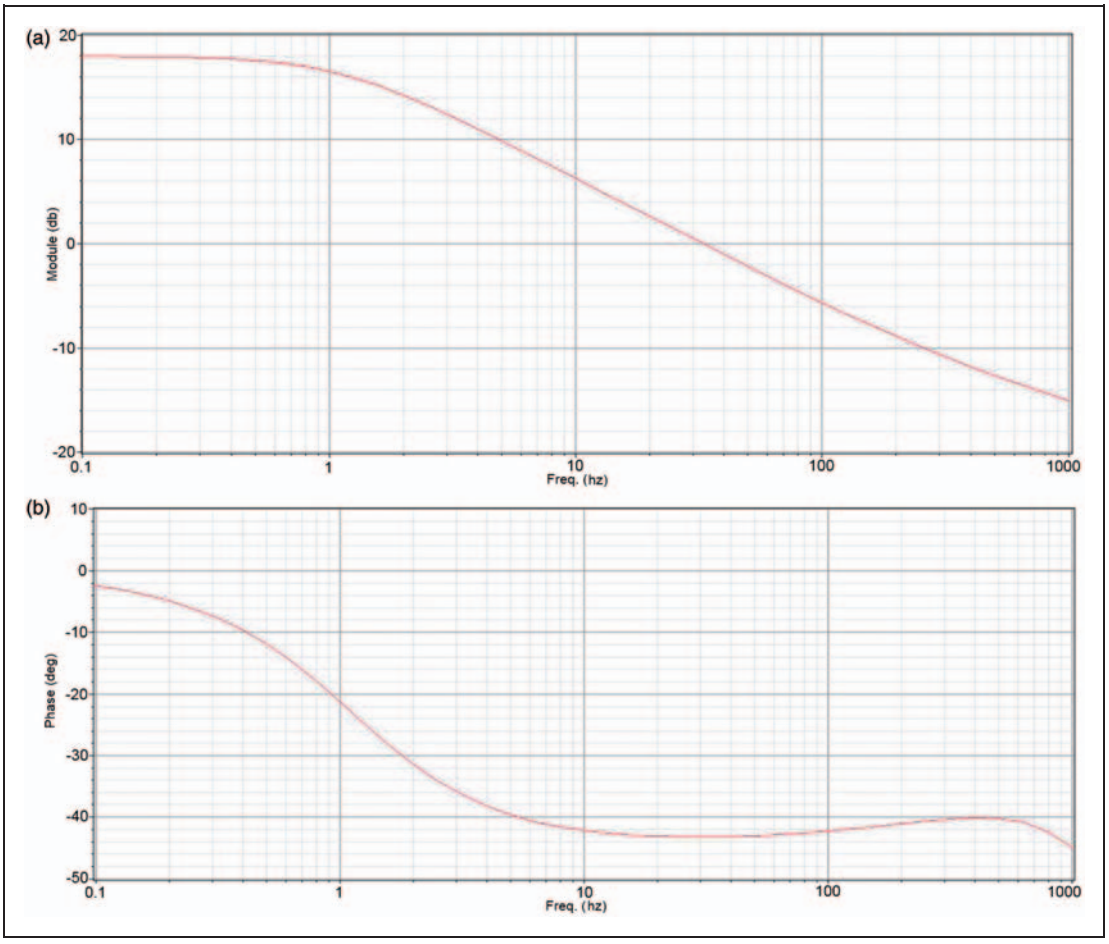

Figure 10. Module and phase Bode plots for the integrator of order 0.5.

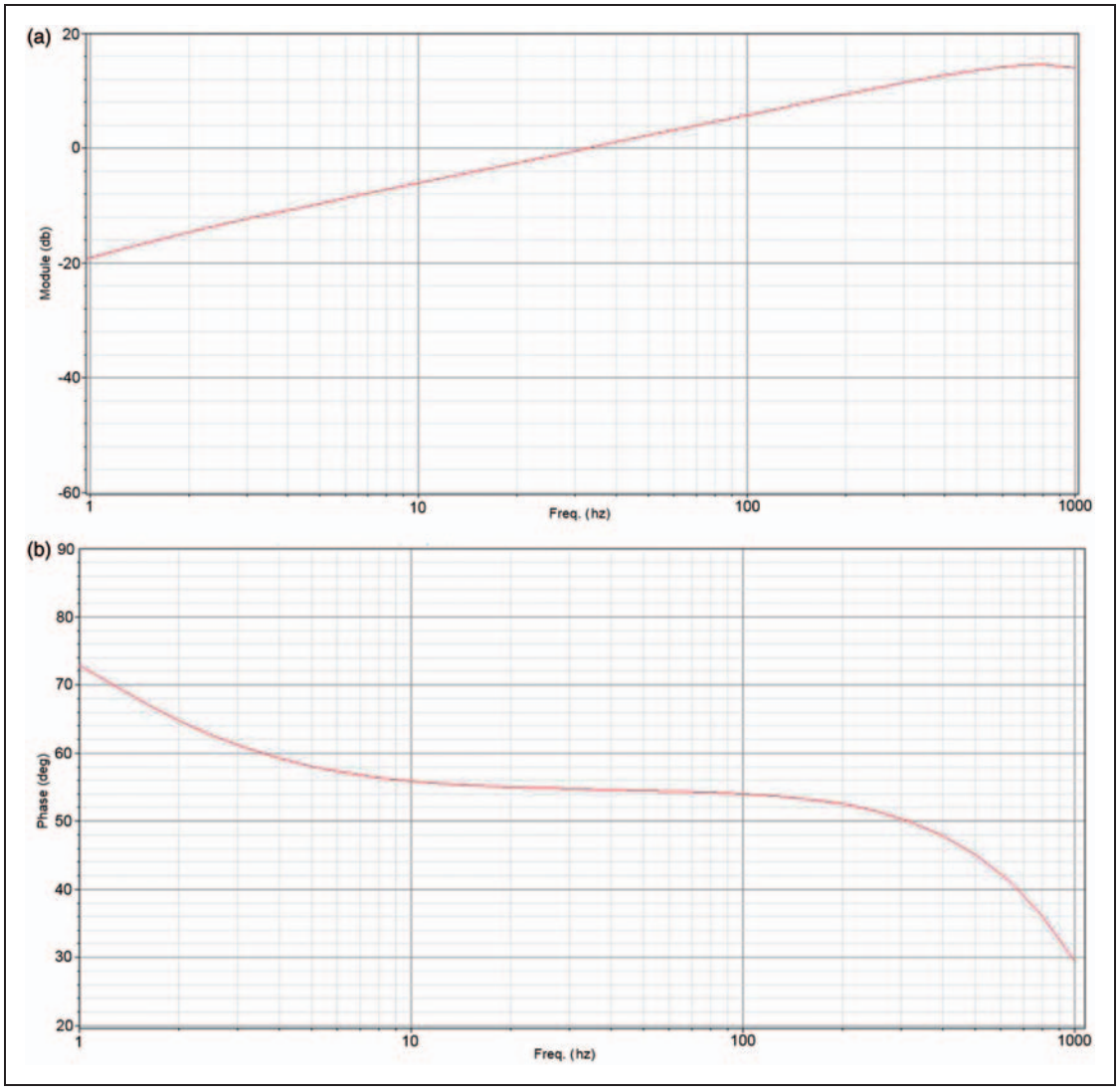

Figure 11. Module and phase Bode plots for the derivator of order 0.6.

In the pink rectangle the fractional order derivator of the FO-PID is outlined, in the yellow one the fractional order integrator, and in the blue one the adder block, realized in SC technology.

3.2. The fractional order integrator

The structure of the fractional order integrator is shown in Figure 6. Each feedback loop of the operational amplifier, made by a capacitor and an SCblock, whose structure realizes a resistance in SC technology, implements a zero-pole filter of the Oustaloup interpolation. Each singular fractional order integrator has the capacitive values determined by the Matlab algorithm, which take into account the influence of the non-idealities, in particular the phenomenon of warping.

3.3. The pole-zero block

In order to simplify the schematic circuit that has a large number of switches, a block named SCblock (Figure 7a) has been implemented realizing a resistor-type structure as the Euler behind and for which the timing that controls the switches and of course the switching capacitors must be specified. Therefore by using the Euler behind transformation the value of the SC according to the value of the implementing resistance is determined as $C = T/R$, where T is the switching time period.

3.4. Switches

The switch is realized with a transmission gate, achieved by using NMOS and PMOS transistors

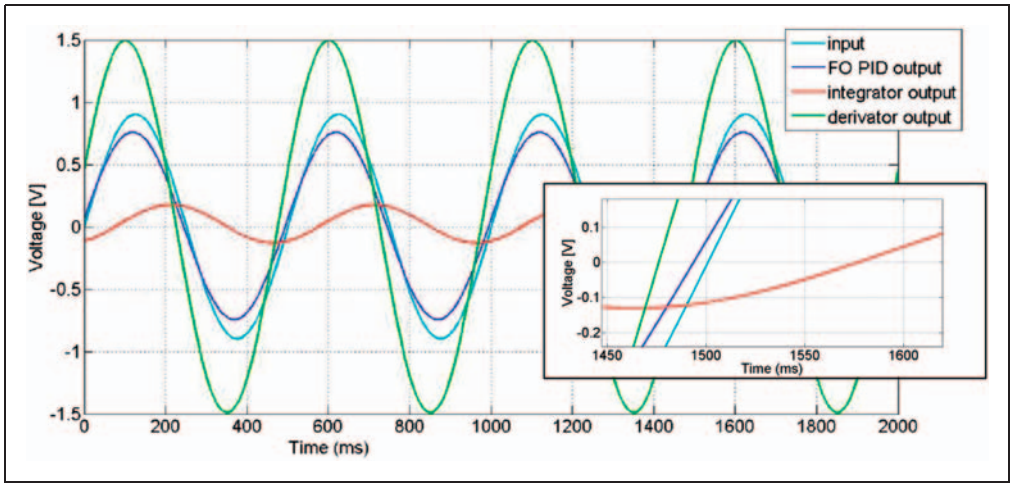

Figure 12. Timing plots for the fractional order proportional-integral-derivative ($K_p + K_i{*}s^{\lambda} + K_d{*}s^{\mu}$) with $\lambda = -0.7$, $\mu = 0.2$ and $K_p = 0.5$, $K_i = 0.2$, $K_d = 0.2$.

in parallel, see Figure 7b. The transistors are sized such that their form factor is $(W/L)_P = (W/L)_N = 5/0.35$.

3.5. The operational amplifier

An SC circuit needs an operational amplifier which has as its prerequisite an appropriate settling time, and also meets the natural stability specifications. The amplifier to be planned is a folded cascade amplifier, which allows the best gain-bandwidth performances with respect to an operational trans-conductance amplifier (OTA) with two gain stages (Giustolisi, 2007). The circuital schematic of the operational amplifier realized on Cadence is shown in Figure 8, while in Figure 9 its performance in module and in phase is shown.

In the bandwidth up to 100 Khz the folded cascade amplifier, implemented in Cadence environment, ensures good performance in module and phase, realizing a constant amplification in all the frequencies of the working bandwidth and no phase displacement (the phase value of 180 degrees is due to the inverting configuration).

4. Results

The hardware implementation of the FO-PID in the Cadence environment is compared with its ideal behavior calculated in the Matlab environment with the developed algorithm. Some results are shown in Figures 10 and 11, where the bode diagrams in module and phase, in particular, for a 0.5 order integrator and a 0.6 order derivative operator, are shown.

The Bode module diagram for the 0.5 order integrator, in the working bandwidth (10 hz ÷ 100 hz), decreases of *10 DB/decade*, while the phase is about constant at *–45* degree (see Figure 10). In Figure 11 the respective results for a 0.6 order derivative operator are shown. The Bode module diagram, in the working bandwidth (10 hz ÷ 100 hz), increases of *12 DB/decade*, while the phase is about constant at *54* degree (see Figure 11).

In Figure 12 the output of the FO-PID ($K_p + K_i{*}s^{\lambda} + K_d{*}s^{\mu}$) *with* $\lambda = -0.7$, $\mu = 0.2$ and $K_p = 0.5$, $K_i = 0.2$, $K_d = 0.2$, and the intermediate signals of the integrator of order 0.7 (output of the yellow block in Figure 5) and the one of the derivator of the order 0.2 (output of the pink block in Figure 5), within input a sinusoidal signal with amplitude equal to 0.9 V and frequency of 2 Hz, are shown. These signals can be compared with the results of the same FO-PID realized in the analog environment and presented in previous work (Caponetto and Dongola, 2008). Therefore they fit the literature results in amplitude and delay. In particular the amplitude of the integrator is attenuated of the factor $(2{*}\pi{*}f)^{0.7} = 5.88$ and delayed of $0.7{*}(T/4) = 87.5$ ms because the period T of the input sinusoidal signal is 500 ms. In the same way the amplitude of the derivator is amplified of the factor $(2{*}\pi{*}f)^{0.2} = 1{,}66$ and delayed of $0.2{*}(T/4) = 25$ ms because the period T of the input sinusoidal signal is 500 ms.

5. Conclusions

This paper has presented the feasibility study of an IC implementation of the FO-PID controller via switched capacitor technology. The realized approach is able to guarantee a good degree of approximation of the FO-PID and simultaneously propose a detailed analysis of the influence of the non-idealities, in particular the phenomenon of warping.

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References

Caponetto R and Dongola G (2008) Field programmable analog array implementation of non integer order $PI^{\lambda}D^{\mu}$ controller. *Journal of Computational and Nonlinear Dynamics* 3(2): 1–8.

Caponetto R, Dongola G and Fortuna L (2008) Switched capacitors implementation of fractional differ-integral operator. In: *3rd IFAC Workshop on Fractional Differentiation and its Applications, FDA 2008*, Ankara, Turkey, 5–7 November 2008.

Caponetto R, Dongola G, Fortuna L and Gallo A (2009) Non integer order operators implementation via switched capacitors technology. In: Baleanu D, Ziya Guvenc B and Tenreiro Machado JA (eds) *New Trends in Nanotechnology and Fractional Calculus Applications*. Netherlands: Springer, pp. 87–96.

Caponetto R, Dongola G, Gallo A and Giustolisi G (2010) Fractional order differ-integral operator in integrated technology. In: *4th IFAC Workshop on Fractional Differentiation and Its Applications, FDA 2010*, University of Extremadura, Badajoz, Spain, 18–20 October 2010.

Dorcak L, Feliu V, Podlubny I and Vinagre BM (2000) On fractional PID controllers: a frequency domain approach. In: *IFAC Workshop on Digital Control. Past, Present and Future of PID Control*, Terrasa, Spain, 4–7 April 2000, pp. 53–58.

Giustolisi G (2007) Two-stage OTA design based on settling time constraints. *Circuits and Systems, ISCAS Symposium*. New Orleans, USA20–27 May 2007, pp. 469–472.

Oustaloup A (1981) Fractional order sinusoidal oscillators: optimization and their use in highly linear FM modulation. *IEEE Transactions on Circuits and Systems* 28(10): 1007–1009.

Oustaloup A (1983) *Systemes asservis lineares d'ordre fractionnaire*. Paris: Masson.

Oustaloup A, Levron F, Mathieu B and Nanot F (2000) Frequency-band complex non integer differentiator: characterization and synthesis. *IEEE Transactions on Circuits and Systems* 47(1): 25–40.

Podlubny I (1999) Fractional order systems and $PI^{\lambda}D^{\mu}$ controller. *IEEE Transactions on Automatic Control* 44(2): 208–214.