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Dual push-pull high-speed rail-to-rail CMOS buffer amplifier for flat-panel displays

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***Abstract*— This paper presents the experimental validation of a low-power, large output swing, class-AB buffer amplifier for column drivers of active-matrix flat-panel displays. By exploiting two complementary input amplifiers and a dual-path push–pull output stage the proposed circuit achieves high-drive performance and rail-to-rail operation. In addition, two current boosters allow area optimization of the output diving transistors by dynamically lowering their threshold voltage. Implemented in a standard triple-well CMOS 0.35-μm technology and supplied from a 3-V supply, the proposed buffer amplifier can drive a 1-nF column line load within a 1.11-μs settling time under a full voltage swing, while drawing only 1.6 μA quiescent current and occupying 5562 μm² of silicon area. As compared to the state of the art, the best Figure of Merit (pF/μs·μA) is found.**

***Index Terms*— liquid crystal display, buffer amplifier, class AB, column drivers, rail-to-rail, settling time.**

I. Introduction

Column drivers of active matrix liquid-crystal displays (LCDs) have a crucial role in the performance of the whole display since they deliver the pixel information [1]. One of the key building blocks a column driver is the output buffer amplifier, which mainly determines the resolution, speed and power consumption of the entire system [2]-[19]. In conventional applications, thousands of output buffers are built on a single chip [1] and consequently, the buffer must occupy a reduced die area and consume low static current to minimize the overall cost of the driver and prolong battery life in portable applications. Moreover, the buffer must drive a column capacitance ranging from 10 pF to 1000 pF and must settle within a horizontal scanning time imposed by the frame frequency [1], [9]-[12], [15]-[17]. Finally, the amplifier should offer a rail-to-rail input/output to arrange a high number of grey levels [7]-[12], [14]-[17]. To fulfill these specifications, in recent years many solutions have been reported in the literature [2]-[18].

With the aim of further enriching the state of the art, in this paper a class-AB buffer amplifier with very low settling time and quiescent current is presented. The proposed buffer amplifier, based on the solution presented by Wang et al. in [9] and by the authors [12], is made up of a rail-to-rail input stage and a dual-path push-pull output stage, with both class-B and class-AB output sections combined together. Compared to the original solution, the main improvement is here represented by the adoption of an auxiliary stage, firstly proposed in [19], that provides dynamic body biasing to the class B section, dynamically decreasing the threshold voltage of the output transistors and thereby offering a way to substantially increase speed and driving capability while reducing the area required by the output devices. The body bias stage in [20] is particularly suited for the considered application. Indeed, output transistors of a buffer amplifier designed for flat-panel displays usually have large aspect ratios. The adoption of the auxiliary stage in [20], also referred in the following as "current booster", thanks to the significant reduction of the output transistor aspect ratio allows to heavily reduce the active area of the amplifier, while providing the same or even higher output current. Finally, it is worth noting that for the first time the solution in [19] and the core topology in [12] are experimentally validated on fabricated prototypes.

The paper is organized as follows. The proposed solution is analyzed in Section I. Section II reports the design simulation results. Section III presents the test results and the comparison with the state of the art. Finally, a conclusion is given in Section IV.

II. Circuit description

The schematic diagram of the proposed solution is shown in Fig. 1. It consists of a rail-to-rail input stage made up of two complementary source coupled pairs, M1-M2 (n-channel pair) and M3-M4 (p-channel pair), with tail current generators MB6 and MB5, respectively, and multi-mirrored active load M5-M12. This input stage is designed using unitary current mirrors to maintain simplicity and minimize mismatches. Diode-connected transistors in the output branch of this stage, MB7-MB8, are exploited to bias the gates of the first layer of output transistors MN2-MP1 providing class-AB output behavior. As shown in [12], the DC current of MN2 and MP1 is expressed by

$$I_{DC} = \frac{K_n K_p (W/L)_{MN2}(W/L)_{MP1}}{\left[\sqrt{K_n (W/L)_{MN2}} + \sqrt{K_p (W/L)_{MP1}}\right]^2} \left(V_{DD} - V_{THn} - |V_{THp}| - V_{GSMB8} - |V_{GSMB7}|\right)^2 \quad (1)$$

This class AB section determines the overall quiescent power dissipation of the output stage, as well as the frequency response and small signal linearity of the buffer amplifier. Operating in class-AB, the current delivered by transistors MN2 and MP1 can increase under large signal excitation, but

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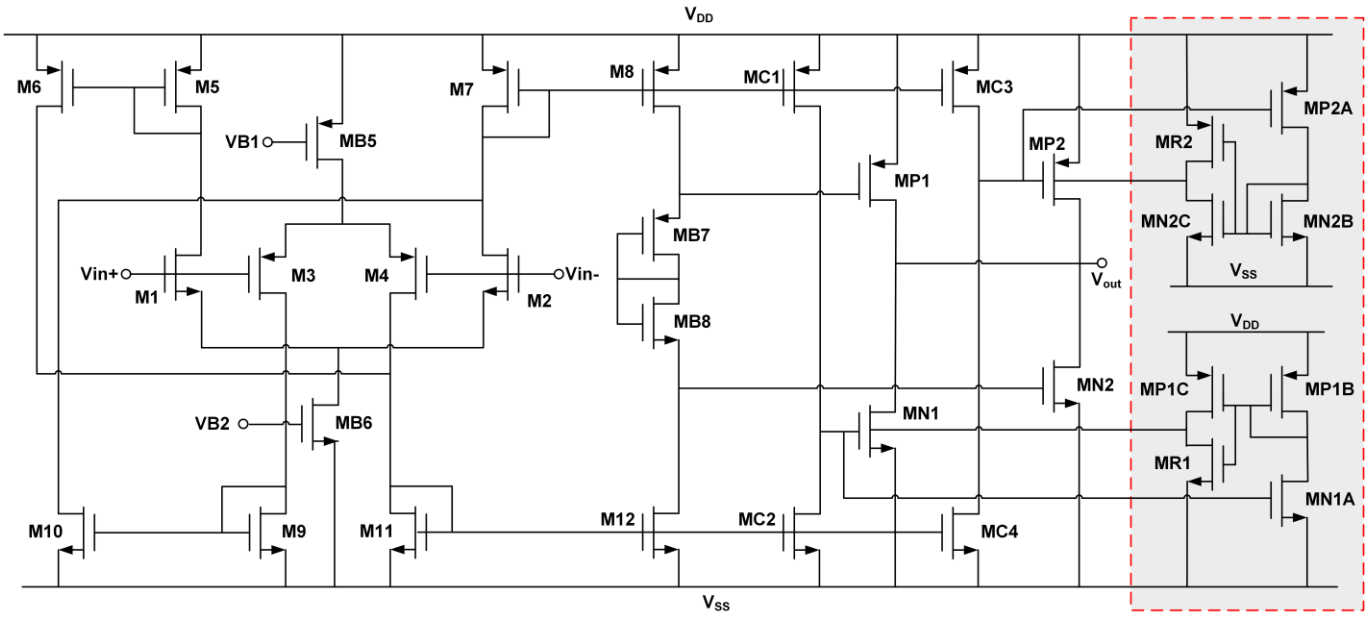

Fig. 1. Circuit schematic of the proposed buffer amplifier.

it is not sufficient to drive loads up to 1 nF without requiring very large active areas of the same transistors. At this purpose, in addition to this first output stage, a parallel class-B output section is included. It is made up of two current comparators, MC1-MC2 and MC3-MC4, and two push-pull driving devices, MN1 and MP2, which are both OFF in their quiescent state. To ensure this, the quiescent drain currents of MC1 and MC4 are designed to be slightly lower than the nominal drain currents of MC2 and MC3, respectively. The above specification is fulfilled under the following design conditions

$$\frac{(W/L)_{MC1}}{(W/L)_7} = \frac{(W/L)_{MC2} - \Delta(W/L)}{(W/L)_{11}} \tag{2a}$$

$$\frac{(W/L)_{MC4}}{(W/L)_{11}} = \frac{(W/L)_{MC3} - \Delta(W/L)}{(W/L)_7} \tag{2b}$$

As a result, this circuit section operates with no quiescent current dissipation and thus provides class-B behavior. Indeed, when a negative (positive) voltage step is applied to the input node V_{in+}, the drain currents in M1 and M2 (M3 and M4) will be respectively increased and decreased, causing the drain currents of MC1 (MC4) to raise accordingly. If the input step amplitude ΔV is greater than the equivalent offset voltage V_{offset} at the input of the current comparators, then the drain voltage of MC1 (MP2) will increase (reduce) to switch-ON MN1 (MP2). Since the gate-source voltage of MN1 (MP2) can reach the value of V_{DD} (V_{SS}), its drain current, I_{SRn} (I_{SRp}), represents the major contribution to the negative (positive) amplifier slew rates, which are thus now expressed by

$$SR^- = \left.\frac{dV_{HL}(t)}{dt}\right|_0 \approx \frac{I_{SRn}}{C_L}\ ,\ \Delta V > V_{offset} \tag{3a}$$

$$SR^+ = \left.\frac{dV_{LH}(t)}{dt}\right|_0 \approx \frac{I_{SRp}}{C_L}\ ,\ |\Delta V| > V_{offset} \tag{3b}$$

With the aim of increasing I_{SRn} (I_{SRp}) while optimizing area occupation, this dual path class-AB/B output stage is modified by including two current boosters [20], whose schematic diagram is highlighted within dashed box in Fig. 1. The principle of operation of the current boosters is to forward bias in a dynamic way the source-to-bulk junctions of MN1 and MP2, leading to a reduced threshold voltage and, in turn, to a higher overdrive without increasing their aspect ratios. The adoption of theses current boosters allows to increase driving capability with a marginal increase of circuit complexity. Consequently, high-speed driving capabilities can be achieved during the limited amplifier transient operation.

It is to be noted that an exclusive class-B output stage cannot be used in LCD buffer applications because, as long as $\Delta V < V_{offset}$, the output driving devices MN1 and MP2 remain in their cut-off region. This adversely affects the buffer large-signal performance with consequent settling time degradation. Furthermore, and perhaps most crucially, small grey steps cannot be correctly processed by the output buffer, as a minimum current mismatch must be guaranteed against process parameter variations to ensure the output transistors to be statically OFF. Therefore, the class-AB section, being adequate to drive limited ΔV values is essential to solve the above class-B inherent drawback.

Regarding closed-loop stability, due to the very large capacitive loads, no additional Miller capacitor is required to achieve frequency compensation, as the loop-gain dominant pole is located at the output node.

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III. Simulation Results

The circuit depicted in Fig. 1 is implemented using the BCD6 technology, provided by STMicroelectronics, whose CMOS transistors have a minimum channel length of 0.35 μm. Following the design guidelines reported in the previous Section, transistor dimensions are set as summarized in Table I. Due the class B operation of the output buffer, the quiescent current can be set small without degradation of the settling behavior. Indeed, the overall quiescent current of the complementary input differential stage, the push-pull devices MP1 and MN2, the current boosters and the biasing network is only 1.6 μA from 3-V power supply.

The robustness of the proposed solution against process and temperature variations is investigated using post-layout corner simulations at -10°C, 27°C and 85°C. The results are summarized in Table II for a loading capacitance, C_L, equal to 1 nF. Finally, a 10-% variation on the supply voltage has been considered and no significant impact on the overall performance was observed.

TABLE I
TRANSISTOR DIMENSIONS

Transistor	Dimension
M_{B5}, M_{B6}	1x(1.0/1.4)
M_{B7}, M_{B8}	2x(0.5/0.5)
M_1, M_2, M_{R1}, M_{R2}, M_{N2B}, M_{P1B}	1x(0.5/0.35)
M_3, M_4, M_{P2A}, M_{N1A},	1x(1.0/0.35)
M_5, M_6, M_7, M_8, M_9, M_{10}, M_{11}, M_{12}, M_{C2}, M_{C3}	1x(0.6/0.7)
M_{C1}, M_{C4}	1x(0.5/0.7)
M_{P1}	2x(1.0/0.5)
M_{N2}	1x(1.0/0.5)
M_{P2}	60x(1.0/0.35)
M_{N1}	30x(1.0/0.35)
M_{N2C}, M_{P1C}	3x(0.5/0.35)

TABLE II
CORNER SIMULATION RESULTS AT DIFFERENT TEMPERATURES (C_L=1 nF)

T=-10°C

Corner	TT	FF	SS	SF	FS
Idd (μA)	1.497	2.734	1.411	1.481	1.516
DC Gain (dB)	91.34	88.87	58.3	89.95	91.71
PM (degrees)	77.35	36.38	89.82	79.34	73.12
SR (V/μs)	5.947	6.717	5.328	6.507	5.464
1% Ts (μs)	1.157	1.051	1.296	1.095	1.235

T=27°C

Corner	TT	FF	SS	SF	FS
Idd (μA)	1.623	3.477	1.408	1.566	1.679
DC Gain (dB)	92.39	89.58	77.88	92.3	91.91
PM (degrees)	53.71	34.3	88.12	59.57	50.32
SR (V/μs)	5.665	6.49	5.096	6.244	5.254
1% Ts (μs)	1.201	1.083	1.363	1.126	1.298

T=85°C

Corner	TT	FF	SS	SF	FS
Idd (μA)	2.17	5.366	1.453	2.018	2.297
DC Gain (dB)	91.46	88.04	92.06	91.58	90.81
PM (degrees)	33.47	29.37	71.0	35.83	32.38
SR (V/μs)	5.372	6.122	4.816	5.934	4.952
1% Ts (μs)	1.271	1.14	1.454	1.184	1.387

It is worth noting that due to the adoption of the current boosters, the active area of the buffer amplifier is 28% lower than the solution reported in [12] which adopts a similar core topology in a technology with the same minimum channel length, but does not entail current boosters (active area of the proposed solution is 46.13 μm^2 whereas the active area in [12] is 65.38 μm^2).

IV. Experimental Results and Comparison

The microphotograph of the fabricated buffer amplifier is shown in Fig. 2. The tracking behavior of the proposed buffer amplifier is verified in Fig. 3, where the response to a 50-kHz full-swing (3 Vpp) input triangular wave. with C_L=1 nF. is reported. As can be inspected, the output voltage basically follows the input voltage for a rail-to-rail input range. Fig. 4 shows the measured transient response to a 50-kHz full-swing input step under a large-size capacitive load of 1 nF. Slew-rate values are found to be 6.5 V/μs and 8.1 V/μs for the rising and falling edges, respectively, whereas positive and negative settling time values within 1% of the final output voltage are 1.20 μs and 1.02 μs, respectively. Finally, the measured open-loop frequency response with C_L=1 nF is reported in Fig. 5.

Table III summarizes the measured performance parameters.

TABLE III
MEASURED PERFORMANCE PARAMETERS (V_{DD}=3V)

Parameter	Value
Supply voltage (V)	3
Total quiescent current (μA)	1.63
Pos./Neg. settling time 1% (μs)	1.20/1.02
Pos./Neg. Slew rate (V/μs)	6.5/8.1
Unity-gain bandwidth (kHz)	190
Phase margin (°)	53

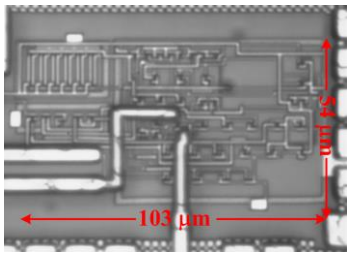

Fig. 2. Chip microphotograph.

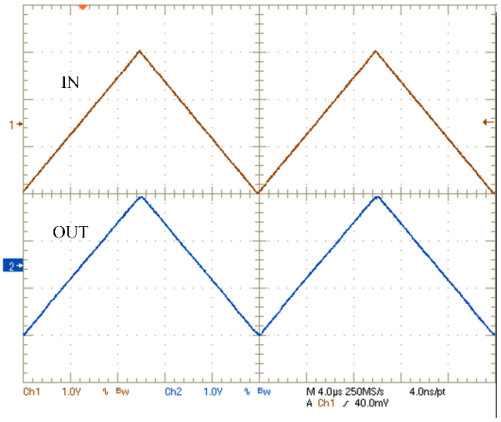

Fig. 3. Measured amplifier transient response to a 50-kHz full-swing input triangular wave.

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TABLE IV
COMPARISON WITH PRIOR ART

	[3]	[4]	[8]	[9]	[10][a]	[11][a]	[12][a]	[13]	[14][a]	[15]	[16]	[17][a]	[18]	**This work**
Year	2002	2002	2006	2007	2010	2010	2010	2011	2011	2011	2014	2015	2015	**2017**
CMOS tech. (μm)	0.6	0.35	0.35	0.35	0.35	0.6	0.35	0.35	0.35	0.35	0.6	0.35	0.13	**0.35**
Operation class	AB	B	B	AB	AB	B	AB	B	AB	B	AB	B	AB	**AB**
Supply voltage (V)	5	3.3	3.3	3.3	3	3	3	3.3	3.3	3.3	5	3.3	0.7	**3**
Load capacitor (pF)	680	600	600	1000	1000	1000	1000	600	600	1200	1000	1000	30000	**1000**
Quiescent current (μA)	30	7.4	5.4	7.7	8	3.5	3.5	5	3	3	32	1.6	24	**1.63**
Settling time (μs)	1.3	8	1.5	1.28	0.8	1.7	0.9	1.5	0.85	1.78	0.71	1.45	2.61	**1.11**
In/Out range (%VDD)	77	97	100	100	100	100	100	97	100	100	100	100	--	**100**
Die area (μm^2)	na	6321	2528.59	2115	625	915	874.5	2940	2160	6588	6643	1380	2725	**5562**
FOM (pF/μs·μA)	17.4	10.1	74.1	101.5	156.3	168.1	317.5	80.0	235.3	224.7	44.0	431.0	479	**553.4**

[a] simulation results

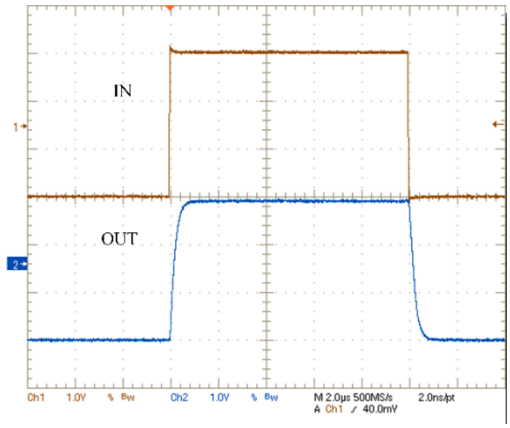

Fig. 4. Measured amplifier transient response to a 50-kHz full-swing input step.

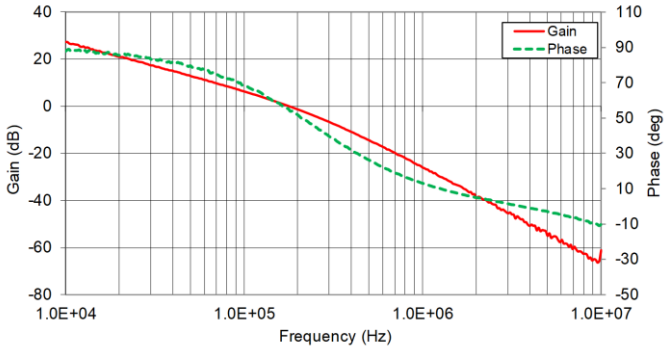

Fig. 5. Measured amplifier loop gain with C_L=1 nF, unity gain bandwidth is 190kHz with phase margin of 53°.

A performance comparison with previously reported LCD output buffers is reported in Table IV. It is apparent that the proposed solution achieves the lowest power consumption. It is comparable only to [17] which, however, is a class B topology. To further demonstrate the effectiveness of the present output buffer, the figure of merit

$$FOM = \frac{C_L}{T_S \cdot I_{DD}} \quad (4)$$

is used, where C_L is the load capacitance of the column lines, T_S is the average settling time and I_{DD} the total quiescent current. It is apparent that the proposed solution achieves the best performance. Again, only [17] and [18] achieve a fairly near FOM value. However, [17] was not experimentally tested while solution reported in [18] is a high-gain general-purpose amplifier designed to drive extremely high capacitive loads, in the range of 10 nF-30 nF. This latter feature mainly determines the increase of the FOM value. Moreover, operation of [18] is not rail-to rail due to the adoption of a simple nMOS differential pair at the input.

V. CONCLUSION

In this paper, a very-low static power rail-to-rail buffer amplifier for active-matrix LCD column drivers is proposed. By adopting a complementary input pair and a class-B output stage, the proposed circuit achieves rail-to-rail operation and a high driving capability. The size of the transistors of the output stage is minimized by adopting an auxiliary circuit that dynamically adapts their threshold voltage and was for the first time used in a real application and experimentally tested. The buffer is implemented in a 0.35-μm triple-well CMOS technology. Experimental measurements show a significant performance improvement as compared to all the other recently proposed solutions.

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