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A Fully-Integrated Watt-Level Power Transfer System with On-Chip Galvanic Isolation in Silicon Technology

Vincenzo Fiore, Egidio Ragonese, *Senior Member, IEEE*, and Giuseppe Palmisano, *Senior Member, IEEE*

***Abstract*— This work presents the design and experimental characterization of a power transfer system performing a dc-dc conversion with on-chip galvanic isolation. The converter is operated in the VHF band, which enables fully integration of all the required components in silicon technology. It consists of only two silicon dice, i.e. a power oscillator with an on-chip isolation transformer and a full-bridge rectifier, which are fabricated in 0.35-µm BCD and 0.13-µm CMOS technology, respectively. A thick SiO2 layer was used, which guarantees galvanic isolation between the transformer windings. A co-design procedure for the system building blocks is proposed, which aims at optimizing the dc-dc converter performance in terms of power efficiency at a given power density. Thanks to the adopted approach, a maximum output power up to 980 mW is demonstrated with a power efficiency of 29.6%. This work outperforms previously reported integrated inductive step up converters in terms of power per silicon area (up to 105 mW/mm^2), while providing on-chip galvanic isolation without any discrete devices or post processing steps.**

***Index Terms*— Full-bridge rectifier, galvanic isolation, integrated transformer, LDMOS, lumped scalable modeling, power oscillator, Schottky diodes, silicon technology.**

I. Introduction

Galvanic isolation is becoming increasingly important in a wide field of applications, whenever high-power equipment is operated by human beings or to guarantee better reliability in harsh industrial environments. However, there are lots of applications where galvanic isolation is also required for relatively low power levels. This is the case for serial link transceivers, sensor interfaces, low-power medical devices, and housekeeping power, such as gate-drivers or controllers for power converters. For these applications, a general block diagram is depicted in Fig. 1. Two domains, *A* and *B*, are galvanically isolated since one of them is subject to hazardous voltages and/or requires a different ground reference. Data signals are transferred across the galvanic isolation barrier to enable bidirectional communication between the two domains, while an isolated power supply for domain *B* is provided from domain *A* by a power transfer technique. For low-power applications, isolated power levels between 100 mW and 1 W

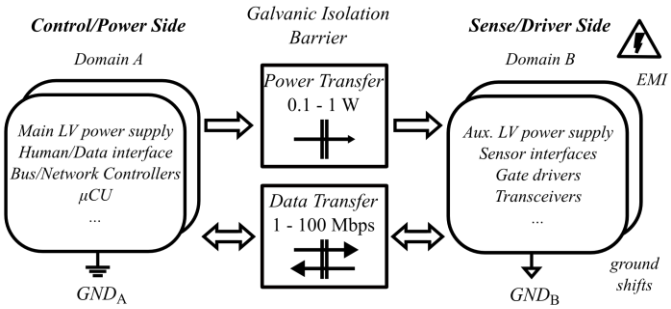

Fig. 1. Block diagram of a galvanically isolated system.

are required. Traditionally, optocouplers and discrete transformers are used for galvanic isolation, but they are bulky and expensive. In recent years, different solutions have been proposed for galvanic-isolated silicon-integrated data transmission using RF links [1], capacitive coupling [2], or integrated coreless transformers [3]-[5]. As far as power transfer is concerned, many implementations have been addressed to the reduction of size in galvanically isolated systems by exploiting smaller HF/VHF discrete transformers [6], [7] either on-board or with system-in-package (SiP) approaches. However, the complexity of these solutions is not compatible with large-scale and low-cost production. At present, the most advanced approach for a galvanically isolated power supply exploits post-processed micro-transformers with Au thick metals and a 20-µm polyimide layer [8], [9], thus requiring three dice to implement the overall dc-dc converter.

This paper presents a highly integrated watt-level power transfer system performing a dc-dc power conversion and providing on-chip galvanic isolation. Differently from previous works, this system does not require post-processing steps or external components and is fully integrated on silicon, since it relies on a standard silicon technology with a thick SiO_2 layer for isolation. Only two dice are used and hence the highest level of integration is achieved for a silicon technology with a standard substrate. The paper proposes a co-design procedure for the system building blocks to achieve the highest power efficiency for given power and silicon area constraints, thus maximizing the performance of this integrated approach.

The paper is organized as follows. Section II describes the architecture of the dc-dc converter. The co-design procedure is presented in Section III. Experimental characterization of the dc-dc converter along with a comparison with the state-of-the-art is carried out in Section IV. Finally, main conclusions are drawn in Section V.

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V. Fiore was with the DIEEI, Università di Catania, Catania I-95125, Italy. He is now with DICE GmbH & Co KG, Linz, A-4040, Austria (e-mail: vincenzo.fiore@infineon.com).

G. Palmisano is with DIEEI, Università di Catania, Catania, I-95125, Italy. (e-mail: giuseppe.palmisano@dieei.unict.it).

E. Ragonese is with STMicroelectronics, Catania, I-95121, Italy (email: egidio.ragonese@st.com).

IEEE Trans. on Power Electronics, vol. 32, no. 3, pp. 1984-1995, March 2017. DOI: 10.1109/TPEL.2016.2556939

II. System Description

The architecture of the proposed galvanically isolated dc-dc converter is depicted in Fig. 2. It includes a transformer-based power oscillator and a full-bridge rectifier, which perform dc-ac and ac-dc conversion, respectively. The core of the system is the integrated transformer, $T_{ISO,}$ which provides on-chip galvanic isolation. It is integrated into the oscillator chip, whereas the second die houses the rectifier. The converter was designed to produce around 1 W with a 20-V output voltage (V_{OUT}) from a 5-V power supply (V_{DD}) to address gate driver applications. Voltage multiplication is achieved by exploiting the turns' ratio of the transformer.

The power oscillator chip was fabricated in a 0.35-µm BCD technology, which provides a galvanic isolation rating as high as 5 kV by means of a thick oxide layer between the top metal layers. The galvanic isolation performance was previously assessed by the technology provider using several transformer test structures [5], [10]. This technology also features LDMOS power devices [11]. The rectifier chip was instead fabricated in a 0.13-µm standard CMOS process, by taking advantage of the available high-voltage Schottky diode with high-frequency operation capability. The whole technology platform was supplied by STMicroelectronics.

The power oscillator adopts a transformer-loaded cross-coupled topology as shown in Fig. 2, which is operated in class D to improve power efficiency. RF class-D oscillators have recently gained attention in highly scaled technologies, for design approaches mainly focused on low power applications [12], [13]. However, the design for power transfer applications with galvanic isolation is quite a different issue due to the low *Q*-factor of the resonating tank and the levels of power involved. LDMOS transistors are used for $M_{1,2}$ to take advantage of their high-frequency and high-voltage/current capability. Since the maximum allowable gate-source voltage, V_{GS_MAX}, is smaller than the maximum drain-gate voltage V_{DG_MAX}, a capacitive coupling through C_B is used to avoid gate-oxide breakdown. Indeed, capacitors C_B perform a voltage partition with the gate capacitance of $M_{1,2}$, which sets the peak of V_{GS}. The transformer is here represented as coupled inductors, $L_{P1,2}$ and $L_{S1,2}$, which are the primary and secondary coils, respectively. It is worth noting that $L_{P1,2}$ resonates with the large parasitic capacitance at the transistor drains. Avoiding an additional tank capacitor maximizes inductance values and thus transformer efficiency. The circuit requires a control loop, which stabilizes the output voltage for a given load power being the output current imposed by the load itself. In this first implementation the control circuit was not included since the design effort was focused on the power link that mainly sets the overall circuit performance such as load power, power efficiency, and silicon area. However, a turn-off circuitry was included that is driven by control terminal V_{CTR} and allows the cross-coupled pair to be on/off switched. This terminal is used to externally vary the output power of the dc-dc converter by feeding a PWM signal, thus demonstrating that different output power levels can be obtained without losing efficiency, as required when performing the control. Finally, traditional approaches can be used for the control circuit [7], [8].

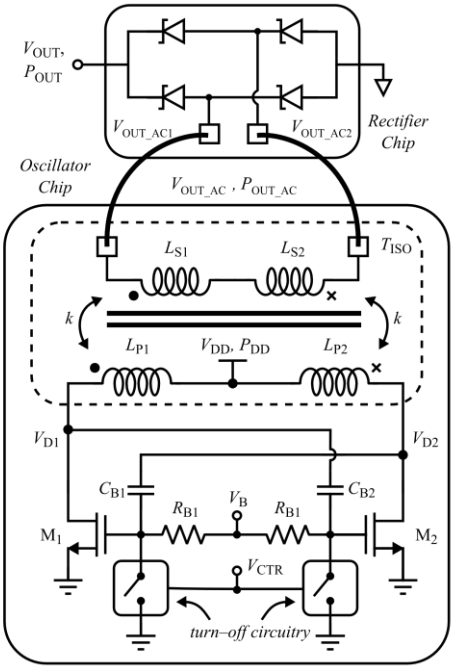

Fig. 2. Architecture of the proposed galvanically isolated dc-dc converter.

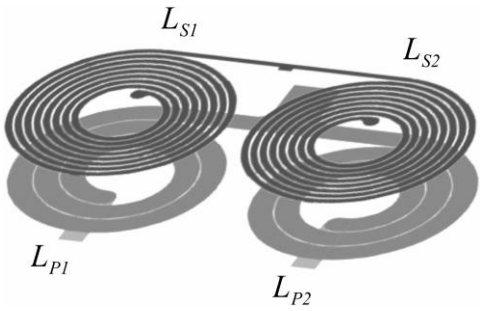

Fig. 3. 3-D view of the isolation transformer, T_{ISO}.

A stacked configuration is used for the transformer, which exploits standard metal 3 and metal 4 for the primary and secondary windings, respectively and the lowest two metals for underpasses, as shown in Fig. 3. Despite the differential topology adopted for the oscillator, a fully symmetric spiral configuration is not a viable solution for the primary coil due to the higher number of underpasses required by a multiturn geometry [14]. Two stacked transformers are instead adopted, thus requiring only two underpasses. The coupling effects between right and left sides are negligible for a distance greater than 70 µm [15]. A high coupling factor, *k*, is mandatory for the transformer since a low one along with the low *Q*-factor would greatly affect power transfer efficiency. Maximizing the overlap area between the primary and secondary windings is therefore crucial to avoid *k*-factor degradation [16]. Since a high transformer turns' ratio must be used to step-up the output voltage, both primary and secondary geometrical parameters must be properly designed to maximize the winding overlap. On the secondary side, two bonding wires are used for the connection towards the rectifier chip. The impact of these bonding wires on system performance is negligible since they are connected in series with the high inductance of $L_{S1,2}$.

IEEE Trans. on Power Electronics, vol. 32, no. 3, pp. 1984-1995, March 2017. DOI: 10.1109/TPEL.2016.2556939

III. System Co–Design

The design of the dc-dc converter poses several challenges since non-linear interactions exist between each building stage involving system optimization. For an intuitive understanding of the main design tradeoffs, the simple circuits shown in Fig. 4 can be used. Specifically, the model in Fig. 4(a), where the rectifier is represented by its equivalent input impedance (R_{RECT} and C_{RECT}), is further simplified with the model in Fig. 4(b). Here, the resonant tank of the oscillator is represented by a lumped RLC network that accounts for both transformer and rectifier loading effects. In particular, inductance L_{EQ} is the equivalent inductive component at the primary side of the transformer, resistance R_P and capacitance C_P account for the transformer loss and parasitic capacitance, resistance R_L and capacitance C_L take into account the reflected rectifier impedance. Finally, capacitor C_C models the equivalent parasitic capacitance of the oscillator core, mainly due to the LDMOS pair. Maximizing power transfer efficiency requires transformer loss resistance R_P to be much higher than reflected rectifier resistance R_L. Unfortunately, since R_P is equal to $\omega \cdot Q_P \cdot L_{EQ}$, high values of R_P are usually achieved by increasing both oscillation frequency and equivalent inductance, which in turn need smaller transistor sizes. On the other hand, the improvement in oscillator active core and rectifier efficiencies needs larger transistors $M_{1,2}$ and rectifier diodes, which increases their parasitic capacitances (i.e., C_C, and C_L), thus reducing oscillation frequency and hence R_P. For example, the adopted LDMOS transistors show small signal gate and drain capacitance around 2 pF/mm and 2.3 pF/mm, whereas their on resistance is around 4.2 Ω × mm. Moreover, larger diodes and hence better rectifier efficiency also means higher R_L, thus requiring an even higher R_P. These simple considerations highlight the strong interactions between the performance of active and passive stages and confirm that no significant result can be achieved by designing each system block as a stand-alone circuit. Optimum performance can then be obtained by adopting an iterative co-design procedure between the converter building blocks.

One of the most important design specifications for an integrated dc-dc converter is its power density, i.e. the ratio of delivered output power to overall silicon area occupation, which is a key figure of merit for fully integrated converters [17]-[19]. The main purpose of the proposed design procedure is to optimize the dc-ac conversion efficiency at a given power density, which means optimum co-design between power transistors and isolation transformer in the oscillator. The starting point was the design of the rectifier, since it defines the equivalent load of the transformer at the secondary coil and sets the upper bound for the oscillation frequency. Then, a lumped geometrically scalable model of the transformer was developed, thus enabling parametric circuit simulations to efficiently explore the design space. By taking advantage of this model, several designs for the whole dc-dc converter were carried out, which were refined by iterating the design procedure. Since optimal operating conditions for the transformer and the active circuitry are contrasting, the iterative procedure may sometimes produce design solutions, which do not comply with target specifications, as will be shown. Finally, starting from the best solution, the system design was completed for integration by taking into account main on-chip and off-chip parasitic effects through an extensive electromagnetic (EM) analysis.

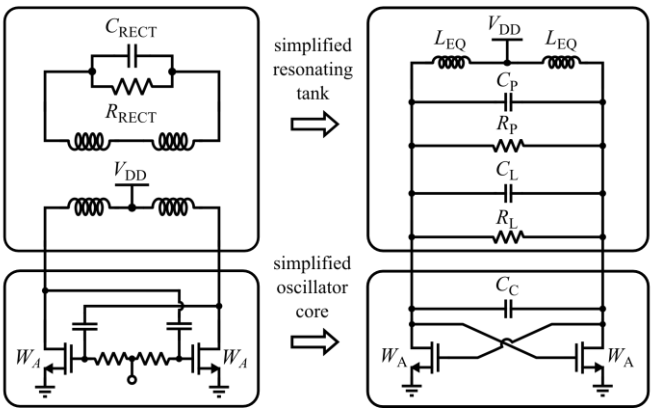

Fig. 4. (a) Schematic of the power oscillator with the equivalent input impedance of the rectifier. (b) Simplified model with lumped RLC tank.

A. Rectifier design

The adopted high-voltage Schottky diode has an elementary active area of 100 μm^2 and a breakdown voltage of 25 V. Its series resistance and junction capacitance are 160 Ω and 17 fF, respectively, while its I/V characteristic is shown in Fig. 5. At a given power and voltage level, the rectifier efficiency, η_{RECT}, is highly affected by the number of elementary diode cells, M, which defines the overall diode size. Table I shows simulated η_{RECT} and input impedance for different values of M. It is apparent that at increasing values of M the percentage of improvement in η_{RECT} reduces. Similar considerations can be drawn for R_{RECT}, while C_{RECT} grows almost linearly with M. The rectifier was evaluated at the nominal output voltage of 20 V and an output power of 1 W. The input impedance is a linearized first-harmonic extrapolation calculated by large-signal periodic steady state (PSS) simulations.

We set M to 40 to tradeoff η_{RECT} with C_{RECT}. This choice also takes into account the increasing complexity of the rectifier layout when a high number of elementary cells have to be connected. Indeed, parasitics due to metal connections highly affect efficiency performance and mainly input

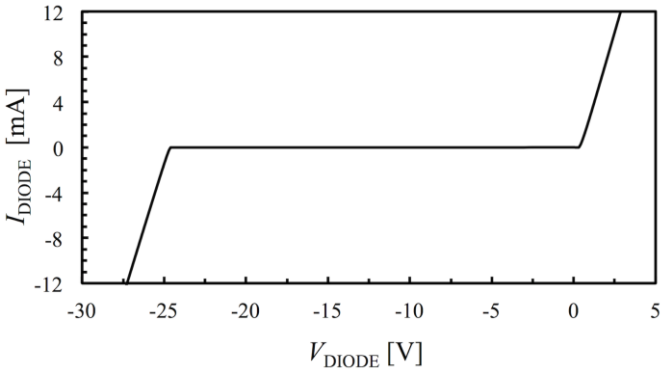

Fig. 5. I/V characteristic of a Schottky-diode basic cell.

IEEE Trans. on Power Electronics, vol. 32, no. 3, pp. 1984-1995, March 2017. DOI: 10.1109/TPEL.2016.2556939

TABLE I
SIMULATED RECTIFIER PERFORMANCE, V_{OUT} = 20 V, P_{OUT} = 1 W

	M	η_{RECT} [%]	R_{RECT} [Ω]	C_{RECT} [pF]
Schematic	10	56	173	0.35
	20	69	192	0.69
	30	80	211	1.04
	40	87	222	1.37
	50	90	226	1.73
Post-layout	40	82	219	3.58

capacitance, as highlighted by the post-layout performance for M=40 reported in Table I. Moreover, parasitic effects due to metal connections also impact the rectifier bandwidth that could in turn further reduce rectifier efficiency if high oscillation frequencies are used. However, simulations showed that for operating frequencies lower than 400 MHz the rectifier characteristics are quite constant and therefore it was modeled by an input impedance of 220 Ω//3.6 pF when the oscillator output power, P_{OUT_AC}, is fixed at 1.25 W. The efficiency degradation due to parasitic resistances was minimized by exploiting all the available metal layers (i.e., metal 1 to metal 4 plus alucap) and optimizing the number of vias. Finally, a 200-pF metal-oxide-metal (MoM) capacitor was integrated into the rectifier chip as a part of the output filter. It exploits the four available metal layers and the inter-metal dioxide of the standard CMOS process.

B. Transformer modelling

A customized design of the transformer is mandatory to maximize system efficiency and hence the availability of an accurate geometrically scalable model is of utmost importance. Unfortunately, there is no easy way to estimate the key electrical parameters of the transformer from its geometrical parameters to provide the required accuracy for evaluating power efficiency in a wide range of the design parameters. Best accuracy can be obtained by using parametric EM simulations, which imply high computational effort and long design time. In the proposed design procedure, the transformer (see Fig. 3) was modelled by means of the geometrically scalable lumped model shown in Fig. 6, which models half its structure, i.e. the single-ended configuration. This approach provides a higher level of accuracy compared to simpler models [20]. Indeed, widely adopted formulae developed for discrete transformers are not useful due to both complex loss and EM coupling mechanisms on silicon. The model in Fig. 6 exploits a π-like configuration with scalable expressions for both reactive and resistive components. In particular, for the inductances $L_{P1/2}$ and $L_{S1/2}$ simple analytical expressions are not applicable due to the large width and area required by the transformer compared to RF inductors for low power applications. Therefore, a monomial fitting expression was used for both primary and secondary coil low-frequency

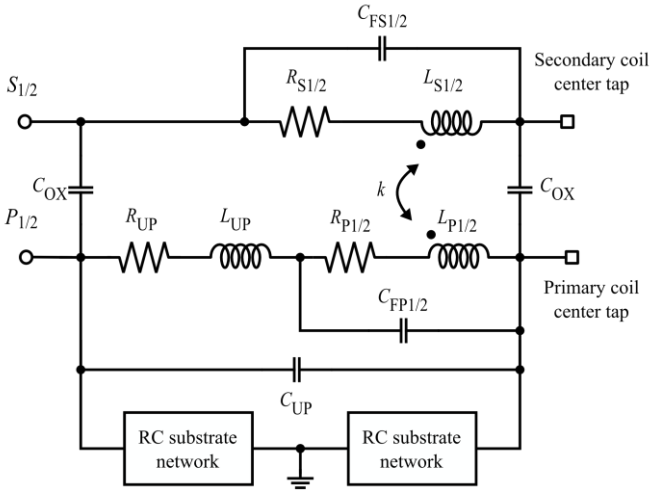

Fig. 6. Geometrically scalable lumped model of T_{ISO} (half structure).

inductances in the model shown in Fig. 5 [21]

$$L = A \times n^b \times w^c \times D_{OUT}^d \times D_{AVG}^e \tag{1}$$

where n, w, D_{OUT} and D_{AVG} are the number of turns, the metal width, the outer diameter and the average diameter of each transformer winding, respectively, while coefficients A, b, c, d, and e are fitting parameters. Model capacitances (i.e., the fringing contributions modelled by $C_{FP1/2}$ and $C_{FS1/2}$, the underpass capacitance, C_{UP}, and the isolation oxide capacitance, C_{OX}) were calculated with the simplified expression for parallel-plate capacitance, while a typical RC network was adopted to model the silicon substrate [14].

Series resistances $R_{P1/2}$ and $R_{S1/2}$ are the most important model parameters to accurately estimate transformer losses, mainly due to current crowding phenomenon in the winding metals. Such phenomenon is due to both skin effect and magnetically induced eddy currents, especially in the inner spirals. It leads to a non-uniform distribution of the current density within the metal tracks of the coils, which can be modelled with a frequency-dependent resistance [14]. For this reason, the following expression was exploited:

$$R = R_{DC} \times \left(1 + \frac{\alpha \left(\frac{f}{f_{CRI}} \right)^2}{1 + \beta \left(\frac{f}{SRF} \right)^2} \right) \times \frac{t}{t_{EQ}} \tag{2}$$

Here R_{DC} is the dc resistance of the coil, α and β are fitting factors, f_{CRI} is the critical frequency [22], which takes into account the crowding effects with respect to the geometrical parameters of the coil, while t and t_{EQ} are the physical and equivalent thicknesses of the metal layers, respectively, the latter being used to model skin effect phenomena [23]. The equation is further improved by a correction term based on the SRF, which accounts for the equivalent resistance reduction taking place nearby the self-resonance region [15].

The proposed model was properly customized for the adopted transformer configuration (see Fig. 3), which was chosen to minimize the length of the bonding wires between

IEEE Trans. on Power Electronics, vol. 32, no. 3, pp. 1984-1995, March 2017. DOI: 10.1109/TPEL.2016.2556939

the oscillator and rectifier dice, simplify the routing to the power supply and the LDMOS transistors and maximize the overlap between primary and secondary windings. These design choices maximize the coupling factor for a given oxide thickness. To this aim, the internal and external diameters were set equal for primary and secondary coils and the number of turns was limited to an integer and half-integer number for secondary and primary coils, respectively. The metal spacing for the primary, s_P, and secondary, s_S, windings was set to minimum allowable value for metal 3 and metal 4, respectively. As a result, we have only three free design parameters for the transformer, i.e. the primary coil outer diameter, D_{OUT_P}, width, w_P, and number of turns, n_P, being secondary coil parameters linked by the following constraints:

$$\begin{cases} D_{OUT\_S} = D_{OUT\_P} = D_{OUT} \\ w_S = \dfrac{2w_P + \left(2n_P - 1\right)\times\left(w_P + s_P\right) - s_S\left(2n_S - 1\right)}{\left(2n_S + 1\right)} \\ n_S = \left\lfloor G\times n_P + 0.5 \right\rfloor, \text{ where } G = \dfrac{\pi}{2}\times\dfrac{V_{OUT}}{2\,V_{DD}} = \dfrac{\pi}{2}\times\dfrac{V_{OUT}}{2\,V_{DD}} \end{cases} \quad (3)$$

To set the turns ratio, G, an ideal full-bridge rectifier was assumed (i.e., $V_{OUT}/V_{OUT\_AC} = 2/\pi$) along with the consideration that the differential voltage at the primary winding is about twice V_{DD}. It is worth mentioning that, thanks to (3) and the relatively high overlap between primary and secondary windings compared to the oxide thickness (i.e., about 20 times larger), the coupling factor, k, for typical transformers for power transfer is very high and almost constant in the adopted technology (e.g., 0.9).

The soundness of the developed model is well demonstrated by the error distributions between calculated electrical parameters and EM data for 30 geometrically scaled transformers (D_{OUT} from 650 µm to 1900 µm, n_P from 1.5 to 3.5, w_P from 60 µm to 300 µm.), as reported in Fig. 7. The x-axis reports the magnitude of the error, which is defined as the difference between EM simulation and model data. The y-axis reports the percentage of transformers that exceed the error value at the corresponding x–axis intercept. Maximum errors for inductance, Q-factor peak, SRF, and k are mostly smaller than 10%, which confirm that the model can be used as a reliable tool within the iterative co-design procedure described below. Fig. 8 shows three typical comparisons between model and EM simulations for the Q-factor.

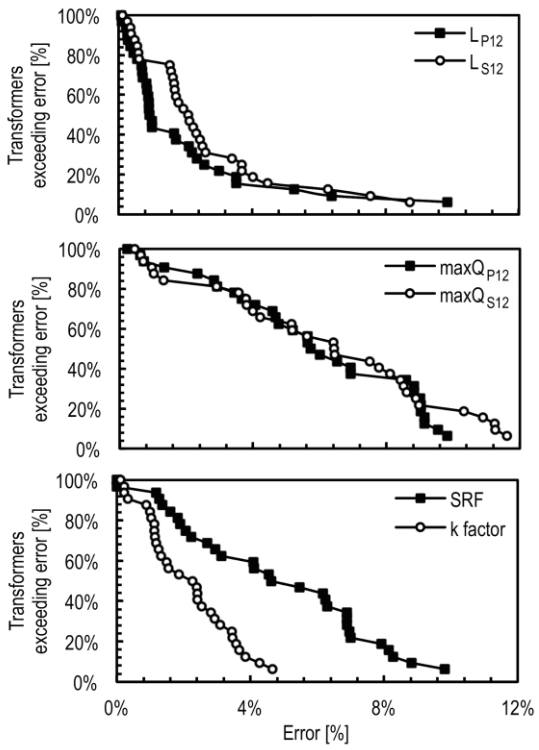

Fig. 7. Error distributions of the geometrically scalable lumped model calculated with respect to EM simulations of the transformer.

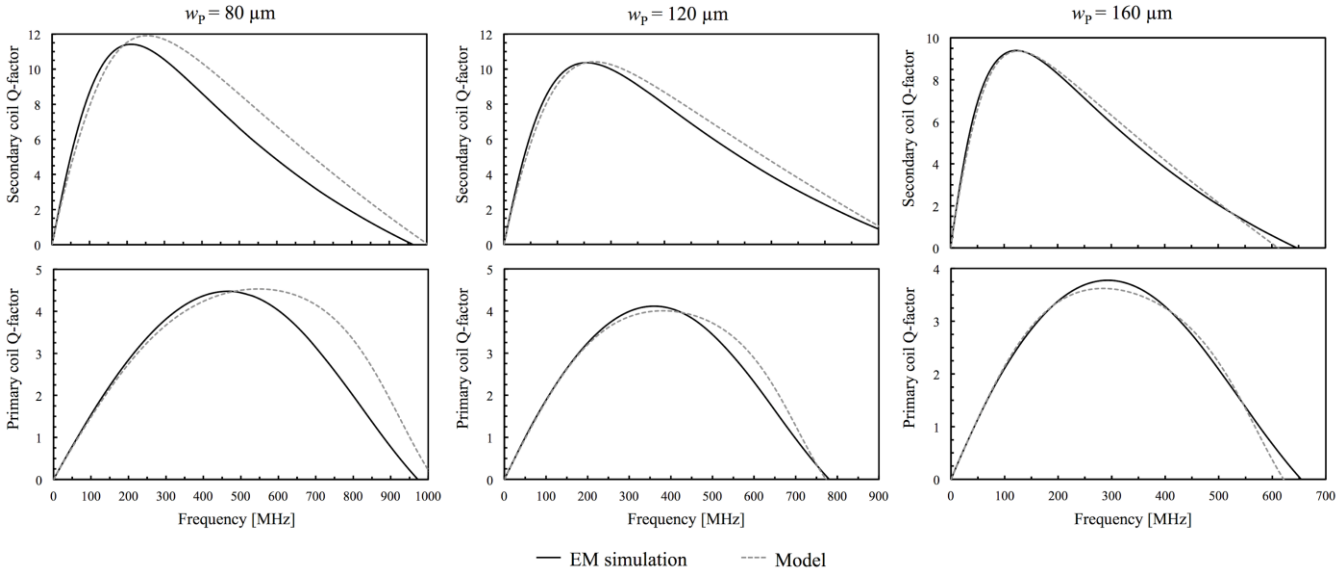

Fig. 8. Comparisons between model and EM simulations for the Q-factor (n_P=2.5, n_S=8, D_{IN} = 600 µm).

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C. Co-design procedure

As discussed at the beginning of this section, the inductance value should be maximized to improve the transformer performance ($\omega \cdot Q_P \cdot L_{EQ}$). However, maximizing the inductance leads to sub-optimal system efficiency due to the reduction of the oscillating frequency. Moreover, for a given area constraint, maximizing the inductance also means that the inductor width must be reduced and hence also the peak quality factor decreases. The following co-design procedure is aimed at optimizing the transformer but taking into account the performance of the oscillator core for the given constraints, so that the optimal inductance values are found.

We firstly recall the main design parameters for each building block of the dc-dc converter to summarize the free design variables. The parameter that defines the rectifier is the multiplicity, M, and only three geometrical parameters define the transformer (i.e., D_{OUT}, n_P, and w_P) thanks to the constraints in (3), which link the inductance ratio L_S/L_P to the step-up ratio required while maximizing the coupling factor. The design parameters of the oscillator core are the size of the power transistors, W_A, the size of the coupling capacitors, C_B, and the biasing voltage, V_B. However, D_{OUT} is constrained by the chip area and V_B, which sets the transistor bias current for the oscillation startup, can be set when the final design is refined. Indeed, the oscillator performance is only slightly dependent on the value of V_B. The proposed co-design procedure is represented in Fig. 9.

In the first step, the constraint on P_{OUT} and V_{OUT} is used to determine the number of diode cells, M, as a tradeoff between η_{RECT} with C_{RECT}, as discussed in Section II. The diode area imposes the rectifier efficiency, η_{RECT}, and its input impedance, $R_{RECT}//C_{RECT}$, and hence the required value of P_{OUT_AC} ($P_{OUT\_AC}^*$) at the output of the power oscillator.

In the second step, the chip area determines the transformer output diameter, D_{OUT}, the transformer size being the main contribution to the overall area. The transformer model in Fig. 6 is used to explore the geometrical design space by sweeping w_P for a given n_P. Since D_{OUT} is fixed, the variation of w_P leads to a variation of the transformer D_{INT} and hence of the transformer fill-factor ρ, as defined in Fig. 9 [24].

In the third step, W_A and C_B are set to allow the power oscillator to deliver the desired ac power for each transformer geometry. In this step, the voltage partition ratio between C_B and the gate capacitance of $M_{1,2}$ was kept constant, which means a capacitor C_B proportional to the transistor size, W_A. Therefore, an elementary cell can be defined for the oscillator active core that is set by the ratio C_B/W_A, thus reducing the active core design parameters to the cell multiplicity, N. To build the active core, N elementary cells are connected together, as shown in Fig. 9. At increasing N, the power at the transformer primary coils and hence output power P_{OUT_AC} increase. On the other hand, the oscillation frequency, f_{OSC}, decreases due to the higher equivalent capacitance of the active devices (C_C in Fig. 4), thus reducing the transformer loss resistance R_P. The reduction of R_P at some value of N can be so high that P_{OUT_AC} starts decreasing and the target power is never reached.

Finally, once the best oscillator core is sized for the selected transformer, a new geometry (i.e., higher w_p or higher n_P) is investigated by restarting the design procedure from step two.

This procedure guarantees best performance is achieved within the allowable geometrical design space. Typical results of the proposed co-design procedure are described by the charts in Fig. 10 showing a design space search constrained by $P_{OUT\_AC}^* = 1.25$ W and $D_{OUT} = 1.3$ mm. An elementary cell with $W_A = 330$ µm and $C_B = 3$ pF was used. Figs. 10(a) to (c) show output power P_{OUT_AC}, dc/ac efficiency $\eta_{DC\text{-}AC}$, and oscillator frequency f_{OSC}, respectively, for three increasing values of n_P. These charts show six curves, each one corresponding to a different transformer implementation, parameterized here by the fill-factor, ρ, which is the geometrical parameter better related to the ac spiral losses [24]. The curves are drawn as a function of multiplicity N and possible design solutions (i.e., the ones that reach the required

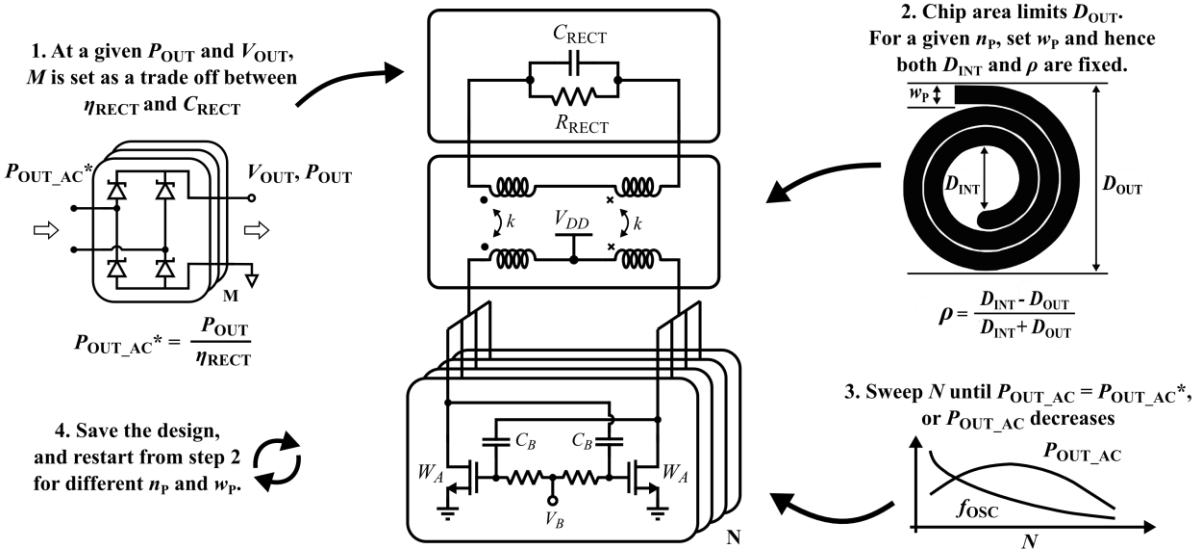

Fig. 9. Graphic representation of the proposed co-design procedure.

IEEE Trans. on Power Electronics, vol. 32, no. 3, pp. 1984-1995, March 2017. DOI: 10.1109/TPEL.2016.2556939

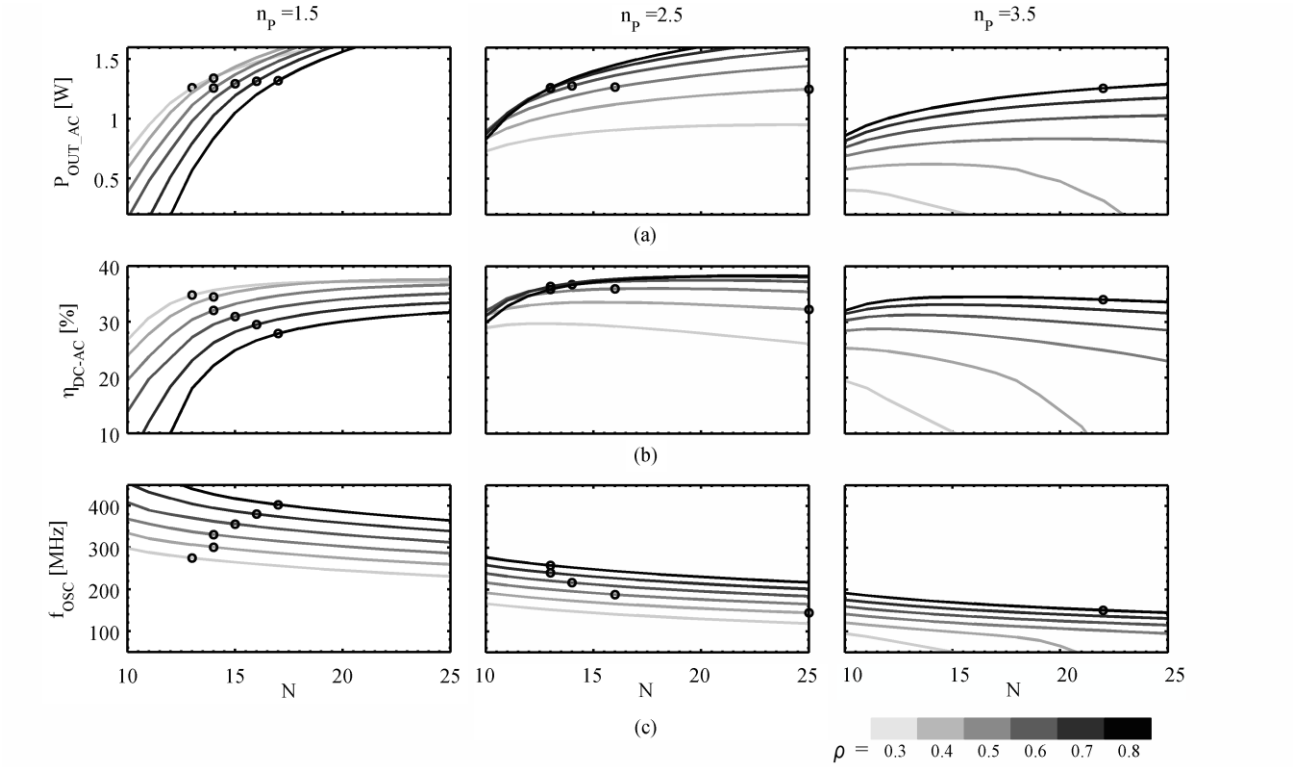

Fig. 10. Typical results of the co-design procedure (a) output ac power, P_{OUT_AC}, (b) dc/ac efficiency, $\eta_{DC\text{-}AC}$, (c) oscillator frequency, f_{OSC}.

P_{OUT_AC}) are highlighted by markers. They are also listed in Table II for better clarity. The displayed results well demonstrate the inherent complexity of an optimum design when the transformer is a free design component as it happens in this case of integrated implementation. The required output power is obtained for all the selected n_P. Although valid solutions are achieved for $n_P = 1.5$, primary coil inductances L_P are quite low and the optimum design cannot be achieved. Indeed, due to the area-constrained design procedure, the use of larger w_P to reduce series losses along with low n_P leads to too low L_P values, whereas increasing the oscillation frequency is not enough to achieve a high $\omega \cdot Q \cdot L$ product (i.e., high R_P in Fig. 4). On the other hand, for $n_P = 3.5$ only one solution is found, which achieves an $\eta_{DC\text{-}AC}$ of 34%, due to the higher dc losses. The most promising solutions are instead obtained with $n_P = 2.5$ that allows a range of w_P in which the best trade-off between dc and ac series losses of primary windings is achieved and efficiency reaches maximum values better than 36%. This w_P range, which is highlighted in bold in Table II, also corresponds to optimum values of ρ around 0.6.

Starting from these solutions, the design flow was iterated by increasing the sampling points closer to the optimal points. For each design cycle, the best solutions were further checked with EM simulations. Finally, the design was completed including the rectifier and parasitic effects due to bonding wires and both the ground and power supply planes. In the final design, the ratio C_B/W_A was adjusted to guarantee operating conditions with maximum allowable gate peak voltage for safe operation and best efficiency. Final values of the design parameters for the proposed dc-dc converter are summarized in Table III and the main expected results in Table IV, whereas Figs. 11(a) and 11(b) show simulated single-ended voltage/current waveforms at the LDMOS drain and rectifier input, respectively.

TABLE II
SUMMARY OF OPTIMIZED DESIGNS FROM FIG. 10

n_P	ρ	w_P [μm]	L_P [nH]	N	P_{OUT_AC} [W]	$\eta_{DC\text{-}AC}$ [%]	f_{OSC} [MHz]
1.5	0.3	154	3.2	13	1.26	34.8	275
	0.4	190	2.7	14	1.34	34.5	301
	0.5	222	2.3	14	1.26	32.1	331
	0.6	250	2.0	15	1.30	30.9	356
	0.7	275	1.7	16	1.32	29.5	380
	0.8	296	1.5	17	1.32	27.9	403
2.5	0.4	127	6.9	25	1.25	32.2	144
	0.5	**148**	**5.8**	**16**	**1.27**	**36.0**	**194**
	0.6	**166**	**5.0**	**14**	**1.28**	**36.7**	**217**
	0.7	**183**	**4.3**	**13**	**1.26**	**36.4**	**240**
	0.8	197	3.8	13	1.26	35.9	258
3.5	0.8	148	7.1	22	1.26	34.0	151

The resonant operation minimizes power losses and hot-carrier degradation in the active devices [25], thus increasing their efficiency and reliability, whereas the transformer involves most of the power losses. Actually, the transformer accounts for more than 56% of the overall losses as shown in Table V, where simulated breakdown of power losses is reported. The large transformer area, its round shape, and the large metal width adopted work together to prevent temperature hotspots and avoid reliability issues.

IEEE Trans. on Power Electronics, vol. 32, no. 3, pp. 1984-1995, March 2017. DOI: 10.1109/TPEL.2016.2556939

TABLE III
DESIGN PARAMETERS FOR THE PROPOSED CONVERTER

Block	Parameter	Value	Unit
Oscillator Core (N=16)	W_A	5.28	[mm]
	C_B	16.6	[pF]
	V_B	1.1	[V]
Isolation Transformer	w_P | w_S	146 | 55	[µm]
	s_P | s_S	1 | 5	[µm]
	D_{OUT}	1330	[µm]
	n_P | n_S	2.5 | 8	turns
	L_P; L_S	6; 52 @ f_{OSC}	[nH]
	Q_P; Q_S	2.9; 8.1 @ f_{OSC}	
	k	0.884	
Rectifier	M	40	diodes

TABLE IV
EXPECTED PERFORMANCE

Converters	Output power	Power efficiency	Oscillation frequency
dc–ac R_{RECT} = 220 Ω C_{RECT} = 3.6 pF	1.12 W	35.5%	198 MHz
dc–dc V_{OUT} = 20 V	0.93 W	30.6%	194 MHz

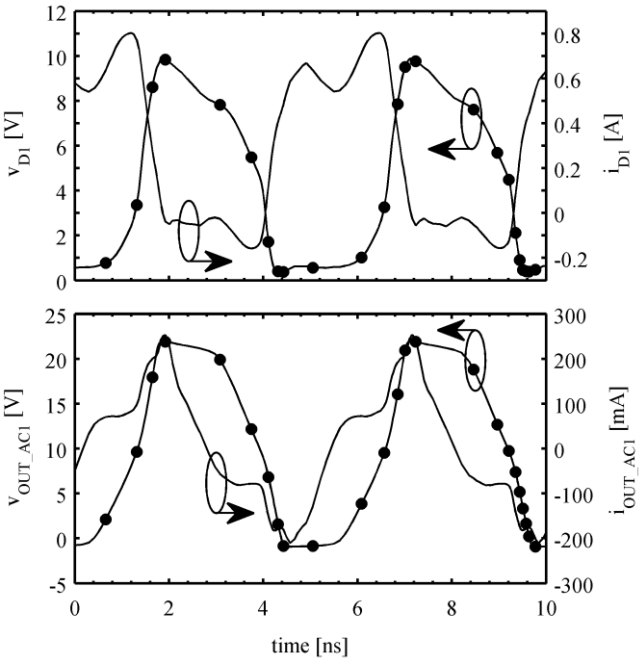

Fig. 11. Simulated single-ended voltage/current waveforms for the final design referred to Fig. 2 - (a) LDMOS drain terminal. (b) rectifier input terminal.

TABLE V
SIMULATED BREAKDOWN OF POWER LOSSES

Block	Power Losses	
	[mW]	[%]
Active Core	744	35.3
Transformer	1089	56.4
Rectifier	176	8.3

IV. EXPERIMENTAL RESULTS

The micrographs of the power oscillator and the full-bridge diode rectifier are shown in Fig. 12(a) and Fig. 12(b), respectively. The oscillator die size is 3.3 mm × 2.6 mm, mainly due to the isolation transformer. The LDMOS active core is placed at the bottom of the die along with the ground plane. A large metal plane provides the power supply connection to the primary coil center tap. Off-chip parasitics were minimized by using multiple bonding wires for both V_{DD} and ground. The rectifier has an actual size of 950 µm × 725 µm. As can be seen, the highlighted MoM capacitors account for almost 50% of the rectifier area. The overall silicon area of the two dice is about 9.3 mm^2.

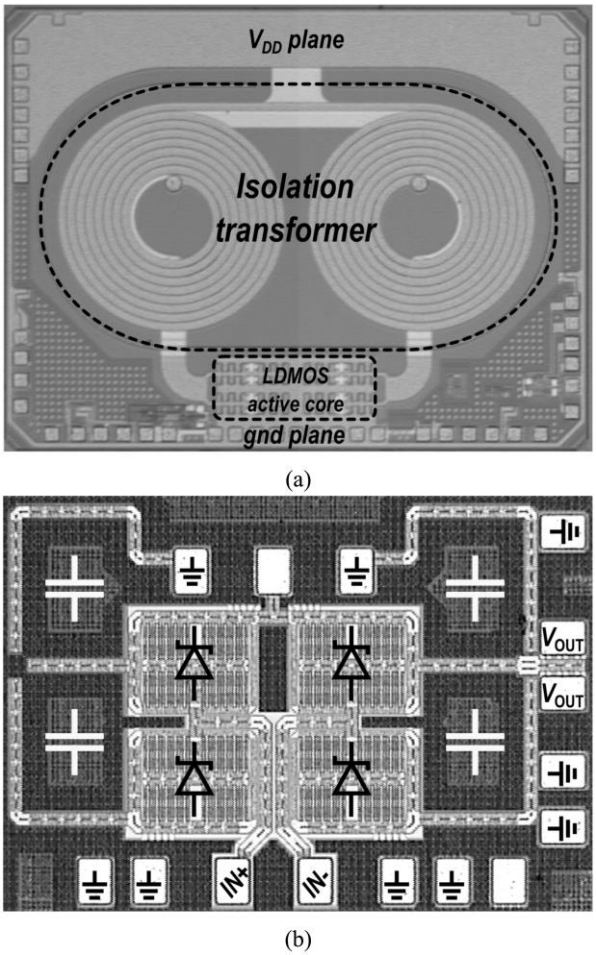

Fig. 12. Micrographs of (a) power oscillator and (b) rectifier.

IEEE Trans. on Power Electronics, vol. 32, no. 3, pp. 1984-1995, March 2017. DOI: 10.1109/TPEL.2016.2556939

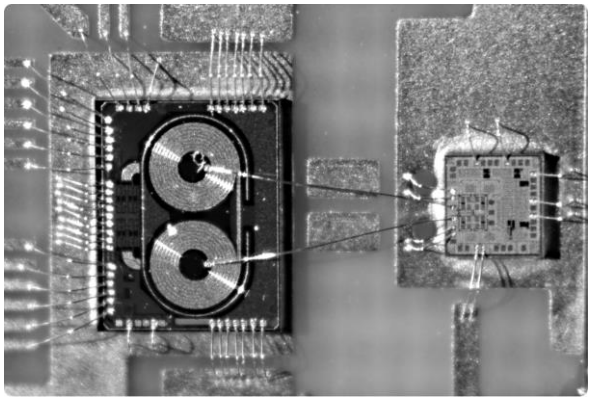

Fig. 13. Micrograph of the overall dc-dc converter assembled on board.

Experimental characterization was carried out in two phases. First, the performance of the dc-ac conversion was evaluated by mounting the power oscillator die on a testing board along with a discrete passive network as an equivalent output load (i.e., a resistance R_L in parallel to a capacitance C_L). The output voltage, V_{OUT_AC}, at the secondary winding of the transformer was captured by means of a high impedance active probing system. Afterwards, the complete system was assembled on the evaluation board, as shown in Fig. 13. Two bonding wires directly connect the secondary coil of the transformer to the rectifier input pads. The dc-dc converter was characterized at increasing dc output voltage, V_{OUT}, by means of a semiconductor parameter analyzer. It was also tested at different output power levels by using the on-chip on–off power control. All measurements were performed at 5-V power supply and room temperature.

A. Measurements of the dc-ac converter

Fig. 14 shows power P_{OUT_AC}, power efficiency $\eta_{DC\text{-}AC}$, and f_{OSC}, measured at the power oscillator output as a function of load capacitance C_L for the nominal value of R_{RECT} of 220 Ω. The curves of P_{OUT_AC} and $\eta_{DC\text{-}AC}$ show a peak value greater than 1 W and 31%, respectively, with C_L around 5 pF. The power oscillator exhibits high robustness with respect to C_L with an efficiency higher than 30% in a range of ±2 pF around the optimum value of C_L. However, compared with the expected values in Table IV, which were found for R_L = 220 Ω and C_L = 3.6 pF (i.e., the simulated equivalent input impedance of the rectifier), a reduction of both output power and efficiency of about 6.5% and four percentage points results, respectively. This is ascribed to a 15% reduction in f_{OSC} due to inaccurate evaluations of LDMOS parasitic capacitances. Indeed, the evaluation of these effects is a well-known problem that requires large-signal RF characterization and proper modelling, not available at the time of design [26]. Finally, Fig. 15 shows a measured voltage waveform at the power oscillator output for R_L = 220 Ω and C_L = 5 pF.

B. Measurements of the dc-dc converter

The full characterization of the system was carried out for two versions of the dc-dc converter, which differ for the metal back-end of the transformer. In particular, the standard back-end (i.e., 0.9-µm Al metal 3 and 3.7-µm Cu metal 4) was enhanced by thickening the primary coil metallization by about 50%, thus improving transformer efficiency. Measurements of both standard and thicker metal converters are presented.

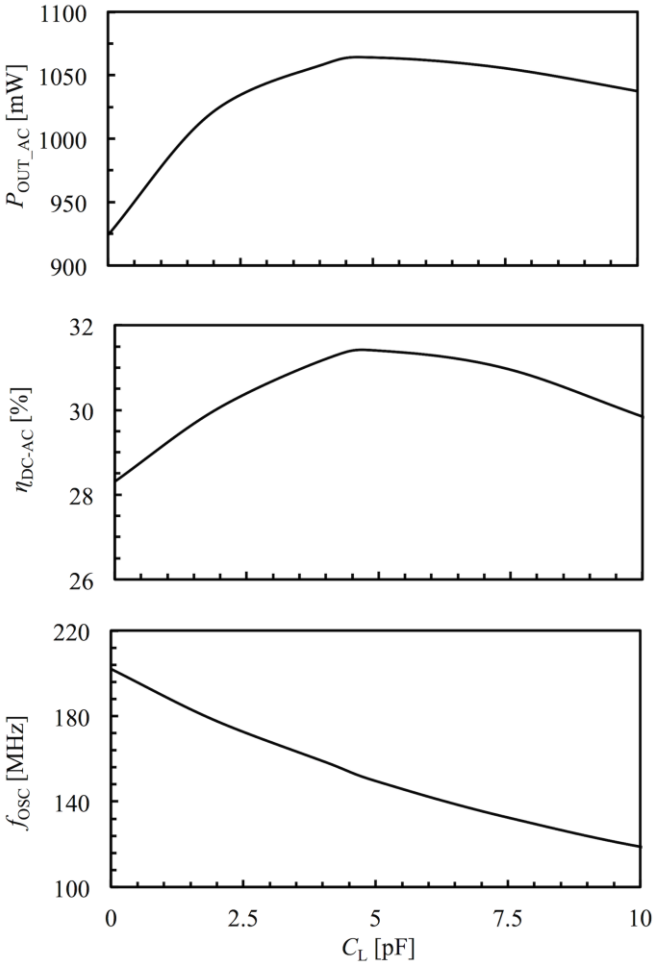

Fig. 14. Output power P_{OUT_AC}, power efficiency $\eta_{DC\text{-}AC}$, and oscillation frequency f_{OSC}, measured at the power oscillator output as a function of load capacitance C_L for R_L = 220 Ω.

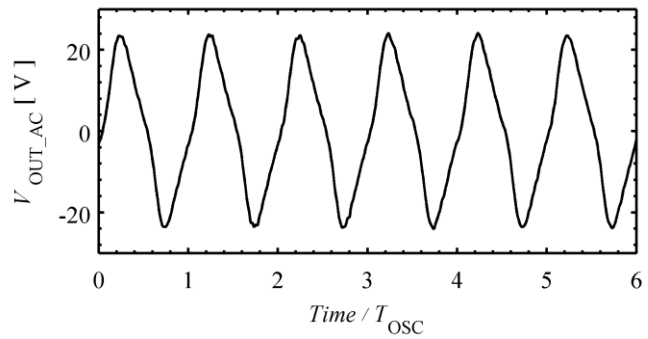

Fig. 15. Output voltage measured at the power oscillator output for R_L= 220 Ω, C_L = 5 pF.

Fig. 16 shows dc output power P_{OUT} and dc-dc power efficiency η, as a function of output voltage V_{OUT}, for both standard and thicker metal back-end. Efficiency increases with V_{OUT}, thanks to a better performance of both the oscillator and the rectifier at higher oscillating voltages. The exploitation of

IEEE Trans. on Power Electronics, vol. 32, no. 3, pp. 1984-1995, March 2017. DOI: 10.1109/TPEL.2016.2556939

a thicker primary coil allows both P_{OUT} and η to be improved by about 200 mW and almost two percentage points, respectively, in nominal conditions (i.e., V_{OUT} = 20 V), approaching values of 980 mW and 29.6%.

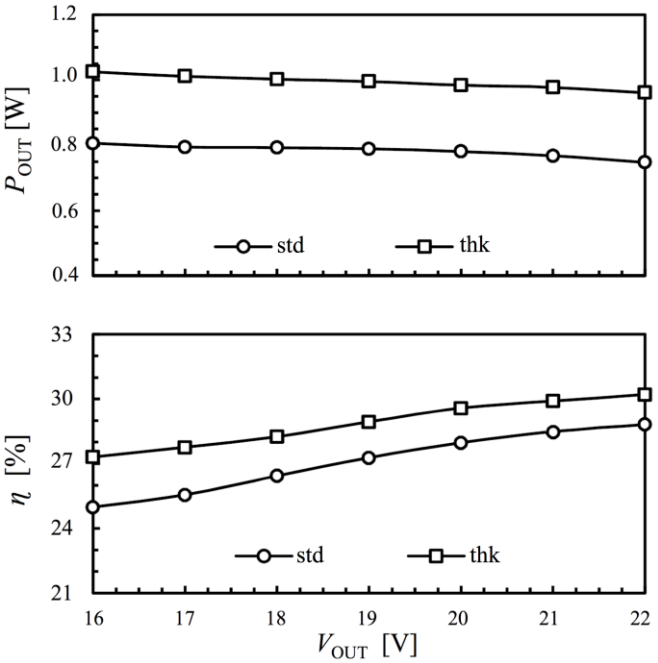

Fig. 16. Output power P_{OUT} and power efficiency η versus V_{OUT}.

The efficiency of both converters was tested at different P_{OUT} by using the on-chip turn-off power control driven by an external 200-kHz PWM signal with duty cycle from 10% to 100%. The curves in Fig. 17 show that η is quite constant with respect to P_{OUT}, thus confirming that output regulation can be achieved without affecting the power transfer efficiency of the converter. Moreover, there is enough unused silicon area in the oscillator chip (see Fig. 12(a)) to include the control circuitry without further increasing overall area occupation.

A comparison with most representative works is carried out in Table VI. Specifically, papers in [27]-[29] are CMOS based fully integrated step-up converters, while [8] and [9] are the

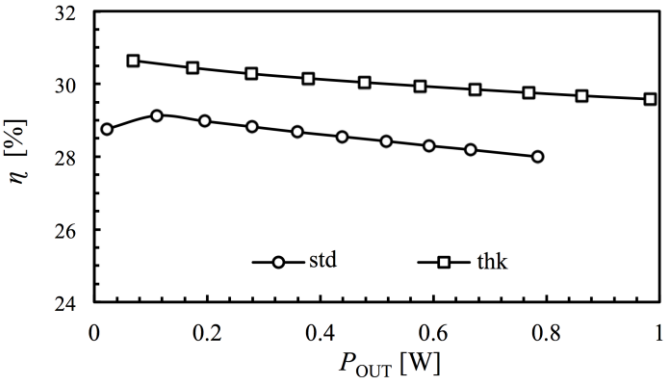

Fig. 17. Power efficiency η versus output power P_{OUT} (V_{OUT} = 20 V).

TABLE VI
COMPARISON WITH STATE OF THE ART INTEGRATED STEP-UP CONVERTERS

Ref.	[26]	[27]	[28]	[8]	[9]	This work (standard metals)	This work (improved metals)
Topology	Fly–back	Boost	Boost	Resonant	Resonant	Resonant	Resonant
Operating frequency, [MHz]	1400	120	100	170	160	165	168
Voltage gain	4.44	3.75	1.83	1	3	4	4
Maximum power, [mW]	**6.4**	**3.6**	**150**	**500[b]**	**275**	**780**	**980**
Efficiency	**19%**	**28%**	**63%**	**33%[b]**	**25%**	**28%**	**29.6%**
Power density, [mW/mm^2]	**50**	**2.1**	**67**	**-**	**-**	**83**	**105**
Galvanic isolation	**no**	**no**	**no**	**5 kV**	**5 kV**	**5 kV[d]**	**5 kV[d]**
V_{OUT}, [V]	8	6	3.3	5	15	20	20
Technology	0.18-µm CMOS	0.18-µm CMOS	0.18-µm CMOS[a]	0.6-µm HV-CMOS, Schottky[c]	0.6-µm HV-CMOS, Schottky[c]	0.35-µm BCD, Schottky	0.35-µm BCD, Schottky
Silicon Area, [mm^2]	0.127	1.69	2.25	-	-	9.3	9.3

[a]Bond–wire inductor. [b]Including closed-loop control circuitry. [c]Post–processed micro–transformer, thick Au metals, thick gate oxide. [d]Transformer isolation rating, guaranteed by technology.

IEEE Trans. on Power Electronics, vol. 32, no. 3, pp. 1984-1995, March 2017. DOI: 10.1109/TPEL.2016.2556939

sole examples of SiP integrated step-up converters providing galvanic isolation. The work in [29] achieves the highest efficiency by using bonding wire inductances, but the power density is lower and mainly the integration approach is not compatible with galvanic isolation. Ref. [8] and [9] achieve galvanic isolation but the power transformer is made up of very thick Au metals thanks to a post-processed back-end. Both works exhibit comparable efficiency but at much lower output power. The proposed solution advances the state of the art of fully integrated inductive step-up converters for both peak power and power density.

CONCLUSIONS

A galvanically isolated dc-dc converter in silicon technology has been presented. The highest level of integration was achieved since only two dice were used without any post-processing step. A co-design procedure is proposed to fully exploit the integrated approach by taking into account the interactions between building blocks. For the first time, this work shows the feasibility of galvanically isolated power conversion up to 1 W with a power efficiency of about 30% in a fully integrated implementation in silicon technology. Indeed, this performance greatly advances state-of-the-art integrated inductive step-up dc-dc converters in terms of both output power and power efficiency with outstanding power density, while also providing on-chip galvanic isolation. Experimental characterization also demonstrates that significant improvements in terms of power density and power efficiency can be achieved by improving the metal back-end, thus enabling a new class of highly integrated devices.

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REFERENCES

[1] N. Spina, G. Girlando, S. A. Smerzi, G. Palmisano, "Integrated galvanic isolator using wireless transmission," *US patent 8,364,195 B2*, granted Jan. 2013.

[2] A. Krone, T. Tuttle, J. Scott, J. Hein, T. Dupuis, N. Sooch, "A CMOS direct access arrangement using digital capacitive isolation," in *Proc. IEEE Int. Solid-State Circuits Conf. Tech. Dig.*, Feb. 2001, pp. 300-301.

[3] S. Kaeriyama, S. Uchida, M. Furumiya, M. Okada, M. Tadashi Maeda; Mizuno, "A 2.5 kV isolation 35 kV/us CMR 250 Mbps digital isolator in standard CMOS with a small transformer driving technique," *IEEE J. Solid-State Circuits*, vol. 47, pp. 435-443, Feb. 2012.

[4] K. Norling, C. Lindholm, D. Draxelmayr, "An optimized driver for SiC JFET-based switches enabling converter operation with more than 99% efficiency," *IEEE J. Solid-State Circuits*, vol. 47, no. 12, pp. 3095-3104, Dec. 2012.

[5] F. Pulvirenti, G. Cantone, G. Lombardo, M. Minieri, "Dispositivi con isolamento galvanico integrato (in Italian)", in *AEIT Convegno Annuale 2014 dalla ricerca all'impresa: necessità di un trasferimento più efficace*, ISBN 9788887237252, Trieste, Sep. 2014.

[6] O. Deleage, J-C. Crebier, M. Brunet, Y. Lembeye, Y. Hung Tran Manh, "Design and realization of highly integrated isolated DC/DC microconverter," *IEEE Trans. on Industry Applications*, vol. 47, no. 2, pp. 930-938, March-April 2011.

[7] D. J. Perreault *et al.*, "Opportunities and challenges in very high frequency power conversion," in *IEEE Applied Power Electronics Conference and Exposition (APEC)*, Feb. 2009, pp. 1-14.

[8] B. Chen, "Fully integrated isolated dc-dc converter using micro-transformers," in *Proc. IEEE Applied Power Electronics Conference and Exposition (APEC)*, Feb. 2008, pp. 335-338.

[9] B. Chen, "Isolated half-bridge gate driver with integrated high-side supply," *Proc. IEEE Power Electronics Specialists Conf. (PESC)*, Jun. 2008, pp. 3615-3618.

[10] V. Palumbo, G. Ghidini, E. Carollo, F. Toia, "Integrated transformer" USA Patent App. 14733009, filed Jun. 8, 2015.

[11] A. Moscatelli, A. Merlini, G. Croce, P. Galbiati, C. Contiero, "LDMOS implementation in a 0.35 μm BCD technology (BCD6)," in *Proc. IEEE Int. Symp. on Power Semiconductor Devices and ICs*, May 2000, pp. 323-326.

[12] L. Fanori, P. Andreani, "Class-D CMOS Oscillators," *IEEE Journal of Solid-State Circuits*, vol. 48, pp. 3105-3119, Dec. 2013.

[13] M. Shahmohammadi, M. Babaie, R.B. Staszewski, "A 1/f noise upconversion reduction technique applied to Class-D and Class-F oscillators," in *Proc. IEEE Int. Solid-State Circuits Conf. Tech. Dig.*, Feb. 2015, pp. 444-445.

[14] A. Scuderi, E. Ragonese, T. Biondi, G. Palmisano, "Integrated inductors and transformers: characterization, design and modeling for RF and mm-wave applications," CRC Press – Taylor & Francis Group, Nov. 2010.

[15] A. Scuderi, T. Biondi, E. Ragonese, and G. Palmisano, "A lumped scalable model for silicon integrated spiral inductors," *IEEE Trans. Circuits Syst. I*, vol. 51, pp. 1203-1209, Jun. 2004.

[16] T. Biondi, A. Scuderi, E. Ragonese, and G. Palmisano, "Analysis and modeling of layout scaling in silicon integrated stacked transformers," *IEEE Trans. Microwave Theory Tech.*, vol. 54, pp. 203 2210 May 2006.

[17] M. Steyaert, T. Van Breussegem, H. Meyvaert, P. Callemeyn, M. Wens, "DC-DC converters: From discrete towards fully integrated CMOS," in *Proc. IEEE European Solid-State Circuits Conf. Tech. Dig.*, Sept. 2011, pp. 42-49.

[18] S. R. Sanders, E. Alon, Le Hanh-Phuc, M.D. Seeman, M John, V.W Ng, "The road to fully integrated DC–DC conversion via the switched-capacitor approach," *IEEE Trans. on Power Electronics*, vol. 28, no. 9, pp. 4146-4155, Sep. 2013.

[19] G. Villar-Pique, H. J. Bergveld, E. Alarcon, "Survey and benchmark of fully integrated switching power converters: switched-capacitor versus inductive approach," *IEEE Trans. on Power Electronics*, vol. 28, no. 9, pp. 4156-4167, Sep. 2013.

[20] M. Kiani and M. Ghovanloo, "A figure-of-merit for designing high performance inductive power transmission links," *IEEE Trans. Ind. Eng.*, vol. 60, no. 11, pp. 5292-5305, Nov. 2013.

[21] S. S. Mohan, *et al.*, "Simple accurate expressions for planar spiral inductances," *IEEE Journal of Solid-State Circuits*, vol. 34, pp.1419-1424, Oct. 1999.

[22] W. B. Kuhn, N. M. Ibrahim, "Analysis of current crowding effects in multiturn spiral inductors," *IEEE Trans. Microwave Theory Tech.*, vol. 49, pp. 31-38, Jan. 2001.

[23] Eo Yungseon, W. R. Eisenstadt, "High-speed VLSI interconnect modeling based on S-parameter measurements," *IEEE Trans. Components, Hybrids, and Manufacturing Technology*, vol. 16, pp. 555-562, Aug. 1993.

[24] J. Craninckx, M. S. J. Steyaert, "A 1.8-GHz low-phase-noise CMOS VCO using optimized hollow spiral inductors," *IEEE J. Solid-State Circuits*, vol. 32, no. 5, pp. 736-744, May 1997.

[25] A. D. Sagneri, D. I. Anderson, D. J. Perreault, "Optimization of integrated transistors for very high frequency DC-DC converters," *IEEE Trans. on Power Electronics*, vol. 28, pp. 3614-3626, Jul. 2013.

[26] C. C. McAndrew, *et al.*, "Advances in LDMOS compact modeling for IC design: the SP-HV model and its capabilities," *IEEE Solid-State Circuits Magazine*, vol. 6, no. 2, pp. 35-46, Spring 2014.

[27] A. Savio, A. Richelli, L. Colalongo, Z. M. Kowacs-Vajna, "A fully-integrated self-tuned transformer based step-up converter," in *Proc. IEEE International Symposium on Circuit and Systems (ISCAS)*, Feb. 2003, pp. 357-360.

IEEE Trans. on Power Electronics, vol. 32, no. 3, pp. 1984-1995, March 2017. DOI: 10.1109/TPEL.2016.2556939

[28] A. Richelli, L. Colalongo, M. Quarantelli, M. Caramina and Z. M. K. Vanja, "A fully integrated inductor-based 1.8V-6-V step-up converter", *IEEE Journal of Solid-State Circuits*, vol. 39, pp. 242-245, Jan. 2004.

[29] M. Wens, K. Cornelissens, M. Steyaert, "A fully-integrated 0.18µm CMOS DC-DC step-up converter, using a bondwire spiral inductor," in *Proc. IEEE European Solid-State Circuits Conf. Tech. Dig.*, Sep. 2007, pp. 268-271.

Vincenzo Fiore received the Master degree in microelectronics and the Ph. D. in System's Engineering from the University of Catania, Italy, in 2012 and 2015, respectively. From 2011 to 2015, he was with the Radio Frequency Advanced Design Center (RF-ADC), a joined research center supported by University of Catania and STMicroelectronics, where he worked on several innovative ICs including the first fully-integrated power transfer systems with on-chip galvanic isolation in silicon technology. He also worked in the field of organic electronics, within the framework of COSMIC Project, and on ASK receivers, for UHF RFID systems. Since 2015 he is with DICE GmbH & Co KG, Linz, Austria, where he is involved in the design of mm-wave and baseband circuits for automotive radar transceivers. His research interests include design and optimization of analog circuits up to mm-wave frequencies.

Egidio Ragonese (M'03–SM'12) received the Laurea degree in electronic engineering and the Ph.D. degree in electronics and automation engineering from the University of Catania, Italy, in 1999 and 2003, respectively. Since 1999 he has been with the Radio Frequency Advanced Design Center (RF-ADC), a joint research center supported by the University of Catania and STMicroelectronics. In 2003 and 2008, he joined the Faculty of Engineering at the University of Catania as Research Associate and Research Assistant Professor, respectively. Since October 2011, he has been with STMicroelectronics, Catania, Italy. He was involved in the design and development of silicon-integrated transceivers for wireless communications. His research interests also included mm-wave integrated circuits for communications, and radar applications. Over the last few years, he has been also active in the field of organic electronics within the framework of two European Research Projects. His recent activity is mainly focused on the design of integrated systems for data/power transfer with galvanic isolation. Dr. Ragonese is co-author of more than 60 papers in international journals and conference proceedings, several patents, and two books on monolithic RF/mm-wave inductive components and highly integrated radar, respectively.

Giuseppe Palmisano (M'08–SM'09) received the Laurea degree in electronic engineering from the University of Pavia, Pavia, Italy, in 1982.

From 1983 to 1991, he was Researcher with the Department of Electronics, University of Pavia, where he was involved in CMOS and BiCMOS analog integrated circuit design. In 1992, he was a Visiting Professor with Universidad Autonoma Metropolitana (UAM), Mexico City, Mexico, where he taught microelectronics for Ph.D. students. In 1993 and 2000, he joined the Faculty of Engineering at the University of Catania, Catania, Italy, as Associate Professor and Full Professor, respectively, teaching microelectronics. Since 1999, he has been leading the Radio Frequency Advanced Design Center (RF-ADC), a joint research center supported by University of Catania and STMicroelectronics, Catania, Italy. He has supervised the design of several innovative analog integrated circuits and systems within the framework of national and European research projects and in collaboration with electronic industries. He is the coauthor of more than 250 papers in international journals and conference proceedings, around 50 international patents, and 3 books. His research interests lie in the area of analog integrated circuit design with special emphasis to RF applications. Recently, he has been facing remotely-powered transceivers with RF energy harvesting and power and data transfer systems with galvanic isolation.