Journal of Physics: Conference Series

PAPER • **OPEN ACCESS**

The Front-end for the new focal plane detector for the NUMEN project

The Front-end for the new focal plane detector for the NUMEN project

D G Bongiovanni[1], C Agodi[1], D Bonanno[2], D Carbone[1], F Cappuzzello[1,3], M Cavallaro[1], G De Geronimo[4], G Gallo[1,3], F Longhitano[2], D Lo Presti[1,3] and S Reito[2] for the NUMEN collaboration

[1] INFN Laboratori Nazionali del Sud, Catania, Italy
[2] INFN Sezione di Catania, Catania, Italy
[3] Dipartimento di Fisica e Astronomia, Università di Catania, Italy
[4] Stony Brook University,100 Nicolls Rd, Stony Brook, NY 11794, USA

E-mail: daniele.bongiovanni@ct.infn.it

Abstract. The design of the front-end electronics for the new tracker of the MAGNEX Focal Plane Detector (FPD) for the NUMEN project is presented. The front-end is based on the VMM chip, developed for ATLAS experiment at CERN. The architecture of the front-end (FE) electronics is designed to be modular and scalable to the final detector. The segmented anode board is designed in order to take advantage of the unique performances of the VMM chip, allowing a digital reconstruction of the track at high event rate. This anode board is connected to front-end by mean of Micro Coax Cable Assembly and does not make use of vacuum connectors. The front-end boards will be placed in air, facilitating in this way the heat dissipation and the connection to the read-out (RO) electronics. An innovative anode read-out strategy allows the reduction of the total number of channels to about 1400 and the measurement of the track at different depth in the detector with 750 μm spatial resolution.

1. Introduction

The foreseen upgrade of the Superconducting Cyclotron of INFN-LNS to reach the high beam intensity necessary for the NUMEN [1, 2, 3, 4] experimental program demands substantial changes in the technologies used for the MAGNEX [5, 6, 7] Focal Plane Detector (FPD) [8] together with new front-end electronics.

The design of front-end (FE) and read-out (RO) electronics was conducted in parallel with the design of the new FPD. In particular, one of the main objectives was to design a modular, scalable, radiation hard architecture, which, in addition, fulfilled the strong requirements in terms of high event rate, easy maintenance and precise synchronization.

The FPD tracker was radically redesigned taking advantage of the possibility to design a brand new full-custom FE and RO electronics.

A new concept for the tracker was developed. The starting point was to extract, for each track, the position of the ions in the volume of the tracker in a fully digital way.

2. The New Focal Plane Detector

The ionization charge is driven by an electric field in the gas towards a multiplying stage, typically a triple GEM or THGEM. Then the electrons are directed towards a first layer of 750 µm pitch strips.

Each strip of this layer is capacitive coupled to a twin strip in a second layer. The charge pulse inducted in the twin strip is then integrated by the FE and shaped.

The shaped signal is compared to a suitable threshold and the logic output of the comparator identifies the hit strip.

In this scenario the position is extracted by only one strip without the need for the calculation of the center of mass.

The value of the capacitance for each channel of the tracker is optimized to ensure maximum chip resolution in terms of charge and time. The drift time is also measured by the FE at sub-ns resolution.

An innovative scheme for the connection of FE electronics to the anode board was developed. The main objective was to place the FE in air to simplify the heat dissipation, the maintenance and, above all, the interconnections to RO. An advantage of this strategy is also the possibility to adopt countermeasure against to high level of radiation during the experiment.

The working principle of the segmented readout board of the new FPD tracker is represented in figure 1.

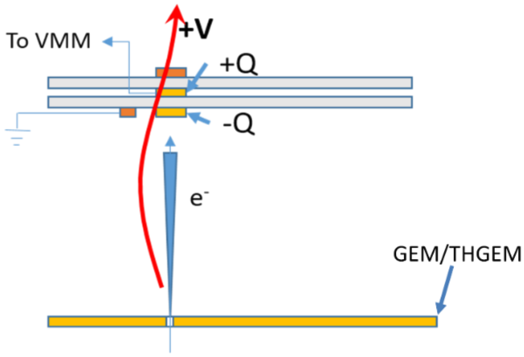

Figure 1. Working principle of the segmented readout board of the new FPD Tracker.

2.1. Design of the FPD

The FPD board has been designed in such a way as to cover the active area of the GEM foil.

This board is made up of 4 layers the first consists of a power supply plane in such a way as to be able to apply a potential difference to align the lines of the electric field, the second is the routing plane of the coupled strips, the third is the layer in which are present the strips exposed to the gas and finally the fourth layer is the ground plane in which there are trenches.

In figure 2 shows the presence of tranches that are transversal to the strips and identify the area in which the charge is collected so as to reduce the number of collisions on the individual strips.

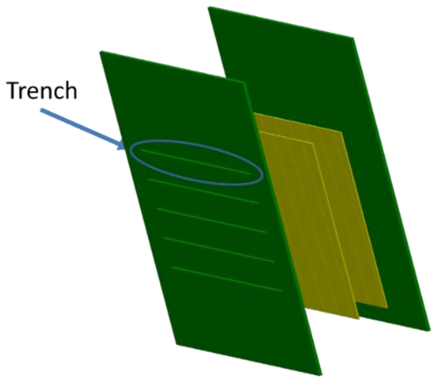

Figure 2. FPD segmented readout board in 3D view

3. The Front-End

The design of the front-end electronics for the new tracker of the NUMEN Focal Plane Detector is presented. The front-end is based on the VMM chip [9], developed for ATLAS experiment at CERN.

The architecture of the front-end electronics is thought to be modular and scalable to the final dimensions of the detector. The segmented anode board was designed in order to take advantage of the unique performances of the VMM chip [10], allowing a digital reconstruction of the track at high event rate.

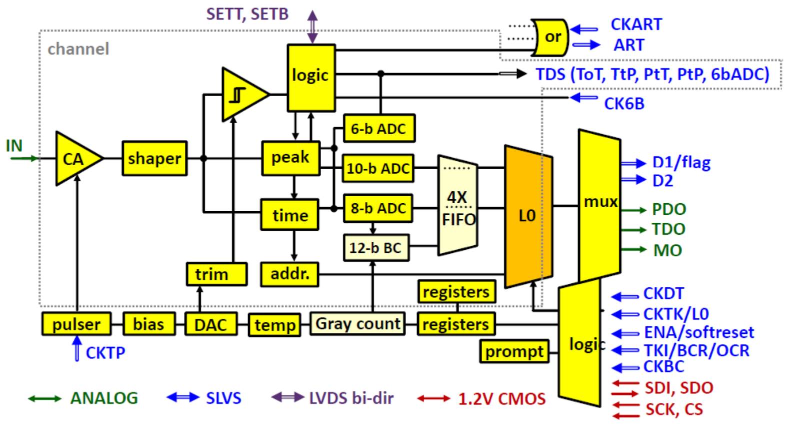

Figure 3. Architecture of the chip VMM3.

Fig. 3 shows the architecture of the VMM3, which is the actual evolution of VMM1, but with a much higher complexity and functionality. Each of the 64 channels provides the peak amplitude and time with respect to the bunch crossing clock signal or other trigger signal in a data driven mode. This is accomplished as follows. Each channel is equipped with a fast comparator with an individually adjustable threshold. When a signal crosses a set threshold a peak detection circuit is enabled.

Neighbour-enable logic allows setting the threshold relatively high and yet recording very small amplitudes. At the peak a time-to-amplitude converter is started and stopped by the trigger signal. The two amplitudes are digitized and stored in a de-randomizing buffer and readout serially with a smart token passing scheme that only reads out the amplitude, timing, and addresses of the channels with information, thus dramatically reducing the data bandwidth required and resulting in a very simple readout architecture.

The VMM3 has 64 channels easing the handling of a large number of channels. It also provides prompt information that can be used to provide pre-trigger signals.

3.1. Mode continuous

In the Numen experiment, the chip will be used using continuous mode.

The ASIC can operate in three modes: direct-outputs, two-phase or analog and continuous or digital.

In continuous (digital) mode a total of 38 bits are generated for each event in the VMM3. The first bit is used as a readout flag, the second is the threshold crossing indicator (it allows discrimination between above-threshold and neighbour events). Next is a 6 bits word for the channel address, followed by 10 bits associated with the peak amplitude, and 20 bits associated with the timing.

The 38-bit word is stored in a 4-events deep de-randomizing FIFO (there is one FIFO per channel) and it is read out using a token-passing scheme where the token is passed first-come first-serve only among those FIFOs that contain valid events. The first token is internally generated as needed and advanced with the token clock signal. The data in the FIFOs is thus sequentially multiplexed to the two digital outputs data0 and data1. The first output data0 is also used as a flag, indicating that events need to be read out from the chip. The external electronics releases a sync signal using the token clock as well (i.e. the token clock provides both advancement and data output synchronization), after which the 38-

IOP Conf. Series: Journal of Physics: Conf. Series **1056** (2018) 012007 doi:10.1088/1742-6596/1056/1/012007

bit data is shifted out in parallel to the data0 and data1 outputs using 19 clock edges of the external data clock.

4. Scheme of connections

The connection between the FPD readout board and FE is made via a vacuum seal board. In this board SAMTEC (SEARAY™ High-Speed/High-Density Array Micro Coax Cable Assembly) connectors have been used.

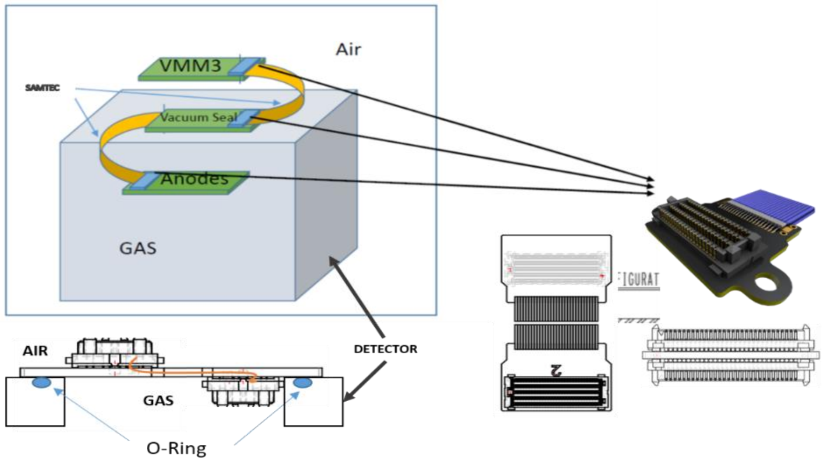

Figure 4. Scheme of connections

This choice allows for easy mounting and no need for vacuum connectors and it was possible to put the electronics in the air, avoiding the problems of heat dissipation in gas.

5. Conclusions

The research and development work on the design of FE-RO electronics for the NUMEN experiment was presented.

In the near future, the FE and RO board produced for a small-scale FPD will be tested, which will adopt all the strategies presented.

During the same period, a dedicated measurement campaign is planned to characterise the radiation tolerance of the FE-RO architecture presented.

References

[1] Cappuzzello F *et al.* 2015 *Journal of Physics: Conference Series* **630** 012018
[2] Agodi C *et al.* 2015 *Nuclear and Particle Physics Proceedings* **265-266** 28-30 ISSN 2405-6014
[3] Cappuzzello F *et al.* 2018 *Eur. Phys. J.* A **54** 72
[4] Cappuzzello F *et al.* 2015 *Eur. Phys. J.* A **51** 145
[5] Cappuzzello F *et al.* 2016 *Eur. Phys. J.* A **52** 167
[6] Cappuzzello F *et al*. 2014 *Nucl. Instrum. Methods Phys. Res.* A **763** 314-319 ISSN 0168-9002
[7] Cunsolo A *et al*. 2007 *Eur. Phys. J.* A ST **150** 343
[8] Cavallaro M *et al.* 2012 *The European Physical Journal* A **48** 59 ISSN 1434-601X
[9] De Geronimo G *et al.* 2007 *IEEE Transactions on Nuclear Science* **54** 541
[10] De Geronimo G *et al.* 2013 *IEEE Transactions on Nuclear Science* **60** 3