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Regulated Charge Pumps: A Comparative Study by Means of Verilog-AMS

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Abstract: This paper proposes a comparative study of regulation schemes for charge-pump-based voltage generators using behavioral models in Verilog- Analog Mixed Signal (AMS) code. An accurate and simple model of the charge pump is first introduced. It allows reducing the simulation time of complex electronic systems made up by both analog and digital circuits while maintaining a good agreement with transistor-level simulations. Finally, a comprehensive comparative study of the different regulation schemes for charge pumps is reported which allows the designer to choose the most suitable topology for a given application and Charge Pump (CP) operative zone.

Keywords: charge pump; regulated DC-DC converters; Systems on a Chip; Verilog-AMS

1. Introduction

In the incoming scenario of the connected world, emerging applications such as the Internet-of-Things (IoT), the Wireless Sensor Networks (WSNs) and the Wireless Body Networks (WBNs) employ self-powered sensor nodes to gather data and share them with the other nodes [1–3]. Systems on a Chip (SoCs), designed for these nodes, integrate several analog and digital electronic circuits targeted to execute a heterogeneous set of tasks. Some of these circuits are used to interface with real world signals and external ICs, such as power and data converters, clock sources, phase locked loops, sensors and actuators. Others, instead, work in multiple voltage/current domains which support several modes, such as standby, low power or reduced clock mode [1].

The interaction between analog and digital blocks needs to be verified to ensure not only correct connectivity of the integrated circuit but also SoC performance within specified requirements. To achieve a proper design of such complex SoCs, robust pre-silicon verification methodologies need to be implemented. The high-level view of the single circuit needs for Analog Mixed Signal (AMS) simulations that target the various features and modes [4–6]. Defining and implementing these simulations with good accuracy is a complex task as well as it is, in most cases, computationally intensive.

Looking from the manufacturing point of view, large simulation times could extend the needed time to put the product on the market (Time-to-Market), which is, as is well known, a crucial constraint for any commercial electronic product. For this purpose, to check the various blocks, it is important to evaluate the possible advantage of using a behavioral view rather than a SPICE-type view for all the analog blocks within a SoC [4–7]. The widely adopted Verilog-AMS is a hardware description language which allows for the behavioral abstraction of the circuits with reduced simulation time and links the verification of analog and digital domains in a coherent framework [5,8].

Among the analog blocks present in a modern SoC, DC-DC converters represent a fundamental sub-system that allows for adapting the input voltage of the overall system to that required by the single blocks. To give an example, the energy-autonomy of the nodes is achieved by scavenging energy from the environment (ambient or body) using different kinds of energy harvesters, such as photovoltaic cells,

thermoelectric generators and vibrational sensors [1,9–12]. Nevertheless, due to the heavy dependence of their output voltage from the operating conditions, these transducers are often unsuitable to directly feed the circuit where they are applied. For this reason, a power management unit (PMU) is mandatory employed to adapt the voltage and power levels with the maximum conversion efficiency.

Figure 1 shows a simplified block diagram of such a PMU for energy-harvesting applications [13–17]. The scheme reported in Figure 1 represents the most general architecture of a PMU for energy-harvesting applications from solar cells or thermoelectric generators. The model adopted in Figure 1 for the energy harvester, made up by a voltage source with an internal resistance in parallel with a capacitor, is suitable, to model PV cells and thermoelectric generators. The circuit is also suitable to model the output of an AC-DC converter (bridge rectifier) connected to a piezoelectric harvester. The input voltage, V_{IN}, provided by the external harvester, feeds the auxiliary circuitry which is geared toward the cold start of the primary boost converter. The first amount of harvested energy is conveyed to an intermediate accumulation element (capacitor C_{INT}) and, after its voltage has reached a target value (typically above the transistor threshold voltage), the stored charge is successively used to start-up the primary converter, switching-on the input source and enabling the gate control signals. Such operations are often flanked by a maximum power point tracker (MPPT), which controls the various sub-blocks in order to preserve the maximum power transfer from the source to the load. Finally, the primary converter is locally managed to obtain a precisely stable output voltage or to optimize power consumption in function of the required load current.

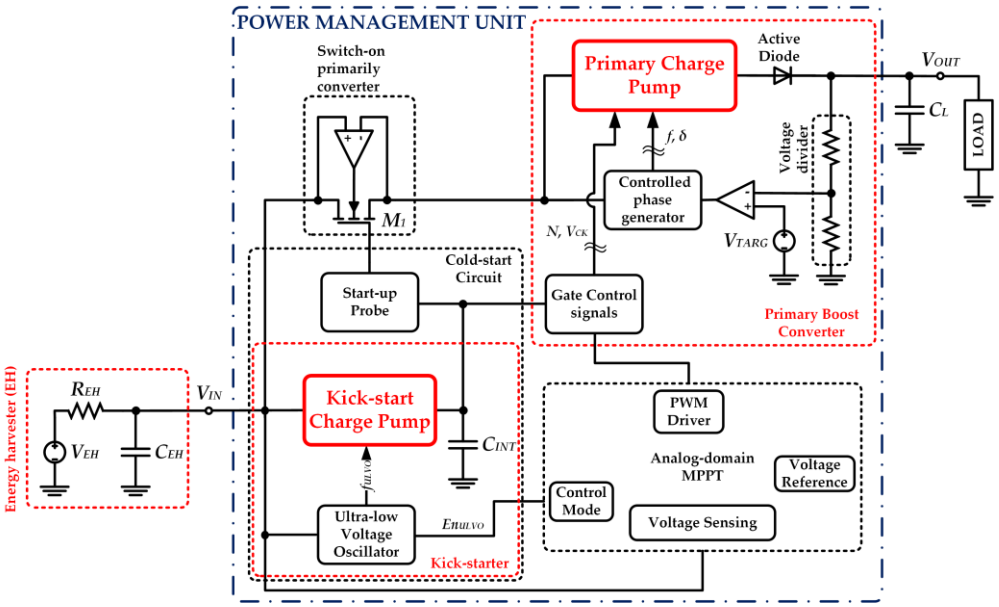

Figure 1. Simplified block diagram of a Charge Pump (CP)-based energy harvesting power management unit (PMU).

The converters (auxiliary and primary) are implemented by using bulk, boost or bulk-boost topologies, which are made-up by energy-storage components (capacitors and/or inductors) and active devices aimed to switch the stored energy from the input source to the load during defined time slots.

Among the converter types, inductor-based converters are mainly suitable for applications requiring power levels typically larger than hundreds of milliwatt [18–20]. However, inductive converters usually require external bulky inductors, as they are unsuitable for fully monolithic implementation. On the other hand, as the main advantage of switched-capacitor converters, the full integration on a silicon substrate is allowed thanks to the high storable energy densities of the capacitive components. Thus, when the output voltage is higher than the input one (boost topology), the converters based on Charge Pump (CP) circuits are the most suited and hence are the widest adopted topologies [9,10,18].

Focusing on CP converters and, in particular, the regulated primary boost converter, as highlighted in Figure 1, this paper aims to review their widely adopted regulation schemes and provides a design tool for reducing simulation time and to choose the optimum architecture according to the specific design constraints, which exploit AMS simulations.

The paper is organized as follows. The Section 2 introduces CPs, describing the behavioral model derived and its validation through transistor-level simulations. The Section 3 reports the overview of the regulation schemes. In particular, each of which has been mathematically analyzed to develop the behavioral view and then simulated and analyzed through their behavioral Verilog-A model. The Section 4 reports the regulation schemes' comparison. Finally, the conclusion and final remarks are included in the Section 5.

2. CPs Behavioral Model

The simplified block scheme of a N-stage CP is shown in Figure 2. In its simplest version, each stage is implemented by a diode (or diode connected transistor) and a capacitor [19]. To get rid of the voltage drop of each diode, a common adopted topology adopts, for each stage, the dual-branch cross-coupled one (also referred in literature as latched CP [20,21]) whose schematic is shown in the red-dashed box of Figure 2.

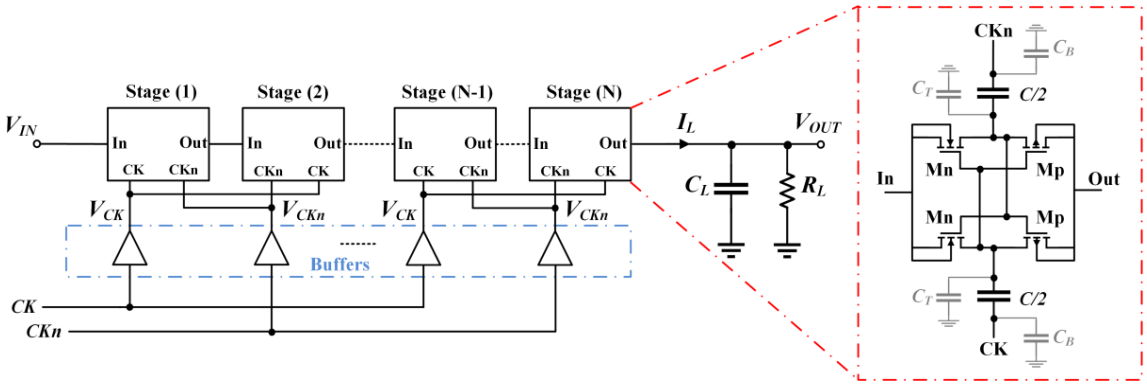

Figure 2. Simplified scheme of a dual-branch cross-coupled charge pump.

In this topology, the gate voltage of the MOSFETs is boosted by the clock amplitude during the conduction phase. This allows the voltage drop of the charge transfer switches, which connect capacitors of two adjacent stages, to be nullified. Therefore, each stage can be modeled with a constant on-resistance equal to R. It is worth noting, however, that the same model can be adapted to any other type of switch, such as a sub-threshold diode-connected or bootstrapped MOS transistor, etc. [10,18,22]. Each pumping capacitor of the considered CP topology has a constant value, $C/2$. Moreover, the two parasitic contributions $C_B = \beta C/2$ and $C_T = \alpha C/2$, being α and β technology-dependent parameters, model the stray capacitances connected to the bottom and top plate of the main capacitor, respectively. The stages are driven by two counterphase clock signals, CK and CKn, having a frequency equal to f, a duty-cycle δ whose range is $0 < \delta \leq 0.5$, and an amplitude V_{CK}, assumed equal to the input voltage V_{IN}. Finally, CP load is modelled with the pair C_L and R_L, which is fed by the output current I_L.

In literature, CPs are often assumed to operate within a Slow Switching Limit (SSL), and, under this working regime, they have been modelled, both for the transient and the steady-state behavior, by an equivalent RC-circuit [23]. However, voltage, power and area constraints of the modern applications also require sometimes the CP working in Fast Switching Limit (FSL) [24]. Thus, with this in mind, in the following, to develop the Verilog-AMS model, we will consider the CP block scheme model reported in Figure 3, which allows us to take into account a wide operating frequency range (i.e., both SSL and FSL).

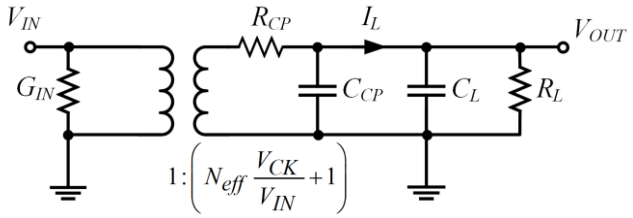

Figure 3. Proposed equivalent model of a cross-coupled charge pump.

In particular, considering the CP model in Figure 3, the ideal power conversion in terms of input voltage, V_{IN}, multiplication is provided by the transformer and the input conductance, G_{IN}, models loss at the input and is given by:

$$G_{IN} = \frac{V_{CK}}{V_{IN}}(\alpha+\beta)\frac{N}{1+\alpha}Cf = \frac{V_{CK}}{V_{IN}}(\alpha+\beta)N_{eff}Cf \tag{1}$$

where N_{eff} is the effective number of stages. In particular, N_{eff} represents the number of stage, N, reduced by a factor due to the charge partition between the stage capacitance and its top plate parasitic. In other words, N_{eff} models the power loss due to continuous commutations of the stray capacitances.

By using the switch-resistance model introduced in [24] and the dynamic CP model in [23], we can find the fundamental equations which describe transient, steady-state and power breakdown by means of settling time, output I/V characteristic (V_{OUT} as function of I_L) and power conversion efficiency, η, respectively expressed by:

$$T_S = R_{CP}(C_{CP}+C_L)\ln\left(\frac{N_{eff}V_{CK}+V_{IN}}{\left(N_{eff}V_{CK}+V_{IN}\right)-V_{TARG}}\right) \tag{2}$$

$$V_{OUT} = \left(N_{eff}V_{CK}+V_{IN}\right)-R_{CP}I_L \tag{3}$$

$$\eta = \frac{V_{OUT}I_L}{V_{IN}I_{IN}} \approx \frac{V_{OUT}I_L}{V_{IN}\left[\left(N_{eff}+1\right)I_L+V_{IN}G_{IN}\right]} \tag{4}$$

where V_{TARG} is the target output voltage, and R_{CP} and C_{CP} are the output impedance and self-capacitance of the charge pump, respectively, given by:

$$R_{CP} = \frac{R}{\delta}\left[\frac{f_n}{f}\left(\coth\left(\frac{f_n}{f}\right)+\cosh\left(\frac{f_n}{f}\right)\right)\right] \tag{5a}$$

$$C_{CP} = \frac{4N^2+3N+2}{12(N+1)}C \quad \text{for even } N \tag{5b}$$

$$C_{CP} = \frac{4N^2-N-2}{12(N+1)}C \quad \text{for odd } N \tag{5c}$$

It is worth noting that, in (5a), the term f_n indicates the natural frequency of the inter-stage charge transferring and its value is equal to $[(C + C_T)\ (R/\delta)]^{-1}$.

In conclusion, considering the CP block scheme model in Figure 3, the fundamental Equations (1)–(5), by using the Verilog-A code we can derive the behavioral model reported in Figure A1 of the Appendix A. Referring to this code, the electrical current supplied to the pump consists of a term useful for its operation and a term dissipated onto the stray capacitors. The output voltage is evaluated by using (3). Output self-capacitance, C_{OUT}, and the output resistance, R_{OUT}, have been accounted for as real functions of the normalized frequency, *fn/f*, which contains the CP parameters. The amplitude of the clock signal is externally defined by *Vck* and not set equal to the input signal. In addition, auxiliary parameters are provided by dynamically changing the number of stages (*dN*), the duty cycle (*dduty*) and the operative

frequency (*dF*). These last parameters, for the sake of simplicity, are realized through electrical signals. Of course, if a parameter variation is not needed, the corresponding signal can be connected to ground. Moreover, since the number of stages is limited by *Nmax*, the total capacitance is *Nmax C*. Additionally, when the charge pump works with a number of stages lower than *Nmax*, the total capacitance is uniformly distributed along the stages.

It is worth noting that Verilog-A can run on an AMS simulator, but it represents a subset of the Verilog-AMS, which is also able to be compiled/simulated using a transistor level SPICE-like simulator (for example Cadence Spectre). On the other hand, to run a Verilog-AMS code, an AMS simulator is mandatory.

In order to verify the effectiveness of the proposed model, several CPs with a different number of stages have been designed and implemented both at transistor level and by using the Verilog-A model, and then simulated with Spectre. In particular, after setting V_{IN} = 0.5 V, δ = 0.5, R = 5 kΩ, C = 100 pF, α = 0.01 and β = 0.1, resulting in a natural frequency $f_n \approx$ 1 MHz, different simulations have been performed for clock frequency values ranging from 10 to 100 MHz. Figure 4a shows the voltage at the output node of a 4- and 8-stages CP with an output capacitance value equal to the total CP capacitance and a 1-MHz clock frequency obtained for the transistor level and the Verilog-A model. Moreover, to show the Verilog-A model accuracy, during any phase (transient and steady-state) and for any condition (load and no-load), a current load of 10 µA was applied only after the CP output voltage reaches its maximum value.

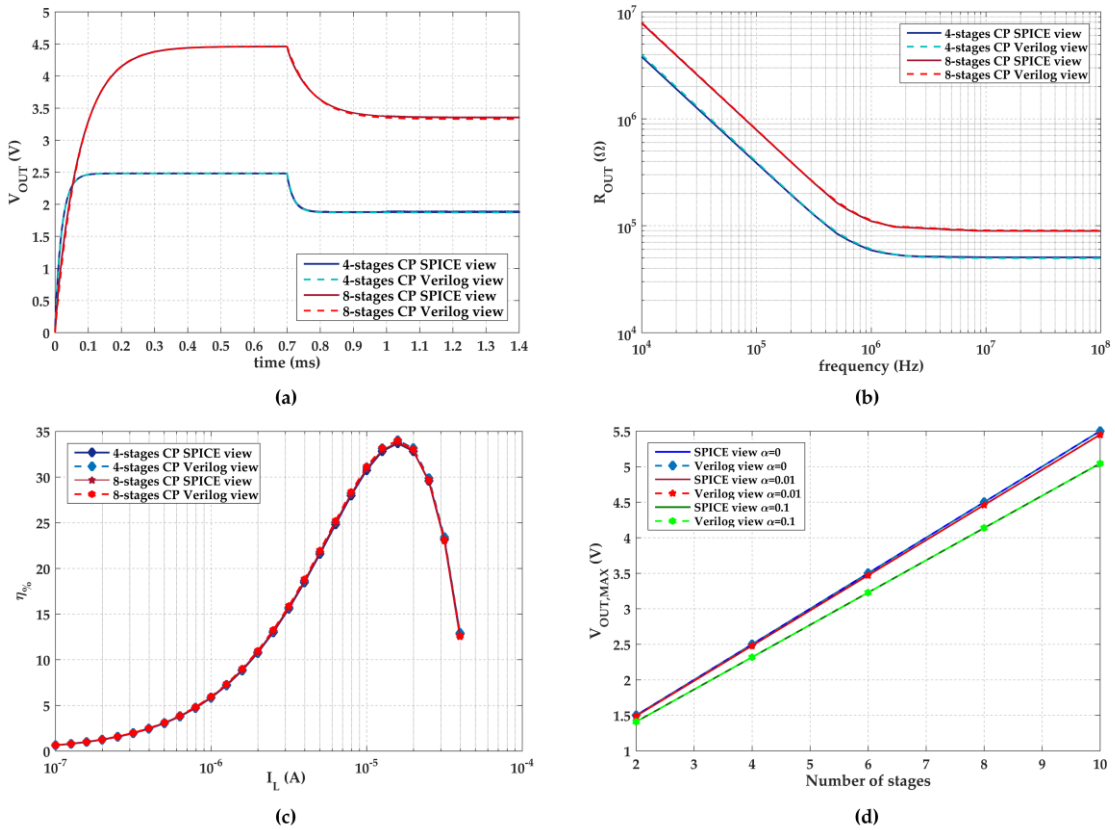

Figure 4. Transistor level and Verilog-A model simulation of the of 4- and 8-stage CPs: (**a**) transient output voltage without current load until 700 µs and, subsequently, a load current I_L = 10 µA; (**b**) output impedances vs. clock frequency; (**c**) power conversion efficiencies vs. output current; (**d**) maximum output voltage vs. the number of stages.

By inspection of Figure 4a, it can be easily observed that the time response of the Verilog-A model very accurately predicts the transistor level simulation, the relative error always being lower than 0.7%. Moreover, Figure 4b,c shows the output resistances of the two CPs as function of the clock frequency

and the power efficiency, η, as function of the output current load. In both cases, the effectiveness and accuracy of the Verilog-A model is demonstrated to describe the steady-state and transient behaviors of the CP from slow to fast switching limits and power breakdown.

Simulation results are summarized in Table 1, it is apparent that also settling time and input power demand are accurately modeled. Finally, a high accuracy is also shown on the maximum output voltage for charge pumps with a different number of stages and assuming various scenarios for the top-plate stray capacitance as depicted in Figure 4d.

Table 1. Simulation results summary for $N = 4$ and $N = 8$.

	View	$V_{OUT,MAX}$ (V)	T_S@90% (µs)	P_{IN} (µW)	V_{OUT} @I_L = 10 µA (V)	R_{OUT} (kΩ)
4-stages CP	**SPICE**	2.48	48.1	37.21	1.879	60.1
	Verilog-A	2.48	47.9	36.69	1.872	60.8
	Error%	0.00	0.42	1.4	0.37	1.17
8-stages CP	**SPICE**	4.46	180.1	66.68	3.351	110.9
	Verilog-A	4.46	179.1	66.38	3.329	113.1
	Error%	0.00	0.56	0.45	0.66	1.98

The computation times needed to simulate the charge pumps at transistor level and by using the Verilog-A model and considering the same simulation window, t_{sim}, set twice the time to reach the 90% of the maximum output voltage, are summarized in Table 2. Of course, as expected, the proposed behavioral model is more efficient. Indeed, the gain, defined as the ratio between the computation time of the Verilog-A model over that of the SPICE model, ranges from 0.4×10^6 up to 51.5×10^6.

Table 2. Computation time comparison.

Case	SPICE		Verilog-A		Max Gain
	@10 kHz	@100 MHz	@10 kHz	@100 MHz	
$N = 1$, $C_L = 100$ pF	34 ms, @t_{sim} = 1 ms	3.72 s, @t_{sim} = 20 µs	9 ms	9 ms	4×10^5
$N = 2$, $C_L = 200$ pF	127 ms, @t_{sim} = 5.8 ms	8.45 s, @t_{sim} = 88 µs	9 ms	9 ms	9×10^5
$N = 3$, $C_L = 300$ pF	318 ms, @t_{sim} = 16.5 ms	21.5 s, @t_{sim} = 0.2 ms	9 ms	9 ms	2.4×10^6
$N = 4$, $C_L = 400$ pF	646.9 ms, @t_{sim} = 35 ms	45.6 s, @t_{sim} = 0.4 ms	10 ms	10 ms	4.6×10^6
$N = 5$, $C_L = 500$ pF	1.21 s, @t_{sim} = 63.4 ms	77.52 s, @t_{sim} = 0.8 ms	10 ms	10 ms	7.8×10^6
$N = 6$, $C_L = 600$ pF	1.98 s, @t_{sim} = 104 ms	129 s, @t_{sim} = 1.2 ms	10 ms	10 ms	1.29×10^7
$N = 7$, $C_L = 700$ pF	3.14 s, @t_{sim} = 158 ms	188.22 s, @t_{sim} = 1.8 ms	10 ms	10 ms	1.88×10^7
$N = 8$, $C_L = 800$ pF	4.58 s, @t_{sim} = 231 ms	287.8 s, @t_{sim} = 2.6 ms	10 ms	10 ms	2.88×10^7
$N = 9$, $C_L = 900$ pF	6.4 s, @t_{sim} = 315 ms	374.1 s, @t_{sim} = 3.5 ms	10 ms	11 ms	3.4×10^7
$N = 10$, C_L =1000 pF	8.92 s, @t_{sim} = 427 ms	514.6 s, @t_{sim} = 4.7 ms	10 ms	10 ms	5.15×10^7

3. Regulation Techniques for Charge Pumps

The voltage at the output of the CP must be regulated in order to set a stable output voltage with constraints imposed by the load. Such constraints depend on the specific application and the supplied circuit type (i.e., purely capacitive, purely resistive or mixed). As an example, in non-volatile memory applications, such as NOR Flash and, more recently, 3D NAND memories [25,26], CP circuits are used to provide operation voltages for a single or multiple word lines (WLs), which exhibit a purely capacitive behavior. For these CPs, the main design specs are settling time and voltage conversion efficiency (VCE). VCE is defined as the ratio between the actual and the ideal output voltage. On the other hand, in energy-autonomous wireless nodes, the equipped sockets, such as sensors, actuators, communication and data-storage sub-systems, consume both static and dynamic power. In these contexts, the load is both capacitive and resistive and an efficient managing of the gathered energy assumes the primary importance. Consequently, power conversion efficiency constitutes the main constraint for these CPs [10,11,22]. Finally, in the CP used in the cold-start of energy-harvesting circuits based on thermoelectric generators, the load is both capacitive and resistive but the main specifications are VCE and settling time [13,15–17].

Ideally, in a conventional regulated N-stages CP, the output voltage can be adjusted from V_{IN} to $(N + 1)$ V_{IN} by changing one or more CP parameters according to the reference voltage, V_{TARG}. Based on the parameter on which they act, regulation schemes could be classified into:

- Adaptive schemes;
- Output resistance modulation schemes;
- Clock amplitude modulation schemes.

In particular, in the adaptive schemes, the stages are rearranged to allow for different CP voltage levels or works within the maximum power efficiency zone at the defined output voltage. In the output resistance modulation schemes, to adapt the CP output resistance to the load, the clock frequency or the duty cycle are changed, thus achieving a target output power or maintaining the maximum power transfer. In the clock amplitude modulation schemes, it is adjusted the clock amplitude, V_{CK}, (i.e., providing it different from the input voltage, V_{IN}) in order to reduce switching power losses or to speed-up the output transient response.

Each of these techniques are briefly discussed and analytically described in the following.

3.1. Regulation Scheme Based on the Adaptive Number of Stages

Adaptive schemes are mainly adopted in applications where the various system sub-blocks need to be supplied with a wide-range voltage. The on-chip voltage generator can be implemented by a cascade of CPs, extremely reduced to a single stage, where each single stage is turned on/off, or rearranged to generate different voltage levels, maintaining high performances for the overall system (e.g., settling time or power efficiency).

Adaptive schemes proposed in literature can be classified into two different categories, namely open-loop and closed-loop schemes. In the first one, the number of stages is set by an external device, such as a DSP or a μ-controller, in order to modify the level of the output voltage in un-regulated mode or to speed-up the transient behavior (Figure 5a) [27,28]. On the other hand, in closed-loop schemes, a block that searches for the optimum number of stages is exploited to adapt the number of active stages with the actual voltage gain, in order to optimize the whole system efficiency (Figure 5b) [29,30]. In the latter scheme, which is the widest adopted one, the generator often includes a further control feedback loop to set the output voltage at a reference voltage.

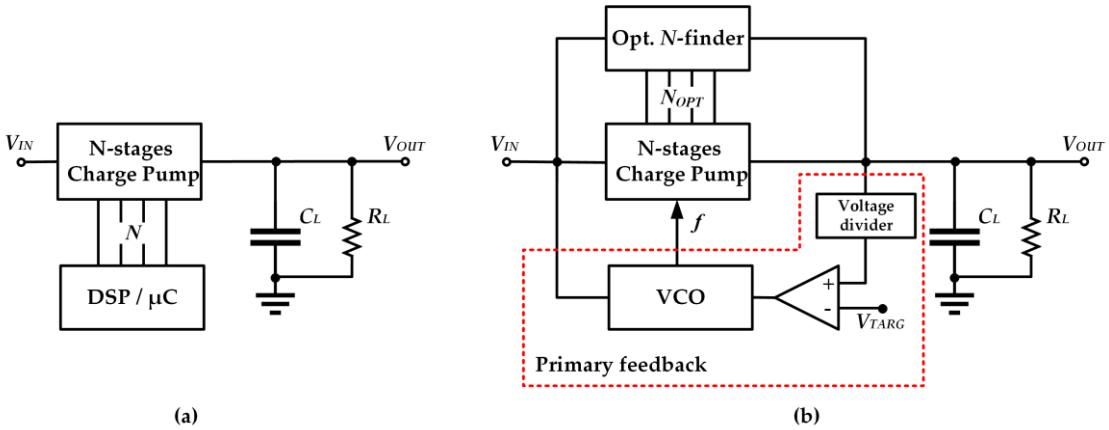

Figure 5. Adaptive topologies: (**a**) open-loop and (**b**) closed-loop.

The number of stages is an integer number higher than unity; hence, only a discrete set of output voltages can be generated, as shown by the staircase plot in Figure 6a. In literature, several papers deal with this topic and introduce design strategies with the aim of evaluating the optimum number of stages, N_{OPT}, under the silicon area [28,31]. In particular, in case we have a pure capacitive load,

the optimum number of stages that minimize the settling time was analytical derived in [28], and its value is given by (Note that the value expressed by (6) must be rounded to the nearest integer.)

$$N_{OPT} \approx \frac{4}{3}(1+\alpha)(k-1) \tag{6}$$

where $k = V_{OUT}/V_{IN}$ is the CP voltage gain. Since N_{OPT}, expressed by (6), is greater than the minimum number of stages (i.e., $N_{min} = (1 + \alpha)(k - 1)$), a possible implementation of the adaptive approach could be based on the adoption of a double-state charge pump, where the number N is commuted between N_{Opt} and N_{min}, to speed-up transient behavior [28]. Moreover, another possible adaptive approach application can be represented by an implementation to generate a finite set of output voltages composed by $(i + 1)V_{IN}$ with $i = 1, 2, 3, \ldots, N$ [27].

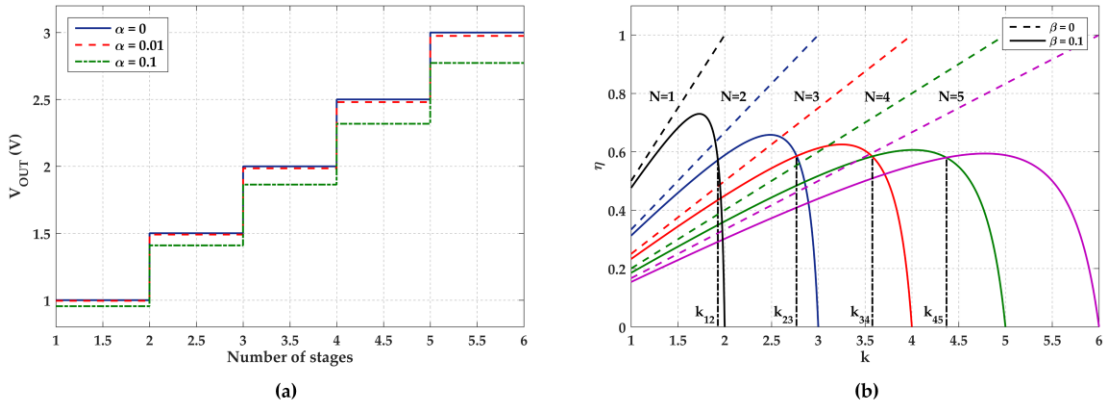

Figure 6. (**a**) Output voltage for different N; (**b**) power conversion efficiency (9) as a function of k.

Considering power-starved applications, the optimization strategy is focused on maximizing power efficiency. At this purpose, the CP must work between the SSL and the FSL, where the output CP resistance can be assumed to be equal to N_{eff}/fC [32]. And, in order to generate the reference output voltage, such value must be set according to:

$$\frac{N_{eff}}{fC} = \frac{\left(N_{eff}+1\right)V_{IN} - V_{OUT}}{I_L} \tag{7}$$

Substituting (1) and (7) in (4), the power efficiency is expressed as a function of the voltage gain, $k = V_{OUT}/V_{IN}$, as:

$$\eta = \frac{k}{\left[\left(N_{eff}+1\right) + \frac{(\alpha+\beta)\left(N_{eff}\right)^2}{\left(N_{eff}+1\right)-k}\right]} \tag{8}$$

It is worth nothing that (8) does not depend neither on the output current, nor on the total CP capacitance. Relationship (4) versus the voltage gain for different values of N and β, assuming $\alpha = 0$, is shown in Figure 6b. By inspecting this figure, it is apparent that the power efficiency reaches its highest values in a limited range of k and it rapidly decreases for higher conversion ratios.

Changing the number of active CP stages, as appear in Figure 7b, we get a right shift on the plot of η, therefore, for a specific k value, it exists an optimal number of stages, which allow the highest efficiency [28] and it is given by:

$$N_{Opt} = \left[\left(1 + \sqrt{\frac{\alpha+\beta}{1+\alpha+\beta}}\right)(1+\alpha)(k-1)\right] \tag{9}$$

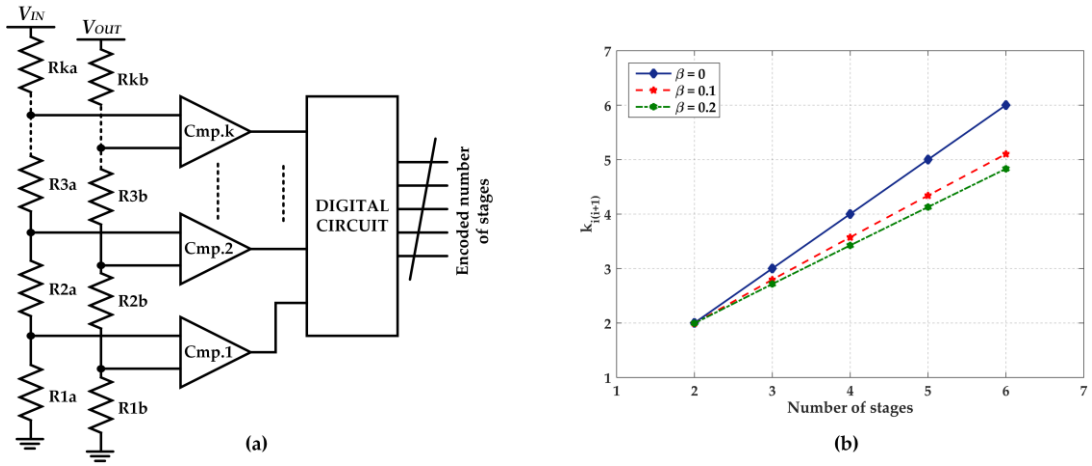

Figure 7. (**a**) Simplified block scheme of optimal *N*-finder; (**b**) estimated gain thresholds as a function of *N*.

Starting from this result, wide-output CPs with reconfigurable stages to select the optimal number of active stages to achieve the maximum efficiency at a given voltage gain were proposed in the literature [27,29,33,34]. In particular, the maximum required output voltage sets the maximum number of stages, thus we get $N_{MAX} = (1 + \alpha)\ (V_{OUT,MAX}/V_{IN} - 1)$.

Considering both plots in Figure 7, a simple but effective strategy can be realized with the use of a thermometer control of the number of stages, setting its value to the integer nearest to $(k - 1)$, and the possibility to rearrange the remaining $(N_{MAX} - k)$-stages to increase the pumping capacitance of the single active stage [31]. For this purpose, the plot in Figure 6b suggests that the optimum number of stages, given by (9), should be maintained for the inherent zone, which is delimited by the intersection with the adjacent curves. As an example, if $k = 3.5$, then $N_{Opt} = 3$, and this number must be set for k from a gain k_{23} to k_{34} given by the intersection of the η-curves for $N = 2$ to 3 and $N = 3$ to 4, as highlighted in Figure 7b. The various gain thresholds, $k_{i(i+1)}$ with $i = 1, 2, \ldots, N - 1$, can be calculated by:

$$k_{i(i+1)} = (i+1) - \frac{\sqrt{[(\alpha+\beta)(2i+1)+1]^2 + 4(\alpha+\beta)(i^2-1)} - [(\alpha+\beta)(2i+1)+1]}{2} \quad (10)$$

Given the value of the coefficients α and β, the normalized gain threshold can be evaluated and used to implement the optimal *N*-finder, as done in [33].

As shown in Figure 7a, the transistor-level implementation of the optimal *N*-finder is made up by a ladder of window comparators, which compares the input weighted values and the output voltage (division factor of the ohmic ladders is set in relationship (10) trough by the gain threshold) and a digital circuit that selects the number of active stages. The Verilog-A description of the adaptive topology, according to Figure 7, is reported in the Appendix A (Figure A2).

The adaptive scheme has been applied on the 8-stage CP presented and analyzed in the previous section, and its Verilog-A model has been simulated using Spectre. In particular, the parameters set in the previous section have been left unchanged, while several simulations have been carried by sweeping the voltage gain, *k*, from 1 to 6. Gain thresholds $k_{i(i+1)}$ are automatically calculated by the code as a function of the various parameters, and Figure 7b reports their values for different scenarios.

The simulation results are plotted in Figure 8. In particular, Figure 8a shows the open-loop output voltage varying the number *N* from 0 to 6. Inspection of the figure allows one to show how, step by step, the dynamic behavior changes, due to the arranging of the pumping capacitance. It also appears that the fastest response is obtained at the minimum output voltage level, whereas the slowest response corresponds to the maximum output voltage level. In Figure 8b, power conversion efficiency versus the

voltage gain is reported. The undulating trend curves confirm that the adaptive topology guarantees an efficiency at the highest values for each gain and condition (different values for α and β).

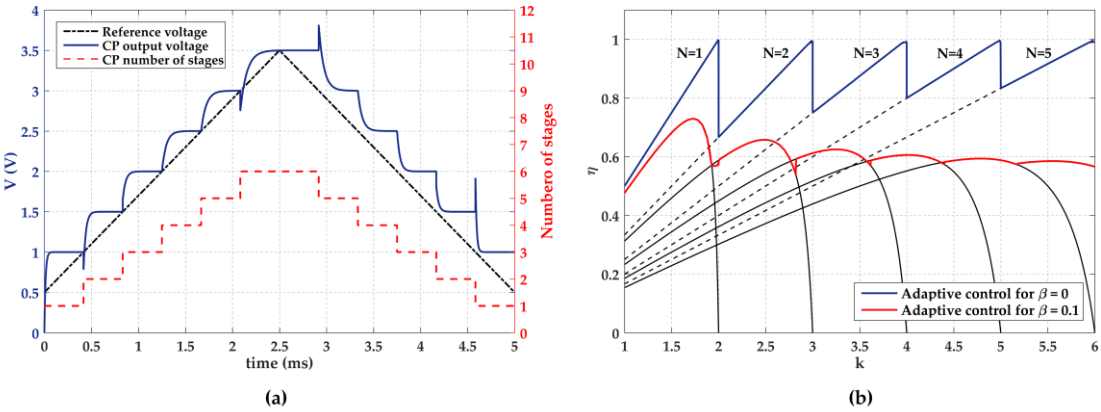

Figure 8. Open-loop output voltage controlled by an external reference (**a**), power conversion efficiency as a function of k (**b**).

It is worth noting that, although the rearranging strategy is the best solution in terms of area occupation, the pumping capacitance redistribution changes the operative zone of the CP. In fact, the natural frequency, f_n, which is normally independent from the number of stages, becomes proportional to N/N_{MAX} (i.e., it is a function of N). To give a practical example, the considered CP considered has $f_n \approx 1$ MHz when $N = N_{MAX} = 8$, while during the adaptive control N could sweeps from 1 to N_{MAX} and in the worst case (i.e., $N = 1$) the natural frequency reaches $f_n \approx 125$ kHz. For a given clock frequency, such as for example 1 MHz, the CP will work in the FSL zone, and the benefit gained by the rearranging strategy is loss. Two possible solutions to solve this drawback are the operative frequency reduction, or the RC product increase to compensate the decrease of f_n. Unfortunately, the first choice would reduce the current CP capability, while the second one would increase the silicon area occupation.

3.2. Regulation Schemes Based on Output Resistance Modulation

The output resistance modulation is a widely adopted regulation scheme to set the output voltage under different output load condition. This kind of feedback is commonly used in various application fields and, as shown in Figure 9, it is made-up by the N-stage CP, a voltage divider, a voltage comparator and, depending on the controlled parameter (i.e., clock frequency or duty cycle), a Voltage Controlled Oscillator (VCO) [35–38] or a Pulse Width Modulator (PWM) [39,40].

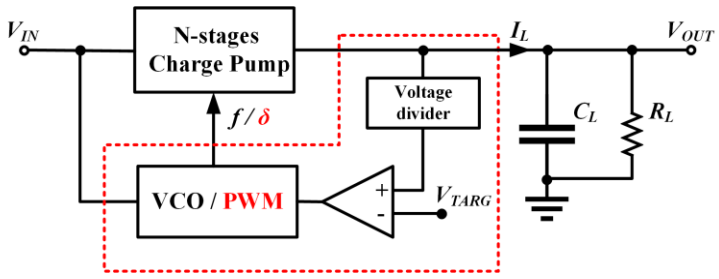

Figure 9. Block scheme of a CP output resistance modulation topology.

Focusing on the frequency-based modulation, the clock frequency acts on the CP output impedance to regulate the output voltage and to tune it according to the reference voltage. However, from Equation (5a), as confirmed by the trend of the curves in Figure 4b, the output impedance value can be changed only if the CP works within SSL. This condition limits the maximum operative frequency and, therefore,

the regulation range. Anyway, the regulation range can be increased by proper pumping capacitance and CP transistors re-sizing. The remaining limits are given by the minimum and the maximum VCO frequency, f_{min} and f_{MAX}, respectively, which define the absolute limits of the regulation range.

Since the regulation acts at the steady state, a proportional control of the CP output resistance can be assumed, and we can write:

$$\frac{N_{eff}}{Cf} = R_{SSL,MAX}[1 + A_{VCO}(k_{VD}V_{OUT} - V_{TARG})] \tag{11}$$

where $R_{SSL,MAX} = N_{eff}/f_{min}C$ is the maximum CP output resistance, A_{VCO}, expressed in (V^{-1}), is the gain of the cascade between OP and VCO and k_{VD} is the voltage partition coefficient of the voltage divider. Thus, within the control range, the closed-loop function for the output voltage results is as follows:

$$V_{OUT} = \frac{\left[\left(N_{eff} + 1\right)V_{IN} - R_{SSL,MAX}I_L\right] + (A_{VCO}R_{SSL,MAX}I_L)V_{TARG}}{1 + k_{VD}(A_{VCO}R_{SSL,MAX}I_L)} \tag{12}$$

and, assuming $A_{VCO}\, k_{VD} >> 1$, the output voltage in (12) approaches the value V_{TARGET}/k_{VD}.

The behavioral model of the control chain is reported in the Appendix A (Figure A3). The variation of the clock frequency is proportional to the difference between the scaled CP output voltage and the reference voltage. Furthermore, frequency range can be set from *fmin* to *fmax*. The closed-loop output voltage and the controlled clock frequency of the 8-stage CP regulated with the output resistance modulation in scheme in Figure 9, as a response to an output current and an input voltage variation are depicted in Figure 10. As expected, the output voltage follows the target one with a restrained error expressed as:

$$\varepsilon = k_{VD}\frac{1 - \left[\left(N_{eff} + 1\right)\frac{V_{IN}}{V_{TARG}} - \frac{R_{SSL,MAX}I_L}{V_{TARG}}\right]}{1 + k_{VD}(A_{VCO}R_{SSL,MAX}I_L)} \tag{13}$$

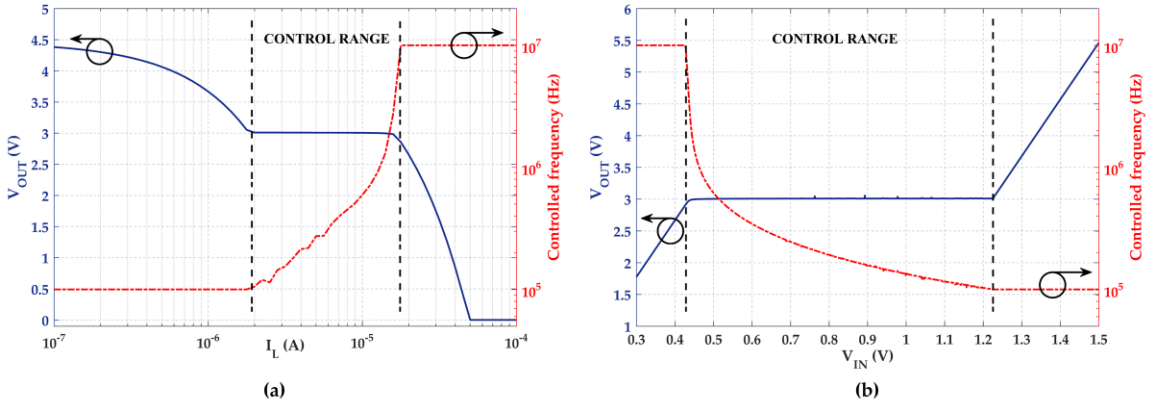

Figure 10. Closed-loop response: (**a**) output voltage and clock frequency for f_{min} and f_{MAX} set to 100 and 10 MHz, respectively, versus the output current and (**b**) the input voltage (I_L = 10 µA).

With the aim of comparing the regulation schemes, two performance parameters commonly adopted for voltage regulators have been considered, namely line and load regulation. In particular, the earlier is defined as the ability of the output voltage to maintain its specified output voltage over changes in the input voltage, and is defined by:

$$LineR = \frac{\partial V_{OUT}}{\partial V_{IN}} = \frac{\left(N_{eff} + 1\right)}{1 + k_{VD}(A_{VCO}R_{SSL,MAX}I_L)} \tag{14}$$

The load regulation is referred to the output current variation rather than the input voltage variation, and it is defined as:

$$LoadR = \frac{\partial V_{OUT}}{\partial I_L} = R_{SSL,MAX}\frac{A_{VCO}\left[k_{VD}\left(N_{eff}+1\right)V_{IN} - V_{TARG}\right]-1}{\left[1+k_{VD}(A_{VCO}R_{SSL,MAX}I_L)\right]^2} \quad (15)$$

Assuming a high gain A_{VCO} = 1000 V^{-1} and a partition coefficient k_{VD} = 0.1, with an output current of 10 µA, the error, line and load regulation are 0.14%, 0.011 and 185.8 Ω, respectively.

Different from the frequency-based type, the duty cycle-based modulation schemes act on the CP output impedance when it works in FSL, where the output impedance value changes as a function of the duty cycle (i.e., $R_{OUT,FSL} = (N_{eff} + 1)\ R/\delta$). This limits the minimum operative frequency, which can be extended by a proper stage components re-sizing. Other limits are due by the minimum and the maximum duty cycle of the pulse width modulator, $\delta_{min} > 0$ and $\delta_{MAX} \leq 0.5$, respectively. Like the frequency-based scheme, a proportional control of the CP output resistance can be assumed, and we can write:

$$\frac{\left(N_{eff}+1\right)R}{\delta} = R_{FSL,MAX}[1 + A_{PWM}(k_{VD}V_{OUT} - V_{TARG})] \quad (16)$$

where $R_{FSL,MAX} = (N_{eff} + 1)R/\delta_{min}$ is the maximum output resistance offered by the CP in FSL, A_{PWM}, expressed in (V^{-1}), is the gain of the cascade between OP and PWM, k_{VD} is the voltage partition of the voltage divider and δ_{min} is the minimum duty cycle. Within the control range, the closed-loop function for the output voltage is given by:

$$V_{OUT} = \frac{\left[\left(N_{eff}+1\right)V_{IN} - R_{FSL,MAX}I_L\right] + (A_{PWM}R_{FSL,MAX}I_L)V_{TARG}}{1 + k_{VD}(A_{PWM}R_{FSL,MAX}I_L)} \quad (17)$$

which has a similar expression of (12). Again, assuming $A_{PWM}\ k_{VD} >> 1$, the output voltage in (17) approaches V_{TARGET}/k_{VD}.

The behavioral model of the control feedback based on the output resistance modulation this is reported in the Appendix A Figure A4. In particular, by referring to the listed code in Figure A4, the variation of the clock duty cycle is made proportional to the difference between the scaled CP output voltage and the reference voltage. Furthermore, the duty cycle range can be set from *δmin* to *δmax*.

The closed-loop output voltage of the whole system has the response to an output load and an input voltage variation shown in Figure 11. As expected, assuming a high gain A_{PWM} = 1000 V^{-1}, the output voltage follows the target one with a restrained error even lower than 1%, while line and load regulation, valued as given in (14) and (15), respectively, are 0.1 and 1.05 Ω.

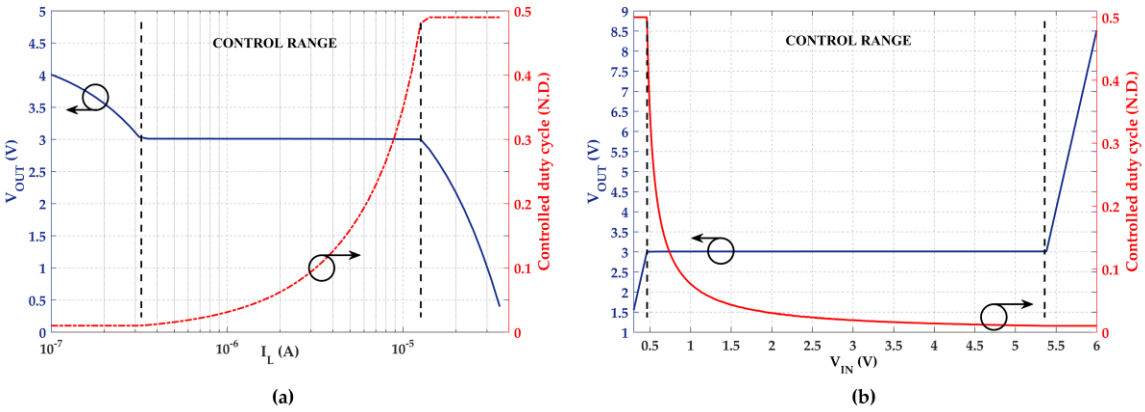

Figure 11. Closed-loop response: output voltage and duty cycle for δ_{min} and δ_{MAX} set to 0.01 and 0.49, respectively, versus the output current (**a**) and the input voltage (**b**).

3.3. Regulation Schemes Based on Clock Amplitude Modulation

Although rarely adopted, regulation schemes based on clock amplitude modulation offer a good compromise between circuit complexity and overall performances. In these schemes, the amplitude of the clock signals is adjusted to target a specific output voltage. This kind of feedback is made-up at least by the *N*-stages CP, a voltage divider, a linear comparator and an auxiliary DC-DC converter which, depending on the targeted application, can reduce [41] or boost [42] the input voltage V_{IN} to feed the buffers that provide the clock signals (Figure 12).

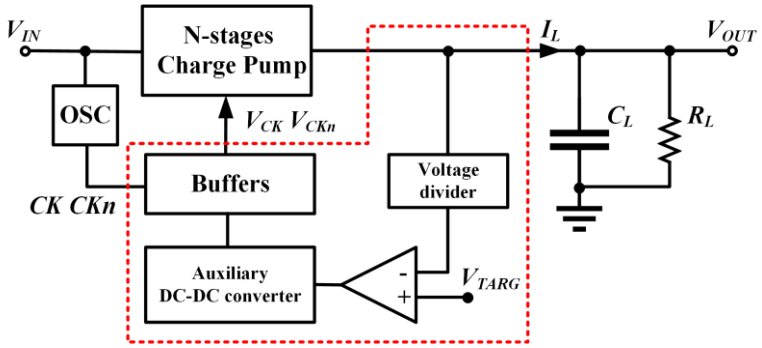

Figure 12. Simplified block diagram of a CP clock amplitude modulation scheme.

The clock amplitude affects the maximum CP output voltage (i.e., $V_{OUT,MAX} = N_{eff}V_{CK} + V_{IN}$) and, specifically, it tends to tune the CP output voltage according to the target voltage value. Therefore, the control is apparently independent from the CP working zone, SSL or FSL. However, it is worth nothing that the CP output resistance limits the CP output current capability; therefore, the regulation range could be limited mainly when CP works in the deep-SSL zone. Moreover, by inspection of (1), input current caused by switching losses can be decreased, making $V_{CK} < V_{IN}$ [41]; vice-versa, by inspection of (2), a boosting of the clock amplitude with respect to the input voltage ($V_{CK} > V_{IN}$) can lead to a settling time reduction [42]. Since the two action affects the CP performance in an opposite way, for these control schemes' application, field can be divided into low-power and high-speed applications, for the earlier and the latter approach, respectively.

A linear modulation of the controlled parameter has been assumed within the control range, hence:

$$V_{CK} = V_{IN}A_{VM}(V_{TARG} - k_{VD}V_{OUT}) \tag{18}$$

where A_{VM}, expressed in (V^{-1}), is the gain of the cascade between comparator and auxiliary DC-DC converter, here re-called voltage modulator, while k_{VD} is again the voltage partition coefficient of the voltage divider. Closed-loop function for the output voltage is simply expressed by:

$$V_{OUT} = \frac{\left(N_{eff}A_{VM}V_{TARG} + 1\right)V_{IN} - R_{CP}I_L}{1 + k_{VD}\left(N_{eff}A_{VM}V_{IN}\right)} \tag{19}$$

Of course, assuming $A_{VM}\ k_{VD} >> 1$, we see that the output voltage in (19) approaches that of V_{TARGET}/k_{VD}.

The behavioral model of the control chain is reported in Figure A5 of the Appendix A, where clock amplitude variation can be set from *Vck_min* ≥ 0 to a *Vck_max* arbitrarily selectable.

The closed-loop output voltage of the system versus the output current and input voltage variations is depicted in Figure 13a,b, for the reduced mode, $0 \le V_{CK} \le V_{IN}$, and Figure 13c,d for the boosted mode, $V_{IN} \le V_{CK} \le 2V_{IN}$. As expected, for a high gain $A_{VM}\ k_{VD} = 100$, the output voltage approaches the target one with an average error equal to 0.1%.

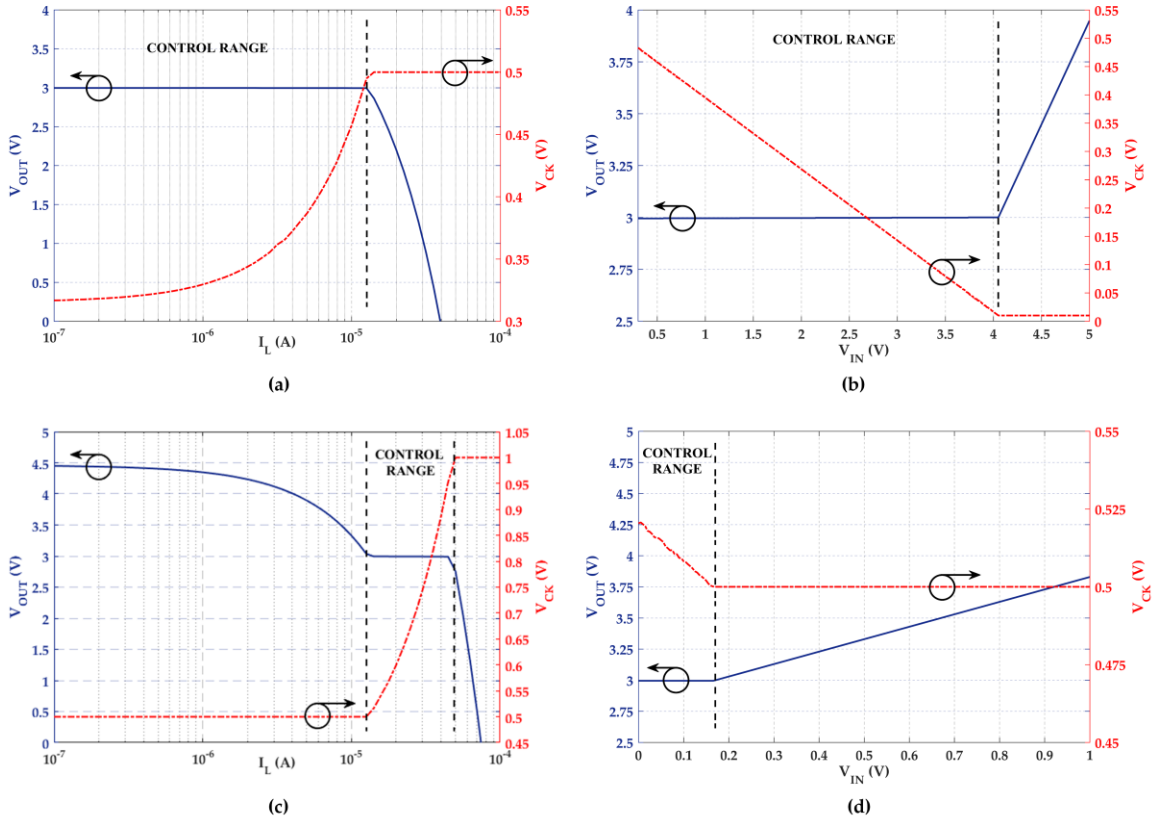

Figure 13. Closed-loop response: output voltage and clock amplitude versus the output current and the input voltage for $0 \leq V_{CK} \leq V_{IN}$ (**a**,**b**) and for $V_{IN} \leq V_{CK} \leq 2V_{IN}$ (**c**,**d**), respectively.

Line and load regulation acquire two different expressions for this kind of control, thus:

$$LineR = \frac{\partial V_{OUT}}{\partial V_{IN}} = \frac{N_{eff} A_{VM} (V_{TARGET} + k_{VD} R_{CP} I_L) + 1}{\left[1 + N_{eff} A_{VM} k_{VD} V_{IN}\right]^2} \tag{20}$$

$$LoadR = \frac{\partial V_{OUT}}{\partial V_{IN}} = \frac{R_{CP}}{1 + N_{eff} A_{VM} k_{VD} V_{IN}} \tag{21}$$

The numerical values for the simulated case are 0.15 and 112.2 Ω, respectively. As compared to the previous analysed schemes, the number of stages further increases the open-loop gain of the feedback, improving line and load regulations.

4. Comparison

The behavioral models of the regulation schemes treated in the previous section allows to highly reduce the simulation time of this kind of mixed signal systems. Moreover, they provide the designer a way to efficiently analyze and compare different solutions, according to the specific design constraints and applications. For this purpose, Figure 14 shows the power conversion efficiencies of the schemes considered and simulated in the previous sections within their regulation ranges. By inspection of Figure 14, the clock amplitude schemes appear to be most efficient when the system must provide relatively high current levels. On the other hand, the frequency modulation scheme is best suited for lower current levels.

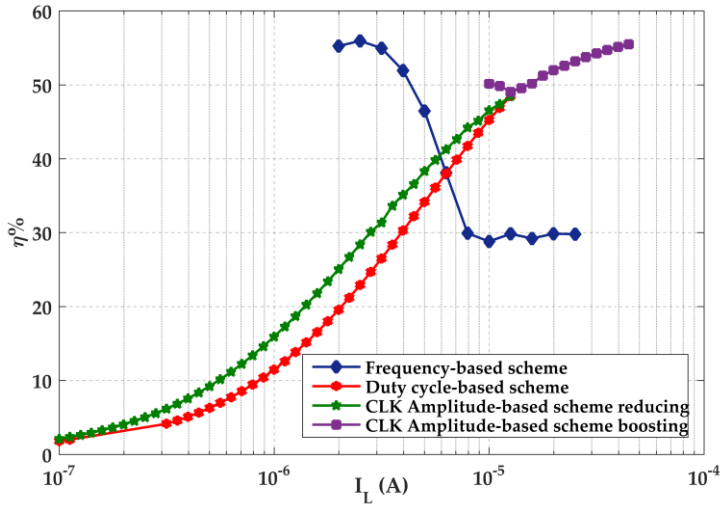

Figure 14. Power conversion efficiency of the considered schemes within the control range.

Finally, Table 3 summarizes the features of each regulation scheme. A qualitative comparison shows that clock amplitude-based schemes can regulate over the widest control range and for all the operative conditions, vice-versa the commonly adopted frequency-based regulation scheme has a narrow output current range. Additionally, adaptive schemes can be used to minimize the input power consumption of the CP-based voltage regulator.

Table 3. Comparison between the regulation schemes.

	Scheme	Control Range	Line Reg.	Load Reg.	Working Zone	Typ. Application
N	**Adaptive**	Depend by primarily feedback			SSL	Low power
R_{OUT}	**Frequency**	Narrow	<0.1	<200 Ω	SSL	General
	Duty cycle	Middle	>0.1	<2 Ω	FSL	General
V_{CK}	**Reducing**	Wide	>0.1	<200 Ω	SSL/FSL	Low power
	Boosting	Narrow	>0.1	<200 Ω	SSL/FSL	High speed

5. Conclusions

In this paper, a behavioral model for charge pumps operating in a wide-range of frequencies has been developed, adopting the Verilog-AMS language. The proposed Verilog-AMS code describes for the first time in literature a comprehensive model of the charge pump, which takes into account transient and steady-state equivalent parameters changes due to operation conditions (from Slow to Fast Switching Limit) and a complete frame of the power consumption. This study has been proposed with the aim of providing the designer with simulation tools that accurately follow the transistor-level response while allowing a huge reduction of the simulation time. Indeed, the proposed model allows for a huge reduction in the simulation time (about six orders of magnitude) as compared to a transistor-level schematic, while maintaining an excellent accuracy (error below 1%).

The model has been exploited to carry out an in-depth analysis of the main regulation schemes usually adopted in regulated DC-DC converters, providing an exhaustive comparison when the charge pump works into all the operative conditions. This study gives the designer a handy and effective tool to select the best regulation scheme according to the given design parameters. Indeed, by adopting the proposed design methodology, the best circuit architecture can be selected without performing time-consuming transistor-level simulations.

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Ethics: The authors have no conflicts of interest in the development and publication of current research.

Appendix A. Code Listings

```
`include "constants.vams"
`include "disciplines.vams"
module CPModel(p1, n1, p2, n2, Vck, dN, dduty, dF);
        inout p1, n1, p2, n2;
        input dN, dduty, Vck, dF;
        electrical p1, n1, p2, n2, int1, int2, dN, dduty, Vck, dF;
        parameter integer Nmax=10, N=1 from [1:Nmax];
        parameter real R=100k, C=10p, f=10k, duty=0.5, alpha=0, beta=0;
        real Gpar, Neff, fn, Rout, Cout, A;
        integer Nnew;
analog begin
        Nnew=N+V(dN,n1);
                                        if(Nnew>Nmax) Nnew=Nmax;
        if(Nnew%2 ==1) A=(4*pow(Nnew,2)-Nnew-2)/(12*(Nnew+1)); //odd number of stages
        else A=(4*pow(Nnew,2)+3*Nnew+2)/(12*(Nnew+1)); //even number of stages
        Cout=A*C*(Nmax/Nnew)*(1+alpha);
        Neff=Nnew/(1+alpha);
        fn=(duty*(1+V(dduty,n1)))/(R*C*(Nmax/Nnew)*(1+alpha)*(1+V(dF,n1)));
        Gpar=(V(Vck,n2)/V(p1,n1))*(Neff*(beta+alpha)*C*(Nmax/Nnew)*f*(1+V(dF,n1)));//Gpar=1/Rpar
        Rout= ((Nnew*cosh(fn/f) + 1)*R*fn)/(duty*f*(1+V(dduty,n1))*sinh(fn/f));
        I(p1,n1)<+ (Neff+1)*I(int1,p2)+V(p1,n1)*Gpar;
        V(int1, n2)<+Neff*V(Vck,n1)+V(p1,n1);
        I(int1, p2)<+V(int1,p2)/Rout;
        V(p2,n2)<+ idt(I(p2,n2),0)/Cout;
end
endmodule
```

Figure A1. Verilog-A code of the charge pump in Figure 3.

```
`include "constants.vams"
`include "disciplines.vams"
module N_controller(Vtarg,Vdd,dN,G);
        input Vtarg,Vdd;
        inout G;
        output dN;
        electrical Vtarg, dN, G,Vdd;
parameter integer Nmax=10;
parameter real alpha=0,beta=0;
integer i,Nnew=1;
real k[1:Nmax];
real A,B;
analog begin
                @(initial_step) begin
                        for(i=1; i<Nmax;i=i+1) begin
                                A=(alpha+beta)*(2*i+1)+1;
                                B=4*(alpha+beta)*(i*i-1);
                                k[i]=(i+1)-0.5*sqrt(A*A+B)+0.5*A;
                        end
                end
        for(i=1; i<Nmax;i=i+1)begin
                if(k[i]*V(Vdd,G)<V(Vtarg,G)) Nnew=i+1;
        end
        if(V(Vtarg,G)<k[1]*V(Vdd,G)) Nnew=1;
        if(Nnew<2) Nnew=1;
        V(dN,G)<+Nnew-1;
end
endmodule
```

Figure A2. Verilog-A code of the adaptive control.

```
module frequency_mod(ref, out, G, fck);
        input ref,out,G;
        output fck;
        electrical ref,out,G,fck,n1;
        parameter real f=100k,fmin=100, fmax=100M;
        parameter real Avco=1 from [1:inf);
        parameter real Kvd=0.1 from (0:1];
        real k;
analog begin
        k=Avco*(V(ref,G)-Kvd*V(out,G));
        if(k<fmin/f-1) k=fmin/f - 1; //case f<fmin
        if(k>fmax/f-1) k=fmax/f - 1; //case f>fmax
V(fck,G)<+k;
end
endmodule
```

Figure A3. Verilog-A code of the frequency-based control.

```
module duty_mod(out,ref,duty,G);
input out,ref,G;
output duty;
electrical out, ref, G, duty;
parameter real duty_max=0.5,duty_min=0.01;
parameter real Apwm=10 from [1:+inf);
parameter real Kvd=0.5 from (0:1];
real k;
analog begin
        k=Apwm*(V(ref,G)-Kvd*V(out,G));
        if(k<2*duty_min-1) k=2*duty_min - 1; //case duty<duty_min
        if(k>2*duty_max-1) k=2*duty_max - 1; //case duty>duty_max
V(duty,G)<+k;
end
endmodule
```

Figure A4. Verilog-A code of the duty cycle-based control.

```
module Vck_mod(out,ref,Vck,G);
input out,ref,G;
output Vck;
electrical out,ref,G,Vck;
parameter real Avm=1 from [1:+inf);
parameter real Vck_min=0.01,Vck_max=1;
parameter real Kvd=0.5 from (0:1];
real k;
analog begin
k=Avm*(V(ref,G)-Kvd*V(out,G));
if(k<Vck_min) k=Vck_min;
if(k>Vck_max) k=Vck_max;
V(Vck,G)<+k;
end
endmodule
```

Figure A5. Verilog-A code of the clock amplitude-based control.

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