

Article

# Analysis of the Input Current Distortion and Guidelines for Designing High Power Factor Quasi-Resonant Flyback LED Drivers

Claudio Adragna<sup>1</sup>, Giovanni Gritti<sup>1</sup>, Angelo Raciti<sup>2</sup>, Santi Agatino Rizzo<sup>3,\*</sup><sup>(D)</sup> and Giovanni Susinni<sup>3</sup>

- <sup>1</sup> Industrial & Power Conversion Division Application Laboratory, STMicroelectronics s.r.l, 20864 Agrate Brianza (MB), Italy; claudio.adragna@st.com (C.A.); giovanni.gritti@st.com (G.G.)
- <sup>2</sup> Istituto per la microelettronica e microsistemi, Consiglio Nazionale Delle Ricerche, 95121 Catania, Italy; angelo.raciti@dieei.unict.it
- <sup>3</sup> Department of Electrical, Electronic and Computer Engineering, University of Catania, 95125 Catania, Italy; giovanni.susinni@unict.it
- \* Correspondence: santi.rizzo@unict.it; Tel.: +39-095-738-2308

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**Abstract:** Nowadays, LED lamps have become a widespread solution in different lighting systems due to their high brightness, efficiency, long lifespan, high reliability and environmental friendliness. The choice of a proper LED driver circuit plays an important role, especially in terms of power quality. In fact, the driver controls its own input current in addition to the LED output current, thus it must guarantee a high power factor. Among the various LED drivers available on the market, the quasi-resonant (QR) flyback topology shows interesting benefits. This paper aims at investigating and analyzing the different issues related to the input current distortion in a QR flyback LED driver. Several effects, such as the distortion caused by the ringing current, crossover distortion due to transformer leakage inductance and crossover distortion due to the input storage capacitor have been experimentally reported. These effects, not previously studied for a high power factor (Hi-PF) QR flyback, have been analyzed in depth. Finally, some practical design guidelines for a Hi-PF QR flyback driver for LED applications are provided.

**Keywords:** converter control; solid-state lighting; power factor correction; Total Harmonic Distortion; primary sensing regulation; flyback; LED lamp

# 1. Introduction

Nowadays, almost a fifth of global electricity consumption is reserved for the lighting system [1]. As an example, in the USA, more than 200 billion kWh each year are expected for lighting systems, and the forecast confirms that the demand is going to increase in the next decade [2]. Traditional lighting equipment, such as incandescent lamps, florescent lamps and tungsten lamps, are environmental unfriendly, due to low efficiency or, in some cases, due to toxic substances that may contribute to the increase in ambient pollution levels [3]. In order to deal with these issues, many governments have already forbidden the trade of incandescent lamps and, on the other hand, encouraged the employment of light-emitting diodes (LEDs). They have been widespread both in private and public lighting systems thanks to their high luminous efficacy, long lifespan, high reliability and environmental friendliness [4]. Generally speaking, a LED lamp can be thought of as a combination of LED semiconductor materials and a driver circuit, thus the choice of the LED driver circuit plays a fundamental role from a power quality point of view. In fact, the driver controls both the LED output current and its own input current. Consequently, it must guarantee a high power factor (PF), and an input current with low total



harmonic distortion (THD) [5,6]. Of course, it is worth remembering that LED lamps must comply with the national and international standards and regulations concerning harmonic currents, such as the standard IEEE-Std-519 and the IEC 61000-3-2.

LED drivers can be roughly grouped into "passive" drivers, since they use only passive components, and "switching" drivers, where there is at least a controllable power switch (e.g., a MOSFET) [7,8]. To further improve the quality of the switching LED drivers, a linear regulator could be added in series to the LEDs array. The linear regulator almost provides a dc output voltage and therefore, it eliminates the low frequency current ripple. Unfortunately, the aforementioned solution increases both the cost and worsens the efficiency.

The main drawback of passive LED drivers is the low PF that often cannot comply with the standard limit. Instead, switching LED drivers can realize a better output current regulation and higher power density, and they are more capable of satisfying the standard limits. Generally, there is a wide variety of LED driver topologies depending on the different power ranges. Furthermore, the topology of the driver can also be selected according to other requirements, including cost, galvanic isolation and efficiency.

The most common switching LED driver topologies for low and medium power applications are mainly based on single-stage (SS) or two-stage (TS) LED architectures. A SS LED driver consists of a dc-dc converter with constant output current regulation that also acts as a power factor correction (PFC). The SS LED drivers can be classified on the bandwidth of the feedback control systems. In the case of a narrow bandwidth (e.g., boost, buck-boost and flyback) the storage capacitor must be located at the output of the converter, otherwise it is placed between the two semi-stages (such as quadratic topologies) [9–11]. Although, the TS drivers consist of two power stages, where the first one acts as a PFC and the second stage performs output current regulation.

Focusing on the SS drivers, one of the main drawbacks is the bulky storage capacitor that also affects both the reliability and the size of the overall system. A PFC topology is usually adopted in the dc-dc stage to obtain high PF, and such a dc-dc stage is also responsible for setting the desired output current. In many of these applications, the power switches and control units are shared and embedded together to ensure a high reliability, efficiency and fast dynamics [12–14]. The reduction in the cost and size of the electronic ballast are additional benefits.

The flyback converter is the most used SS LED driver because it obtains high step-down ability and it provides a good tradeoff among the power quality, the cost, the capacitor size and the efficiency. In integrated lighting applications, a SS discontinuous current conduction mode (DCM) flyback PFC converter is commonly used to drive the LED lamps in order to achieve a high PF. The task is performed by means of a simple circuit configuration used to regulate the lamp current. A flyback LED driver operating in DCM where the PFC proprieties can be easily obtained has been frequently adopted. In this context, the quasi-resonant (QR) flyback LED drivers can effectively reduce the transformer size and weight thanks to the high switching frequency [15], which is not fixed since it increases as the load decreases. Furthermore, the switching losses can be strongly reduced by adopting zero voltage switching (ZVS).

This work aims at investigating and analyzing the different issues due to the input current distortion in a high power factor (Hi-PF) QR flyback LED driver. The THD performance of the whole converter is the result of the correlation of several causes such as the ringing current, crossover distortion due to transformer leakage inductance and crossover distortion due to the input storage capacitor. The input current distortion caused by the ringing current has been widely studied for the boost converter, while—as far as the authors know—it is the first time the problem has been studied for the QR flyback. Moreover, the crossover distortion due to the input storage capacitor in the case of a Hi-PF flyback LED driver has never been treated in literature. Finally, an accurate analysis is performed in this paper by considering the linear approximation of the input voltage and the related comparison with a sinusoidal waveform.

The paper is organized as follows: In Section 2, a classification of several LED drivers is introduced, and their main characteristics are discussed. The main issues related to input current distortion in a Hi-PF QR flyback converter are discussed in Section 3. In Section 4, some practical design guidelines for a Hi-QR flyback driver for lighting applications will be discussed, along with a few experimental results.

# 2. Brief Overview of LED Driver Topologies

In this section, various topologies of passive and switching LED drivers are described and classified. The passive drivers are simpler and more reliable and they operate at the line frequency. No active control is developed, so a significant current ripple can occur. The switching drivers can strongly reduce the current distortion and improve the PF with the additional advantage of being suitable for high frequency operations, thus enabling reduced size. On the other hand, switching LED drivers are less reliable than passive ones.

#### 2.1. Passive LED Drivers

Passive LED drivers are characterized by the exclusive use of passive components (e.g., resistors, capacitors, magnetic components). The insertion of an impedance between the ac line and the LED lamp load to limit the current is mandatory. One of the main drawbacks of these topologies is the low PF and high THD, which are sometimes not enough to meet the standards [16].

Passive LED drivers can be classified into lossy and lossless impedance drivers. The strength and simplicity of the lossy impedance driver is due to the use of a resistor  $R_L$  or a linear regulator on the dc side, as depicted in Figure 1. In many practical applications, it is widespread to use a bulky step-down transformer from high to low voltage. It has two-fold benefits—it reduces the voltage drop on the resistor with an increase in the overall system efficiency and, at the same time, guarantees galvanic isolation. A large electrolytic capacitor  $C_S$  is typically used in order to avoid flickering.



Figure 1. Typical application of a passive "lossy" LED driver.

A passive driver with a lossless impedance (an inductor, capacitor or their combinations), usually placed in the ac side to limit the LED output current, is shown in the example in Figure 2. An inductor  $L_{in}$  is usually adopted with the aim of replacing the less efficient and low-frequency transformer. The  $L_{in}$  usually behaves as an additional input filter (by means of  $C_{in}$ ) which smooths the input current and leads to advantages such as reducing the input current distortion [17–19]. Instead of using a bulky electrolytic capacitor (E-CAP) that ensures a constant output current, a non-E-CAP is often used on the dc side, still achieving a higher PF with respect to the lossy counterpart. This solution can ensure a longer lifetime and smaller size of the overall system, although there is a small output current ripple in the LED load. Notwithstanding, lossless passive drivers can reach high efficiency, above 90% [18].



Figure 2. Typical application of a passive "lossless" LED driver.

Passive drivers can be easily employed in outdoor applications and they are very cost effective, especially for low-power applications. The main drawbacks of passive LED drivers are their lack of a proper output current control and their having an input current THD that does not always meet the standards target.

## 2.2. Switching LED Driver

Switching LED drivers bring various advantages arising from the use of the switching devices. Moreover, switching LED drivers can embed into a single electronic ballast with various functionalities, such as circuit fault protection and active and high PFC [20]. They are especially employed in indoor applications, since the whole circuit control is compact, reliable and effective with a low and controllable ripple output current. Another strength point of switching LED drivers is their higher efficiency in comparison to the passive ones. Switching LED driver topologies can be classified into two main categories, SS and TS, as shown in Figure 3. The SS drivers consist of a single power stage that acts as both a dc-dc regulator and PFC, shown in Figure 3a, with a storage capacitor  $C_s$ . On the other hand, the TS drivers are used for high-power applications. The aforementioned drivers comprise two power conversion stages that can perform different functions. In general, the first stage acts as a PFC and the second one as a dc-dc regulator and filter [21], as depicted in Figure 3b.



Figure 3. (a) SS switching LED driver topology. (b) TS switching LED driver topology.

In the following section, there is a brief focus on SS LED drivers with the main advantages of different topologies adopted in the literature.

SS drivers usually have a low component count and among them a power switch that controls a power conversion stage. However, it is often difficult for a SS driver to simultaneously ensure good performance in many respects, such as high efficiency, high PF, constant current output and so on. SS drivers are suitable for low and medium power class applications (below 70 W) where size and cost are usually more critical than PF and efficiency. The storage capacitor is usually placed downstream from the dc-dc converter, that is on the high frequency side, as shown by the red capacitor in Figure 4, to obtain a high PF. Notwithstanding, another approach can be found in some embedded LED drivers where the capacitor is placed on the low frequency side, as shown by the blue capacitor in

Figure 4. More specifically, such an approach has sometimes been used in very low power applications (below 5 W) [22]. Indeed, nowadays, in this power range, passive LED drivers are adopted to guarantee an inexpensive cost. Figure 5a shows the waveforms of the current drawn by LED lamps when the capacitor is placed on the low and high frequency side. The waveforms confirm that the dc-dc converter can guarantee PFC only when the storage capacitor is placed downstream from the dc-dc converter itself. Although the input current drawn by the LED lamp has a better THD when the capacitor is placed at the high frequency side, a higher output current ripple occurs in comparison to the previous solution, as shown in Figure 5b. However, the required storage capacitance is not always able to handle both the low and the high frequency ripple [23].



**Figure 4.** Switching-mode single-stage driver: depending on the position of the capacitor *Cs*, the single dc-dc converter can provide both PFC and output current regulation.



**Figure 5.** Simulation of the current  $I_{ac}$  drawn by the LED lamp (**a**), and the output LED load current  $I_{LED}$  (**b**). The blue represents the case when the storage capacitor is directly connected on the low frequency side and the red on the high frequency side.

The SS LED drivers can be roughly classified on the bandwidth of the feedback control systems. In the case of a narrow bandwidth (e.g., boost, buck-boost and flyback) the storage capacitor must be located at the output of the converter. Instead, in the case of a wide bandwidth system (e.g., quadratic or single-stage single-switch input current shaper topologies) the storage capacitor is placed between the two semi-stages. In the following, the narrow bandwidth systems have been analyzed. In detail, a huge number of conventional LED drivers are widely discussed in literature, such as buck [24–26], buck-boost [27], SEPIC [28,29], flyback [30,31], half-bridge [32–34] and push-pull converters [35,36]. Furthermore, PFC can be achieved with valley-fill circuits [37]. Other approaches, such as coupled-inductor modified converters [38–41] and valley-fill modified converters [42], show a simple solution to the step-down ratio requirement without compromising the efficiency and system complexity.

The flyback converter has been widely adopted in LED driver lamps because of its simple structure and high PF. One of the strengths is its efficiency, which can be improved by using the leakage energy or using soft-switching techniques [43]. In spite of the flyback LED driver having various advantages, in many practical applications the QR mode operation has become one of the most familiar methods in LED driver applications. It is worth noting the decrease in switching losses with respect to a flyback converter operated with a fixed frequency. Moreover, the QR driver has an enhanced transient response in DCM operation [44,45] and it may have a smaller EMI filter [46]. In fact, in applications operated from the mains, the switching frequency is modulated at twice the mains frequency due to the voltage ripple appearing across the input capacitance. The switching frequency span depends on the amplitude of this input voltage ripple. This causes the spectrum to be spread over some frequency bands, rather than being concentrated on single frequency values.

In addition, the QR driver has a higher safety degree under short circuit conditions, since the switch is not enabled until the primary windings are fully demagnetized. Therefore, transformer saturation is not possible. On the other hand, the QR flyback LED driver may have a high ripple output current and high conduction losses in comparison to the fixed frequency driver.

It is important to point out that the difference between a DCM flyback and a QR flyback is in the turn-on mechanism. In a DCM flyback converter, the gate driver provides a constant switching frequency, while in a QR flyback a variable frequency is used, where the off time depends on the resonant valley detection of the drain-to-source voltage ringing that follows transformer demagnetization. Figure 6 depicts the drain-to-source voltage waveforms in the case of a DCM flyback, shown in Figure 6a, and a QR flyback, shown in Figure 6b, thus highlighting the benefit in terms of reduced switching losses.



Figure 6. Drain to source voltage waveforms for a DCM flyback (a), and a QR flyback (b).

A simplified schematic of a QR flyback LED driver (not for Hi-PF applications) is shown in Figure 7. The primary current  $I_p$  starts to flow into  $L_p$  when the power switch is turned on. The voltage at the secondary is such that the diode is reverse biased, hence the capacitance  $C_{out}$  supplies the LED string. Once the switch is turned off, the current  $I_p$  goes to zero and the voltage across both windings reverses, so that the output diode is forward-biased. Then, the current starts flowing in the secondary winding and  $C_{out}$  can be charged by the energy stored in the transformer. It is worth noting that, while the current flows on the secondary side, the drain-source voltage is equal to the rectified input  $V_{in}(t)$  plus the reflected output voltage  $V_R$  at the primary windings. The transformer takes a time  $T_{FW}$  to demagnetize, and as soon as the energy transfer is completed, the drain-source voltage starts ringing. The main reason for this energy exchange phenomenon is due to a resonant tank between the inductance  $L_{pp}$  and the capacitance  $C_{pp}$ . The inductance  $L_{pp}$  is the sum between the leakage inductance of the copper paths and the primary winding  $L_p$ . The latter it is the prevalent contribution, hence  $L_{pp}$  can be simply approximated as  $L_{p}$ . The capacitance  $C_{pp}$  can be expressed as the sum of the parasitic capacitances on the primary circuit and the capacitances of the secondary circuit referred to the primary one. The latter are due to the parasitic capacitances of the secondary circuit and to the output capacitance Cout. The primary circuit capacitance includes various contributions: the output parasitic capacitance  $C_{oss}$  of the MOSFET; the junction capacitance of the diode; the package capacitance; the intra-winding capacitance of the transformer; plus other stray contributors together and so on [47–51].  $C_{oss}$  is a strongly nonlinear capacitance and, especially in the latest MOSFET generations, it increases dramatically (100 times or more) when the drain–source voltage,  $v_{DS}$ , falls below few tens volt; i.e.,  $C_{pp}$  is a function of  $v_{DS}$ :  $C_{pp}(v_{DS})$ . In the following, this capacitance will be considered constant or, at least, not significantly impacting the overall  $C_{DS}$ . Hence, the resonant frequency  $f_r$  can be represented as:

$$f_r = \frac{1}{2\pi \sqrt{L_{pp}C_{pp}(v_{DS})}} \approx \frac{1}{2\pi \sqrt{L_pC_{DS}}}$$
(1)



Figure 7. QR resonant flyback valley-switching.

In applications, the inductance  $L_p$  is measured with an impedance meter or by measuring the di/dt when a voltage square wave is applied, while  $C_{DS}$  is esteemed by Equation (1) from the measurement of the drain–source voltage ringing.

Bearing in mind that, in a conventional QR topology a feedback voltage loop is used, and this loop controls the average value of the secondary current  $I_s$ , it follows that the switching frequency is continuously adjusted depending on the output current load. In this way the switching device turns on when necessary, provided that the inner controller is able to detect a valley in the ringing drain–source voltage. The switching period *T* can be expressed as:

$$\begin{cases} T = T_{on} + T_{FW} + T_{ring} \\ T_{ring} = \frac{1}{2} [1 + 2(k - 1)] T_r \end{cases}$$
(2)

where  $T_{on}$  is the on time of the power switch,  $T_{FW}$  is the time interval where the current flows on the secondary side and  $T_{ring}$  is the time interval during which the drain–source voltage rings.  $T_{on}$  is reduced as the load reduces, hence at very light load the frequency is high. Therefore, the maximum switching frequency imposes a minimum  $T_{on}$ . In this case, a further load reduction involves an increment of  $T_{ring}$ . In detail,  $T_{ring}$  strictly depends on the load level and it is imposed by keeping off the switch for some valley points in the drain–source voltage. In other terms, it depends on the number of the valley points k "skipped" by the controller. More specifically, k increases as the load level decreases. The term k is equal to 1 until  $T_{on}$  is greater than its minimum value, i.e. the switch is turned on at the fist valley on the drain–source voltage waveform (one-half of the resonant period). Thus, the QR mode operation of the converter represents the condition k = 1.

The reason behind the turn-on during a valley point of the drain–source voltage is the achievement of lower capacitive switching losses:

$$E_s = \frac{1}{2}C_{DS}V_{DS}^2 \tag{3}$$

This mechanism is able to minimize in a significant way the switching losses. It is worth noting that the bill of material of a QR driver contains only a few simple components, which implies an inexpensive solution [51,52].

Finally, Figure 8 compares the performance between a QR flyback, a buck-boost and a hybrid solution [36–49] in terms of some key factors. The high step-down ability (HSDA) [36–38], efficiency (EFF) [38–41], compact capacitor volume (CAP) [42], cost (COST) [43–46] and low power range applications (LP) [47,48] have been taken into account for the three converters. The comparison highlights the superior performance of the QR flyback converter, which makes it the preferred choice for LED driver applications.



**Figure 8.** Performance of three main SS LED driver topologies: high step-down ability (HSDA), efficiency (EFF), reduced capacitor (CAP), cost (COST) and low power applications (LP).

#### 3. Analysis of Input Current Distortion due to Power Processing and Power Circuit

## 3.1. Generic Control Method Obtaining High Power Factor

Although the QR flyback converter topology is extremely popular since it is a very cost-effective solution with high performance, the converter features inherent distortion of the input current [48]. Normally, this distortion is not a concern for compliance with the IEC61000-3-2, however, some input current THD targets (e.g., <10% at full power) are becoming market requirements that are very difficult to achieve, especially when working with lighting equipment over 25 W [53].

As shown in Figure 7, the storage capacitor of the QR flyback is placed on the low frequency side of the dc-dc converter. With the aim to reduce the input current THD, the capacitor should be placed downstream from the converter, according to the waveform simulations in Figure 5a (red trace) related to the capacitor position of Figure 4. In this perspective, the converter can be considered as a Hi-PF QR flyback, which has a rectified voltage in input and the storage capacitor downstream of the power stage. The aforementioned solution strongly reduces the harmonics distortions of the input current drawn by the LED lamp.

The control gear in a Hi-PF QR flyback converter has a twofold task: firstly, it is responsible for regulating the output voltage or current and, simultaneously, it has to maintain a low THD of the input current. For the sake of completeness, the characteristics and proprieties of the control method that have to be considered to achieve a Hi-PF QR flyback converter will be briefly discussed.

The control method, shown in Figure 9, is responsible for the turn on and turn off of the switch.

Henceforth, the quantities depending on the instantaneous line voltage will be considered as a function of the term  $\theta = 2\pi f_{line}t$ .

The target of the control method is to obtain an input current very similar to a sinusoid in-phase with the input voltage to achieve high-PF. Regardless of the specific control method, the previous target can be partially converted into obtaining a primary current, as shown by  $I_p$  in Figure 7, whose peak envelope, detailed by the green elements in Figure 9, leads to a sinusoid in-phase with the input voltage. To obtain such an envelope, the control method must turn off the switch when the current

on the primary side reaches one of the (green) peaks in Figure 9. To obtain a similar result for the secondary current, shown by the red elements in Figure 9, a similar control must be adopted for the switch turn on. The turn on must occur when the transformer is fully demagnetized, thanks to a zero-current detector. In other terms, the combination of these switching rules, which result in a variable switching frequency, shown in Figure 9, ensures that the peaks of the primary current, in a half period of the rectified voltage  $V_{in}(\theta)$ , can be enveloped by a rectified sinusoid. The primary current  $I_p(\theta)$  in a switching cycle is triangular shaped and flows only during the switch on-time, as sketched by the green triangles shown in Figure 9. During the off time, the secondary current  $I_s(\theta)$  flows and it is represented by the red triangles. Therefore, the switching frequency SW is variable, where the  $T_{ON}(\theta)$  and  $T_{OFF}(\theta)$  are modulated to achieve a sinusoidal current envelope.



Figure 9. Primary and secondary currents in a QR-controlled Hi-PF flyback converter.

However, the primary current  $I_p(\theta)$  flows only during the on-time of the power switch, and this means that the average value of the primary current deviates significantly from an ideal sinusoid. To ensure good performance and low THD input current for a Hi-PF driver LED, the quantity  $D^2T$  (*D* is the duty ratio) must be constant along each line half-cycle, thus a unity PF is obtained [54].

In this paper, it is assumed that the generic control method implements the previous features. For the sake of simplicity to obtain a quantitative expression of the input current  $I_{in}$ , the following assumptions have been considered:

- 1. The line voltage is sinusoidal, and the input bridge rectifier is ideal, thus the voltage at the bridge output terminal is a rectified sinusoid.
- 2. The voltage drop across the power switch in the on-state is negligible and there is negligible energy accumulation on the dc side of the bridge.
- 3. The transformer windings are perfectly coupled (i.e., no leakage inductance).
- 4. The turn-off transient of the power switch has negligible duration so that  $T_{FW}$  immediately follows  $T_{ON}$ .
- 5. The converter is operated so the power switch is turned on in each cycle after the secondary current becomes zero, therefore in either QR-mode (i.e., on the first valley of the ringing in the drain–source voltage) or DCM.
- 6. The output voltage is constant along a line half-cycle.
- 7. During the time interval elapsing from the instant when the transformer demagnetizes to the instant when the power switch is turned on, the transformer current is zero; consequently, the initial current during the on-time is zero too. This time interval is equal to  $T_r/2$  in the case of the converter being used in QR mode.

It is worth generalizing the relation to  $D^2T$  when a variable switching frequency is used, in particular:

$$D^{2}T = \left[\frac{T_{ON}(\theta)}{T(\theta)}\right]^{2}T(\theta) = \frac{T_{ON}(\theta)^{2}}{T(\theta)} = \text{constant}$$
(4)

where the dependences of  $T_{ON}$  and T on  $\theta$  point out that they are a function of the instantaneous line voltage  $V_{ac}$ . Assuming that the rectified voltage  $V_{in}$  is sinusoidal in  $0 \le \theta \le \pi$ , according to assumption 1, it can be written as:

$$V_{in}(\theta) = V_{in,pk}\sin(\theta) \tag{5}$$

where  $V_{in,pk}$  is the amplitude of the rectified voltage.

By considering the current flowing in the primary windings during the time interval  $T_{ON}$ , and bearing in mind the inductance current–voltage differential relation, the peak value of primary current  $I_{pkp}(\theta)$  can be expressed as:

$$I_{pkp}(\theta) = \frac{1}{L_p} \left( V_{in,pk} \sin(\theta) \right) T_{ON}(\theta)$$
(6)

The generic control method must ensure that the height of the triangles depicted in Figure 9 varies along a line cycle as expressed by Equation (6). To reach this target, the control method must properly vary the width of  $T_{ON}(\theta)$  as well as  $T_{OFF}(\theta)$ . The input current  $I_{in}(\theta)$  is the average value of each triangle over a switching cycle, hence, taking Equation (6) into account:

$$I_{in}(\theta) = \frac{1}{2} I_{pkp}(\theta) \frac{T_{ON}(\theta)}{T(\theta)} = \frac{1}{2L_p} \left( V_{in,pk} \sin(\theta) \right) \frac{T_{ON}(\theta)^2}{T(\theta)}$$
(7)

It is worth noting that, if the ratio  $T_{on}(\theta)^2/T(\theta)$  is maintained constant by the controller, the input current  $I_{in}(\theta)$  can be assumed sinusoidal. Figure 10 summarizes the key current waveform in the Hi-PF driver LED.



**Figure 10.** Current waveforms of the circuit in Figure 7: line cycle time scale of the primary current  $I_p$ , secondary current  $I_s$ , input rectified current  $I_{in}$  and current in the ac side  $I_{ac}$ .

Despite the fact that a suitable control method leads to a Hi-PF QR flyback driver according to the previous features, there are different inherent causes of distortion in the input current to be faced. The distortion due to these causes is reported in the next section where the THD has been experimentally evaluated. After that, in the following subsections, these causes, due to the power processing mechanism of the QR flyback converter that are not ascribable to the specific control method (although the control method may mitigate them), are described.

#### 3.2. Experimental Verification of the Input Current Distortion in a Hi-PF QR Flyback LED Driver

A prototype of a Hi-PF QR flyback LED driver was set up to highlight the distortion occurring, even when a control method implementing the previous features is adopted. The main parameters of the converter are summarized in Table 1.

Parameter	Value
Input voltage range $[V_{ac}]$	90–265 V
Line frequency range $[f_l]$	47–63 Hz
Rated output voltage [Vout]	48 V
Regulated dc output current [I <sub>out</sub> ]	700 mA
Expected full-load efficiency $[\eta]$	86%
Transformer primary inductance $[L_p]$	500 µH
Reflected voltage $[V_R]$	120 V
Drain–Source capacitance [C <sub>DS</sub> ]	150 pF

Table 1. Main characteristics of the Hi-PF QR flyback converter.

The prototype was built and its performance evaluated on the bench. The PF was greater than 0.98 over the input voltage range at full load. At 50% load, at low line it was nearly equal to that at 100% load, but at high line it dropped to about 0.97 at 230  $V_{ac}$ . Figure 11 depicts the experimental waveforms of the input current  $I_{ac}(\theta)$  (blue trace), the output voltage (red trace), the drain current of the MOSFET (green trace) and the current sense voltage reference for the controller (purple trace). The measurements were carried out at full load both at 110  $V_{ac}$  (60 Hz) and 230  $V_{ac}$  (50 Hz). From the experimental evidence, the shape of the measured  $I_{ac}(\theta)$  was very close to an ideal sinusoid waveform. It is worth noting that the harmonic contribution the prototype boards met the European norm EN61000-3-2 Class-C and Japanese norm JEITA\_MITI Class-C, both of which are relevant to lighting equipment, at full load and nominal input voltage mains, as depicted in Figure 11.

A small distortion in the input current is apparent in Figure 11 (blue trace) by looking at the zero crossing of the waveform. Therefore, as previously mentioned, notwithstanding the enhanced performance of a Hi-PF QR flyback LED driver, there are still different inherent causes of distortion in the input current that are not ascribable to the specific control method. The causes are the ringing current, the crossover distortion due to transformer leakage inductance and crossover distortion due to the input storage capacitor. Generally speaking, being the converter in a nonlinear system, the overall THD of the input current cannot be the sum of each individual distortion contribution. Due to the number and the complexity of the distortion causes and, above all, due to the complexity of their mutual multi-interactions, the only way to have a sensible estimate of the overall result in terms of input current THD is to resort to simulations.

It is worth noting that the distortion of the input current  $I_{ac}(\theta)$  caused by the ringing effect has already been studied theoretically for boost PFC [55–57], while in the case of a Hi-PF QR flyback it has not yet been treated. Furthermore, the crossover distortion due to the input storage capacitor in the case of a Hi-PF flyback LED driver has never been studied. Finally, the crossover distortion due to transformer leakage inductance has also been theoretically analyzed in depth.



**Figure 11.** Steady-state waveforms at full-load: (a)  $V_{in} = 110$  V at 60 Hz. (b)  $V_{in} = 230$  V at 50 Hz. They have been overlapped by the harmonic contributions of the input current (green bars) with the Japanese norm JEITA\_MITI Class-C (a), and European norm EN61000-3-2 Class-C (b) (red bars) for lighting equipment.

## 3.3. Distortion Caused by the Ringing Current

In a flyback, the drain-to-source voltage rings as soon as the secondary winding is fully demagnetized. The energy is exchanged between the total capacitance  $C_{DS}$  of the drain node and the primary inductance of the flyback transformer  $L_p$ . For the sake of simplicity, assumption 3 has been assumed, and consequentially it has been carried out an equivalent circuit of the QR flyback during the time interval  $T_{neg}$ , which is the duration of the negative portion of the primary current,  $I_p$ . The duration of the positive portion,  $T_{pos}$ , of the primary current is equal to  $T_{ON}$  when the current in the turn-on instant of the power switch is zero. The simplified circuit model and the key waveforms are depicted in Figure 12.

In Figure 12a, the voltage across  $L_p$  is equal to the reflected output voltage  $V_R$ , which is almost constant during  $T_{FW}$ , according to the previous assumption 6. After that, the voltage across  $L_p$  and  $C_{DS}$  and the current trough them start to oscillate. More specifically, the analytical expressions of  $V_{DS}(t)$  and  $I_p(t)$  in the time interval  $T_{neg}$ , can be written as:

$$V_{DS}(t) = \begin{cases} V_{in}(t) + V_R \cos(2\pi \frac{t}{T_r}) & 0 < t \le T_z \\ 0 & T_z < t \le T_{neg} \end{cases}$$
(8)

$$I_p(t) = \begin{cases} -Y_L V_R \sin\left(2\pi \frac{t}{T_r}\right) & 0 < t \le T_z \\ I_p(T_z) + \frac{V_{in}}{L_p}t & T_z < t \le T_{neg} \end{cases}$$
(9)

$$Y_L = \sqrt{\frac{C_{DS}}{L_p}} \tag{10}$$

where  $Y_L$  is the characteristic admittance of the  $C_{DS}$ - $L_p$  tank circuit and  $T_z$  is the time interval needed for the  $V_{DS}$  to fall zero when  $V_{in} < V_R$ ; that is:

$$V_R \cos\left(2\pi \frac{T_z}{T_r}\right) = -V_{in}(T_z) \tag{11}$$

When QR-mode is adopted, the device can be turned on, but according to assumption 5, the current must reach zero.  $T_{zz}$  is the time interval needed for the primary current  $I_p$  to ramp linearly until zero from the current value  $I_p(T_z)$ . In DCM operation, considering that  $I_p$  oscillates around zero, and that ringing is damped, after a few ringing cycles, assumption 7 can be considered exactly true; with QR operation, the negative current just after demagnetization is not compensated by subsequent positive contributions as in DCM. Considering zero the average value of  $I_p$ , as per assumption 7, is already a better approximation as compared to totally neglecting  $T_R$  (i.e., assuming the operation is exactly at the boundary between DCM and CCM). However, in this context, assumption 7 is just a simplification, whose impact on the shape of the input current, quantitatively expressed by its THD, needs to be assessed. Being the ringing current at the turn-on instant of the power switch equal to the initial current during the on-time interval, this current may or may not be zero, which has an impact on the shape of the input current may or may not be zero, which has an impact on the shape of the input current may or may not be zero, which has an impact on the shape of the input current may or may not be zero, which has an impact on the shape of the input current may or may not be zero, which has an impact on the shape of the input current may or may not be zero, which has an impact on the shape of the input current and, consequently, on its THD too.

When  $V_{in} > V_R$ , in QR-mode, the turn on occurs at the first valley of the ringing in the drain voltage that follows the transformer demagnetization. Therefore, in this case,  $T_{neg}$  is equal to  $T_r/2$ .



**Figure 12.** (a) Simplified equivalent circuit during  $T_{neg}$ , (b) key waveforms in QR-mode and DCM operations.

By neglecting the input capacitor  $C_s$  from the QR flyback schematic in Figure 7, the following considerations are valid: during  $T_{on}$  a charge  $Q_{pos}$  is provided from the input source and stored in the transformer; during  $T_{FW}$ , the energy is mostly delivered to the output; finally, in  $T_{neg}$ , a negative charge  $Q_{neg}$  is returned to the input source. The average input current during a switching cycle can therefore be expressed as:

$$\left\langle I_p \right\rangle = \frac{Q_{pos} - Q_{neg}}{T} \tag{12}$$

As shown in Figure 9, the positive charge  $Q_{pos}$  is clearly given by:

$$Q_{pos} = \frac{1}{2} I_{pkp} T_{on} \tag{13}$$

To evaluate the absolute value of the negative charge  $Q_{neg}$ , it is necessary to consider Equations (8)–(10), that describe the  $V_{DS}(t)$  and  $I_p(t)$  variations in the time interval  $T_{neg}$  (when QR operation is only considered) and distinguish two cases.

1.  $V_{in} > V_R$ . In the time interval (0,  $T_{neg}$ )  $V_{DS}(t)$  is always greater than zero and the current  $I_p(t)$  is sinusoidal;  $T_{neg}$  equals half the ringing period. The average value of  $I_p(t)$  during  $T_{neg}$  is  $2/\pi$  times the negative peak value  $|I_{vyp}| = Y_L V_R$ , therefore:

$$Q_{neg} = T_{neg} \frac{2}{\pi} Y_L V_R = \frac{T_r}{\pi} Y_L V_R = 2V_R C_{DS}$$
(14)

2.  $V_{in} \leq V_R$ . The current  $I_p(t)$  is sinusoidal in the subinterval (0,  $T_z$ ).  $T_z$  can be expressed as:

$$T_{z} = \frac{T_{r}}{2} \left( 1 - \frac{1}{\pi} \cos^{-1} \left( \frac{V_{in}}{V_{R}} \right) \right)$$
(15)

and the current Ip(t) evaluated when t = Tz is:

$$I_p(T_z) = -Y_L V_R \sqrt{1 - \left(\frac{V_{in}}{V_R}\right)^2}$$
(16)

As depicted in Figure 12b, in the time interval  $T_{zz}$ ,  $I_p(t)$  ramps up linearly to zero. Hence,  $T_{zz}$  can be expressed as:

$$T_{zz} = \frac{L_p}{V_{in}} \left| I_p(T_z) \right| \tag{17}$$

Since  $T_{neg}$  is the sum of  $T_z$  and  $T_{zz}$ , it can be written:

$$T_{neg} = T_z + T_{zz} = \frac{T_r}{2} \left[ 1 + \frac{V_R}{V_{in}} \sqrt{1 - \left(\frac{V_{in}}{V_R}\right)^2} - \cos^{-1}\left(\frac{V_{in}}{V_R}\right) \right]$$
(18)

which is always greater than  $T_r/2$ , except when  $V_{in} = V_R$ . Finally,  $Q_{neg}$  is given by the sum of the two contributions,  $Q_{neg1}$  during the subinterval (0,  $T_z$ ) and  $Q_{neg2}$  during the subinterval ( $T_z$ ,  $T_{neg}$ ). After some mathematical steps,  $Q_{neg}$  can be evaluated as:

$$Q_{neg} = Q_{neg1} + Q_{neg2} = \int_0^{T_z} Y_L V_R \cos\left(2\pi \frac{t}{T_r}\right) dt + \int_{T_z}^{T_{neg}} I_p(T_z) + \frac{V_{in}}{L_p} t dt = \frac{1}{2} C_{DS} \frac{\left(V_{in} + V_R\right)^2}{V_{in}}$$
(19)

Considering Equation (12), the overall input current  $I_{in}(\theta)$  can be found by adding the contributions obtained in Equations (7) and (13), which also takes into account the ringing oscillations along each line half-cycle. Hence it can be written as:

$$I_{in}(\theta) = \begin{cases} \frac{1}{2}I_{pkp}(\theta)\frac{T_{on}(\theta)}{T(\theta)} - \frac{2}{T(\theta)}V_RC_{DS} & V_{in} > V_R\\ \frac{1}{2}I_{pkp}(\theta)\frac{T_{on}(\theta)}{T(\theta)} - \frac{1}{2T(\theta)}\frac{(V_{in}+V_R)^2}{V_{in}}C_{DS} & V_{in} \le V_R \end{cases}$$
(20)

It is evident that the positive term in Equation (20) does not introduce any distortion, provided that the generic control method provides  $I_{pkp}(\theta)$ , as in Equation (6), and satisfies Equation (4). The contribution of the ringing current, related exclusively to the negative terms, takes into account

the ringing contributions derived in Equations (14) and (19). They represent a twofold effect: they downwards offset the input current waveform, which produces crossover distortion and, considered that the offset is a function of the instantaneous line voltage, they distort its shape as well. It is worth noting that the distortion contribution is not ascribable to the control method; that is, it is not due to the control but is inherent in the power processing mechanism of any Hi-PF QR flyback converter. On the other hand, the control method may compensate or mitigate it. First of all, the contribution of the ringing current can be reduced by lowering the switching frequency (i.e., a longer  $T(\theta)$ , obtained with a larger  $L_p$  value) and using a low reflected voltage  $V_R$ . However, a larger  $L_p$  value implies a bigger flyback transformer, and a lower  $V_R$  increases the primary *rms* current and, consequently, the conduction losses. A trade-off is therefore required. A smaller  $C_{DS}$  also helps to reduce the ringing contribution, however, it is important to underline that a tradeoff between switching losses and EMI should be found. In fact, the lower the  $C_{DS}$ , the faster the  $V_{DS}$  transient at turn-off, and this faster transient may adversely affect both the efficiency of the power switch, as well as the EMI.

LED driver applications are typically specified to accommodate a certain range of output voltages  $V_{out}$  to power different types and lengths of LED string. Thus the contribution of the ringing current is expected to be maximum at the upper end of the  $V_{out}$  range and minimum at the lower end of the  $V_{out}$  range. In fact, lowering  $V_{out}$  will simultaneously reduce  $V_R$  and increase  $T(\theta)$ .

## 3.4. Crossover Distortion Due to the Input Capacitor

The storage capacitor *Cs* placed downstream of the input bridge, as depicted in Figure 7, is part of the EMI filter, which is always needed in an SMPS connected to the power line to restrict the conducted emission within the limits envisaged by the relevant EMI regulations. The capacitor has a twofold effect: it contributes to the voltage–current phase-shift and worsens the THD by maintaining a residual voltage on the dc side of the input bridge rectifier. The latter causes a non-conduction zone as the line voltage approaches zero, therefore, assumption 2 is no longer valid for the following analysis. This phenomenon also occurs for systems without a PFC and is an additional source of crossover itself, which interacts with the other distortion mechanisms. A quantitative analysis of this crossover distortion can be carried out independently from the topology employed in a PFC.

In these terms, any PFC and, consequently, the Hi-PF QR flyback converter can be modeled with an equivalent resistor ( $R_{eq}$ ) that can be expressed as:

$$R_{eq} = \frac{V_{PK}^2}{2P_{in}} \tag{21}$$

where  $V_{PK}$  is the peak of the rectified line voltage  $V_{in}(\theta)$  and  $P_{in}$  is the input power of the converter.

Generally speaking, the dead zone in  $I_{ac}(\theta)$  increases at large  $C_S$  values, high line voltage and low load (large  $R_{eq}$ ). In quantitative terms, the dead zone starts, near the zero-crossing, when the rate of fall in the line voltage  $V_{ac}(\theta)$  exceeds the rate of the voltage  $V_{in}(\theta)$  across  $C_S$ , limited by the time constant  $R_{eq} C_S$ , so that from that instant on it is  $V_{ac}(\theta) < V_{in}(\theta)$ , as shown in Figure 13.

Focusing on the  $V_{ac}(\theta)$  and  $V_{in}(\theta)$  near the zero-crossing zone, shown in Figure 13a, and neglecting the voltage drop across the input bridge rectifier, the phase angle  $\alpha$  at which the slope of the two voltages are equal can be found with the following relation:

$$\left|\frac{dv_{ac}(\theta)}{d\theta}\right| = \left|\frac{dv_{in}(\theta)}{d\theta}\right| \quad \Rightarrow \quad 2\pi f_L V_{PK} \cos \alpha = \frac{1}{R_{eq}C_s} V_{PK} \sin \alpha \tag{22}$$

Solving for  $\alpha$ :

$$\tan \alpha = 2\pi f_L R_{eq} C_s \tag{23}$$



**Figure 13.** Detail of  $V_{ac}(\theta)$  (red trace) and  $V_{in}(\theta)$  (blue trace) near voltage zero-crossing (**a**), and zoomed view of the yellow area, intersection of  $V_{ac}(\theta)$  and  $V_{in}(\theta)$  (**b**). Values are normalized to  $V_{PK}$ .

From  $\pi$ - $\alpha$  on,  $V_{in}(\theta)$  follows an exponential decay until the phase  $\theta$  is equal to  $\pi + \beta$ , where it is again  $|V_{ac}(\theta)| \ge V_{in}(\theta)$ , which marks the end of the dead zone. In this interval the expression of  $V_{in}(\theta)$  can be assumed as:

$$V_{in}(\theta) = \sin \alpha e^{-\frac{\theta - (\pi - \alpha)}{\tan \alpha}}$$
(24)

Beyond the angle  $\pi + \beta$ ,  $V_{ac}(\theta)$  and  $V_{in}(\theta)$  are again both sinusoidal and overlapping until they have a phase shift equal to  $\alpha$  away from the next zero-crossing. The duration of the dead zone is clearly  $\alpha + \beta$ .

The phase angle  $\beta$  can be found at the intersection of an exponential curve with a sinusoidal one, which results in a transcendental equation with no closed-form solution. Since  $\beta$  is small, it is possible to find an approximate solution  $\beta_a$ , substituting the last part of the exponential function (from  $\theta = \pi$  to  $\theta = \pi + \beta$ ) with its expansion in Taylor series to the first order ( $e^{-\theta} \approx 1-\theta$ ). In a similar way it can be done for the rectified sinusoid (*sin*  $\theta \approx \theta$ ). Therefore, the value  $\Lambda$  of the input voltage, evaluated when the phase angle is  $\pi$ , can be computed as follows:

$$\Lambda = V_{in}(\pi) = \sin \alpha e^{-\frac{\alpha}{\tan \alpha}} \approx \frac{\sin \alpha}{e}$$
(25)

As shown in Figure 13b, at the intersection of the two straight lines, the phase angle is  $\pi + \beta_a$ .

$$\begin{cases} V_{in1}(\theta) = \Lambda \left(1 - \frac{\theta - \pi}{\tan \alpha}\right) \\ V_{in2}(\theta) = \theta - \pi \\ \beta_a = \frac{\Lambda \tan \alpha}{\Lambda + \tan \alpha} \end{cases}$$
(26)

The truncation of the exponential Equation (24) to the first order introduces an underestimation, as depicted in Figure 13b, hence Equation (26) provides an approximated value  $\beta_a < \beta$ . On the other hand, if Equation (24) is approximated to the second order, which provides a better approximation of Equation (24), an overestimation will result and the approximated value  $\beta_a > \beta$  is less than 4% larger than the value provided by Equation (26), which proves that the accuracy of the first assumption is valid anyway.

The previous analysis shows that the storage capacitor  $C_S$  can be assumed as a source of crossover distortion, even if  $R_{eq}$  is a real resistor. The key point is the inability of  $V_{in}(\theta)$  to keep pace with  $V_{ac}(\theta)$  on the falling edge of the sinusoid, due to the maximum discharge rate of  $C_S$  through  $R_{eq}$ . However, its net impact is the result of the interaction with the other sources of distortion, previously analyzed.

In fact, it has been assumed that a resistor  $R_{eq}$  that represents the whole converter, which implicitly means that the ratio of  $V_{in}(\theta)$  to  $I_{in}(\theta)$  is constant in  $(0, \pi)$ ; i.e.,  $I_{in}(\theta)$  is pure sinusoidal in  $(0, \pi)$ . Actually, the distortion of the current shape, caused by all the previously considered sources, tends to reduce

 $I_{in}(\theta)$  with respect to the undistorted case. Instead, considering the same model approach, if it can be assumed that the  $R_{eq}$  changes along the sinusoid, then  $R_{eq} = R_{eq}(\theta) = V_{in}(\theta)/I_{in}(\theta)$ . Figure 14 shows  $R_{eq}(\theta)$  obtained by dividing a sinusoidal input voltage and the current drawn that takes into account the distortion caused by the ringing current in Equation (20).



**Figure 14.** Variation of  $R_{eq}(\theta)$  along the sinusoid for the prototype converter caused by the ringing current.

 $R_{eq}(\theta)$  is almost flat for a wide range of the sinusoid except when the current is approaching the zero crossings. The increase in  $R_{eq}(\theta)$  produces an early dead zone with respect to the case with a fixed  $R_{eq}$ . The corresponding value of  $\alpha$  would be the solution of the equation:

$$\tan \alpha = 2\pi f_L R_{eq}(\alpha) C_s \tag{27}$$

The solution of Equation (27) must be defined in the interval ( $\pi/2$ ,  $\pi$ ), where tan  $\alpha$  has a finite value and consequentially also  $R_{eq}(\alpha)$ . As a result, the dead zone caused by the input capacitor  $C_s$  starts before  $R_{eq}(\theta)$  diverges, and  $I_{ac}(\theta)$  must cross zero before  $I_{in}(\theta)$ . In other words, as long as the bridge rectifier conducts,  $I_{ac}(\theta)$  is the sum of  $I_{in}(\theta)$  and the current through  $C_S$ , which is essentially a sinusoid leading by 90 degrees. This causes  $I_{ac}(\theta)$  to lead  $I_{in}(\theta)$ , whereas without  $C_S$  they would be essentially coincident.

Within the dead zone, the relation  $R_{eq}(\theta) = V_{in}(\theta)/I_{in}(\theta)$  is no longer the one shown in the diagram of Figure 14 because of both the voltage  $V_{in}(\theta)$  and the  $I_{in}(\theta)$  are not sinusoidal. Besides, the voltage retained by  $C_s$ , which makes  $V_{in}(\theta) > |V_{ac}(\theta)|$ , and  $T_{ON}(\theta)$  and  $T(\theta)$  will be much smaller than those predicted during the control method design, which was carried out assuming a sinusoidal input voltage, as per Equation (5). The resulting switching frequency may be higher. As long as some energy is delivered to the output,  $C_s$  (which is the only source of energy, since no current comes from the reverse-biased bridge rectifier), keeps on discharging and as long as  $I_{in}(\theta) > 0$ . If the peak current becomes lower than the critical peak primary current for no energy transfer, the energy is no longer transferred to the output and bounces back and forth between  $C_s$  and  $L_p$ , except for the energy dissipated during this process. As a consequence,  $C_s$  is discharged at a lower rate. Instead, if the peak current does not go below that critical value, the discharge rate of  $C_s$  has no change.

When  $|V_{ac}(\theta)| \ge V_{in}(\theta)$  and the dead zone ends at  $\theta = \beta$ , it is possible to observe an abrupt variation in  $I_{ac}(\theta)$ . This is caused by the bridge rectifier that is forward-biased, as  $I_{ac}(\theta)$  has to transition from zero to  $I_{ac}(\beta)$ , which is already greater than zero because of the leading phase of  $I_{ac}(\theta)$ .

It is worth mentioning that, near the zero crossing interval, the input voltage is far from constant in a switching cycle and the switching frequency may come close to the frequency related to the resonance between  $C_S$  and  $L_p$ . So, the  $V_{in}(\theta)$  has sinusoidal behavior, rather than constant. Additionally, the resonance of the inductors and capacitors in the EMI filter can also be stimulated, so that different resonance phenomena may coexist. This means that the modeling approach used throughout the present discussion is not always valid in describing the practical behavior.

#### 3.5. Crossover Distortion Due to Transformer's Leakage Inductance

In practical cases, the real transformer's windings are not perfectly coupled. This phenomenon causes a crossover distortion that affects the input current shape and degrades the THD. Therefore, in the following subsection, the analysis of the distortion no longer takes into account assumptions 3 and 4.

In a real transformer, a portion of the energy stored in the primary winding cannot be transferred to the secondary winding because of imperfect magnetic coupling. In other words, this can be modeled by considering the primary inductance  $L_p$  split into two distinct elements: the magnetizing inductance  $L_M$  perfectly coupled to the secondary winding and the leakage inductance  $L_{lk}$  (uncoupled). In these terms, it is useful to define the coupling coefficient  $\sigma$  such that  $L_M = \sigma L_p$  and  $L_{lk} = (1 - \sigma) L_p$ . Typical values of  $\sigma$  range from 0.95 to 0.99.

The energy stored in the leakage inductance is not transferred to the output and this energy would overcharge  $C_{DS}$  well over  $V_{in}(\theta) + V_R$ , in most cases exceeding the voltage rating of the power switch. A typical solution is to use a clamp circuit which limits  $V_{DS}(t)$  at a well-defined and properly selected value  $V_{CL}$  (>  $V_R$ ) above  $V_{in}(\theta)$ . Figure 15 shows the equivalent circuit of the Hi-PF QR flyback converter during the off time and the current waveforms underlining the effect of  $L_{lk}$ .



**Figure 15.** (**a**) Simplified equivalent circuit during off time. (**b**) Current in the real primary windings (blue trace) and in the secondary windings (black trace).

When the power switch is turned off, the primary current firstly charges the capacitance  $C_{DS}$ , thus the  $V_{DS}(t)$  evolves until the voltage of the magnetizing inductance  $L_M$ ,  $V_M$ , equals  $-V_R$ . During this time interval  $T_{ps}$ , the primary current  $I_p$  is flowing through  $L_M$  and  $L_{lk}$ , so there is an inductive voltage divider. Therefore:

$$V_{M} = -\frac{L_{M}}{L_{p}}V_{p} = \frac{L_{M}}{L_{p}}[V_{in}(\theta) - V_{DS}(t)]$$
(28)

In the instant when the voltage  $V_M$  equals  $-V_R$ , the voltage  $V_p$  across the primary winding can be expressed as:

$$V_p = \frac{L_p}{L_M} V_R = \frac{1}{\sigma} V_R \tag{29}$$

Immediately after the time interval  $T_{ps}$ , the current starts flowing through D1 and the energy starts being transferred to the output.  $V_{DS}(t)$  keeps on ramping up until it reaches  $V_{in}(\theta) + V_{CL}$  in a time  $T_{LK}$ . After that,  $V_{DS}(t)$  is clamped,  $L_{lk}$  starts being demagnetized with a rate equal to  $(V_R - V_{CL})/L_{lk}$  and

the current through D1 reduces at the same rate. The portion of the primary current  $I_p(t)$  of the leakage inductance varies from the peak value,  $I_{pkp}(\theta)$ , until zero in a time interval equal to  $T_{LK}(\theta)$ . Hence:

$$I_p(t) = I_{pkp}(\theta) - \frac{V_{CL} - V_R}{(1 - \sigma)L_p}t$$
(30)

As soon as  $I_p(t)$  is equal to zero, it can be written in the analytical expression of  $T_{LK}$ :

$$T_{LK}(\theta) = \frac{(1-\sigma)L_p}{V_{CL} - V_R} I_{pkp}(\theta)$$
(31)

Bearing in mind the current that flows in  $L_M$  can be written as:

$$I_M(t) = I_{pkp}(\theta) - \frac{V_R}{\sigma L_p}t$$
(32)

Meanwhile, the secondary current reaches its peak value  $I_{pks}(\theta)$ :

$$I_{pks}(\theta) = nI_M(T_{LK}) = n \left[ 1 - \frac{V_R}{V_{CL} - V_R} \frac{1 - \sigma}{\sigma} \right] I_{pkp}(\theta)$$
(33)

After that, the magnetizing inductance on the secondary side starts being demagnetized at a rate  $V_{R/L_M}$  until it zeroes in a time  $T_{DEM}$ , as shown in Figure 15. The presence of  $L_{lk}$  splits the time interval  $T_{FW}$  in a first subinterval  $T_{LK}$  needed to demagnetize the leakage inductance (and magnetize the secondary winding) and a second subinterval  $T_{DEM}$  needed to demagnetize the secondary winding. It is possible to prove that the resulting  $T_{FW}$  can be expressed as:

$$T_{FW}(\theta) = \frac{L_M}{V_R} I_{pkp}(\theta) = \sigma \frac{L_p}{V_R} I_{pkp}(\theta)$$
(34)

(i.e., the one calculated neglecting the leakage inductance multiplied by the coupling coefficient  $\sigma$ ).

The presence of  $L_{lk}$  clearly compromises the input-to-output transfer energy, thus the dead zone where there is no energy transfer is expected to occur over a wider phase angle range of the line voltage. In fact, the "no energy transfer" condition concerns only the portion of the primary voltage  $V_p$  across the magnetizing inductance  $L_M$ . Combining Equations (8), (9) and (28), it is possible to find that the condition for no energy transfer, solved for  $I_{pkp}(\theta)$ , yields:

$$I_{pkp}(\theta) \le Y_L \sqrt{\left(\frac{V_R}{\sigma}\right)^2 - V_{in}^2(\theta)}$$
(35)

The critical peak primary current for no energy transfer, expressed by Equation (35), is larger than the ideal case ( $\sigma = 1$ ), thus confirming the forecast of a wider dead zone related to this phenomenon.

It is noteworthy to compare the critical value of  $I_{pkp}(\theta)$  in Equation (35) to that determined by the ringing current after demagnetization and the relative positions of the dead zones they generate.

Bearing in mind that the on time can be written as:

$$T_{ON} = \frac{L_p}{V_{in}} I_{pkp} \tag{36}$$

The region around zero crossings where there is no input-to-output energy transfer ( $I_{in}(\theta) = 0$ ), can be written by considering the combination of the input current in Equation (20) in the case of  $V_{in} < V_R$ , and Equation (36):

$$I_{pkp} = \frac{(V_{in} + V_R)^2}{V_{in}} \frac{C_{DS}}{L_p} \frac{V_{in}}{I_{pkp}}$$
(37)

Combining Equations (10)–(37), the ringing current after demagnetization related to the dead zone can be expressed as:

$$I_{pkp}(\theta) \le Y_L[V_{in}(\theta) + V_R] \tag{38}$$

Figure 16 shows the ratio of the critical value of  $I_{pkp}(\theta)$  for no input-to-output energy transfer, as in Equation (35), to that caused by the ringing current, as in Equation (38). The ratio is expressed as a function of the parameter  $K_v$ :

$$K_v = \frac{V_{PK}}{V_R} \tag{39}$$

where  $V_{PK}$  is the peak value of the rectified line voltage  $V_{in}(\theta)$ . The dashed blue line represents the ideal case. As is evident from Figure 16, the dead zone becomes even larger near the zero crossings. Therefore, the lack of input-to-output energy transfer may override the dead zone caused by the ringing current needed for the demagnetization of the secondary winding in a time  $T_{DEM}$ .



**Figure 16.** Ratio of the critical value of  $I_{pkp}(\theta)$  for no input-to-output energy transfer in dead zone, caused by leakage inductance, as in Equation (35), to that caused by ringing current, as in Equation (38), as a function of Kv for  $\sigma = 0.95$ .

## 4. Conclusions

The standard limitations regarding the input current distortion in LED driver applications may be stringent, especially in large lighting systems. Therefore, the choice of a proper LED driver aiming at current harmonics reduction is crucial. At the same time, the solution must be economical, compact and reliable.

The QR flyback shows the highest figure of merit (FOM) among the different LED driver solutions analyzed in the literature. With this aim, this work has investigated and has analyzed the different inherent causes of distortion in the input current and the power processing mechanism of the proposed QR flyback converter that are not ascribable to the control method.

Several effects, such as the distortion caused by the ringing current, crossover distortion due to transformer leakage inductance and crossover distortion due to the input storage capacitor, have been analyzed in depth. It is important to point out that the converter is a nonlinear system and, consequentially, the overall THD of the input current cannot be evaluated as a simple sum of the THD associated to each individual contribution, where the aforementioned issues are mutually interacting or partly overlapping, such as those creating a dead zone in the line current.

Some useful design hints have been extracted and discussed in order to provide some suggestions for an optimized design of a QR flyback LED driver converter. In detail, the following list summarizes all the possible precautions to bear in mind.

1. The impact of the ringing current after transformer demagnetization can be mitigated by lowering the switching frequency, using a low reflected voltage  $V_R$  or choosing a power MOSFET with a

 $R_{DS(on)}$  with an optimized  $R_{DS(on)}/C_{oss}$  FOM. These criteria also help to reduce the phenomenon of

- the lack of input-to-output energy transfer near the zero crossings of the line voltage.
- 2. The leakage inductance of the transformer should be kept as low as practically possible. This choice essentially optimizes the converter efficiency but does not impact the reduction in the dead zones near the zero crossings of the line voltage caused by other phenomena (essentially, the input capacitor CS).
- 3. The input storage capacitor CS should be minimized to reduce the dead zone near the line voltage zero crossings and the current leap occurring in the proximity of the dead zone. However, particular attention should be paid to the following points.
  - a. The diodes of the input bridge rectifier are usually slow-recovery ones, so the primary current at the switching frequency may require an enhanced filter on the ac side of the bridge and may cause the diodes of the bridge to overheat.
  - b. Close to the zero crossings, the switching frequency can be very low. If the ringing frequency related to  $C_S$  and  $L_p$  is comparable with the switching one, it may generate current spikes that would degrade the current THD.
- 4. Class-X capacitors are generally used along with inductors for EMI filtering, necessary for the certification of the final product. Class-X capacitors can degrade the PF, although they do not contribute to the THD. From this perspective, on the one hand, the design of the filter must make the device compliant with the standards. On the other hand, there is a degree of freedom that can be exploited to minimize PF lowering at high line and light load. The filters should be designed with the largest inductance and the smallest capacitance practically possible.

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# Nomenclature

$V_{ac}(t,\theta)$	[V]	Line voltage input.
$V_{in}(t,\theta)$	[V]	Rectified line voltage.
$V_{PK}$	[V]	Peak of the rectified line voltage $V_{in}$ ( $\theta$ ).
$I_{ac}(t, \theta)$	[A]	Line input current.
$I_p(t, \theta)$	[A]	Current on the primary windings.
$I_s(t, \theta)$	[A]	Current on the secondary windings.
Iout	[A]	Output constant current.
Vout	[V]	Output constant voltage.
$L_P$	[Ω]	Inductance of the primary windings.
$L_s$	[Ω]	Inductance of the secondary windings.
Ton	[s]	On time of the power switch
$T_{FW}$	[s]	Time interval where the current flows on the secondary side.
Tneg	[s]	Time interval where the drain-source voltage rings
Т	[s]	Time interval of the switching period.
$C_{DS}$	[F]	Drain to source capacitance of the MOSFET.
$V_{DS}(t)$	[V]	Drain to source voltage of the MOSFET.
$I_{pkp}(\theta)$	[A]	Current amplitude on the primary windings.
$V_R$	[V]	Reflected voltage.
$T_r$	[s]	Time period of drain voltage ringing.
$T_z$	[s]	Time interval needed for $V_{DS}$ to fall to zero.
$T_{zz}$	[s]	Time interval needed for primary current to ramp linearly until zero.
$Y_L$	[Ω]	Characteristic admittance of the $C_{DS}$ - $L_p$ tank circuit.
Qpos	[C]	Charge accumulates from the input source.

Qneg	[C]	Charge returned to the input source.
L <sub>M</sub>	[Ω]	Magnetizing inductance.
$T_{LK}$	[s]	Time interval needed to demagnetize the leakage inductance.
σ		Coupling coefficient of $L_m$ .
$I_{pks}(\theta)$	[A]	Current amplitude on the secondary windings.
R <sub>eq</sub>	[Ω]	Equivalent resistor of the converter.
P <sub>in</sub>	[W]	Input power.

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