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# Systematic Characterization of Plasma-Etched Trenches on 4H-SiC Wafers

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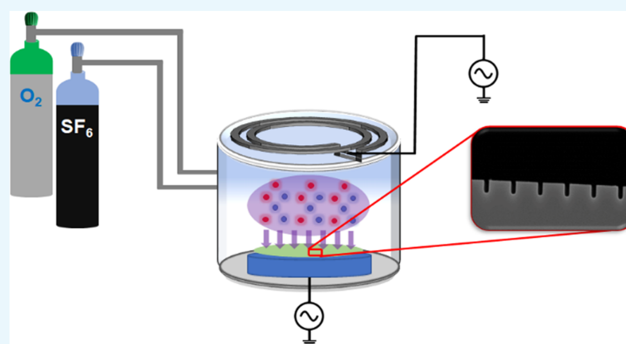
**ABSTRACT:** Silicon carbide power semiconductors overcome some limitations of silicon chips, and therefore, SiC is an attractive candidate for next-generation power electronics. In addition, the number of possible vertical devices that can be obtained on a given surface using the trench technique is significantly larger than that attainable using a planar setup. Moreover, a SiC trench power metal oxide semiconductor field-effect transistor (power MOSFET) structure removes the junction field-effect transistor (JFET) region (that would decrease the current flow width) and improves the channel density, thus reducing the specific electrical resistance. Consequently, in the present study, we report on the chemical bonding state of elements and structural characterization of trenches, obtained using $SF_6$-based plasma etching, on the 4H-SiC polytype substrate. An interferometric algorithm that finds the endpoint to stop etching governed the trench depth. Scanning electron microscopy, transmission electron microscopy, atomic force microscopy, and X-ray photoelectron spectroscopy analyses stated the high quality and uniformity of the trenches. These materials are particularly promising for the fabrication of the SiC MOSFET to be implemented in the manufacturing of power devices.




## INTRODUCTION

Silicon chips in power devices and power systems show some restrictions since silicon has limited thermal conductivity (working temperatures no greater than 150 °C) and a low band gap (1.1 eV), thus conferring high power loss and low switching frequencies to the devices.

A silicon carbide power metal oxide semiconductor field-effect transistor (power MOSFET) can overcome these limitations. In fact, SiC shows excellent physical and electrical properties (band gap: 3.3 eV, thermal conductivity better by a factor of 3 with respect to common silicon, working temperatures up to 200 °C, and tolerated voltages of the $10^3$ V order).[1,2] Actually, much smaller specific conduction resistance of SiC unipolar devices, with respect to the Si parent devices, allows smaller SiC chips with lower parasitic capacitance and higher switching speed. Therefore, silicon carbide devices are better suited for high-power, high-temperature, and high-frequency (HF) applications.[3−6]

Silicon carbide, a hard ceramic, exists in a large number of crystalline polytypes and is chemically inert, and its etching is a crucial technological step.[7,8] Moreover, for electronic uses, it requires high-quality etching to provide edge termination, contact to buried layers, and backside wafer thinning.[9]

In this context, the number of possible vertical devices that can be obtained on a given surface using the trench technique is larger than that attainable using a planar setup.

SiC shows excellent chemical stability toward wet etching that is only possible either using solid KOH that at temperatures above 600 °C sublimes and attacks SiC or with photoelectrochemical etching. For that reason, the use of plasma-based etching is necessary to obtain clean samples. In general, dry etching is a key technology comparable in importance to lithography as a means for scaling and enhancing the integration level of semiconductor devices. For this reason, dry etching for semiconductors and the plasma-based physical−chemical reactions have recently been reviewed by pointing out the contribution of this technology to progress in semiconductor integrated circuits, the related mechanism, the required equipment, and the future challenges and outlook.[10,11] It is observed that SiC plasma etching involves both chemical and physical mechanisms. The etching

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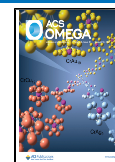

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requires the breaking of Si−C bonds, followed by the chemical interaction of reactive species with silicon and carbon to produce volatile compounds. Plasma chemistries based on highly reactive fluorine radicals generate volatile $SiF_x$ and $CF_x$ products.[12] Accordingly, $CF_4$, $SF_6$, $NF_3$, $CBrF_3$, and $CHF_3$ are the typical reactant gases, even though some gas mixtures were also used.[13,14] In addition, the relative anisotropy of plasma etching, obtained by biasing the substrate, allows precise control of the line width at the subnanometer scale. Besides, this line width control is very difficult during wet etching of SiC. So, etching of SiC with fluorinated gases is usually performed with the aid of additional noble gases for mass transport. Among the other characteristics frequently investigated during these processes, the etch rate, etching anisotropy (through the line edge profile), and taper angle (supplementary angle to the angle between the sidewalls and the bottom surface plane of the given trench) are important issues. Concerning the taper angle,

$$\text{taper angle} = \tan^{-1}\left(2 \times \left(\frac{\text{trench depth}}{\text{top CD} - \text{bottom CD}}\right)\right)$$

the trench shape has to be conic (angles in the 86−87° range) to facilitate the filling of the trench with gate oxide, during the successive synthesis of the MOSFET.[15−20]

Previous studies already reported high etching rate values for SiC using plasma based on $SF_6/O_2$ mixtures. In fact, Khan et al. investigated the inductively coupled plasma (ICP) etching of SiC using a $SF_6/O_2$ plasma and obtained anisotropic etch profiles with smooth surfaces and high etch rates.[21] Also, Wang and Yao et al. obtained trenches with a vertical profile using $SF_6/O_2$, but it was necessary to use a $BCl_3/N_2$ gas mixture to smooth the bevel (taper) angle.[22] Similarly, Tang et al. investigated a method for ultrafast etching of SiC by integrating a femtosecond laser with ICP etching based on $SF_6/O_2$ and obtained taper angles of 117°.[23] Likewise, Zekentes et al. used a $SF_6$/Ar gas mixture to perform etching of SiC and monitored both the etch rate and SiC surface roughness by interferometry.[24] Jiang et al. studied the plasma etching of SiC using a $Cl_2$/Ar mixture and observed high etch rates and the absence of microtrenches at a substrate temperature of −80 °C.[25] XPS analysis confirmed a small amount of Cl-related residues on the etched SiC surfaces.[25] The microtrenching phenomenon is referred to a V-shaped groove formed on the bottom adjacent to the sidewall, due to an enhancement in local etch rates induced by the ion reflection from the trench surface sidewalls.[17] Recently, Iankevich et al. demonstrated the formation of highly oriented (90° taper angle) structures with subnanometer surface roughness in thermally stimulated SiC, at 150 °C, using $SF_6/O_2$ ICP dry etching.[26] The increased etching temperature also caused a monotonic increase in the etching rate. Also, Cardinaud et al. reported on thin-film etching using $SF_6$/Ar and found smooth surfaces, free of fluorinated products, for etching mixtures with a high percentage of argon (95%).[27]

All these examples clearly indicate that the different adopted etching conditions need to be optimized in the perspective of scaling up the process of obtaining SiC trenches suitable for high-quality MOSFET fabrication. For example, in almost all of the already reported studies, no particular attention was paid to obtain a good conic shape of the trench structures that is fundamental for the subsequent filling of them with gate oxide for the MOSFET fabrication.

Thus, in the present study, we report on the electronic and structural characterization of SiC trenches obtained using $SF_6$-based plasma etching. We used interferometric endpoint detection (IEPD) for monitoring and precisely manage the trench depth.[28] Scanning electron microscopy (SEM), transmission electron microscopy (TEM), atomic force microscopy (AFM), and X-ray photoelectron spectroscopy (XPS) measurements revealed that the obtained trenches are of high quality and uniform. In fact, without any additional cooling or heating, using our optimized conditions, we anticipate to have obtained good SiC etch rates, trench depth uniformity between the wafer center and edge, taper angles suited for the successive MOSFET manufacturing, absence of microtrenches and SiC contaminants, no damage of the crystallographic planes of the trench sidewalls, and surface roughness ($R_{ms}$) below 0.2 nm. These characteristics make these SiC trenches almost perfect for MOSFET manufacture.

## ■ RESULTS AND DISCUSSION

Generally, etching processes can either be wet, using aggressive solutions or molten salts, or dry, using ion bombardment or plasma etching.[29−35] Plasma etching of SiC already proved to be suitable to get smooth profiles with a high degree of directionality. Using high-density and low-pressure plasmas allows fast anisotropic etching of SiC. This etching process is ion-induced and limited by the concentration of the reactive species within the gas mixture.[35] Above all, etching selectivity of SiC, with respect to $SiO_2$, in terms of directionality is fundamental to get optimal edge definitions. As already reported, SiC etching proceeds via an ion-enhanced mechanism, by the perpendicular bombardment of the surface by positive ions that are accelerated by a sheath potential that develops on surfaces exposed to the plasma.[11] The etching mechanism involves the synergistic action of physical and chemical mechanisms. The atomic bond Si−C is broken by the action of ion bombardment.[14] The different types of defects enhance the etching rate, and the Si−Si and C−C bond formation allows the partially separated atoms to be removed by chemical reactions, the latter being possible in many cases, thanks to the presence of the energetic ion flux. The chemical mechanism is determined by the volatility of the reaction byproducts and the energy of the ionized species. Highly volatile etch byproducts are critical for fast etching. Therefore, etch byproducts should have relatively high room temperature vapor pressure or equivalently low boiling point. $SiF_x$ and $CF_x$ are the main SiC etch products of fluorinated plasma chemistries.[14] $O_2$ addition to $SF_6$ plasma gives another pathway for volatilizing the carbon atoms in the forms of CO and $CO_2$, which induces the increase of the etch rate.[21] Therefore, the choice of plasma chemistry in terms of volatility and stability of the etch products is important. For these reasons, as already stated, we optimized the experimental conditions to get the best profile control of the trench pattern and chemical structure of the final SiC trenches (Scheme 1).[36]

Table 1 summarizes the most important structural data of our SiC etched system (trench depth/etch rate, depth uniformity, and taper angle) upon varying power, pressure, and gas flows.

We started present SiC trench formation using etching parameters already reported in the literature and then varied them to optimize the trench quality. In fact, typical powers for SiC trench procedures are in the 500−2000 W range[21,22,35,37] and pressures are in a few tens of Pascal range.[24] Often, the Ar


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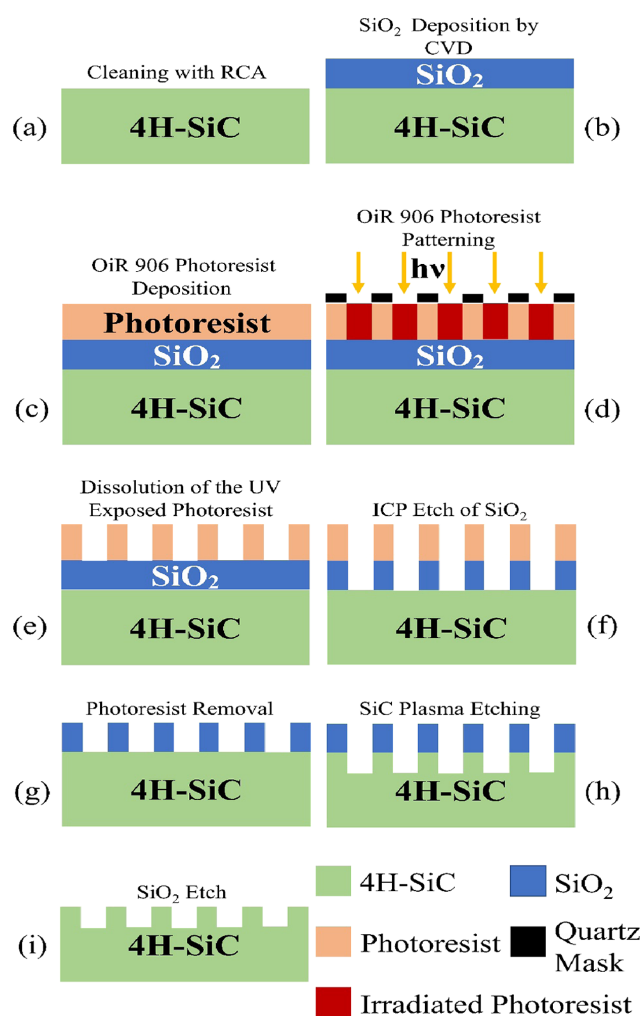
**Scheme 1. Manufacturing Steps for the SiC Trench: (a) Cleaning of the SiC Substrate with an RCA Solution; (b) $SiO_2$ (~1.6 μm) Hard Mask Deposition; (c) Photoresist Deposition; (d) Photoresist Patterning; (e) Solvent Dissolution of the Exposed Photoresist; (f) Plasma Etching of $SiO_2$; (g) Polymer Photoresist Removal; (h) SiC Etching for Trench Formation; and (i) $SiO_2$ Hard Mask Removal**




flow for the SiC etching is kept 2 orders of magnitude larger than that of $SF_6$, and the oxygen flow is about 10 sccm.[27,35] The only process parameter that we kept constant in all tests was the $SF_6$ flow (6 sccm). Noteworthy, the depth uniformity percentage between the center and edge of the same wafer or different wafers was statistically determined using the following well-known equation where the lower depth uniformity % value stands for the better trench uniformity

$$\text{depth uniformity }\% = \frac{(\text{max depth value} - \text{min depth value})}{2 \times \text{depth average}} \times 100$$

Experiment 1 produced a taper angle of 90°, a mean etch rate of 11.7 nm/s, and a depth uniformity of 2.6%. With experiment 2, we observed a less vertical profile of the trench (taper angle 86°), a mean etch rate of 11.0 nm/s, and a depth uniformity of 1.4%. No microtrenches were observed. So, the power decrease from 1700 to 1300 W (experiments 1 and 2) determines a decrease of the taper angle (from 90 to 86°) and improved depth uniformity (from 2.6 to 1.4%). This result is in agreement with the fact that high ICP power values induce the increase of the density of the reactive ions in the chamber, which in turn increases the rate of chemical reactions on the etched surface, correlated to a greater number of ions with higher kinetic energies impinging per unit area on the substrate, resulting in high vertical etching and not uniformity between the center and edge of the wafer.[21] Therefore, it is intuitive that if the ICP power decreases (from 1700 to 1330 W), the main results will be the decrease of the etch rate and the improvement of depth uniformity.

Then, we increased the power at 1500 W and decreased the total pressure from 67 to 34 Pa to explore the influence of the pressure. The trench obtained by experiment 3 continues to show an almost vertical profile (taper angle of 89°), a mean etch rate of 12.3 nm/s, and a depth uniformity of 2.9%. In fact, it is known that the decrease of the pressure induces the increase of the mean free path and the average lifetime of ions in the etching chamber.[21] This effect increases the directionality of the ions impinging on the SiC samples and produces a high vertical profile and decreases the mean trench depth.[21] Consequently, if the overall pressure decreases, the etch rate decreases as well and the depth uniformity improves.

**Table 1. Comparison of the SiC Trench Results in Terms of Etch Rate, Depth Uniformity, and Taper Angle (Figure S1) upon Different Experimental Conditions**

| experiment | ICP power (W) | pressure (Pa) | $SF_6$ (sccm) | $O_2$ (sccm) | Ar (sccm) | He (sccm) | etch rate (nm/s) | | depth uniformity (%) | taper angle (deg) |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | C[a] | E[b] | | |
| 1 | 1700 | 67 | 6 | 10.5 | 344 | 344 | 12.0 | 11.4 | 2.6 | 90 |
| 2 | 1300 | 67 | 6 | 10.5 | 344 | 344 | 11.1 | 10.8 | 1.4 | 86 |
| 3 | 1500 | 34 | 6 | 10.5 | 344 | 344 | 12.6 | 11.9 | 2.9 | 89 |
| 4 | 1500 | 17 | 6 | 10.5 | 344 | 344 | 9.7 | 9.4 | 1.6 | 90 |
| 5 | 1500 | 67 | 6 | 7.0 | 344 | 344 | 13.5 | 13.0 | 1.9 | 89 |
| 6 | 1500 | 67 | 6 | 6.0 | 344 | 344 | 10.5 | 10.3 | 1.0 | 90 |
| 7 | 1500 | 67 | 6 | 10.5 | 115 | 573 | 9.7 | 8.4 | 7.2 | 85 |
| 8 | 1500 | 67 | 6 | 10.5 | 573 | 115 | 12.0 | 11.7 | 1.3 | 90 |
| 9 | 1500 | 67 | 6 | 10.5 | 344 | 344 | 14.0 | 14.1 | 0.4 | 87 |

[a]Wafer center. [b]Wafer edge. The sum of Ar and He flows in all of the experiments was kept to 688 sccm. The Ar flow of 115 sccm corresponds to 1/6 of 688 sccm. The Argon flow of 573 sccm comes from 5 × 115 sccm. The flow of 344 sccm is 1/2 of 688 sccm.



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The results of experiment 4 showed a taper angle of 90°, a mean etch rate of 9.6 nm/s, and a depth uniformity of 1.6%. Therefore, using the above conditions, we did not obtain the desired trench metrical data. Hence, we decreased the $O_2$ flow and increased the total pressure again. The results of the trench obtained after experiment 5 show an almost vertical profile of the trench (taper angle of 89°), a mean etch rate of 13.3 nm/s, and a depth uniformity of 1.9%. After experiment 6, we noted a vertical profile of the trench (taper angle of 90°), a mean etch rate of 10.4 nm/s, and a depth uniformity of 1.0%. Hence, the decreased oxygen flow (from 10.5 to 6−7 sccm) caused the worsening of the taper angle that resulted in an almost vertical profile. In fact, $O_2$ helps the dissociation of $SF_6$, thus providing a good fluorine concentration and the decrease of the trench depth.[21] In this context, we observed a muted influence of the oxygen flow since its decrease from 10.5 to 7.0 sccm (with a concomitant increase of the overall pressure) caused an increased etch rate but a further decrease to 6.0 sccm, as expected, lowered the etch rate again. So, we decided to again increase and fix the oxygen flow at 10.5 sccm and modify the Ar/He flow. After experiment 7, we observed a taper angle of 85°, a mean etch rate of 9.1 nm/sec, and a depth uniformity of 7.2%. In contrast, after experiment 8, the taper angle increased again to 90°, the mean etch rate was 11.9 nm/s, and the depth uniformity was 1.8%. These further results are in agreement with the fact that a low concentration of argon, a gas that contributes to the sputtering, lowers the etch rate and strongly worsens the depth uniformity. After these latter two experiments, we decided to keep both Ar and He flows identical (344 sccm). Experiment 9 produced a taper angle of 87°, a mean etch rate of 14.1 nm/s, and a depth uniformity of 0.4%. As a result, these latter conditions allowed achieving a good round bottom profile with smooth sidewalls of the trench and no evidence of microtrenching (vide infra). The absence of microtrenching in the present work is due to the delicate balance of the oxygen concentration which, in our condition, is only 1.5% but enough to remove carbon in the form of volatile products such as CO, $CO_2$, and $COF_2$ and control the quality of the trench in terms of taper angle, etch depth, and top and bottom critical dimension (CD).[21] These data are the best in terms of the overall quality of the SiC trenches useful for the subsequent MOSFET fabrication.

The chemical bonding state of elements and morphological characterization of the optimized trench etching on SiC in terms of chemical composition, lateral dimension, depth, and depth profile were investigated with SEM, TEM, AFM, and XPS analyses.

Figure 1 shows a representative SEM image of the trenches obtained in the SiC wafer before the HF + $NH_4F$ treatment to remove the $SiO_2$ hard mask. It is clear that the trench involves both the remaining $SiO_2$ (hard mask) and the SiC.

The in-plane view of the SEM analysis of the trenches in the SiC wafer, after the HF + $NH_4F$ treatment (Figure 2), indicates that the obtained trenches are highly ordered. The lateral dimension of a given trench, measured at the upper part of the SiC wafer, resulted as 950 ± 5 nm.

The high-resolution section SEM analysis of the trenches in the SiC wafer, after the HF + $NH_4F$ treatment (Figure 3), confirms that the $SiO_2$ hard mask was completely removed and that the lateral dimensions of the trenches are 950 ± 5 nm at the top of the trench and 810 ± 5 nm at the bottom of the trench. The trench depth is 1180 ± 5 nm. Thanks to the interferometric method adopted to stop etching, the obtained trenches are uniform, with a taper angle of 87° and depth uniformity below 1%. Therefore, the present experimental etching conditions resulted in a high degree of anisotropy with high etch mask selectivity and produced conic bottom trench profiles and smooth surfaces.

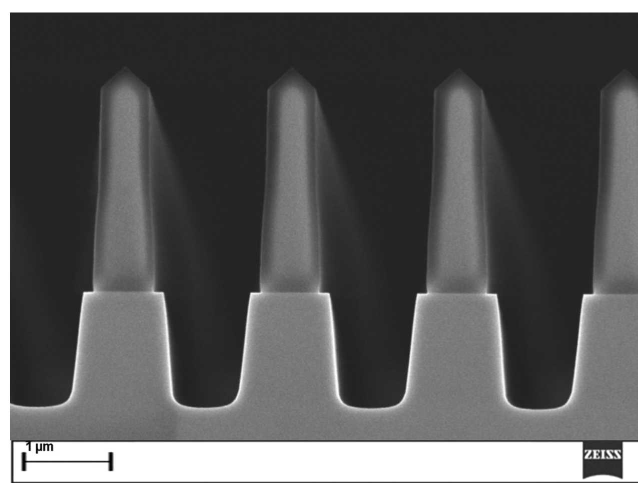


**Figure 1.** SEM section analysis of the trenches in the SiC wafer before the HF + $NH_4F$ treatment to remove the $SiO_2$ hard mask.

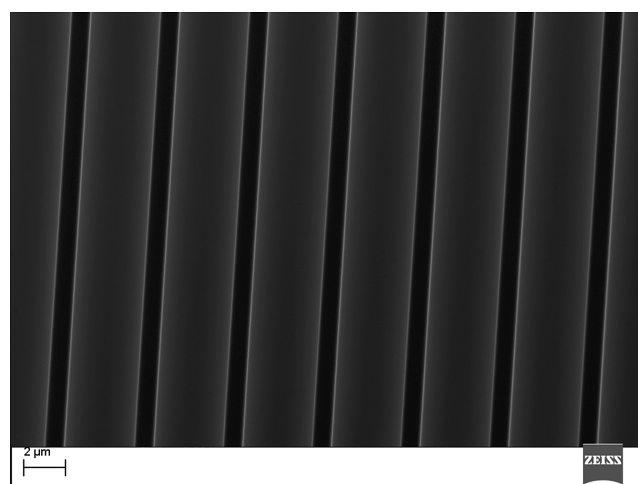


**Figure 2.** In-plane view of the SEM analysis of the trenches in the SiC wafer after the HF + $NH_4F$ treatment.

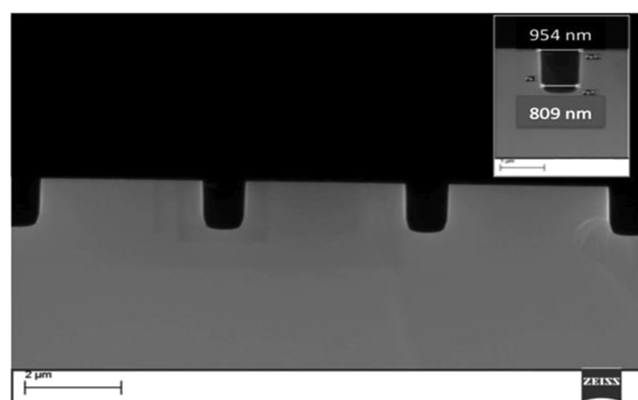


**Figure 3.** Representative section SEM analysis of the trenches in the SiC wafer after the HF + $NH_4F$ treatment.



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In addition, we also investigated the structural properties of the obtained trenches by cross-sectional transmission electron microscopy to evaluate the shape and roughness of the sidewalls. TEM analysis of the trench (Figure 4) shows the terraces of (11−20) planes (cyan lines), the surface plane and the normal to the surface plane (red lines), and the internal trench surface walls (green lines). As expected, it is observed that the two frontal internal surfaces atomically reconstruct differently because of the angular differences between the internal walls and the internal atomic planes of the crystal. In fact, (11−20) planes are at low surface energy and the crystal tends to cover itself with these planes.

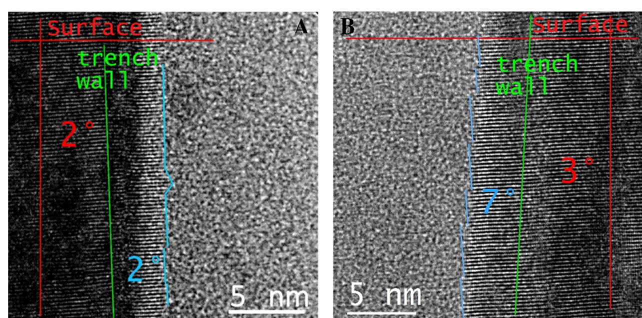


**Figure 4.** TEM analysis of the section of a representative trench in the SiC wafer after the HF + $NH_4F$ treatment: (A) left internal wall of the SiC trench and (B) right internal wall of the SiC trench.

From these data, it appears that the angles between the surface normal and the internal walls are 2 and 3° for the left and right walls, respectively. These results indicated that the trench is symmetrically flared (of about 2°) with a very flat surface. The angles between the surface normal and the (11−20) family planes are 2 and 7° for the left and right walls, respectively. This result was not unexpected since the crystalline planes are asymmetric (4°) with respect to the surface off-axis of the 4H-SiC substrate, and therefore, the angles of the two sidewalls must be different. The walls at 7° with respect to the crystallographic direction show much more frequent steps with respect to those at 2°. The terrace dimension is 5 nm for the left walls and in the 2−4 nm range for the right walls. In theory, each given step between the terraces could be a potential defect, but the widespread roughness could also induce electric problems to the specific device. During the ICP process for trench formation, a sidewall protection mechanism takes place, thanks to the formation of a protective film like a $SiF_xO_y$ polymer that prevents invasion by radicals during etching.[10,17] This fluorinated polymer coating was removed with the HF + $NH_4F$ treatment. As a consequence, the roughness of the trench sidewalls became negligible, thanks to the protection of this film from possible damage during the plasma process.[10,17]

We also performed AFM measurements on SiC wafers before and after etching for the trench formation. The mean roughness ($R_{ms}$) before any etching was 0.14 nm with a peak-to-peak value of 0.96 nm. A blank SiC wafer after etching its surface showed an $R_{ms}$ value of 0.16 nm. After etching the SiC to get trenches, the $R_{ms}$ value resulted in 0.18 nm with a peak-to-peak value of 1.55 nm (Figure S2).

The chemical bonding state of elements of the trenches in the 4H-SiC wafer, after the HF + $NH_4F$ treatment, was performed by means of X-ray photoelectron spectroscopy. This technique is ideal for an accurate description of the surface electronic structure and to identify the chemical composition.[38,39] Figure 5 shows the high-resolution C 1s XP spectrum of this 4H-SiC sample. This spectrum was fitted using three Gaussian components at 283.2 (main peak), 285.0, and 286.3 eV, which are safely ascribed to C−Si, C−C, and C−O states, respectively.[40−42] The peak at 285.0 eV is due to some surface adventitious carbon contamination omnipresent in air-exposed materials. Moreover, the small peak at 286.3 eV is due to some SiC surface oxidation during the plasma etching with $O_2$ and $SF_6$. In this spectrum, there is no evidence of C−F states (usually found above 290 eV). Moreover, signals of neither fluorine nor sulfur compound were found in the F 1s (∼685 eV) or S 2p (∼162 to 168 eV) binding energy regions, thus confirming the absence of any fluorine or sulfur contamination (Figures S3−S4).

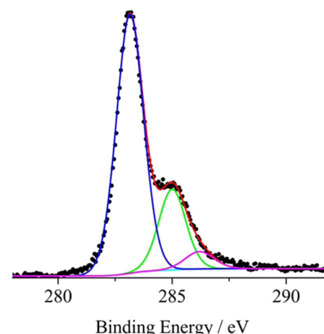


**Figure 5.** Al K$\alpha$-excited XPS of the 4H-SiC wafer, after the HF + $NH_4F$ treatment, in the C 1s binding energy region. The black dots refer to the experimental profile. The blue line refers to the Gaussian component at 283.2 eV; the green line refers to the Gaussian component at 285.0 eV, the magenta line refers to the Gaussian component at 286.3 eV, and the red line superimposed on the experimental profile refers to the sum of the Gaussian components.

Figure 6 shows the high-resolution Si 2p XP spectrum of the trenches in the 4H-SiC wafer after the HF + $NH_4F$ treatment. This spectrum was fitted with two Gaussian components at 100.7 and 102.8 eV, safely assigned to Si−C and Si−O states, respectively.[40−42] This latter very weak peak indicates that the

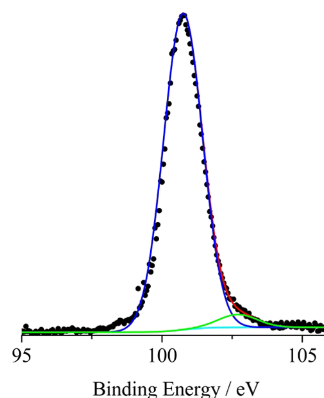


**Figure 6.** Al K$\alpha$-excited XPS of the 4H-SiC wafer, after the HF + $NH_4F$ treatment, in the Si 2p binding energy region. The black dots refer to the experimental profile. The blue line refers to the Gaussian component at 100.7 eV, the green line refers to the Gaussian component at 102.8 eV, and the red line superimposed on the experimental profile refers to the sum of the Gaussian components.


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presence of $SiO_2$ on the 4H-SiC wafer surface is almost negligible.

Finally, Figure 7 shows the high-resolution O 1s XP spectrum of the 4H-SiC wafer after the HF + $NH_4F$ treatment.

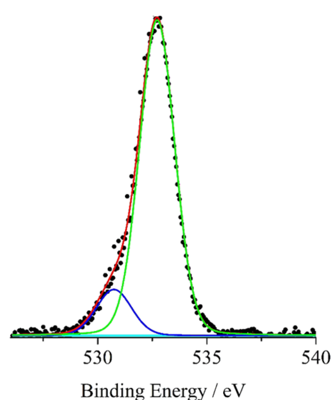


**Figure 7.** Al K$\alpha$-excited XPS of the 4H-SiC wafer, after the HF + $NH_4F$ treatment, in the O 1s binding energy region. The black dots refer to the experimental profile. The blue line refers to the Gaussian component at 530.7 eV; the green line refers to the Gaussian component at 532.7 eV; and the red line superimposed on the experimental profile refers to the sum of the Gaussian components.

This spectrum was fitted using two Gaussian components at 530.7 and 532.7 eV. The lower energy peak located at 530.7 eV is due to Si−O suboxides.[41] The peak at 532.7 eV is assigned to $SiO_2$.[43]

The XPS atomic concentration analysis indicated a Si/C = 1.0 atomic ratio, in agreement with what was expected for the 4H-SiC phase. This, in turn, rules out any carbon-rich sidewall surfaces as a result of etching.

## CONCLUSIONS

The main aim of this work was the formation and characterization of trenches on the 4H-SiC polytype surface. Present SEM, TEM, AFM, and XPS investigations have been useful to shed light on both the morphology and electronic structure of the trenches for the successive fabrication of SiC MOSFET (650 V breakdown) devices. To resume, we obtained the trenches using $SF_6$-based plasma etching on the SiC substrate. Besides some surface adventitious carbon contamination, due to the air exposure of the materials, we found that SiC surface oxidation, due to the plasma etching with $O_2$ and $SF_6$, is almost negligible, while no evidence at all of any fluorine contamination was found.

Concerning the trench morphologies, we found that the angles between the surface normal and the internal walls are 2 and 3° for the left and right walls, respectively, thus indicating that the trench is symmetrically flared with a very flat surface. The angles between the surface normal and the (11−20) planes are 2 and 7° for the left and right walls, respectively, according to the asymmetric crystalline planes of the 4H substrate with respect to the surface. Also, the lateral dimension and trench depth were uniform (950 ± 5 and 1180 ± 5 nm, respectively). The optimum taper angle resulted to be 87° and the surface roughness was only 0.18 nm. No microtrenches at all were observed. The depth uniformity was only 0.4%. These data confirm that the trenches on the SiC substrate are very suitable for the fabrication of SiC MOSFET devices.

## EXPERIMENTAL METHODS

**SiC Trench.** A commercial 4H-SiC polytype substrate 6″, belonging to the $C_{6v}^{4}$-$P6_3mc$ space group and showing the hexagonal wurtzite symmetry with a doubled ABC... stacking sequence, was selected for trench etching, and Scheme 1 shows the adopted manufacturing steps. After the standard cleaning of the SiC substrate with an RCA solution ($H_2O/H_2O_2$ 30%/$NH_3$ 28%, 5:1:1 v/v/v),[43−45] a thick $SiO_2$ (~1.6 $\mu$m) layer, to be used as a hard mask for SiC etching, was deposited on the SiC wafer using a chemical vapor deposition technique (with tetraethyl orthosilicate, TEOS, by Novellus Concept One CVD Dielectric Deposition System, Livingstone, U.K.). Deposition parameters were as follows: TEOS = standard 1.8 mL/min, $O_2$ = 8 standard liters per min (sLm), total pressure = 2930 Pa, high-frequency (HF) power = 0.6 kW, low-frequency (LF) power = 0.45 KWatt, and deposition temperature = 350 °C. Then, we performed a lithography step to pattern the oxide by spinning a polymer photoresist (photoresist Fujifilm OiR 906, thickness of 1.9 $\mu$m). We protected portions of the $SiO_2$ surface with a distant quartz mask. Then, the system was irradiated with UV light at 365 or 248 nm, and afterward, we developed an exposed polymer surface (solvent dissolution using an OPD 4280 Fujifilm surfactant). Plasma etching was performed in an ICP reactor (using a TEL UNITY Me Ox, dipole ring magnet (DRM), Company Tokyo Electron Ltd., Tokyo) to etch the oxide not covered by the polymer (pressure: 8.00 Pa/power 1300 W/$C_4F_8$ 10.0 sccm/$O_2$ 5.0 sccm/Ar 500.0 sccm, experimental uncertainty for gas flow measurements = 0.1 sccm).[22] After $SiO_2$ etching, the polymer photoresist was totally removed in a downstream chamber with $O_2$ plasma, using GASONICS L3510 plasma system. This plasma is consistent with active monatomic oxygen species that chemically react with the photoresist on the surface of the wafer and are very effective for cleaning semiconductor wafers. This process was followed by wet etching for the removal of polymer residues using a $H_2SO_4/H_2O_2$ (v/v 9:1) solution. SiC trench etching was performed in an ICP chamber (pressure: 67 Pa/power 1500 W/$SF_6$ 6 sccm/$O_2$ 10.5 sccm/Ar 344 sccm/He 344 sccm) equipped with an interferometric endpoint (TEL UNITY SiC, Company Tokyo Electron Ltd., Tokyo). The choice of $SF_6$ as a source of fluorine radicals was mainly due to the fact that $SF_6$ produces a concentration of F radicals higher than those by other etchant gases (e.g., $CF_4$ and $NF_3$). In addition, the absence of carbon atoms in the $SF_6$ structure avoided the formation of low volatile, carbon-containing etching byproducts, which could be the main pollutants of the sidewalls. Argon in the reaction mixture was not simply a carrier gas but also sputtered the SiC surface, thus increasing the etch rate, broke the Si−C bonds, and made the surface of the sidewalls smoother, as $Ar^+$ ions helped to remove fluorocarbon and similar etch products from the wafer surface.[14] Instead, the main function of He was to allow the optimal ignition and sustenance of the plasma since ultraviolet photons were produced using a He gas discharge and the photons emitted by helium plasma had energies of 21.21 eV (He I) and 40.80 eV (He II). After ignition, the helium plasma self-sustained and self-ionized, thus giving a photoelectronic band at 4.99 eV. In these conditions, the interferometric endpoint detection allowed tuning the etching depth with an uncertainty of 5 nm and we performed SiC trench depths across an 800−1400 nm range. The obtained best etch rate, measured by interferometry, resulted in about 829 nm/min


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and we obtained a trench profile with a round trench bottom and undamaged sidewalls.[21−26]

The final step was the full $SiO_2$ removal in a wet bench with standard chemistry (HF + $NH_4F$ 1:1 at 28 °C). At this stage, we obtained the SiC wafer with a pattern of trenches in the order of a micron. It is noteworthy that we optimized the conditions reported in this study for CVD, lithography, ICP $SiO_2$ plasma etching, polymer removal with $O_2$ plasma, SiC trench etching, and finally $SiO_2$ wet etching. These conditions are the best in terms of morphology, chemical structure, absence of microtrenches, and reproducibility of the final SiC trench formation.[37] In fact, while it has been reported that the microtrench phenomenon in SiC etching can be eliminated by subsequent thermal chlorine etching above 900 °C,[18,19] by the addition of HBr to $SF_6/O_2$,[20] or cyclically switching between anisotropic dry etching with $SF_6/O_2$ and polymer passivation with $C_4F_8$ that generates $CF_2$ neutral radicals in the plasma atmosphere to coat the surface and serve as a protective barrier to avoid these microtrenches,[37] within our above reported experimental conditions ($O_2$ concentration in the reaction gas mixture only 1.5%),[17] we did not observe any microtrench. As a general indication, within the above conditions and setup, the minimum value of the critical dimension (CD) of the SiC trench was 0.25 $\mu$m, while the maximum value of the depth trench was 10 $\mu$m.

**Scanning Electron Microscopy.** The surface morphology of the trench on SiC was examined by field emission scanning electron microscopy (FE-SEM) using a SUPRA VP 55 microscope (ZEISS, Jena, Germany). The trench depth was estimated using both interferometry and cross-sectional SEM analyses. In particular, we performed some initial trench/interferogram blank tests, also confirmed by SEM measurements, to build an endpoint algorithm. Once the system was set up, some more sections were made to confirm the reliability of the algorithm. So, the endpoint was used to stop etching. This process was not performed for a given fixed time, but the interferometric endpoint algorithm decided when to stop etching so that the entire etched wafer batch had the same trench depth (Figure S5). We measured the lateral dimension and trench depth in many different trenches belonging to the same or different wafers by SEM whose experimental uncertainty was ∼5 nm.

**Transmission Electron Microscopy.** Transmission electron microscopy (TEM) measurements were performed with a JEOL JEM2010F using a 200 KeV electron beam.

**X-Ray Photoelectron Spectroscopy.** X-ray photoelectron spectra (XPS) were recorded with PHI 5600 Multi Technique System (Physical Electronics GmbH, Feldkirchen, Germany, base pressure of the main chamber: $3 \times 10^{-8}$ Pa).[38,39] Samples, placed on a molybdenum specimen holder, were excited with Al K$\alpha$ X-ray radiation using a pass energy of 5.85 eV. The instrumental energy resolution was ≤0.5 eV. Structures due to the Al K$\alpha$ X-ray satellites were subtracted prior to data processing. XPS peak intensities were obtained after the removal of the Shirley background. Spectra calibration was achieved by fixing the Ag $3d_{5/2}$ peak of a clean sample at 368.3 eV; this method turned the C 1s peak of the adventitious carbon contamination at 285.0 eV.[46] Atomic concentration analysis was performed by taking into account the relevant atomic sensitivity factors.[39] The fitting of some XPS spectra was carried out using XPSPEAK4.1 software, by fitting the spectral profiles with symmetrical Gaussian envelopes, after subtraction of the background. This process involved data refinement, based on the method of the least-squares fitting, and was carried out until there was the highest possible correlation between the experimental spectrum and the theoretical profile. The residual or agreement factor $R$, defined by $R = [\sum (F_{obs} - F_{calc})^2 / \sum (F_{obs})^2]^{1/2}$, after minimization of the function $\sum (F_{obs} - F_{calc})^2$, converged to the value of 0.03.

**Atomic Force Microscopy.** The morphology of the SiC samples was also observed by atomic force microscopy (AFM) using a Solver P47 NTD-MDT instrument. The noise level before and after each measurement was 0.01 nm. AFM characterization was performed in a high-amplitude mode (tapping mode, resonance frequency: 150 Hz).

## ASSOCIATED CONTENT

### Supporting Information

The Supporting Information is available free of charge at https://pubs.acs.org/doi/10.1021/acsomega.1c02905.

Representative section SEM analyses of the trenches in the SiC wafer with the related taper angles evidenced (Figure S1); AFM image of the trenches on the SiC wafer (Figure S2); Al K$\alpha$-excited XPS of the 4H-SiC wafer, after the HF + $NH_4F$ treatment, in the F 1s binding energy region (Figure S3); Al K$\alpha$-excited XPS of the 4H-SiC wafer, after the HF + $NH_4F$ treatment, in the S 2p binding energy region (Figure S4); and SiC trench etching process evaluated by interferometric endpoint detection (Figure S5) (PDF)

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