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Review

Compact Galvanically Isolated Architectures for Low-Power DC-DC Converters with Data Transmission

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Abstract: This paper reviews state-of-the-art architectures for galvanically isolated DC–DC converters with data transmission for low-power applications. Such applications do not have stringent requirements, in terms of power efficiency, but ask for very compact, highly integrated implementations. To this aim, architecture simplicity is crucial, especially when data transmission and/or output power regulation are required. Since the bottleneck of galvanically isolated systems is the isolation device (i.e., typically a stacked thick oxide or polyimide transformer), the reduction of the number of isolated links, while preserving both power and data functionalities, is the more effective strategy to increase the level of integration, reduce the form factor, and have a lower cost per channel. Specifically, this review compares the pros and cons of different architectures that address this challenge differently from traditional solutions.

Keywords: amplitude shift keying (ASK); electromagnetic coupling; integrated circuits; multiplexing; polyimide; oxide; rectifiers; Schottky diode; system-in-package (SiP); transformers

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1. Introduction

A galvanically isolated system consists of two isolated domains that exchange data signals across the galvanic barrier (see Figure 1). Full isolation is provided if the power supply of domain 2, V_{DD2}, is provided from the power supply of domain 1, V_{DD1}, by means of a galvanically isolated DC–DC converter [1]. Nowadays, galvanic isolation is highly required in low-power applications (i.e., lower than 100 mW), such as factory automation, process control, building automation, portable instrumentation, etc. An important aim is to avoid ground loops in signal conditioning and data transmission. Other significant examples of low-power isolated systems are multichannel sensor interfaces for industrial and medical devices. A common application is to provide an analog-to-digital converter (ADC) with isolated power, along with low data rate communication [2–4], as represented in Figure 2. The supply power on the isolated side is provided by an isolated DC–DC converter, while a digital data isolator performs data transmission from the ADC to the microcontroller unit. Since the power consumption of the ADC is typically about few milliwatts, a low-power DC–DC converter is sufficient, while the specifications for the digital isolator (i.e., data rate, common-mode transient immunity, etc.) manly depend on the custom application. Galvanically isolated DC–DC converters with data transmission are also largely used in isolated gate drivers for motor drive in industrial and automotive applications, typically based on a half-bridge topology for n-type power switches [5]. Gate drivers (GDs) are the interface between the controller and the power stage. They minimize both the conduction loss and switching time of the power switching devices, while avoiding destructive conditions that occur when both devices, M_1 and M_2, are conducting at the same time. Figure 3 shows a simplified scheme of fully isolated GDs, including both an

isolated power converter and data transfer interface for high-side power supply and amplifier driving (GD_A and GD_B), respectively.

GD applications often require isolated power levels well above 100 mW, consequently high-power transfer efficiency (PCE) is mandatory, which limits the effectiveness of fully integrated solutions [6,7]. It is worth noting that in half-bridge GD applications (Figure 3), the main data transmission (i.e., from controller to GDs) has the same direction of the power transfer, whereas in isolated ADC applications (Figure 2), it has the opposite direction (i.e., from the ADC to MCU). This is an important difference for the definition of the architecture of galvanically isolated DC–DC converters with data transmission. Finally, although not highlighted in Figures 2 and 3, an isolated power converter usually requires an additional isolated data link in the opposite direction of the power link for the output power regulation.

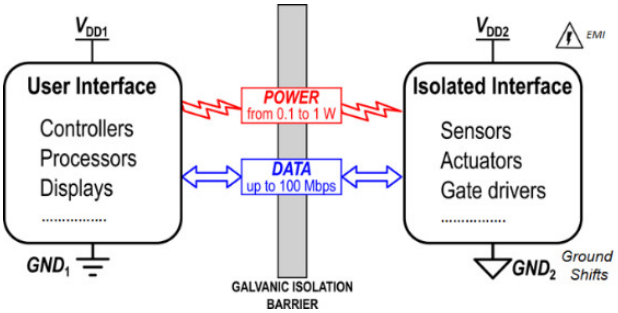


Figure 1. Simplified block-diagram of a galvanically isolated system. Reproduced from [1]. Copyright 2019, Springer Nature Customer Service Centre GmbH.

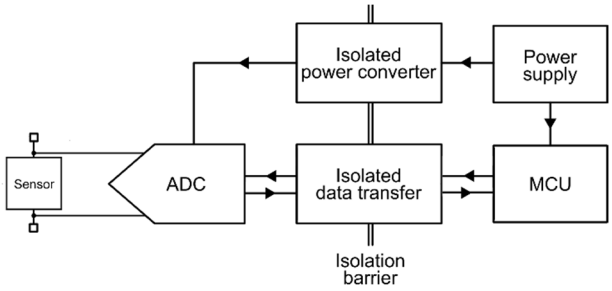


Figure 2. Simplified scheme of an isolated ADC for a sensor interface.

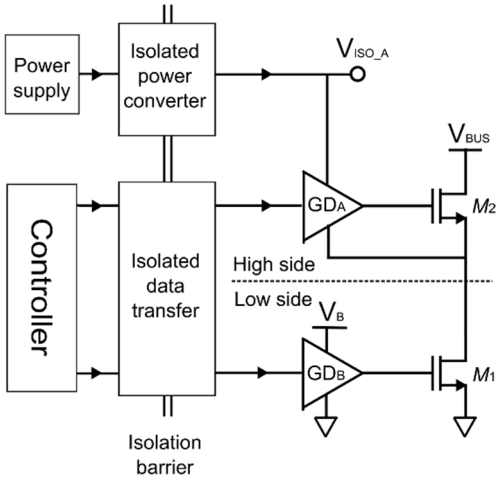


Figure 3. Simplified scheme of an isolated gate driver application for half-bridge configuration.

In this scenario, small form factor, multi-channel capability, and low cost per channel drive the next generation of isolated DC–DC converters [8]. This review presents the most

promising architectures proposed in the last years for low-power galvanically isolated DC–DC converters with data transmission. Specifically, it describes the most interesting architectures aimed at reducing the number of isolated links and, hence, meeting the demanding request of lower form factor and reduced cost per channel, while preserving both power and data functionalities.

The paper is organized as follows. Section 2 reviews selected architectures for low-power, galvanically isolated DC–DC converters, in comparison with the traditional commercial implementations. Two main applications are discussed, i.e., isolated ADCs and isolated half-bridge GDs. Section 3 summarizes and compares the pros and cons of the described architectures, while Section 4 draws main conclusions, highlighting the most promising research trends.

2. Compact Architectures for Highly Integrated Isolated DC–DC Converters

Highly integrated DC–DC converters are mainly based on isolation transformers that exploit the inductive coupling between stacked metal windings isolated by a dielectric layer of a proper thickness (i.e., silicon dioxide or polyimide) [6–13]. Isolation transformers enable power transfer up to several hundreds of milliwatts, with maximum power efficiencies of about 30% [11,14]. The inductive approach is suited to data transmission with high common-mode transient immunity (CMTI) performance [15]. Finally, isolation transformers can be fabricated to withstand isolation ratings from basic to reinforced [16].

Traditional architectures for integrated isolated systems exploit several physical isolated links, each of them requiring a dedicated isolation component. In other words, such architectures include at least four isolation devices (e.g., transformers). Specifically, they include an isolated link for the power transmission (i.e., the isolated power link), an isolated link for the feedback path for power regulation, and at least two isolated data links for bidirectional data communication. Such architectures have been widely adopted for commercial implementations.

A typical example, reported in Figure 4, depicts an isolated DC–DC converter using dedicated transformers for power transfer, control feedback, and bidirectional data channels, respectively [10]. Due to the high complexity, a system-in-package (SiP) approach is often exploited by using stand-alone, post-processed isolation devices, instead of integrated ones [13,17]. Isolation capacitors can be used for both data and control feedback channels in the place of transformers with some advantage, in terms of package size [18]. This architecture is highly flexible and can be used for both applications shown in Figures 2 and 3.

However, for a significant decrease of the overall isolator size and cost, the reduction of the number of isolated links is mandatory, as schematically represented in Figure 5 [19–23]. Research efforts have been addressed to share the same isolation device for more than one functionality (i.e., power, data, and control). Hereinafter, promising architectures are fully discussed, with a special focus on low-power isolated ADC applications, in which the main data transmission is in the opposite direction, with respect to the isolated power transfer one. Section 2.4 is, instead, dedicated to isolated GDs, which have different architectural requirements and, therefore, need different solutions.

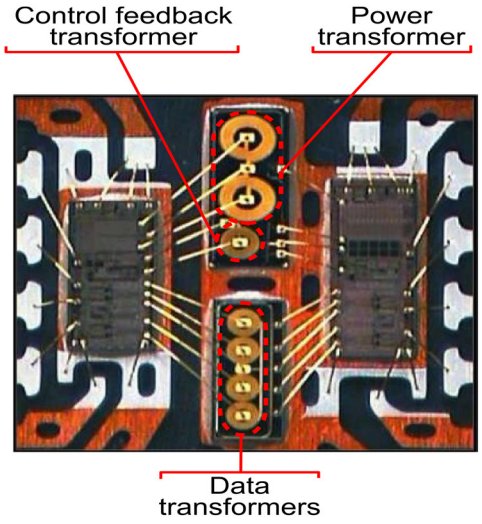


Figure 4. Die photograph of an isolated DC–DC converter with data links. Reproduced from [10]. Copyright 2008, IEEE.

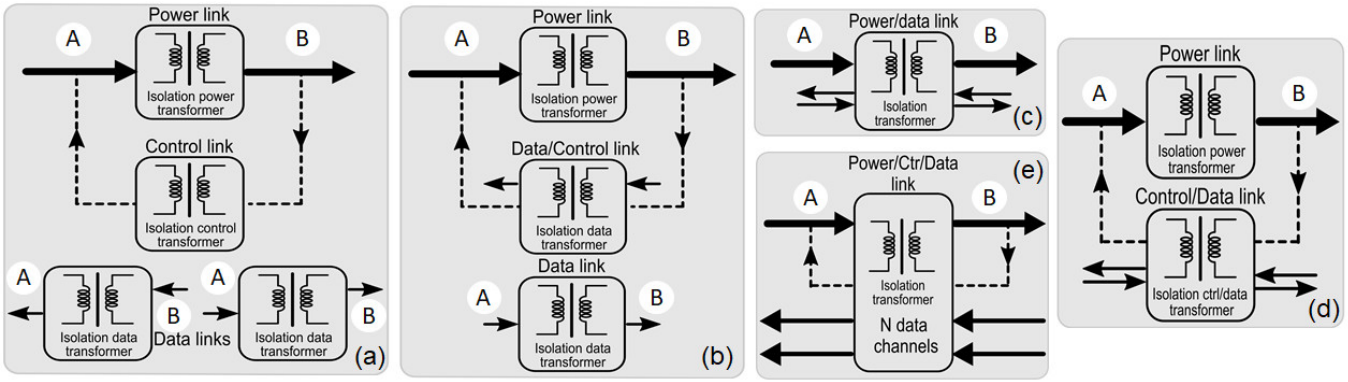


Figure 5. Architectures for galvanically isolated power/data transfer systems: (**a**) Traditional [19]. (**b**) In [20]. (**c**) In [21]. (**d**) In [22]. (**e**) In [23]. Reproduced from [17]. Copyright 2019, IEEE.

2.1. Triple Transformer Architecture for Low-Power Isolated ADC

The traditional architecture in Figure 5a can be simplified by getting rid of the dedicated control link for power regulation. Indeed, the control bit stream can be multiplied along with the data stream (from B to A) on the same physical isolated link. Typically, this is compatible with most DC–DC applications, since the bitrate for power regulation is quite low and, hence, data multiplexing does not significantly degrade the overall performance. Of course, bidirectional communication requires a third dedicated data link (from A to B). Basically, a triple transformer architecture includes a power transformer and two data transformers for bidirectional communication, while multiplexing data, along with the control bits on the same transformer (from B to A).

A triple transformer architecture has been demonstrated in an isolated delta–sigma ADC for shunt-based current sensing in [20]. The isolated ADC was implemented with a SiP approach, by means of polyimide power/data transformers providing 5-kVrms isolation (see Figure 6 for cross-section and the top-view of the isolation power transformer). The block diagram and the die photograph of the isolated ADC with triple transformers are shown in Figure 7a and 7b, respectively. This solution can be simplified into a double transformer architecture by eliminating a data transformer, only for the applications in which bidirectional communication is not required.

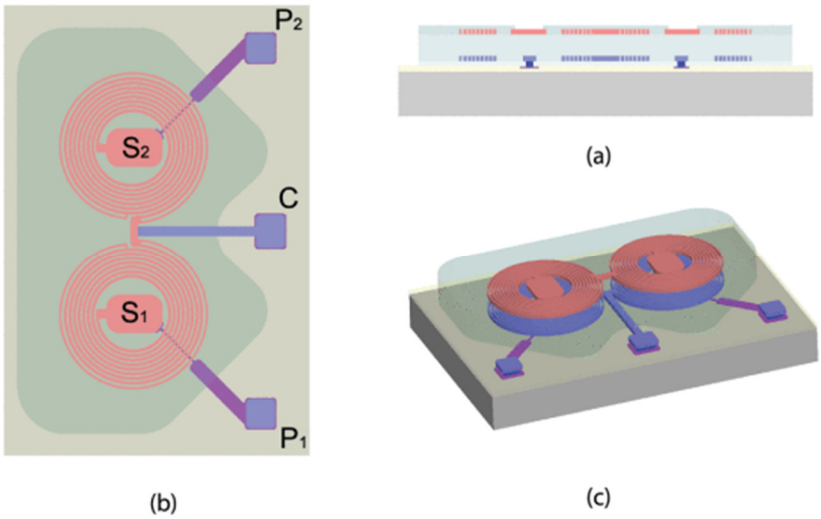


Figure 6. Isolation polyimide transformer. (**a**) Cross-section. (**b**) Top-view. (**c**) Three-dimensional view. Reproduced from [20]. Copyright 2016, IEEE.

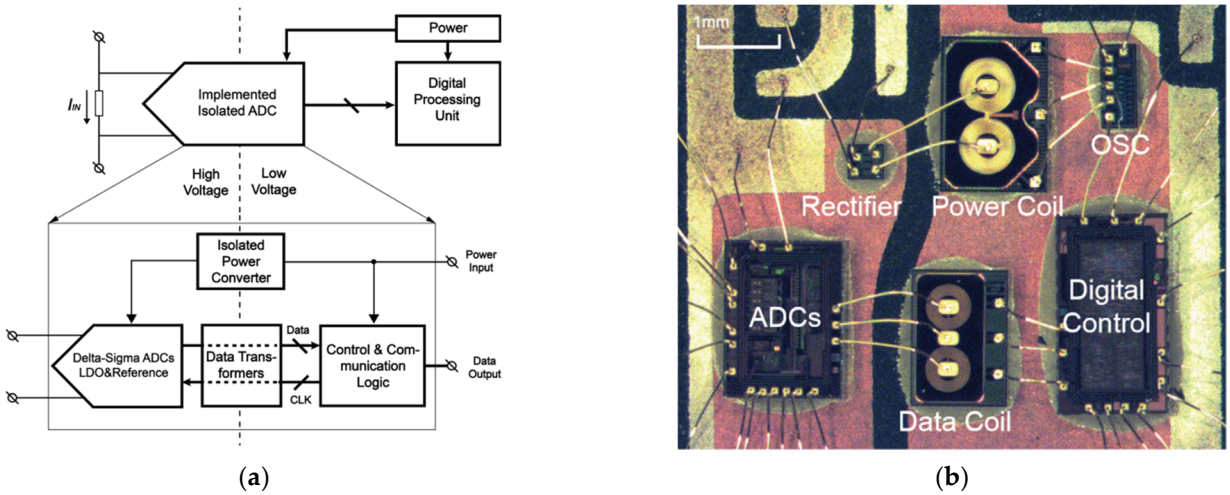
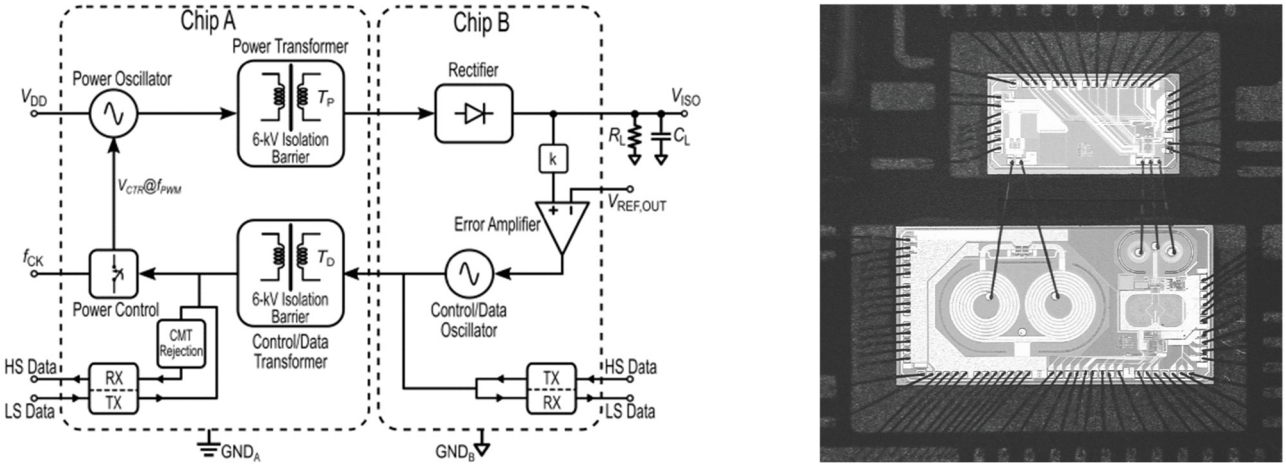


Figure 7. Isolated delta–sigma ADC (**a**) Block diagram. (**b**) Micrograph. Reproduced from [20]. Copyright 2016, IEEE.

2.2. Double Transformer Architecture for Low-Power Isolated ADC

An effective reduction of the isolated links can be achieved by using a bidirectional, half-duplex data communication. A novel solution has been proposed in [24] and consists of a dedicated isolated link for high-efficiency power transfer and an isolated signal link, used for both output voltage/power regulation and bidirectional half-duplex data communication, as represented in Figure 5d.

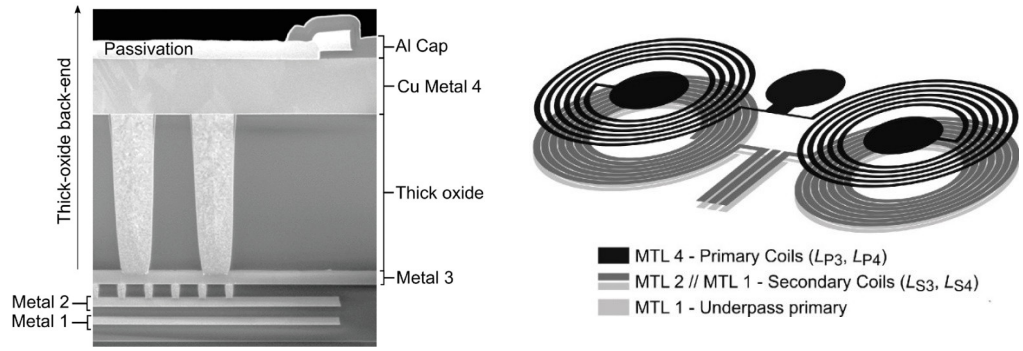
The architecture was implemented in [22], according to the block-diagram shown in Figure 8a. The power link is made up of a 350-MHz power oscillator, an isolation transformer, and a power rectifier. The output voltage, V_{ISO}, is regulated by a feedback control link, consisting of a low-power 900-MHz oscillator, whose oscillation amplitude changes according to the output power. The oscillation voltage of the RF oscillator is the control variable that drives the power control block to turn the power oscillator on and off. The control link is also exploited for bidirectional half-duplex data communication, by means of amplitude shift keying (ASK) modulation of the RF oscillation signal. The high-speed (HS) data stream from chip B to chip A includes a common-mode transient (CMT) rejection block, in order to improve CMTI. On the other hand, a low-speed (LS) data communication from chip A to chip B is also provided for those applications where configuration data are required to set chip B operation.



(**a**) (**b**)

Figure 8. DC–DC converter with bidirectional data communication (**a**) Block diagram. (**b**) Micrograph. Reproduced from [22]. Copyright 2018, IEEE.

The photograph of the isolated converter is reported in Figure 8b. It consists of only two dice, since on-chip thick oxide isolation transformers are used for both power and data/control links. The scanning electron microscope (SEM) cross-section of the adopted thick oxide technology is shown in Figure 9a. This technology enables isolation ratings up to 6 kV. Figure 9b depicts the layout view of the data/control transformer of the converter, which adopts a *S*-shape coil connection to improve the EM immunity (EMI) of the data link and, therefore, avoid bit error rate degradation due to external magnetic fields.



(**a**) (**b**)

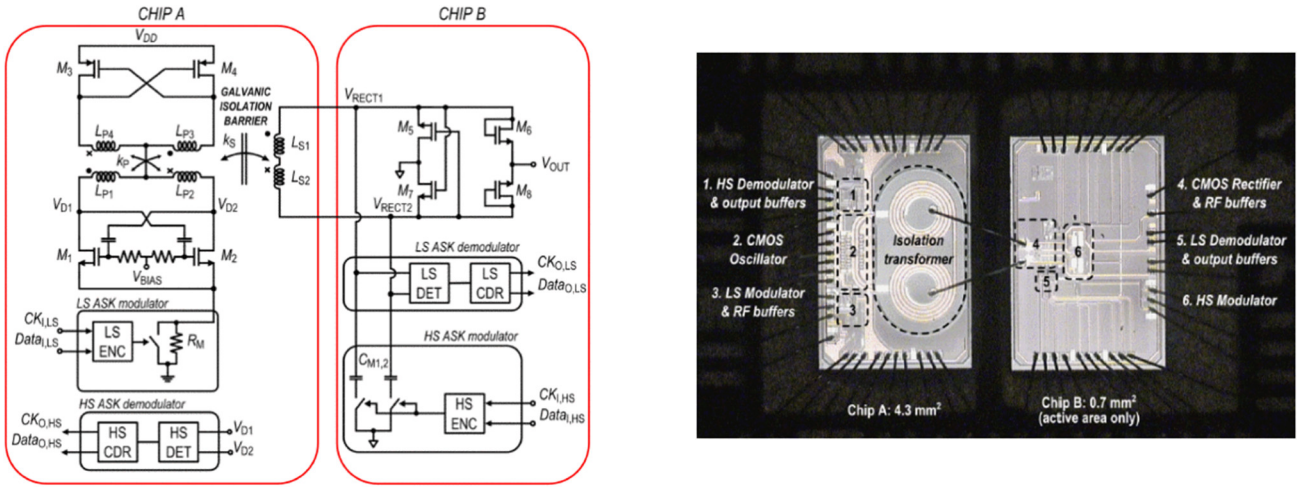
Figure 9. Isolation thick oxide transformer. (**a**) SEM cross-section. (**b**) Layout view of the data/control transformer with *S*-shape. Reproduced from [22]. Copyright 2018, IEEE.

2.3. Single Transformer Architectures for Low-Power Isolated ADC

The very first single-transformer architecture with data transmission capability (see Figure 5c) was patented in [25]. A fully CMOS implementation was presented in [21]. This system is able to transfer both power and data through the same power transformer. Bidirectional half-duplex data communication is achieved by means of an ASK modulation of the power oscillating signal at the primary and/or secondary windings of the power transformer, using a low modulation index to preserve efficiency. The block-diagram and the micrograph of this single-transformer power transfer system with bidirectional data communication are shown in Figure 10a and 10b, respectively. The system exploits the same on-chip isolation transformer technology shown in Figure 9a. Unfortunately, this solution can be adopted only when output regulation is not required, since the power control signal is not provided. Moreover, it has a poor CMTI performance, due to primary

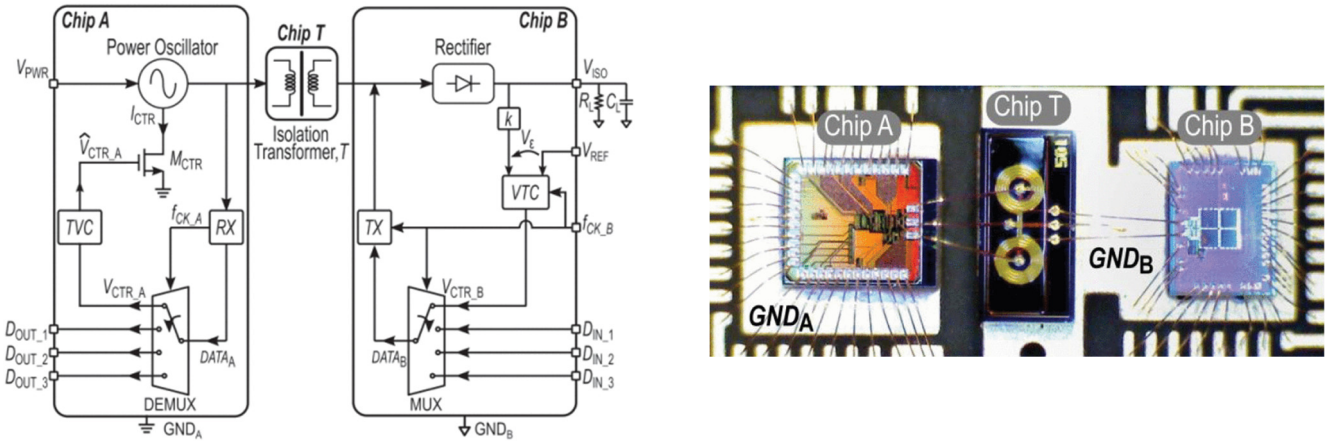
to secondary winding capacitances, especially when a large power transformer is used for better efficiency.

To overcome both limitations, the alternative single-transformer architecture (Figure 5e) can be used. It is a new patented solution [26], which makes compliant both regulated power and data functionalities on the same isolation transformer link. The architecture was implemented in [23] according to the block-diagram in Figure 11a, while the micrograph is shown in Figure 11b. Although this system is well-suited to a two-chip SiP, by using thick oxide isolation, an isolation approach based on a stand-alone polyimide transformer was used. The SEM cross-section and the layout of the adopted polyimide-based transformer are shown in Figure 12a,b. Differently from the widely adopted on/off control scheme, the dc output power is regulated by means of a continuous-time feedback loop. In this way, the power oscillator is always on, thus enabling the power signal modulation for data communication and feedback control. The control data are multiplexed together with the bitstream of N data channels and then transmitted across the galvanic barrier (from B to A) by means of an ASK modulation of the power signal.



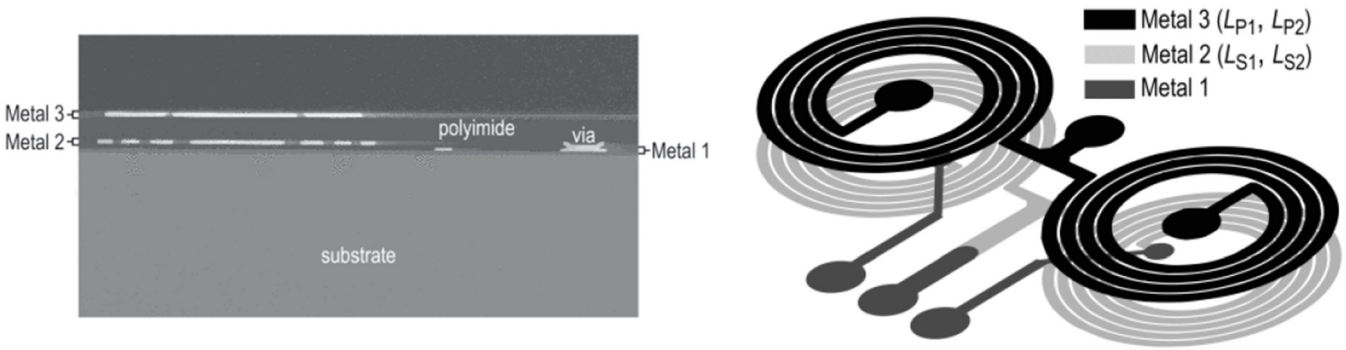
(**a**) (**b**)

Figure 10. Single-transformer DC–DC converter with bidirectional data communication (**a**) Block diagram. (**b**) Micrograph. Reproduced from [21]. Copyright 2016, IEEE.



(**a**) (**b**)

Figure 11. Single-transformer DC–DC converter with bidirectional data communication and power regulation. (**a**) Block diagram. (**b**) Micrograph. Reproduced from [23]. Copyright 2020, IEEE.



(**a**) (**b**)

Figure 12. Isolation polyimide transformer (**a**) SEM cross-section (**b**) Layout view. Reproduced from [23]. Copyright 2020, IEEE.

On side A, a receiver with a demultiplexer recovers data, control, and clock signals. The recovered data bitstream is allocated on the output data channels, whereas the low-frequency control signal performs a continuous-time power oscillator regulation. This last architecture is well-suited for sensor applications, since CMTI and power conversion efficiency performance must be properly traded off, due to the use of a single isolation transformer. The proposed DC–DC converter architecture is also compatible with bidirectional half-duplex communication with data rates of at least 5 Mbit/s from chip A to chip B, as in [21,22]. It is worth mentioning that, during chip A to chip B communication the power control is disabled (i.e., data transfer from chip B to chip A is not possible at the same time), but no effect on the isolated supply voltage, V_{ISO}, occurs (being the time constant of the load in the order of milliseconds).

2.4. Compact Architectures for Isolated Half-Bridge GDs

As already said in Section 1, isolated half-bridge GD applications are hardly compliant with a fully integrated approach, due to excessively high levels of isolated power (well above 100 mW) and inadequate PCE performance of standard micro-transformer technologies [13,27]. Indeed, typical PCE values for a traditional isolation process (i.e., without magnetic materials) are around 30% [6,7,11,28], with a record of 34% [14,29]. On the other hand, the adoption of magnetic materials [30,31] or glass-based fan-out wafer-level packaging [32] demonstrated enabling a PCE of about 50%, at the expense of higher complexity and fabrication costs. Specifically, only data transfer functionalities (i.e., without isolated power transfer) are usually implemented with an integrated approach, either adopting transformer-based [33] and capacitive isolation devices [34] or a package-scale isolation barrier with RF planar coupling [35–37]. On the other hand, high-power, high-efficiency isolated DC–DC conversion is still implemented by means of an off-chip, discrete transformer. For these reasons, very few innovative solutions have been proposed for isolated half-bridge GD applications. With reference to Figure 3, as isolated half-bridge GD (high-side) requires the following isolated links:

1. Power link for GD/diagnostic circuit power supply (left to right);
2. Data link for power regulation (right to left);
3. Data link for GD PWM (left to right);
4. Data link for configuration (left to right);
5. Data link for monitoring (right to left).

An isolated PWM GD with auxiliary energy and bidirectional FM/AM signal transmission via single transformer has been presented in [38]. Compared to [21], it allows bidirectional communication by exploiting FM/AM transmission in the place of AM/AM one. However, both isolated (auxiliary) power and data rates are lower than in [20];

specifically, the data rate for PWM is too low (only 1 Mbit/s) for GD application, thus making this architecture more suited to isolated ADCs.

A new architecture has been proposed in [39]. The work exploits a dual-frequency shift keying (FSK) modulation without an external reference clock to implement two independent data links (i.e., up to 21 Mbit/s and 500 kbit/s for the GD PWM and configuration data, respectively), along with a low-power link (i.e., 123 mW with 23% PCE only for diagnostic circuit power supply) on the same isolation stacked transformer, fabricated on a flexible PCB with 25-µm copper layers and 100-µm isolator. A third isolated data link is also implemented for monitoring, with a maximum data rate of 14 Mbit/s, by using another isolation PCB transformer (adopting a concentric configuration with the first transformer to save space). Despite the low integration level, due to the PCB isolation transformers, the architecture is very interesting for reducing the number of physical isolated channels.

Another compact architecture for isolated GDs has been patented in [40]. The proposed solution takes advantage of two synchronized coupled oscillators [41] to transmit isolated power and data on the same transformer link, while being compliant with power regulation, according to the simplified schematic in Figure 13. Specifically, the first oscillator, OSC 1, is used for simultaneous data transmission (at low bit rate) and constant power transfer, while the second synchronized oscillator, OSC 2, is used for variable power transfer (to guarantee output power regulation, thanks to PWM-controlled turn-off circuitry). Half-duplex bidirectional communication is implemented by means of backscattering at the secondary coil of the isolation transformer and can be used for output power control.

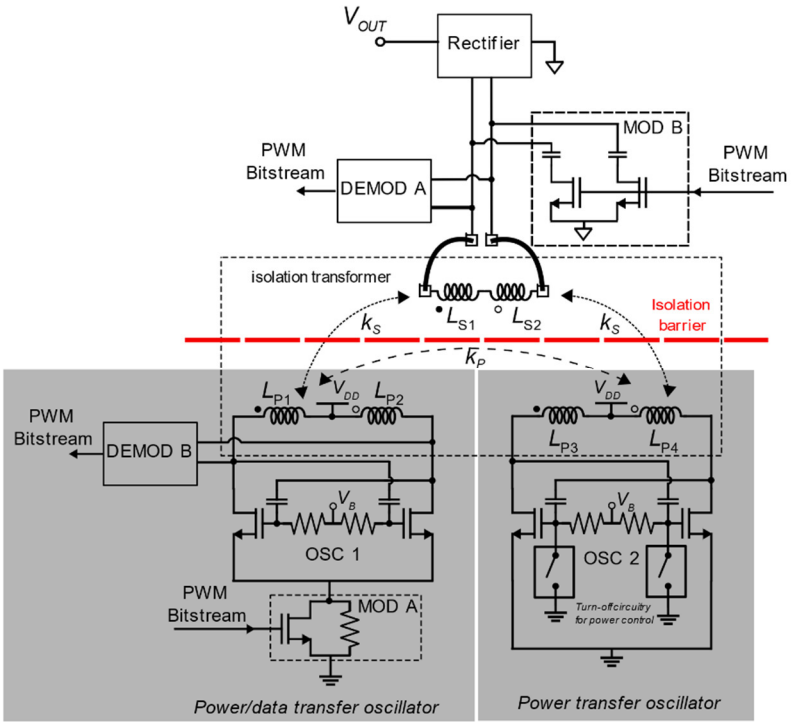


Figure 13. Simplified schematic of compact architecture for isolated GDs based on synchronized coupled oscillators.

3. Architecture Comparison for Low-Power Isolated ADC

The performance of the analyzed DC–DC architectures for low-power isolated ADC is compared in Table 1. Several considerations arise from this comparison. The commercial architectures, such as [19], are developed for maximum flexibility to allow an easy use

in all applicative environments. This is accomplished by means of dedicated isolated links for power, control, and bidirectional data, at the cost of lower-level integration and higher costs. High isolated power and conversion efficiency are achieved, thanks to a customized power transformer and pulse-width modulation (PWM) control scheme, while bidirectional high data rate communication is provided. It is worth mentioning that isolation rating and CMTI performance are highly related to the isolation technology.

On the other hand, more compact solutions [20] can be used in customized applications with an acceptable reduction of flexibility or performance. The key point is sharing functionalities on the same isolation physical channel. Two main strategies are exploited, i.e., data multiplexing and ASK modulation of a RF carrier. Data multiplexing can be used to share the isolation transformer for data and control bits, as in [20], by using a simple bang–bang control scheme to minimize the required bitrate. ASK modulation can be exploited either on the control channel to implement half-duplex communication, as in [22], or on the power channel in the unregulated converter of [21]. Moreover, both techniques (i.e., ctrl/data multiplexing and ASK modulation) can be combined in the single-transformer architecture of [23], provided that a continuous-time control scheme is adopted in the place of a PWM one. Of course, such simplifications limit both output power and efficiency performance, especially in single-transformer architectures, where a design tradeoff must be done for the isolation component. However, the benefits, in terms of level of integration, form factor, and lower cost per channel are significant with a reduction of chip number and area consuming isolation devices (see last two rows of Table 1).

Table 1. Performance comparison of DC–DC converter architectures for low-power isolated ADC.

Parameters	[19]	[20]	[21]	[22]	[23]
Supply voltage [V]	3.3	3.3	3	3.3	5 [(1)]/1.8
Isolated output voltage [V]	3.3	3.3	2 [(2)]	3.3	3.3
Max. output power [mW]	116	9.1	20.4	93	50
Power efficiency [%]	20	22	9	19	14
Oscillation frequency [MHz]	180	200	330	350	300
Control scheme/frequency [kHz]	PWM/625	Bang-bang/1700	n.a. [(2)]	PWM/100	Continuous-time
Data carrier frequency [MHz]	n.a. [(3)]	n.a. [(3)]	330	850	300
No. of data/configuration channels	2/0	3 [(4)]/1	1/1 [(5)]	1/1 [(5)]	3 [(4)]/0
Max channel data rate [Mb/s]	25 (×2)	1.7 (×3)	40	50	10 (×3)
Maximum isolation level	Basic	Reinforced	Basic	Basic	Reinforced
CMTI [kV/μs]	35	n.a.	n.a.	50	50
Silicon technology	HV-CMOS Schottky diode	0.25-μm CMOS 0.35-μm DMOS Schottky diode	0.35-μm BCD		0.18-μm BCD 0.13-μm CMOS Schottky diode
Isolation technology	Post–processed polyimide transformer with Au metals		Integrated SiO_2 transformer with Cu/Al metals		Post–processed polyimide transformer with Au metals
No. of transformers	4 (1 power, 1 ctr, 2 data)	3 (1 power, 2 data/ctrl)	1	2 (1 power, 1 data/ctrl)	1
No. of dice	4	6	2	2	3

[(1)] Power oscillator supply voltage; [(2)] output voltage is not controlled; [(3)] pulse modulation; [(4)] 3 multiplexed data channels; [(5)] half-duplex.

4. Conclusions

In this review, the most promising research trends for galvanically isolated DC–DC converters have been discussed, with the aim of providing the reader with alterative architectures for highly integrated compact implementations. The reduction of the number

of isolated links, while preserving both power and data functionalities, is crucial. The evaluation of the most suited architecture must be done according to the specific application requirements (i.e., isolated output power, data rate, power regulation, half/full duplex, and CMTI). To this aim, Table 2 can drive the designer into this evaluation phase, guaranteeing an aware choice.

Table 2. Galvanically isolated DC–DC converter with data communication for low-power ADC: architecture selection.

Architeture	Power Link	Data Communication	Isolated Power Regulation	Data Rate	CMTI
Triple-transformer	Dedicated	Full duplex	YES (e.g., Bang-bang)	Medium	Mainly limited by the isolation technology
Double-transformer	Dedicated	Half-duplex	YES (PWM)	Medium/high	Mainly limited by the isolation technology
Single-transformer	Shared with data	Half-duplex	NO	Medium/high	Tradeoff with power efficieny conversion
Single-transformer with ouput power regulation	Shared with data/ctr	Half-duplex	YES (continuous-time)	Medium	Tradeoff with power efficieny conversion

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