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An Experimental Comparison of Galvanically Isolated DC-DC Converters: Isolation Technology and Integration Approach

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Abstract: This paper reviews state-of-the-art approaches for galvanically isolated DC-DC converters based on radio frequency (RF) micro-transformer coupling. Isolation technology, integration level and fabrication issues are analyzed to highlight the pros and cons of fully integrated (i.e., two chips) and multichip systems-in-package (SiP) implementations. Specifically, two different basic isolation technologies are compared, which exploit thick-oxide integrated and polyimide standalone transformers, respectively. To this aim, previously available results achieved on a fully integrated isolation technology (i.e., thick-oxide integrated transformer) are compared with the experimental performance of a DC-DC converter for 20-V gate driver applications, specifically designed and implemented by exploiting a stand-alone polyimide transformer. The comparison highlights that similar performance in terms of power efficiency can be achieved at lower output power levels (i.e., about 200 mW), while the fully integrated approach is more effective at higher power levels with a better power density. On the other hand, the stand-alone polyimide transformer approach allows higher technology flexibility for the active circuitry while being less expensive and suitable for reinforced isolation.

Keywords: basic isolation; electromagnetic coupling; gate drivers; integrated circuits; polyimide; rectifiers; reinforced isolation; Schottky diode; silicon dioxide; system in package; transformers

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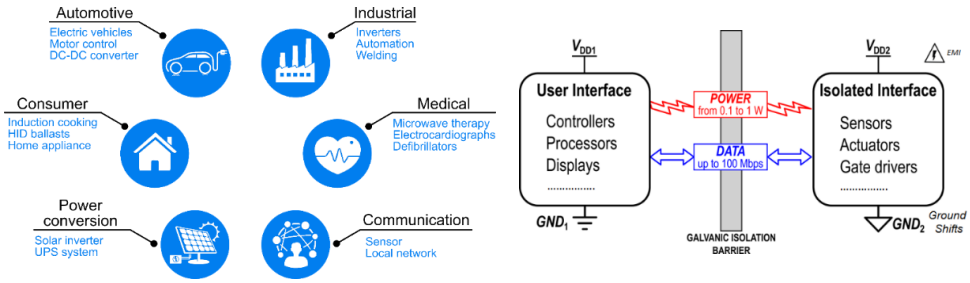
1. Introduction

Safety rules for equipment operated by human beings, along with severe reliability requirements for electronics in harsh environments, call for galvanic isolation in several application fields, even at very low power levels, as summarized in Figure 1a [1]. A typical galvanically isolated system is shown in Figure 1b [1]. It consists of two isolated domains (i.e., with different isolated ground references) that exchange data signals across the galvanic barrier. However, full isolation is provided only if the power supply of Domain 2, V_{DD2}, is provided from the power supply of Domain 1, V_{DD1}, by means of a galvanically isolated DC-DC converter. Usually, power levels from a few tens of mW to about 1 W can be transferred across the galvanic barrier by means of magnetic coupling. To this aim, micro-transformer devices are currently used, which exploit a dielectric layer between two stacked spiral windings to withstand an isolation voltage of several kilovolts [2,3]. Typically, by using one galvanic barrier (i.e., one transformer), the basic isolation level can be achieved (i.e., about 5–6 kV). Reinforced isolation, which is the highest level of isolation, requires the use of two galvanic barriers connected in series (i.e., double isolation) in order to comply with the 10-kV surge test of the VDE 0884-11 standard [4]. Double isolation for a power transfer has been demonstrated by using an LC hybrid approach (i.e., an isolation capacitor and an isolation transformer in a resonant mode operation), which boosts efficiency with respect to a traditional two-series-connected scheme [5]. However, less costly solutions for reinforced isolation rely on one galvanic barrier by means of an isolation transformer with increased thickness for the dielectric layer [6,7].



(**a**) (**b**)

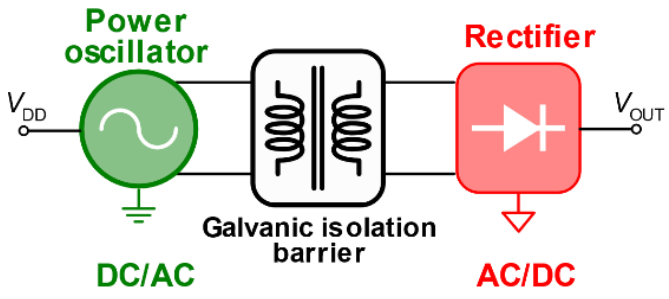
Figure 1. (**a**) Galvanic isolation application fields; (**b**) simplified block diagram of a galvanically isolated system. Reproduced from [1]. Copyright 2019, Springer Nature Customer Service Centre GmbH.

This paper reviews commonly used transformer-based technologies for galvanically isolated DC-DC conversion, which are based on fully integrated thick-oxide transformers [8,9] and post-processed stand-alone polyamide transformers [7,10,11], respectively. To this aim, isolation technologies are compared by means of previously available results and new experimental data of a DC-DC converter specifically designed and implemented. The comparison is carried out at a similar isolation rating (i.e., 5 kV) in terms of electrical performance (i.e., isolated output power and efficiency), integration level, design flexibility and fabrication costs in order to highlight the pros and cons of the two approaches.

The paper is organized as follows. Section 2 describes the system architecture and main circuit topologies for galvanically isolated DC-DC converters, while the characteristics of the two isolation technologies under comparison are detailed in Section 3. Section 4 presents the design and experimental performance of a 5-kV 200-mW DC-DC converter for gate drivers, along with a wide comparison between the integration technologies for power transfer applications.

2. Galvanically Isolated DC-DC Conversion: System and Circuit Description

A galvanically isolated DC-DC converter requires a transformer-based power link to exploit the magnetic coupling between two isolated windings, according to the general scheme in Figure 2. When isolated power regulation is required, a further isolated data link (not represented in Figure 2) must be included for the feedback control, which typically uses a pulse-width modulation (PMW) approach [9]. In common implementations (see Figure 2), the DC-AC conversion is performed by a radio frequency (RF) power oscillator, while a diode rectifier is used for the AC-DC conversion of the isolated voltage at the secondary winding. The isolation transformer can be also used for the voltage step-up, as required by gate driver applications, typically operated at about 20 V.



$$\eta = \frac{P_{OUT}}{P_{DD}} = \eta_{OSC} \cdot \eta_{TRASF} \cdot \eta_{RECT}$$

Figure 2. Galvanically isolated DC-DC converter scheme and power efficiency expression, η.

The crucial performance of an isolated power link is its power efficiency, η. Indeed, it limits the maximum reliable output power due to thermal dissipation issues. The overall efficiency of the isolated power link is mainly determined by the product of the efficiencies of the three main building blocks (i.e., η_{OSC}, η_{TRASF} and η_{RECT}). Therefore, it is mandatory to maximize each contribution to obtain a significant DC-DC performance. As far as the power oscillator is concerned, transformer-loaded implementations are straightforward, as the primary winding can be easily used for the LC tank. On the other hand, transistor availability in the adopted integration technology drives the choice of the circuit topology. The main oscillator topologies for the DC-AC conversion are shown in Figure 3. The most efficient solution is the *D*-class oscillator with cross-coupled transistors working as power switches (Figure 3a), which boosts the drain voltages above the supply voltage, V_{DD} [12,13]. Unfortunately, this solution requires the cross-coupled pair to be implemented with special transistors with very high breakdown for drain voltage, such as the laterally diffused transistors (LDMOS) that are usually integrated into the bipolar-CMOS-DMOS (BCD) technologies [14,15]. In this topology, capacitors C_B are used to perform a voltage partition with the gate capacitance of $M_{1,2}$, thus properly setting the V_{GS} peak to prevent gate-oxide breakdown. If only standard MOS devices are available, as in a CMOS process, the traditional complementary cross-coupled oscillator shown in Figure 3b is an option. It maximizes the oscillation amplitude within the supply voltage, thus avoiding the risk of transistor breakdown while giving the advantage of nearly doubled transconductance at the same current level compared with a simple cross-coupled oscillator. Circuit topologies in Figure 3c,d are enhanced versions of the traditional complementary cross-coupled oscillator [16]. They take advantage of current-reuse (CR) and power, combining techniques to improve both output power and efficiency. On the other hand, they require three-winding isolation transformers with a more complex configuration compared to the other circuit topologies. Proper operation of such oscillators requires frequency synchronization at the primary windings, which can be obtained either with a pure inductive (Figure 3c) [17] or hybrid coupling (i.e., inductive and capacitive as in Figure 3d) between the p-MOS and n-MOS cross-coupled pairs [18].

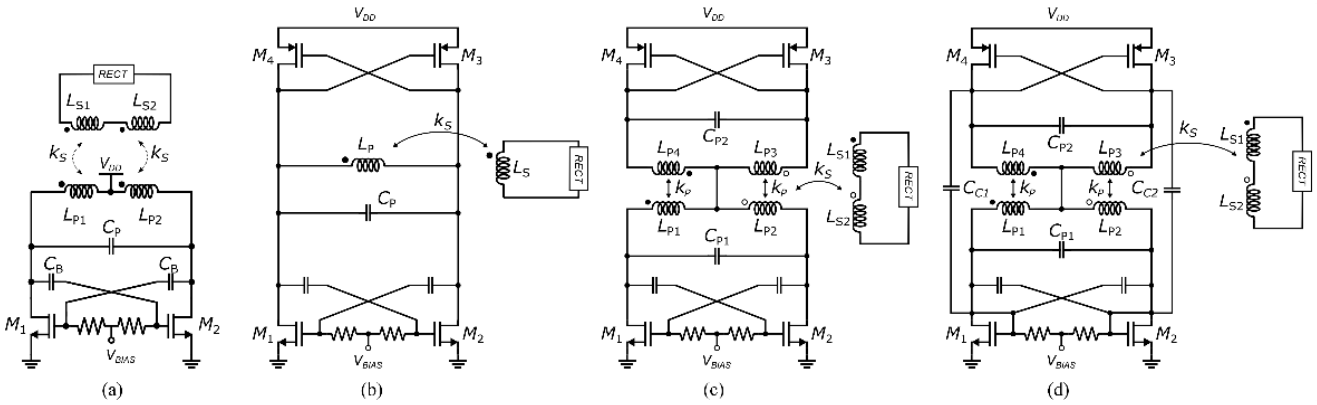


Figure 3. Power oscillator topologies for DC-AC conversion: (**a**) *D*-class oscillator; (**b**) complementary cross-coupled oscillator; (**c**) inductively coupled CR oscillators; (**d**) hybrid-coupled CR oscillator.

Typical isolation transformer configurations for an isolated power link are reported in Figure 4. A traditional stacked transformer with a high turn ratio for voltage step-up is shown in Figure 4a, which is well suited for gate-driver applications. A three-winding transformer can be implemented by means of an interleaved configuration (Figure 4b) for both CR oscillator topologies, while a tapped winding arrangement (Figure 4c) is only compatible with the hybrid coupling one. Due to the three-winding transformer structure, a small voltage step-up can be performed, and therefore, both current-reuse oscillator topologies are suitable for low-/medium-voltage applications. Transformer efficiency, η_{TRASF}, is the very bottleneck of the overall system. It is related to both series and parallel

losses taking place in the metal windings and substrate, respectively [19]. Therefore, it is of utmost importance to use thick conductive layers (i.e., copper or gold), as well as fabricating the transformer on a low-conductivity substrate (<10^4 S/m). A crucial role is also played by the magnetic coupling coefficient, k, between the primary and secondary windings. It is inversely related to the isolation layer thickness and then to the maximum isolation rating of the transformer. The AC-DC conversion is performed by means of a full-wave rectifier. A traditional bridge configuration is preferred for high-voltage applications (i.e., V_{OUT} > 8–10 V) [13,17,18,20], where the diode threshold losses can be tolerated. Alternatively, a simple full-wave rectifier is preferred at the cost of including a center tap connection also for the secondary winding of the isolated transformer [7]. Schottky diodes are mandatory to achieve a rectifier efficiency above 80% while enabling operation in the VHF band. If the adopted technology does not include Schottky diodes, the rectifier can be also implemented by using diode-connected transistors, especially at lower output voltages, also including a threshold compensation scheme [2,5,9].

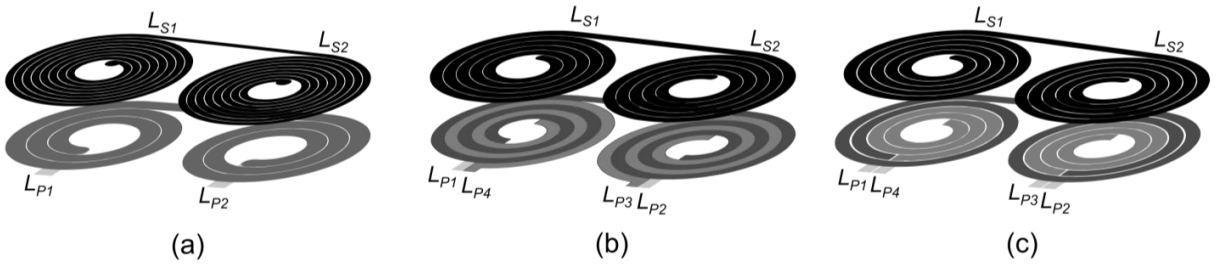


Figure 4. Three-dimensional (3D) views of isolation transformer configurations for DC-DC conversion. (**a**) Stacked topology; (**b**) three-winding interleaved transformer; (**c**) three-winding tapped transformer. Reproduced from [19]. Copyright 2018, Elsevier.

Figure 5 can be used to drive the topology selection for the three building blocks of a galvanically isolated DC-DC converter.

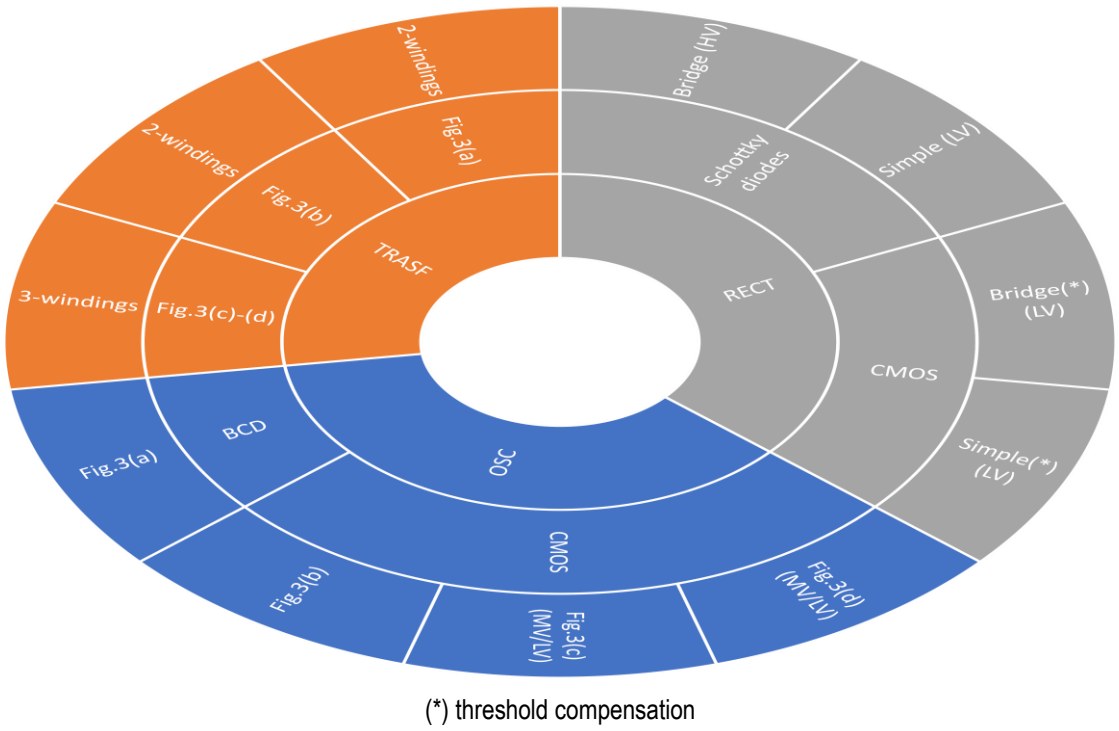


Figure 5. Building block topology selection for galvanically isolated DC-DC converters.

3. Isolation Technology

A crucial role in the performance of a galvanically isolated DC-DC converter is played by the isolation transformer, whose characteristics affect system power efficiency and maximum isolation rating, as well as the integration level and overall costs. Basically, there are two different approaches that are discussed in the following subsections.

3.1. Integrated Isolation Transformers

The first isolation approach adopts integrated transformers (i.e., integrated along with the active circuitry) exploiting a dedicated back end of line (BEOL) with thick silicon dioxide (SiO_2), whose simplified cross-section is shown in Figure 6a. This approach has several important advantages. It enables the highest possible integration level, i.e., two chips per isolated physical channel. Indeed, the isolation transformer can be embedded into the first die by exploiting the on-chip direct connection between the oscillator drains and the transformer primary winding, while the second die hosting the rectifier is connected to the isolated secondary winding through bonding wires, as represented in Figure 7a. Moreover, thanks to the high dielectric strength of silicon dioxide (i.e., about 1000 V/µm), basic isolation can be achieved by using sufficiently close stacked windings, thus keeping the magnetic coupling coefficient, k, quite high. On the other hand, metal layers with limited thickness, t (about 3 µm for the top metals), must be used to comply with the integration process, while very close spacing, s, between winding turns (usually equal to t) can be exploited to increase both the inductance-to-area ratio and Q-factors, as well. A performance limitation of an integrated transformer is its isolation capability, as severe reliability issues (i.e., wafer mechanical stress and second-order breakdown effects) occur when the oxide thickness overcomes approximately 10 µm, which corresponds to basic isolation levels (i.e., 5–6 kV). However, the most limiting drawback of this approach is the need for a low-conductivity substrate (typically lower than 10 S/m) to hinder the energy losses due to the magnetically induced eddy currents [19], which calls for RF-oriented technologies, such as CMOS or BiCMOS. As previously outlined in Section 2, BCD technologies are widely used for high-voltage applications (such as isolated gate driver interfaces), also thanks to the availability of LDMOS devices for efficient D-class oscillators. Typically, BCD platforms are built on a very high conductive substrate (i.e., about 10^4 S/m) to hinder latch-up phenomena. Such a substrate is not compatible with an acceptable efficiency for the isolation transformer. For these reasons, the fully integrated isolation approach can be used only with special BCD technologies, which exploit a silicon-on-oxide-insulation (SOI) substrate (see Figure 6a) with a consequent increase in cost by about 30%.

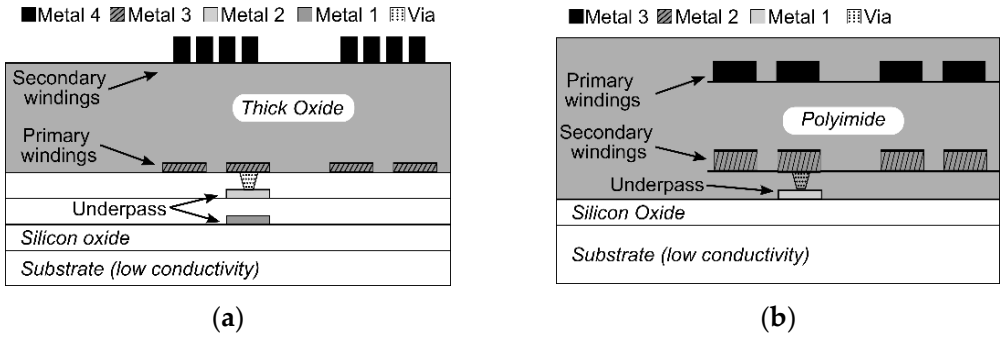


Figure 6. Isolation technology comparison: (**a**) thick-oxide technology; (**b**) polyimide technology.

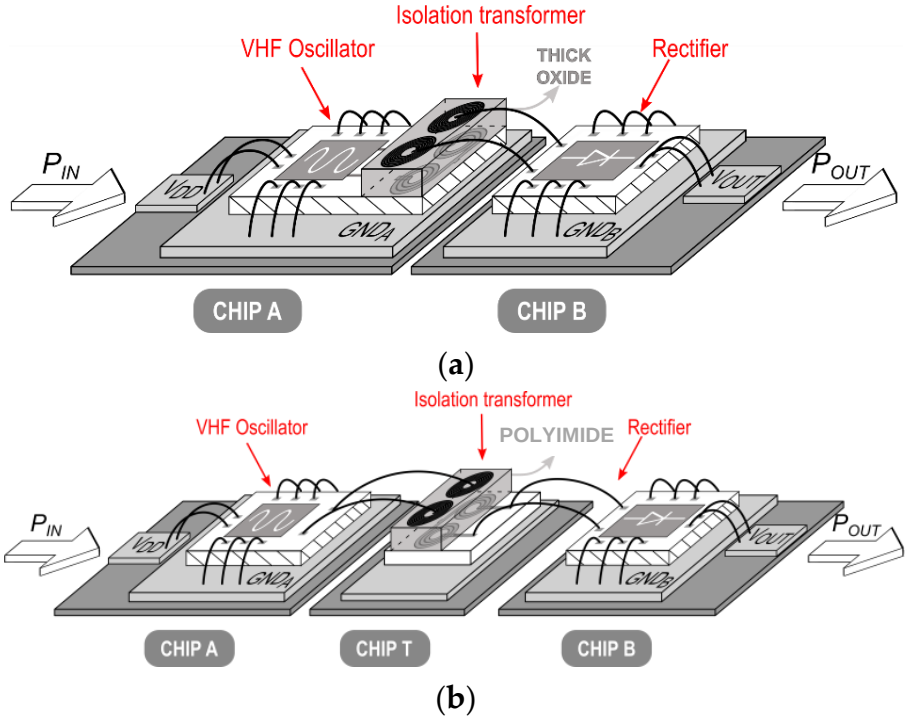


Figure 7. SiP implementation approaches: (**a**) integrated transformer; (**b**) standalone isolation transformer. Reproduced from [19]. Copyright 2018, Elsevier.

3.2. Stand-Alone Isolation Transformers

An alternative isolation technology uses a standalone transformer implemented in a third die by using low-cost fabrication, as shown in Figure 6b. Typically, the adopted dielectric is a polyimide that has been traditionally used in the semiconductor industry for stress relief. It has a lower dielectric strength compared with silicon dioxide (i.e., about 250 V/μm), and thus thicker insulation is required to withstand the same isolation voltage. Consequently, polyimide transformers have a lower magnetic coupling coefficient than silicon oxide transformers at the same isolation rating. Because no constraints are given by active device integration, both substrate and BEOL can be properly chosen to improve winding Q-factors and hence transformer transfer efficiency. To this aim, a low-conductivity substrate and thick Au metals are exploited. However, the use of thick metals could affect the minimum spacing, s, between winding turns, thus limiting both inductance-to-area ratio and Q-factors. The most limiting drawback of this approach is the reduction of the integration level, as three chips are required to implement a single isolated physical channel, as shown in Figure 7b. Specifically, bonding wires are also used to connect the power oscillator drains to the primary (upper) winding of the isolation transformer. This produces additional off-chip parasitics into the main LC tank of the power oscillator and involves the codesign with the isolation transformer in comparison with the fully integrated approach [13]. On the other hand, the standalone transformer technology provides better flexibility in terms of isolation rating, as the polyimide thickness between the transformer windings can be tuned to guarantee different isolation levels (from basic to reinforced one) without significant modifications of the other two chips (i.e., Chips A and B in Figure 7b). Another advantage relies on the complete freedom to fabricate Chips A and B, whose technologies can be chosen without any constraints from the isolation transformer. A final consideration is the overall cost of the galvanically isolated DC-DC converter. It is the result of a combination of silicon and package costs and drives the choice between silicon integrated or standalone transformers. Typically, because silicon area consumption of on-chip transformers prevails in the overall area of die A, the three-chip approach is cheaper than the two-chip approach, thanks to the lower cost of the standalone isolation die.

4. Experimental Comparison

The comparison between the isolation approaches described in Section 3 is carried out by taking advantage of two different technologies by STMicroelectronics, which are based on fully integrated thick-oxide and standalone polyimide transformers, respectively. Figure 8 depicts the scanning electron microscope (SEM) cross-section for both isolation technologies. The thick-oxide technology in Figure 8a is available on 0.35 µm BCD platforms (with an SOI option for power transfer applications). The transformer can be integrated on Chip A along with the oscillator active core (see Figure 7a). An isolation rating of 5 kV is guaranteed by the oxide layer between a Cu-thick metal (Metal 4) and an Al-thin metal (Metal 3) (i.e., 3.7 and 0.9 µm, respectively) [8,13]. A 6-kV isolation level is achieved by using the oxide layer between Metals 3 and 2 [9]. Several experimental results are already available on this isolation technology, which can be used for the proposed comparison. The polyimide technology in Figure 8b is used to fabricate a stand-alone isolation transformer (i.e., Chip T in Figure 7b). A full Au metal back-end is preferred to minimize the winding series resistances. Specifically, two upper 5-µm thick metals are used for the primary and secondary windings, while a 3-µm metal (Metal 1) is exploited for the underpasses. High resistivity substrate is adopted to minimize losses due to both magnetically induced and vertical displacement currents without using any shielding structure requiring additional masks and higher manufacturing costs [21]. The polyimide transformer technology withstands basic to reinforced isolation voltages (i.e., 5 to 10 kV), thanks to a variable insulator thickness (from 20 to more than 30 µm) that is obtained by several deposition steps. The main parameters for the polyimide isolation technology are summarized in Table 1.

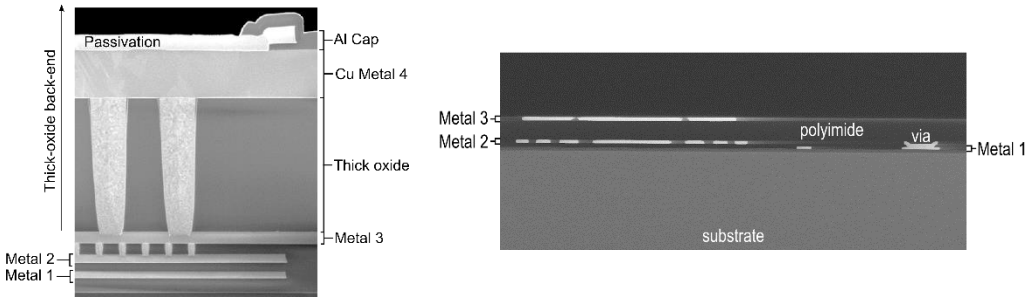


Figure 8. Isolation technology SEM: (**a**) thick-oxide technology. Reproduced from [9]. Copyright 2018, IEEE; (**b**) polyimide technology. Reproduced from [7]. Copyright 2020, IEEE.

Table 1. Main process stack parameters for polyimide isolation technology.

Layer	Permittivity, ε_R	Loss Tangent	Conductivity S/m
Metals	-	-	3.8×10^7
Polyimide	3	<0.01	-
Silicon substrate	11.7	-	0.6

By exploiting the stand-alone polyimide transformer approach, a galvanically isolated DC-DC converter for gate driver applications was specifically designed and characterized for an extensive comparison with the fully integrated thick-oxide technology. For a fair comparison, the basic isolation option was chosen. A three-chip architecture (as depicted in Figure 7b) was used to convert the 5-V voltage supply, V_{DD}, to a 20-V output voltage, V_{OUT}, for a maximum isolated output power, P_{OUT}, of about 200 mW. An operative frequency of about 250 MHz was chosen for the DC-DC conversion as a tradeoff among the efficiency performance of its three building blocks. Chip A was designed in a 0.18-µm BCD technology by STMicroelectronics, which provides high-voltage LDMOS transistors suited for a *D*-class power oscillator (see Figure 3a). It is worth mentioning that the adopted

LDMOS devices have similar performance to those previously used for fully integrated thick-oxide DC-DC converters [9,13]. On the other hand, Chip B was fabricated in the same 0.13-µm CMOS process by STMicroelectronics used in [13,17,18]. Indeed, such technology provides a high-frequency Schottky diode with an elementary active area of 100 µm^2 and a breakdown voltage of 25 V. The rectifier efficiency, η_{RECT}, depends on the number of elementary diode cells in parallel, M. It was set equal to 2 to maximize performance at V_{OUT} and P_{OUT} of about 20 V and 200 mW, respectively. A full-bridge topology was preferred, as the voltage drops across two series-connected diodes are negligible. As far as the isolation transformer is concerned, a fully stacked two-winding topology was adopted to maximize the magnetic coupling coefficient, k. The coil geometry was optimized by means of EM simulations in ADS Momentum. A high turn ratio was chosen to obtain the required step-up voltage. The overall geometrical parameters of primary and secondary windings are reported in Table 2. The microphotograph of the fabricated polyimide isolation transformer (i.e., Chip T in Figure 7b) is shown in Figure 9. The dashed box highlights the 20-µm polyimide layer that is required to guarantee basic galvanic isolation. The transformer secondary primary winding outputs are connected to the rectifier input (V_{R1} and V_{R2}) and to the oscillator open drains (V_{D1} and V_{D2}), respectively, with the center tap available for the voltage supply connection (i.e., V_{DD}). Figure 10 shows the simulated performance of the isolation transformer in terms of inductance and Q-factor of primary and secondary windings as a function of frequency. Table 3 summarizes the electrical performance of the isolation transformer at the operative frequency of 250 MHz.

Table 2. Geometrical parameters of the polyimide isolation transformer.

Transformer Windings	MTL No.	t (µm)	n	w (µm)	s (µm)	d_{OUT} (µm)
Primary	3	5	4.5	53	8.5	1012
Secondary	2	5	12	15.5	8.5	1012

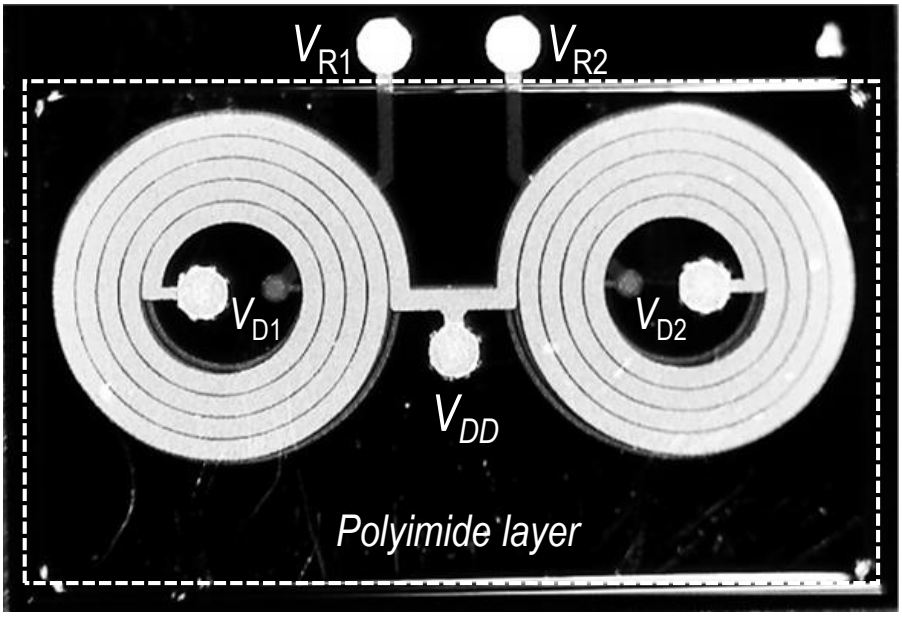
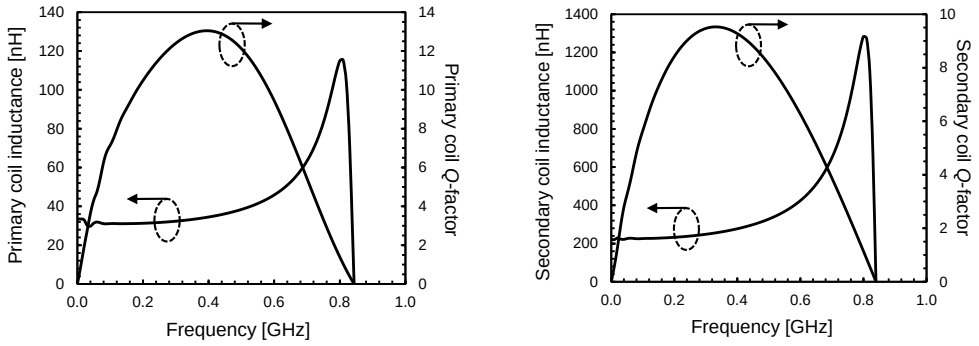


Figure 9. Micrograph of the stand-alone polyimide isolation transformer (Chip T).



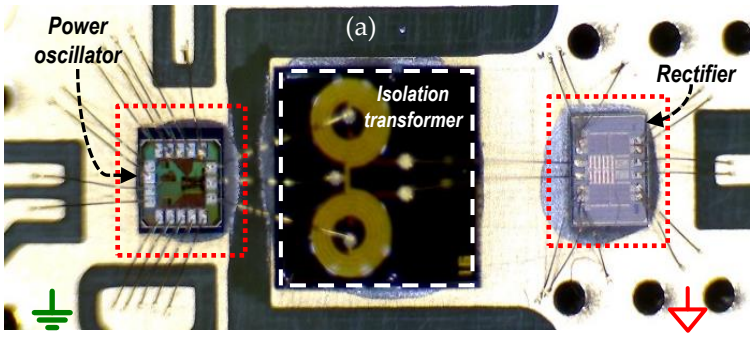
(**a**) (**b**)

Figure 10. Transformer simulated performance: (**a**) primary winding; (**b**) secondary winding.

Table 3. Electrical parameters of the polyimide isolation transformer at 250 MHz.

Transformer Winding	Inductance (nH)	*Q*-Factor	*k*	Self-Resonance Frequency (MHz)
Primary	32	11.6	0.81	840
Secondary	239	9.1		

The DC-DC converter was assembled chip on board for electrical characterization. A photo of the assembled chips, along with the corresponding sizes, is shown in Figure 11a, while the testing printed circuit board (PCB) is depicted in Figure 11b. The DC-DC converter was characterized at increasing dc output voltage, V_{OUT}, from 15 to 20 V by means of a semiconductor parameter analyzer. All measurements were performed at a 5-V power supply, V_{DD}, and room temperature. Figure 12 shows the isolated output power, P_{OUT}, and the power efficiency, η, as a function of the isolated output voltage, $V_{OUT.}$ The DC-DC converter achieves its best performance at a V_{OUT} of about 18.5 V, delivering an isolated output power of 215 mW with 25% efficiency. At a 20-V output voltage, the measured P_{OUT} and η are 200 mW and 24.5%, respectively.



Power oscillator (Chip A)
Tech: 0.18-µm BCD
Size: 1058 µm x 1058 µm

Transformer (Chip T)
Tech: Polyimide isolation
Size: 2400 µm x 2400 µm

Rectifier (Chip B)
Tech: 0.13-µm CMOS
Size: 904 µm x 1214 µm

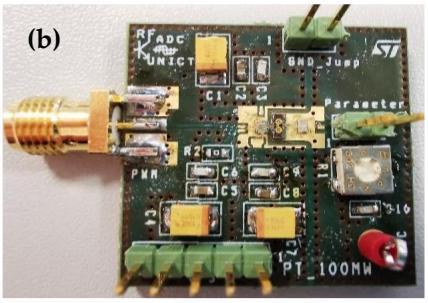


Figure 11. (**a**) Isolated DC-DC converter assembled chip on board; (**b**) testing PCB.

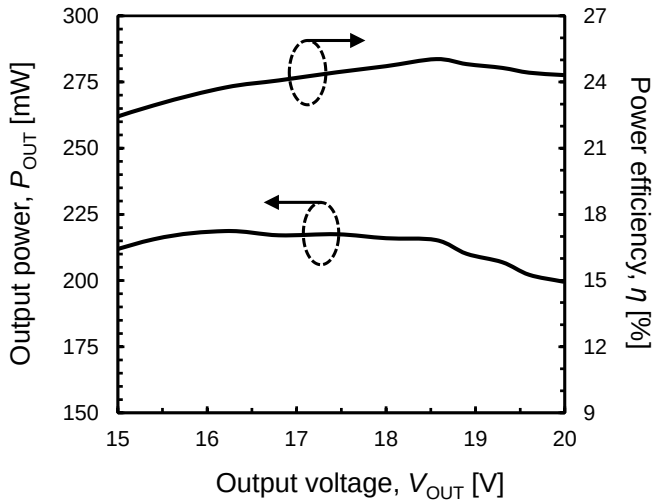


Figure 12. Power efficiency, η, and output power, P_{OUT}, vs. isolated output power.

The experimental performance is summarized and compared with state-of-the-art galvanically isolated DC-DC converters adopting different basic isolation technologies in Table 4. The comparison only includes isolated converters for high-/medium-voltage applications (i.e., with a voltage gain from 1.6 to 4), which require the most complex isolation transformers in terms of turn ratio compared to DC-DC converters with almost unitary voltage gain [3,11]. Moreover, traditional isolation technologies are considered, i.e., without the adoption of magnetic materials, which considerably boost both output power and efficiency performance at the expense of a more complex and expensive process [22].

Table 4. State of the art of isolated DC-DC converters for HV/MV applications (basic isolation).

Refs.	**[13]**	**[18]**	**[19]**	**[20]**	**This Work**
Isolation		Thick oxide		Polyimide	Polyimide
Isolation transformer		3.7-µm Cu		6-µm Au	5-µm Au
BEOL		0.9-µm Al		6-µm Au	5-µm Au
Isolation transformer substrate		BCD SOI		Low conductivity	Low conductivity
Chip no.		2		3	3
Oscillator topology	LDMOS D-class	CMOS CR inductively coupled	CMOS CR hybrid-coupled	HV CMOS D-class	LDMOS D-class
Rectifier topology		Schottky diode full bridge			
P_{OUT} (mW)	780	200	300	225	200
η (%)	28	27	24	25	24.5
V_{DD}/V_{OUT} (V)	5/20	5/8	5/10	5/15	5/20
f_{OSC} (MHz)	165	240	225	160	250
Power density (mW/mm^2)	83	19	36	n.a.	25

From the comparison in Table 4, several considerations arise. Better performance results are achieved with *D*-class power oscillators, enabled by high-BV devices (such as LDMOS of HV MOS), especially when V_{OUT} is higher than 10 V. On the other hand, the widespread adopted topology for the rectifier is the Schottky diode full bridge, as it allows efficient operation in the VHF band. Finally, two-chip implementations achieve higher power densities than the three-chip one at the expense of higher costs due to larger expensive silicon chips. It is worth noting that, despite significant differences in the isolation technologies, similar power efficiency results are achieved. For deeper analysis, the proposed DC-DC converter is compared with the DC-DC converters in [13,18], which shares both similar circuit topologies and technologies for the active circuitries. Specifically, Table 5 reports the simulated power efficiency breakdown among the DC-DC converter building blocks, also including efficiencies of the bonding wires from the oscillator to the transformer, η_{B1}, and from the transformer to the rectifier, η_{B2}. It is quite evident that the advantage of a customized isolation transformer (i.e., 60% efficiency) is frustrated by the need for additional bonding wires between Chips A and T. This is only partially due to

additional bonding wire losses while being mainly related to the degradation of power oscillator efficiency, η_{OSC}, which is 17 percentage points lower than in [13]. Indeed, only a fully integrated approach for the isolation transformer guarantees an effective codesign between the oscillator active core and the transformer itself, which benefits from a very accurate prediction of on-chip interconnection parasitics for the actual optimization of DC-AC power efficiency.

Table 5. Simulated power efficiency breakdown for galvanically isolated DC-DC converters.

	Isolation Transformer Technology	Simulation					Measurement		Unit
		η_{OSC}	η_{B1}	η_{TRAF}	η_{B2}	η_{RECT}	η	η	
[13] [1]	On-chip thick oxide	75.5	90	52.6	-	85.5	30.6	28	[%]
[18]	On-chip thick oxide	73	90	50	-	75	24.6	24	[%]
This work	Standalone polyimide	58	90	60	90	90	25.4	24.5	[%]

[1] Efficiency values are calculated from Tables IV and V in [13].

5. Conclusions

An experimental comparison of galvanically isolated DC-DC converters for high-voltage applications was presented in order to analyze the benefits and drawbacks of the two most adopted isolation approaches in terms of performance, design flexibility, integration level and costs. To this aim, a DC-DC converter was specifically designed and implemented by using a polyimide-based low-cost technology for 5-kV basic isolation. Despite better transfer efficiency of the isolation transformer with respect to a fully integrated approach, the overall efficiency performance is affected by additional losses, the codesign optimization is quite involved due to off-chip parasitics in the DC-AC conversion and, finally, the power density is lower. On the other hand, a three-chip architecture is more flexible and suitable for a continuous silicon process upgrade (i.e., process scaling) while being able to achieve up to a 10-kV isolation rating, thanks to more than 30-µm thick polyimide layers.

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