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Single miller capacitor frequency compensation techniques: Theoretical comparison and critical review

Alfio Dario Grasso[1] | **Davide Marano**[2] | **Gaetano Palumbo**[1] | **Salvatore Pennisi**[1]

[1]Department of Electrical, Electronics and Computer Engineering (DIEEI), University of Catania, Catania

[2]INAF (National Institute of Astrophysics), Astrophysical Observatory of Catania, Catania, Italy

Correspondence
Alfio Dario Grasso, Dipartimento di Ingegneria Elettrica Elettronica e Informatica (DIEEI), University of Catania, I-95125 Catania, Italy.
Email: agrasso@dieei.unict.it

Abstract

This paper presents a systematic analytical comparison of the single-Miller capacitor frequency compensation techniques suitable for three-stage complementary metal–oxide–semiconductor (CMOS) operational transconductance amplifiers (OTAs). The comparison is carried out with the aid of a figure of merit that expresses a trade-off among gain-bandwidth product, load capacitance, and total transconductance, for equal values of the phase margin. The results found can be used before the transistor-level design step and provide useful guidelines for the optimization of the small-signal performance. Simulations by using a 65-nm standard CMOS technology confirming the effectiveness of the theoretical comparison for 10 different OTA topologies are also provided.

KEYWORDS

CMOS analog integrated circuits, frequency compensation, multistage amplifiers, operational transconductance amplifiers

1 | INTRODUCTION

Despite the topic of three-stage amplifiers is not certainly new,[1–3] it has received persistent and growing attention from the analog designers community. Indeed, continuous technological scaling, specially designed for low-power high-performance digital circuits, leads to a strong reduction in the intrinsic transistor voltage gain. Thus, more than two stages are usually required to achieve adequate gains in nanometer technologies, especially under a low-voltage supply that prevents the use of cascoded topologies, apart from the first stage.

To ensure closed-loop stability of three-stage amplifiers the nested Miller compensation (NMC),[1–6] suitable when the only inverting stage is the output one, or the reversed nested Miller compensation (RNMC),[7–9] suitable when the intermediate gain stage is the only inverting one, have been traditionally exploited. Both techniques adopt two compensation capacitors, which exploit the Miller effect, to split low-frequency poles and to achieve the desired phase margin and transient response. Starting from these basic approaches, several advanced techniques and design strategies have been proposed both for NMC-based[10–15] and for RNMC-based[16–22] solutions, to provide a higher gain-bandwidth product.

As a further advance in three-stage amplifier design, increased interest in single Miller capacitor (SMC) compensation has also recently emerged,[23–36] especially when large capacitive loads have to be driven.[32–34]

Indeed, assuming equal static power consumption, these topologies seem to offer improved bandwidth performance and better large-signal performance with respect to the topologies based on NMC or RNMC.[34–38]

In this paper, after a thorough review of the SMC topologies presented in the literature, an analytical comparison among the most interesting and performing solutions is presented. Starting with a preliminary definition of the design procedure, which adopts the phase margin as the main design parameter, the comparison is carried out with the aid of a figure of merit (FOM) which was originally proposed by Pugliese et al.[39] and efficiently adopted to compare NMC and RNMC in three-stage amplifiers and MC for two-stage amplifiers.[39–48] The proposed approach allows in-depth analysis to be achieved and provides useful design guidelines for the optimization of the small-signal performance while ensuring inherently good time-domain performance.

The paper is organized as follows. Section 2 introduces the general notation, the main assumptions, and parameters definition. The analytical FOM is discussed in Section 3. Then, 10 different single-Miller compensation topologies of three-stage OTAs are analyzed in Sections 4 and design equations, which allow setting the compensation network for a given value of the phase margin, are highlighted. The analytical FOMs of the chosen topologies are then discussed in Section 5, along with a theoretical and graphical-based comparison. Section 6 summarizes the simulation results of the transistor-level implementations. Finally, concluding remarks are given in Section 7.

2 | PRELIMINARY ASSUMPTIONS AND NOTATION

2.1 | General notation

Figure 1 shows a block diagram of a general three-stage amplifier adopting the SMC frequency compensation. V_1 and V_2 denote the voltages at the internal high-impedance nodes and, for all the compensation approaches treated in this paper, g_{mi}, R_{oi}, and C_{oi} are the transconductance, output resistance, and output (parasitic) capacitance of the ith amplifier gain stage, respectively. Parameters g_{m3}, R_{o3}, and C_L are the output stage transconductance, the output resistance, and the loading capacitance, respectively. The Miller compensation capacitor is denoted as C_C. Hence, being the DC voltage gain given by

$$A_0 = \prod_{i=1}^{3} A_i = g_{m1}R_{o1}g_{m2}R_{o2}g_{m3}R_{o3} \tag{1}$$

where A_i is the voltage gain of the ith stage, $g_{mi}R_{oi}$. Besides, assuming a dominant-pole behavior, where the dominant pole angular frequency, p_1, is

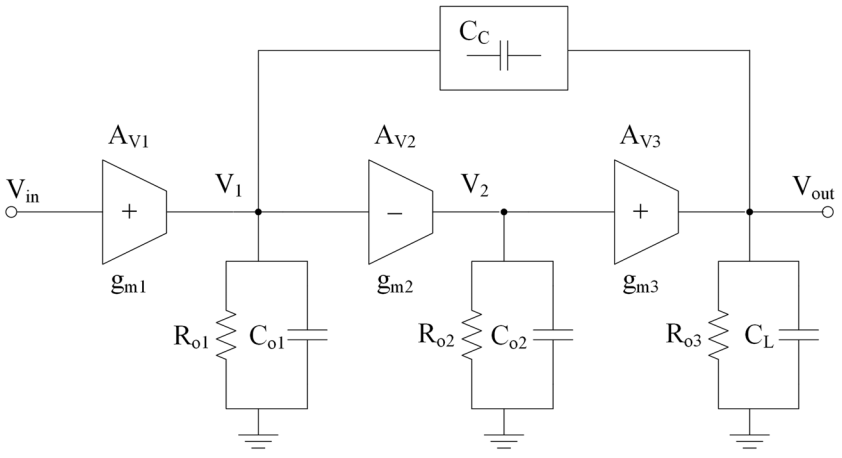

FIGURE 1 Simplified block diagram of a three-stage amplifier with SMC

$$p_1 = \frac{1}{R_{o1}A_2A_3C_C} \tag{2}$$

the open-loop amplifier gain-bandwidth product results to be

$$\omega_{GBW} = \frac{g_{m1}}{C_C} \tag{3}$$

2.2 | Assumptions

In order to simplify the relationships of the amplifier transfer functions without losing accuracy, three general assumptions are adopted in the followings:

1. the DC gain of each amplifier stage is much greater than the unity (i.e., $A_{oi} = g_{mi}R_{oi} >> 1$);
2. the capacitive load, as well as the compensation capacitors, are much greater than the stage output parasitic capacitances (i.e., C_C, $C_L >> C_{oi}$);
3. parasitic inter-stage coupling capacitances are negligible.

2.3 | Parameter definitions

Usually, in general-purpose feedback amplifiers, the output stage most significantly affects the performance of the whole amplifier in terms of power dissipation, linearity, and closed-loop bandwidth.[49] Hence, following the method proposed and exploited in other studies,[40–42] we consider the normalized stage transconductances, G_{Nmx}, with respect to the last stage transconductance, g_{m3}

$$G_{Nmx} = \frac{g_{mx}}{g_{m3}} \tag{4}$$

where x is 1 or 2 for the first and second stage, respectively. Additionally, x could also refer to auxiliary transconductances such as that of current or voltage followers, or to feed-forward stages adopted in the compensation branches.

Finally, it is also useful to introduce the parameters

$$c_{Noi} = \frac{C_{oi}}{C_L} \tag{5}$$

which represent the normalized-to-C_L ith output parasitic capacitance.

3 | FIGURES OF MERIT

3.1 | Traditional numerical FOMs

Traditionally, to compare small- and large-signal performance of three-stage amplifiers, two couple of numerical FOMs were introduced and adopted.[6,18]

$$FOM_S = \frac{\omega_{GBW}}{V_{DD}I_{DD}}C_L \tag{6}$$

$$FOM_L = \frac{SR}{V_{DD} I_{DD}} C_L \tag{7}$$

$$IFOM_S = \frac{\omega_{GBW}}{I_{DD}} C_L \tag{8}$$

$$IFOM_L = \frac{SR}{I_{DD}} C_L \tag{9}$$

where SR is the average amplifier slew rate, V_{DD} is the supply voltage and I_{DD} is the overall amplifier biasing current. FOMs 6–9 allow to assess the performance with respect to power consumption and current consumption for a defined load condition.

While useful and frequently adopted, these *FOM*s depend upon the amplifier topology and fabrication technology, and thus, they do not allow to carry out an effective coherent comparison among the several compensation networks available.

3.2 | Analytical FOM

To perform a more general comparison irrespective of the adopted technology and specific design constraints, the authors introduced a *FOM* which can be evaluated from the amplifier open-loop transfer function, which is given by[40–42]

$$FOM = \frac{\omega_{GBW}}{g_{m1} + g_{m2} + g_{m3} + g_{mCOM}} C_L = \frac{G_{Nm1}}{1 + G_{Nm1} + G_{Nm2} + G_{NmCOM}} \frac{C_L}{C_C} \tag{6}$$

where g_{mCOM} and G_{NmCOM} represent the sum of any extra compensation network transconductance and its normalized value, respectively. Several advantages are obtained considering this *FOM* [40–42]:

a. the total amplifier transconductance is a key design parameter that is heavily related to significant design specifications such as power consumption and silicon area occupation (in CMOS amplifiers with MOSFETs in saturation the small-signal transconductance represents the trade-off between transistor area and biasing current);
b. for a CMOS transistor operating in saturation region (i.e., strong inversion) g_m is given by $2I_{BIAS}/V_{DSsat}$, and hence, assuming a certain constant V_{DSsat}, the transconductance represents an assessment of power dissipation. This property also holds for a CMOS transistor operating in its subthreshold region (i.e., in weak inversion), since g_m is equal to $2I_{BIAS}/V_t$, where V_t is the thermal voltage kT/q;
c. the *FOM* can be analytically evaluated regardless of the amplifier topology, fabrication technology, and other design choices, thus allowing accurate and coherent performance comparisons among different compensation topologies;
d. for each compensation network, the *FOM* function provides information on the compensation topology efficiency versus the transconductance values distribution among the amplifier stages;
e. the *FOM* gives the ratio between the gain-bandwidth product of the compensated three-stage amplifier with respect to a single-stage amplifier under both the same load conditions and total small-signal transconductance;
f. the *FOM* is also strongly related to the large-signal amplifier behavior.

With reference to point (e), let us define ω_{GBW1} as the gain-bandwidth product of a single-stage amplifier having load C_L and total small-signal transconductance g_{mTOT} both equal to those of a three-stage amplifier. Remembering that $\omega_{GBW1} = C_L/g_{mTOT}$, we get from 6 that $FOM = \omega_{GBW}/\omega_{GBW1}$.

Regarding point (f), despite the *FOM* in Grasso et al.[40] was introduced only to account for the small-signal behavior, a more in-depth analysis shows that it provides information also on the large-signal performance.[41] Indeed, in multistage amplifiers the overall slew rate is limited by the slowest stage, which, assuming a Class AB output stage, is typically due to the Class A input stage driving the largest compensation capacitor, C_C; hence, the slew rate, SR, can be assumed to be expressed by

$$SR = \frac{I_1}{C_C} \tag{7}$$

where I_1 is the first stage bias current. Let us consider now a pure single-stage amplifier with bias current and load capacitance equal to those of a three-stage amplifier, I_{TOT} and C_L. Under the approximation that the saturation voltage, V_{DSsat}, is equal for all transistors (working in saturation region), the ratio between the overall slew rate of the three-stage amplifier in 7 and the slew rate of the considered single-stage amplifiers expressed by

$$\frac{SR}{SR_1} = \frac{I_1}{I_{TOT}} \frac{C_L}{C_C} \cong \frac{g_{m1}}{g_{mTOT}} \frac{C_L}{C_C} \tag{8}$$

which is exactly the *FOM* given in 6.

4 | SINGLE MILLER TOPOLOGIES

This section gives a short but in-depth analysis of the most significant SMC techniques.[23–36] The first SMC topology named damping-factor-control frequency compensation (DFCFC) was presented in Leung et al.[23] It exploits an active damping-factor-control (DFC) block, which controls the damping factor caused by the non-dominant complex poles and a feed-forward stage.

After 5 years, two novel topologies were presented,[24] the first is SMC with only a feed-forward branch from the second stage input to the output, and the second, named SMFFC, with two feed-forward stages (the latter was also adopted in Zhang et al.[31]). Since then, several SMC topologies were progressively introduced.[25–37] In particular, although not experimentally tested, SMC with nulling resistance to compensate the right half plane (RHP) zero was presented,[25] followed by a topology with a current buffer in series with the Miller capacitor,[26] and almost the same topology was again treated (unless for a feed-forward branch which does not give significant impact).[29] A topology which adds left half plane (LHP) zeros in the inner nodes thanks to a passive resistance-capacitance series was developed in Peng et al.[27] The topology was further extended in Di Cataldo et al.,[37] by including a resistance in series to the Miller capacitance. Finally, the other solutions are again with a current buffer or an active element in series with the Miller capacitance.[28,30,32][36]

In the following, we will consider the block schemes of the topologies as reported in the original papers. However, as it will be shown, some feed-forward paths do not significantly affect the transfer function and hence can be neglected from the small-signal point of view.

4.1 | SMC and SMFFC topologies

A high-level block scheme of both SMC and SMFFC topologies is shown in Figure 2.[24]

The open-loop transfer function of the amplifier adopting the pure SMC in Figure 2 (obtained for $g_{mf1} = 0$) is

$$A(s) = \frac{A_0}{\left(1+\frac{s}{p_1}\right)} \cdot \frac{1+\left(\frac{g_{mf2}A_2C_{o2}-g_{m2}C_C}{g_{m2}g_{m3}A_2}\right)s-\frac{C_{o2}C_C}{g_{m2}g_{m3}}s^2}{1+\left(\frac{C_L}{g_{m3}A_2}+\frac{g_{mf2}C_{o2}}{g_{m2}g_{m3}}\right)s+\frac{C_{o2}C_L}{g_{m2}g_{m3}}s^2} \approx \frac{A_0}{\left(1+\frac{s}{p_1}\right)} \cdot \frac{1+\left(\frac{g_{mf2}A_2C_{o2}-g_{m2}C_C}{g_{m2}g_{m3}A_2}\right)s-\frac{C_{o2}C_C}{g_{m2}g_{m3}}s^2}{1+\frac{C_L}{g_{m3}A_2}s+\frac{C_{o2}C_L}{g_{m2}g_{m3}}s^2} \tag{9}$$

According to the results summarized in Appendix A and adopting the normalization introduced in the previous section, the phase margin, ϕ, can be evaluated using the equation

$$\tan(\phi - \phi_B) = \frac{A_2\left(G_{Nm2}C_C^2 - G_{Nm1}^2C_{o2}C_L\right)}{G_{Nm1}G_{Nm2}C_CC_L} \tag{10}$$

where f_B is the contribution of zeros on phase margin. Setting $G_{Nmc} = g_{mf2}/g_{m3}$ yields

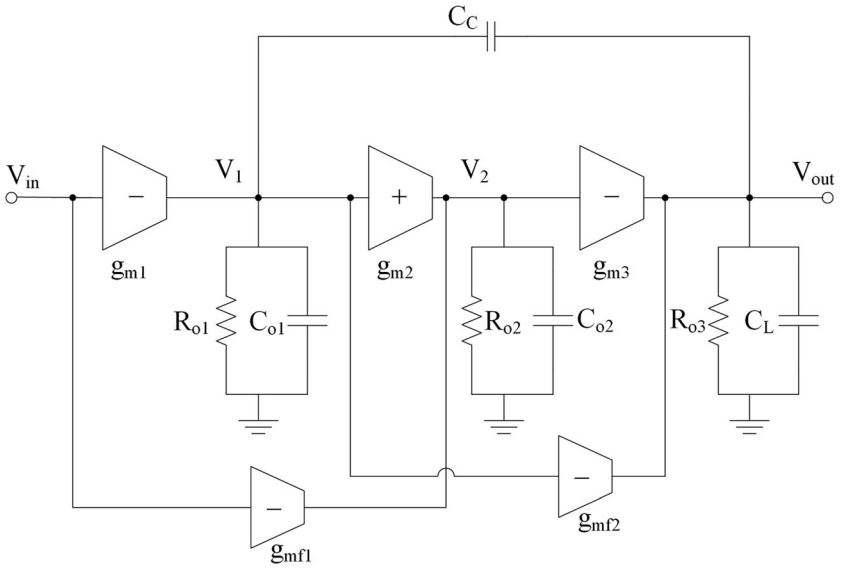

FIGURE 2 Simplified block diagram of: SMC topology ($gmf_1 = 0$) and SMFFC topology

$$\begin{aligned}\phi_B &= \tan^{-1}\left[\frac{G_{Nm1}\left(G_{Nmc}A_2C_{o2} - G_{Nm2}C_C\right)}{A_2\left(G_{Nm2}C_C + G_{Nm1}^2C_{o2}\right)}\right] \\ &\approx \tan^{-1}\left(\frac{G_{Nm1}G_{Nmc}C_{o2}}{G_{Nm2}C_C}\right)\end{aligned} \tag{11}$$

It is worth noting that the above results are more accurate than the original ones in,[24] where the zero is neglected. From 10, we can derive the Miller capacitance, C_C, whose relationship is in Table 1, and substituting it into 11, we can find the value of ϕ_B in Table 2.

In the SMFFC topology, a feed-forward stage provides a LHP zero which compensates for the first non-dominant pole[24]* and also makes negligible the effect of the other feed-forward stage. The transfer function of the SMFFC in Figure 2 is given by

$$A(s) = \frac{A_0}{\left(1+\frac{s}{p_1}\right)}\cdot\frac{1+\left[\frac{g_{mf2}A_2C_{o2}-g_{m2}C_C}{g_{m1}g_{m2}g_{m3}A_2}+\frac{g_{mf1}C_C}{g_{m1}g_{m2}}\right]s-\frac{C_{o2}C_C}{g_{m2}g_{m3}}s^2}{1+\left(\frac{C_L}{g_{m3}A_2}+\frac{g_{mf2}C_{o2}}{g_{m2}g_{m3}}\right)s+\frac{C_{o2}C_L}{g_{m2}g_{m3}}s^2} \approx \frac{A_0}{\left(1+\frac{s}{p_1}\right)}\cdot\frac{1+\frac{g_{mf1}C_C}{g_{m1}g_{m2}}s-\frac{C_{o2}C_C}{g_{m2}g_{m3}}s^2}{1+\frac{C_L}{g_{m3}A_2}s+\frac{C_{o2}C_L}{g_{m2}g_{m3}}s^2} \tag{12}$$

Then, from Appendix A and normalizing the stage transconductances, we get

$$\tan(\phi-\phi_B) = \frac{A_2\left(G_{Nm2}C_C^2 - G_{Nm1}^2C_{o2}C_L\right)}{G_{Nm1}G_{Nm2}C_CC_L} \tag{13}$$

where the value of ϕ_B is reported in Table 2. Evaluating C_C from 13, we get again the same relationship found for the SMC and SMFFC (Table 2).

The solution[31] is very similar to the two above treated topologies; it is adopted in an amplifier topology named current-reuse single Miller feed-forward compensation (CRSMFC). Compared to the SMFFC, it presents an additional voltage gain, K, along with the first feed-forward path; thus, it can be simply analyzed using the same relationship of the SMFFC but substituting the transconductance g_{mf1} with $g'_{mf1} = Kg_{mf1}$.

TABLE 1 Normalized miller compensation capacitance

SMC topology	C_C/C_L	
SMC, SMFFC	$\frac{G_{Nm1}\tan(\phi-\phi_B)}{2A_2}\left[1+\sqrt{1+\frac{4A_2^2}{G_{Nm2}\tan^2(\phi-\phi_B)}c_{No2}}\right]$	
IAC, IIAC	$\frac{(A_2+G_{Nm2}K_{Ra})G_{Nm1}\tan(\phi-\phi_B)}{2A_2K_{Ra}G_{Nm2}}\left[1+\sqrt{1+\left(\frac{A_2K_{Ra}}{A_2+G_{Nm2}K_{Ra}}\right)^2\frac{4G_{Nm2}}{\tan^2(\phi-\phi_B)}c_{No2}}\right]$	
DACFC	Case 1, phase margin given by the third non-dominant pole	$\frac{G_{Nm1}c_{no1}\tan(\phi-\phi_B)}{G_{Nmc}}$
	Case 2, neglecting the highest pole and zero	$\frac{G_{Nm1}G_{Nmc}\tan(\phi-\phi_B)c_{No2}}{2G_{Nm2}c_{No1}}\left[\sqrt{1+\frac{4G_{Nm2}[G_{Nm1}+3G_{Nmc}\tan(\phi-\phi_B)]c_{No1}^2}{G_{Nm1}G_{Nmc}^2\tan^2(\phi-\phi_B)c_{No2}}}-1\right]$
CFCC	Case 1, phase margin given by the third non-dominant pole	$G_{Nm1}K_{Ro2}c_{No2}\tan(\phi-\phi_B)$
	Case 2, neglecting the highest pole and zero	$\frac{G_{Nm1}\tan(\phi-\phi_B)}{2A_2}\frac{c_{No1}}{c_{No2}}\left(1+\sqrt{1+\frac{4A_2c_{No2}^2}{G_{Nmc}c_{No1}\tan^2(\phi-\phi_B)}}\right)$
CBMCPC, CLIA	$G_{Nm1}\sqrt{\frac{\left(1+\frac{G_{Nmc}}{G_{Nm1}}\tan(\phi-\phi_B)\right)c_{No2}}{G_{Nm2}G_{Nmc}K_{Ra}}}$ substitute c_{o2} with c_{o1} for the CLIA	
CBMPPC	$\sqrt{\frac{G_{Nm1}\tan(\phi-\phi_B)c_{No1}c_{No2}}{G_{Nm2}K_{Ra}c_{Na}}}$	
ASMIHF	Case 1, phase margin given by the fourth pole and third zero	$\frac{G_{Nm1}A_2c_{No2}\tan(\phi-\phi_B)}{G_{Nm2}}$
	Case 2, neglecting the highest pole and zeros	$\sqrt{\frac{G_{Nm1}(G_{Nm1}+G_{Nmc}\tan(\phi-\phi_B))c_{No1}}{G_{Nmc1}A_2}}$

TABLE 2 Analytical expression of parameter Φ_b

Topology	Φ_B	
SMC	$\tan^{-1}\left[\frac{G_{Nmf2}\tan\phi}{2A_2}\left(\sqrt{1+\frac{4A_2^2}{G_{Nm2}\tan^2\phi}c_{No2}}-1\right)\right]$	
SMFFC	$\tan^{-1}\frac{G_{Nmf1}C_C}{G_{Nm2}C_C+G_{Nm1}^2C_{o2}}\approx\tan^{-1}\frac{G_{Nmf1}}{G_{Nm2}}$	
IAC	0	
IIAC	$\tan^{-1}(G_{Nm1}K_{Rc})$ with $K_{Rc}=g_{m3}R_C$	
DACFC, CFCC	Case 1, phase margin given by the third non-dominant pole	0
	Case 2, neglecting the highest pole and zero	$\tan^{-1}\left(\frac{G_{Nm1}}{2G_{Nmc}}\right)$
CBMCPC, CBMPPC	$\tan^{-1}\left(\frac{G_{Nm1}}{G_{Nmc}}\right)$	
CLIA	$\tan^{-1}\left(\frac{G_{Nm1}}{2G_{Nmc}}\right)$	
ASMIHF	Case 1, Phase margin given by the fourth pole and third zero	$\tan^{-1}\left(\frac{c_{No1}G_{Nmf2}G_{Nmc}}{G_{Nmf1}}\sqrt{\frac{2}{3}\frac{A_2}{G_{Nm1}c_{No1}}}\right)$
	Case 2, Neglecting the highest pole and zeros	$\tan^{-1}\left(\frac{G_{Nm1}}{G_{Nmc1}}\right)$

4.2 | IAC and IIAC topologies

A topology referred to as impedance adapting compensation (IAC), with a resistance-capacitance series at an inner node was presented in Peng et al.[27] It creates a LHP zero to compensate the effect of high-frequency poles. Then, a more general topology, named IIAC (improved IAC), with an additional resistance in series with the Miller capacitance was also presented and analyzed in Di Cataldo et al.[37]

The block scheme of the two topologies is shown in Figure 3. The IAC transfer function is expressed by

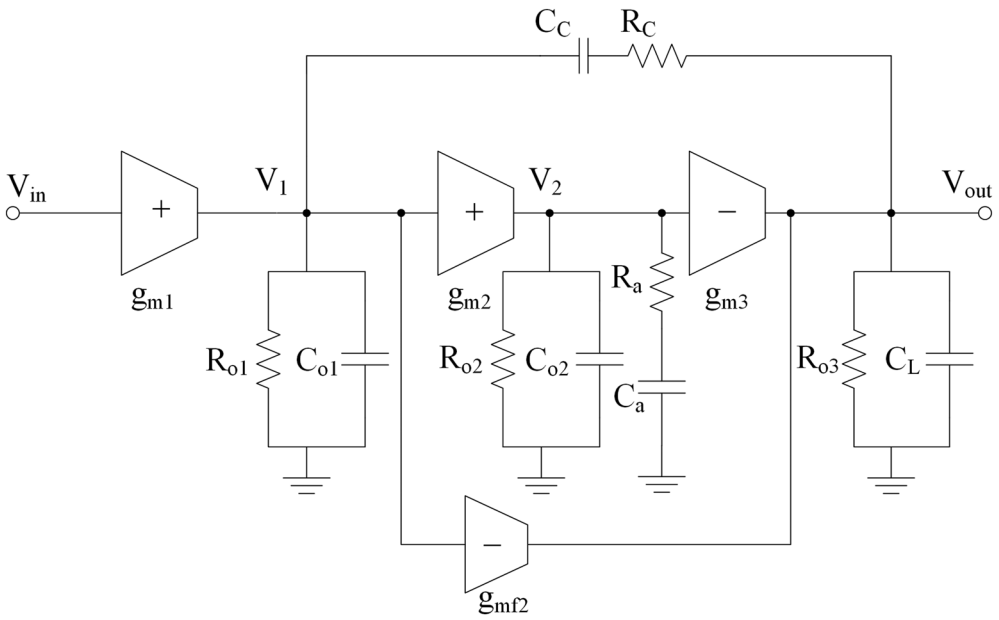

FIGURE 3 Simplified block diagram of IIAC topology. The IAC topology is obtained by setting $R_C = 0$

$$A(s) \approx \frac{A_0}{\left(1+\frac{s}{p_1}\right)} \cdot \frac{1+R_C C_C s}{1+\frac{C_L(A_2+g_{m2}R_a)}{g_{m2}g_{m3}A_2R_a}s+\frac{C_{o2}C_L}{g_{m2}g_{m3}}s^2} \tag{14}$$

Then, from Appendix A and normalizing the stage transconductances, we get

$$\tan(\phi-\phi_B) = \frac{A_2\left(G_{Nm2}C_C^2 - G_{Nm1}^2 C_{o2}C_L\right)}{G_{Nm1}G_{Nm2}C_C C_L} \tag{15}$$

where the value of ϕ_B is reported in Table 2.

By inspection of the frequency-dependent factor of 13, it is independent of g_{m1}, g_{mf2}, and C_a; hence, the feed-forward transconductance g_{mf2} is useless to achieve frequency compensation (a more accurate relationship can be found in Di Cataldo et al.,[37] but in any case, it is still independent of g_{m1}).

Applying the results in Appendix A and normalizing, we get

$$\tan(\phi-\phi_B) = \left(\frac{K_{Ra}A_2}{G_{Nm2}k_{Ra}+A_2}\right)\frac{G_{Nm2}C_C^2 - G_{Nm1}^2 C_{o2}C_L}{G_{Nm1}C_C C_L} \tag{16}$$

where $K_{Ra} = g_{m3}R_a$. Parameter ϕ_B is equal to 0 for IAC, while it has a finite value for IIAC (see Table 2). As given in Table 2, the same Miller capacitance relationship is obtained for both topologies.

4.3 | DACFC topology

The topology named dual-active-capacitive-feedback compensation (DACFC),[28] whose block scheme is depicted in Figure 4, is the first solution that adopts current buffers in the Miller compensation path (modeled in Figure 4 with g_{mc} and g_{mc2}).

The DACFC transfer function is given by

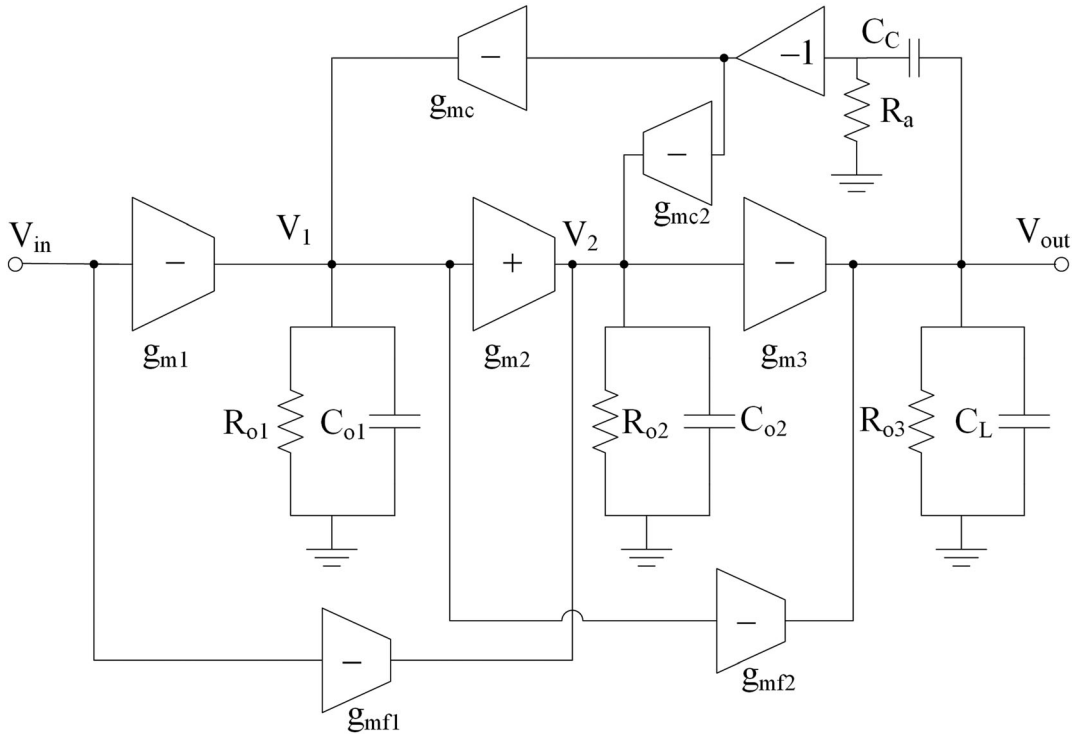

FIGURE 4 Simplified DACFC block diagram

$$A(s) \approx \frac{A_0}{\left(1+\frac{s}{p_1}\right)} \cdot \frac{1+s\frac{C_C}{2g_{mc}}}{1+\frac{g_{mc}C_{o2}C_L(3C_{o1}-C_C)}{g_{m2}g_{m3}C_{o1}C_C}s+\frac{C_{o2}C_L}{g_{m2}g_{m3}}s^2} \cdot \frac{1+s\frac{g_{mf1}C_{o1}}{g_{m1}g_{m2}}}{1+s\frac{C_{o1}}{g_{mc}}} \tag{17}$$

where, according to Guo and Lee,[28] relations $g_{mc2} = g_{m2}$, $R_a = 1/g_{mc}$, and $R_aC_C \approx 2R_2C_{o2}$ have been assumed. Note that the transfer function is independent of g_{mf2}. Moreover, the dual-active capacitive feedback not only avoids the RHP zero, but also produces two beneficial LHP zeros.

Following the design strategy suggested in Guo and Lee,[28] these two LHP zeros can be exploited to compensate the phase shift due to the complex and conjugate non-dominant poles. Thus, the phase margin is only due to the third non-dominant pole, given by g_{mc}/C_{o2}, yielding

$$\tan(\phi - \phi_B) = \frac{G_{Nmc}C_C}{G_{Nm1}C_{o1}} \tag{18}$$

where $\phi_B = 0$ (Table 2). Again, from 18, the Miller compensation capacitor reported in Table 1 is found.

On the other hand, a simpler design strategy can be followed by neglecting the highest pole and zero in 17. Then, from this simplified transfer function, which also becomes independent from g_{mf1}, we get

$$\tan(\phi - \phi_B) = \frac{C_{o1}\left(G_{Nm2}C_C^2 - G_{Nm1}^2C_{o2}C_L\right)}{G_{Nm1}G_{Nmc}C_{o2}C_L(3C_{o1}-C_C)} \tag{19}$$

where ϕ_B in Table 2 has to be used, and the resulting equation is reported in Table 1.

4.4 | CFCC topology

The cross feed-forward cascode compensation (CFCC) topology is like the DACFC one, but is simpler, having only a current buffer in series with the Miller capacitance (Figure 5).[29] Unless for the feed-forward transconductance, g_{mf2}, which as shown in 20, does not impact the compensation, it is equal to the topology previously presented in Guo and Lee.[26]

The CFCC transfer function is

$$A(s)=\frac{A_0}{\left(1+\frac{s}{p_1}\right)}\cdot\frac{1+s\frac{C_C}{2g_{mc}}}{1+\frac{C_{o1}C_L}{g_{m3}A_2C_{o2}}s+\frac{C_{o1}C_L}{g_{m3}g_{mc}A_2}s^2}\cdot\frac{\left(1+s\frac{g_{mf1}C_{o1}}{g_{m1}g_{m2}}\right)\left(1-s\frac{g_{m1}C_{o2}}{g_{mf1}g_{m3}}\right)}{1+sR_{o2}C_{o2}} \tag{20}$$

From the design strategy presented in Chong and Chan,[29] where it is assumed that the RHP zero can be neglected, by using the two LHP zeros to compensate the phase shift caused by the complex and conjugate non-dominant poles, the phase margin is given by the third non-dominant pole only, $1/R_{o2}C_{o2}$. We get

$$\tan(\phi-\phi_B)=\frac{1}{G_{Nm1}K_{Ro2}}\frac{C_C}{C_{o2}} \tag{21}$$

where $\phi_B=0$ (Table 2) and $K_{Ro2}=g_{m3}R_{o2}$. The Miller compensation capacitor is given in Table 1.

Again, like done for the DACFC topology, we can neglect the highest pole and zero and simplify 20 into

$$A(s)\approx\frac{A_0}{\left(1+\frac{s}{p_1}\right)}\cdot\frac{1+s\frac{C_C}{2g_{mc}}}{1+\frac{C_{o1}C_L}{g_{m3}A_2C_{o2}}s+\frac{C_{o1}C_L}{g_{m3}g_{mc}A_2}s^2} \tag{22}$$

which is now also independent of g_{mf1}. By applying A4 and A5, we get

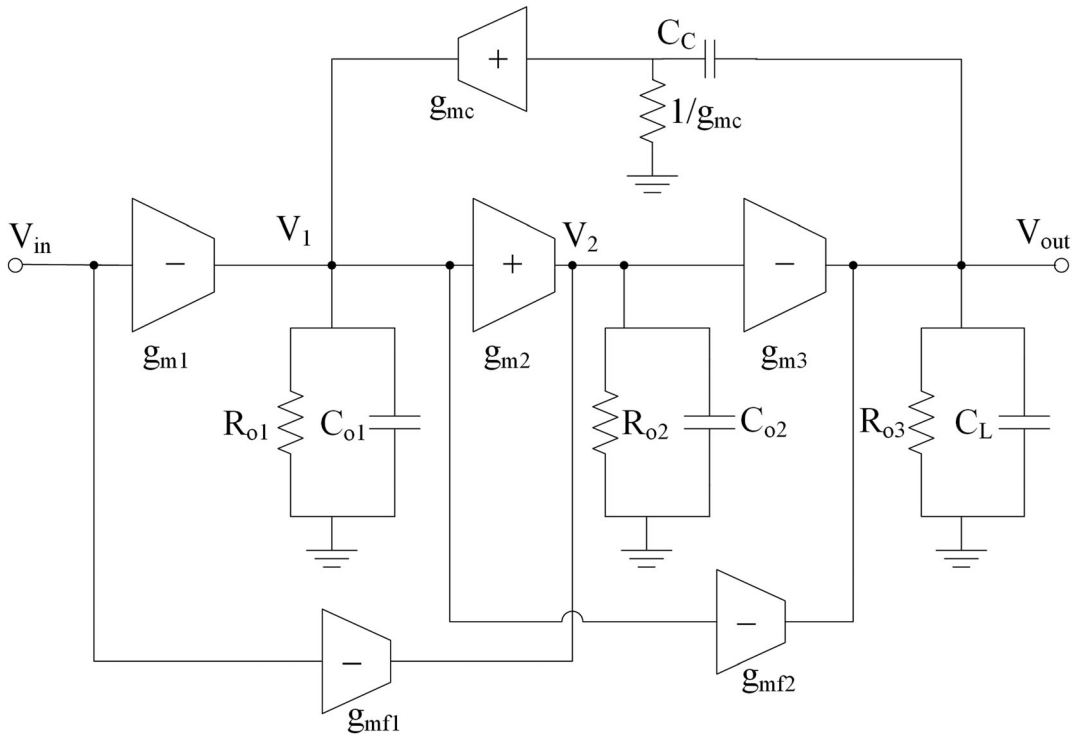

FIGURE 5 Simplified CFCC block diagram

$$\tan(\phi-\phi_B)=\frac{G_{Nmc}A_2C_C^2-G_{Nm1}^2C_{o1}C_L}{G_{Nm1}G_{Nmc}C_{o1}C_CC_L}C_{o2} \tag{23}$$

where ϕ_B is in Table 2 (equal to the DACFC second case) and the Miller compensation capacitor is reported in Table 1.

4.5 | CBMCPC and CLIA topologies

Although presented slightly before,[29] an evolution of the CFCC was proposed in Tan et al.[30] Indeed, as shown in Figure 6A, current buffer Miller compensation and parallel compensation (CBMCPC) is a CFCC with an added parallel compensation with a resistor and a capacitor at the output of the first stage.

The CBMCPC transfer function is given by

$$A(s)=\frac{A_0}{\left(1+\frac{s}{p_1}\right)}\cdot\frac{1+s\frac{C_C}{g_{mc}}}{1+\frac{C_aC_L}{g_{m3}A_2C_C}s+\frac{C_aC_L}{g_{m3}g_{mc}A_2}s^2}\cdot\frac{1+sR_aC_a}{1+sR_2C_{o2}}\cdot\frac{1+s\frac{g_{mf2}C_{o2}}{g_{m2}g_{m3}}}{1+sR_aC_{o1}} \tag{24}$$

Note that the frequency-dependent part of 24 is independent of g_{m1}. Moreover, by setting $R_aC_a=R_{o2}C_{o2}$ as design strategy, relationship 24 simplifies to

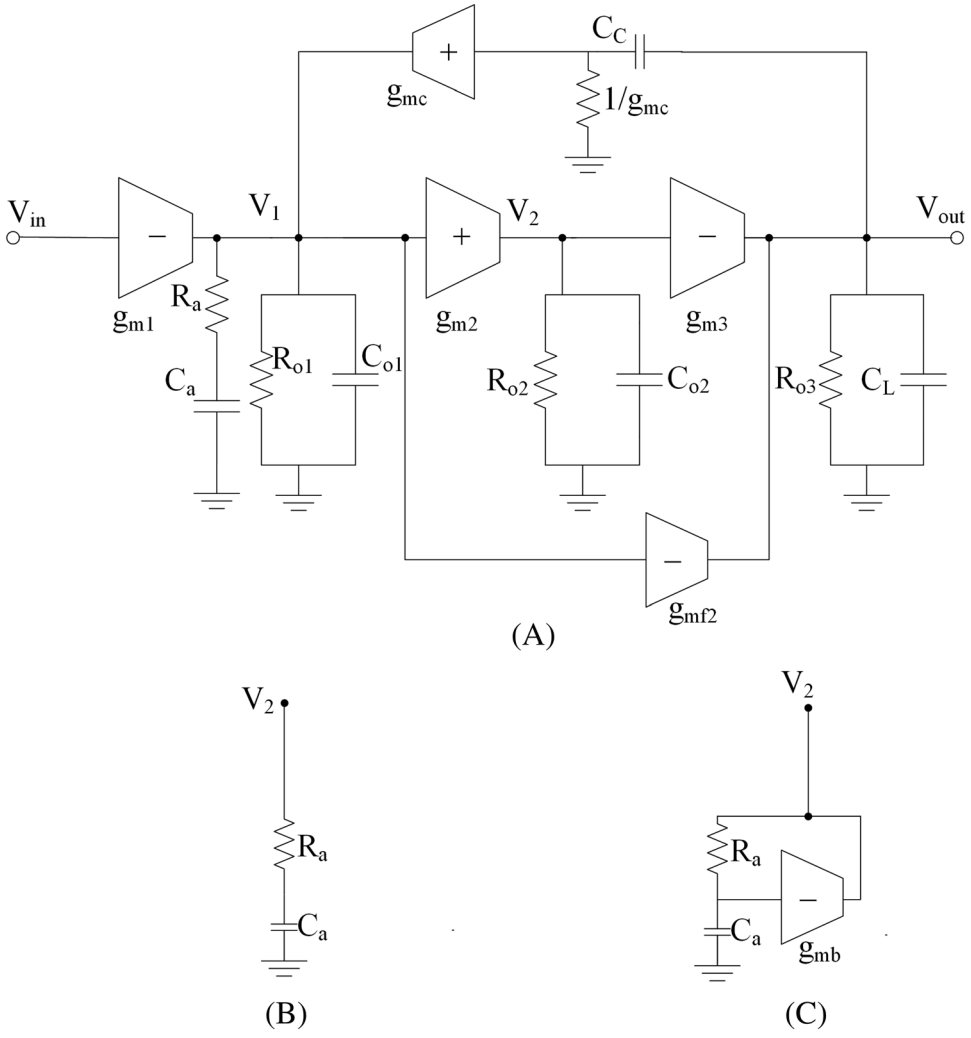

FIGURE 6 (A) Simplified CBMCPC block diagram; (B) additional compensation elements for CLIA and (C) CBMPPC

$$A(s)=\frac{A_0}{\left(1+\frac{s}{p_1}\right)}\cdot\frac{1+s\frac{C_C}{g_{mc}}}{1+\frac{C_{o2}C_L}{g_{m2}g_{m3}R_aC_C}s+\frac{C_{o2}C_L}{g_{m2}g_{m3}g_{mc}R_a}s^2} \tag{25}$$

which yields

$$\tan(\phi-\phi_B)=\frac{G_{Nm2}G_{Nmc}K_{Ra}C_C^2-G_{Nm1}^2C_{o2}C_L}{G_{Nm1}G_{Nmc}C_{o2}C_L} \tag{26}$$

where $K_{Ra}=g_{m3}R_a$ and ϕ_B is given in Table 2. The Miller compensation capacitor derived from 26 is shown in Table 1.

The cascode local impendence attenuation (CLIA) topology presented in Tan and Ki[33] differs from the CBMCBC only for the inner node where the resistance-capacitance series shown in Figure 6B is inserted at the output of the second stage. Its transfer function, unless for a very negligible pole-zero doublet (explicitly expressed in Tan and Ki[33]), is expressed by

$$A(s)=\frac{A_0}{\left(1+\frac{s}{p_1}\right)}\cdot\frac{1+s\frac{C_C}{2g_{mc}}}{1+\frac{C_{o1}C_L}{g_{m2}g_{m3}R_aC_C}s+\frac{C_{o1}C_L}{g_{m2}g_{m3}g_{mc}R_a}s^2} \tag{27}$$

and the frequency-dependent part of 27 is independent of g_{m1} and g_{mf2}. Hence, from the results in Appendix A, tan $(\phi-\phi_B)$ is given by 26 with C_{o1} instead of C_{o2} and ϕ_B in Table 2. Hence, the Miller compensation capacitor reported in Table 1 is equal to that of CBMCBC, but with C_{o1} instead of C_{o2}.

4.6 | CBMPPC topology

The topology in Yan et al.,[32] named current buffer Miller compensation and parasitic-pole cancelation (CBMPPC), like DACFC, CFCC, CBMCPC, and CLIA, has again a current buffer in the Miller compensation path, but it also includes an active block to implement a LHP zero as shown in Figure 6C.

The complete transfer function with five poles and three zeros is reported in Yan et al.[32] According to the design strategy suggested there, $R_aC_a=R_{o2}C_{o2}$ must be set, and like for the CBMCPC, the transfer function can be simplified into

$$A(s)=\frac{A_0}{\left(1+\frac{s}{p_1}\right)}\frac{\left(1+s\frac{C_C}{g_{mc}}\right)}{1+\frac{C_{o1}C_{o2}C_L}{g_{m2}g_{m3}R_aC_aC_C}s+\frac{C_{o1}C_{o2}C_L}{g_{m2}g_{m3}g_{mb}R_aC_C}s^2} \tag{28}$$

where, unlike the simplified derivation in Yan et al.,[32] an LHP zero is also included.

Again, as expected, the transfer function is independent of g_{mf2}. As usual, applying the relationship in Appendix A, we get

$$\tan(\phi-\phi_B)\approx\frac{G_{Nm2}k_{Ra}C_aC_C^2}{G_{Nm1}C_{o1}C_{o2}C_L} \tag{29}$$

with the same ϕ_B value of the CBMCBC (Table 2). The resulting relationship for the Miller compensation capacitor is given in Table 1.

4.7 | ASMIHF topology

The last topology was recently proposed by Marano et al.[35] (Figure 7) and refined in Grasso et al.[36] It is named active single-Miller capacitor compensation with inner half-feed-forward (ASMIHF) and its transfer function is

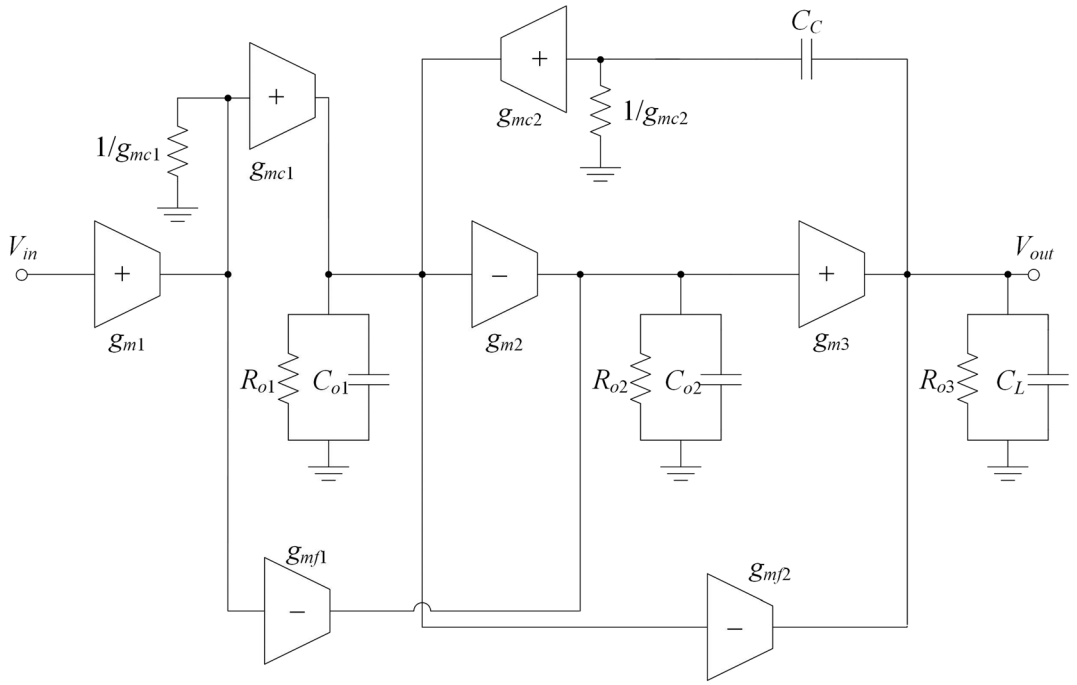

FIGURE 7 Simplified ASMIHF block diagram

$$A(s)=\frac{A_0}{\left(1+\frac{s}{p_1}\right)}\cdot\frac{\left(1+\frac{C_C}{g_{mc}}s\right)\left(1+\frac{g_{mf1}C_{o1}}{2g_{m2}g_{mc}}s\right)}{1+\frac{C_{o1}C_L}{g_{m3}A_2C_C}s+\frac{C_{o1}C_L}{g_{m3}g_{mc1}A_2}s^2}\cdot\frac{\left(1+\frac{g_{mf2}g_{mc}C_{o2}}{g_{mf1}g_{m1}g_{m3}}s\right)}{1+R_{o2}C_{o2}s} \tag{30}$$

After compensating the complex and conjugate non-dominant poles with the first two zeros, according to the design procedure in Marano et al.,[35] the phase margin is only due to the fourth pole, $1/R_{o2}C_{o2}$, and the third zero, $g_{mf1}g_{m1}g_{m3}/g_{mf2}g_{mc}Co_2$. Thus, we get

$$\tan(\phi-\phi_B)=\frac{C_C}{G_{Nm1}K_{Ro2}C_{o2}} \tag{31}$$

with ϕ_B given by

$$\phi_B=\tan^{-1}\left(\frac{G_{Nmf2}G_{Nmc}}{G_{Nmf1}}\frac{C_{o2}}{C_C}\right) \tag{32}$$

and the Miller compensation capacitance reported in Table 1.

Also in this case, a simpler design strategy can be pursued by neglecting the highest pole and the two highest zeros. In this case, the transfer function simplifies into

$$A(s)=\frac{A_0}{\left(1+\frac{s}{p_1}\right)}\cdot\frac{1+\frac{C_C}{g_{mc}}s}{1+\frac{C_{o1}C_L}{g_{m3}A_2C_C}s+\frac{C_{o1}C_L}{g_{m3}g_{mc1}A_2}s^2} \tag{33}$$

and yields

$$\tan(\phi-\phi_B)=\frac{G_{Nmc1}A_2C_C^2-G_{Nm1}^2C_{o1}C_L}{G_{Nm1}G_{Nmc1}C_{o1}C_L} \tag{34}$$

where ϕ_B is reported in Table 2. Thus, the resulting Miller compensation capacitance is given in Table 1.

5 | ANALYTICAL COMPARISON

To compare all the SMC topologies discussed in the previous section, we evaluated for each technique the analytic *FOM* defined in Section 3 and summarized in Table 3, with the parameter g_{mCOM} for each compensation technique reported in Table 4.

Extraction of a ranking among the topology considered is not trivial, because of the complex *FOM* relationships and the numerous parameters involved. However, an in-depth analysis allows several useful considerations to be derived, as detailed below. Moreover, a graphical-based *FOM* comparison can be also carried out. First, we assume that parameter g_{m3} is the maximum stage transconductance in the amplifier. Hence, the normalized parameters G_{Nm1} and G_{Nm2} are always lower or equal than 1, and the same condition can be considered for all the other transconductances in the amplifier, such as g_{mf1}, g_{mf2}, g_{mc}, g_{mc2}, and g_{mb}. Of course, according to Table 4, the normalized transconductance G_{NmCOM} can be higher than 1. Moreover, the normalized parasitic capacitances are assumed to be lower than 1 and, for

TABLE 3 Analytical expressions of the *FOM* in 6

Topology	FOM	
SMC, SMFFC	$\frac{G_{Nm2}\tan(\phi-\phi_B)}{2A_2c_{No2}(1+G_{Nm1}+G_{Nm2}+G_{NmCOM})}\left[\sqrt{1+\frac{4A_2^2c_{No2}}{G_{Nm2}\tan^2(\phi-\phi_B)}}-1\right]$	
IAC, IIAC	$\frac{(G_{Nm2}K_{Ra}+A_2)\tan(\phi-\phi_B)}{(1+G_{Nm1}+G_{Nm2}+G_{NmCOM})2c_{No2}K_{Ra}A_2}\left[\sqrt{1+\left(\frac{K_{Ra}A_2}{G_{Nm2}K_{Ra}+A_2}\right)^2\frac{4G_{Nm2}c_{No2}}{\tan^2(\phi-\phi_B)}}-1\right]$	
DACFC	Case 1, phase margin given by only the third non dominant pole	$\frac{G_{Nmc}}{c_{No1}(1+G_{Nm1}+G_{Nm2}+G_{NmCOM})\tan(\phi-\phi_B)}$
	Case 2, neglecting the highest pole and zero	$\frac{G_{Nm1}G_{Nmc}\tan(\phi-\phi_B)}{2c_{No1}(1+G_{Nm1}+G_{Nm2}+G_{NmCOM})(G_{Nm1}+3G_{Nmc}\tan(\phi-\phi_B))}\cdot\left[\sqrt{1+\frac{4G_{Nm2}c_{No1}^2(G_{Nm1}+3G_{Nmc}\tan(\phi-\phi_B))}{G_{Nm1}G_{Nmc}^2c_{No2}\tan^2(\phi-\phi_B)}}+1\right]$
CFCC	Case 1, phase margin given by only the third non dominant pole	$\frac{1}{(1+G_{Nm1}+G_{Nm2}+G_{NmCOM})c_{No2}K_{Ro2}\tan(\phi-\phi_B)}$
	Case 2, neglecting the highest pole and zero	$\frac{G_{Nmc}\tan(\phi-\phi_B)}{2c_{No2}(1+G_{Nm1}+G_{Nm2}+G_{NmCOM})}\cdot\left(\sqrt{1+\frac{4A_2c_{No2}^2}{G_{Nmc}c_{No1}\tan^2(\phi-\phi_B)}}-1\right)$
CBMCPC, CLIA	$\frac{1}{1+G_{Nm1}+G_{Nm2}+G_{NmCOMP}}\sqrt{\frac{G_{Nm1}G_{Nm2}G_{Nmc}K_{Ra}}{(G_{Nm1}+G_{Nmc}\tan(\phi-\phi_B))c_{No2}}}$ substitute c_{o2} with c_{o1} for the CLIA	
CBMPPC	$\frac{1}{1+G_{Nm1}+G_{Nm2}+G_{NmCOM}}\sqrt{\frac{G_{Nm1}G_{Nm2}K_{Ra}c_{Na}}{c_{No1}c_{No2}\tan(\phi-\phi_B)}}$	
ASMIHF	Case 1, phase margin given by the fourth pole and third zero	$\frac{1}{(1+G_{Nm1}+G_{Nm2}+G_{NmCOM})c_{No2}K_{Ro2}\tan(\phi-\phi_B)}$
	Case 2, neglecting the highest pole and zeros	$\frac{1}{1+G_{Nm1}+G_{Nm2}+G_{NmCOM}}\sqrt{\frac{G_{Nm2}G_{Nmc1}A_2}{(G_{Nm1}+G_{Nmc1}\tan(\phi-\phi_B))c_{No1}}}$

TABLE 4 Analytical expression of parameter g_{mCOM}

Topology	g_{mCOM}
SMC, IAC, IIAC	g_{mf2}
SMFFC	$g_{mf1}+g_{mf2}$
DACFC	$g_{mf1}+g_{mf2}+g_{mc}+g_{mc2}$
CFCC	$g_{mf1}+g_{mf2}+g_{mc}$
CBMCPC, CLIA	$g_{mf2}+g_{mc}$
CBMPPC	$g_{mf2}+g_{mc}+g_{mb}$
ASMIHF	$g_{mf1}+g_{mf2}+g_{mc}+g_{mc1}$

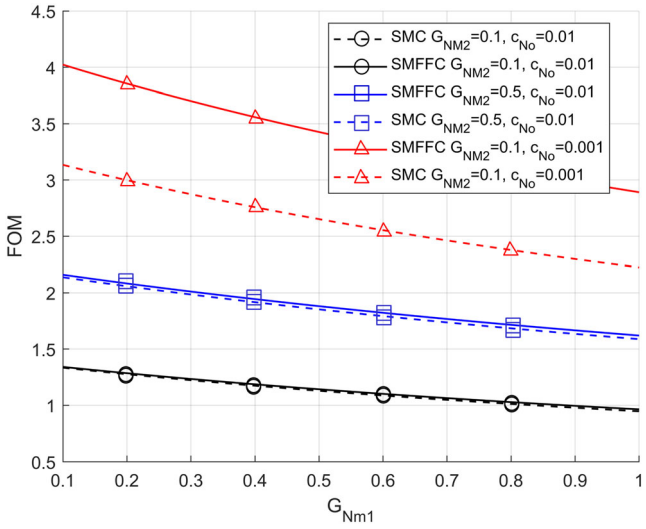

FIGURE 8 *FOM* comparison for SMC and SMFFC topologies [Colour figure can be viewed at wileyonlinelibrary.com]

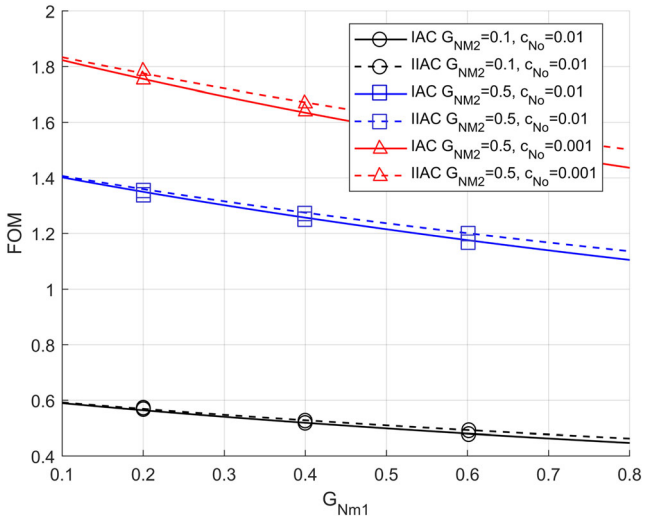

FIGURE 9 *FOM* comparison for IAC and IIAC topologies [Colour figure can be viewed at wileyonlinelibrary.com]

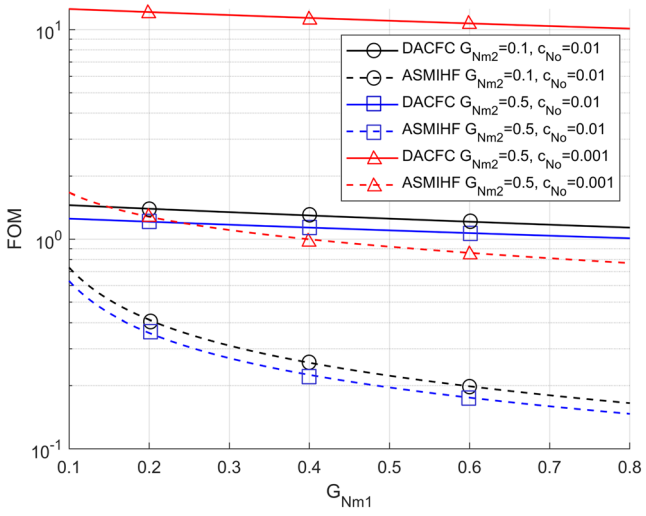

FIGURE 10 *FOM* comparison for DACFC and ASMIHF topologies [Colour figure can be viewed at wileyonlinelibrary.com]

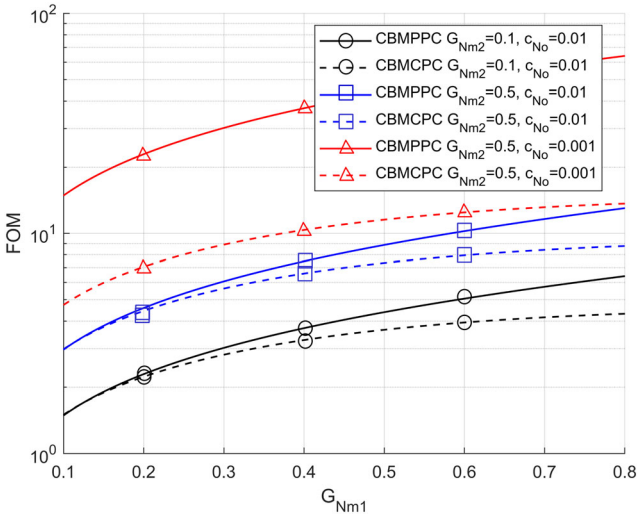

FIGURE 11 *FOM* comparison for CBMCPC and CBMPPC topologies [Colour figure can be viewed at wileyonlinelibrary.com]

the sake of simplicity, they are set equal (i.e., $c_{No} = c_{No1} = c_{No2}$). In the following, we will always consider the phase margin, ϕ, equal to 70°, to optimize the 1% settling time of the amplifier frequency response,[9,50] but the same considerations and conclusion can be obtained for a different phase margin value. We evaluate the *FOM* versus G_{Nm1} for two G_{Nm2} values, namely, 0.1, and 0.5, and for c_{No} equal to 0.01 or 0.001. Finally, we assume as typical values $G_{Nmf1} = 0.1$, $G_{Nmf2} = 1$, $G_{Nmb1} = G_{Nmc2} = G_{Nmc} = 0.1$, $c_{NA} = 0.01$, $K_{RA} = K_{Rc} = 50$, $K_{Ro2} = 200$, and $A_2 = 30$.

Let us start considering the compensation techniques SMC and SMFFC, which differ only for the ϕ_B value. The *FOM* for the SMFFC, which is the most efficient, is reported in Figure 8. This plot shows that the *FOM* always increases by decreasing G_{Nm1} and increasing G_{Nm2} and is always lower than 2 and 4 for c_{No} equal to 0.01 and 0.001, respectively. Moreover, the comparison shows that the increased complexity of SMFFC is justified only for high-capacitive loads (lower values of c_{No}).

Regarding IAC and IIAC, again they differ only for the ϕ_B value. Their *FOM* is plotted in Figure 9, where IIAC always shows a slight better performance than IAC.

Concerning the topologies DACFC, CFCC, and ASMIHF which can have two different design strategies, both previously reported for completeness, we will consider only Case 1, which represents the best strategy. The other case is surely simpler to implement but does not allow the highest gain-bandwidth product to be achieved. Hence, considering the most advantageous case 1 of DACFC, CFCC, and ASMIHF, from Table 3, they have a similar *FOM* relationship, which is inversely proportional to C_o. By comparing the DACFC and CFCC *FOM*s and remembering from Table 4 that for these two topologies ϕ_B is equal, we can write

$$\frac{FOMDACFC}{FOMCFCC} = g_{mc}R_{o2} \tag{35}$$

Hence, the ratio of the *FOM*s of DACFC and CFCC is a voltage gain typically higher than 1. For this reason, the inferior CFCC topology is not considered in the following.

Regarding the comparison between DACFC and ASMIHF, despite the *FOM* ratio seems equal to 33, it is not actually, since ϕ_B values of the two topologies are different, so that a more detailed investigation is necessary.

The *FOM*s of DACFC and ASMIHF are plotted in Figure 10 and show under the same conditions the advantage of DACFC with respect to the ASMHF topology, especially for high capacitive loads. DACFC seems to be particularly advantageous also when compared to the other topologies considered up to now. Interestingly, the *FOM* of DACFC and ASMIHF decrease by increasing G_{Nm2}.

Regarding CBMCPC and CLIA, they have the same pole expression under the assumption that C_{o1} is equal to C_{o2} and differ only slightly for the expression of the zero. Consequently, they have the same *FOM* expression and differ for

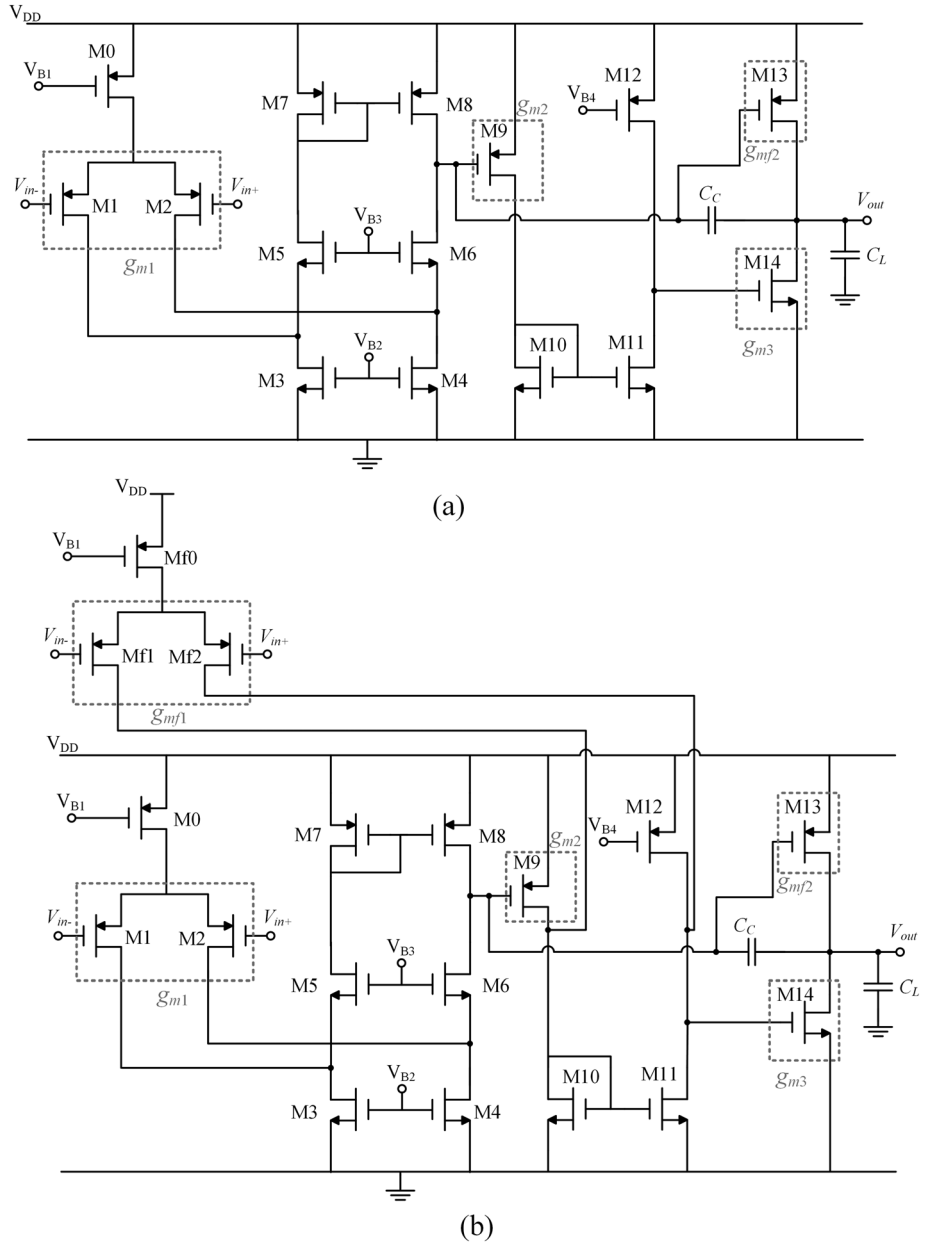

FIGURE 12 Simplified schematic of (a) SMC and (B) SMFFC topology

the value of ϕ_B, as shown in Tables 1 and 2. As a result, the *FOM* values of CBMCPC are slightly higher than those of CLIA.

The last comparison is then carried out for CBMCPC and CBMPPC in Figure 11. From this comparison, it is apparent that CBMPPC shows the highest performance for high capacitive values ($c_{No1} = 0.001$) and *FOM* values higher than 10. However, CBMCPC and CBMPPC exhibit comparable *FOM* values for lower capacitive loads. Moreover, depending on the design conditions, CBMPPC can achieve the best *FOM* as compared to the other topologies considered.

It is worth noting that the above comparison is highly dependent upon the specific set of the various parameters adopted to plot the various graphs. Therefore, it is difficult to establish an absolute ranking among all the considered compensation topologies. Nonetheless, using the proposed approach the designer can assess which of the various solutions is better suited for the given design specifications.

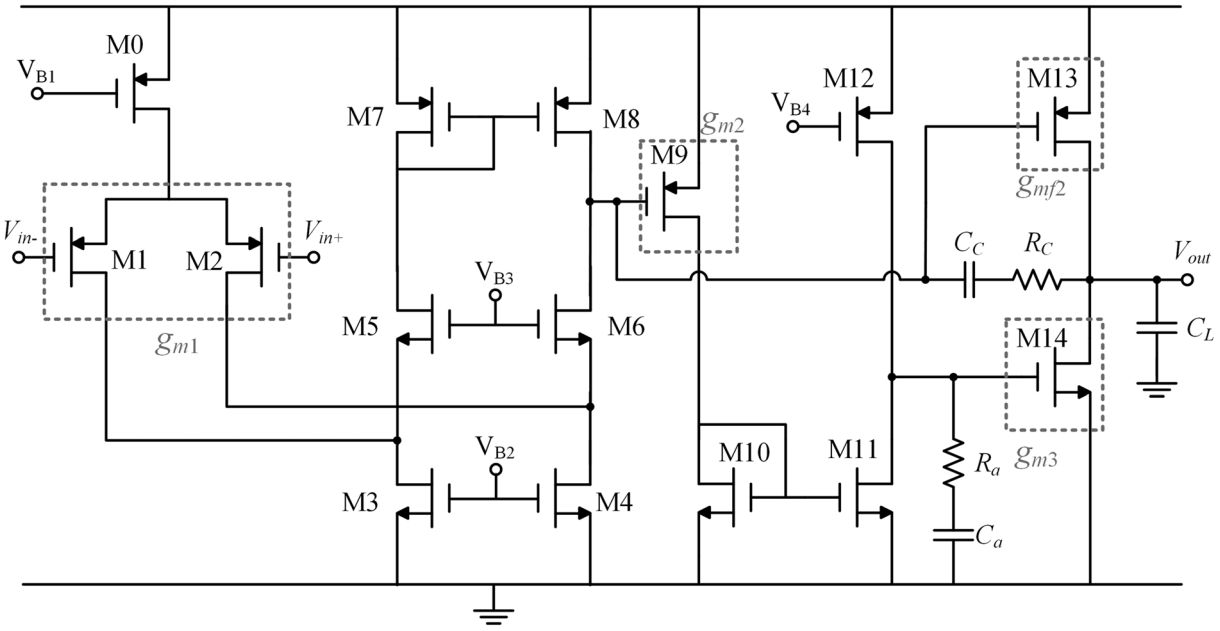

FIGURE 13 Simplified schematic of IIAC topology and IAC topology (for $R_C = 0$)

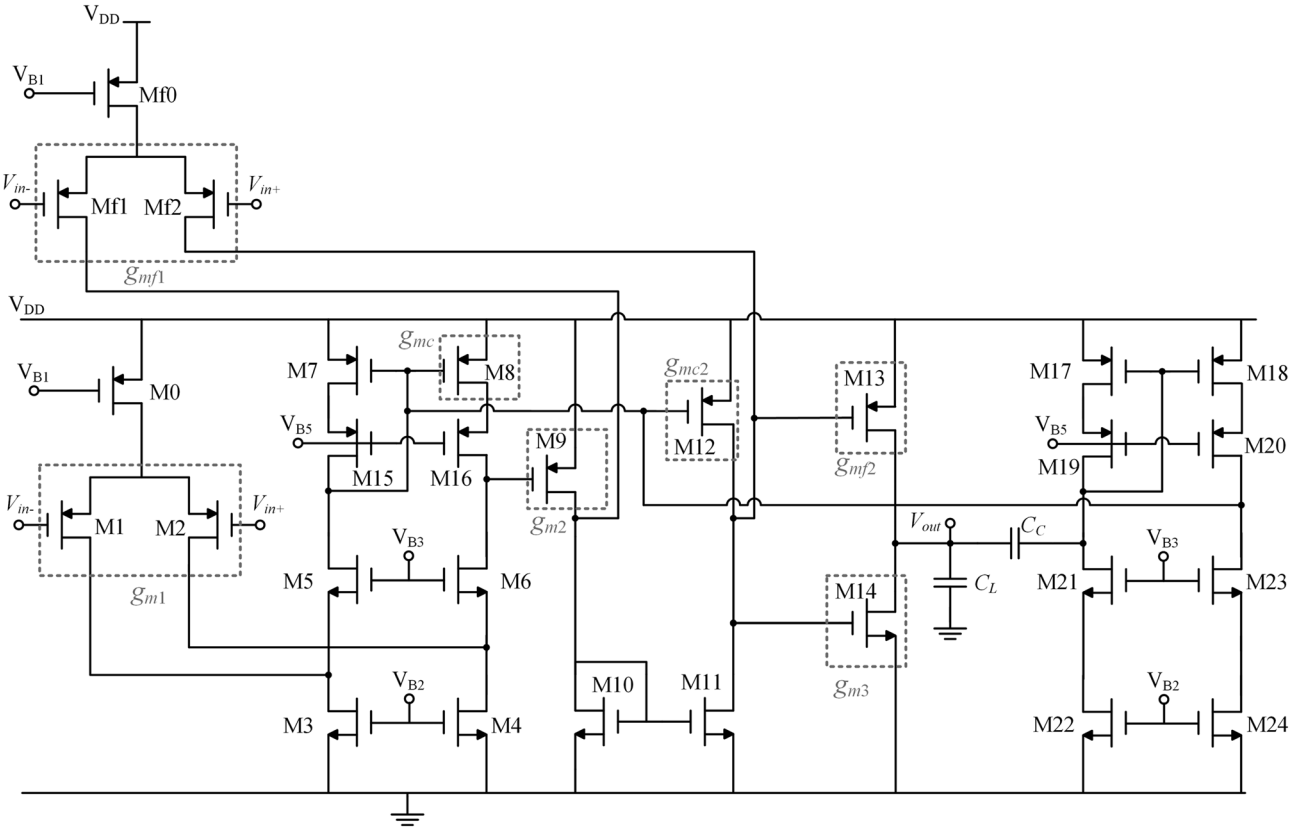

FIGURE 14 Simplified schematic of DACFC topology

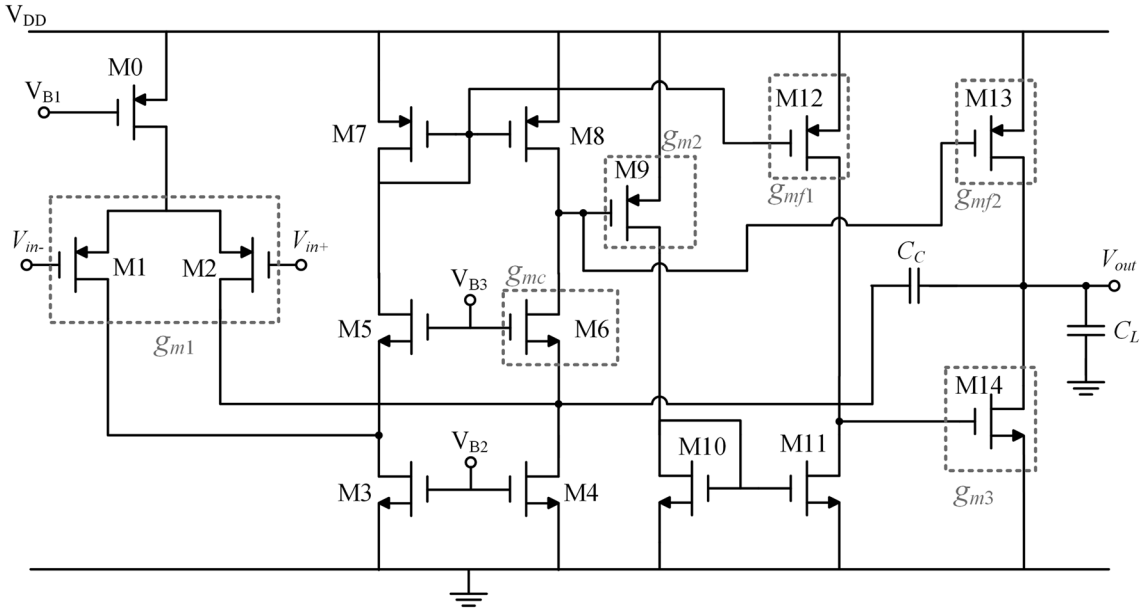

FIGURE 15 Simplified schematic of CFCC topology

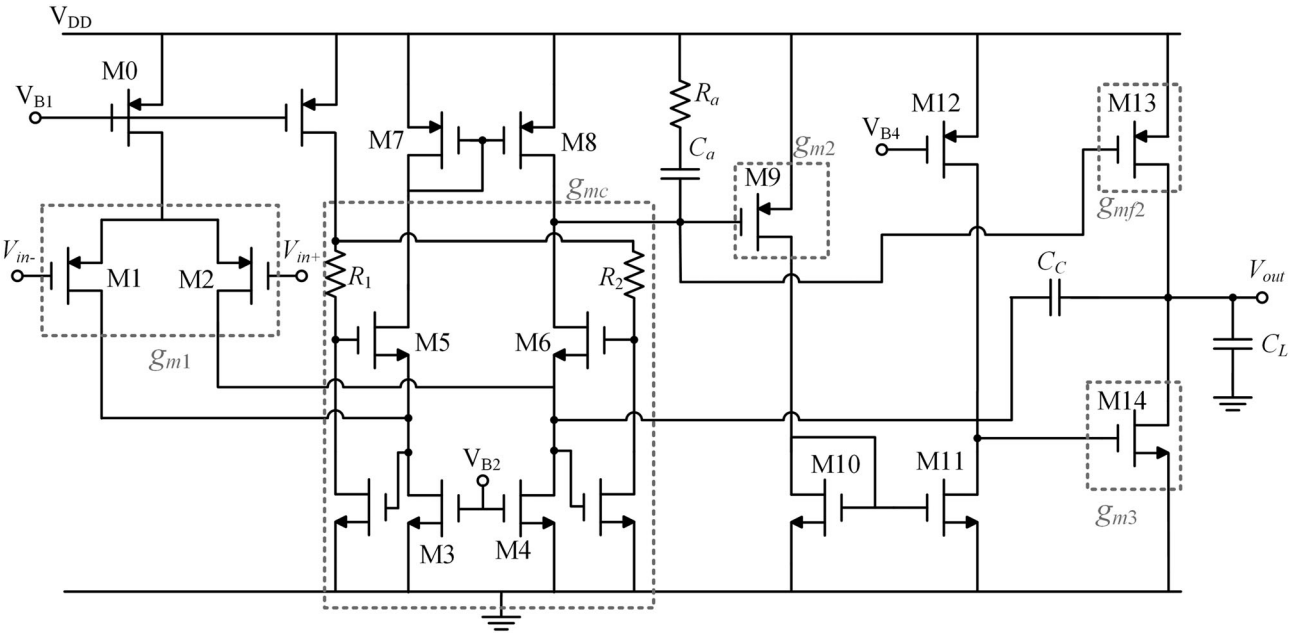

FIGURE 16 Simplified schematic of CBMCPC topology

6 | SIMULATION RESULTS

To further confirm the results obtained in the previous section, transistor-level simulations using a 65-nm standard CMOS technology supplied by STMicroelectronics are carried out. Among the MOS devices available in the design kit, we used the I/O transistors, with a minimum channel length of 0.28 μm and a nominal supply voltage of 2.5 V.

The compensation topologies considered in the previous sections have been implemented using the schematic of the original papers and reported in Figures 12–19. In all topologies, the transconductance g_{mf2} is implemented by connecting the gate of the load transistor of the last stage (M13) to the output of the first stage. The first stage is always

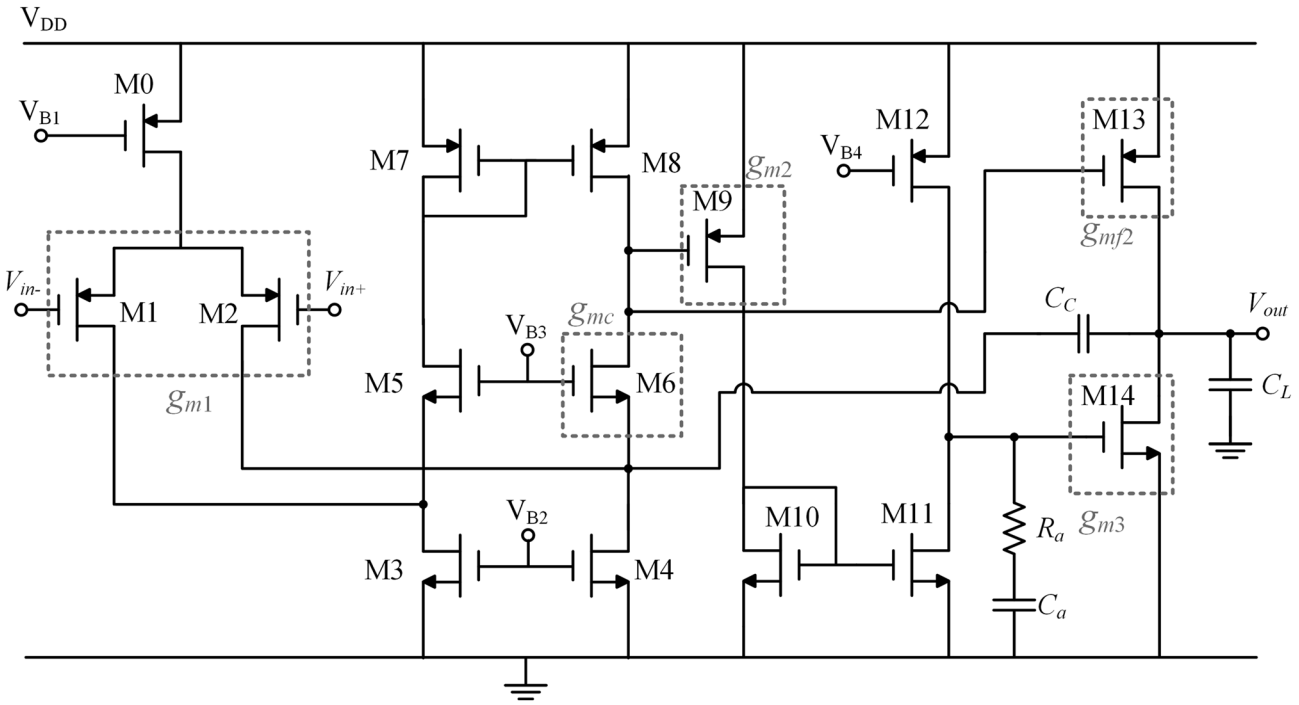

FIGURE 17 Simplified schematic of CLIA topology

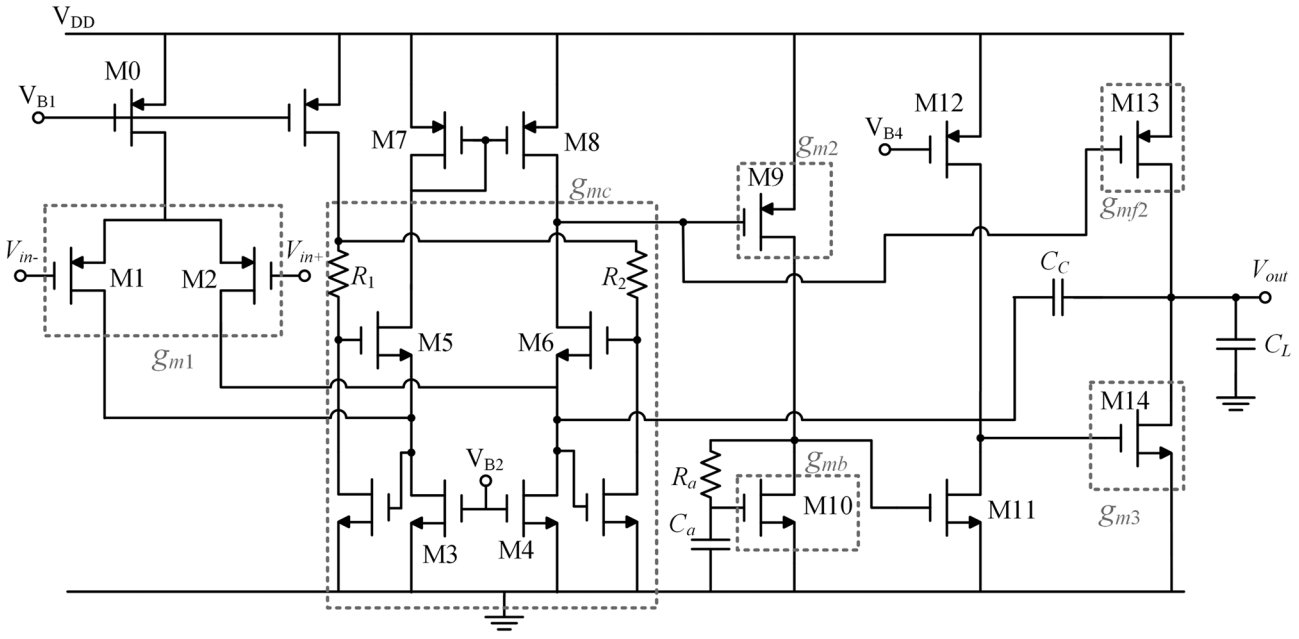

FIGURE 18 Simplified schematic of CBMPPC topology

implemented by a classic folded-cascode topology, which is however fully cascoded (i.e., also in the *p*-channel MOSFET side) only for DACFC and ASHMIF to allow exploiting the embedded current buffers. Note, however, that this solution is not practicable when lower supply voltages are used. For CBMCPC and CBMPPC topologies, the transconductance stage g_{mc} is implemented through a wideband current buffer made up of transistors M3–M8 and R_1–R_2 as done in the original papers,[30,32] respectively. The resulting value of g_{mc} is given by $(1 + 2{\cdot}g_{m5,6}{\cdot}R_{1,2})\, g_{m8}$.

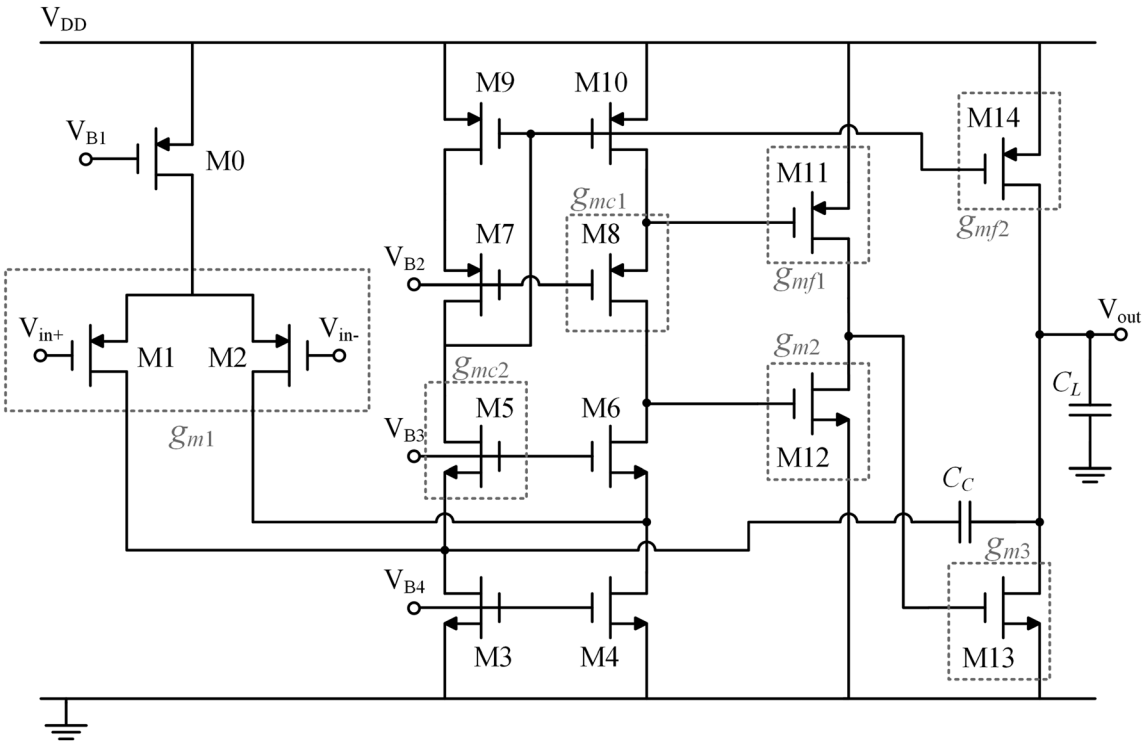

FIGURE 19 Simplified schematic of ASMIHF topology

TABLE 5 Normalized transconductances and passive element values ($C_L = 100$ pF)

Topology	G_{Nm1}	G_{Nm2}	G_{Nmf1}	G_{Nmc}	G_{Nmc2}	A_2	K_{Ra}	K_{Rc}	K_{Ro2}	G_{NmCOM}	C_{o1} (fF)	C_{o2} (fF)	C_A (pF)	C_C (pF)
SMC	0.117	0.125	—	—	—	39.2	—	—	—	1.011	—	265	—	2.26
SMFFC	0.117	0.129	0.127	—	—	22.8	—	—	—	1.132	—	324	—	2.44
IAC	0.117	0.125	—	—	—	39.2	88	—	—	1.011	—	265	2	3.32
IIAC	0.117	0.125	—	—	—	39.2	88	66	—	1.011	—	265	2	2.20
DACFC	0.117	0.129	0.127	0.130	0.126	22.7	—	—	—	1.394	389	324	—	0.96
CFCC	0.117	0.125	—	0.533	—	39.2	—	—	311	1.668	—	265	—	2.66
CBMCPC	0.117	0.125	—	1.260	—	—	61	—	—	2.275	—	265	0.15	0.30
CLIA	0.117	0.125	—	1.260	—	—	61	—	—	2.275	—	265	0.15	0.32
CBMPPC	0.117	0.125	—	1.260	—	—	83	—	—	3.144	381	265	0.25	0.29
ASMIHF	0.117	0.125	0.079	0.125	0.170	—	—	—	320	1.384	381	268	—	1.01

All the amplifiers were designed for a target phase margin equal to 70° and a load capacitance of 100 pF. The normalized transconductance and components values in the compensation network of the simulated amplifiers are given in Table 5 and were set according to the design equations reported in Section 3. Simulation results are summarized in Table 6 where the theoretical and simulated *FOM*, evaluated using Table 3 and 6, respectively, are given in the last two columns. Case 1 is considered for DACFC, CFCC and ASHMIF. Theoretical and simulated *FOM* values are found in good agreement with the design equations in Sections 3 and 4, thus confirming the validity of the proposed methodology.

It is worth noting that some parameters are strictly related to the transistor level implementation of the various stages and may have a strong impact on the amplifier performance.

TABLE 6 Simulation results

Topology	A_0 (dB)	PM (deg)	f_{GBW} (MHz)	SR_{av} (V/μs)†	Power (μW)	*FOM* theor.	*FOM* sim.
SMC	92	70	3.55	1.68	181	2.31	2.26
SMFFC	86	75	3.35	1.55	202	2.03	2.02
IAC	92	69	2.29	1.45	181	1.30	1.21
IIAC	92	72	3.58	1.79	181	2.36	2.28
DACFC	87	74	8.07	2.41	230	4.63	4.40
CFCC	92	69	2.79	1.41	190	1.52	1.44
CBMCPC	98	68	2.77	1.43	222	1.11	1.13
CLIA	98	66	2.65	1.44	222	1.05	1.08
CBMPPC	98	65	29	8.9	222	9.31	12.3
ASMIHF	101	73	7.96	2.29	190	5.22	4.35

TABLE 7 Comparison summary

Topology	Additional active stages	Design effort	Transistor-level implementation complexity	Performance
SMC	Low	Low	Low	Medium
SMFFC	Medium	Low	Medium	Medium
IAC	Low	Low	Low	Low
IIAC	Low	Low	Low	Low
DACFC	High	High	High	High
CFCC	High	Low	Low	Medium
CBMCPC	High	Medium	High	High
CLIA	High	Low	Low	Medium
CBMPPC	High	Medium	High	High
ASMIHF	High	Medium	Low	High

As an example, the amplifier compensated using the SMFFC topology shows a reduction of the *FOM* value due to a lower value of the gain of the second stage, as compared to the SMC case, which is due to the connection of the output of the additional differential pair that implements the g_{mf1}. For the same reason, the value of C_{o2} is higher for SMFFC as compared to SMC. Overall, a lower *FOM* value is obtained with respect to that one can expect from a first look at Figure 8, where equal values for A_2 and C_{o2} are assumed. Same considerations can be done for DACFC and ASHMIF for which this effect is more pronounced due to the different C_{o1} and C_{o2} values.

7 | CONCLUSIONS

In this paper, the main compensation topologies for three-stage amplifiers exploiting only one Miller capacitor are analyzed. Design equations with the phase margin as the main design parameter are derived for all the considered solutions and an analytical comparison is carried out by exploiting a FOM that expresses a trade-off among gain-bandwidth product, load capacitance, and total transconductance, for equal values of phase margin. By adopting the proposed approach, additional information is provided to the designer with respect to a particular compensation topology among all those available.

Simulation results confirm the accuracy of the theoretical analysis and the validity of the proposed comparison. Despite the intrinsic difficulty to define an absolute ranking among the 10 considered compensation topologies, since their performance is dependent on the specific set of design conditions, some general considerations can be drawn. Considering the theoretical analysis and the transistor-level simulation results, a qualitative summary showing the main features of the different topologies is reported in Table 7. It can be concluded that among the topologies considered, IAC and IIAC are in general the less interesting; SMC, SMFFC, and CFCC represent a good compromise between

design complexity and performance; ASMIHF, DACFC, CBMCPC, and CBMPPC can provide advantageous performance in typical conditions, although the latter three solutions entail a more complex transistor level implementation.

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DATA AVAILABILITY STATEMENT

The data that support the findings of this study are available from the corresponding author upon reasonable request.

ORCID

Alfio Dario Grasso https://orcid.org/0000-0002-5707-9683
Davide Marano https://orcid.org/0000-0001-9433-4199
Gaetano Palumbo https://orcid.org/0000-0002-8011-8660
Salvatore Pennisi https://orcid.org/0000-0002-5803-484X

ENDNOTE

* Referring to Equation A1 in the Appendix A, we can use the feed-forward transconductance to set $a_1 = b_1$.

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APPENDIX A

Assuming the following typical transfer function of the open-loop gain of a three-stage amplifier with DC gain A_0 and dominant pole p_1

$$A(s) = \frac{A_0}{\left(1+\frac{s}{p_1}\right)} \frac{1+b_1 s+b_2 s^2}{1+a_1 s+a_2 s^2} \tag{A1}$$

the phase margin is given by

$$\phi = 180^{\circ} - \tan^{-1}\frac{\omega_{GBW}}{p_1} - \tan^{-1}\frac{a_1\omega_{GBW}}{1-a_2{\omega_{GBW}}^2} + \tan^{-1}\frac{b_1\omega_{GBW}}{1-b_2{\omega_{GBW}}^2} \approx \tan^{-1}\frac{1-a_2{\omega_{GBW}}^2}{a_1\omega_{GBW}} + \tan^{-1}\frac{b_1\omega_{GBW}}{1-b_2{\omega_{GBW}}^2} \tag{A2}$$

where the approximation holds since $\omega_{GBW} >> p_1$.

From A2, applying trigonometric functions properties, we get

$$\tan\phi = \frac{1+(a_1b_1-a_2-b_2){\omega_{GBW}}^2+a_2b_2{\omega_{GBW}}^4}{\omega_{GBW}[(a_1-b_1)+(b_1a_2-a_1b_2){\omega_{GBW}}^2]} \tag{A3}$$

In practical cases, it is convenient to separate the contribute due to the zeros, represented by the last term in relationship A2, and hence we can rewrite A2 as[41]

$$\tan(\phi-\phi_B) = \frac{1-a_2{\omega_{GBW}}^2}{a_1\omega_{GBW}} \tag{A4}$$

where ϕ_B is given by

$$\phi_B = \tan^{-1}\frac{b_1\omega_{GBW}}{1-b_2{\omega_{GBW}}^2} \tag{A5}$$