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# Package-Scale Galvanic Isolators Based on Radio Frequency Coupling: Micro–Antenna Design

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**Abstract:** This paper presents the design of on-chip micro-antennas for package-scale galvanic isolators based on RF planar coupling. A step-by-step design procedure is proposed, which aims at the maximization of the weak electromagnetic coupling between the RX and TX antennas integrated on side-by-side co-packaged chips to enable both high isolation rating and common-mode transient immunity thanks to the high dielectric strength and low capacitive parasitics of a molding compound-based galvanic barrier, respectively. Micro-antenna design guidelines are drawn, highlighting the main relationship between coil coupling performance and their layout parameters, which are often in contrast with respect to traditional integrated inductor ones.

**Keywords:** common-mode transient immunity (CMTI); electromagnetic coupling; galvanic isolation rating; on-chip antennas; package; radio frequency; tapered spiral



**Citation:** Spataro, S.; Spina, N.; Ragonese, E. Package-Scale Galvanic Isolators Based on Radio Frequency Coupling: Micro–Antenna Design. *Electronics* **2022**, *11*, 291. https://doi.org/10.3390/electronics11030291

Academic Editor: J.-C. Chiao

Received: 8 December 2021
Accepted: 15 January 2022
Published: 18 January 2022

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## 1. Introduction

Nowadays, the adoption of isolation techniques is mandatory in order to improve safety and reliability in several applications (e.g., industrial sensors, medical equipment, gate drivers for motor control, etc.). A general block diagram of a galvanically isolated system is shown in Figure 1. Typically, two domains, A and B, must be galvanically isolated for two reasons i.e., one of them is subject to hazardous voltages, and/or different ground references are required. Data signals are transferred across the galvanic isolation barrier to enable bidirectional communication between the two interfaces.

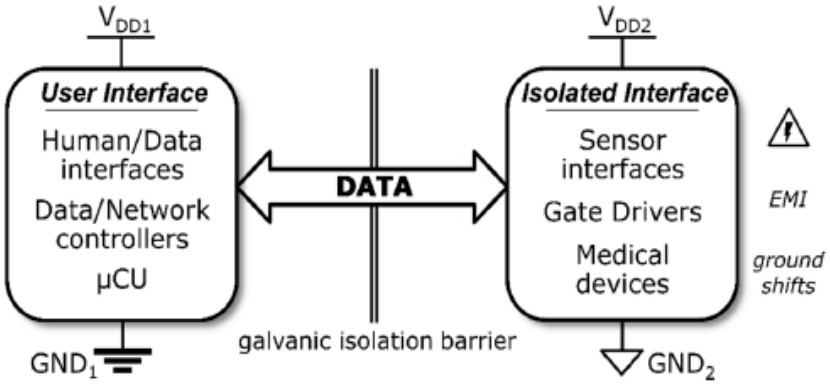



**Figure 1.** Simplified block diagram of a galvanically isolated system.

According to the current standardization for semiconductor galvanic isolators [1], one of the most important performance parameters is the maximum surge isolation voltage, $V_{SURGE}$. It quantifies the capability of the isolator to withstand very high voltage impulses of a certain transient profile, which can arise from direct or indirect lightning

strikes, faults, and short-circuit events. The highest level of isolation, namely reinforced isolation, is certified if a single isolation barrier passes a 10-kV surge test. Another crucial parameter is the common-mode transient immunity (CMTI), which measures the capability of the isolation device to withstand rapid shifts of grounds (i.e., high d$V$/dt), and whose typical values range from 50 kV/µs to 200 kV/µs. Typically, the CMTI performance is related to the parasitic capacitive effects of the adopted galvanic barrier. It is of utmost importance to improve the isolation rating, still maintaining competitive performance in terms of data rate and CMTI. In the near future, application fields, such as the industrial, the automotive, and the medical one, will demand $V_{\mathrm{SURGE}}$ up to 20 kV. Moreover, the higher switching frequencies allowed by wideband power devices, such as gallium nitride high-electron-mobility transistors (GaN HEMT) and silicon carbide (SiC) MOSFETs, will require a CMTI beyond 200 kV/µs [2,3]. Traditional chip-scale isolators are based on capacitors [4,5], transformers [6–14], and LC hybrid networks [15], which exploit either thick silicon dioxide or polyimide layers as an isolation barrier. These approaches reveal inherent limitations in terms of both isolation rating and CMTI due to the maximum manufacturable dielectric thickness and related capacitive parasitics, respectively. A promising approach is represented by the package-scale isolation, which consists in building up a galvanically isolated system by using standard packaging/assembling techniques along with radiofrequency (RF) coupling between two on-chip micro-antennas. A high-potential solution exploits the near-field coupling between two micro-antennas integrated on two side-by-side co-packaged chips, taking advantage of standard molding compound as isolation barrier [16–18]. This paper presents an optimized design procedure of on-chip micro-antennas for package-scale galvanic isolators based on RF coupling. The paper is organized as follows. A brief introduction on package-scale planar isolation and the description of both architecture and circuits of a data transfer system are reported in Section 2. Micro-antenna optimization is detailed in Section 3 by means of a step-by-step design example, taking advantage of full-wave 3D electromagnetic (EM) simulations. Final conclusions are drawn in Section 4.

## 2. Galvanic Isolators Based on RF Planar Coupling

This Section gives an overview of the main characteristics of a galvanic isolator based on a package-scale barrier, highlighting main advantages with respect to traditional chip-scale implementation. Design challenges for system architecture, circuit topologies, and on-chip micro-antennas are discussed in Sections 2.2 and 2.3, respectively.

### *2.1. Chip-Scale Isolation vs. Package-Scale Isolation*

The chip-scale isolation approach is based either on silicon dioxide ($SiO_2$) or on polyimide layers, traditionally used in the semiconductor industry for intermetal isolation and wafer stress relief, respectively. Oxide and polyimide galvanic barriers have different breakdown voltage (BV), fabrication costs, and especially integration levels. Indeed, an oxide barrier can be integrated along with the active circuitry in a two-chip system-in-package (SiP) for each isolated channel (see Figure 2a), guaranteeing an isolation rating of about 6 kV thanks to the high $SiO_2$ BV (i.e., about 1000 V/µm) [6,19]. However, oxide insulation is upper limited by the maximum reliable thickness (i.e., about 10 µm) due to both wafer mechanical stress and second-order BV effects. On the other hand, a polyimide layer can be used to build a stand-alone post-processed isolation-chip (i.e., a capacitor or a transformer) at the expense of a lower integration level (i.e., from two to three chips per each isolated channel, as shown in Figure 2b) [12,14]. Due to a lower BV (i.e., about 250 V/µm), a polyimide barrier requires about a three times thicker layer to sustain the same isolation voltage of an oxide barrier. The overall fabrication costs are the result of a complex combination of silicon and package costs, but typically a silicon-integrated isolation barrier is more expensive than a stand-alone post-processed polyamide one. In any case, both approaches are highly limited in terms of CMTI performance due to the relatively low distance trough insulator (DTI), which is in the order of tens of microns

(typically from 10 µm to 30 µm). Indeed, due to such low DTI, the galvanic barrier exhibits high capacitive parasitics (in the order of tens of femtofarads), and hence high common-mode currents are produced by ground shifts, thus limiting the maximum tolerable voltage slope i.e., the CMTI performance.

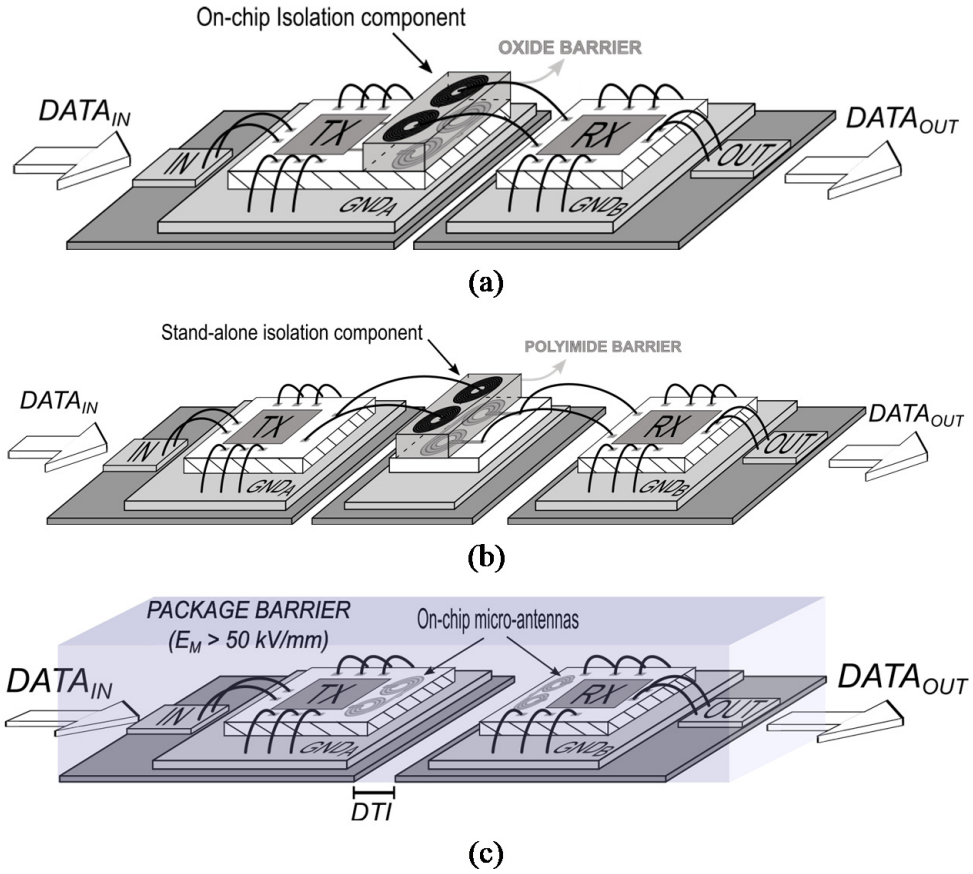



**Figure 2.** Chip-scale versus package-scale isolation: integrated barrier (**a**); stand-alone post-processed barrier (**b**); package-scale barrier (**c**).

Package-scale isolation drastically changes the traditional paradigm. Its key advantage is the use of the molding compound as an isolation layer between two side-by-side co-packaged chips along with the exploitation of a wider DTI (typically hundreds of microns between the chip lead frames) with the aim of increasing the isolation rating while reducing the capacitive parasitics of the galvanic barrier. The physical channel for data communication exploits the week near-field EM coupling (i.e., RF coupling) between two micro-antennas integrated on two side-by-side co-packaged chips, as shown in Figure 2c. In this approach, the DTI must be chosen to guarantee the required isolation rating, ensuring at the same time a reasonable coupling level between the micro-antennas. It should also be noted that the minimum value of the DTI can be often limited by packaging/assembling issues. Standard molding compounds exhibit dielectric strength ($E_M$) of about 50–100 kV/mm, thus enabling reinforced isolation (i.e., $V_{SURGE} \geq 10$ kV) with a DTI of just 200 µm [20,21], which produces very low capacitive parasitics and hence CMTI better than 200 kV/µs [18].

Package-scale isolation based on RF coupling has other advantages compared to traditional isolation approaches. Firstly, a customized technology/component is not required, whereas standard packaging is sufficient to guarantee outstanding isolation and CMTI performance. Moreover, the approach is highly flexible and can be tailored to the application specifications without time-consuming and expensive technology development. On the other hand, such advantages are counterbalanced by a larger silicon area consumption

due to on-chip antennas on both chips, as shown in Figure 2b. Finally, the RF coupling isolation approach is only suited to data transmission. In particular, due to high isolation channel loss, carrier-based modulation is mandatory to enable CMTI performance better than 200 kV/µs with a consequent higher power consumption compared to the impulsive modulation approaches. Package-scale isolation based on RF coupling is compared with the state-of-the-art approaches in Table 1.

**Table 1.** State-of-the-art galvanic isolation approach comparison.

| Isolation Approach | Isolation Layer | No. Chips | Isolation Scale | Custom Technology | Modulation | Power | Design Flexibility | DTI [µm] | Isolation [kV] | CMTI [kV/µs] | Si Area |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Inductive | $SiO_2$/ Polyimide | 2/3 | Chip | Required | Impulsive/ Carrier-based OOK | YES | Low | 10–30 | 5–20 | 75–200 | Medium |
| Capacitive | $SiO_2$/ Polyimide | 2/3 | Chip | Required | Impulsive | NO | Low | 10–30 | 5–10 | 50–150 | Low |
| RF coupling | Molding compound | 2 | Package | Not required | Carrier-based OOK | NO | High | 300–700 | 10–25 | 200–250 | Medium/high |

### *2.2. System Architecture and Circuit Description*

The simplified block-diagram of a package-scale galvanic isolator based on RF planar coupling is shown in Figure 3 with reference to a single physical channel. Due to the extremely low magnetic coupling coefficient, $k$, between the transmitter (TX) and receiver (RX) micro-antennas, $L_{TX,}$ and $L_{RX}$, carrier-based narrowband communication is mandatory to achieve significant performance in terms of both data rate and CMTI [16–18]. Typically, data transmission adopts on-off keying (OOK) pulse width modulation (PWM) of the RF carrier. Indeed, the PWM technique ensures higher robustness compared to the traditional amplitude-shift keying (ASK) modulation, since the bit information is the RF burst duration rather than its amplitude.

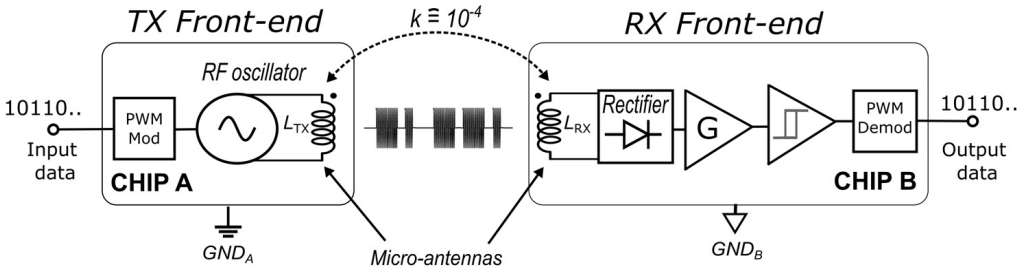



**Figure 3.** Simplified block-diagram of galvanic isolator based on RF coupling (single physical channel).

The TX front-end is integrated into Chip A and mainly consists of an RF oscillator adopting the micro-antenna, $L_{TX}$, as an inductive tank. The oscillator is properly turned on and off by the PWM digital stream produced by the PWM modulator. Chip B integrates the RX front-end that exploits the RX micro-antenna, $L_{RX}$, weakly coupled to the TX one, to detect the magnetically induced RF voltage. After rectifying and filtering, the RX envelope voltage, further amplified by the gain stage $G$, drives a hysteresis comparator to reconstruct the transmitted PWM signal. Finally, a baseband PWM demodulator is used to draw the original digital bit stream. Due to the high channel loss (about 30–45 dB depending on the adopted technology and chip distance), the system is operated in narrowband mode with both micro-antennas resonating at the RF carrier frequency, $f_{RF.}$

The most critical blocks of the galvanic isolator architecture in Figure 3 are the RF oscillator and the rectifier stage. In particular, the RF oscillator design is very challenging due to stringent specifications in terms of the current consumption for a given oscillation voltage and the start-up time. When thick oxide/lateral transistors with high breakdown voltages are available, as in the BCD technologies [6–10], the *D*-class topology is highly preferred, as shown in Figure 4a. Indeed, the *D*-class oscillator boosts the oscillation voltage

well above two times the supply voltage, $V_{DD}$, [22] provided that the maximum drain-gate voltage $V_{DG\_MAX}$ is high enough. Since the maximum allowable gate-source voltage, $V_{GS\_MAX}$, is smaller than $V_{DG\_MAX}$, coupling capacitors, $C_B$, are used to perform a voltage partition with the gate capacitance of $M_{1,2}$ thus properly setting the $V_{GS}$ peak to prevent gate-oxide breakdown. Additional capacitor $C_P$ is used to tune the oscillation frequency, $f_{RF}$. Alternatively, if only standard MOS devices are available, the traditional inductor-loaded complementary cross-coupled oscillator shown in Figure 4b can be exploited. It maximizes the oscillation amplitude within the supply voltage, while giving the advantage of nearly doubled transconductance at the same current level compared with a simple cross-coupled oscillator, also minimizing the startup time. As far as the rectifier stage is concerned, key performance parameters are sensitivity and input impedance, along with CMTI and power consumption. A mixer-based solution has been adopted in [18]. However, it requires an additional pre-amplification stage and quite high-power consumption. On the other hand, very interesting solutions are based on common-source (CS) configurations that inherently provide high input impedance along with high gain, and lower power consumption, as in [23].

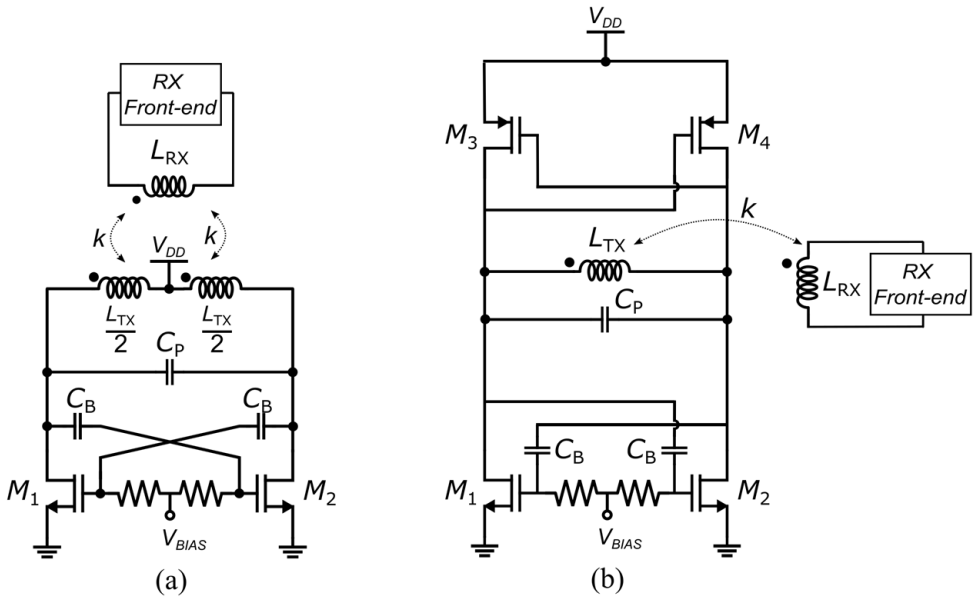



**Figure 4.** RF oscillator topologies for galvanic isolator based on RF coupling: D class oscillator (**a**); complementary cross-coupled oscillator (**b**).

Typically, galvanically isolated interfaces require multi-channel capability, which can be implemented by multiplexing different data channels on the same physical link, provided that a sufficiently high data rate is available [11,14]. However, several applications also require bidirectional communication, such as in isolated gate drivers. For half-duplex data transfer, a single physical isolated link can be used, while full-duplex communication calls for an additional physical link [18] (see Figure 5).

The design of a bidirectional full-duplex galvanic isolator has to cope with the TX-to-RX cross-talk between channels, as represented in Figure 5. It can be fatal for data transmission due to the high loss of the isolated link. A simple solution is to increase the spacing between channels at the cost of a higher silicon area, as done in [18]. However, channel spacing must be more than twice the DTI to achieve a TX-to-RX rejection better than 15 dB. Therefore, it is mandatory to exploit different RF resonance frequencies (i.e., $f_{RF}$ separation) for each channel [16].

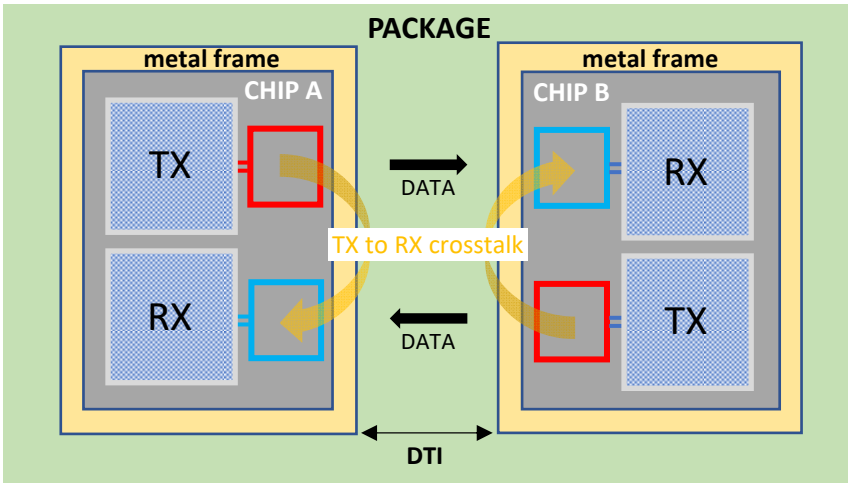



**Figure 5.** Representation of bidirectional full-duplex galvanic isolator based on RF coupling.

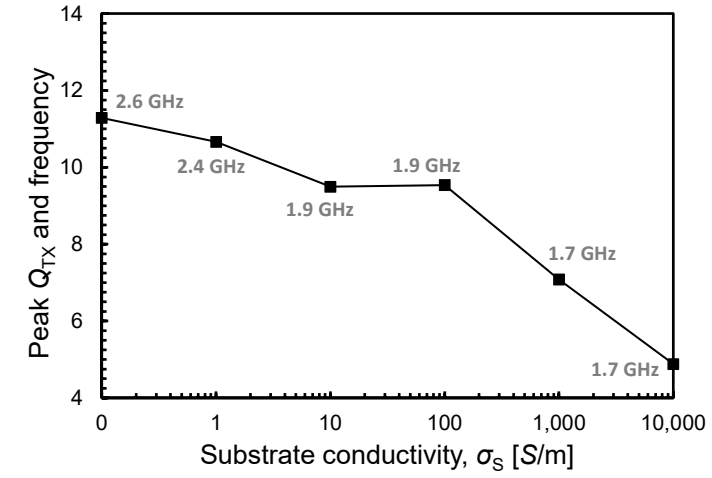
### *2.3. On-Chip Micro-Antenna Design Guidelines*

The design of on-chip micro-antennas has several similarities with the design of RF spiral inductors [24]. However, in galvanic isolator applications, the main goal is the reduction of the channel loss that is highly related to antenna EM coupling. Therefore, some important differences with traditional inductors must be highlighted to properly address the micro-antenna design. As for inductive components, the integration process plays a key role since it determines the loss phenomena taking place in the substrate and the coil itself. Low conductivity substrate and thick top metal layers are crucial to reducing parallel and series losses, respectively. As far as the substrate conductivity, $\sigma_S$, is concerned, main performance parameters of micro-antennas are highly degraded for $\sigma_S$ higher than $10^3$ S/m, such as quality factors ($Q_{TX}$ and $Q_{RX}$), magnetic coupling coefficient ($k$), and TX-to-RX coupling loss, as defined below [18].

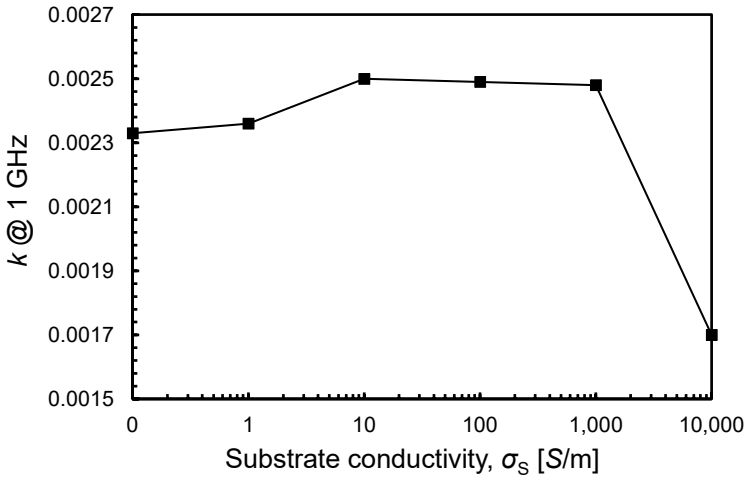
$$TRX = -20log_{10}\left|\frac{V_{RX}}{V_{TX}}\right| \quad (1)$$

where $V_{RX}$ and $V_{TX}$ are the voltage at the RX and TX micro-antennas, respectively.

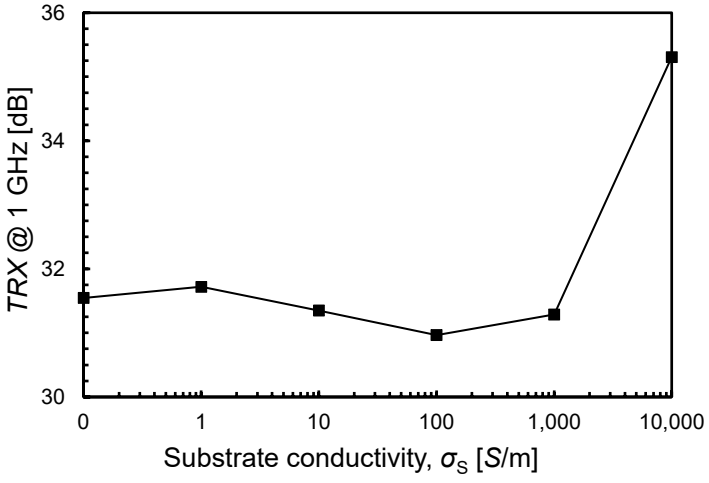
This is demonstrated in Figure 6 by means of parametric 3D-EM simulations of a typical RX/TX antenna configuration at a distance of 600 µm. Specifically, reported curves reveal an optimum range of the substrate conductivity between 10 S/m and 100 S/m. Such conductivity values are typical for RF CMOS and BiCMOS technologies. Unfortunately, galvanic isolated interfaces are also required in standard BCD platforms, largely used in power applications (e.g., gate drivers). Such technologies adopt very highly doped substrate ($\sigma_S > 10^4$ S/m), which poses additional challenges in the micro-antenna design. In particular, the most representative performance parameter for galvanic isolators based on lateral RF coupling is the TX-to-RX coupling loss, *TRX*, in the resonance condition. As shown in Figure 6c, *TRX* is worsening by more than 4 dB for a substrate conductivity of $10^4$ S/m. It is worth mentioning that for such isolators, it is mandatory that the system is operated in resonance condition to reduce the channel loss. This can be better understood by comparing the *TRX* performance with and without the resonance condition, which reveals an improvement of 13 dB at the operating frequency of 1 GHz, as depicted in Figure 7.




(**a**)




(**b**)




(**c**)

**Figure 6.** Micro-antenna performance as a function of substrate conductivity, $\sigma_S$, obtained by means of 3D EM simulations of typical TX/RX antenna configuration at a 600-µm distance: (**a**) peak of $Q_{TX}$ and corresponding frequency; (**b**) magnetic coupling coefficient, *k*, between TX and RX antennas at 1 GHz; (**c**) TX-to-RX coupling loss at 1 GHz (open-circuit and resonance conditions).

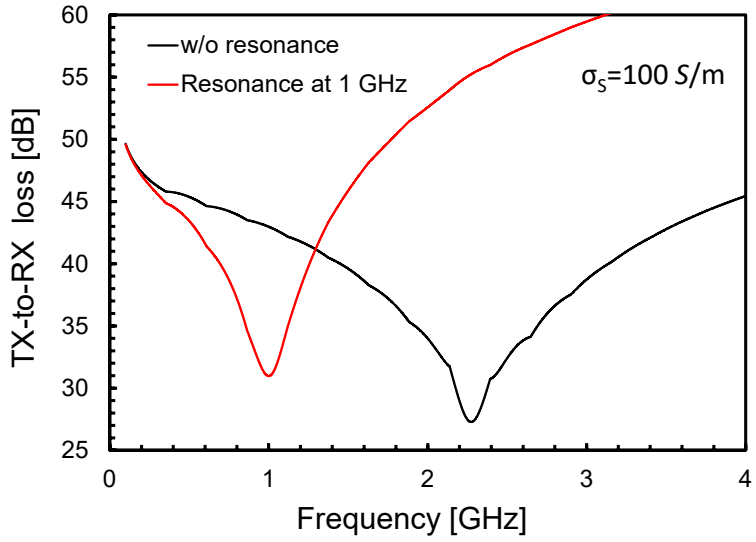



**Figure 7.** TRX performance in open-circuit conditions for $\sigma_S$ = 100 S/m.

The main design target is minimizing the TX-to-RX coupling loss i.e., maximizing the induced voltage at the RX antenna for a given voltage at the TX one. A simple but effective design expression in open circuit condition can be easily drawn by modeling the isolated channel at the operative frequency, $f_{RF}$, as shown in Figure 8. The adopted model takes into account the overall micro-antenna losses (i.e., both ohmic series losses and substate losses) by means of the equivalent resistances, $R_{TX}$ and $R_{RX}$, series connected to the equivalent antenna inductance values, $L_{TX}$, $L_{RX}$. Magnetic and electric couplings between micro-antennas are modeled by the magnetic coupling factor, $k$, and parasitic capacitance, $C_M$, respectively. In actual implementations, being a parasitic capacitor, $C_M$, very low (i.e., below 5 fF), its coupling effect can be neglected to simplify calculations. The resulting design expression is reported below.

$$\left|\frac{V_{RX}}{V_{TX}}\right|_{OC} = \frac{k \cdot N}{\sqrt{1 + \frac{1}{Q_{TX}^2}}} \tag{2}$$

$$N = \sqrt{\frac{L_{RX}}{L_{TX}}} \tag{3}$$

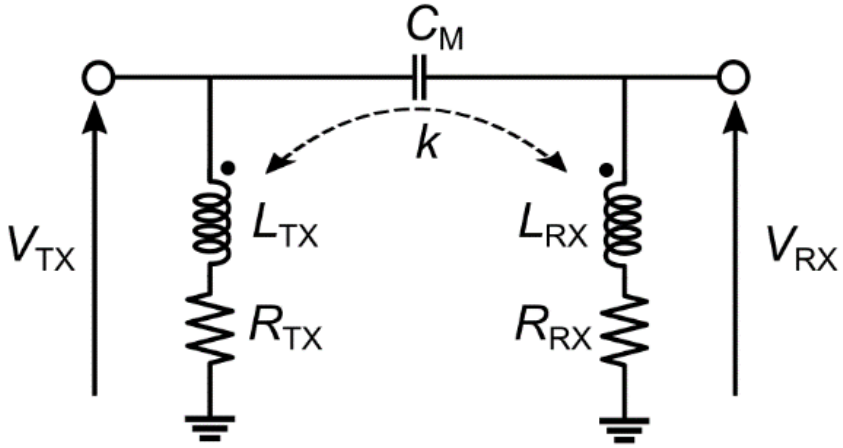



**Figure 8.** Simplified model of the isolated channel for *TRX* evaluation.

From Equations (1)–(3), it is evident that minimizing *TRX* requires the maximization of the magnetic coupling coefficient, $k$, the step-up ratio, $N$, and quality factor of the TX antenna, $Q_{TX}$.

As far as the antenna shape is concerned, although polygonal and circular spirals achieve 10–20% higher $Q$-factors compared to squared ones at gigahertz frequencies [25,26], they do not ensure maximum EM coupling, thus recommending the use of square or rectangular coils, which benefit of longer laterally facing sides. The aspect ratio of the rectangular antenna, $AR$, (i.e., ratio of its longer-facing side to its shorter side) must be optimized by accounting for contrasting performance, such as the $Q$-factor and the EM coupling (see Figure 9). Indeed, the higher is $AR$ the lower is the coil $Q$-factor, due to increased current crowding into the inner windings [27], the higher is the EM coupling between antennas thanks to longer-facing sides. Moreover, if bidirectional channels are present, the TX-to-RX cross-talk plays an important role in defining the antenna $AR$. Indeed, exploiting an $AR$ higher than one also reduces the parasitic EM coupling between different adjacent channels (see Figure 5).

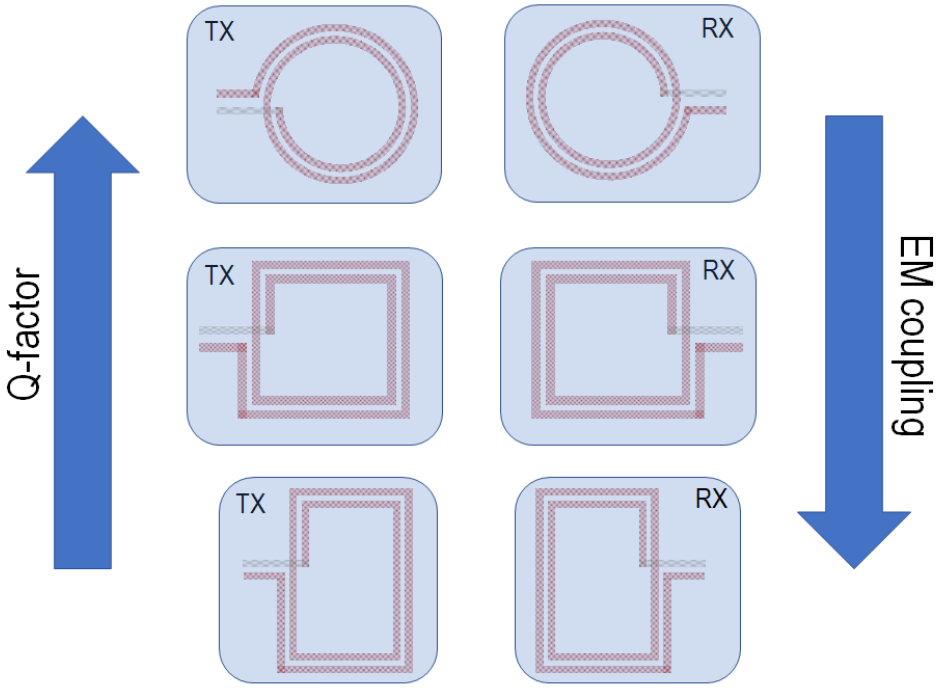



**Figure 9.** Micro-antenna shape optimization.

A final consideration is about the TX antenna spiral layout, which has to comply with the adopted oscillator topology. Indeed, a simple not symmetric spiral can be used in a complementary cross-coupled oscillator (see Figure 4b), as in [16,18]. On the other hand, if a $D$-class oscillator is preferred, a symmetric antenna topology is mandatory to ensure the central tap connection for the supply voltage, $V_{DD}$. In this situation, an effective solution to increase the EM coupling between antennas is the adoption of two identical coils in a U-shape fashion, as shown in Figure 10, since the current flowing in the antenna has a clock-wise direction in both single windings.

The starting point for the design of the micro-antennas is the definition of their layout parameters (i.e., the number of turns, $n$, the inner diameter, $d_{IN}$, the metal width, $w$, and the metal spacing, $s$) to set the low-frequency inductance values. The latter can be easily calculated with good precision by means of closed-form equations available in the literature [28], also enriched with the metal thickness, $t$, to improve the accuracy for high $t/w$ ratio (i.e., very thick and/or narrow coils). The antenna inductance, $L_{RX}$, is mainly dependent on the number of turns, $n$, and the inner diameter, $d_{IN}$. Given the operative

frequency, $f_{RF}$, $L_{RX}$ is also upper bounded by the input parasitic capacitance of the RX front-end. A general design guideline is using a small metal width, $w$, along with a high number of turns to achieve the highest value of the inductance-to-area ratio and therefore the highest self-resonance frequency for the RX antenna. It is worth mentioning that if the input impedance of the RX front-end (i.e., of the envelope detector in Figure 3) is sufficiently high (i.e., nearly open condition), the degradation of the $Q_{RX}$ due to a small $w$ is irrelevant for the induced voltage at the RX antenna. Given the $L_{RX}$ value, the maximization of the step-up ratio, $N$, calls for the use of the lowest value of $L_{TX}$ (i.e., low number of turns) compatible with a proper operation of the RF oscillator in terms of startup time and power consumption. In this perspective, since a crucial role is played by the $\omega QL$ product of the TX antenna, the maximization of the $Q$-factor is mandatory. To this aim, a sufficiently large metal width, $w$, is preferable, while the coil external diameter is already defined by the RX antenna geometry to maximize the TX-to-RX EM coupling.

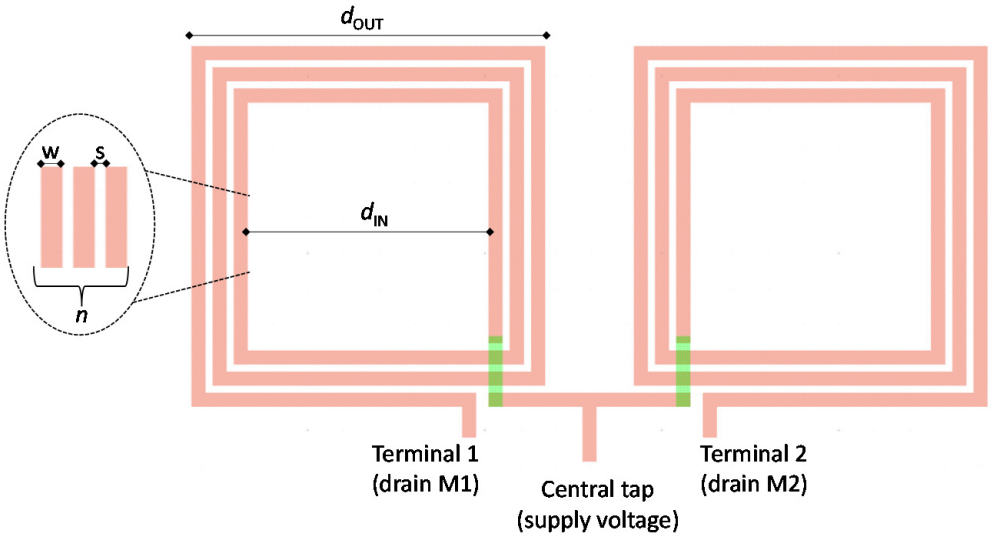



**Figure 10.** Micro-antenna U-shape configuration for *D*-class oscillator.

A final consideration has to be done about the tuning between the TX oscillation frequency, $f_{RF}$, and the RX antenna resonance frequency, $f_{RX}$, which is mandatory to minimize *TRX*, as shown in Figure 7. On the TX side, since the oscillator core parasitic capacitances are highly nonlinear due to signal variations of several volts, they are very difficult to be accurately modeled [29]. To avoid unpredictable simulation errors, it is highly suggested to set the oscillation frequency, $f_{RF}$, by means of a dominant parallel capacitor $C_P$ (i.e., at least ten times higher than the parasitic capacitance) and then consider its statistical variations within a Montecarlo simulation run. On the RX side, small-signal modeling of the envelope detector parasitic capacitances is sufficiently reliable, but an additional small capacitance can be used for fine-tuning of $f_{RX}$.

## 3. Micro-Antenna Optimization

### *3.1. On-Chip Micro-Antenna Design Guidelines*

In this work, a 0.32-µm BCD technology by STMicroelectronics has been used for each of the two side-by-side co-packaged chips. The process provides a BEOL with three thin Al layers along with a top thick Cu metal. This fabrication technology had been chosen since it is largely adopted in high-voltage applications (i.e., for gate drivers in both industrial and automotive environments). Moreover, it offers high-voltage, laterally diffused metal-oxide-semiconductor (LDMOS) transistors well suited to implement a *D*-class oscillator. However, it adopts a very conductive silicon substrate (i.e., $\sigma_S$ is about $10^4$ S/m) which is very critical for the EM coupling between the micro-antennas (see Figure 6). The adoption of such technology for a package-scale galvanic isolator, is particularly useful to

highlight some design issues. Indeed, the high value of $\sigma_S$ requires careful optimization of the micro-antennas to minimize the TX-to-RX coupling loss. The design of the galvanic isolator has been carried out by means of EM simulations of the micro-antennas. Although time-consuming, a 3D full-wave simulator (i.e., Ansoft HFSS) was preferred to a more traditional 2D (i.e., Keysight ADS Momentum) one due to its higher accuracy in terms of EM coupling when the substrate conductivity is quite high. In this regard, Figure 11 reports a comparison between the results obtained by the two mentioned EM tools for the same antenna configuration. The average error in terms of *TRX* is about 6 dB in the analyzed frequency range, which is probably due to the parasitic couplings through the highly conductive substrate that a 2D simulator is not able to distinguish for each antenna dice.

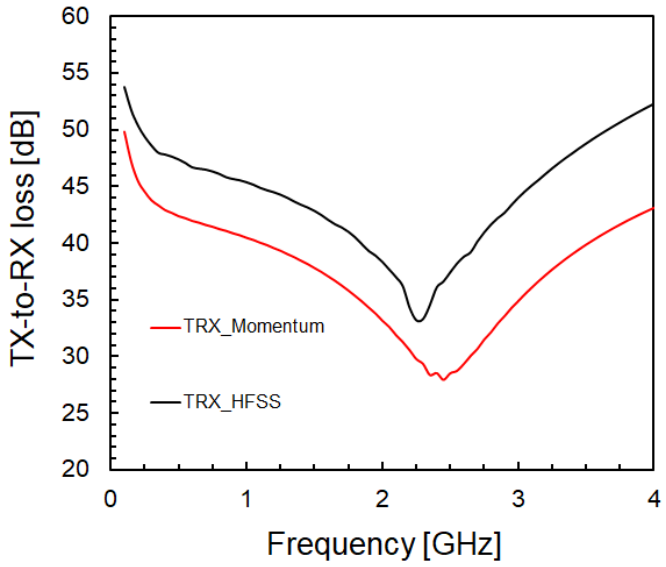



**Figure 11.** Comparison between HFSS and ADS Momentum: TRX for RF coupled antennas on a high conductive substrate ($\sigma_S = 5 \times 10^4$ S/m).

A 3D-view of the simulated antennas in HFSS is shown in Figure 12. For the EM simulation set-up, a box of molding compound surrounding the two chips was encased within a box of air. A first-order absorbing boundary condition (ABC) was assigned on the whole air-box surface except for the two regions under the chip frames where perfect-E boundary conditions hold. Each micro-antenna was excited by means of three lumped ports (i.e., the two-terminal and the center tap connection). Finite tetrahedral first-order elements were used for the mesh, which was adaptively refined through ten steps. Moreover, in order to improve the solution quality, an additional mesh refinement was adopted in the antenna metal traces and in the molding compound region between the dies. Finally, the solution frequency was equal to the operative frequency, $f_{RF}$, while a wider frequency sweep from 0.1 GHz up to 8 GHz was set.

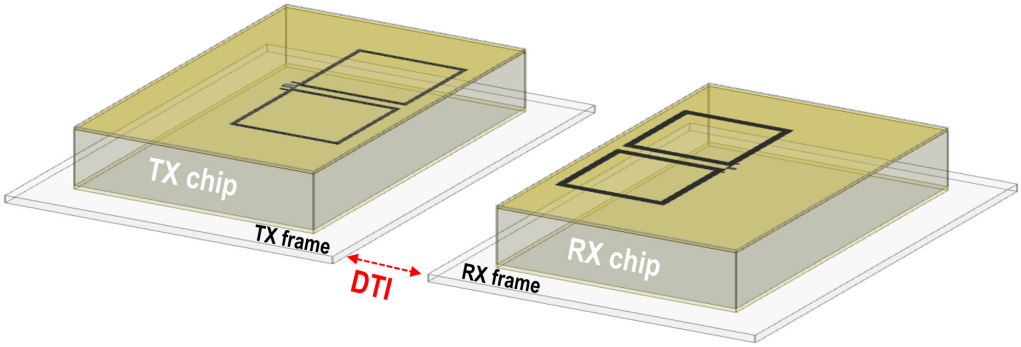



**Figure 12.** 3D EM simulation view of TX and RX micro-antennas for a package-scale galvanic isolator.

### *3.2. Optimization Flow for TX and RX Antennas*

The adopted design flow is described in the block diagram in Figure 13. The first step, A, includes the definition of the DTI between chips and RF carrier frequency, $f_{RF}$. The DTI must comply with both the isolation rating and assembling constraints. In this design example, it has been set to 500 µm to achieve an isolation rating higher than 10 kV (i.e., reinforced isolation) by using a standard molding compound ($\varepsilon_r$ = 5.5). The RF carrier frequency, $f_{RF}$, is upper limited by the oscillator operation at a given current budget. Other constraints could be related to the specific application (i.e., data rate, channel multiplexing, EM emissions or external interferences, etc.). In this work, $f_{RF}$ has been set equal to 1.5 GHz.

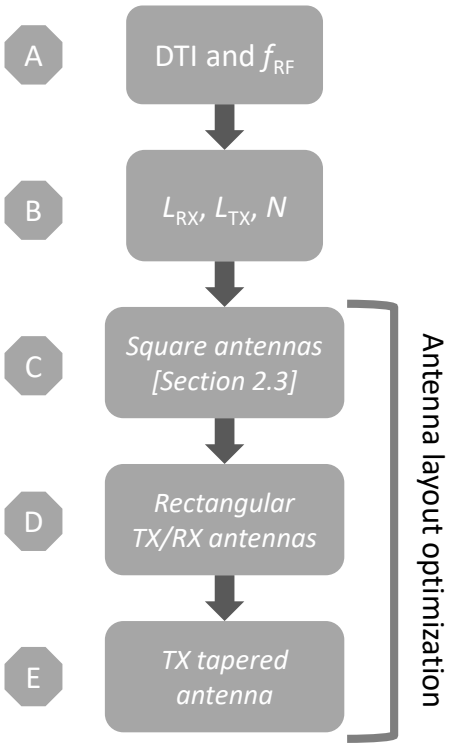



**Figure 13.** Simplified block diagram of the proposed design flow.

In step B, both antenna inductance values are properly chosen. The starting point is the RX antenna inductance, $L_{RX}$, which is set to the highest possible value compatible with the input capacitance of the RX front-end. The voltage step-up ratio, $N$, is then maximized by using the lowest value of the TX antenna inductance, $L_{TX}$, that allows the RF oscillator to be properly operated at a reasonable value of $Q_{TX}$ and without exciding the current consumption constraint.

As previously said, the design of the micro-antenna layout is crucial to minimize the TX-to-RX coupling loss. Indeed, according to (2) and (3), the maximization of the magnetic coupling coefficient, $k$, must be pursued. In the flow diagram shown in Figure 13, a three-step optimization is proposed for the antenna geometry optimization (namely steps C, D, and E). Table 2 summarizes the main antenna geometrical parameters for each layout configuration. It is worth noting that through the whole optimization process both $L_{TX}$ and $L_{RX}$ and thus $N$, are kept broadly constant at the operative frequency (about 7 nH and 78 nH for $L_{TX}$ and $L_{RX,}$ respectively). In the initial antenna optimization step (C in Figure 13), both TX/RX coils have been drawn according to the general design guidelines discussed in Section 2. Specifically, square antennas with two windings in a U-shape fashion have been designed, as shown in Figures 10 and 12. For the RX antenna, the minimum allowed metal trace (i.e., 1.6 µm) has been chosen. On the other hand, the width of the TX spiral has been properly set to comply with the minimum $Q$-factor, $Q_{TX\_MIN}$, required by the RF

oscillator. It is worth noting that in the adopted BCD technology the antenna *Q*-factors are very low due to highly conductive substrate, which produces a consequent increase of the oscillator current consumption. Specifically, using a *D*-class oscillator topology with LDMOS devices, the minimum value of the *Q*-factor for the TX antenna, $Q_{TX\_MIN,}$ is equal to 4 in the adopted process for a TX current budget of about 15 mA.

**Table 2.** Geometrical parameters of TX/RX antennas.

| Antenna Layout | $d_{out,\ max}$ [μm] | TX Antenna | | | | RX Antenna | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | *AR* | *W* [μm] | *s* [μm] | *n* | *AR* | *w* [μm] | *s* [μm] | *n* |
| C | 306 | 1 | 4 | 1.5 | 2 | 1 | 1.6 | 1.7 | 6 |
| D | 345 | 1.03 | 7 | 1.5 | 2 | 1.30 | 1.6 | 1.7 | 6 |
| E | 345 | 1.03 | 1.6 (*)/9.8 | 1.5 | 2 | 1.30 | 1.6 | 1.7 | 6 |

* Antenna facing side.

Moving to the next optimization step (D in Figure 13), the rectangular shape is adopted for both antennas. The aim is to exploit longer laterally facing sides of the antennas to improve the magnetic coupling, as claimed in (2). The aspect ratio, *AR*, of the RX antenna has been increased up to 1.3, still ensuring almost the same self-resonance frequency, *SRF*. On the other hand, for the TX antenna, only a slight variation of *AR* is allowed in order to avoid a further *Q*-factor degradation due to the increase of inner coil current crowding effects. It is worth mentioning that the TX coil perimeter increases going from step C to step D, thus allowing an effective increase of the metal width (from 4 to 7 μm) to keep the $L_{TX}$ value almost constant.

In the last step E, further optimization is carried out by using a tapered coil configuration (i.e., using a variable width in the same coil) with the aim of increasing the magnetic coupling between the RF micro-antennas. To properly drive the design of an effective tapered coil, three simple test cases for package-scale RF isolators have been compared by means of 3D EM simulations. Each adopted test case employs two identical one-turn square coils for both RX and TX antennas, respectively, whose main geometrical and electrical parameters are summarized in Table 3.

**Table 3.** Geometrical and electrical parameters of the three test cases.

| Test Case | Geometrical Parameters | | | | Electrical Parameters @ 8 GHz | |
|---|---|---|---|---|---|---|
| | *n* | $d_{IN}$ [μm] | $w_{MIN}$ [μm] | $w_{MAX}$ [μm] | *L* [nH] | *k* |
| 1 | 1 | 340 | 8 | 8 | 1.07 | $5.3 \times 10^3$ |
| 2 | 1 | 340 | 2 (*) | 11.4 | 1.08 | $5.7 \times 10^3$ |
| 3 | 1 | 340 | 4.6 | 32 (*) | 1.04 | $4.5 \times 10^3$ |

* Antenna facing side.

The operative frequency has been chosen about a fifth of the *SRF* since a similar proportion holds for the TX antenna in the actual isolator design. Specifically, the first test case is the reference one since it adopts a traditional single turn coil with a fixed width (i.e., 8 μm). Two different tapered structures are evaluated, which are obtained by using a reduced or enlarged width for the antenna facing side for test cases 2 and 3, respectively (i.e., 2 or 32 μm). To keep constant both inductance and, to some extent, the *SRF*, the width of the non-facing sides is properly increased or reduced for test cases 2 and 3, respectively.

Figure 14 compares the magnetic field distribution for the simulated test cases. EM simulations reveal that the magnetic field strength in the antenna facing side becomes greater as the width decreases. On the other hand, the magnetic field in the non-facing sides reduces as the width increases. This qualitative analysis is further confirmed by the

magnetic coupling coefficient, $k$, that achieves the highest value for test case 2, as shown in Table 2. However, in the actual isolator design, the trace width of the RX antenna has been already minimized (i.e., the slightest width allowed by the technology) and no further improvements are achieved by a tapered structure that instead can be adopted for the TX antenna, as detailed in Table 2.

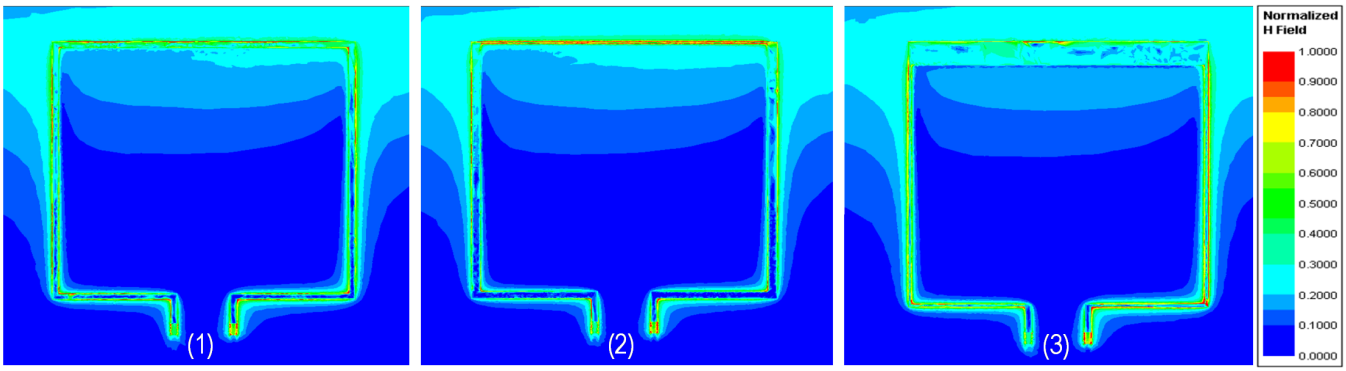



**Figure 14.** Normalized magnetic field distribution for the simulated test cases in Table 3.

Figure 15 reports both inductance and $Q$-factor curves of the TX antenna for each design steps C, D, and E. On the other hand, no significant performance variations occur in the RX antenna from design step C (see Figure 16) to D, while the antenna remains unchanged from D to E. The increase of the TX antenna parasitic capacitance produces a slight reduction of its $SRF$, while the $Q$-factor at the operating frequency of 1.5 GHz always guarantees a proper operation of the RF oscillator (i.e., higher than $Q_{TX\_MIN}$). Thanks to the antenna optimization procedure, the magnetic coupling factor, $k$, is improved by about 19% from steps C to E, which, in turn, produces a reduction of the TX-to-RX coupling loss in open circuit and resonance condition of about 1.7 dB, as shown in Figure 17.

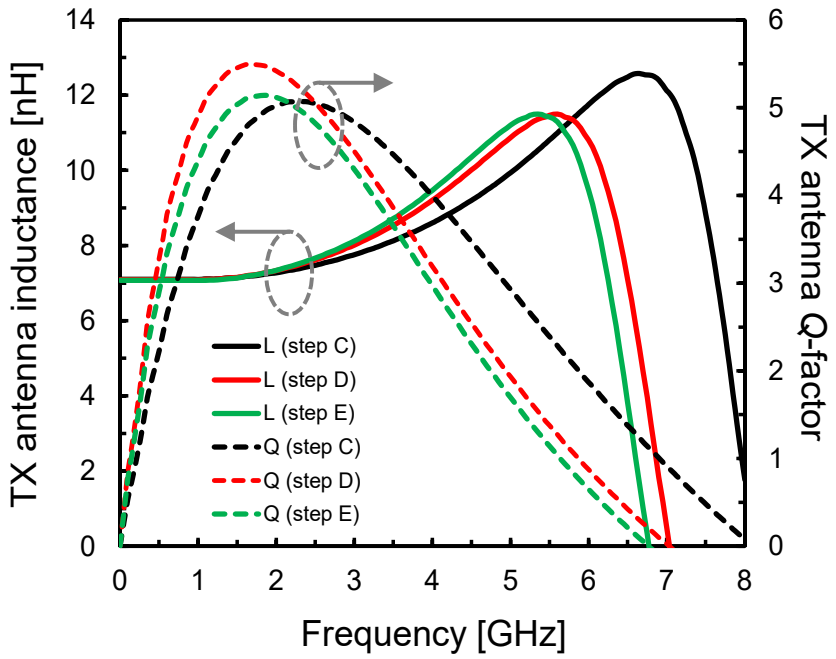



**Figure 15.** Inductance and Q-factor of the TX antenna for steps C, D, and E.

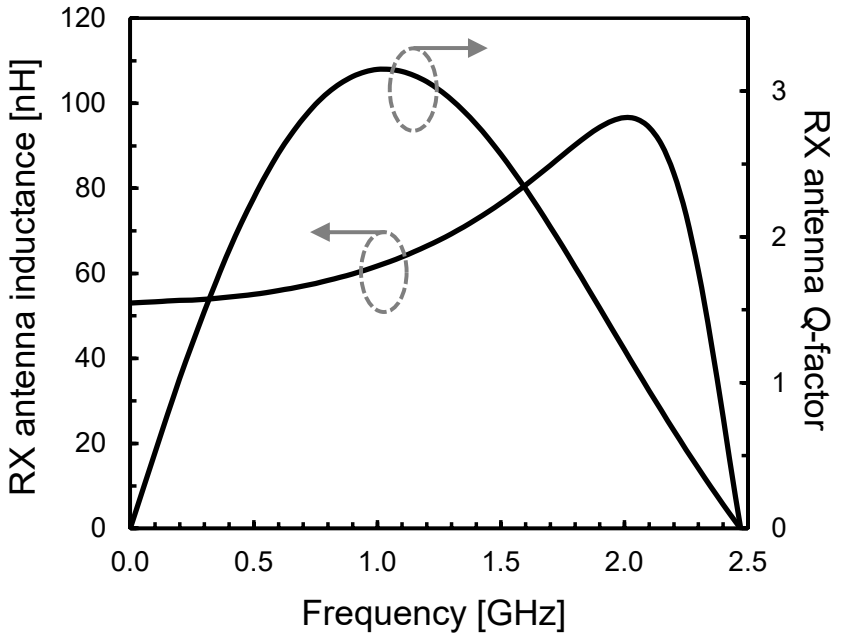



**Figure 16.** Inductance and *Q*-factor of the RX antenna for step C.

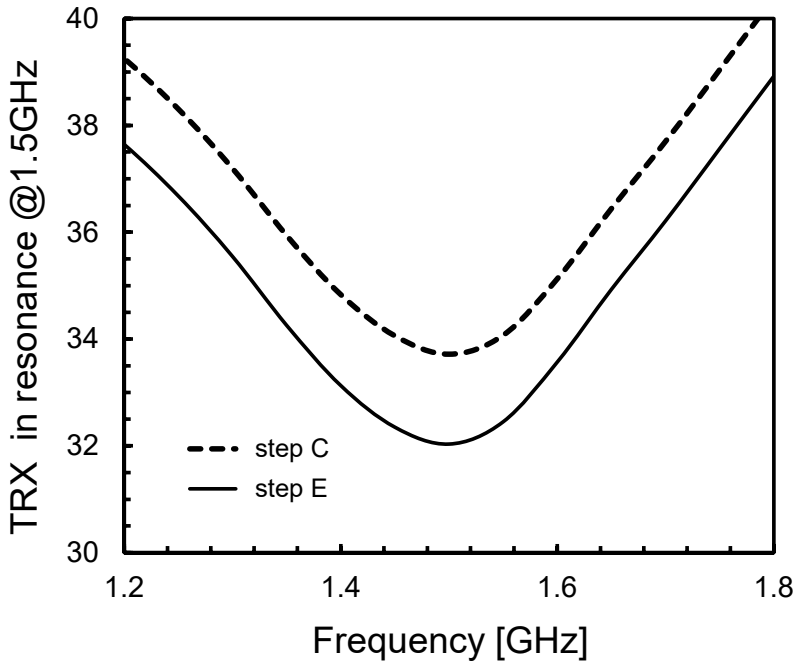



**Figure 17.** TRX in open circuit and resonance condition at 1.5 GHz.

For the sake of completeness, Figure 18 depicts the magnetic field distribution at the operative frequency (i.e., 1.5 GHz) for the TX/RX micro-antenna configuration in design step E, obtained by means of 3D EM simulations with a TX antenna differential excitation.

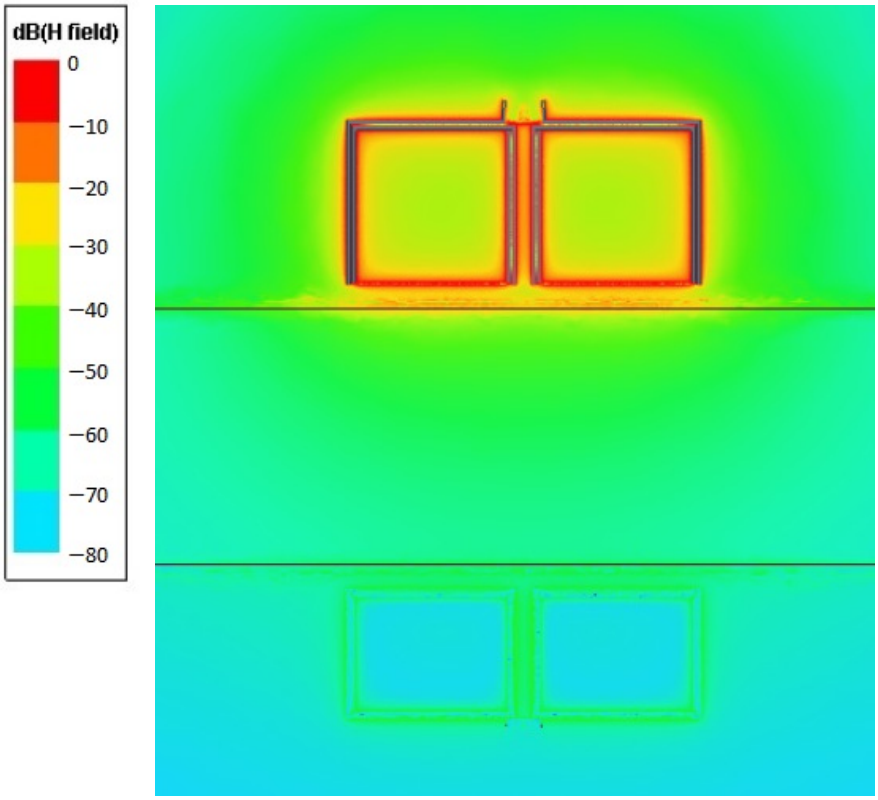



**Figure 18.** Magnetic field distribution at the operative frequency (i.e., 1.5 GHz) for the TX/RX micro-antenna configuration (design step E).

## 4. Conclusions

This paper has disclosed an effective design procedure of on-chip micro-antennas for package-scale galvanic isolators based on RF planar coupling. For the first time, key design guidelines have been proposed and then the antenna optimization flow has been verified by means of 3D EM simulations carried out for a galvanic isolator integrated in a 0.32-μm BCD technology. The main results of the proposed optimization procedure are:

(1) a significant improvement of the EM coupling in terms of magnetic coupling factor (i.e., 19% in the reported design example)
(2) a consequent reduction of the TX-RX coupling loss (i.e., 1.7 dB in the reported design example).

Such performance has been achieved without affecting the design parameters related to both TX and RX front-ends, being only the result of the optimization of the galvanically isolated channel. The proposed micro-antenna design procedure will be adopted in the next integrations of complete package-scale galvanic isolators in different technology platforms (i.e., CMOD. BCD, GaN).

**Author Contributions:** Conceptualization E.R.; validation S.S. and E.R.; formal analysis S.S. and E.R.; investigation, S.S., N.S. and E.R.; project administration, E.R.; supervision, E.R.; writing—original draft, E.R.; writing—review and editing, E.R. All authors have read and agreed to the published version of the manuscript.

**Funding:** This work was supported in part by the University of Catania through the Project "Programma Ricerca di Ateneo UNICT 2020-22 linea 2".

**Data Availability Statement:** The data presented in this study are available on request from the corresponding author.

**Conflicts of Interest:** The authors declare no conflict of interest.

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