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Structural characterization of semiconductor multi-layer pad

Michele Calabretta[1], Alessandro Sitta[1], Salvatore Massimo Oliveri[2] and Gaetano Sequenzia[2]

Abstract

Structural mechanics and mechanical reliability issues are becoming more and more challenging in the semiconductor industry due to the continuous trend of the device dimensional shrinkage and simultaneous increased operative temperature and power density. As main consequence of the downsizing and more aggressive operative conditions, the mechanical robustness assessment is now having a central role in the device engineering and assessment phase. The risk of mechanical crack in the brittle oxide layers, which are embedded in pad stacks, increases during the device manufacturing processes such as the electrical wafer testing and during wire bonding. This risk increases with the presence of intrinsic mechanical stress in individual layers resulting from the metal grain growth mechanisms, the stack layers' interfacial mismatches in coefficients of thermal expansion and the temperature stress induced by doping diffusion and film deposition. The current trend of innovation in the electronic industry is going over the semiconductor material itself and it is now impacting the improvement of the Back-End of Line. Key actors are becoming the interactions between the semiconductor die and the device packaging such as adhesion layers, barriers and metal stacks. In the present work, different pad structures have been structurally analyzed and benchmarked. The experimental characterization of the pad structures has been done through a flat punch nano-indentation to investigate on the mechanical strength and the crack propagation. The considered mechanical load reproduces the vertical impact force applied during wire bonding process to create the bond-pad electrical interconnection. The obtained testing results have been compared to finite element models to analyze the stress distribution through the different layers' stacks. Scope of this work is to demonstrate the validity of the proposed integrated numerical/experimental methodology, showing the impact of the metal connections layouts by the analysis of the stress notch factors and crack propagation behaviour.

Keywords

Pad, finite element, nanoindentation, stress analysis

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Introduction

The constant trend of downscaling the structures in the microelectronics industry is addressing the device designers to consider the stress management as a key factor for the final product optimization. From a structural standpoint the device optimization is based on the containment of the intrinsic stress caused by the layers deposition, by the proper selection of the thermal budget applied during the device fabrication, by the optimization of the assembly processes with relevant mechanical impact such as the die attach and wire bonding and by the crack propagation analysis through the multi-layered stack during the real application lifetime conditions. Moreover due to the recent and constant increase in Gold (Au) cost, Copper (Cu) wires are becoming an attractive solution to manage the overall package cost. As counterpart, Copper wires introduce much higher mechanical stress to the underlying bond pad structures due to the higher stiffness and lower ductility of Copper in comparison to Gold. According to this, the layer composition of metal and dielectric and their layout represent a driving factor for die development in terms of compatibility and proper matching with the assembly processes conditions like as the wire

[1]Automotive and Discrete Group R&D, STMicroelectronics, Catania, IT
[2]Dipartimento di Ingegneria Elettrica Elettronica e Informatica (DIEEI), Università degli Studi di Catania, Catania, IT

Corresponding author:
Gaetano Sequenzia, Dipartimento di Ingegneria Elettrica Elettronica e Informatica (DIEEI), Università degli Studi di Catania, Viale Andrea Doria, 6, 95125, Catania, IT.
Email: gsequenzia@diim.unict.it

bonding force and dissipated power in order to optimize performances and mechanical reliability. Due to the brittleness of the oxide dielectric layers, the application of an external mechanical load such as the wire bonding process could represent a serious risk of the entire die mechanical integrity.[1–4] Considering the continuous trend of reducing the device thickness to improve the on-resistance electrical behaviour, several structural options have been proposed. A solution consists in using a soft material interposed in the metal stack[5,6] or in the use of a thicker final metal layer to prevent the mechanical issue related to the device top side.[7] For what concern Vertical Integrated Power Device, the presence of connecting vias to link the different layer of metal been presented as a reliability risk factor.[8–11] This issue is enhanced by the higher energy and force required by copper wire bonding.[12,13] Due to the mentioned mechanical issues, Finite Element Analysis is an interesting tool to characterize the induced stress on pad structure and to optimize pad mechanical performances.[2,14–17]

Shen et al.[14] have studied how pad structure affects cracks in dielectric layer by means of wire bonding experiments and developing a 3D Finite Element Model using the commercial software Ansys. Some strong hypotheses have been assumed for numerical analysis, such as the replacement of the real deformed free air ball with a equivalent cylinder and the simplification of the real capillary/ball contact during ultrasound by a defined displacement load $u(t)$. Simulations have confirmed maximum tensile stress is the most appropriate parameter to detect oxide failure and that top dielectric layer is the most prone to fail due to wire bonding induced stress. Chen et al.[15] have proposed a 2D Finite Element Analysis in Marc Mentat with the purpose to characterize the stress distribution in silicon substrate generated by the ball formation in Cu-Cu wire bonding process. Simulation results have been correlated with micro-Raman spectroscopy measurements in silicon and microscopic analysis of grain distortion to underline copper plasticity. Liu et al.[16] have proposed a 2D approach Ansys-based to simulate the entire wire bonding process, both for ball bonding process and ultrasound application. Contacts between capillary and free air ball (FAB) and between FAB and bond-pad have been accounted to a reliable deformation and stress calculation. Finite Element Analyses have shown that a thicker bond pad reduces stress in bond-pad while plugs inside the dielectric enhance stress concentration in the contact regions between plugs and dielectric. Mancaleoni et al.[2] have recently extended this last approach in 3D Finite Element Model with Marc Mentat software. Another kind of approach[17] is focused on the crack propagation analysis during nanoindentation by extended finite element analysis (XFEM) and cohesive zone method (CZM) in ABAQUS on a dedicated sample made by silicon substrate and a specific dielectric (silicon nitride in the specific case study). By the way, it seems that no model has been developed, like in the presented work, to calculate the induced stress and deformation in a bond-pad structure during a nanoindentiation test.

Methods and materials

Methods

The proposed approach is an integrated method made by the combination of experimental tests and numerical simulations in order to understand the phenomena and reproduce it by mechanical modeling. A novel methodology combining experimental nanoindentation tests with finite element (FE) analysis has been proposed for the structural analysis and optimization framework. Nanoindentation technique is typically adopted for characterizing material mechanical properties highlighting the cracking issues and the thin film fracture toughness.[17–19] The experimental procedure consists in penetrating the tested material by an indenter tip with a controlled applied load. One of the nanoindentation output is the material hardness that is obtained dividing the maximum applied load by the contact area between tip and the tested sample. From the load monitoring during the penetration of the tip and its relaxation is it possible to study the mechanical behaviour of the stacked layers: the physical analysis on the tested samples could underline if local damage occurred. In the presented work, the maximum dielectric layers' tensile stress induced by the virtual reproduction of the nanoindentation test has been calculated by FE model as function of the applied penetration force. The considered model has been correlated with experiments on two different pad layouts by means of physical analysis. The tested samples have been prepared by using a Focus Ion Beam (FIB) and then analyzed by Scanning Electron Microscopy (SEM) for structural integrity and the incipient crack detection check. After the model validation, two additional layouts proposal have been virtually evaluated without the need of the experimental activity thanks to the developed methodology.

Test vehicles and experimental test

The considered test vehicles are Vertical Intelligent Power Device (VIPower), a technology that combines, through the stacked metal for electrical interconnection, the Vertical Double Diffused MOS "Power" devices and the "intelligent" CMOS components for Power-Analog-Mixed design. The analysis of the present work has been addressed to the device front side in order to characterize the mechanical integrity under mechanical load of the exposed pad. A design benchmark in terms of mechanical behaviour has been done showing the difference due to the

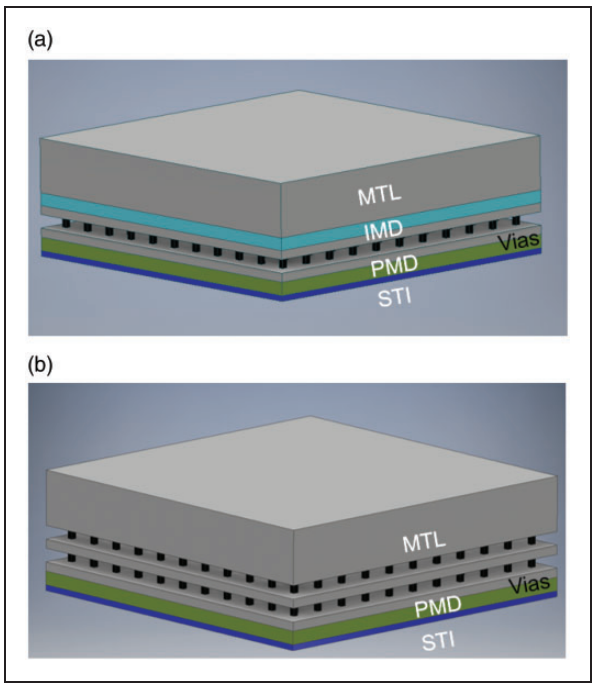

Figure 1. Pad stacks 3D CAD-models used for the comparison, in which IMD layers (in cyan) have been hidden if there are vias inside. Pad B shows the presence of tungsten vias both in IMD2 and IMD1 layers, whereas pad A has tungsten vias only in IMD1. (a) Pad A. (b) Pad B.

presence or not of the tungsten vias throughout the dielectric layers of the pad as reported in Figure 1.

The considered device is constituted by a Silicon substrate insulated by shallow trench isolation (STI) field oxide. The overhead pad stacks are composed by three Aluminum-Copper (AlCu) metal layers, which are interleaved by two tetraethil orthosilicate (TEOS) dielectric layers (IMD), and could be connected by tungsten vias. Underneath the lowest metalization layer a pre-metal dielectric (PMD) layer made by Borophosphosilicate glass (BPSG) has been considered. Ti layers have been engineered as barriers over each metallization. The overall device structure has been graphically described in Figure 2. The mechanical assessment has been done by means of Nanoindentation technique using a CSM Instruments' Nanoindenter Tritec NHT 50-160. Considering the soft behavior of the top metal layer, it has been required a wide and uniform contact area between tip and surface in order to control the tip penetration. Indeed, the Nanoindenter has been equipped with a diamond flat punch tip that consists of truncated cone geometry in which the smaller circle penetrates the indented sample. In this specific case study the radius of the tip contacting area is $5\,\mu$m radius. Residual tip imprints on pad metal have been reported in Figure 3.

Several applied load values, ranging from 50 to 200 mN, have been applied on two pad layouts. The load exploration has been done to search for a

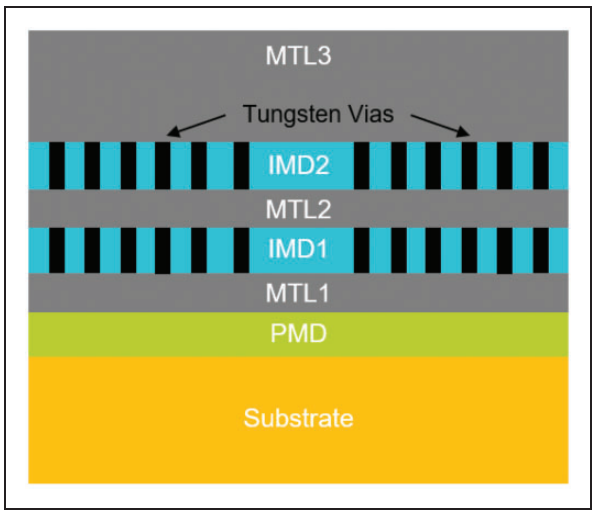

Figure 2. Device simplified cross-section schematic.

Figure 3. Nanoindentation tip imprints on aluminum metal.

suitable force magnitude able to highlight the differential mechanical behavior between the pad solution under analysis. The load exploration has been performed using a fixed time frame for the entire indentation with the consequent of considering different strain rate for each testing condition. As depicted in Figure 4, each indentation penetration force has been linearly increased from 0 to maximum value in 30 s, a period of 10 s has been considered as dwell time and finally the unloading occurs linearly in 30 s.

Figure 5 shows the force-penetration behavior at different applied loads on pad A. Observing Figure 5, it has been highlighted tip penetration does not decrease during the nanoindentation unloading phase. This means achieved pad metal deformation is almost totally permanent. No significative differences have been observed between the indentation curves of pad A (reported in Figure 5) and B in terms of overall displacement. A dedicated physical analysis has been employed to characterize the mechanical effect of the vias on the pad layers.

Focused ion beam (FIB) has been performed on the indented samples in order to investigate by

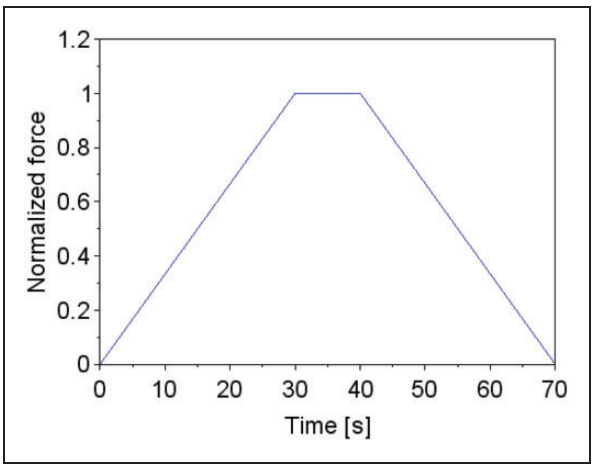

Figure 4. Normalized load time profile during nanoindentation.

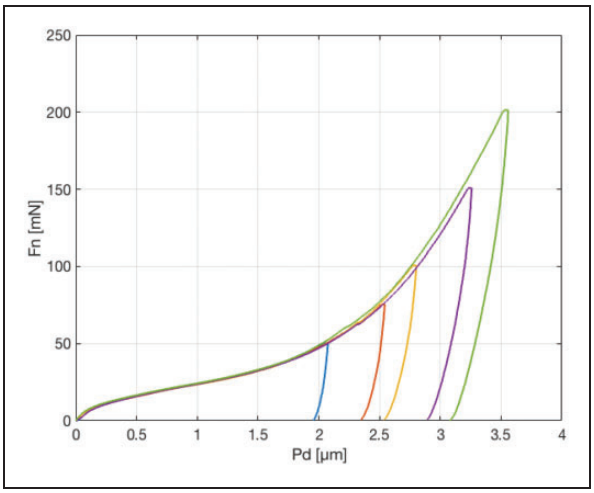

Figure 5. Force vs penetration curves for the nanoindentation trials on pad A. Different load conditions, varying from 50 to 200 mN, has been considered.

scanning electron analysis (SEM) the mechanical robustness of layers inside pad structures considering different indentation load. As experimental equipment, it has been used a Zeiss Neon 40. Secondary electron imaging mode has been considered for experimental acquisitions. The scope of this analysis has been to point out if the pad structures A and B show a different mechanical robustness after nanoindentation tests. SEM analyses have been performed on samples indented at 100 mN and at 75 mN, as shown respectively in Figures 6 and 7.

SEM analysis at 100 mN has detected crack in both pad structures, even if it appears to be more severe in pad B. Considering analysis pads indented with a lower load (75 mN), it has been shown crack signs in top IMD layer of pad B close to the tungsten plugs. In pad A, there isn't any crack formation in the top IMD layer, in which there are no tungsten vias. According to the observed different behavior between the top IMD layer of pad A and B, vias

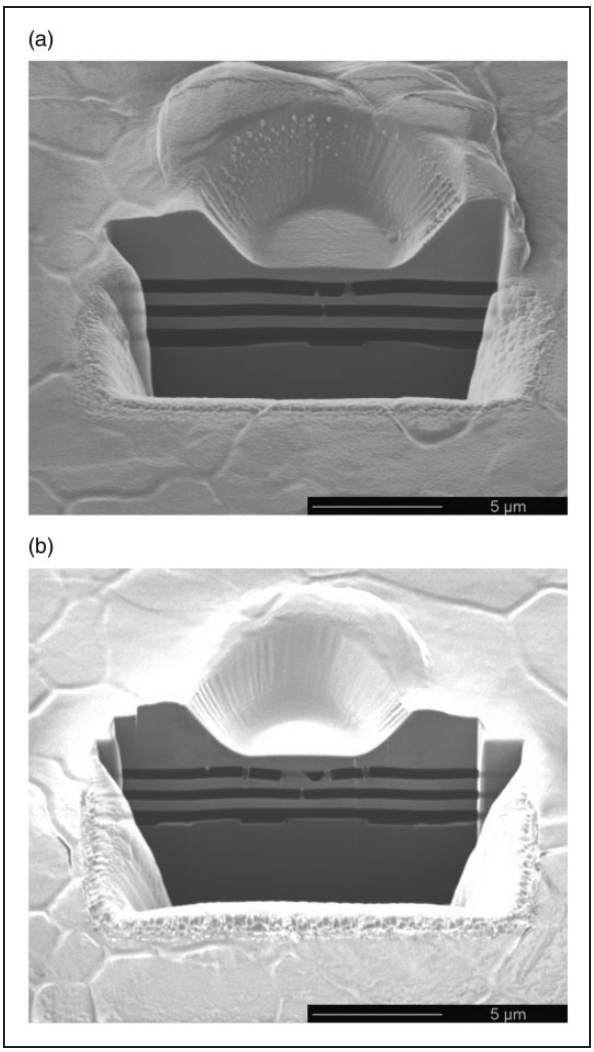

Figure 6. Scanned Electron Microscopy (SEM) of samples after the application of 100 mN indentation load. The top IMD is cracked in both pad structures. (a) Pad A. (b) Pad B.

have shown a negative impact on the pad mechanical robustness under nanoindentation load.

Finite element analysis

A 3D Finite Element Model has been developed to evaluate the mechanical robustness of different pad layouts during nanoindentation test. Simulations have been employed using COMSOL Multiphysics software. First, numerical results have been benchmarked and aligned with the experimental evidences in terms of failure mechanisms during nanoindentation load, as shown in Figure 7, and nanoindentation force/displacement curve. The analyzed pad structures A and B have been reported in Figure 1. Once the model has been validated, the mechanical behavior of two new pad layouts (pad C and D) has been assessed only virtually, not performing dedicated experiments. More details on these pad structure and the related simulation results have been later discussed.

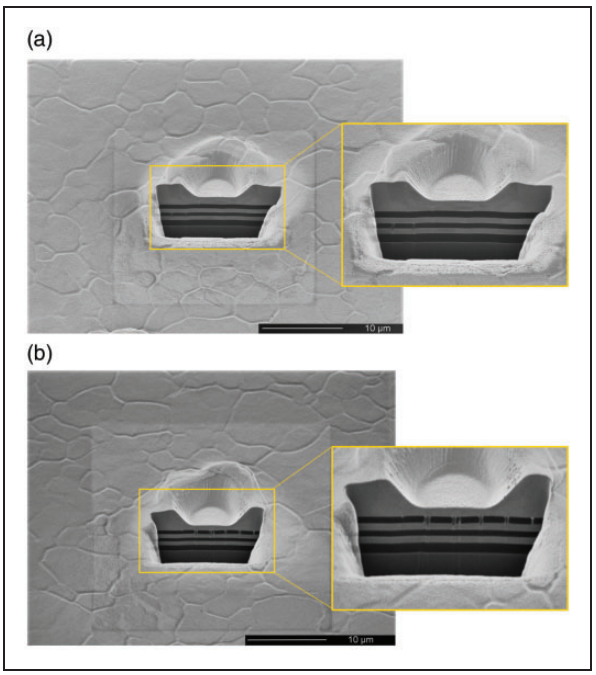

Figure 7. Scanned Electron Microscopy (SEM) of samples under 75 mN of indentation load. Some crack signs have been detected in pad B close to the vias. (a) Pad A. (b) Pad B.

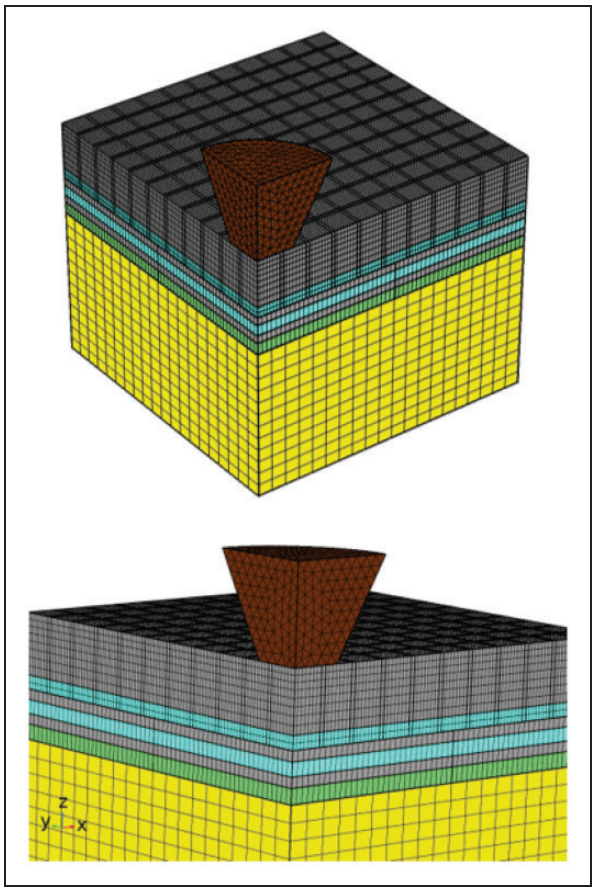

Figure 8. Implemented mesh for 3D finite element model of pad B. Not coherent mesh at interfaces have been highlighted.

The pad structure has been reproduced in finite element model according to the schematic reported in Figure 2. Layers, such as Ti barriers or STI, have been neglected due to their thickness, two or more magnitude orders smaller, than other layers. About 103,000 elements (mainly linear hexahedral) have been used to reproduce stack layers. Flat punch tip, which consists of 5 μm diameter and cone angle 60°, has been reproduced by tetra elements. The realized solid model, including tip and pad B, is drawn in Figure 8.

As depicted in picture, not coherent mesh has been created at some device interfaces, in particular between diamond tip and metal 3, IMD2 and metal 2 and PMD and substrate. These mesh discontinuities have been managed suppressing all relative nodal displacements at the interfaces. An exception has been considered for diamond tip and AlCu metal contact pair that has been accounted using a penalty-based formulation. According to this method, proper nodal loads act to prevent the penetration of one surface's nodes into the segments of the other. When a node starts to infiltrate into a surface, a dedicated force tends to push out the penetrating node from the penetrated surface. These applied loads are proportional to the penetration depth and to a constant called "contact stiffness" which shall depend on contacting material stiffness. Higher contact stiffness prevents penetration improving model accuracy but it could cause model convergence issue. During the model setup it has been searched for a contact stiffness which has be a trade-off between accuracy and model stability.

According to their brittle behavior, dielectric layers (IMD and PMD) and silicon have been modeled as linear elastic material. The flow mechanical curve of AlCu alloy has been experimentally measured by dedicated nanoindentation test with constant strain rate and using a spherical indenter. These tests have been employed on samples made by AlCu metal film deposited on a blanket silicon substrate. It has been considered a post-process procedure that allows to convert the hardness data at different strain into stress-strain flow curve.[20] According to Tabor relation, indentation hardness H and stress σ are correlated by the constraint factor C^* which depends on strain and on the ratio between indentation reduced modulus E_r and stress.[21] Comparing nanoindentation with uniaxial test, constraint factor has been expressed as function of coefficient μ which represents the ratio between contact stiffness S and the slope of the load/contact depth curve.[20] According to this methodology, AlCu mechanical flow curve has been measured at $0.03\,s^{-1}$ as shown in Figure 9.

The materials properties used for the simulation have been reported in Table 1. From the table it could be observed diamond is much stiffer than other materials. Flat punch tip behaves as an almost perfect rigid body during the simulation. Considering

the experimental evidence of oxide brittle failure, the calculated maximum principal stress has been used, in accordance with literature,[14] as failure criteria to predict and benchmark the crack initiation.

Pad A and B simulation results and experimental correlation

Target of numerical model has been the analysis of the stress distribution inside the oxide layers. A nanoindentation curve up to 75 mN of maximum load has been virtually reproduced. Figure 10 compares the calculated nanoindentation curve with the experimental one. An overview of the maximum principal stress inside the whole pad has been pictured in Figure 11, highlighting IMD2 is the most stressed layer. According to the entire pad behavior, it has been focused the stress distribution inside the IMD2, as depicted in Figure 12. In this picture, the maximum principal stress has been plotted looking to the top and bottom IMD2 side, considering both pad A and B. Stress in pad A reaches 800 MPa on the top side and 1200 MPa on the bottom side. In pad B, higher stress has been pointed out in the IMD2 top side (1500 MPa).

Performed analysis has underlined stress is higher in pad B than in pad A, presenting the maximum value on the top side near the vias.

The interpretation of this behavior is that the tungsten vias represent a notch for stress distribution in dielectric layer. Due to the high induced stress, interfaces between vias and IMD are the most probable locations where cracks can initiate. This observation is in accordance with the results found by Liu et al.,[16] already discussed in section 1, which has

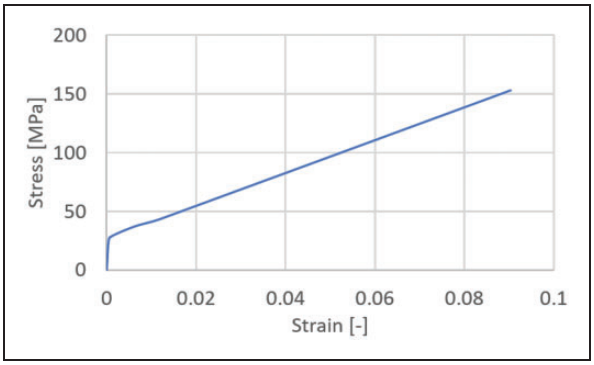

Figure 9. Mechanical flow curve for AlCu alloy extracted from nanoindentation test at strain rate of 0.03 s^{-1}.

Table 1. Material properties considered for mechanical FE simulation.

Part	Compound	E [GPa]	ν
Indenter Tip	Diamond	1141	0.07
Metalization	AlCu	70	0.33
Inter Metal Dielectric	TEOS	81	0.25
Vias	Tungsten	411	0.28
Pre Metal Dielectric	BPSG	61.5	0.17
Substrate	Silicon	169	0.23

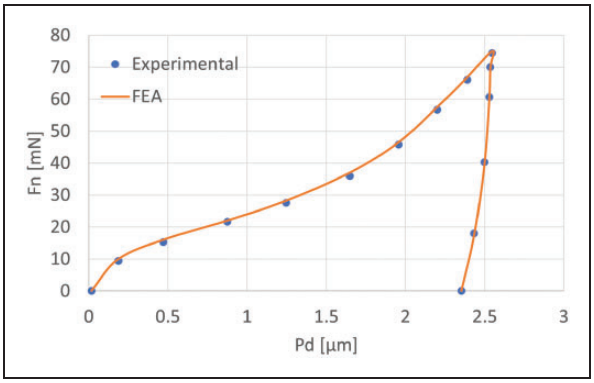

Figure 10. Nanoindentation simulated curve compared with experimental result.

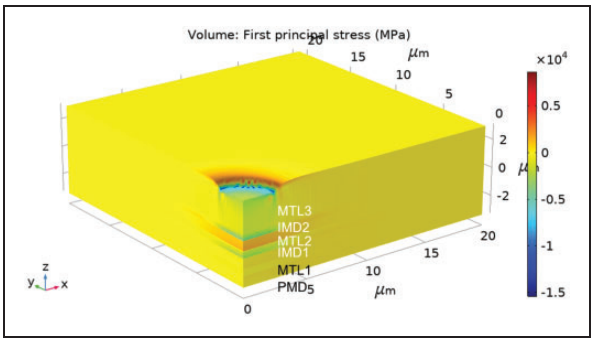

Figure 11. First principal stress inside the whole pad structure From the picture it could be observed IMD 2 is the most stressed brittle layer.

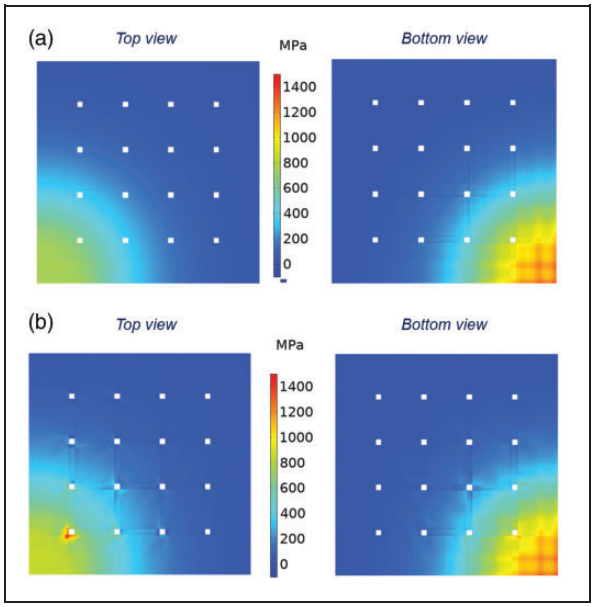

Figure 12. Maximum principal stress inside IMD2 layer and benchmark between pad A (on the left) and B (on the right). (a) Pad A. (b) Pad B.

forecast tungsten vias increases mechanical stress in intermetal dielectric layer.

From this consideration, it has been expected crack starts to propagate near tungsten vias in pad B IMD2 layer. The failure analysis reported in Figure 7 is aligned with simulation results: a sign of crack initiation is visible only in the IMD2 of pad B option, close to tungsten vias. As validated by experiments and according to literature wire bonding simulation,[16] tungsten plugs induce a notch effect with consequent stress concentration. The proposed nanoindentation results have been in accordance with some literature findings about wire bonding process. IMD layers have been highlighted as the weakest structure of pad layout by numerical model[14] and process characterization.[3] The mentioned correlation with literature outcomes enforces the proposed methodology which would experimentally reproduce the mechanical stress induced by wire bonding process. Nanoindentation allows to replicate the mixed energetic and the thermo-mechanical condition of wire bonding process with the advantage of a controlled load in terms of energy, displacement or force. In order to complete the analysis, maximum principal stress component has been studied along the IMD1, as depicted in Figure 13. As already observed in Figure 11, IMD1 layer is much less stressed than IMD2. Reached maximum in IMD1 is lower than 150 MPa as reported in the graph and it is similar in both pad options.

Additional pad options

Once numerical model has been validated by experiments, two more different stack layouts have been evaluated using simulation tool. Pad C does not take into account the MTL2 layer having a thicker dielectric, resulting stiffer and less prone to crack oxide. Pad D represents a trade-off between pad A and pad C: thicker and thinner oxide with vias coexist and they are interleaved in the same layout. Layouts C and D have been depicted in Figure 14.

Figure 15 shows the stress calculated in the top side of IMD2 for the new pads. These new layouts show good performances under compressive quasi-static loads such as the nanoindentation, as depicted in Figure 15. Maximum stress is around 300 MPa in pad C and 500 MPa in pad D. However, as the dielectric gets thicker, the stack becomes more sensitive to transversal and localized loads. This could affect the overall performances of the pad under the wire

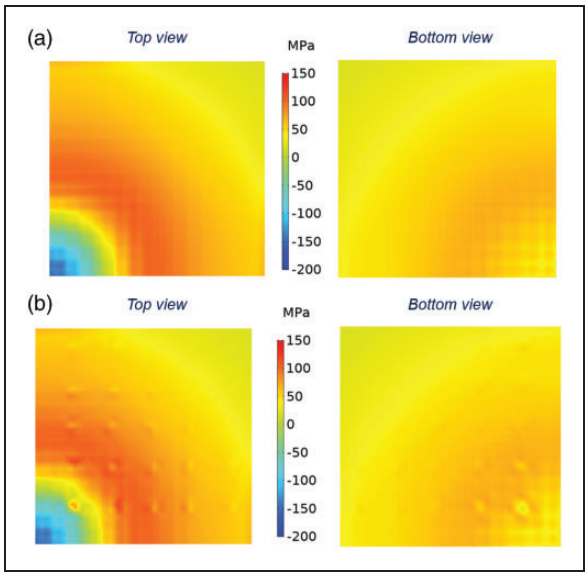

Figure 13. Maximum principal stress inside IMD1 layer and benchmark between pad A (on the left) and B (on the right). (a) Pad A. (b) Pad B.

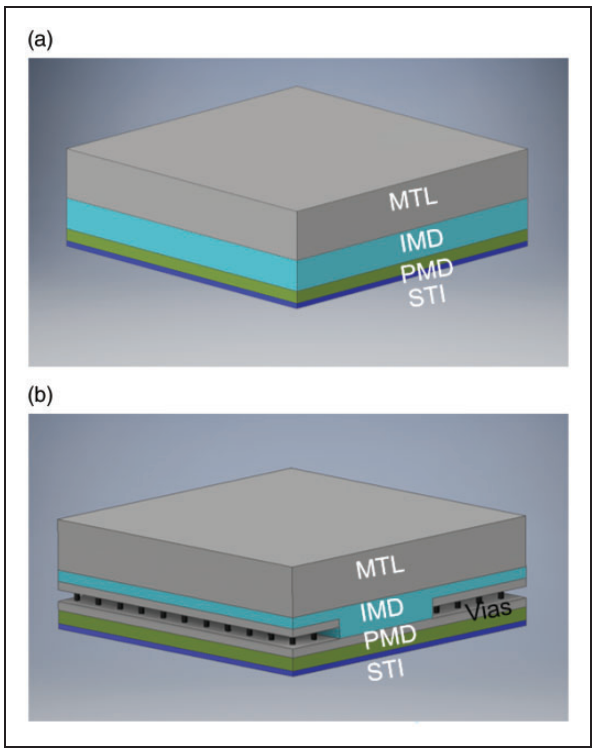

Figure 14. Pad stacks 3D CAD-models used for the comparison, in which IMD layers (in cyan) have been hidden if there are vias inside. Pad C has a thick dielectric without any tungsten vias. In pad D, there is a succession of thick dielectric and thinner IMD layer with vias. (a) Pad A. (b) Pad B.

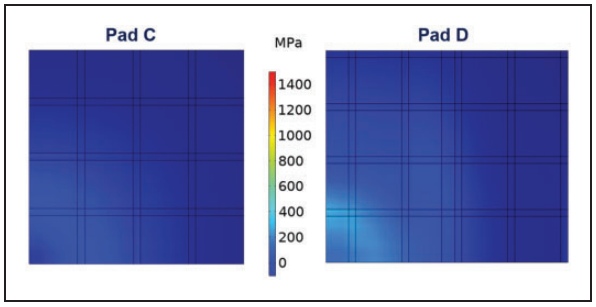

Figure 15. Stress results in the front side of IMD2 for pad C and D options.

bonding: a verification of the expected behavior during wire bonding should be performed by a 3D Finite Element Model. Furthermore, it could be considered that pad C and D have a reduced number of metal's layers (one and two, respectively). It has a detrimental effect on the layout capability of new pad structures: it has been evaluated if a such downgrade is feasible to improve reliability performances.

Conclusions

In the presented activity, a mechanical assessment in terms of pad structural mechanical strength has been performed benchmarking different design options. A mixed experimental and numerical method has carried out. Different test samples have been tested by means of nanoindentation at different maximum load. In order to study and detect the pad mechanical failure, SEM analysis has been performed on cross section samples prepared by FIB. Numerical model has been developed to reproduce the experimental nanoindentation test and to analyze the stress distribution in brittle oxide layers. Both experimental and numerical analyses have shown pad A is less stressed than pad B due to the notch effect induced by tungsten vias in the top inter metal dielectric layer. According to the developed Finite Element approach, two additional pad layouts, with thicker oxide (pad C) and interleaved structure (pad D), have been virtually mechanically assessed. In these optimized options, stress on brittle layers has been drastically reduced in comparison with original pad B option. The proposed methodology has allowed to quickly benchmark between different pad design in terms of mechanical strength providing a robust method, which helps the device design to set *ab-initio* the proper pad structure, shorting the needed time-to-market and reducing the experimental effort. Furthermore, it helps to improve the device lifetime and its compatibility with mechanical impacting assembly process. Future works could be addressed to characterize the adhesion properties inside the pad structure by nanoscracth test at different temperature and strain rate.

Declaration of Conflicting Interests

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ORCID iD

Michele Calabretta https://orcid.org/0000-0001-9322-182X

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