Realization of a fractional-order RLC circuit via constant phase element

Riccardo Caponetto¹ · Salvatore Graziani¹ · Emanuele Murgano¹

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Abstract

In the paper, a fractional-order RLC circuit is presented. The circuit is realized by using a fractional-order capacitor. This is realized by using carbon black dispersed in a polymeric matrix. Simulation results are compared with the experimental data, confirming the suitability of applying this new device in the circuital implementation of fractional-order systems.

Keywords Fractional-Order Calculus · Constant-Phase Element · Analog fractional-order RLC circuit · Carbon-black-based device

1 Introduction

Fractional-Order Calculus (FOC) has been investigated for centuries by mathematicians and physicians. Only in the last thirty years, engineers have been able to envisage and finally exploit fractional-order calculus potentialities, so that, nowadays, it is applied in many research areas; from automatic control in [25–27,30], to medical applications in [22,39], from time series and long memory effects modelling [17,33,41], to economics [19] as well as in civil engineer applications [4]. For a comprehensive state of the art related to FOC applications see [36].

Inside the FOC framework, the realization of electronics devices whose behavior is described by means of FOC has aroused particular interest in the researchers. These elements can be defined as Fractional-Order Elements (FOEs). Furthermore, among the FOEs, a particular cluster is deeply investigated due to its unique properties: the Constant-Phase Elements (CPEs). Theoretically, a CPE has a constant phase in all the frequency range and, hence, can be thought as a generalization of the commercial capacitor or inductor.

The first CPE, called Fractor, was patented by Bohannan, see [8], and in [7] it has been applied in motor control appli-

 Riccardo Caponetto riccardo.caponetto@unict.it
 Salvatore Graziani salvatore.graziani@unict.it
 Emanuele Murgano emanuele.murgano@unict.it

¹ DIEEI, University of Catania, Viale A. Doria 6, 95125 Catania, Italy



Different technologies have been developed, which can be classified as: multi-components and single components [35]. Heavised introduced the possibility to model the input impedance of transmission lines by using half-order capacitors [16]. That work triggered the interest of FOEs multicomponent realizations. More specifically, multi-component realizations are obtained thanks to RC-based networks. Passive RC components and Op-Amps-based circuit are exploited for realizing different types of networks (such as infinite, semi-infinite, domino or nested) [31]. The above mentioned approach requires a large number of electronics devices. The number and size of the involved components represent a bottleneck for their application in micro- or nano-electronics. Many technologies have been proposed for the realization of single-component FOEs. Among possible implementations, the possibility of mimicking the fractal geometry of many natural processes and living organisms has been exploited. In [21], the influence of the electrical parameters on the input impedance of a fractal structure realized on silicon is presented. Electrochemical FOEs have been proposed [5]. FOEs, in this class, exploit generally the porous structure of suitable polymeric materials. Solid-state FOEs are currently the most widely investigated technology. They can be classified as follows: graphene-polymer dielectric [18], carbon black-polymer dielectric [11] and MoS2-polymer composites [3]. Finally, the use of CNTs, see [1], introduced a new family of FOEs. CNTs are dispersed in a polymeric matrix and, as result, a dispersive resistive-



capacitive network is obtained, which can be modeled by using RC ladder structures.

In [12,13] the authors introduced and characterized a CPE based on Ionic Polimeric Metal Composites. In the papers a simplified model of a IPMC has been presented a possible realization of CPE. In particular the fractional-order feature of the device has been related with the platinum absorption time, that represent a technological parameter for the CPE realization.

In [24], it has been experimentally proved that the MWCNT (MultiWall Carbon NanoTubes) can be used to realize fractional capacitors, $(0 < \alpha < 1)$. The CPE devices have been realized using two copper plates as electrodes of dimension $1.5 \times 1.5 cm^2$ and in between a dielectric made up of a mixture of MWCNT and epoxy to separate the electrodes. Inside the electrode, another copper plate of dimension $1 \times 1 cm^2$ is placed.

In [2] poly (vinylidene fluoride)-based polymers and their blends are used to fabricate electrostatic fractional-order capacitors. Thissimplebut effective method allows toprecisely tune the constant phase angle of the resulting fractional-order capacitor by changing the blend composition.

All the above list CPE have been realized using materials that possess an intrinsic fractional-order nature. However, in all the different technological realization of CPEs, they have a constant phase only in a limited frequency range, A great challenge is to realize CPEs with a constant phase in a wide frequency domain. Besides, it must be pointed out that using classical CMOS technology it is possible to design and realize effective fractional-order capacitors, see [38].

A possible application of such a device can be represented by the realization of analog filters. Exploiting a CPE, it is possible to add more constraints due to more degree of freedom related to the fractional-order of the active elements. Among the possible filters, particular interest has been addressed to RLC circuits.

More specifically, fractional-order RLC circuits have been described and analyzed in literature. In the pioneering work, [20], an analytical study of the circuit is given in terms of the Mittag-Leffler function, depending on the order γ of the fractional differential equation. The paper introduces an auxiliary parameter that represents the fractional time components in the system, components that show an intermediate behavior between a conservative and dissipative system. In [32], the authors introduce some generalized fundamentals for fractional-order $RL_{\beta}C_{\alpha}$ circuits, as well as a gradientbased optimization technique in the frequency domain. The concepts introduced in the paper have been verified by analytical, numerical, and PSpice simulations. In [34], the conditions for checking the realizability of fractional-order impedance functions by passive networks, composed of a fractional element (either a fractional capacitor or a fractional inductor) and some RLC components, are presented. Necessary and sufficient conditions are given on a fractional-order impedance function to be realized by a passive network composed of a fractional element and RLC components. In [40], the analysis of phase and magnitude resonance conditions for a series RLC circuit is considered. The peculiarity of the papers consists of considering a supercapacitor as a circuit component. In the paper described above, the RLC system is either solved in analytical form or implemented and studied by using a finite order approximation. None of the described papers uses devices with intrinsic fractional order nature in the realization of the fractional-order RLC circuit. On the contrary proposed circuits are realized by using either digital or analog approximations the fractional-order elements.

The authors have already investigated the possibility of using CPE devices for the realization of fractional order circuits. In [9] a first-order fractional RC circuit has been introduced, while in [10], starting from state-space description, fractional-order Wien oscillator has been described.

In this paper, a new CPE, whose technological realization is described in [6,11], is applied for realizing a fractionalorder RLC circuit. To the best of authors knowledge this is the first reported case of a fraction RLC circuit realized by using a device with inherent fractional nature. Simulation results, compared with the experimental data, confirm the possibility to apply this new device in real circuits. In particular, the paper is structured as follows: Sect. 2 gives an overview on the fractional-order calculus and on the ideal fractionalorder RLC circuit; Sect. 3 shows and analyses the obtained experimental results while in Sect. 4 conclusions are drawn.

2 Methods

In this section, a brief overview on the fractional-order calculus and a detailed analysis on the ideal fractional-order RLC circuit will be given.

2.1 Fractional-order calculus

Fractional-Order Calculus can be considered as a generalization of the commonly used integer-order one [28]. Thought integer-order derivatives and integral of a function are common concepts, it is possible to compute derivatives of non-integer-order, e.g. 0.7, as well as non-integer integrals, e.g. of order 0.2 of a function. Fractional calculus allows to manage these concepts. The non integer order operator ${}_{a}\mathcal{D}_{t}^{\alpha}$ with a, t, and $\alpha \in \mathbb{R}$ is defined as follows:

$${}_{a}\mathcal{D}_{t}^{\alpha} = \begin{cases} \frac{d^{\alpha}}{dt^{\alpha}} & : \alpha > 0\\ 1 & : \alpha = 0\\ \int_{a}^{t} (d\tau)^{-\alpha} : \alpha < 0 \end{cases}$$
(1)

Three different definitions can be used to compute the previous operators [28]: in the continuous-time domain, the

Riemann-Liouville (RL) and Caputo (Cp) definitions can be used, while in the discrete case, the Grunwald-Letnikov (GL) one.

Contextually, FOSs can be described also in the Laplace domain. For example, a fractional-order integrator is described by the following transfer function:

$$I_m(s) = \frac{1}{s^{\alpha}} \tag{2}$$

with $\alpha \in \Re$. The realization of such an integrator as a single electronic component is one of the most active research fields in these years: for this reason, in the past, many scientists proposed several and different approaches to emulate and approximate this behavior utilizing integer-order components in a specified frequency domain [29,42].

In control system theory, particular interest is devoted to the implementation of the integrator in (2). Three possible approaches can be adopted. The first is based on the digital implementation, that after the mapping from the *s* to *z* domain, concludes in applying the difference equation methods. This is the case when microcontrollers or specific DSPs are used for the implementation, see [15]. The second approach is based on the design of integrated circuits using standard technology, such CMOS, see for example [14,38]. The third approach, the one proposed here, is based on the realization of new electronic devices whose constituting material posses intrinsic fractional-order nature.

In general, considering a fractional-order device, if the angular frequency ω is used, its impedance in the Laplace domain can be obtained as follows:

$$F(j\omega) = \frac{K}{(j\omega)^{\alpha}} \tag{3}$$

being *K* the gain of the impedance and α the fractionalorder of the impedance. From (3) both module and phase can be evaluated and are $|F(j\omega)| = K/\omega^{\alpha}$ and $\angle (F(j\omega)) = -\alpha \cdot \pi/2$. The phase for common resistors, capacitors and inductors are 0, $-\pi/2$ and $\pi/2$, respectively.

Eq. (3) suggests that depending on the value of α different behaviors can be modeled. Note that if $\alpha \in \mathbb{R}$, an arbitrary constant phase is obtained and these devices can be defined as Constant Phase Elements.

2.2 The fractional-order RLC circuit model

The general schematic of a RLC series circuit is shown in Fig. 1. If $\alpha = \beta = 1$, the standard RLC circuit is obtained.

By applying the Kirchhoff's Voltage Law, considering also that $i(t) = C \frac{dV_c}{dt}$, the following expression holds:

$$LC\frac{d^2V_c(t)}{dt^2} + RC\frac{dV_c(t)}{dt} + V_c(t) - V_{in}(t) = 0$$
(4)



Fig. 1 Fractional-order RLC series schematics

On the other hand, if a general fractional-order RLC circuit is considered, the equation requires some adjustments because the fractional-orders of inductor and capacitor must be considered according to their analytical expressions, respectively,

$$V_L(t) = L \frac{d^\beta i(t)}{dt^\beta}, \quad i(t) = C \frac{d^\alpha V_c(t)}{dt^\alpha}$$
(5)

So, Eq. (4) can be rearranged as:

$$LC\frac{d^{\beta}}{dt^{\beta}}\left(\frac{d^{\alpha}V_{c}(t)}{dt^{\alpha}}\right) + RC\frac{d^{\alpha}V_{c}(t)}{dt^{\alpha}} + V_{c}(t) - V_{in}(t) = 06$$

and considering the chain-rule for the fractional-order derivatives, i.e. $\mathcal{D}^{\alpha} \left[\mathcal{D}^{\beta} f(t) \right] = \mathcal{D}^{\alpha+\beta} f(t)$:

$$LC\frac{d^{\alpha+\beta}V_c(t)}{dt^{\alpha+\beta}} + RC\frac{d^{\alpha}V_c(t)}{dt^{\alpha}} + V_c(t) - V_{in}(t) = 0$$
(7)

Exploiting the Laplace transform, it is possible to study the behavior of the fractional-order RLC circuit in the frequency domain,

$$LCs^{\alpha+\beta}V_c(t) + RCs^{\alpha}V_c(s) - V_{in}(s) = 0,$$
(8)

and therefore the transfer function of the circuit will be:

$$G(s) = \frac{V_c(s)}{V_{in}(s)} = \frac{1}{LCs^{\alpha+\beta} + RCs^{\alpha} + 1}$$
(9)

Another aspect to focus on is related to the natural pulsation ω_c of a RLC circuit. While for the traditional implementation of the circuit it can be calculated as:

$$\omega_c = \frac{1}{\sqrt{LC}},\tag{10}$$

in the case of a non-integer-order one the natural pulsation ω_c assumes, see [32], the following form:

$$\omega_c = \left(\frac{\sin\left(\frac{\alpha\pi}{2}\right)}{LC\sin\left(\frac{\beta\pi}{2}\right)}\right)^{\frac{1}{\alpha+\beta}} \tag{11}$$

Deringer

$$\frac{d^{\alpha} x_1(t)}{dt^{\alpha}} = x_2(t)$$

$$\frac{dx_2(t)}{dt} = -\frac{1}{LC} x_1(t) - \frac{R}{L} x_2(t) + \frac{1}{LC} v_{in}(t)$$
(12)

On the other hand, if the fractional-order RLC circuit is evaluated in the frequency domain, by imposing $s = j\omega$, in (9) the asymptotic phase lag can be evaluated as follows:

$$G(j\omega) = \frac{1}{LC \cdot (j\omega)^{\alpha+\beta} + RC \cdot (j\omega)^{\alpha} + 1} = \frac{N(j\omega)}{D(j\omega)} \to$$
(13)

$$\angle \left[G(j\omega) \right] = \angle N(j\omega) - \angle D(j\omega) = -\angle D(j\omega)$$

After some manipulations, the following expression is obtained:

$$\angle D(j\omega) =$$

$$= \arctan \frac{\omega^{\alpha} \left[LC\omega^{\beta} \sin\left((\alpha + \beta)\frac{\pi}{2}\right) + RC\sin\left(\alpha\frac{\pi}{2}\right) \right]}{LC\omega^{\alpha + \beta} \cos\left((\alpha + \beta)\frac{\pi}{2}\right) + RC\omega^{\alpha} \cos\left(\alpha\frac{\pi}{2}\right) + 1}$$
(14)

The asymptotic phase value, Φ_{as} , can be evaluated as:

$$\Phi_{as} = -\lim_{\omega \to +\infty} \angle D(j\omega) \tag{15}$$

Finally, the following expression can be obtained:

$$\mathcal{L}D(j\omega) = = \arctan \frac{\omega^{\alpha} \left[LC\omega^{\beta} \sin\left((\alpha+\beta)\frac{\pi}{2}\right) + RC\sin\left(\alpha\frac{\pi}{2}\right) \right]}{\omega^{\alpha} \left[LC\omega^{\beta} \cos\left((\alpha+\beta)\frac{\pi}{2}\right) + RC\cos\left(\alpha\frac{\pi}{2}\right) + \frac{1}{\omega^{\alpha}} \right]}$$
(16)

whose asymptotic value is:

$$\Phi_{as} = -\left(\alpha + \beta\right) \frac{\pi}{2} \tag{17}$$

Simulation analyses of the implemented circuit, represented as reported in (12), have been carried out exploiting the FOM-CON toolbox [37].

3 Experimental results and discussion

3.1 The CPE description

In [6,11], the authors demonstrated the possibility of realizing a CPE by using Carbon Black (CB) and a polymeric



Fig. 2 CB-based CPE device

matrix. More specifically, devices were realized using Sylgard, as the polymeric matrix, and CB as a dispersed filler. Nanostructured devices, named in the following CB-FOEs, were obtained. The CB-FOEs were fabricated by mixing the PDMS and a crosslinking agent, in a weight ratio of 1 : 10, in a Teflon crucible. Sylgard was purchased from DowCorning as a two part liquid elastomer kit. Part A (consisting in the vinyl-terminated PDMS prepolymer) was mixed with Part B (the crosslinking curing agent, consisting in a mixture of methylhydrosiloxane copolymer chains with a Pt catalyst and an inhibitor). CB (acetylene, 100% compressed, 99.9+%, specific area $75 m^2/g$, bulk density $170 \div 230 g/L$, average particle size $0.042 \mu m$) was purchased from AlfaAesar and used as received.

The mixture was mixed for 10 *min*. CB has been added for achieving the desired concentration. The mixture was stirred for further 10 *min*, for enhancing the dispersion of the CB.

Curing at different temperatures was carried out, taking into account both the manufacturer recommended curing time and the heat propagation through the mold. This resulted in a stabilization time, required for the temperature of the curing PDMS approaching the desired curing temperature. The mixture was used for realizing the dielectric of the capacitors by pouring the viscous mixture into copper-made electrodes. The mixture was allowed crosslinking at room temperature, or in an oven preheated to the desired temperature, for 48 *h*. More specifically cylindrical capacitors, whose geometry is shown in Fig. 2, were realized.

The capacitor considered in the following has height $h = 8 \ cm$, internal diameter $a = 0.6 \ cm$ and the external one $b = 1.2 \ cm$.

A detailed description of the realization procedure for the aforementioned device is given in [6].

The results reported in [6,11] allows to foresee a dependence of the order α from the curing temperature and, therefore, the possibility of controlling, by design, the of noninteger coefficient. In particular, among the different curing temperature values and percentages of CB diffused inside the dielectrics, in this paper the CPE obtained with a curing temperature of 130° *C* and a CB percentage equal to 2 % has been taken into account.



Fig. 3 Bode diagram of the CB-FOE



Fig. 4 Bode diagrams of the C130B and the identified model

In Fig. 3, the Bode diagram of the impedance of the considered FOE is reported. The diagram has been obtained by using a spectrum analyzer Keysight Technologies E5061B.

Looking at the frequency range [1, 1000] kHz, both the slope of the magnitude diagram and the value of the phase lag give evidence of the fractional nature of the device.

An identification procedure has been performed, in the frequency range mentioned above, to model the capacitor as (3). The following values, $C = 2.2 n F/s^{1-\alpha}$ and $\alpha = 0.82$,

have been obtained, see Fig. 4. They will be used in the following of the paper.

It is possible to argue that at the very low frequencies (lower than 5Hz) resistive behaviors prevail. This is probably due to leakage resistances and, hence, the proposed device does not act as a CPE for frequencies lower than 1 k Hz. Moreover, in the investigated frequency range, the phase variation in the flat area is about $\sim \pm 5 deg$. It was not possible to



Fig. 5 Fractional-order RLC circuit implementation

investigate frequencies larger than those reported in Fig. 3, because of instrument limitations.

Tough devices obtained with the described technology have been used for years, no significant changes have observed in their electrical characteristics, giving evidence of stability.

A fractional-order RLC series circuit was realized by using the CB-FOE device. Commercial inductor,(i.e., with $\beta = 1$), and resistance were used for the circuit realization. The circuit, shown in Fig. 5, has been realized with a resistor $R = 1 k\Omega$, an inductor with a nominal value L = 47 mH and $\beta = 1$, and the aforementioned CB - FOE fractional-order capacitor with $C = 2.2 nF/s^{1-\alpha}$ and $\alpha = 0.82$.

3.2 The FO-RLC model identification

An ideal FO-RLC circuit of Fig. 1 has been proposed as model for the real circuit depicted in Fig. 5, without considering any parasitic effects. The Bode diagrams of the real circuit and the proposed nominal model, obtained by exploiting the parameters defined before, are shown in Fig. 6.

Table 1Parameters of theinductor EECM	Parameter	Value
	R _{par}	15.874 $G\Omega$
	C_{par}	12.707 pF
	R_s	$0.459 \ k\Omega$
	L_{real}	39.8 mH

As it is possible to notice, the nominal model is not able to fit the real response of the circuit. Further investigations on each components have been performed in order to build a more reliable model.

3.3 The FO-RLC complete model identification

The other two components of the circuit (i.e. resistor and inductor) have been deeply analyzed in order to consider any parasitic effects (if present) or to use more accurate real value of their impedances.

Firstly, the response of the resistance R has been measured with a digital multimeter and it is equal to $R_{real} = 997.6 \ \Omega$.

In order to deal with the parasitic components of the inductor, an Equivalent Electric Circuit Model (EECM) has been identified. The schematic of the EECM is reported in Fig. 7, while in Table 1 parameters of the model are reported.

The identified frequency response of the inductor is compared with experimental measurements in Fig. 8. From the dot-marked line, it is quite evident the presence of a resonance peak, at about 250 kHz, due to inductor parasitic components.

The global fractional-order RLC circuit has been obtained by the series connection of the resistance R_{real} , the capacitance C^{α} and the ECCM of the inductor.

Figure 9 shows the comparison between the frequency response of the fractional-order RLC circuit model with that of the real circuit, highlighting a well-performed identifica-







Fig. 7 Inductor EECM

tion procedure that allows to model the real behavior of the system under investigation.

Fig. 8 Bode diagrams of the inductor and its EECM

3.4 Discussion and model validation

Looking at Fig. 9, it is possible to notice that the FO-RLC circuit, as expected, has a resonant peak. This occurs at about 50 kHz. The parasitic effects produce an undesired anti-resonant like effect at 250 kHz. Such parasitic effects are responsible for discrepancies that can be observed in the high-frequency range for both the module and the phase graphs shown in Fig. 6.

Based on such consideration, further investigation are limited up to 100 kHz. More specifically, three different sinusoidal tones, the first one at 10 kHz, the second one at 50 kHz and the last at 100 kHz, have been chosen as forcing inputs to the circuit. The first tone was intended for investigating the behavior of the circuit at low frequencies, the second one to evaluate the response in the neighborhood of the resonance frequency, while the third tone was used for investigating the circuit at frequencies higher than the circuit resonance frequency. Both the model simulation and



Fig. 9 Bode diagrams of the real FO-RLC circuit and the real equivalent model







Fig. 12 Sinusoidal input @ 100 *kHz*

8.289 deg

Frequency

51.286 kHz

63.648 kHz

Table 2 Maximum deviation values		
Deviation	Value	
Module	1.704 <i>dB</i>	

Phase

the experimental investigation of the fractional-order RLC circuit, at these three tones, will shown in the following.

The acquired responses and the corresponding model simulations are shown in Figs. 10, 11 and 12. It is possible to notice that, at both the lowest and the highest considered frequency values, the model simulations are in agreement with the experimental results, while, at 50 kHz the amplitude of the real circuit output is higher than the simulated one. This discrepancy is due to a imperfect fit between real and equivalent model. Looking at Fig. 9, in correspondence of $f = 50 \ kHz$, a module difference of almost 2 dB can be detected and such a difference justifies the variation of about 0.2 V.

This variation is further confirmed by the error values for the Bode diagrams in the interval [1, 100] kHz. The obtained values, along with the corresponding frequency values, are reported in the Table 2. Frequencies close to the circuit resonance frequency are obtained. Finally, the real Bode diagram allows to validate the identified order α of the fractional-order capacitor because the circuit asymptotic value is almost equal to the one of the simulated model.

In Table 3 different parameters characterizing the Bode diagrams, the sinusoidal, and step responses have been evaluated for the real and simulated fractional-order RLC circuit respectively. The values obtained for the corresponding integer order RLC circuit (i.e., same R, L and C values, and $\alpha = 1$) are also reported in the table for the sake of comparison.

The step response has been also investigated, see Fig. 13. Although the pseudo-periods of the oscillation, both for the real and the simulated responses, do not show relevant differences, the simulated response is more dumped than the real one: this phenomenon is justified by analyzing the Bode diagram of Fig. 9, where, in correspondence of the peak resonance, the real module is slightly higher than the simulated one.

The values presented in the table outline the dependence of the non-integer-order RLC parameters on the non-integerorder value α . In the following, evidence will be given of the role of the fractional nature of the capacitor in the obtained circuits behavior. More specifically, the investigation will be performed for the case of the high frequency phase lag. In this investigation the parasitic effects of the inductor are neglected. The following notation has been adopted: *IO* indicates the integer-order RLC circuit, *FO-S* is used for the simulated fractional-order RLC circuit, and *FO-R* for the real fractional-order RLC circuit.

More specifically, for $\alpha = 0.82$ the corresponding asymptotic value, estimated according to 17, is -163.8 deg. The values reported in Table 3 are in agreement with the analytical estimation.

Results obtained during the model identification and validation show that the adopted linear model is a good approximation of the device real behavior for the investigated working condition.

4 Conclusions

In this paper a fractional-order RLC^{α} circuit, realized by using a CPE constructed with a CB nanostructured dielectrics, has been introduced. To the best of the authors' knowledge, it is the first realization of fractional-order RLC

Estimated for Bode diagram (Fig. 9)	ΙΟ	FO-S	FO-R
Resonance peak	10.1 <i>dB</i>	8.4 <i>dB</i>	9.9 <i>d</i> B
Resonance frequency	15.2 <i>kHz</i>	46.7 <i>kHz</i>	51.3 <i>kHz</i>
Module slope	-40 dB/dec	$\tilde{-}38 dB/dec$	//
Phase value	-180 deg	-163.8 deg	-163 deg
Sine response (Figs. 10 and 12)			
Amplitude peak-to-peak @ 10 kHz	1.462 V	0.975 V	1 V
Amplitude peak-to-peak @ 50 kHz	0.122 V	2.195 V	2.64 V
Amplitude peak-to-peak @ 100 kHz	0.024 V	0.313 V	0.3 V
Step response (Fig. 13)			
Rise time	$1.128 \cdot 10^{-5} s$	$4.3 \cdot 10^{-6} s$	$4.3 \cdot 10^{-5} s$
98% Settling time	$2.138 \cdot 10^{-4} s$	$1.032 \cdot 10^{-4} s$	$1.104 \cdot 10^{-4} s$
Overshoot	58%	37%	50%

Table 3Parameters fordifferent responses

Fig. 13 Step response



circuit employing a real CPEs as a fractional capacitor. The circuit has been investigated in the frequency domain [1, 1000] kHz. Two models have been proposed and the validation of the models both in time and frequency domain is given. Evidence is given about the possibility of accurately modeling the fractional-order RLC circuit. Reported results show that new behavior can be obtained because of the fractional nature of the capacitor. Finally, further studies are required to fully characterize the dependence of the FOE from environmental quantities, such as temperature and humidity. The obtained results are encouraging and let foresee a possible application of these devices in analog fractional-order circuits.

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