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A Memory-Targeted Dynamic Reconfigurable Charge Pump to Achieve a Power Consumption Reduction in IoT Nodes

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ABSTRACT Targeting the more recently adopted low-power memories for data-logging operation in IoT nodes, this paper presents a simple reconfigurable dual-branch cross-coupled charge pump (CP) topology in which clock amplitude scaling and modulation of the number of stages are exploited to improve power efficiency and/or change the output voltage without degrading speed performance. The proposed solution allows a reduction of the power conversion losses, maintaining speed, maximum output voltage and silicon area unaltered as compared to the conventional charge pump. Post-layout simulation results confirm the effectiveness of the proposed topology which can be adapted to any other kind of linear charge pump.

INDEX TERMS DC-DC converter, Dickson Charge Pumps, power management for solid-state memories, ultra-low power.

I. INTRODUCTION

Recently, Switched-Capacitor DC-DC step-up converters, also known as Charge Pumps (CPs), are finding use in an ever-increasing number of integrated microelectronic systems when power supply voltage level needs to be boosted. Thanks to their fully-integrable schemes, CPs are often exploited in monolithically implemented solutions and are applied in a wide field of applications ranging from non-volatile memories, implantable devices and energy-autonomous sensor nodes for the Internet of Things (IoT) [1]–[9].

Focusing on these latter applications, distributed nodes should allow robust data-logging, while preserving long-term system life. For this purpose, low voltage and low power architectures for storage banks are exploited. Nevertheless, such circuits barely work with a supply voltage lesser than 1 V and show poor speed performance. In the other hand, high voltage ensures operations into the adequate noise margin. Unfortunately, charge pump circuits used to provide such high voltage levels consume a lot of power, often deteriorating efficiency of the whole system.

Therefore, power efficiency and power consumption are two fundamental aspects on which the CP design considerations are often focused. In literature several papers dealt with this topic [10]–[12], and are mainly focused on the well-known Dickson CP (Fig.1) for its efficiency and advantages in an IC realization [13].

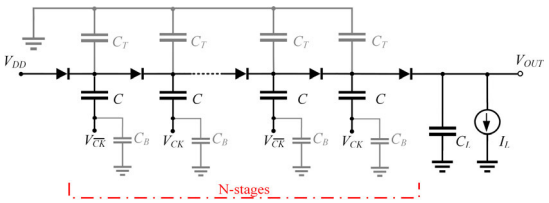

FIGURE 1. Schematic diagram of the conventional Dickson CP.

Considering, in particular, the Dickson CP power consumption, papers [10] and [11] report two optimized design strategies for power consumption reduction, taking into account the only bottom or both bottom and top plate parasite capacitances. On the other hand, in [12] authors explored the possibility to reduce power conversion losses by scaling the clock amplitude voltage, thus increasing the CPs number of stages to maintain the output voltage unaltered. Advantages of this strategy are also confirmed by the study reported in [14], which compares regulation schemes for CPs working in a wide range of clock frequency. Although this method allows to strongly reduce power consumption, the increase of CP settling time is a cost not often payable. As a typical example, flash memories require dual polarity or dual level

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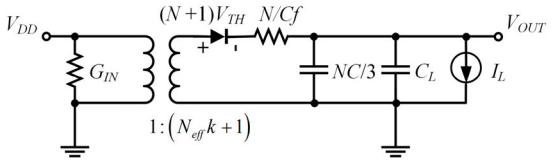

FIGURE 2. Equivalent model of a Dickson Charge Pump.

voltages, often higher in absolute value than the available power supply, for erasing and programming the data.

In this case, the CP speed (i.e., settling time) establishes the higher bound for the reading and writing operation velocity [15], [16]. Therefore, to get rid of these drawbacks, in this paper a simple but effective dynamic reconfigurable dual-branch cross-coupled CP topology, which include only few low-power auxiliary circuits and can exploits the power advantage due to a halved clock amplitude, is introduced. Starting from a CP topology that can work through 2×2 different states, the applied management scheme dynamically moves the CP through the two states: High-speed/High-power and the Low-speed/Low-power, thus permitting a fast start-up together with a power efficient operation at the nominal output voltage. The two additional states, also available, but not used in the considered application, should be used to achieve conditions with two different output voltages (doubled or halved respect to the nominal one).

This paper is organized as follows. In section II, the concept behind the solution is theoretically described and compared with the traditional topology, showing, in particular, its advantage when the load does not require high current levels. In section III, transistor-level implementation of the proposed topology is described in detail. A design example using a standard 65-nm CMOS technology is reported with post-layout simulation results which validate the topology in section IV. Finally, conclusions and future perspectives close the paper in Section V.

II. PRINCIPLE OF OPERATION

A. CHARGE PUMP MODELING

Let us consider the simplified schematic of a classical N-stage Dickson CP in Fig 1. Without loss of generality, the charge transfer device is assumed to be an ideal diode, but it can be any other type of device (e.g., a diode-connected or bootstrapped MOS transistor, a cross-coupled configuration, etc.) [2]. Each stage capacitor has a constant capacitance value, C, resulting from a uniform distribution along the stages of the total CP capacitance. In the block scheme in Fig. 1, for each stage capacitor the two parasitic contributions due to the bottom and top parasitic capacitances, $C_B = \alpha_B C$ and $C_T = \alpha_T C$, are also included, where the coefficients α_B and α_T are technological dependent parameters. The CP load is modelled with the terms C_L and I_L.

Assuming that the CP operates within Slow Switching Limits [19], where the charge from one stage to the other is assumed to be entirely transferred, during the steady-state we can model the CP by the equivalent circuit in Fig. 2.

In the model of Fig. 2, V_{OUT} and N/Cf represent the output voltage and the output impedance, respectively [12], being f the clock frequency, the input impedance, G_{IN}, models the power consumption due to continuous switching of the stray capacitances and its value is given by

$$G_{inf} = \alpha_B N C f k^2 V_{DD} \tag{1}$$

with k the ratio between the amplitude of the clock signal, V_{CK}, and the input voltage, V_{DD}, respectively. Concerning the transformer, it operates an ideal power conversion and the effective number of stages, N_{eff}, is expressed as

$$N_{eff} = \frac{N}{1+\alpha_T} \tag{2}$$

Neglecting second order leakages, like reverse losses or inverse saturation currents of the parasitic junctions, charge pump total power loss during on-state is given by

$$P_{LOSS} = (N+1)\, V_{TH} I_L + \frac{N I_L^2}{fC\,(1+\alpha_T)} + \alpha_B N C f\, (kV_{DD})^2 \tag{3}$$

B. CHARGE PUMP DESIGN CONSIDERATION

In order to reduce CP power loss, it can be noted from (3) that the product fC, which coincides with the stage admittance of a single stage CP, can be set to minimize the input power, thus maximizing power efficiency. As an example, Fig. 3a depicts power losses of a generic design as function of the stage admittance, fC. Its trend shows an absolute minimum expressed by

$$(fC)^* = \frac{I_L}{CkV_{DD}} \sqrt{\frac{1}{\alpha_B\,(1+\alpha_T)}} \tag{4}$$

By inspection of (4), it seems that the stage admittance and, hence, the minimum power loss, given by

$$P_{LOSS,\min} = (N+1)\, V_{TH} I_L + 2N \frac{I_L}{C} \sqrt{\frac{\alpha_B}{(1+\alpha_T)}} kV_{DD} \tag{5}$$

can be arbitrarily made as low as the output current decreases. On the other hand, the CP settling time, which is related to its time constant

$$\tau_S = \frac{N}{fC}\left(\frac{NC}{3} + C_L\right) \tag{6}$$

increases proportionally to the stage admittance.

Figure 3b reports the time constant as a function of the stage admittance and, in the same plot, the time constant vs. the ratio between the load capacitance and the CP equivalent capacitance for $fC = 10$ (nested graph). As it can be seen, when the admittance decreases the time constant and, therefore, the settling time increases suddenly. Such condition limits the effective choice for the product fC, thus a tread-off between speed and power consumption must be often pursued for the design of a charge pump.

Focusing on the IoT nodes which carry out the operation of data-logging, the design of the CP is mainly constrained

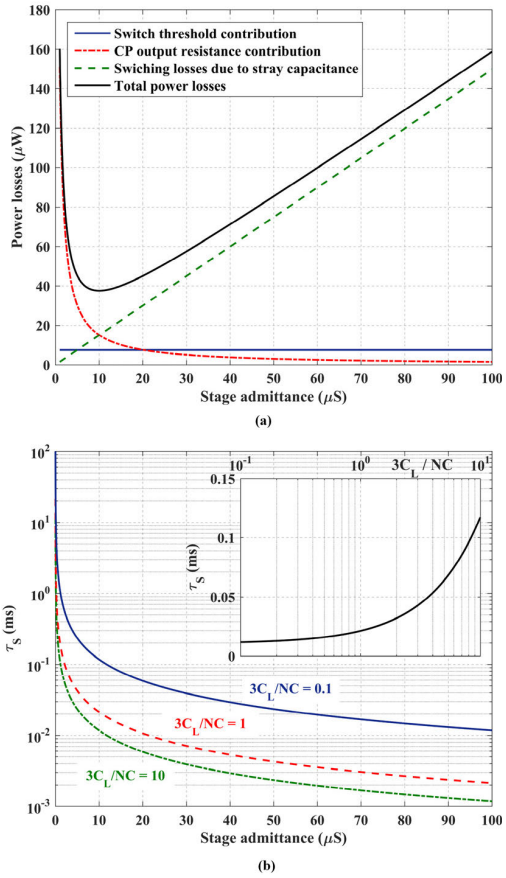

FIGURE 3. Power losses (a) and time constant (b) as function of the single stage admittance of a generic design.

by achieving a specific settling time, for example to guarantee the memory access time which respects the used protocol [15], [16], [18]. In such a case, the admittance has to be set to satisfy the speed constraints and, especially for recent low-power memories, switching losses due to stray capacitances prevail CP power consumption without the possibility to be minimized.

An original strategy to overcome the limit on the minimization of the CP power consumption can be pursued by using the analysis in [12], where it is shown how the same output voltage can be generated by two CPs with the same topology and same total pumping capacitance, C_{CP}, but different clock amplitude $V_{CK,1}$ and $V_{CK,2}$. In particular, we can write

$$N_1 V_{CK,1} - N_2 V_{CK,2} = (N_1 - N_2)\left[V_{TH} + (N_1 + N_2)\frac{I_L}{fC_{CP}}\right] \tag{7}$$

where N_1 and N_2 are the number of stages of the two CPs. Thus, remembering that for self-boosted switches, like bootstrapped-MOSFET and cross-couple configuration, threshold voltage is negligible and, since, as previously stated, low-power memories require fast access time while consume low current, therefore, (7) can be approximated with zero.

To compare the switching power losses for the two CPs with equal output voltage but different number of stages and clock amplitude, we can write

$$\frac{P_{LOSS,2}}{P_{LOSS,1}} = \frac{\alpha_B C_{CP} f \left(V_{CK,2}\right)^2}{\alpha_B C_{CP} f \left(V_{CK,1}\right)^2} = \left(\frac{V_{CK,2}}{V_{CK,1}}\right)^2 \approx \left(\frac{N_1}{N_2}\right)^2 \tag{8}$$

from which it is apparent that in a group of charge pumps the longest one (for instance the second if $N_2 > N_1$) has the best power performances, and this advantage shows a superlinear (squared) behavior. As a numerical example, assuming $N_2 = 2\,N_1$ the losses ratio is almost equal to 0.25, which means a significant 75% reduction on the power losses.

It is worth noting that the increase in the number of stages, however, results in a CP speed reduction. Indeed, from [16], defining T_S as the CP settling time, we get

$$\frac{T_{S,2}}{T_{S,1}} = \frac{\frac{N_2^2}{fC_{CP}}\left(\frac{C_{CP}}{3} + C_L\right)}{\frac{N_1^2}{fC_{CP}}\left(\frac{C_{CP}}{3} + C_L\right)} = \left(\frac{N_2}{N_1}\right)^2 \tag{9}$$

The ratio in (9) results to be independent by the output load capacitance, C_L. By its inspection, $T_{S,2}$ is four times higher than $T_{S,1}$, if $N_2 = 2\,N_1$. Thus, to get rid of this drawback, we propose a simple but effective topology which is based on a CP with a programmable number of stages, allowing to gain power efficiency without speed degradation.

III. THE PROPOSED DYNAMIC TOPOLOGY

Starting from the considerations discussed in the previous Section, in order to reduce the power losses of the charge pump without slowing down the transient response, it is proposed to dynamically change the number of stages and reducing the clock amplitude with the constraint to keep unchanged the steady-state output. In particular, during the start up a CP with the minimum number of stages has to be configured, while once the steady state is reached the CP is configured with a larger number of stages to minimize the power loss.

Note that the reduction of the clock frequency can be exploited to reduce power losses but since power losses are proportional to $NCf(V_{CK})^2$, reducing the clock amplitude represent a much more effective design strategy.

The simplified scheme of the proposed topology is reported in Fig. 4. It includes a Clock Amplitude Reducer (CKAR), whose scheme is shown in the left-most red dashed box, able to generate (under the control of the enable signal *CKAR_En*) a clock supply voltage, V_{CK}, equal to V_{DD} or to $0.5V_{DD}$. The CKAR signal feeds the buffers chain used to drive the pumping capacitors of the basic cross-coupled dual-branch CP topology, whose single stage is shown in the right-most red dashed [2], [19].

The general architecture is then completed by few auxiliary digital gates and MOS transistors (*Ma*, *Mb*), which allow to select the number of stages to include during the various system operations.

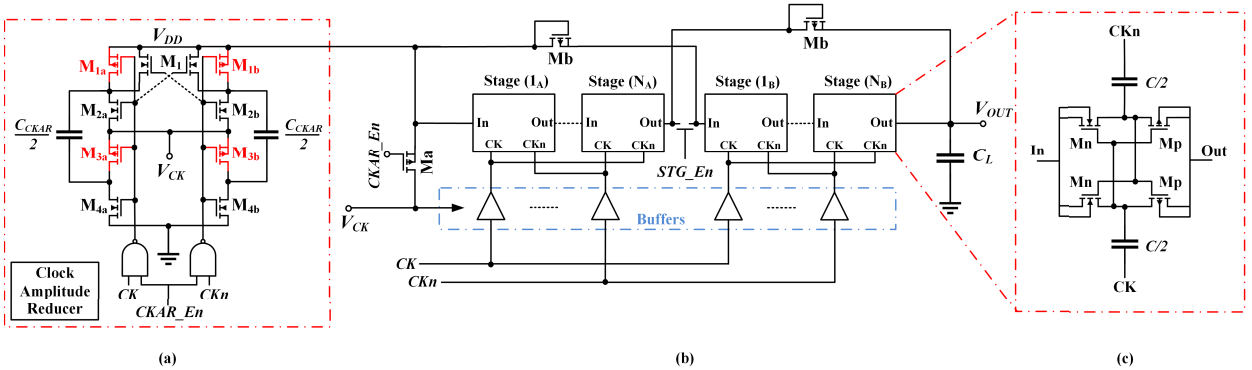

FIGURE 4. Simplified block diagram of the proposed architecture: clock amplitude reducer (a), charge pump (b), single stage topology(c).

Concerning the CKAR, the architecture is inspired by the DC-DC buck converter proposed by Grasso *at Al.* in [7]. In this scheme, red transistors are PMOS, whilst the others are NMOS transistors whose bodies are grounded. Since the two counter-phase clock signals are assumed to be always running, the working principle can be summarized in two different modes, depending on the state of the control signal *CKAR_En*: transparency (*CKAR_En* = "0") and reduction (*CKAR_En* = "1"). When the transparency mode occurs, only NMOS transistors conduct and the two pumping capacitors are connected in parallel to the supply, setting $V_{CK} = V_{DD}$. Otherwise, in reduction mode, capacitors distribute alternately the supply voltage, halving the output voltage. The used topology has the advantage to reduce the output voltage ripple, because the output node is refreshed with a doubled effective frequency.

According to (7), an increase of a factor 2 of the stage number, N, is applied, making the topology, through the control signals *STG_En* and *CKAR_En*, commutable in 2×2 different configurations briefly summarized in Table 1. In particular, the stage enable signal, *STG_En*, forces the CP to work with either a halved number of stages (*STG_En* = "0") or all the stages (*STG_En* = "1"). The *CKAR_En*, instead, allows to enable/disable the CKAR. It is apparent that in our proposed topology, only two configurations are used, the one with *STG_En* = "0" and *CKAR_En* = "0" for the start-up phase and the one with *STG_En* = "1" and *CKAR_En* = "1" in steady state. While the other two configurations (i.e., *STG_En* = "0" - *CKAR_En* = "1" and *STG_En* = "1" - *CKAR_En* = "1") are not used.

By inspection of (8) and (9), a reduction of the power consumption can be achieved without loss in the speed if the CP is started from the state "00" and, once the steady state is reached, commutated into the state "11".

Note that since the maximum output voltage is given by

$$V_{OUT} = N_{eff} V_{CK} + V_{DD} \tag{10}$$

a further potential feature of the proposed topology is its ability to set the output node from a halved to a doubled voltage respect to the nominal one commutating the control signal *STG_En* and *CKAR_En* from "01" to "10".

TABLE 1. Map of CP states.

		CKAR_En = 0	*CKAR_En* = 1
STG_En	0	$V_{OUT} = N_{eff} V_{DD} + V_{DD}$ *HS/HP*	$V_{OUT} = N_{eff} \frac{V_{DD}}{2} + V_{DD}$
	1	$V_{OUT} = 2N_{eff} V_{DD} + V_{DD}$	$V_{OUT} = 2N_{eff} \frac{V_{DD}}{2} + V_{DD}$ *LS/LP*

HS: *High Speed;* **LS:** *Low Speed;* **HP:** *High Power;* **LP:** *Low Power*

Regarding the state "11", ideally the CP with CKAR, which has the doubled number of stages, shows power conversion losses four times lower than the original CP. However, since the CKAR and the auxiliary circuits have finite power consumptions and occupy silicon area, they have been accounted in the total power and area architecture estimations.

It is worth noting that the CKAR has a finite driving capability and it must be properly modelled to take into account the finite level of current it provides to the CP. Hence, following the approach reported in [19], an equivalent *RC* time constant of the CKAR has to be evaluated and combined with the equivalent model in Fig. 2. At this purpose, it can be noted that the CKAR without an output load reaches its steady-state output voltage (i.e., a halved voltage with respect to the power supply) in only one period. This means that the CKAR equivalent capacitance is equal to zero, and only an equivalent resistance has to be considered. Moreover, since the CKAR is in series with the CP, the whole equivalent circuit, which includes the CP and the CKAR, results equal to the one reported in Fig. 2, but with the output equivalent impedance, R_{OUT}, given by

$$R_{OUT} = \frac{N^2}{C_{CPf}} + \frac{N^2}{C_{CKARf}} \tag{11}$$

From (11), it is apparent that in order to avoid worsening the output impedance a trade-off must be found between the total CP pumping capacitance and the capacitance of the CKAR. In particular, if the load is purely capacitive (very-low output current load in steady state), two different design strategies can be adopted, as detailed in the following.

The first simple design choice is to set $C_{CKAR} = C_{CP}$. it allows to minimize the output impedance of the whole system at the price of doubling the silicon area (assuming that the area of the charge pump is mainly determined by the area of the capacitors). A second strategy is to set $C_{CKAR} = C_{CP} = 0.5C_{TOT}$, which allows an efficient design without a silicon area increase. In this latter case, a capacitance C_{TOT} is equally split between the charge pump and the CKAR, but since the rise time depends on C_{CP}, this design choice leads to a slower CP.

For the sake of conciseness, in this paper only the first design strategy is adopted, where C_{CKAR} has been set to C_{CP}. Note, however, that although this choice leads to an occupied area increase, we exploited the use of different kind of capacitors available in the adopted technology to minimize the occupied area (as detailed in the next Section), thus making the proposed topology a very attractive technique to reduce the power losses and improve the power efficiency, without losing speed performance during the start up.

The proposed charge pump circuit is assumed to work in slow switching limit (SSL), which means that clock semi-period is enough larger than the highest RC-constant present in the circuit. This allows to neglect non ideal effects related to the actual generation of the clock like duty cycle distortion and jitter.

IV. SIMULATION RESULTS AND COMPARISON

To verify the effectiveness of the proposed topology and the actual advantage in term of power efficiency due to the clock reduction technique, a 2- to 4-stages CP has been designed and simulated using a standard 65-nm CMOS technology provided by STMicroelectronics. Assuming $V_{DD} = [450 - 750]$ mV, $f = 10$ MHz and $C_L = 40$ pF, the transistor aspect ratio are $(W/L)_a = 27/0.09$, $(W/L)_b = 15/0.15$, $(W/L)_1 = 4.5/0.09$, $(W/L)_{(1-3)a,b} = 4.5/0.09$, $(W/L)_{(4)a,b} = 0.18/0.09$ and the capacitance value $C_{CKAR} = 80$ pF. While for the single stage, aspect ratios of the cross-connected MOSFETs are $(W/L)_{n,p} = 0.6/0.06$ and the total pumping capacitance per stage is 20 pF.

The drivers and the NAND gates are implemented with standard cells having x7 and x5 driving capability, respectively. Considering the minimum generated CKAR voltage, MOS transistors with the lowest threshold voltage available for this technology ($V_{TH,max} = 300$ mV) are used. Moreover, Poly-to-Pwell and Metal-Insulator-Metal (MIM) capacitors are adopted for the CKAR and the stage capacitance, respectively. This combination allows to reduce the system total occupied area, thanks to the possibility to allocate all the active and passive components under the MIM capacitors, as can be noted in Fig. 5, where the full layout of the conventional and proposed CP is shown. Hence, as it appears by inspection of Fig. 5, the area occupation by the proposed architecture and the conventional one is equal. The routing overhead due to the increased complexity of the proposed solution is negligible since also all the additional metal interconnections are contained in the same area.

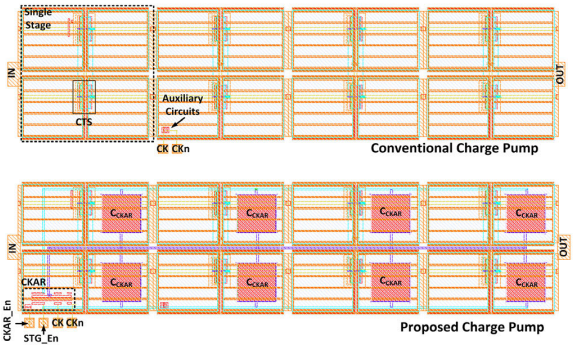

FIGURE 5. Layout view of the two compared CPs.

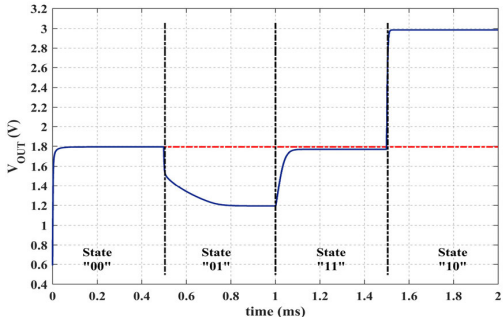

FIGURE 6. Complete operative cycle transient output voltage of the proposed CP for $V_{DD} = 600$ mV.

Transient post-layout simulations were run for a conventional latched (also named cross-coupled) CP with a number of stages equal to 2 and 4.

The comparison between every couple of CPs (with and without CKAR) was carried out for equal steady-state output voltage and total capacitance. The slight impact of the auxiliary circuitry on the power consumption of the proposed CP, as respect to a conventional CP, are shown in Table 2 where post-layout simulation results are reported for $V_{DD} = 600$ mV. In particular, it summarizes the input power (i.e, the steady state power losses), the Voltage Conversion Efficiency ($VCE_{\%}$), which is the ratio between the actual and the maximum ideal output voltage in steady-state, and the rise time, evaluated at 90% of the steady state output voltage.

The results show that $VCE_{\%}$ and rise time are almost equal for every simulated couple, whereas, as expected, slight increment in the power losses, due to the power dissipation of the CKAR and the auxiliary circuits, appears in the proposed system. The red angular arrow highlights the results of the two main compared topologies: the 2-stage latched CP and the 4-stage proposed CP with halved clock amplitude.

Figure 6 reports the transient output voltage of the proposed CP during a complete operative cycle, from the state "00" to the state "11". It confirms that output voltage can be set on three different values, according to Table 1.

Monte Carlo simulation results (100 occurrences) and corner analysis for three temperature values, -10, 27 and 80 °C, are summarized in Table 3 and IV, respectively. Obtained standard deviations (σ) show the robustness of the proposed topology to process, mismatches and temperature variations.

TABLE 2. Post-layout simulation results for $V_{DD} = 0.6$ V.

V_{CK}	Parameter	Proposed CP		Latched CP	
		2 stages	4 stages	2 stages	4 stages
V_{DD}	P_{LOSS} (nW)	***494.8***	1095	436.8	1044
	VCE (%)	***99.3***	99.5	99.7	99.5
	Rise Time (µs)	***4.22***	8.2	4.22	8.2
$V_{DD}/2$	P_{LOSS} (nW)	181.1	***281.2***		
	VCE (%)	99.4	***99.3***		
	Rise Time (µs)	20.34	***56.9***		

TABLE 3. Monte Carlo simulation results for $V_{DD} = 0.6$ V.

Parameter	-10°C		27°C		85°C	
	µ	σ	µ	σ	µ	σ
V_{CK} (mV)	319	2.2	308	3	301	0.9
V_{OUT} (V)	1.67	0.08	1.78	0.04	1.86	0.02
P_{LOSS} (nW)	254.6	2.5	287.4	1.7	309.3	1.2
Rise Time (µs)	5.88	0.59	4.92	0.46	4.24	0.29

TABLE 4. Corner analysis for $V_{DD} = 0.6$ V (Worst Corner).

Parameter	-10°C	27°C	85°C
	C_{MAX} + SS	C_{MAX} + SS	C_{MAX} + FF
V_{CK} (mV)	314.2	302.8	302.2
V_{OUT} (V)	1.63	1.62	1.72
P_{LOSS} (nW)	275.9	304.5	368,8
Rise Time (µs)	7.98	6.28	3.67

This is further stated by the comparison in Table 4 with the achieved results in the worst corner for the power losses. Note that in Table 4 the worst-case corner for the pumping capacitor (C_{MAX} is considered).

The plot in Fig. 7a shows the time response of the two compared CPs for three different values of the power supply voltage. The proposed topology was commuted from the state "00" to the state "11" after 50 μs, and the curves reveal that, after a brief transient, the output voltage reaches the output value of the traditional topology. It can be observed that the dynamic response of the proposed solution is lower due to the increase of the output resistance given by the series connection with the CKAR.

Inspection of the plot reveals that the proposed CP can work under a supply voltage of 450 mV, although the output voltage of the proposed CP is lower than that of the conventional one by 8 mV. To get rid of this reduction, the bootstrapping technique can be adopted [2].

In Fig. 7b the ratios of the simulated V_{OUT}, P_{LOSS} and the conversion ratio of the block CKAR as functions of the supply voltage V_{DD} are plot. Despite the finite power consumptions of the CKAR and of NAND gates degrade the potential advantage introduced by the adopted architecture, which ideally is predicted by relationship (4), as apparent from Fig. 7b, it is still advantageous, and a mean power saving of 36% is achieved.

Finally, in Fig. 7c it is reported the power conversion efficiency, PCE%, (i.e., the ratio between output and input power) of the proposed CP for the states "00" and "11". It shows that the proposed CP in the state "00" has the highest PCE% for heavy loads. Indeed, for light loads (i.e. value of R_{OUT} higher than $10^5\Omega$) the current dissipation of the CKAR

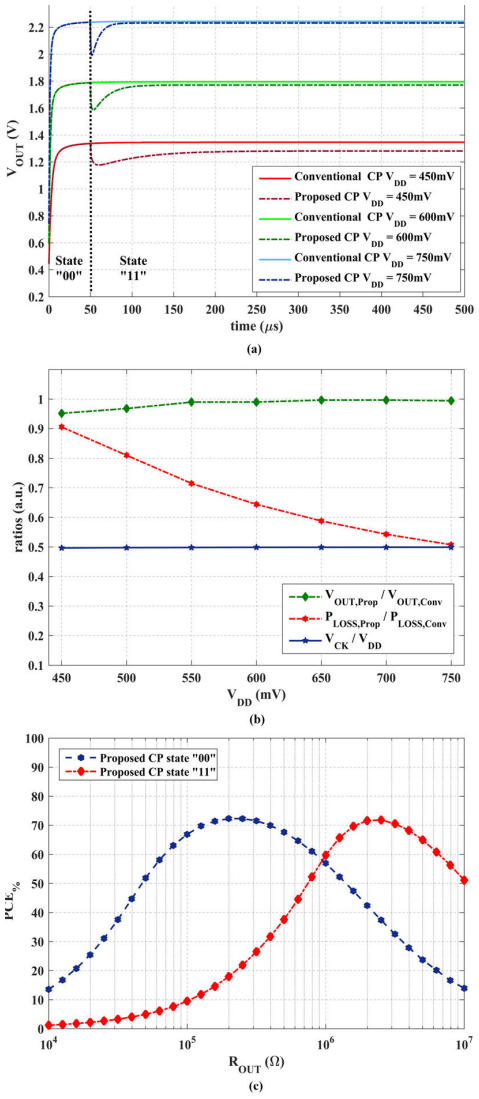

FIGURE 7. Transient output voltage comparison (a); CKAR conversion and power loss ratios (b); power efficiency comparison (c).

(even if equal to only 50 nA), sensibly lowers the PCE%. On the other hand, for low output currents the proposed CP exhibits the highest PCE% when working in the state "11".

In order to compare the proposed solution with the state of the art of reconfigurable charge pump circuits for energy harvesting applications, main data of the proposed solution and the one in the literature are summarized in Table 5. The comparison apparently shows that the proposed CP occupies the smallest area and exhibits the lowest quiescent power. To further compare the different solutions, the figure of merit

$$FoM_Q = \frac{QuiescentPower}{Frequency_{MAX} * Area} \tag{12}$$

is considered, which evaluates the energy per area lost during each cycle, due to quiescent state of the charge pump. From Table 5 it can be seen that the proposed architecture shows the best performance.

Finally, a comparison normalized respect to the technology node is considered by introducing the figure of

TABLE 5. Performance comparison.

Ref	[6]	[20]	[21]	[22]	**This work**[a]
***Tech.* (nm)**	180	180	130	180	65
Architecture	Voltage doubler	Voltage doubler	Modified Bootstrap	Hybrid	Cross-coupled
Aux. circuits	MPPT	OVC	OVC	OVC	CKAR
***Input range* (V)**	0.45-3	0.14-0.5	> 0.27	1	0.45-0.75
***Output range* (V)**	3	2.2-5-2	1.4	3-6	1.2-3
***Peak PCE* (%)**	89	50	65	58	73
# stages	3	4	4	6	4
***Load cap.* (pF)**	2050 [b]	1000	500	54	40
***Frequency* (MHz)**	up to 1.05	up to 19	up to 1	up to 20	10
***Quiescent Power* (μW)**	3.84	0.006	2.62	--	0.0002
***Area* (mm^2)**	0.032	0.86	0.42	0.5	0.023
***FoM*$_Q$ (pJ/mm^2)**	114.3	3.7E-4	6.24	--	9E-5
***FoM*$_{Qnode}$ (fJ/nm^2)**	0.13	1E-5	0.16	--	5E-7

[a] post-layout simulations; [b] off-chip capacitors;
Acronyms: MPPT (Maximum power point tracker), OVC (output voltage controller)

merit

$$FoM_{Qnode} = \frac{QuiescentPower}{\min .channel\_length^2} \tag{13}$$

It can be observed from Table 5 that the proposed solution achieves the best performance. It should be noted, however, that solutions [6] and [22] show higher quiescent current due to some auxiliary analog and digital circuits related to the specific application.

V. CONCLUSION

In this paper, a dynamically reconfigurable linear charge pump which exploits the clock amplitude reduction to improve power efficiency, while maintaining speed performance is described and analyzed. Theoretical analysis and post-layout simulation results showed that the proposed technique is advantageous and useful in the case of energy-constricted applications requiring a small number of stages to boost the input voltage and feed a purely capacitive load.

In particular, the topology presented, whose auxiliary circuitry has negligible power consumption, allows to reduce the power loss of more than 35% without any penalty on the CP speed performance.

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