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Multi-Level Multi-Input Converter for Hybrid Renewable Energy Generators

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Abstract: A three-phase multi-level multi-input power converter topology is presented for grid-connected applications. It encompasses a three-phase transformer that is operated on the primary side in an open-end winding configuration. Thus, the primary winding is supplied on one side by a three-phase N-level neutral point clamped inverter and, on the other side, by an auxiliary two-level inverter. A key feature of the proposed approach is that the N-level inverter is able to perform independent management of N-1 input power sources, thus avoiding the need for additional dc/dc power converters in hybrid multi-source systems. Moreover, it can manage an energy storage system connected to the dc-bus of the two-level inverter. The N-level inverter operates at a low switching frequency and can be equipped with very low on-state voltage drop Insulated-Gate Bipolar Transistor (IGBT) devices, while the auxiliary inverter is instead operated at low voltage according to a conventional high-frequency two-level Pulse Width Modulation (PWM) technique and can be equipped with very low on-state resistance Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET) devices. Simulations and experimental results confirm the effectiveness of the proposed approach and its good performance in terms of grid current harmonic content and overall efficiency.

Keywords: multi-level inverter; multi-input converter; renewable energy sources; maximum power point tracking; solar power; wind power; open-end winding

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1. Introduction

The number of electricity generators powered by renewable energy sources (RESs) is continuously increasing because of concerns about environmental pollution and the limited reserves of fossil energy sources such as oil, coal, and gas [1]. Grid-connected photovoltaic (PV) and wind turbine (WT) generators are the most widely diffused types of RES power plants and their specific cost is continuously decreasing [2–4]. However, available solar and wind energy are affected by some factors, such as season cycle, daily cycle, temperature, and weather conditions, which make them intermittent and stochastic. Therefore, a power plant relying only on a single form of RES and without an energy storage capability can hardly cope with the requirements for a reliable electric power generation unit. Hybrid renewable energy systems (HRESs) combining more than one energy source are a viable solution to this problem [5] because they are effective not only in enhancing the reliability of power supply but also in reducing the size of energy storage systems [6,7]. However, in HRESs, a specific dc–dc power converter is normally used to manage each input power source, leading to a quite complex and expensive structure [8,9].

The multiple input power converter (MIPC) concept is a possible alternative to HRESs having to cope with sources with different power capacity and/or voltage levels, providing a well-regulated dc output voltage. Both isolated and non-isolated dc/dc multi-input converters find application in hybrid vehicles [10], the aerospace industry, and RES power plants. A non-isolated double input dc/dc converter is proposed in [11] combining buck and buck-boost single-input topologies, while an *n*-input buck-boost topology is presented in [12], which however could not supply the load simultaneously from different sources. A bidirectional multi-input dc/dc converter was also developed in [13], which is burdened by high conduction losses. The efficiency of an MIPC can be increased by exploitation of zero voltage switching approaches, as in [14,15]. Some MIPC topologies have been purposely developed for application in HRESs [16]. Among them, three-port dc/dc converters are of major interest. They feature an input port, an output one, and a storage port, enabling a bidirectional power flow towards/from an energy storage system (ESS). Some non-isolated three-port converters are discussed in [17–21].

A different approach is proposed in this paper, where a particular kind of multiple-input multi-level converter (MMC) is exploited to connect photovoltaic and wind generators to an energy storage system and a three-phase ac grid. It is based on an open-end winding configuration, the asymmetrical hybrid multi-level inverter (AHMLI), whose applications on both motor drives and grid-connected generators are discussed in [22,23] and which has also been successfully exploited to reduce the overvoltage caused by long cables in PWM motor drives [24] as well as to realize a high-speed Gen-set [25,26]. In the present HRES application, the AHMLI topology encompasses an open-end winding three-phase transformer (OWT) whose primary winding operates in an open-end configuration. The primary winding is, in fact, supplied on one side by a three-phase neutral point clamped (NPC) multi-level inverter (MLI) and, on the other side, by a conventional two-level inverter (TLI). The MLI operates at a low switching frequency (<1 kHz), thus featuring very low switching power losses. It is tasked to control the active power supplied to the grid, while also managing *N-1* unidirectional input power flows, being *N* the number of the output voltage levels. Thus, *N-1* energy sources (ESs) such as photovoltaic (PV) strings or wind turbines (WTs) can be managed without the introduction of additional dc/dc power converters. Moreover, it can also accomplish a multi-channel maximum power point tracking (MPPT) function at the string level on PV arrays. Compared with the MLI, the TLI operates at a high switching frequency, but at a lower dc bus voltage. It is tasked to control the grid current and to compensate for low-order current harmonics and unbalanced components. Moreover, its dc-bus can act as the storage port of a three-port dc–dc converter, enabling the connection of an energy storage system (ESS) to the HRES. In other words, energy sources connected to the MLI are managed by the TLI, avoiding the introduction of dc/dc power converters.

The paper is organized as follows. Section 2 presents the proposed approach and its application to 5LI + TLI and 3LI + TLI topologies. In Section 3, the operations of these topologies are discussed. Simulation and experimental results are presented in Sections 4 and 5, respectively. Finally, Sections 7 and 8 concern the discussion and conclusion.

2. The Proposed MMC Topology

The proposed MMC for HRESs, tailored around the AHMLI topology, is shown in Figure 1. The primary winding of the three-phase transformer is connected to an *N*-level NPC inverter on one side and to an auxiliary TLI on the other side. The secondary winding is instead connected to a three-phase ac grid. The NPC inverter, which acts as an *N*-level multi-input converter, encompasses $N-1$ DC-bus capacitors C_j, each one connected to a dc power source of voltage V_{ck} ($k = 1,2,3,N-1$). According to the AHMLI topology and assuming that the two inverters are supplied by two independent power sources, V_{DC}' and V_{DC}'', a phase voltage V_{pj} ($j = 1,2,3$) of the primary winding of the OWT is given by:

$$V_{pj} = V_{NPCj} - V_{TLIj} - V_{O'O''} = \frac{2l'-2}{4} V_{DC}' - (2l''-1) V_{DC}''/2 - V_{O'O''} \quad l' = 0,1,2 \quad l'' = 0,1 \tag{1}$$

where V_{NPCj} is the NPC output j-phase voltage referred to the mid-point O' (Equation (2)), V_{TLIj} is the TLI output j-phase voltage referred to the mid-point O'' (Equation (3)), V_{DC}'' is the dc-bus voltage of the TLI, V_{DC}' is the total dc-bus voltage of the NPC, and $V_{O'O''}$ is the voltage between the mid points O' and O'' of the dc-buses of the two inverters (Equation (4)).

$$V_{NPCj} = \frac{2l'-2}{4} V_{DC}' \quad l' = 0,1,2 \tag{2}$$

$$V_{TLIj} = \frac{2l''-1}{2} V_{DC}'' \quad l'' = 0,1 \tag{3}$$

$$V_{O'O''} = \frac{1}{3} \sum_{j=1}^{3} (V_{MLIj} - V_{TLIj}) \tag{4}$$

As V_{NPCj} may take N levels, while V_{TLIj} may take two, the transformer primary phase voltage V_{pj} may take $2N$ levels, whose amplitude is a function of V_{DC}' and V_{DC}''. Table 1 shows that in terms of phase voltage levels, the proposed configuration is equivalent to a conventional multi-level inverter with a larger number of power devices. From another point of view, a lower phase voltage THD (Total Harmonic Distortion)is obtained with the same number of switches.

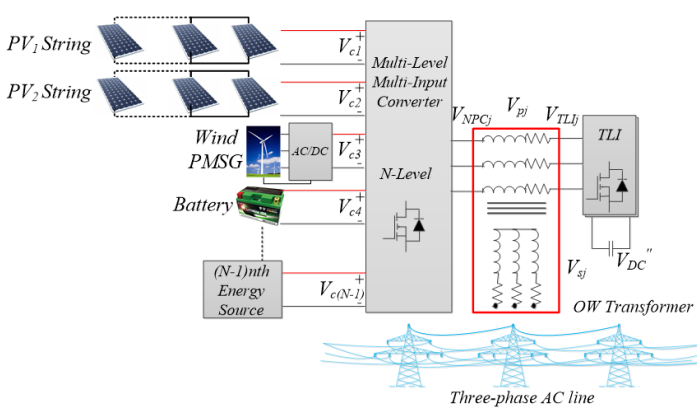


Figure 1. Proposed multi-level converter (MMC) configuration.

Table 1. Basic multi-level inverter (MLI) topologies vs. the asymmetrical hybrid multi-level inverter (AHMLI).

MLI	NPC or Flying Capacitor		MMC (MLI+TLI) $V_{DC}'' = V_{DC}'/[(N-1)]$			
	Power Switches	Phase Voltage Levels	Power Switches			Phase Voltage Levels
			MLI	TLI	MLI+TLI	
3-L	***12***	***9***	*12*	*6*	***18***	***17***
5-L	***24***	***17***	*24*	*6*	***30***	***25***
7-L	***36***	***25***	*36*	*6*	***42***	***33***
9-L	***48***	***33***	*48*	*6*	***54***	***41***

As an example of an HRES application of the AHMLI topology, a six-level MMC is shown in Figure 2. PV strings, or groups of strings, are directly connected to the NPC's dc-bus capacitors while the permanent magnet synchronous generators of the wind turbines are connected through a three-phase controlled rectifier or a diode rectifier and an output dc-link capacitor. All dc sources must have about the same rated output voltage in order to prevent largely unbalanced dc-bus voltages. However, the TLI is able to compensate a NPC DC-bus capacitor voltage variation ΔV_c provided that it is lower than V_{DC}'', thus achieving a sinusoidal grid current. The dc-buses of the NPC and auxiliary inverters are isolated between them in order to prevent the circulation of zero-sequence currents [22]. Moreover, the TLI dc-bus is supplied through a floating capacitor; thus, an additional power source is not required. Another example is shown in Figure 3, where a five-level NPC inverter is used. In this case, an ESS is connected to the TLI dc-bus, and a bidirectional power flow can be managed towards/from the ESS. In both examples, the NPC provides the active power flow to the grid, while the TLI works as an active power filter, while also regulating the output current and the NPC dc-bus capacitor voltages V_{ck}.

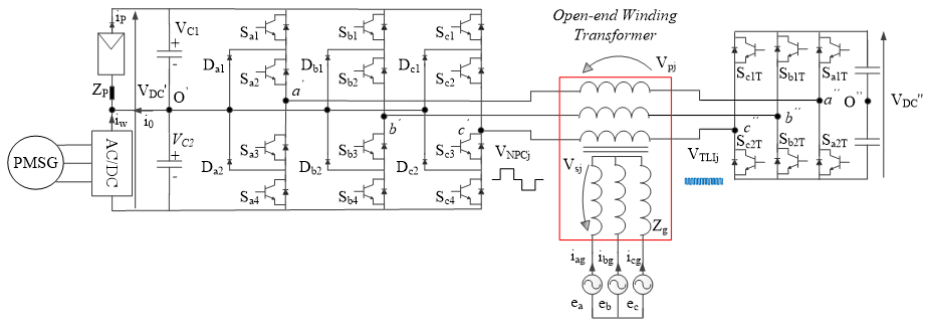


Figure 2. Six-level MMC (three-level inverter (3LI) + two-level inverter (TLI)) with two energy sources.

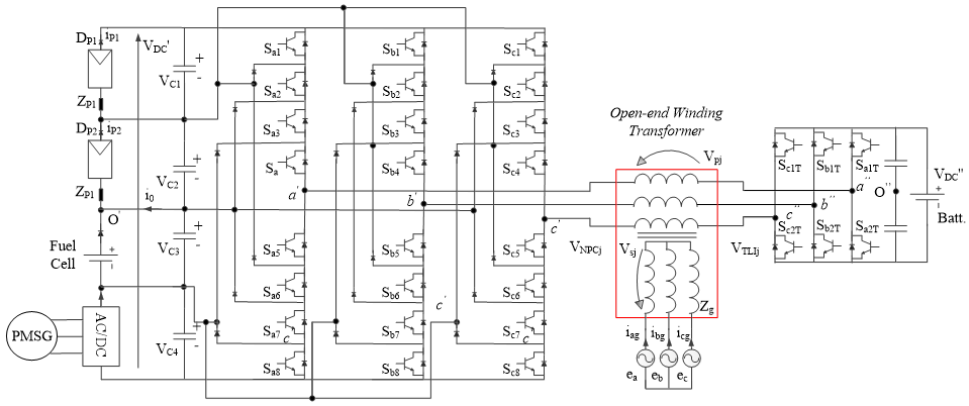


Figure 3. Ten-level MMC (5LI + TLI) with four energy sources and an energy storage device.

3. Proposed MMC Topology Operation

In order to manage multiple input sources while controlling the main power flow towards the grid, a suitable control system has been developed that is divided into two main parts: an MLI control subsystem and a TLI control subsystem.

3.1. MLI Control Subsystem

MLI switching power losses are kept low by taking advantage of low-frequency space vector modulation (SVM) or step modulation (ST). However, these modulation techniques must be suitably modified to allow for a direct periodical connection between

the *N-1* energy sources connected to the MLI dc-bus and the TLI. This is necessary to enable independent voltage control on each of the *N-1* MLI dc-bus capacitors. According to (1), the space diagram of the transformer primary phase voltage V_{jp} is obtained by combining the voltage space vector diagrams of the two inverters. The simplest MMC configuration that can be obtained according to the proposed approach encompasses a three-level inverter (3LI + TLI), which provides six voltage levels if $V_{DC}'' = V_{DC}'/(N-1)$. Such an MMC may take $3^3 = 27$ switching states; however, only 19 different voltage vectors can be generated, because some of the switching states are redundant. The MMC voltage space vector diagram can be obtained by adding the voltage space vector diagram of the TLI at the top of each voltage vector of the 3LI, as shown in Figure 4 [27]. Each input dc source can be independently managed by exploiting its periodical connection to the transformer's primary winding, which occurs when the 3LI generates one of the twelve possible low-voltage vectors (LVVs), namely PPO, OON, POO, ONN, ONO, POP, NNO, OOP, NOO, OPP, NON, and OPO, according to Figure 4 and Table 2. As an example, Figure 5 shows that when the voltage vector PPO is generated, the capacitor C_1, which represents the output capacitor of the energy source ES_1, is directly connected to the TLI. Hence, when the voltage vector PPO is generated, V_{C1}, that is, the voltage across C_1, can be regulated by controlling the power stream between the 3LI and the TLI. This is accomplished through a closed loop voltage controller managing the power exchange between ES_1 and the TLI dc-bus capacitors through a specific set of components V_{kj} of the TLI reference voltage, as shown in Figure 5c. In practice, the voltage regulator, by processing the difference between the C_1 reference voltage V_{c1}* and the actual value V_{c1}, generates a coefficient I, which is multiplied by the actual values of the transformer's primary currents to obtain V_{kj}. Therefore, if I is positive, an additional power transfer is instated directed towards C_1, thus increasing V_{c1}. If I is negative, the additional power flow is directed from C_1 to the TLI dc-bus capacitors, thus discharging C_1 and reducing V_{c1}. Hence, it is possible to charge or discharge C_1 when the MLI generates the vector PPO. The same applies for the other dc bus capacitors when the MLI is generating the specific LVV.

In general, for a *N*-level NPC converter, *N-1* space vectors can be exploited for controlling *N-1* input dc sources. For instance, Figure 6 shows the space phasor diagram of a 10-level MMC composed of a five-level NPC and a TLI (5LI + TLI) as that shown in Figure 3, where V_{DC}''/V_{DC}' is set to 0.25. The energy sources that can be managed in this case are four, namely ES_1, ES_2, ES_3, and ES_4, each one connected to the MLI dc-bus through an output capacitor C_j $(j = 1\ldots4)$. The voltage V_{Cj} across the output capacitor C_j can be regulated by acting on the six LVVs shown in Figure 6, being P_1, P_2, O, N_1, and N_2 the possible states of the j-leg, as shown in Table 3. When the vector R_2 $(P_2P_2P_1)$ is generated, the capacitor C_1 is directly connected to the TLI through the primary windings of the transformer, as shown in Figure 7, making possible the regulation of the voltage V_{c1} by controlling the power stream between the two converters.

For low modulation indexes, it is possible to regulate the voltage of the *N-1* dc-bus capacitors without modification of the conventional multilevel SVM or SM strategies, because the top of the reference voltage vector V_m* always lies inside the hexagon encompassing R_1, R_2, R_3, R_4, R_5, and R_6. According to the basic multi-level SVM strategy, the voltage–time Equation (5) referred to a stationary *q,d* reference frame gives the switching times t_a, t_b, and t_c from the voltage reference V_m* and the switching period T_m. As shown in Figure 8a, for low modulation indexes, V_a coincides with the null state V_0, while V_b and V_c are those LVVs whose tops coincide with the vertices of the triangle in which the top of the reference voltage vector lies. However, as shown in Figure 8b, for medium and high modulation indexes, no LVVs are selected according to the conventional SVM strategy; thus, they must be purposely introduced in the inverter switching path. This can be obtained by substituting one of the vectors V_a, V_b, or V_c of Equation (5) with a switching sequence including the LVV that must be activated, and other two voltage vectors V_1 and V_2. If, as shown in Figure 8c, the LVV R_1 must be activated, the switching times t_R, t_1, and t_2 are given by Equation (6), being T_a obtained by solving Equation (5). A similar procedure

can be adopted to modify the switching patterns generated according to the standard multi-level SM.

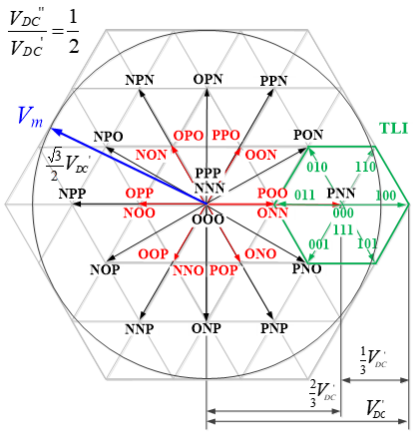


Figure 4. Three-level neutral point clamped (NPC) + TLI voltage space vector diagram ($V_{DC}''/V_{DC}' = 1/2$).

Table 2. Six-level MMC low voltage vectors.

Vector	S_{a1}	S_{a2}	S_{a3}	S_{a4}	S_{b1}	S_{b2}	S_{b3}	S_{b4}	S_{c1}	S_{c2}	S_{c3}	S_{c4}
PPO	1	1	0	0	1	1	0	0	0	1	1	0
OON	0	1	1	0	0	1	1	0	0	0	1	1
POO	1	1	0	0	0	1	1	0	0	1	1	0
ONN	0	1	1	0	0	0	1	1	0	0	1	1
ONO	0	1	1	0	0	0	1	1	0	1	1	0
POP	1	1	0	0	0	1	1	0	1	1	0	0
NNO	0	0	1	1	0	0	1	1	0	1	1	0
OOP	0	1	1	0	0	1	1	0	1	1	0	0
NOO	0	0	1	1	0	1	1	0	0	1	1	0
OPP	0	1	1	0	1	1	0	0	1	1	0	0
NON	0	0	1	1	0	1	1	0	0	0	1	1
OPO	0	1	1	0	1	1	0	0	0	1	1	0

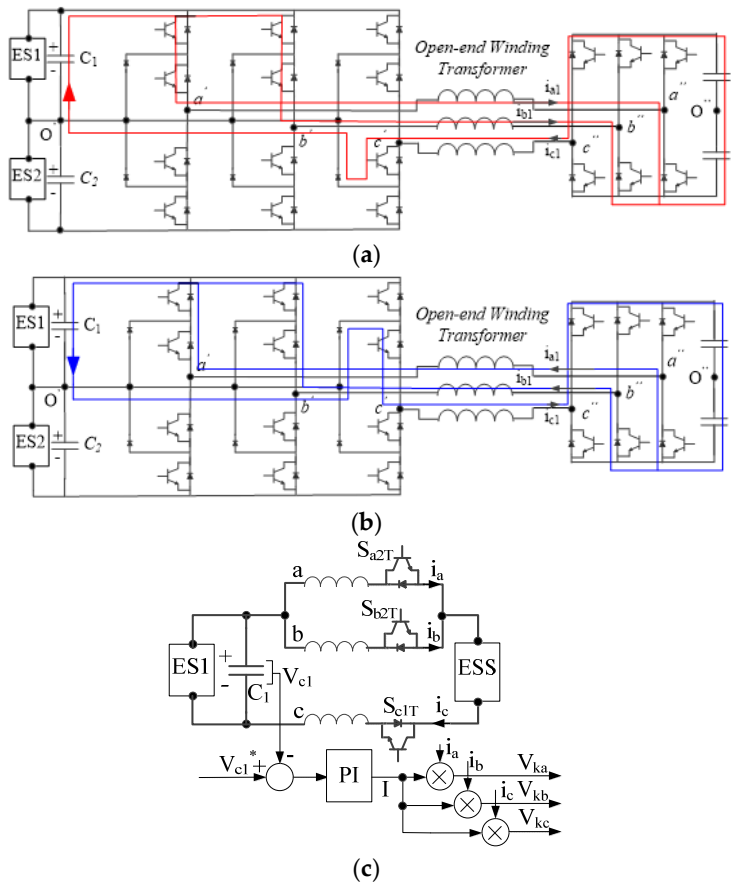


Figure 5. Three-level inverter (3LI) + TLI: C_1 voltage control when the PPO vector is generated: (**a**) discharging; (**b**) charging; (**c**) equivalent voltage control loop during PPO.

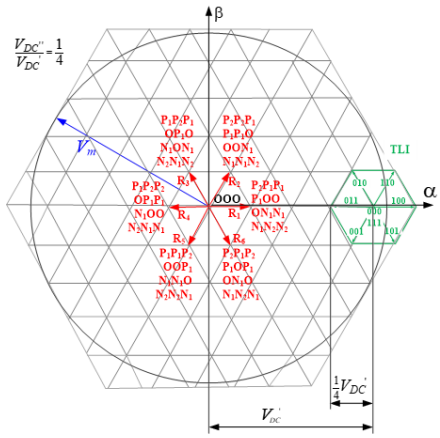


Figure 6. Five-level inverter (5LI) + TLI voltage space vector diagram ($V_{DC}''/V_{DC}' = 1/4$).

Table 3. Five-level NPC j-leg states.

Vector	S_{j1}	S_{j2}	S_{j3}	S_{j4}	S_{j5}	S_{j6}	S_{j7}	S_{j8}
P_2	1	1	1	1	0	0	0	0
P_1	0	1	1	1	1	0	0	0
O	0	0	1	1	1	1	0	0
N_1	0	0	0	1	1	1	1	0
N_2	0	0	0	0	1	1	1	1

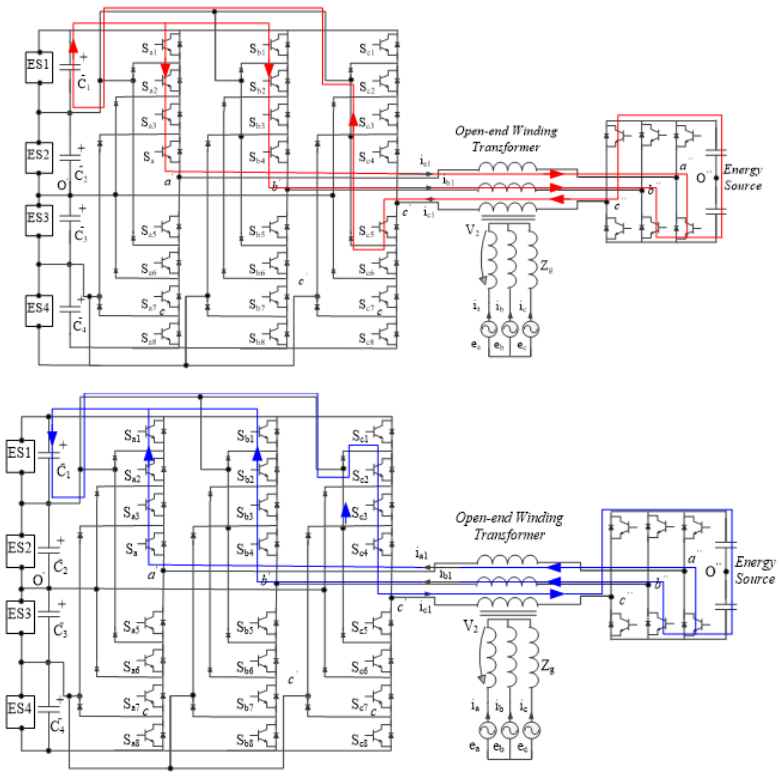


Figure 7. Five-level inverter (5LI) + TLI: C_1 voltage control when the $P_2P_2P_1$ vector is generated: (up) discharging; (down) charging.

$$\begin{cases} T_m V_{m\alpha}{}^* = t_a V_{a\alpha} + t_b V_{b\alpha} + t_c V_{c\alpha} \\ T_m V_{m\beta}{}^* = t_a V_{a\beta} + t_b V_{b\beta} + t_c V_{c\beta} \\ T_m = t_a + t_b + t_c \end{cases} \tag{5}$$

$$\begin{cases} T_a V_{a\alpha} = t_1 V_{1\alpha} + t_2 V_{2\alpha} + t_R V_{R1\alpha} \\ T_a V_{a\beta} = t_1 V_{1\beta} + t_2 V_{2\beta} + t_R V_{R1\beta} \\ T_a = t_1 + t_2 + t_R \end{cases} \tag{6}$$

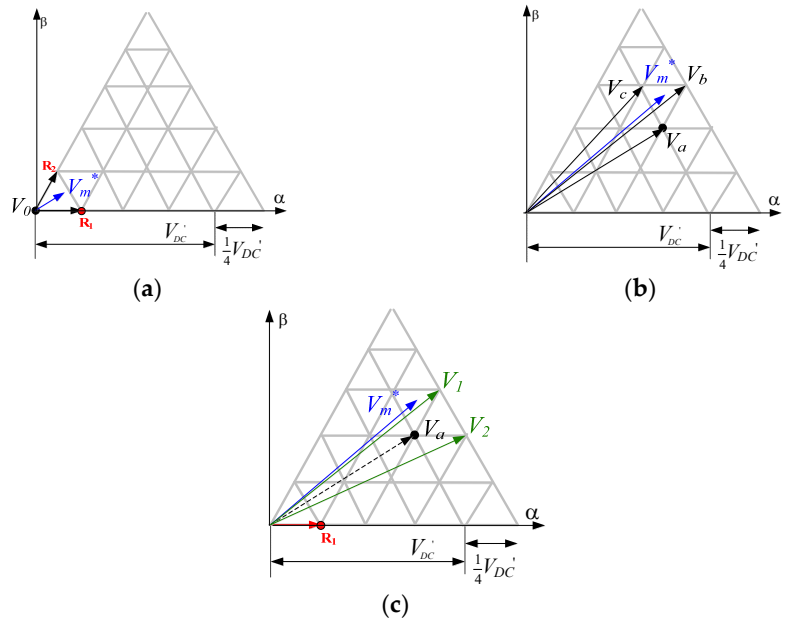


Figure 8. Five-level inverter (5LI) + TLI. (**a**) Space vector modulation (SVM) at a low modulation index. (**b**) SVM at a high modulation index. (**c**) Modified SVM.

3.2. TLI Operation and 3LI + TLI Control Algorithm

Transformer primary voltage harmonics generated by low-frequency modulation of the main inverter are then cancelled by the TLI. In fact, the TLI working at a high switching frequency plays the role of an active power filter while also managing the power flows originating from the *N-1* energy sources connected to the MLI dc-bus and compensating for possible imbalances caused by different dc-bus capacitor voltages. This makes it possible to avoid the introduction of additional dc/dc converters, which otherwise would be necessary to connect each energy source to the system. The MMC control system encompasses a synchronous *qd* current controller regulating the transformer's primary current and the *N-1* voltage controllers to manage the energy sources connected to the MLI dc-bus [28]. A schematic of the control system developed for the proposed MMC is shown in Figure 9 for a 3LI + TLI configuration. It consists of three main blocks, namely TLI dc-bus current (battery) control, NPC dc-bus voltage (energy sources) control, and regulation of active and reactive power at the primary side of the transformer. Moreover, a *N-1* channels maximum power point tracking function can be provided in order to cope with PV arrays connected as energy sources. In this case, according to Figure 5, the MPPT sets the reference voltages V_{c1} and V_{c2}, whose sum V_{DC} *' constitutes the reference for the q-axis 3LI current regulator. The reactive power is instead controlled by acting on the d-axis current. An independent control on V_{c1} and V_{c2} is obtained by two voltage controllers, whose outputs are processed in order to obtain the components V_{kja} of the TLI reference voltages as shown in Figure 5c. Whenever one LVV is active, *k* is set to 1 and the reference coefficient *I* is computed to charge or discharge the considered capacitor. At the same time, the correct MLI voltage vector path is selected according to Equations (5) and (6) in order to connect the specific energy source to the TLI, thus establishing a power stream from the energy source to the TLI d-bus. Further components of the TLI reference voltage V_{hj} and V_{battj} are computed dealing, respectively, with the compensation of harmonics generated by the low-frequency operation of the MLI (Equation (7)) and control of the battery current i_{DC}''. Hence, the *j*-phase TLI reference voltage is given by Equation (8) while V_{hj} is written in (7).

$$V_{hj} = V_{NPCj} - V_{1NPCj} \tag{7}$$

$$V_{TLIj}{}^{*} = V_{hj} + V_{Battj} + V_{kj} \tag{8}$$

being V_{1NPCj} the fundamental component of the NPC output phase voltage V_{NPCj}. The TLI current control is also able to compensate for imbalanced voltages on the 3LI dc-bus by adapting the duty cycle of the TLI at each half-cycle. This capability depends on the value of V_{DC}'', which is the maximum capacitor voltage deviation value that can be compensated for. Hence, the TLI ensures a sinusoidal grid-current during $V_c = V_{cn} \pm V_{DC}''$ for all NPC dc-bus capacitors.

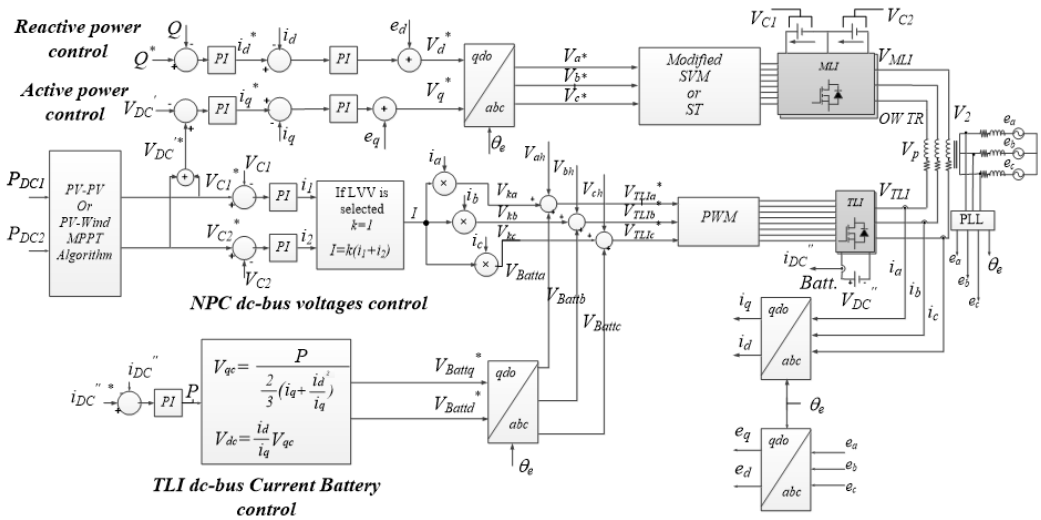


Figure 9. Six-level MMC (3LI + TLI).

4. Simulation Results

The effectiveness of the proposed topology was first evaluated through a simulation, taking into account a scaled model of a hybrid renewable energy generator tailored around an open-end winding *5 kVA-230/400 V* three-phase transformer, a three-level NPC inverter exploiting a *1 kHz* SVM strategy with a *400 V* dc-bus voltage, a TLI PWM operating at *10 kHz*, and a three-phase grid. The parameters of the system components are listed in Tables 4–11. These include the main data of the IGBT and diodes on the NPC MLI and those of the power MOSFET devices present on the TLI.

Two cases are taken into consideration: a fully PV system with an ESS; and a hybrid PV–wind one with an ESS. The system model was developed using the MATLAB/Simulink environment and setting a *1 μs* sample time. Output power characteristics of the PV modules are shown in Figure 10. Each PV string consists of five modules in order to achieve a peak voltage of *200 V* on the NPC dc-bus capacitors C_1 and C_2. Operation of the first configuration is shown in Figure 11, dealing with NPC dc-bus voltages V_{C1} and V_{c2}, the output power of ES_1, ES_2, and the battery, the irradiances of PV strings G_{PV1} and G_{PV2}, the transformer's primary and secondary voltages, the NPC output voltages V_{NPCj}, the grid currents, the TLD bus voltage V_{DC}'' and current i_{DC}', the battery's state of charge (SOC), and the qd-axes current components. At $t = 0.5s$, the solar insolation on the ES_2 PV string falls down from 1000 W/m^2 to *700 W/m*^{2}. Then, the ES_2 output power decreases from *600 W* to *560 W*. According to Figure 10, the voltage V_{c2} is then reduced to track the maximum power point by acting on the TLI according to the voltage control scheme of Figure 5c. Once V_{c2} has reached the new optimal value, an imbalanced voltage condition ($V_{c1} = 200\ V$, $V_{c2} = 165\ V$) occurs. However, the three-phase grid currents are kept sinusoidal by the TLI current control system by drawing power from the ESS, as the SOC diagram confirms. In this case, in fact, the TLI dc-bus voltage $V_{DC}'' = 210\ V$ is sufficient to compensate for the $\Delta V_{c2} = (200 - 165)\ V = 35\ V$ voltage deviation. Figure 12 deals instead with operation of the second configuration, when the rotor speed of the wind turbine ω_{rm} drops from *1500* to *0*

rpm. Additionally, in this case, the TLI dc-bus voltage $V_{DC}'' = 210\ V$ is sufficient to compensate for the $\Delta V_{c2} = (200 - 200)\ V = 0\ V$ voltage deviation. The proposed system is able to manage a bidirectional power stream towards/from the energy storage system as shown in Figure 13. The irradiances considered for PV_1 and PV_2 are not the same, being respectively *1000 W/m²* and *700 W/m²*, while the battery current varies from 2.5A to −2.5A. The battery SOC trend demonstrates the bidirectional power capability of the proposed configuration.

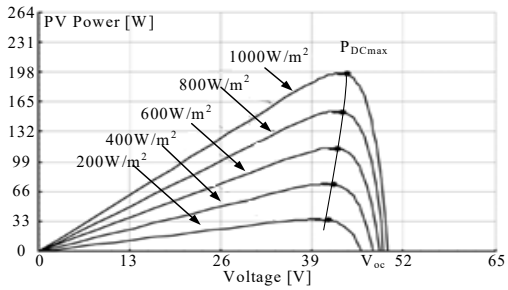


Figure 10. P-V diagrams of photovoltaic modules.

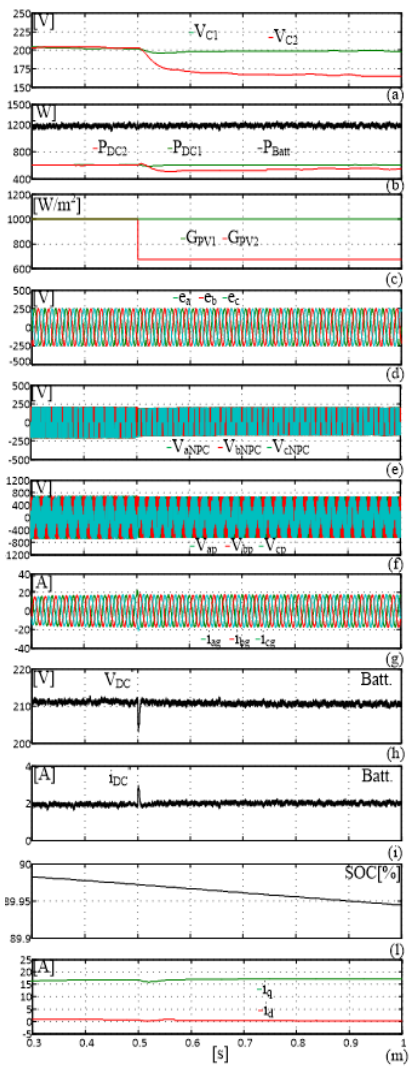


Figure 11. Six-level MMC-G_{PV2} drop from 1000 W/m² to 700 W/m². (**a**) String voltages V_{c1} and V_{c2}. (**b**) ES_1, ES_2, and energy storage system (ESS) output power. (**c**) G_{PV1} and G_{PV2}. (**d**) Grid voltage. (**e**)

NPC output voltage. (**f**) Primary voltage. (**g**) Grid current. (**h**) Battery voltage. (**i**) Current. (**l**) State of charge (SOC). (**m**) Output d,q axes currents.

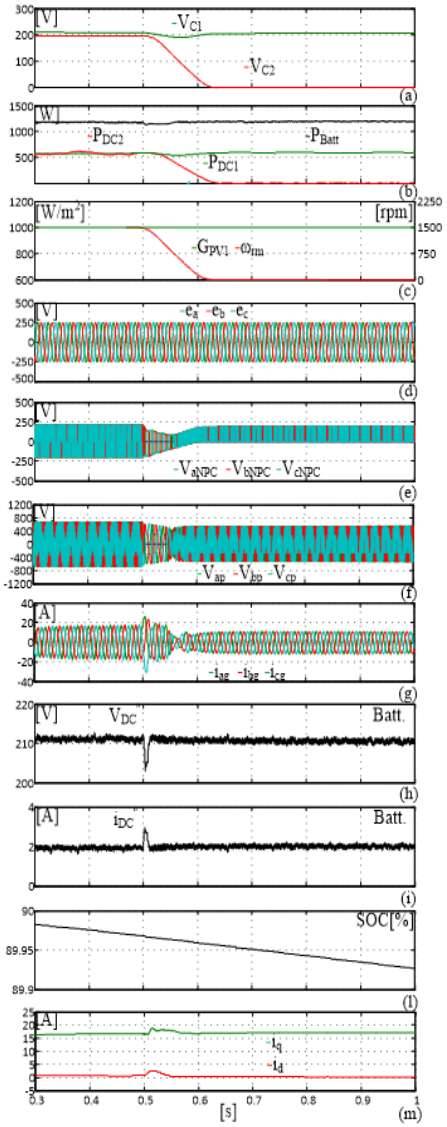


Figure 12. Six-level MMC-wind turbine (WT) shut-down G_{PV1} = 1000 W/ m². (**a**) V_{c1} and V_{c2}. (**b**) ES_1, ES_2, and ESS output power. (**c**) G_{PV1} and PMSG rotor speed ω_r. (**d**) Grid voltage. (**e**) NPC output voltage. (**f**) Primary voltage. (**g**) Grid current. (**h**) Battery voltage. (**i**) Current. (**l**) SOC. (**m**) Output d,q axes currents.

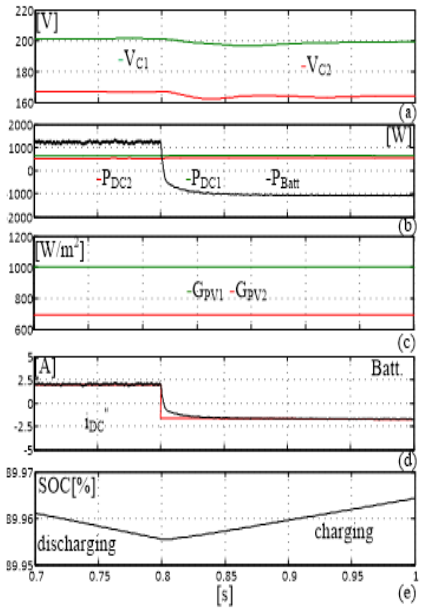


Figure 13. Si-level MMC-battery current transition from 2A to −2A with GPV1 ≠ GPV2. (**a**) String voltages Vc1 and Vc2. (**b**) Output power of PV1, PV2, and the battery. (**c**) Solar power GPV1 and GPV2. (**d**) Battery current. (**e**) Battery SOC.

Table 4. Three-phase grid.

e_g (V)	400
f (Hz)	50
L_g (mH)	3

Table 5. Three-phase transformer.

A_n (kVA)	5
V_{n1} (V)	400
V_{n2} (V)	400
t	1

Table 6. PV modules (STC).

P_{nom} (W)	200
V_{mpp} (V)	40
I_{mpp} (A)	5
I_{cc} (A)	5.40
V_{open} (V)	47.8
string	5 modules

Table 7. Wind Turbine.

Pn (W)	1000
Vn (V)	220
ω_{wind} (m/s)	10
ω_{max} (m/s)	55
ω_0 (m/s)	2
Generator	Permanent Magnet Synchronous Generator PMSG

Table 8. Battery.

(Ah)	*50*
Vn (V)	*400*
Type	*Lithium-Ion*

Table 9. Diodes.

V_{DS} *(V)*	*1000*
I_n *(A)*	*30*
t_{rd} *(ns)*	*67*
Q_r *(μC)*	*1.5*

Table 10. MLI-IGBT (STGW40N120K).

V_{ce} *(V)*	*1200*
V_{enON} *(V)*	*2.7*
I_n *(A)*	*40*
t_r *(ns)*	*48*
t_f *(ns)*	*338*

Table 11. TLI-MOSFET (IRFB5615PBF).

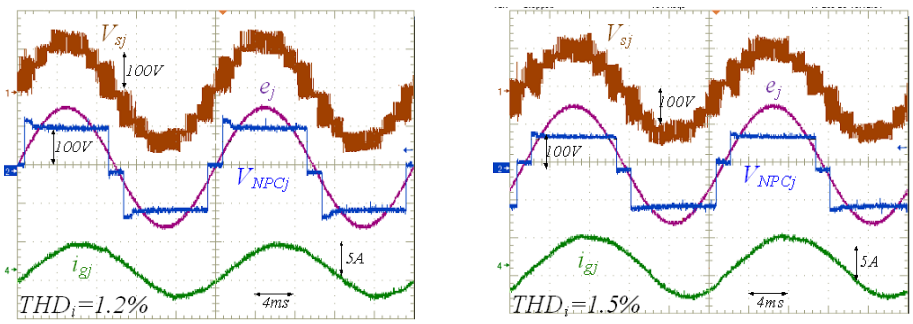
V_{DS} *(V)*	*150*
R_{DSON} *(mΩ)*	*32*
I_n *(A)*	*35*
t_r *(ns)*	*17.2*
t_f *(ns)*	*35*

5. Experimental Assessment

Experimental tests were accomplished on a six-level MMC encompassing an open-end winding *5 kVA-230 V/400 V* three-phase transformer, a 3LI-NPC inverter with a *200 V* dc-bus voltage exploiting an SM strategy, and a two-level inverter PWM operating at *10 kHz*. A *100 V*, *40 Ah* Lithium-ion battery was connected to the dc-bus of the TLI. All system parameters are listed in Tables 4–11. The control system was realized around a DSpace/1103 board running at *10 kHz*. The primary winding of the transformer was connected, on one side, to the NPC MLI and, on the other side, to the TLI. Programmable PV module emulators played the role of two PV strings connected to the NPC dc-bus. Steady-state operation under balanced and imbalanced conditions is shown in Figure 14a and b, dealing with the 3LI + TLI output voltage, grid voltage, grid current, and 3LI output step voltage. In Figure 14a, a balanced condition is considered with $V_{c1} = 100\ V$, $V_{c2} = 100\ V$. Hence, the TLI acts only as an active power filter in order to compensate for the low-order harmonic generated by the NPC low switching frequency modulation. Figure 14b instead deals with the imbalanced condition with $V_{c1} = 100\ V$, $V_{c2} = 70\ V$, and $V_{DC}'' = 100\ V$. Although the NPC dc-bus voltages are imbalanced, the grid current is sinusoidal with a THD as low as 1.5%. In this case, the TLI not only works as an active filter but also as a voltage imbalance compensator. A reduction in the dc voltage generated by PV_1 string is shown in Figure 15a, where V_{c1} is changed from *100 V* to *70 V*. Such an imbalance causes a variation in the peak voltage in the positive half-cycle of V_{jNPC}, but the current is kept sinusoidal by the TLI. Figure 15b deals with power generated by the two PV strings P_{PV1} and P_{PV2} provided by the battery P_{TLI} and the output one P_g. The reduction in V_{c2} causes a reduction in P_{PV2} from *320 W* to *180 W* according to the P–V profile of Figure 10. The same power variation is present in the grid power P_g because the active power produced by the TLI's battery is kept constant. Figure 16 shows a detailed view of the waveforms of V_{aNPC} and i_{ag} in the test

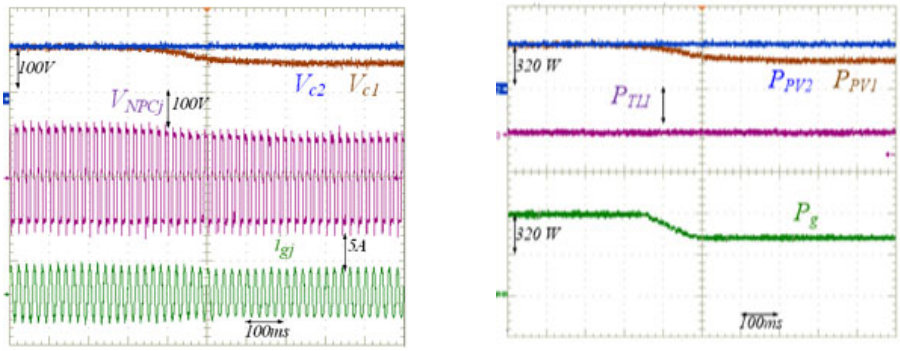
of Figure 15. The TLI compensates for the unbalanced voltages and almost perfectly shapes the grid current.

A further test was performed dealing with battery current control, as shown in Figure 17, dealing with battery current, voltages V_{c1} and V_{c2}, and grid current. The voltages are kept balanced at $V_{c1} = 100\ V$ and $V_{c2} = 100\ V$, while the battery current is changed from $-3A$ to $2A$. Hence, the battery is first discharged and then charged. A negative battery current means that the battery feeds power P_{batt} to the grid according to Figure 17. Vice-versa, a positive battery current means that the battery is charged from the grid. The harmonic spectrum of the grid current at a rated load is shown in Figure 18, fully complying with the IEC 61000-3-2 standard on power quality.



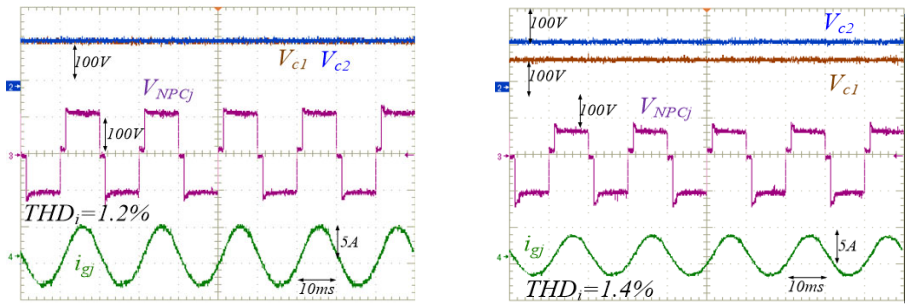
(**a**) (**b**)

Figure 14. The (3LI + TLI) steady state. (**a**) Balanced voltage, $V_{DC}' = 200\ V$, $V_{c1} = 100\ V$, $V_{c2} = 100\ V$, $V_{DC}'' = V_{DC}'/2 = 100\ V$. (**b**) Unbalanced voltage, $V_{DC}' = 170\ V$, $V_{c1} = 70\ V$, $V_{c2} = 100\ V$, $V_{DC}'' = 100\ V$. Secondary phase voltage V_{sj}, grid phase voltage e_j, grid phase current i_{gj}, and NPC output voltage V_{NPCj}, ($V_g = 150\ V$, 50 Hz, TLI PWM 10 kHz).



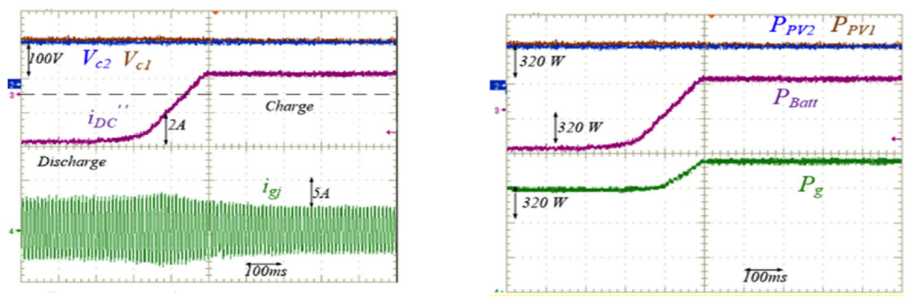
(**a**) (**b**)

Figure 15. The (3LI + TLI) photovoltaic (PV) power variation. (**a**) PV voltages V_{c1} and V_{c2}, NPC output voltage V_{NPCj}, and grid current i_{gj}. (**b**) PV power P_{PV1} and P_{PV2}, TLI output active power P_{TLI}, and grid active power P_g. ($V_g = 150V$, 50Hz $V_{DC}'' = 100\ V$, TLI 10 kHz PWM).



(**a**) (**b**)

Figure 16. The (3LI + TLI) steady state. (**a**) Balanced voltage, $V_{DC}' = 200$ V, $V_{c1} = 100$ V, $V_{c2} = 100$ V, $V_{DC}'' = V_{DC}'/2 = 100$ V. (**b**) Unbalanced voltage, $V_{DC}' = 170$ V, $V_{c1} = 70$ V, $V_{c2} = 100$ V, $V_{DC}'' = 100$ V. Secondary voltage V_{sj}, grid voltage e_j, grid current i_{gj}, and NPC output voltage V_{NPCj} ($V_g = 150$ V, 50 Hz, TLI 10 kHz PWM).



(**a**) (**b**)

Figure 17. The (3LI + TLI) battery current variation from 2*A* to −2*A* with $G_{PV1} \neq G_{PV2}$. (**a**) String voltages V_{c1} and V_{c2}. Battery current i_{DC}''. Grid current i_{gj} (**b**) String power P_{V1}, P_{V2}. Battery power P_{Batt}, grid active power P_g.

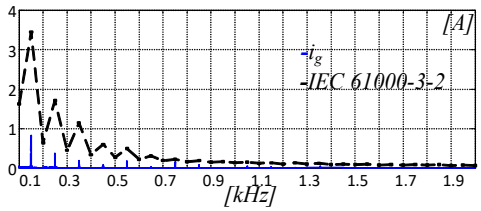


Figure 18. The (3LI + TLI) grid current spectrum vs. IEC 61000-3-2 limits.

6. Power Losses Analysis

A power losses analysis was accomplished by considering the efficiency $\eta_{3LI+TLI}$ of the 3LI + TLI converter and that of the transformer η_{TR}. Hence, the total efficiency is obtained as Equation (9). The efficiency of the converter was estimated by computation of the power devices conduction P_c and the switching P_{sw} losses. According to [29], the 3LI is equipped with a high-voltage and low-frequency IGBT, while a low-voltage, high switching frequency MOSFET is used in the TLI. The main data on these power devices are listed in Tables 9–11. Conduction losses of the IGBT and MOSFET were computed according to Equations (10) and (11), respectively, while switching losses were evaluated by Equation (12) for both power switches. Furthermore, the diodes' reverse recovery power losses are also considered in Equation (13) and were included in the total power losses calculation.

$$\eta_{Tot} = \eta_{3LI+TLI}\eta_{TR} \tag{9}$$

$$P_{c\_MLI} = \delta V_{ce(on)} i_{RMS} \tag{10}$$

$$P_{c\_TLI} = R_{DS(on)} i_{RMS}^2 \tag{11}$$

$$P_{sw} = 0.5 V_{ce} i_{RMS} f_{sw} (t_{rise} + t_{fall}) \tag{12}$$

$$P_D = V_{DR} f_{sw} (t_{rd} i_{RMS} + Q_r) \tag{13}$$

$$\eta_{TR} = \frac{A_n \cos(\varphi)}{A_n \cos(\varphi) + i P_{fen} + P_{cun}/i} \tag{14}$$

where δ is the duty cycle, t_r and t_f are the rise and fall times of the power switches, i_{RMS} is the Root Mean Square (rms) value of the switch current, V_{ce} is the collector-to-emitter voltage, $V_{ce(on)}$ is the collector-to-emitter saturation voltage, $R_{DS(on)}$ is the static drain-to-source on resistance, f_{sw} is the switching frequency, V_{DR} is the diode's reverse voltage, t_{rd} is the diode's reverse recovery time, and Q_r is the reverse recovery charge. The efficiency of the three-phase transformer was computed as a function of iron losses P_{fen}, rated copper losses P_{cun}, power factor cos(φ), rated power A_n, and load coefficient $I = i_g/i_{gn}$, being i_{gn} the rated current of the transformer, Equation (14). Figure 19 shows the conduction and switching losses of the two inverters as a function of the load coefficient i. Specifically, P_{3LI_c} and P_{TLI_c} are the conduction losses of 3LI and TLI, respectively, while P_{3LI_sw} and P_{TLI_sw} are the switching losses, which increase with the load current from 2.6% at $i = 0.1$ to 8% at $i = 1$. The switching power losses of the 3LI are quite low due to the low switching frequency. The total efficiency of the two inverters $\eta_{3LI+TLI}$ and that of the transformer η_{TR} are shown in Figure 20 as function of the load ratio. The peak efficiency of the converter is 98.9% at i = 1, while the minimum is 95.2% at i = 0.2. The efficiency of the transformer, η_{TR}, reaches its peak value of 96.5% for i = 3/4. Finally, the total efficiency was obtained according to Equation (9) and is shown in Figure 20c. It reaches the maximum value of 95% at i = 0.7.

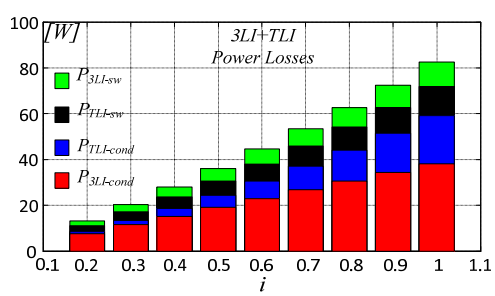


Figure 19. Power losses of 3LI + TLI vs. load current.

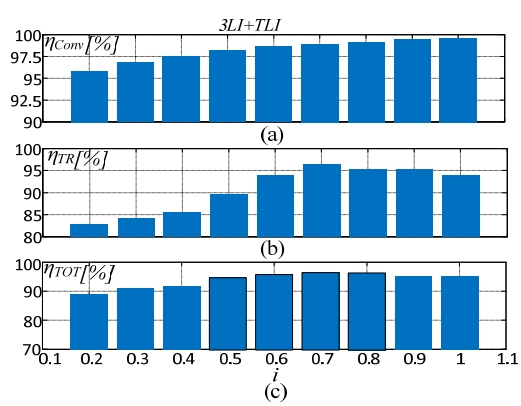


Figure 20. Efficiency vs. load current. (**a**) Three-level inverter (3LI) + TLI efficiency. (**b**) Transformer efficiency. (**c**) Total efficiency.

7. Discussion

Simulation and experimental results confirm that independent management of N-1 power sources and an ESS can be accomplished by using an AHMLI structure composed of a N-level inverter, an open primary winding transformer, and a two-level inverter. This makes unnecessary the introduction of additional dc–dc converters to connect the input ES and the ESS to the grid inverter. Such a structure is also able to compensate for a possible imbalance among the output voltages of energy sources, provided that it does not exceed the dc-bus voltage of the auxiliary TLI. Under this limit, the proposed configuration is also able to cope with a full shut-down of one of the input ESs. Moreover, an independent N-1-channel MPPT can be provided to manage multi-string PV arrays. As proved by experimental tests, the proposed configuration produces an almost perfectly sinusoidal grid current, despite the fact that the main inverter is operated at a low switching frequency in order to improve the efficiency. In fact, the current shaping is accomplished by the auxiliary TLI, which operates at a high switching frequency, but at a remarkably lower dc-bus voltage. This allows us to equip the TLI with fast and powerful MOSFET devices producing low switching and conduction power losses. The efficiency performance of the proposed structure is confirmed by a power losses analysis, which gives global efficiency levels similar to those obtainable with conventional conversion systems for HRESs, but with a more simple and less expensive structure.

8. Conclusions

The goal of this work was to prove that a multi-input conversion system can be constructed from an AHMLI topology exploiting an open-end primary winding transformer. The coherence of such a concept was confirmed first theoretically and then by simulation and experimental tests. Applied to hybrid renewable energy systems exploiting multiple energy sources and an energy storage system, the proposed approach allows us to largely reduce the complexity and cost of the power conversion systems, avoiding the introduction of additional dc–dc converters to interface each energy source with the grid-connected inverter. Further developments of the proposed concept will deal with applications in other sectors, such as electric vehicles and the aerospace industry.

Author Contributions: A.T. and S.F. conceived the original idea. A.T., S.F. and L.D.T. developed the theory and performed the computations. S.D.C., G.S. and M.C. verified the analytical methods. All authors discussed the results and contributed to the final manuscript. All authors have read and agreed to the published version of the manuscript.

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