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Efficient Design Strategy for Optimizing the Settling Time in Three-Stage Amplifiers Including Small- and Large-Signal Behavior

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Abstract: An analytical criterion for the optimization of the small-signal settling time in three-stage amplifiers is carried out. The criterion is based on making equal the two exponential decays of the step response. Including slew-rate effects, a useful design strategy for the design of three-stage operational transconductance amplifier is provided. Extensive time-domain simulations on a transistor-level design in a 65-nm CMOS process confirm the validity of the proposed approach.

Keywords: settling time; design optimization; operational amplifiers; three-stage amplifiers; feedback amplifiers; low-voltage

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1. Introduction

Among the various analog and mixed-signal integrated circuits, the operational transconductance amplifier (OTA) is certainly one of the most fundamental building blocks. Over the past few decades, the approach to their design has changed according to the technological scaling that, in turn, has been driven by the manufacturing processes of integrated circuits (ICs). The lowering of the intrinsic gain in MOS transistors ($g_m r_d \sim 10$), the scaling down of the power supply voltage ($V_{DD} < 1$ V) and the consequent preclusion to the adoption of cascade configurations, moved the interest of the research towards multistage amplifier topologies [1–8]. In this background, the 'speed' of OTAs has been evaluated and compared using the gain-bandwidth product (GBW) as the main performance metric.

In the last 15 years, the extending demand for circuits with fast response to step inputs (i.e., discrete-time or switched-capacitor circuits, data converters, voltage regulators, etc.) has pushed the scientific community towards the design and the optimization of the settling time in low-voltage and multistage CMOS OTAs [9–19]. A significant number of design procedures have been proposed. However, many of them use complex relationships to forecast the settling time from the amplifier parameters, thus becoming unpractical in a real design. Moreover, most of them do not include the slew-rate (SR) limitations that occur under large-signal condition and that, as known, can have a serious impact on the time response.

Since the 1970s, the SR in OTAs has been analyzed in detail [20–27]. However, this specific literature has either produced complex results that did not lead to manageable design equations or provided accurate SR models that were limited to specific topologies.

Recently, in [28], the authors developed an interesting and general approach for the design of three-stage OTAs from settling-time requirements including also SR effects. Although the technique provides accurate results, it relies on the graphical analysis of the contour plots of the so-called Normalized Settling Time (NST) that change with different settling errors. Consequently, no analytical design criterion exists and, if the amplifier is required to settle within a given settling error, a new contour plot must be produced.

In this paper, we provide an analytical design criterion for optimizing the small-signal settling time of a three-stage amplifier, based on making equal the two exponential decays

of the step response. This allows the designer to deal with a well-defined strategy avoiding the generation of contour plots and the design through graphical methods. Moreover, the approach considers large-signal effects since it also includes the slew-rate modeling exploiting the results in [28]. The proposed strategy is used to design a three-stage OTA from settling-time specifications. Extensive time-domain simulations confirm the validity of the proposed design strategy.

2. Settling-Time Modeling in Three-Stage Amplifiers

In this section, we develop a model for the settling time in three-pole amplifiers. First, we model the small-signal settling time in an all-pole amplifier (i.e., the loop gain of the amplifier has no zeros). Then, we propose a new and analytical design criterion to optimize the settling time that is based on making equal the two exponential decays of the step response. Next, we extend this design criterion to practical cases of generic amplifiers with one or more zeros in the transfer function of the open-loop gain. Finally, we extend the settling-time model by including the effects of slew-rate limitations so that we take into account the large-signal behavior, also.

2.1. Modeling of a Pure Three-Pole Amplifier

Pure three-pole amplifiers have no zeros in the transfer function of the open-loop gain. They belong to the class of the all-pole amplifiers and are modeled by

$$T(s) = \beta a(s) = \frac{\beta a_0}{1 + \frac{s}{\omega_d}} \cdot \frac{1}{1 + a_1 s + a_2 s^2} \tag{1}$$

where $a(s)$ is the direct gain of the OTA, β is the feedback factor, $a_0 = a(0)$ is the dc gain, ω_d is the frequency of the dominant pole and where coefficients a_1 and a_2 represent the non-dominant poles, in general, complex-conjugate. As long as $\beta a_0 \gg 1$, the significant range of frequencies lies for $\omega \gg \omega_d$ and the dc gain with the dominant pole simplify into

$$\frac{\beta a_0}{1 + \frac{s}{\omega_d}} \approx \frac{1}{s/\mathrm{GBW}} \tag{2}$$

where $\mathrm{GBW} = \beta a_0 \omega_d$ stands for the gain-bandwidth product of the amplifier. Hence the open-loop gain is

$$T(s) = \frac{1}{\frac{s}{\mathrm{GBW}}(1 + a_1 s + a_2 s^2)}. \tag{3}$$

As explained in [29], the non-dominant poles in (3) arise because of an *internal feedback loop* nested in the main (external) loop. This situation is represented in Figure 1a where the stage of the internal loop is made up of an inner amplifier characterized by an internal gain-bandwidth product, GBW_i, and by an internal non-dominant pole, ω_s.

Manipulating the internal feedback loop in Figure 1a we obtain the equivalent block schematic in Figure 1b, where the inner stage is expressed in terms of the internal gain-bandwidth product and of the *internal separation factor*, $K_i = \omega_s/\mathrm{GBW}_i$. This latter parameter is accountable for the stability of the internal loop (i.e., in a two-pole amplifier, the separation factor impacts on the phase margin as $K \approx \tan(\mathrm{PM})$ and, in this specific case, the internal separation factor affects the internal phase margin, only). As a rule of thumb, we can assume that the minimum separation factor required for stabilizing the inner stage is $K_i = 1$ [30].

For $K_i > 1$ the inner stage is stable and, at a coarse but functional approximation, we can disregard the term $s^2/(\omega_s^2 K_i)$ in the 'non-dominant poles' block in Figure 1b. Consequently, the whole amplifier stability depends on the ratio between the overall second pole, GBW_i, and the gain-bandwidth product, GBW, i.e., on the *external separation factor*, defined as $K_e = \mathrm{GBW}_i/\mathrm{GBW}$.

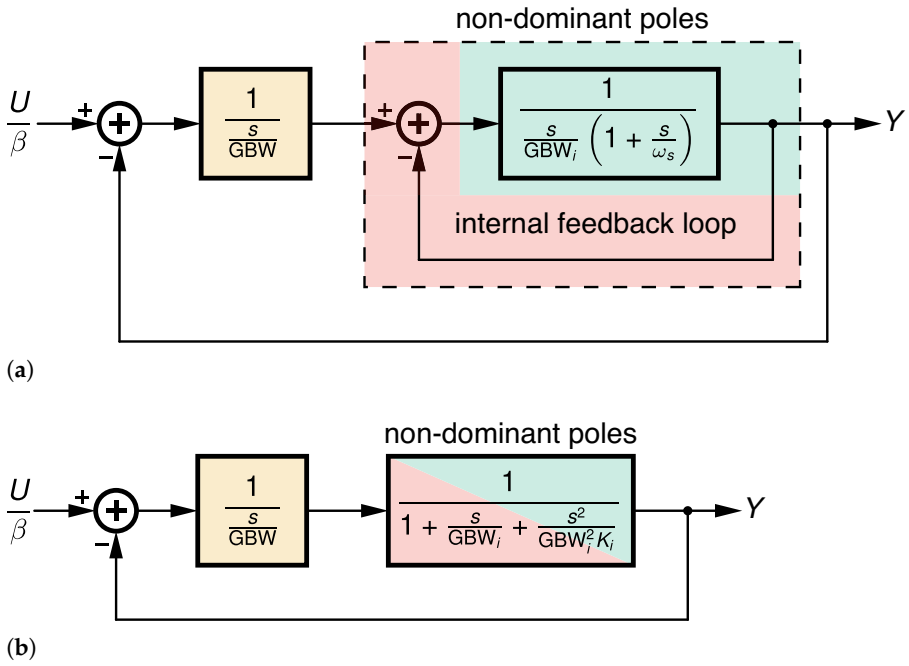


Figure 1. Block schematic modeling of a pure three-pole amplifier. (**a**) The non-dominant poles are due to an inner amplification stage fed back by a local loop. (**b**) The transfer function that models the non-dominant poles is that of a closed-loop feedback amplifier.

Using the two separation factors, the open-loop gain becomes

$$T(s) = \frac{1}{\frac{s}{\mathrm{GBW}}\left(1 + \frac{s}{K_e \mathrm{GBW}} + \frac{s^2}{K_e^2 K_i \mathrm{GBW}^2}\right)} \tag{4}$$

and, if $T(s)$ has the form expressed in (3), we can evaluate

$$K_e = \frac{1}{a_1 \mathrm{GBW}}, \tag{5a}$$

$$K_i = \frac{a_1^2}{a_2}. \tag{5b}$$

Normalizing the complex frequency with respect to the GBW we obtain a dimensionless version of the transfer function that allows analysis of the time response of the amplifier in a very convenient manner. To do so, we define the dimensionless frequency as $\hat{s} = s/\mathrm{GBW}$ and the corresponding dimensionless time as $\hat{t} = \mathrm{GBW} \cdot t$ so that the open-loop transfer function turns into

$$T(\hat{s}) = \frac{1}{\hat{s}\left(1 + \frac{\hat{s}}{K_e} + \frac{\hat{s}^2}{K_e^2 K_i}\right)}. \tag{6}$$

When the system (6) is closed in a feedback loop, its response to a unity step input is a function of the dimensionless time, $\hat{t}$, and of the separation factor vector, $\mathbf{K} = (K_e, K_i)$, i.e., $y = y(\hat{t}, \mathbf{K})$. From the output response, $y(\hat{t}, \mathbf{K})$ we can evaluate the *dynamic settling error* (DSE)

$$\mathrm{DSE}(\hat{t}, \mathbf{K}) = \frac{y(\infty) - y(\hat{t}, \mathbf{K})}{y(\infty)} \tag{7}$$

and the dimensionless settling time as

$$\hat{t}_s(\epsilon, \mathbf{K}) = \min\left\{\hat{t}^\star : \left|\mathrm{DSE}(\hat{t}, \mathbf{K})\right| \leq \epsilon \; \forall \, \hat{t} \geq \hat{t}^\star\right\} \tag{8}$$

being ϵ, the *accuracy level*. Therefore, the final settling-time results

$$t_s = \frac{\hat{t}_s(\epsilon, \mathbf{K})}{\text{GBW}}. \tag{9}$$

From (9) it is apparent that minimizing the small-signal settling time means both maximizing the GBW and minimizing the quantity $\hat{t}_s(\epsilon, \mathbf{K})$ by a proper optimization of the separation factor vector, $\mathbf{K}$. Since the maximization of the GBW is a straightforward task, we must find a criterion for the optimization of the dimensionless settling time, $\hat{t}_s(\epsilon, \mathbf{K})$.

In the following, to compare different settling-times at different accuracy levels, ϵ, it is convenient to use the Normalized Settling Time (NST). This is defined as the settling time of the amplifier under test normalized with respect to the settling time of a single-pole amplifier with the same GBW. In a single-pole amplifier, the settling time is $t_{s(\text{sp})} = |\ln \epsilon|/\text{GBW}$, therefore the normalized settling-time results in

$$\text{NST} = \frac{\text{GBW}}{|\ln \epsilon|} t_s = \frac{\hat{t}_s}{|\ln \epsilon|} \tag{10}$$

where the latter equivalence was derived from (9).

2.2. Optimization of the Dimensionless Settling Time

In a third-order system, the response to a unity step input in the time-domain takes the form

$$y(t) = 1 + A_1 \mathrm{e}^{-\alpha_1 t} + A_2 \mathrm{e}^{-\alpha_2 t} \left[\cos(\omega t) + \frac{\beta - \alpha_2}{\omega} \sin(\omega t) \right] \tag{11}$$

whose corresponding Laplace transform is

$$Y(s) = \frac{1}{s} + A_1 \frac{1}{s + \alpha_1} + A_2 \frac{s + \beta}{(s + \alpha_2)^2 + \omega^2}. \tag{12}$$

If the residues A_1 and A_2 are in the same order of magnitude, we may assume that the behavior of the amplifier's time response is mainly ruled by the two exponential decays, α_1 and α_2. Therefore, a design criterion for optimizing the amplifier speed is to set equal the two exponential decays so that $\alpha = \alpha_1 = \alpha_2$. In this way none of the exponential terms will be responsible for slowing down the time response. As known, the two exponential decays depend on the poles of the closed-loop transfer function, $G(s) = sY(s)$, whose denominator is

$$D(s) = (s + \alpha) \left[(s + \alpha)^2 + \omega^2 \right] = s^3 + 3\alpha s^2 + \left(3\alpha^2 + \omega^2 \right) s + \alpha \left(\alpha^2 + \omega^2 \right). \tag{13}$$

Using (4), the closed-loop gain is

$$G(s) = \frac{T(s)}{1 + T(s)} = \frac{K_e^2 K_i \text{GBW}^3}{s^3 + K_e K_i \text{GBW} s^2 + K_e^2 K_i \text{GBW}^2 s + K_e^2 K_i \text{GBW}^3} \tag{14}$$

and, equating the coefficients of the denominator of (14) to the coefficients of (13), we obtain the system of equations

$$K_e K_i \text{GBW} = 3\alpha, \tag{15a}$$

$$K_e^2 K_i \text{GBW}^2 = \alpha^2 \left[3 + \left(\frac{\omega}{\alpha} \right)^2 \right], \tag{15b}$$

$$K_e^2 K_i \text{GBW}^3 = \alpha^3 \left[1 + \left(\frac{\omega}{\alpha} \right)^2 \right]. \tag{15c}$$

Manipulating (15) we obtain the constraint that set equal the two exponential decays in terms of K_e and K_i

$$K_e K_i - 3 - \frac{2}{9} K_e K_i^2 = 0 \tag{16}$$

or, relating K_e in terms of K_i,

$$K_e = \frac{3}{K_i\left(1 - \frac{2}{9}K_i\right)} \tag{17}$$

whose plot is reported in Figure 2. Observe that since the condition in (16) is independent of the GBW, it represents a design criterion for the optimization of the dimensionless settling time, $\hat{t}_s$.

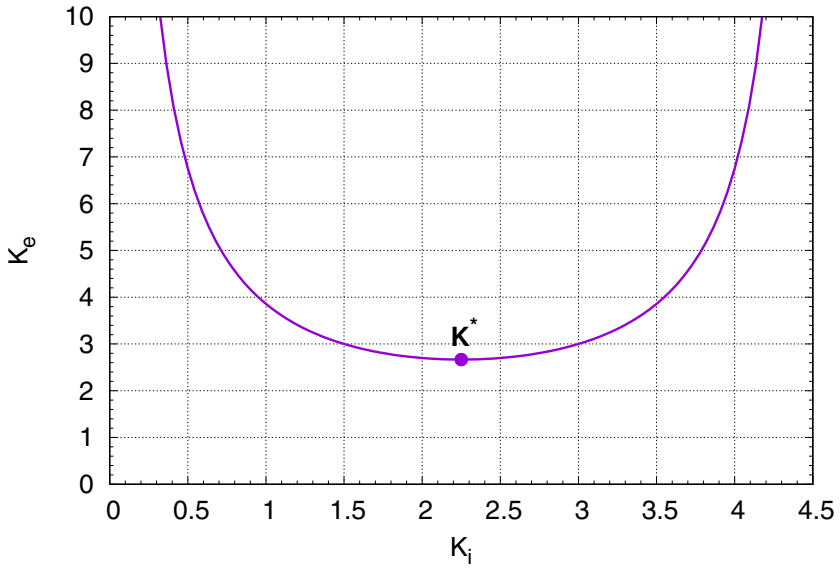


Figure 2. Plot of K_e versus K_i for making the same exponential decay in the time response to a step input. The optimum bias point is for $\mathbf{K}^\star = (9/4, 8/3)$.

Among the possible constraints set by (16), the most convenient is represented by the point $\mathbf{K}^\star$ in Figure 2, placed at the minimum value of K_e. Using (17) to find this minimum yields

$$\mathbf{K}^\star = (K_e^\star, K_i^\star) = \left(\frac{8}{3}, \frac{9}{4}\right). \tag{18}$$

The plot of the phase margin, PM, versus K_i for an ideal three-pole system designed with the constraint in (16) is shown in Figure 3. The point $\mathrm{PM}^\star = 68.4$ deg identifies the phase margin observed at the optimum bias point set by $(K_e^\star, K_i^\star) = (8/3, 9/4)$.

To further demonstrate the goodness of our design criterion, in Figure 4 we plot the normalized settling time, NST, versus the internal separation factor, K_i, for a three-pole system designed with the constraint in (16) and for different accuracy levels, ϵ. The colored spots, all at the point of abscissa $K_i^\star = 9/4$, identify the normalized settling-times observed at the optimum bias point. Even if the proposed criterion does not identify the absolute minimum settling time, a satisfactorily settling time is established in a very simple manner. This is more evident considering that as reported in [29], a circuit designed for obtaining the minimum possible settling time always deviates from its target when unavoidable statistical variations of process or design parameters are taken into account.

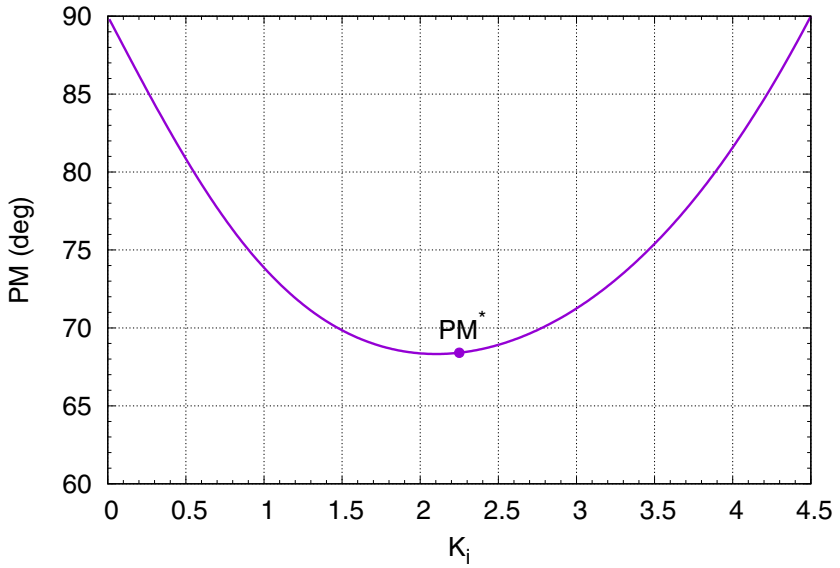


Figure 3. Plot of the phase margin, PM, versus the internal separation factor, K_i, for a three-pole system designed with the constraint in (16). The point PM$^\star = 68.4$ deg identifies the phase margin observed at the optimum bias point set by $(K_e^\star, K_i^\star) = (8/3, 9/4)$.

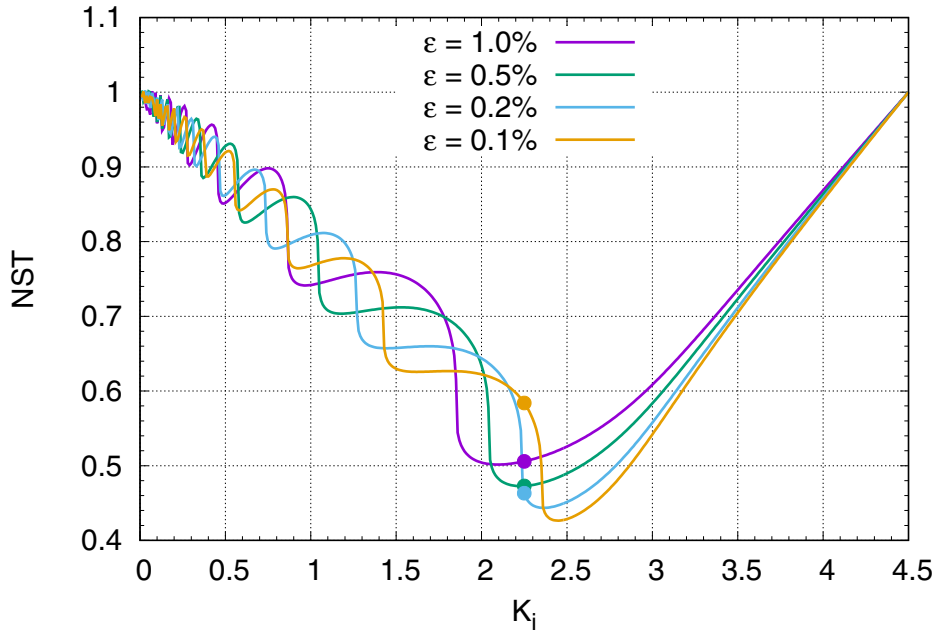


Figure 4. Plot of the normalized settling time, NST, versus the internal separation factor, K_i, for a three-pole system designed with the constraint in (16) and for different accuracy levels, ϵ. Colored spots identify the normalized settling-times observed at the optimum bias point set by $(K_e^\star, K_i^\star) = (8/3, 9/4)$.

2.3. Extension to Generic Three-Pole Amplifiers

A generic three-pole amplifier has one or two zeros in the loop gain, i.e.,

$$T(s) = \frac{1 + b_1 s + b_2 s^2}{\frac{s}{\mathrm{GBW}}(1 + a_1 s + a_2 s^2)}. \tag{19}$$

As demonstrated in [28] and briefly reported in Appendix A, if the frequency of the GBW lies below the zeros of $T(s)$, two *global separation factors* can be introduced

$$\hat{K}_e = \frac{(1 + b_1\mathrm{GBW})^2}{a_1\mathrm{GBW} + b_2\mathrm{GBW}^2}, \tag{20a}$$

$$\hat{K}_i = \frac{\left(a_1\mathrm{GBW} + b_2\mathrm{GBW}^2\right)^2}{a_2\mathrm{GBW}^2(1 + b_1\mathrm{GBW})}. \tag{20b}$$

The global separation factors can be used to make the condition of a time response with two equal exponential decays. More specifically, the dimensionless settling time of the generic three-pole amplifier is optimized by setting $\hat{K}_e$ and $\hat{K}_i$ to the same values that we would choose for the pure three-pole amplifier, i.e., setting $\hat{K}_e = K_e^\star = 8/3$ and $\hat{K}_i = K_i^\star = 9/4$.

To verify the correctness of our approach, we designed the ideal amplifier in Figure 5 making $\hat{K}_e = 8/3$ and $\hat{K}_i = 9/4$ and compared its time response to that of an ideal pure three-pole amplifier with the same GBW and designed with $K_e = 8/3$ and $K_i = 9/4$. We expect similar behaviors, i.e., very small NSTs, in the interval 0.4–0.6, for both circuits.

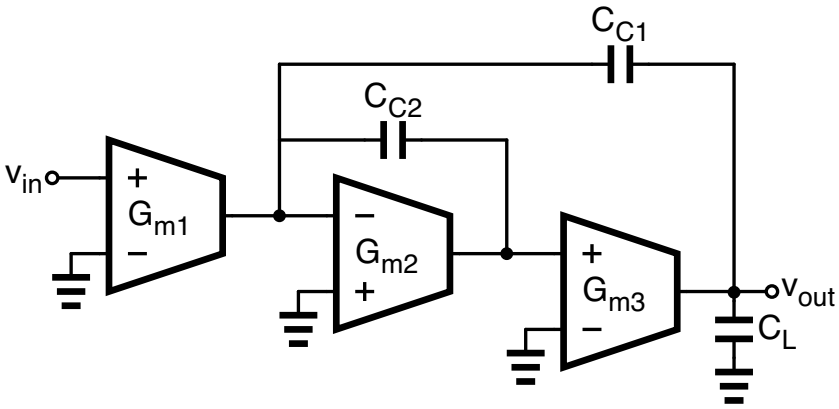


Figure 5. Block schematic of a three-stage amplifier. Capacitors C_{C1} and C_{C2} perform the Reversed Nested-Miller Compensation (RNMC).

The amplifier in Figure 5 exploits the well-known Reversed Nested-Miller Compensation (RNMC) for which the coefficients of the transfer function in (19) are

$$\mathrm{GBW} = \frac{G_{\mathrm{m1}}}{C_{\mathrm{C1}}}, \tag{21a}$$

$$a_1 = \frac{C_{\mathrm{L}}C_{\mathrm{C2}}}{C_{\mathrm{C1}}G_{\mathrm{m3}}} + \frac{C_{\mathrm{C2}}}{G_{\mathrm{m3}}} - \frac{C_{\mathrm{C2}}}{G_{\mathrm{m2}}}, \tag{21b}$$

$$a_2 = \frac{C_{\mathrm{C2}}C_{\mathrm{L}}}{G_{\mathrm{m2}}G_{\mathrm{m3}}}, \tag{21c}$$

$$b_1 = -\frac{C_{\mathrm{C2}}}{G_{\mathrm{m2}}}, \tag{21d}$$

$$b_2 = -\frac{C_{\mathrm{C1}}C_{\mathrm{C2}}}{G_{\mathrm{m2}}G_{\mathrm{m3}}}. \tag{21e}$$

In our design, we assumed that the amplifier required a GBW of 100 Mrad/s (about 15.5 MHz) for driving a load capacitor $C_{\mathrm{L}} = 2\,\mathrm{pF}$. Supposing that $G_{\mathrm{m1}} = 100\,\mu\mathrm{A/V}$ was set by noise specifications, from (21a) we obtained $C_{\mathrm{C1}} = 1\,\mathrm{pF}$. Then we substituted (21) into (20) and finalized our design by solving for $(\hat{K}_e, \hat{K}_i) = (8/3, 9/4)$. The procedure led to $C_{\mathrm{C2}} = 1.1\,\mathrm{pF}$ and $G_{\mathrm{m2}} = G_{\mathrm{m3}} = 752\,\mu\mathrm{A/V}$. The time response of this 'generic amplifier' is depicted in Figure 6. For an effective comparison, the time response of a 'pure three-pole

amplifier' with the same GBW is depicted also. It is observed a good matching between the two curves.

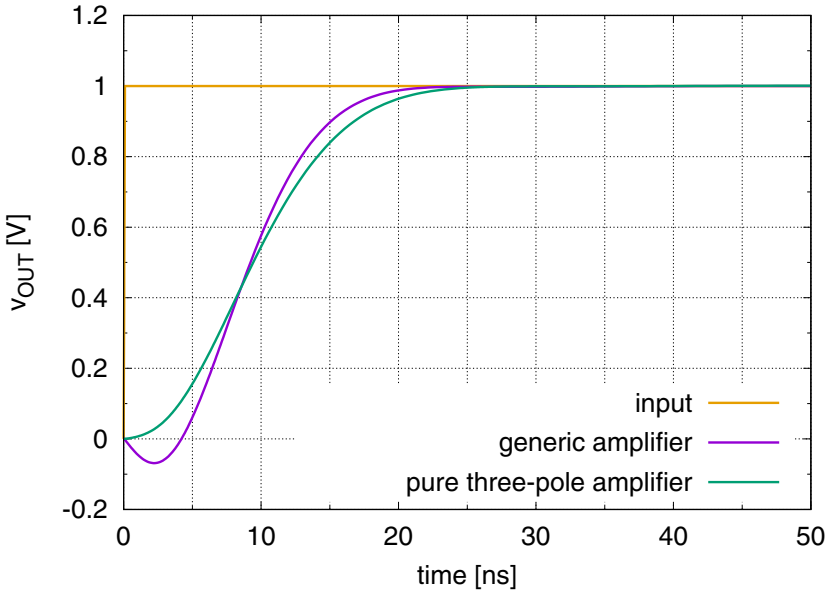


Figure 6. Time-domain behavior of two three-pole amplifiers in response to a unity step input. The two amplifiers are designed with the same GBW and separation factors.

The details, in terms of settling time and NST, are reported in Table 1 for the two amplifiers. As expected, the approach for the optimization of the 'generic amplifier' produces a time response nearly as fast as the time response of the pure three-pole one.

Table 1. Evaluation of the settling time, t_s, for the generic amplifier and for the pure three-pole amplifier, at different accuracy levels. The amplifiers are designed setting $\hat{K}_e = 8/3$ and $\hat{K}_i = 9/4$. The NST is also reported for an effective comparison.

ϵ %	Generic Amplifier t_s (ns) (NST [–])	Pure Three-Pole Amplifier t_s (ns) (NST [–])
1.0	20.4 (0.44)	23.5 (0.51)
0.5	21.8 (0.41)	25.3 (0.48)
0.2	30.4 (0.49)	29.2 (0.47)
0.1	35.8 (0.52)	40.4 (0.58)

2.4. Extension to Slew-Rate Modeling

Slew-rate effects in operational amplifiers can be included using the simple model introduced in [31] and analyzed in detail in [28].

The model assumes that the slew-rate limitation is in the first stage of the amplifier and, in particular, that it depends on the capacitor that determines the dominant pole. If this assumption is not satisfied, the amplifier can experience a positive feedback connection during its slewing period that degrades its speed performance and results in an inefficient design. In a good design, this inefficiency must be avoided either using slew-rate enhancers or class-ab topologies [30,32,33] in the stages placed after the first one.

As a second constraint, the model assumes that the amplifier is designed so to exhibit NST ≤ 1 in small-signal condition. In our case, this simply means that the amplifier can be designed in the optimum bias point set by $(\hat{K}_e, \hat{K}_i) = (8/3, 9/4)$.

If the two assumptions described above are satisfied, the dimensionless settling time of the amplifier is bounded by

$$\hat{t}_s \leq \begin{cases} |\ln \epsilon| & \text{for } \left|\frac{\Delta Y}{\nu}\right| < 1 \\ |\ln \epsilon| + \frac{\Delta Y}{\nu} - \left(1 + \ln \frac{\Delta Y}{\nu}\right) & \text{for } \left|\frac{\Delta Y}{\nu}\right| \geq 1 \end{cases} \tag{22}$$

where ΔY is the output step voltage of the amplifier and

$$\nu = \frac{I_{o1}}{\beta G_{m1}} \tag{23}$$

defines the *equivalent saturation limit* of the first stage, expressed in terms of its maximum short-circuit output current, I_{o1}, of its small-signal transconductance, G_{m1}, and of the overall feedback factor, β.

Also, in this case, to compare different settling-times at different accuracy levels, ϵ, we can define the NST by normalizing the settling time of the amplifier under test with respect to the *small-signal* settling time of a single-pole amplifier with the same GBW. From this definition and considering (10), the NST comes from dividing (22) by $|\ln \epsilon|$, i.e.,

$$\text{NST} \leq \begin{cases} 1 & \text{for } \left|\frac{\Delta Y}{\nu}\right| < 1 \\ 1 + \frac{\frac{\Delta Y}{\nu} - \left(1 + \ln \frac{\Delta Y}{\nu}\right)}{|\ln \epsilon|} & \text{for } \left|\frac{\Delta Y}{\nu}\right| \geq 1 \end{cases}. \tag{24}$$

3. The Design Strategy with Settling-Time Constraints

In this section, we propose a design strategy based on settling-time constraints. It relies on two design equations. The first design equation is represented by the system in (20) and refers to the small-signal behavior. Using this system of equations, we guarantee that the small-signal settling time of the amplifier is less than (or comparable to) the settling time of a single-pole amplifier with the same GBW.

The second design equation stems from the dimensionless settling time in (22) and accounts for the large-signal effects in terms of slew-rate. Considering that $\hat{t}_s = \text{GBW} \cdot t_s$, the settling-time constraint allows us to dimension the GBW from

$$\text{GBW} = \frac{|\ln \epsilon| + \frac{\Delta Y}{\nu} - \left(1 + \ln \frac{\Delta Y}{\nu}\right)}{t_s}, \tag{25}$$

where the maximum possible value for $\Delta Y/\nu$ must be considered. Considering (23) we obtain that

$$\frac{\Delta Y}{\nu} = \beta \frac{G_{m1}}{I_{o1}} \Delta Y. \tag{26}$$

The feedback factor, β, is a parameter that is specified by the application and cannot be freely chosen by the designer. In some particular cases the feedback factor can be programmed in a range of values (i.e., in switched-capacitor circuits, β can be selected by changing the connections of a proper array of capacitors) so that $\beta = \beta_{max}$ must be considered in the design equation.

Concerning the ratio G_{m1}/I_{o1}, it depends on the quiescent point of the first stage and, in the common case of a CMOS source coupled differential pair, it is

$$\frac{G_{m1}}{I_{o1}} = \frac{\Gamma}{2}, \tag{27}$$

where Γ is the g_m-over-I_D ratio of the input transistors [34]. The plot of the g_m-over-I_D versus the gate-source overdrive is reported in Figure 7 for two complementary devices

of a 65-nm CMOS process. Other nanometer CMOS processes have similar plots with no practical differences compared to the curves in Figure 7 [35]. Since, in the analog design context, transistors are biased so that $V_{GS} \sim V_{TH}$, the choice of the g_m-over-I_D ratio has a limited range (typically, $8\,V^{-1} \leq \Gamma \leq 16\,V^{-1}$).

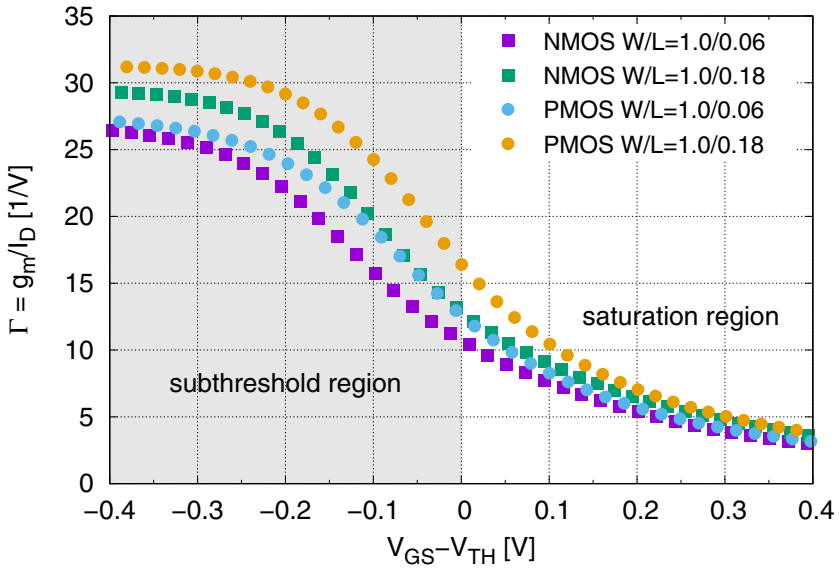


Figure 7. Plot of the g_m-over-I_D ratio versus V_{GS}–V_{TH} for two standard-threshold complementary devices of a 65-nm CMOS process. The plots for two different channel lengths are shown. The darker area identifies the subthreshold region. The lighter one, identifies the saturation region.

Finally, for the maximum output step, ΔY, we can consider the highest possible value set by the power supply, V_{DD}.

From all these considerations, based on the required settling time, the GBW is dimensioned according to

$$\mathrm{GBW} = \frac{|\ln \epsilon| + \beta\frac{\Gamma}{2}V_{DD} - \left[1 + \ln\left(\beta\frac{\Gamma}{2}V_{DD}\right)\right]}{t_s}. \tag{28}$$

The draft of the proposed design strategy is reported in the flow-chart in Figure 8. More specifically, once that the GBW is determined based on the settling time specification, the designer has two design equations that allows him to set two suitable parameters of the OTA. The remaining parameters can be chosen freely or based on other constraints set by noise, power dissipation or other critical figures of merit that, in general, depend on the application or on the amplifier topology.

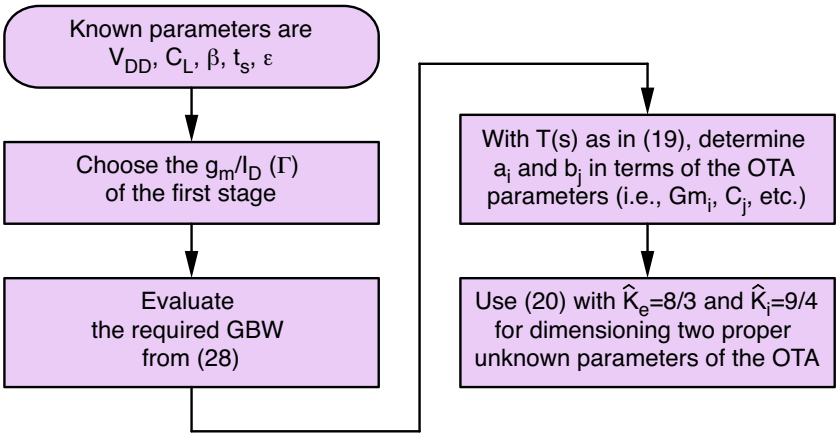


Figure 8. Flow-chart of the proposed design strategy.

4. Design Example and Validation

To demonstrate and confirm the proposed design strategy, we apply it to the design of an appropriate three-stage OTA for the switched-capacitor (SC) application depicted in Figure 9.

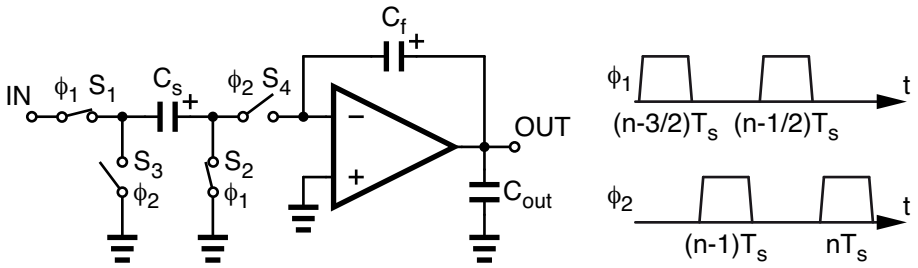


Figure 9. Forward-Euler SC integrator.

Here the circuit acts as a forward-Euler SC integrator and, assuming T_s is the sampling period, it works as follows. During the sampling phase, ϕ_1 at time $t = (n-1/2)T_s$, switches S_1 and S_2 close, the sampling capacitor, C_s, charges at the input voltage, v_{IN}, while the feedback capacitor, C_f, maintains the charge processed at the previous time, $t = (n-1)T_s$. During the evaluation phase, ϕ_2 at time $t = nT_s$, the sampling capacitor, C_s, discharges through the virtual ground node and transfers its charge to capacitor C_f, thus updating the output. The charge balance is represented by $\Delta Q_{C_s} = \Delta Q_{C_f}$ and leads to

$$v_{\mathrm{OUT}}(n) = v_{\mathrm{OUT}}(n-1) + \frac{C_s}{C_f} v_{\mathrm{IN}}(n-1/2), \tag{29}$$

where we omitted the obvious dependance on the sampling period, T_s, and used the equivalence $v_{\mathrm{OUT}}(n-1/2) = v_{\mathrm{OUT}}(n-1)$.

During the sampling phase, ϕ_1, the OTA does not change its output and remains in the 'hold' condition. During the evaluation phase, ϕ_2, the output is fed back to the inverting terminal by the voltage divider composed by C_f and C_s so that the OTA experiences a feedback factor $\beta = C_f/(C_s + C_f)$. At the same time, the OTA is loaded by an equivalent capacitor given by $C_{\mathrm{L}} = C_{\mathrm{out}} + C_s C_f/(C_s + C_f)$. These two parameters shall be considered during the design of the OTA.

In our design example, we assume that the capacitors of the integrator in the figure are $C_s = C_f = C_{\mathrm{out}} = 0.4\,\mathrm{pF}$. Therefore, the OTA has to be designed considering $C_{\mathrm{L}} = 0.6\,\mathrm{pF}$ and $\beta = 0.5$. We assume that the integrator operates with a sampling frequency of 25 MHz and that the target settling time is 20 ns within a 0.5% error. The power supply is $V_{\mathrm{DD}} = 1\,\mathrm{V}$.

We apply the design strategy to the transistor-level amplifier in Figure 10 made up of a differential pair (M1–M5) and two common-source stages (M6–M7 and M8–M9). The compensation is achieved through capacitors C_{C1} and C_{C2}, using a modified Reverse Nested-Miller Compensation, named RNMC-ICBFF. More specifically, capacitor C_{C2} is connected between the output and the input nodes of the second stage. Capacitor C_{C1} is connected between the output of the third stage and the input of the second one. In this latter connection the mandatory signal inversion is accomplished through the Inverting Current Buffer (ICB) made up of the current mirror M3–M4. Transistor M9, which provides the bias current to the third stage, acts also as a feed-forward (FF) stage, G_{mf}.

The slew-rate enhancer, M10, is added in parallel to M9 to improve the SR performance at the output node during negative steps. Since M10 is a high-threshold transistor, it is normally off in bias condition. When node v_2 goes high and M8 switches off, M10 switches on and sinks the extra current required by the load.

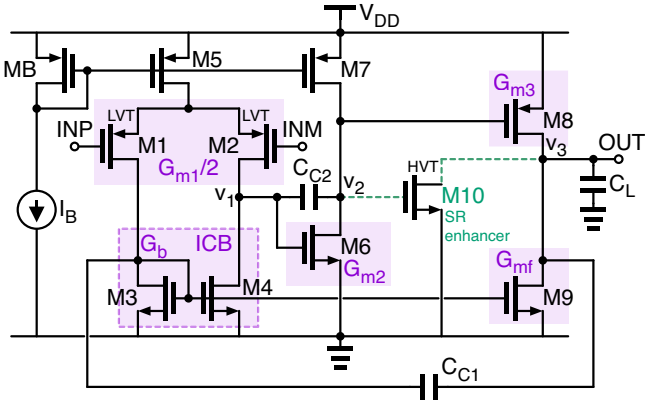


Figure 10. Transistor-level schematic of a three-stage OTA compensated with the Reversed Nested-Miller Compensation with Inverse Current Buffer and Feed-Forward stage (RNMC-ICBFF).

Using the equivalent block schematic in Figure 11, we evaluate the open-loop transfer function of the amplifier. Neglecting the contributions of transconductors' output resistances and parasitic capacitors, it takes the form in (19) where

$$\mathrm{GBW} = \frac{\beta G_{\mathrm{m1}}}{C_{\mathrm{C1}}}, \tag{30a}$$

$$a_1 = \frac{C_{\mathrm{C2}}}{G_{\mathrm{m3}}}\left(1 - \frac{G_{\mathrm{m3}}}{G_{\mathrm{m2}}} + \frac{C_{\mathrm{L}}}{C_{\mathrm{C1}}} + \frac{G_{\mathrm{mf}}}{G_{\mathrm{b}}}\right), \tag{30b}$$

$$a_2 = \frac{C_{\mathrm{C2}}C_{\mathrm{L}}}{G_{\mathrm{m3}}G_{\mathrm{b}}}, \tag{30c}$$

$$b_1 = \frac{C_{\mathrm{C1}}}{2G_{\mathrm{b}}} + \left(\frac{G_{\mathrm{mf}}}{2G_{\mathrm{b}}} - \frac{G_{\mathrm{m3}}}{G_{\mathrm{m2}}}\right)\frac{C_{\mathrm{C2}}}{G_{\mathrm{m3}}}, \tag{30d}$$

$$b_2 = -\frac{C_{\mathrm{C1}}C_{\mathrm{C2}}}{2G_{\mathrm{b}}G_{\mathrm{m3}}}\left(1 + \frac{G_{\mathrm{m3}}}{G_{\mathrm{m2}}}\right). \tag{30e}$$

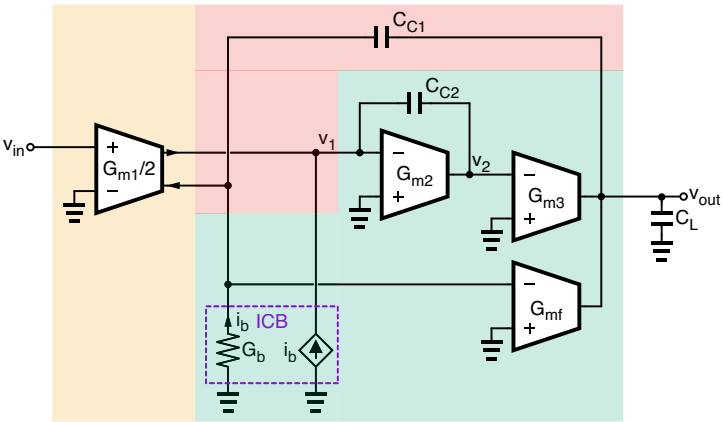


Figure 11. Block schematic of a three-stage OTA compensated with the Reversed Nested-Miller Compensation with Inverse Current Buffer and Feed-Forward stage (RNMC-ICBFF). Referring to the block schematic in Figure 1a, we can identify (1) the block responsible for the dominant pole and the GBW of the amplifier (light-yellow area); (2) the internal block with two real poles (light-green area); (3) the internal feedback across the internal block (light-red area). The overall feedback that will connect the output v_{out} to the input v_{in} is not drawn.

For the input transistors of the differential pair we choose $\Gamma = 16\,\mathrm{V}^{-1}$ and, just for simplifying the design, the same value is adopted for the g_m-over-I_D of all the remaining transistors of the amplifier. Then, using (28), we obtain the minimum required GBW of 55 MHz. Observe that, in case of nanometer technologies, due to the low transistor intrinsic

gain ($g_m r_d \sim 10$), Equation (30a) overestimates the actual GBW that, in this specific case, is better approximated by

$$\text{GBW} = \frac{\beta G_{\text{m1}}}{C_{\text{C1}}} \cdot \frac{1}{1 + \frac{C_{\text{C2}}/C_{\text{C1}}}{G_{\text{m3}} R_{\text{o3}}}}, \tag{31}$$

being R_{o3} the output resistance of the third stage. To make up for this error, which can be as high as 20%, we dimension the GBW by increasing the value obtained from (28) by 20%. Hence, we consider GBW = 66 MHz in our design equations.

The condition of making the same g_m-over-I_D ratio implies that transistors that share the same current have the same transconductance or, in other words, that $G_{\text{b}} = G_{\text{m1}}$ and $G_{\text{m3}} = G_{\text{mf}}$. Therefore, defining

$$n = \frac{G_{\text{m3}}}{G_{\text{m2}}}, \tag{32}$$

$$m = \frac{G_{\text{mf}}}{G_{\text{b}}} = \frac{G_{\text{m3}}}{G_{\text{m1}}}, \tag{33}$$

$$T = \frac{C_{\text{C2}}}{G_{\text{m3}}}\text{GBW}, \tag{34}$$

$$\chi = \frac{C_{\text{L}}}{C_{\text{C1}}}, \tag{35}$$

we write the following normalized coefficients

$$a_1\text{GBW} = (1 - n + m + \chi)T, \tag{36a}$$

$$a_2\text{GBW}^2 = \beta\chi T, \tag{36b}$$

$$b_1\text{GBW} = \frac{\beta}{2} - \left(n - \frac{m}{2}\right)T, \tag{36c}$$

$$b_2\text{GBW}^2 = -\frac{\beta}{2}(1 + n)T, \tag{36d}$$

that can be substituted in (20) to obtain

$$\hat{K}_e = \frac{(1 + b_1\text{GBW})^2}{a_1\text{GBW} + b_2\text{GBW}^2} = \frac{\left[1 + \frac{\beta}{2} - \left(n - \frac{m}{2}\right)T\right]^2}{\left[1 - n + m + \chi - \frac{\beta}{2}(1 + n)\right]T}, \tag{37a}$$

$$\hat{K}_i = \frac{\left(a_1\text{GBW} + b_2\text{GBW}^2\right)^2}{a_2\text{GBW}^2(1 + b_1\text{GBW})} = \frac{\left[1 - n + m + \chi - \frac{\beta}{2}(1 + n)\right]^2 T}{\beta\chi\left[1 + \frac{\beta}{2} - \left(n - \frac{m}{2}\right)T\right]} \tag{37b}$$

where $\hat{K}_e = 8/3$ and $\hat{K}_i = 9/4$.

Setting different values for n and m, we use MATLAB to solve (37) for T and χ and to evaluate the remaining amplifier parameters from

$$C_{\text{C1}} = \frac{C_{\text{L}}}{\chi}, \tag{38a}$$

$$G_{\text{m1}} = G_{\text{b}} = \frac{C_{\text{C1}}}{\beta}\text{GBW}, \tag{38b}$$

$$G_{\text{m3}} = G_{\text{mf}} = mG_{\text{m1}}, \tag{38c}$$

$$G_{\text{m2}} = \frac{G_{\text{m3}}}{n}, \tag{38d}$$

$$C_{\text{C2}} = \frac{T}{\text{GBW}}G_{\text{m3}}. \tag{38e}$$

The results of the dimensioning procedure are reported in Table 2 for different values on n and m. The table reports also the estimated current dissipation of the OTA as $I_{DD} = (2G_{m1} + G_{m2} + G_{m3})/\Gamma$, the Figure-of-Merit (FOM) that computes the speed-dissipation-load trade-off as FOM $=$ GBW $\cdot\, C_L/(V_{DD} \cdot I_{DD})$ and, neglecting the flicker noise for the sake of simplicity, the square root of the input noise spectral density, estimated as $S_n = 2 \cdot 4KT(2/3)(1/G_{m1})(1 + G_{m1}/G_b)$. As it can be observed, if the noise is satisfactorily to our application, the best choice in terms of current dissipation and FOM is the design corresponding to the row with $n = 1$ and $m = 4$.

Table 2. Results of the dimensioning procedure.

n –	m –	G_{m1},G_b (μA/V)	G_{m2} (μA/V)	G_{m3},G_{mf} (μA/V)	C_{C1} (pF)	C_{C2} (pF)	I_{DD} (μA)	FOM (–)	Noise (nV/Hz$^{\frac{1}{2}}$)
1	1	2000	2000	2000	2.40	2.40	500	0.50	4.70
1	2	464	929	929	0.56	0.51	174	1.42	9.76
1	3	252	756	756	0.30	0.27	126	2.00	13.2
1	4	172	687	687	0.21	0.18	107	2.29	16.0
2	1	663	332	663	0.80	1.33	145	1.71	8.16
2	2	6611	6611	13221	7.97	17.7	2066	0.12	2.58
2	3	658	987	1975	0.79	1.14	267	0.93	8.19
2	4	309	619	1239	0.37	0.45	155	1.62	11.9

We design the circuit in the Cadence environment and the corresponding transistors' aspect ratios are reported in Table 3.

Table 3. Transistors' aspect ratios for the RNMC-ICBFF OTA.

Transistor	Aspect Ratio
M1 *, M2 *	2.5/0.12
M3, M4	2.2/0.25
M5	8/0.25
M6, M9	8.8/0.25
M7	16/0.25
M8	9.4/0.12
M10 **	10/0.12
MB	4/0.25

* Low-voltage transistors; ** High-voltage transistors.

The open-loop gain of the circuit in Figure 9 is simulated and reported in Figure 12 in terms of Bode diagram. The reported GBW is 62 MHz with a phase margin of 61 deg.

All the following transient simulations deal with the time response of the SC integrator during the evaluation phase, ϕ_2. In particular, all the steps are referred to the output signal and are centered around the analog ground, $V_{AGND} = V_{DD}/2 = 0.5\,V$. This means that to simulate an output step of $\Delta V = +100\,mV$, we first precharge the output node at $v_{OUT}(n-1) = V_{AGND} - \Delta V/2 = 0.45\,V$ and then we apply a constant input signal $v_{IN} = (C_f/C_s)\Delta V$. In this manner, from (29), the output jumps at $v_{OUT}(n) = v_{OUT}(n-1) + \Delta V = 0.55\,V$.

The output step responses of the closed-loop amplifier to different step amplitudes are shown in Figure 13. Figure 13a,b depict the transient behavior of a ±100-mV output step for the rising edge and the falling one, respectively. The simulated settling-times are 12.2 ns (NST $=$ 0.92) and 15.0 ns (NST $=$ 1.13), respectively, for an accuracy level of 0.5%. Figure 13c,d show the transient behavior of a ±800-mV output step. In this case, the signal excursion is close to the rail-to-rail situation but still ensuring that no transistor exit from the saturation region. As expected, the slew-rate increases the 0.5% settling time

up to 13.2 ns (NST = 0.99) and 17.8 ns (NST = 1.34), for the rising edge and the falling one, respectively.

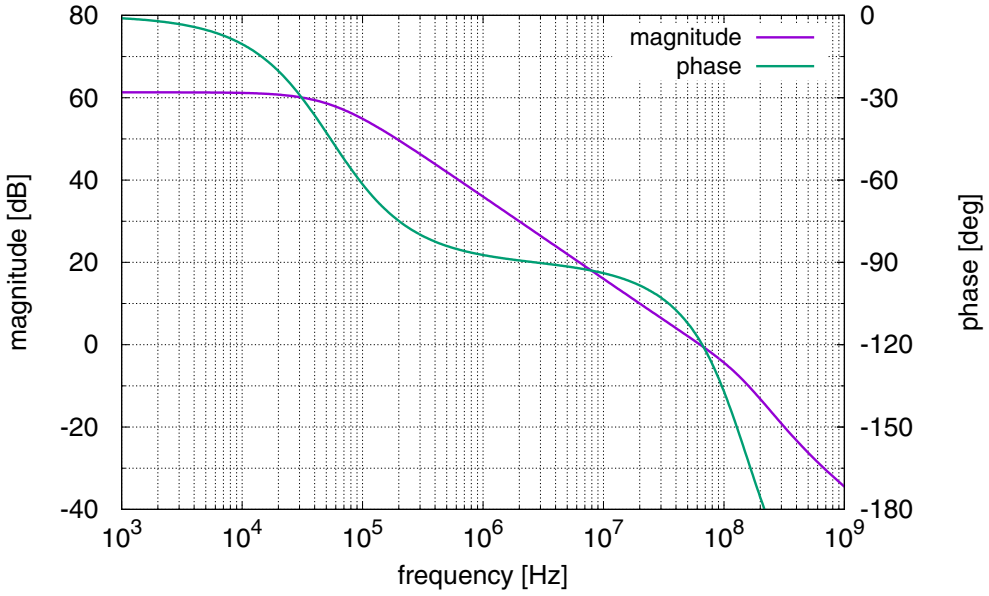
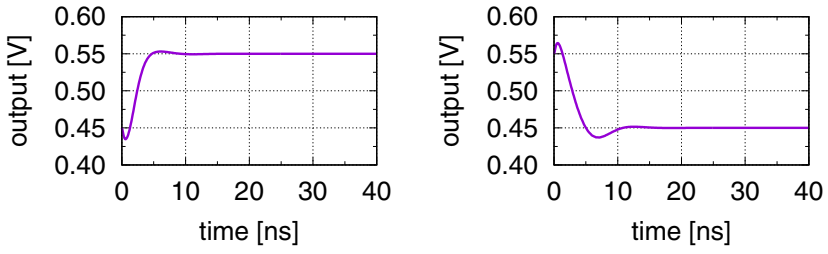


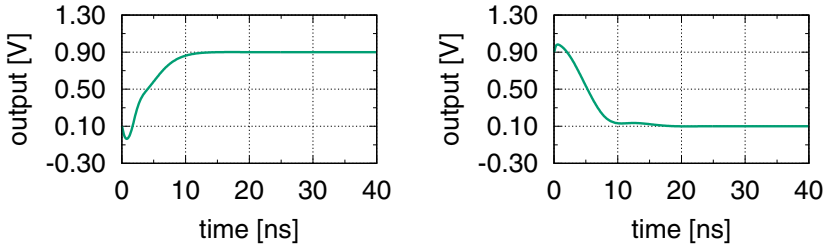
Figure 12. Bode diagram of the open-loop gain of the circuit in Figure 9.

Figure 14 shows the plot of the 0.5% settling time versus the step amplitude at the output node. The curve of the single-pole case, evaluated from (22), is also reported. As expected, for the rising edge, the settling time remains well below the single-pole limit up to 0.9 V. Above this value, some transistors enter the triode region, and the settling time goes out specifications. The falling output step suffers from slew-rate limitation at the output node. This is mitigated by the SR enhancer that allows the settling time to follow the single-pole limit up to 0.9 V, also in this case.



(**a**) Output step $\Delta V = +100\,\text{mV}$.

(**b**) Output step $\Delta V = -100\,\text{mV}$.



(**c**) Output step $\Delta V = +800\,\text{mV}$.

(**d**) Output step $\Delta V = -800\,\text{mV}$.

Figure 13. Transient simulation of the closed-loop OTA compensated with the RNMC-ICBFF. The steps are centered around $V_{\text{AGND}} = 0.5\,\text{V}$ and are related to the output voltage by $\Delta V = v_{\text{OUT}}(n) - v_{\text{OUT}}(n-1)$.

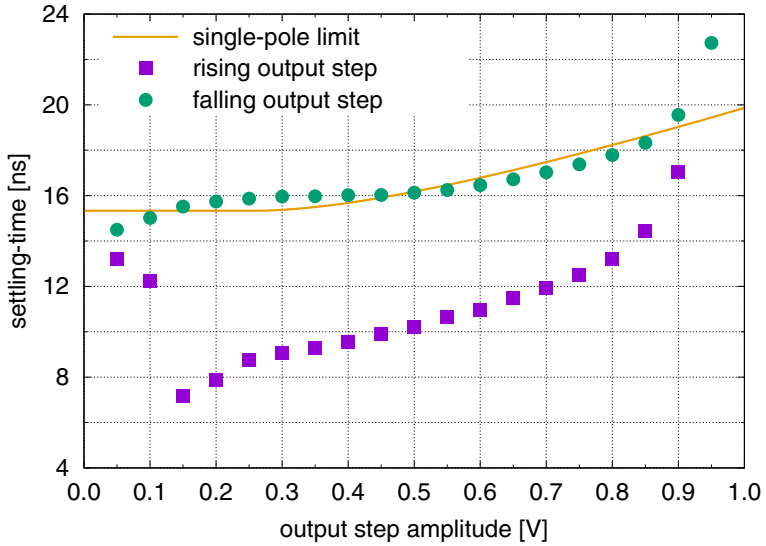
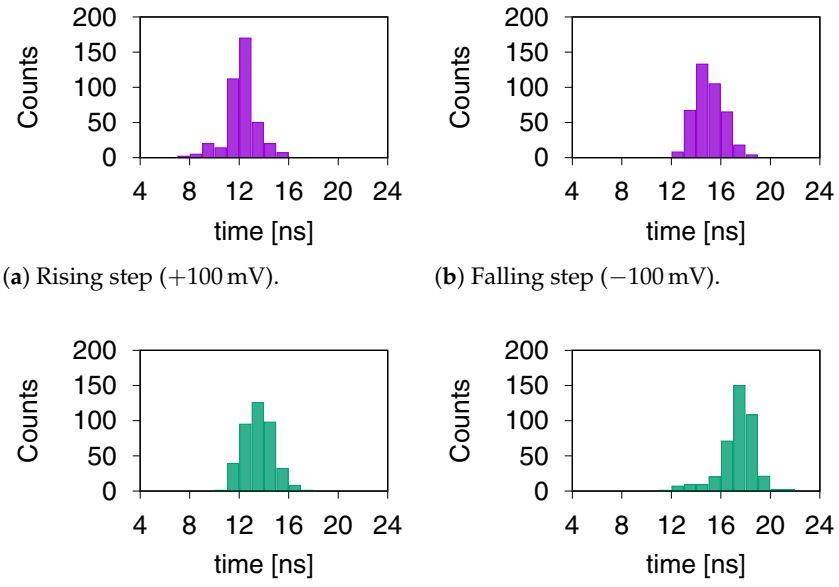


Figure 14. Settling time versus output step amplitude for the closed-loop amplifier compensated with the RNMC-ICBFF. The plot shows also the single-pole limit evaluated using (22) with (9).

A 400-run Monte-Carlo simulation is performed to estimate how the circuit behaves under both global and local process variations. The results are condensed in the histograms in Figure 15. Figure 15a,b refer to the ±100-mV output step cases. Figure 15c,d refer to the ±800-mV output step cases. Except for a small number of samples in the 800-mV falling step case (Figure 15d), all the runs fall inside the settling-time specifications of 20 ns, a very good result considering that the circuit was not designed to be robust against process variations. However, it is easy to extend the design strategy to the worst-case corner of a PVT scenario or to integrate it with the approach described in [29].



(**a**) Rising step (+100 mV).

(**b**) Falling step (−100 mV).

(**c**) Rising step (+800 mV).

(**d**) Falling step (−800 mV).

Figure 15. Monte-Carlo simulation of the settling time of the closed-loop OTA compensated with the RNMC-ICBFF.

5. Conclusions

In this paper, we provided an analytical design criterion for the optimization of the small-signal settling time in a three-stage amplifier, based on making equal the two exponential decays of the step response. Included the slew-rate effects to the design criterion we carried out a design strategy that was used to design a three-stage OTA from settling-time specifications. Extensive time-domain simulations confirmed the validity of the proposed design strategy.

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Appendix A. Global Separation Factors

Closing in feedback the pure three-pole system in (4) leads to the following closed-loop transfer function

$$G(s) = \frac{G_0}{1 + c_1 s + c_2 s^2 + c_3 s^3}, \tag{A1}$$

where

$$c_1 = \frac{1}{\mathrm{GBW}}, \tag{A2a}$$

$$c_2 = \frac{1}{K_e \, \mathrm{GBW}^2}, \tag{A2b}$$

$$c_3 = \frac{1}{K_e^2 K_i \, \mathrm{GBW}^3}. \tag{A2c}$$

In this situation, the two separation factors can be evaluated from the coefficients of the closed-loop transfer function as

$$K_e = \frac{c_1^2}{c_2}, \tag{A3a}$$

$$K_i = \frac{c_2^2}{c_1 c_3}. \tag{A3b}$$

In the case of a generic three-pole amplifier, the transfer function includes two zeros in the loop gain, as in (19), and the resulting closed-loop transfer function is

$$G(s) = G_0 \frac{1 + b_1 s + b_2 s^2}{1 + c_1 s + c_2 s^2 + c_3 s^3} \tag{A4}$$

where

$$c_1 = \frac{1}{\text{GBW}} + b_1, \tag{A5a}$$

$$c_2 = \frac{a_1}{\text{GBW}} + b_2, \tag{A5b}$$

$$c_3 = \frac{a_2}{\text{GBW}}. \tag{A5c}$$

As long as the GBW remains below the zeros of $G(s)$ we can assume that the amplifier time response is mainly determined by the poles of its closed-loop transfer function. This consideration allows us to define the equivalent or *global separation factors* using the coefficients of its closed-loop gain, as we did in (A3), so that

$$\hat{K}_e = \frac{c_1^2}{c_2} = \frac{(1 + b_1\text{GBW})^2}{a_1\text{GBW} + b_2\text{GBW}^2}, \tag{A6a}$$

$$\hat{K}_i = \frac{c_2^2}{c_1 c_3} = \frac{\left(a_1\text{GBW} + b_2\text{GBW}^2\right)^2}{a_2\text{GBW}^2(1 + b_1\text{GBW})}. \tag{A6b}$$

Therefore, we can optimize the step response of the generic three-pole amplifier by design the amplifier so that $\hat{K}_e = 8/3$ and $\hat{K}_i = 9/4$. Once again, since the coefficients are normalized with respect to the GBW, the optimization will affect the dimensionless settling time, only.

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