Charge Pumps for Ultra-Low-Power Applications: Analysis, Design and New Solutions

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***Abstract*— In this paper a brief tutorial of charge pump topologies for management of self-powered nodes in ultra-low-power applications, such as internet of things nodes, is presented. It aims to provide to the designer guidelines to choose the most suitable solution, according to the given design specifications. After a brief historic evolution, the main design equations of charge pumps and a collection of the recent proposed topologies and regulation schemes are discussed, allowing for qualitative insight into the state-of-the-art of integrated topologies.**

***Index Terms*— Charge Pumps; DC-DC Converters; Energy harvesting; IoT; Sensor Networks.**

I. Introduction

In emerging ultra-low-power applications, as the Internet-of-Things (IoT) and the Wireless Sensor Networks (WSNs), self-powered sensor nodes are employed to gather data from the environment and share them with the final user [1], [2]. For these devices, energy-autonomy is achieved by scavenging energy from the ambient using different kinds of transducers, such as photovoltaic cells, thermoelectric generators and vibration sensors [3]–[10].

Nevertheless, due to the heavy dependence of their output voltage from the operating conditions, these transducers are often unsuitable to directly feed the circuit where they are applied. For this reason, a power management integrated circuit (PMIC) is employed in order to adapt power profiles with the maximum conversion efficiency.

Figure 1 shows a simplified block diagram of a PMIC. The input voltage, V_{IN}, provided by an external transducer, feeds the main power converter and the auxiliary circuitry (e.g. oscillators, error amplifiers and kick-start system), therefore these blocks must enable self-start-up in critical conditions, i.e. low-voltage and low-power levels provided by the external energy harvesters [11]–[13]. The main converter is then properly managed to obtain a precise stable output voltage or to optimize power consumption versus the required load current.

In particular, the power converters can be implemented using switched inductor (SI) or switched capacitor (SC) topologies. The SI are suitable for applications requiring high power levels, but require off-chip bulky components, such as inductors or transformers. Thus in low-power and low-area applications, such as IoT and WSN nodes, SC converters represent a better alternative, since they are amenable for full on-chip integration [14]–[37].

In literature, SC converters with a voltage gain higher than one are usually referred as charge pumps (CPs) or voltage multipliers [38], [39]. These have been traditionally adopted in non-volatile memories and SRAMs [40]–[42], where the main design constraints are low settling time and silicon area, or LCD drivers and RF antenna switch controllers, where the main constraint is the current drivability [43], [44].

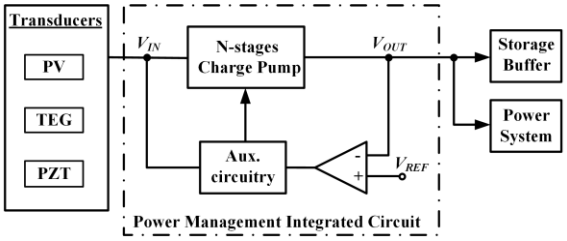

Fig. 1. Simplified block diagram of a CP-based energy harvesting power management integrated circuit (PMIC).

More recently, CPs have been widely used to adapt the voltage levels between two or more functional blocks and to convey the electric energy, extracted from surrounding environment, towards a storage buffer. Hence, it is becoming an essential building blocks for energy-autonomous systems, such as battery-less circuits, biomedical implants, IoT and WSN nodes. In these latter contexts, the design of a PMIC based on CPs is a challenging task since it must fulfill a very-low-input voltage supply (few hundred of millivolts) and high-power conversion efficiency.

At this purpose, several works on CP circuits for low-voltage and low-power applications have been presented in literature [14]–[37]. The bar graph in Fig. 2 reports the overview of a bibliographic analysis, based on the IEEE journal collection, which reveals the increasing number of ICs including at least one CP, thus confirm of the relevance and the wide applicability of these building blocks.

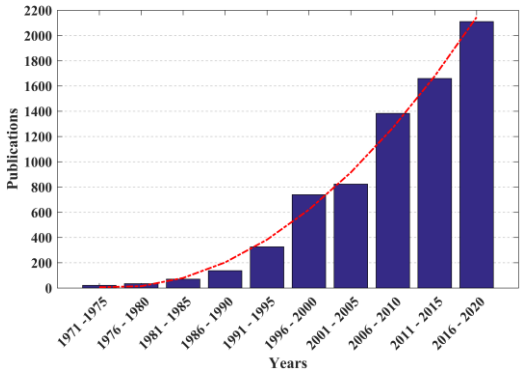

Fig. 2. IEEE journals concerning charge pump circuits over the years.

Historically, CP circuits originated with the Villard cascade, better known as Cockcroft–Walton voltage multiplier, which uses serial capacitor ladders [45], [46]. Since the Villard cascade has a relatively large output impedance, (proportional to N^3, being N the number of stages), various types of multipliers with different topologies have been proposed to reduce the output impedance.

By alternately switching the state from in-serial to in-parallel and vice-versa, Brugler theoretically showed that the serial–parallel multiplier had a lower output impedance (proportional to N) than that of Cockcroft-Walton [47]. Falkner suggested that parallel capacitor ladders reduced the output impedance as well the parallel topology [48]. It was successively validated by means of the first on-chip CP implemented by Dickson in 1976 [49].

Another direction for improving CP performance is represented by the increase on the maximum attainable voltage gain, G_{MAX}. At this purpose, Ueno et al. proposed the Fibonacci SC multiplier whose G_{MAX} is given by the N-th Fibonacci number, F(N) [50]. The multipliers whose G_{MAX} is given by 2^N were proposed by the same authors with multi-phase switching clocks and patented by Cernea in the version with two-phase clocks [51]. These CPs are characterized by a different mode of charge transfer between the capacitors of the various stages.

From the design point of view, attention must be payed also to the maximum drop voltages across the capacitors (V_{CAP}) or the charge transfer switches (V_{CTS}), as well as the sensitivity to parasitic contributions (S_{PAR}). These characteristic parameters, with the before mentioned maximum voltage gain, G_{MAX}, and output impedance, R_{CP}, are briefly summarized in Table I [38].

Note that recent integrated high-voltage generators are mainly based on the Dickson linear topology due to its general better performance as compared the other topologies [38], [52]. For this reason, this tutorial mainly targets the Dickson CP presenting its behavioural model (Section II), trade-offs and design considerations (Section III), the main charge transfer switch topologies (Section IV) and regulation schemes (Section V). Concluding remarks are reported in Section VI.

TABLE I. MAIN CHARACTERISTIC PARAMETERS OF CHARGE PUMPS

CHARGE PUMP	G_{MAX}	R_{CP}	S_{PAR}	V_{CAP}	V_{CTS}
Cockcroft-Walton	$N+1$	$\propto N^3$	+	$2\,V_{IN}$	$2\,V_{IN}$
Dickson		$\propto N$	-	$N\,V_{IN}$	$2\,V_{IN}$
Serial-Parallel		$\propto N$	+++	V_{IN}	$N\,V_{IN}$
Fibonacci	F(N + 1)	$\propto$ (sum F(j))^2	++	$\approx$ F(N - 1) V_{IN}	
Exponential (2^N)	2^N	$\propto (2^N - 1)^2$	+++	$\approx 2^{N-1}\,V_{IN}$	

Note: Sensitivity, S_{PAR}, varies qualitatively from low (-) to very high (+++).

II. EQUIVALENT MODEL OF CHARGE PUMPS

As a typical example of Dickson CP, let us consider the simplified block diagram depicted in Fig. 3, which represents a traditional N-stage Dickson CP. The reader who is not familiar with CPs is suggested to refer to [39] for a simple and effective explanation of how a Dickson CP works.

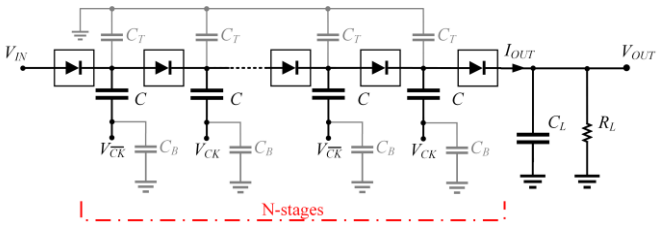

Fig. 3. Simplified block diagram of a N-stages Dickson CP.

Without loss of generality, the single charge transfer switch (CTS) (boxed diode) is assumed to be a device which can be modelled with an on-resistance and a constant voltage drop respectively equal to R and V_T. This simple model can be easily adapted to different type of switches (e.g., sub-threshold diode-connected or bootstrapped MOS transistor, etc.) [11], [28].

Each pumping capacitor has a constant capacitance value, C, and for each of them two parasitic contributions at the top plate, $C_B=\alpha_B C$, and bottom plate, $C_T=\alpha_T C$, are also included, where the coefficients α_B and α_T are technological dependent parameters. The topology exploits two counterphase clock signals whose frequency, duty-cycle and amplitude are expressed by f, δ and V_{CK}, respectively. Finally, CP load is modelled with the pair C_L-R_L, which is fed by the output current I_{OUT}.

In literature, CPs are often assumed to operate within Slow Switching Limit (SSL) region, i.e. an operating regime in which during each clock semi-period all the charge is totally transferred from one pumping capacitor to the following one. In SSL region the CP can be modelled, in both the transient and the steady-state, by an equivalent RC-circuit [53], [54].

However, voltage, power and area constraints of the modern applications require power converters working also in Fast Switching Limit (FSL) region [55] (i.e., the operating regime in which during each clock semi-period the charge is not totally transferred from one pumping capacitor to the other). With this in mind, the wide-frequency range model, shown in Fig. 4, was proposed in [28].

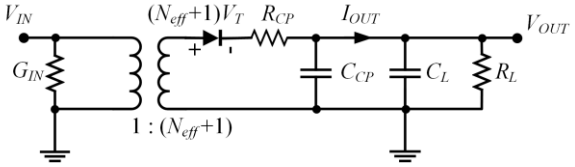

Fig. 4. Equivalent model of a Charge Pump.

The transformer in Fig. 4 operates an ideal power conversion of the input voltage, V_{IN}, while the input conductor, G_{IN}, given by

$$G_{IN} = (\alpha_B + \alpha_T)\,NCf \qquad (1)$$

models the power loss due to continuous commutations of the bottom and top stray capacitances C_T and C_B. Moreover, in Fig. 4, $N_{eff}= N/(1+\alpha_T)$ is the effective number of stages (i.e. N reduced by a factor due to the charge partition of the stage capacitor with the top plate stray capacitance), R_{CP} and C_{CP} are the output impedance and self-capacitance of the charge pump,

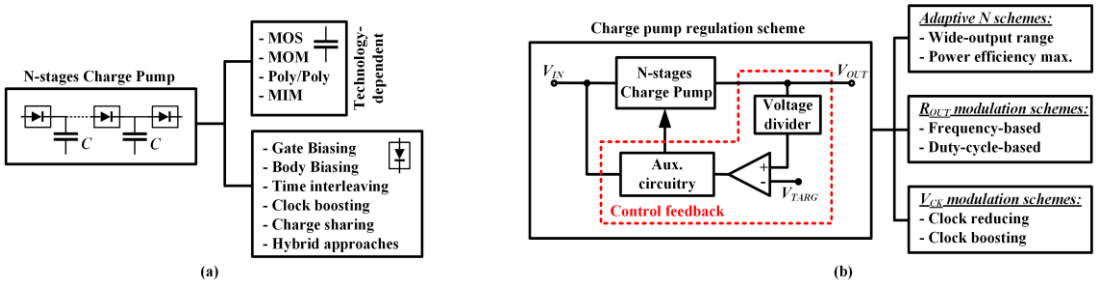

Fig.5 Charge pump classifications according to: (a) stage capacitor type and CTS topology; (b) regulation scheme.

respectively given by

$$R_{CP} = (R/\delta)\left[N \coth\left(\frac{1}{f\tau}\right) + \operatorname{csch}\left(\frac{1}{f\tau}\right)\right] \Big/ f\tau \quad (2a)$$

$$C_{CP} = \frac{4N^2+3N+2}{12(N+1)} C \quad \textit{for even } N \quad (2b)$$

$$C_{CP} = \frac{4N^2-N-2}{12N} C \quad \textit{for odd } N \quad (2c)$$

where in (2a), the term τ indicates the time constant of the inter-stage charge transfer and its value is equal to $RC(1+\alpha_T)/\delta$.

A useful alternative expression for (2a) considering only the extreme values for R_{CP}, thus $R_{CP,SSL}=N_{eff}/fC$ and $R_{CP,FSL}=(N+1)R/\delta$, is given by

$$R_{CP} \approx \sqrt{R_{CP,SSL}^2 + R_{CP,FSL}^2} \quad (3)$$

By using (3) instead of (2a) an often-tolerable maximum error of 7% occurs.

By using the switch-resistance-aware model introduced in [55] and the dynamic CP model in [53], where relationship (2) of the model in Fig. 4 are derived, it can be found the fundamental equations which describe transient, steady-state and power breakdown by means of the intrinsic time constant, the V_{OUT}-I_{OUT} characteristic and the power efficiency, respectively expressed by

$$\tau_{CP} = R_{CP}(C_{CP} + C_L) \quad (4)$$

$$V_{OUT} = (V_{IN} - V_T) + N_{eff}(V_{CK} - V_T) - R_{CP} I_{OUT} \quad (5)$$

$$\eta = \left[1 + \frac{(N_{eff}+1)V_T I_{OUT} + R_{CP} I_{OUT}^2 + (\alpha_B + \alpha_T) NCfV_{CK}^2}{V_{OUT} I_{OUT}}\right]^{-1} \quad (6)$$

Equations (2) and (3) are strictly valid for a Dickson CP. Note, however, that the model in Fig. 4 has a general applicability, can be hence used for any different kind of CP by simply replacing the correct values of the various parameters.

III. Trade-Offs and Design Considerations

The main features of CPs reported in Table I give information about maximum drop voltages across the capacitors ($V_{CAP} = NV_{IN} = V_{OUT} - V_{IN}$) or the charge transfer switches ($V_{CTS} = 2V_{IN}$), which establish the guidelines to choose the most suitable components.

For the Dickson CP, a particular role is played by the capacitors, since the voltage drop that they must sustain increases with the number of stages. CMOS technologies provide different kind of capacitors: from the standard MOS and Metal-Oxide-Metal (MOM) capacitors to those which requires optional manufacturing steps as the thick oxide MOS, Poly-Poly (PP) and high-K Metal-Insulator-Metal (MIM) capacitors. Their suitability in CPs is assessed considering three parameters, namely parasitic contributions, breakdown voltage (BV) and capacity per unit area.

Parasitic contributions of a capacitors are mainly related to the distance of the top and bottom plate from the substrate. As an example, the MIM capacitors, which are typically implemented in the highest metal levels, exhibit low parasitic capacitances and, consequently, are among the best choices for highly compact and efficient CPs.

The BV of a capacitor depends on the distance between the capacitor plates which is set by the maximum oxide thickness. This latter parameter is related to the nominal supply voltage of the adopted technology. In applications requiring on-chip generation of a voltage higher than the nominal supply one, like CPs, the pumping capacitors closest to the output node (i.e., those that must sustain a voltage higher than the BV) can be implemented by the series of two or more MIM capacitors or by using MOM capacitors with opportunely spaced metals [38]. Unfortunately, in both cases an unavoidable increase of the silicon occupied area occurs.

As detailed in the next Section, CTSs are implemented by using active devices, such as MOSFETs and/or diodes, whose main limiting factors are the gate oxide and the implants/substrate junction breakdown voltages, threshold voltage, on/off resistance, and parasitic capacitances. While the first one limits the maximum input voltages V_{IN} and V_{CK}, the second one limits the output voltage, since it is the highest voltage in the circuit. Extension of the output voltage over the junction BV can be achieved by adopting triple-well technologies. Available deep N-Well can be exploited as substrate for stages whose node voltages exceed the junction BV [56]. However, over-voltage protections (OVP) of input and output nodes are mandatory to be sure that CP operates in a safety mode.

Reduction of the parameter in (4) and (6) is the target to pursuit. Design parameter are N, R_{CP}, C_{CP}, while the choice of capacitor and topology of the CTS is aimed to reduce their nonidealities, thus V_T, α_B and α_T, as well as, other factors, to be considered in CPs for ultra-low-voltage applications, as the minimum input voltage for which the CTSs are able to guarantee the desired forward to backward current ratio [57] and the input total energy, whose expression is

$$E_{IN} = (C_{CP} + C_L)\left[V_{OUT}(n\tau_{CP}) - V_{OUT}(0)\right]^2 \quad (7)$$

where $V_{OUT}(n\tau_{CP})$ and $V_{OUT}(0)$ are the target output voltage,

reached after *n*-times τ_{CP}, and its initial value, respectively. These factors affect the start-up of the CP. The input energy can be easily reduced exploiting pre-charging technique introduced in [19], which allows, also, to speed-up the CP; while the minimum input voltage can be reduced by apply biasing techniques to CTS or boosting the input voltages [11], [42]. In the other hand, focusing on the steady-state phase, a trade-off between speed and power consumption has to be often found. Neglecting static power dissipation, such as current load-dependent power losses, switching losses constitute the heaviest contribute. It increases with the clock frequency, as in the opposite manner the settling time depends on. In such case, reduction of the clock amplitude [58] and modulation of switching frequency [28] are fruitful strategies to achieve balanced performance for the designed CP.

IV. Charge Transfer Switch Topologies

Since the choice of the pumping capacitors is limited to those available in the specific adopted technology, the circuit topology of the CTS constitutes one of the main diversification factors among the various CP architectures proposed in literature. This aspect is highlighted in Fig. 5a where a summary of the different kind of capacitors and CTS topologies is summarized [11].

In the first monolithic integrated CP [49], the CTS was implemented with a diode-connected n-type MOSFET, which works in saturation or in the cut-off region. The CP steady-state voltage output is given by (3). Since V_T is in turn a function of the source-bulk voltage, it could become a limiting factor for voltage gain and efficiency [59]. To get rid of this drawback, several solutions which exploit gate and body (or bulk) biasing have been proposed in literature [31], [60]–[63].

As depicted in Fig. 6a, Gate Biasing Technique (GBT) exploits auxiliary circuits to generate the gate control signal of the transistor implementing the stage switch in order to improve its electrical properties, such as threshold voltage and on/off resistance. GBTs can be classified into controlled- and not-controlled-switch techniques. In the first case a gate voltage is controlled by a signal provided by an auxiliary circuit, otherwise in the second case each transistor is simply connected to the node signals already present in the CP itself.

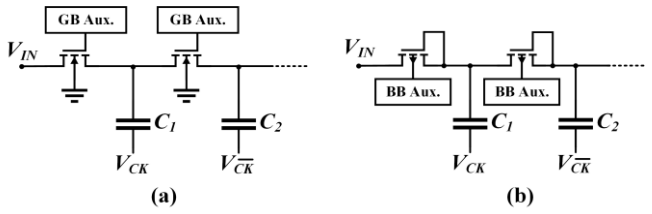

Fig. 6. Simplified diagram of (**a**) gate biasing and (**b**) bulk biasing technique

A CP adopting controlled-switch technique was applied on memories by Atsumi et al. [60]. A four-phase non-overlapped clock, where two shortest phases are boosted to $2V_{IN}$, is needed, and a small auxiliary local boosting capacitor is added to further boost the gate voltage during the forward conduction phase. This topology is usually named bootstrap CP. The main transistor works in triode region since the overdrive voltage is increased by the difference between the amplitude of the two clock signals. Thus, the CP efficiency and current drivability are improved, even if V_{IN} is less than V_T.

Body Biasing Techniques (BBTs) exploit the bulk terminal of the transistor and the body effect of the threshold voltage to improve its characteristics as a switch. These techniques are finding a wide use in low-voltage applications, where the limited input voltage guarantees the parasitic bipolar junctions to not turn on [63]. In general applications, BBTs are classified into forward, backward and dynamic, according to the way the body diodes are biased. Recently, the current-mode body biasing technique has been introduced in [63] in order to improve the performance of a diode-connected PMOS during both forward conduction and backward cut-off phases.

In general, the CP results in a noisy block. Indeed, it has an output voltage ripple expressed by

$$V_{ripple} = \frac{I_L}{fC_L} \tag{8}$$

Thus, specification of the output voltage ripple binds the choice of a minimum value for the output capacitance. Moreover, a high input current ripple makes the employ of large input by-pass capacitors necessary. A solution to both problems is given by time-interleaved CPs [25]. The idea behind this topology is to split a single CP into two or more smaller pumps working in complementary time slots. This strategy increases the equivalent frequency with which the current is sunk from the supply and delivered to the load, thus lowering the voltage ripple. The time-interleaving paradigm is the basis of the well-known dual-branch cross-coupled (or latched) CPs, originally proposed in [64], [65] and whose scheme is reported in Fig. 7. This kind of CTS allows also to get rid of the transistor threshold voltage thus becoming one of the widely adopted topology [22], [29], [32], [64]–[66].

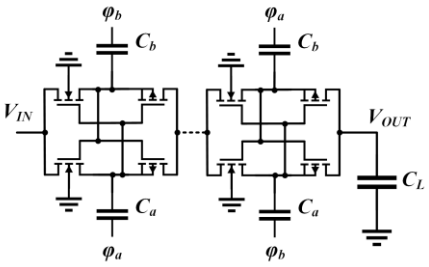

Fig. 7. Dual-branch cross-coupled charge pump block scheme.

With the aim of reducing the energy requested from the input source during the transients, charge sharing techniques have been also proposed in literature [67], [68]. The adiabatic CP focuses on the slow charging condition (adiabatic principle) in order to reduce the energy which is not transferred to the load. This technique is useful in applications where the main constraint derives from the limited power budget.

Finally, hybrid approaches or reconfigurable charge pumps, also known as adaptative CPs, are increasingly used in that cases where the operative conditions, as example the input voltage level or the current load, could drastically change [39].

V. Charge Pump Regulation Schemes

The output voltage of the CP must be regulated in order to set a stable value with constraints imposed by the load. Such constraints depend on the specific application and the supplied circuit type (i.e., purely capacitive, purely resistive or mixed). As an example, in non-volatile memory applications, such as NOR Flash and, more recently, 3D NAND memories [40], [69], [70], CP circuits are used to provide operation voltages for a single or multiple word lines, which exhibit a purely capacitive behavior. For these CPs, the main design specs are settling time and voltage conversion efficiency (VCE)[1]. On the other hand, the building blocks of energy-autonomous wireless nodes consume both static and dynamic power. Therefore, the load is both capacitive and resistive and, consequently, power conversion efficiency of the CPs constitutes the main constraint in these applications [4], [11]. Finally, in CPs used in cold-start of energy harvesting circuits based on thermoelectric generators the load is both capacitive and resistive but the main specifications are VCE and settling time [17], [71]–[73].

Ideally, in a conventional regulated N-stages CP, the output voltage can be adjusted from V_{IN} to $(N+1)V_{IN}$ by changing one or more CP parameters according to the reference voltage, V_{TARG}. Based on the parameter on which they act, regulation schemes can be classified into adaptive, output resistance and clock amplitude modulation, as summarized in Fig. 5b.

In the adaptive schemes the stages are rearranged to allow different CP voltage levels or works within the maximum power efficiency zone at the defined output voltage [41], [74]–[76]. In the widest adopted closed-loop adaptive scheme, whose simplified block diagram is shown in Fig. 8, a block that searches for the optimum number of stages is exploited to adapt the number of active stages with the actual voltage gain, in order to optimize the whole system efficiency [75], [76]. This scheme often includes a further control feedback loop to set the output voltage at a reference voltage, which can be implement with one of the other regulation schemes.

In the output resistance modulation schemes, the clock frequency and/or the duty cycle are changed by exploiting a Voltage Controller Oscillator (VCO), to adapt the CP output resistance to the load [77]–[80].

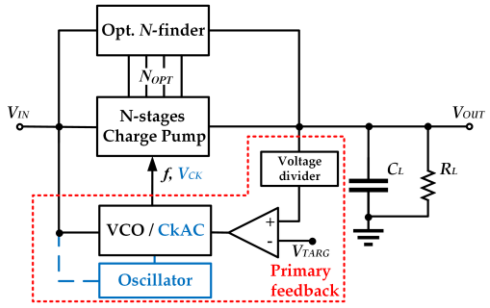

Fig. 8. Simplified block diagram of an adaptive scheme.

In the clock amplitude modulation schemes, instead, the clock amplitude is modulated to reduce switching power losses (clock reducing) or to speed-up the output transient response (clock boosting) [42], [58].

Table II reports the main features of the regulation schemes, where the load range is the range in which the control works.

TABLE II. Comparison between the regulation schemes

REG. SCHEME	*Controlled parameter*	*Load range*	*Working zone*	*Typical Application*
Adaptive	N	DPF*	SSL	Low power
Frequency mod.	R_{OUT}	Narrow	SSL	General
Duty cycle mod.		Middle	FSL	General
Clock reducing	V_{CK}	Wide	SSL/FSL	Low power
Clock boosting		Narrow	SSL/FSL	High speed

** Depends on Primary Feedback.*

VI. Conclusions and Future Perspectives

This tutorial has briefly illustrated as the charge pump circuits, and in particular the Dickson CP, evolved along the years and the importance they have gained in modern low-power applications.

An equivalent model for the CP working on a wide-frequency range has been discussed and the main adopted charge transfer switch topologies have also been considered together with a comparison of the different regulation schemes. Thus, a comprehensive overview of the main design solutions is offered to the reader.

Regarding future perspectives, we have to consider that the minimum open circuit voltage of transducers is likely determined by the minimum operating voltage of the oscillator and control circuits to drive the CP. Thus, circuit designers need to develop extremely low voltage building blocks to make power management integrated circuits functional even under low environmental energy conditions.

In CP that can work at an input voltage as low as, e.g., 0.1 V, the leakage current of the CTS has to be taken into account to get optimum design [81]. With leakage current relatively large, the capacitance per stage would need to be increased. Moreover, it should be considered that leakage current increases with process variations and that is highly temperature-dependent too. Thus, optimum design needs to be reconsidered for process and temperature tolerance. In conclusion, especially for extremely low voltage applications, numerous open research challenges remain unsolved, thus providing many areas for future designers to explore.

[1] VCE is defined as the ratio between the actual and the ideal output voltage.

References

[1] M. Alioto, Ed., *Enabling the Internet of Things: From Integrated Circuits to Integrated Systems*. Springer International Publishing, 2017.

[2] F. Al-Turjman, *Internet of Nano-Things and Wireless Body Area Networks (WBAN)*. CRC Press, 2019.

[3] K. O. Htet, R. Ghannam, Q. H. Abbasi, and H. Heidari, 'Power Management Using Photovoltaic Cells for Implantable Devices', *IEEE Access*, vol. 6, pp. 42156–42164, 2018, doi: 10.1109/ACCESS.2018.2860793.

[4] L. Vračar, A. Prijić, D. Nešić, S. Dević, and Z. Prijić, 'Photovoltaic Energy Harvesting Wireless Sensor Node for Telemetry Applications Optimized for Low Illumination Levels', *Electronics*, vol. 5, no. 2, Art. no. 2, Jun. 2016, doi: 10.3390/electronics5020026.

[5] A. D. Grasso and S. Pennisi, 'Micro-scale inductorless maximum power point tracking DC-DC converter', *IET Power Electron.*, vol. 6, no. 8, pp. 1634–1639, Sep. 2013, doi: 10.1049/iet-pel.2012.0553.

[6] U. Çilingiroğlu, B. Tar, and Ç. Özmen, 'On-Chip Photovoltaic Energy Conversion in Bulk-CMOS for Indoor Applications', *IEEE Trans.*

Circuits Syst. Regul. Pap., vol. 61, no. 8, pp. 2491–2504, Aug. 2014, doi: 10.1109/TCSI.2014.2304652.

[7] E. Dimaggio, F. Rossella, and G. Pennelli, 'Management of the Output Electrical Power in Thermoelectric Generators', *Electronics*, vol. 8, no. 12, Art. no. 12, Dec. 2019, doi: 10.3390/electronics8121514.

[8] V. Leonov, T. Torfs, P. Fiorini, and C. Van Hoof, 'Thermoelectric Converters of Human Warmth for Self-Powered Wireless Sensor Nodes', *IEEE Sens. J.*, vol. 7, no. 5, pp. 650–657, May 2007, doi: 10.1109/JSEN.2007.894917.

[9] J. McCullagh, 'An Active Diode Full-Wave Charge Pump for Low Acceleration Infrastructure-Based Non-Periodic Vibration Energy Harvesting', *IEEE Trans. Circuits Syst. Regul. Pap.*, vol. 65, no. 5, pp. 1758–1770, May 2018, doi: 10.1109/TCSI.2017.2764878.

[10] M. Wahbah, M. Alhawari, B. Mohammad, H. Saleh, and M. Ismail, 'Characterization of Human Body-Based Thermal and Vibration Energy Harvesting for Wearable Devices', *IEEE J. Emerg. Sel. Top. Circuits Syst.*, vol. 4, no. 3, pp. 354–363, Sep. 2014, doi: 10.1109/JETCAS.2014.2337195.

[11] A. Ballo, A. D. Grasso, and G. Palumbo, 'A Review of Charge Pump Topologies for the Power Management of IoT Nodes', *Electronics*, vol. 8, no. 5, p. 480, May 2019, doi: 10.3390/electronics8050480.

[12] Z. G. Wan, Y. K. Tan, and C. Yuen, 'Review on energy harvesting and energy management for sustainable wireless sensor networks', in *2011 IEEE 13th International Conference on Communication Technology*, Sep. 2011, pp. 362–367, doi: 10.1109/ICCT.2011.6157897.

[13] A. D. Grasso, G. Palumbo, and S. Pennisi, 'Switched-Capacitor Power Management Integrated Circuit for Autonomous Internet of Things Node', *IEEE Trans. Circuits Syst. II Express Briefs*, vol. 65, no. 10, pp. 1455–1459, Oct. 2018, doi: 10.1109/TCSII.2018.2856260.

[14] S. Abdelaziz, A. Emira, A. G. Radwan, A. N. Mohieldin, and A. M. Soliman, 'A low start up voltage charge pump for thermoelectric energy scavenging', in *2011 IEEE International Symposium on Industrial Electronics*, Jun. 2011, pp. 71–75, doi: 10.1109/ISIE.2011.5984135.

[15] A. Ballo, A. D. Grasso, and G. Palumbo, 'A High-Performance Charge Pump Topology for Very-Low-Voltage Applications', *IEEE Trans. Circuits Syst. II Express Briefs*, pp. 1–1, 2019, doi: 10.1109/TCSII.2019.2932471.

[16] A. Mahmoud, M. Alhawari, B. Mohammad, H. Saleh, and M. Ismail, 'A Gain-Controlled, Low-Leakage Dickson Charge Pump for Energy-Harvesting Applications', *IEEE Trans. Very Large Scale Integr. VLSI Syst.*, vol. 27, no. 5, pp. 1114–1123, May 2019, doi: 10.1109/TVLSI.2019.2897046.

[17] S. Bose, T. Anand, and M. L. Johnston, 'Integrated Cold Start of a Boost Converter at 57 mV Using Cross-Coupled Complementary Charge Pumps and Ultra-Low-Voltage Ring Oscillator', *IEEE J. Solid-State Circuits*, vol. 54, no. 10, pp. 2867–2878, Oct. 2019, doi: 10.1109/JSSC.2019.2930911.

[18] M. Ashraf and N. Masoumi, 'A Thermal Energy Harvesting Power Supply With an Internal Startup Circuit for Pacemakers', *IEEE Trans. Very Large Scale Integr. VLSI Syst.*, vol. 24, no. 1, pp. 26–37, Jan. 2016, doi: 10.1109/TVLSI.2015.2391442.

[19] A. Ballo, A. D. Grasso, and G. Palumbo, 'Charge Pump Improvement for Energy Harvesting Applications by Node Pre-Charging', *IEEE Trans. Circuits Syst. II Express Briefs*, pp. 1–1, 2020, doi: 10.1109/TCSII.2020.2991241.

[20] M. Coustans, F. Krummenacher, and M. Kayal, 'A Fully Integrated 60 mV Cold-Start Circuit for Single Coil DC–DC Boost Converter for Thermoelectric Energy Harvesting', *IEEE Trans. Circuits Syst. II Express Briefs*, vol. 66, no. 10, pp. 1668–1672, Oct. 2019, doi: 10.1109/TCSII.2019.2922683.

[21] A. K. Gupta, A. Joshi, V. Gajare, H. S. Ghanshyam, and A. Dutta, 'Power efficient reconfigurable charge pump for micro scale energy harvesting', in *2013 IEEE Asia Pacific Conference on Postgraduate Research in Microelectronics and Electronics (PrimeAsia)*, Dec. 2013, pp. 73–76, doi: 10.1109/PrimeAsia.2013.6731181.

[22] J. Goeppert and Y. Manoli, 'Fully Integrated Startup at 70 mV of Boost Converters for Thermoelectric Energy Harvesting', *IEEE J. Solid-State Circuits*, vol. 51, no. 7, pp. 1716–1726, Jul. 2016, doi: 10.1109/JSSC.2016.2563782.

[23] K. Rawy, T. Yoo, and T. T.-H. Kim, 'An 88% Efficiency 0.1–300- μ W Energy Harvesting System With 3-D MPPT Using Switch Width Modulation for IoT Smart Nodes', *IEEE J. Solid-State Circuits*, vol. 53, no. 10, pp. 2751–2762, Oct. 2018, doi: 10.1109/JSSC.2018.2833278.

[24] J. Kim, J. Kim, and C. Kim, 'A Regulated Charge Pump With a Low-Power Integrated Optimum Power Point Tracking Algorithm for Indoor Solar Energy Harvesting', *IEEE Trans. Circuits Syst. II Express Briefs*, vol. 58, no. 12, pp. 802–806, Dec. 2011, doi: 10.1109/TCSII.2011.2173971.

[25] Y. Wang, N. Yan, H. Min, and C.-R. Shi, 'A High-Efficiency Split–Merge Charge Pump for Solar Energy Harvesting', *IEEE Trans. Circuits Syst. II Express Briefs*, vol. 64, no. 5, pp. 545–549, May 2017, doi: 10.1109/TCSII.2016.2581589.

[26] Y. Shih and B. P. Otis, 'An Inductorless DC–DC Converter for Energy Harvesting With a 1.2-$ \mu\hboxW$Bandgap-Referenced Output Controller', *IEEE Trans. Circuits Syst. II Express Briefs*, vol. 58, no. 12, pp. 832–836, Dec. 2011, doi: 10.1109/TCSII.2011.2173967.

[27] H. Peng, N. Tang, Y. Yang, and D. Heo, 'CMOS Startup Charge Pump With Body Bias and Backward Control for Energy HarvestingStep-Up Converters', *IEEE Trans. Circuits Syst. Regul. Pap.*, vol. 61, no. 6, pp. 1618–1628, Jun. 2014, doi: 10.1109/TCSI.2013.2290823.

[28] A. Ballo, M. Bottaro, A. D. Grasso, and G. Palumbo, 'Regulated Charge Pumps: A Comparative Study by Means of Verilog-AMS', *Electronics*, vol. 9, no. 6, Art. no. 6, Jun. 2020, doi: 10.3390/electronics9060998.

[29] J. Kim, P. K. T. Mok, and C. Kim, 'A 0.15 V Input Energy Harvesting Charge Pump With Dynamic Body Biasing and Adaptive Dead-Time for Efficiency Improvement', *IEEE J. Solid-State Circuits*, vol. 50, no. 2, pp. 414–425, Feb. 2015, doi: 10.1109/JSSC.2014.2375824.

[30] X. Liu, L. Huang, K. Ravichandran, and E. Sánchez-Sinencio, 'A Highly Efficient Reconfigurable Charge Pump Energy Harvester With Wide Harvesting Range and Two-Dimensional MPPT for Internet of Things', *IEEE J. Solid-State Circuits*, vol. 51, no. 5, pp. 1302–1312, May 2016, doi: 10.1109/JSSC.2016.2525822.

[31] H. Fuketa, S. O'uchi, and T. Matsukawa, 'Fully Integrated, 100-mV Minimum Input Voltage Converter With Gate-Boosted Charge Pump Kick-Started by LC Oscillator for Energy Harvesting', *IEEE Trans. Circuits Syst. II Express Briefs*, vol. 64, no. 4, pp. 392–396, Apr. 2017, doi: 10.1109/TCSII.2016.2573382.

[32] H. Yi, J. Yin, P. Mak, and R. P. Martins, 'A 0.032-mm20.15-V Three-Stage Charge-Pump Scheme Using a Differential Bootstrapped Ring-VCO for Energy-Harvesting Applications', *IEEE Trans. Circuits Syst. II Express Briefs*, vol. 65, no. 2, pp. 146–150, Feb. 2018, doi: 10.1109/TCSII.2017.2676159.

[33] S. Yoon, S. Carreon-Bautista, and E. Sánchez-Sinencio, 'An Area Efficient Thermal Energy Harvester With Reconfigurable Capacitor Charge Pump for IoT Applications', *IEEE Trans. Circuits Syst. II Express Briefs*, vol. 65, no. 12, pp. 1974–1978, Dec. 2018, doi: 10.1109/TCSII.2018.2794299.

[34] C.-W. Liu *et al.*, 'An 82.9%-Efficiency Triple-Output Battery Management Unit for Implantable Neuron Stimulator in 180-nm Standard CMOS', *IEEE Trans. Circuits Syst. II Express Briefs*, vol. 66, no. 5, pp. 788–792, May 2019, doi: 10.1109/TCSII.2019.2909813.

[35] H. Kawauchi and T. Tanzawa, 'A 2V 3.8μW Fully-Integrated Clocked AC-DC Charge Pump with 0.5V 500Ω Vibration Energy Harvester', in *2019 IEEE Asia Pacific Conference on Circuits and Systems (APCCAS)*, Nov. 2019, pp. 329–332, doi: 10.1109/APCCAS47518.2019.8953130.

[36] K.-C. Woo and B.-D. Yang, 'A 0.35V 90nA Quiescent Current Output-Capacitorless NMOS Low-Dropout Regulator Using a Coarse-Fine Charge-Pump Circuit', *IEEE Trans. Circuits Syst. II Express Briefs*, pp. 1–1, 2020, doi: 10.1109/TCSII.2020.2984806.

[37] R. Umaz, 'A Power Management System for Microbial Fuel Cells with 53.02% Peak End-to-end Efficiency', *IEEE Trans. Circuits Syst. II Express Briefs*, pp. 1–1, 2019, doi: 10.1109/TCSII.2019.2951810.

[38] T. Tanzawa, *On-chip High-Voltage Generator Design: Design Methodology for Charge Pumps*, 2nd ed. Springer International Publishing, 2016.

[39] G. Palumbo and D. Pappalardo, 'Charge Pump Circuits: An Overview on Design Strategies and Topologies', *IEEE Circuits Syst. Mag.*, vol. 10, no. 1, pp. 31–45, First 2010, doi: 10.1109/MCAS.2009.935695.

[40] T. Tanzawa and S. Atsumi, 'Optimization of word-line booster circuits for low-voltage flash memories', *IEEE J. Solid-State Circuits*, vol. 34, no. 8, pp. 1091–1098, Aug. 1999, doi: 10.1109/4.777107.

[41] G. Palumbo and D. Pappalardo, 'Charge pump circuits with only capacitive loads: optimized design', *IEEE Trans. Circuits Syst. II Express Briefs*, vol. 53, no. 2, pp. 128–132, Feb. 2006, doi: 10.1109/TCSII.2005.855732.

[42] A. Ballo, A. D. Grasso, G. Giustolisi, and G. Palumbo, 'Optimized Charge Pump With Clock Booster for Reduced Rise Time or Silicon Area', *IEEE Trans. Circuits Syst. II Express Briefs*, vol. 66, no. 12, pp. 1977–1981, Dec. 2019, doi: 10.1109/TCSII.2019.2898716.

[43] TianRui Ying, Wing-Hung Ki, and Mansun Chan, 'Area-efficient CMOS charge pumps for LCD drivers', *IEEE J. Solid-State Circuits*, vol. 38, no. 10, pp. 1721–1725, Oct. 2003, doi: 10.1109/JSSC.2003.817596.

[44] A. R. Guraliuc, N. Chahat, C. Leduc, M. Zhadobov, and R. Sauleau, 'End-Fire Antenna for BAN at 60 GHz: Impact of Bending, On-Body Performances, and Study of an On to Off-Body Scenario', *Electronics*, vol. 3, no. 2, Art. no. 2, Jun. 2014, doi: 10.3390/electronics3020221.

[45] T. Tanzawa, 'Innovation of Switched-Capacitor Voltage Multiplier: Part 1: A Brief History', *IEEE Solid-State Circuits Mag.*, vol. 8, no. 1, pp. 51–59, winter 2016, doi: 10.1109/MSSC.2015.2495678.

[46] J. D. Cockcroft, E. T. S. Walton, and E. Rutherford, 'Experiments with high velocity positive ions.—(I) Further developments in the method of obtaining high velocity positive ions', *Proc. R. Soc. Lond. Ser. Contain. Pap. Math. Phys. Character*, vol. 136, no. 830, pp. 619–630, Jun. 1932, doi: 10.1098/rspa.1932.0107.

[47] J. S. Brugler, 'Theoretical performance of voltage multiplier circuits', *IEEE J. Solid-State Circuits*, vol. 6, no. 3, pp. 132–135, Jun. 1971, doi: 10.1109/JSSC.1971.1049670.

[48] A. H. Falkner, 'Generalised Cockcroft-Walton voltage multipliers', *Electron. Lett.*, vol. 9, no. 25, pp. 585–586, Dec. 1973, doi: 10.1049/el:19730433.

[49] J. F. Dickson, 'On-chip high-voltage generation in MNOS integrated circuits using an improved voltage multiplier technique', *IEEE J. Solid-State Circuits*, vol. 11, no. 3, pp. 374–378, Jun. 1976, doi: 10.1109/JSSC.1976.1050739.

[50] F. Ueno, T. Inoue, I. Oota, and I. Harada, 'Emergency power supply for small computer systems', in *1991., IEEE International Sympoisum on Circuits and Systems*, Jun. 1991, pp. 1065–1068 vol.2, doi: 10.1109/ISCAS.1991.176549.

[51] R.-A. Cernea, 'Charge pump circuit with exponetral multiplication', US5436587A, Jul. 25, 1995.

[52] A. Cabrini, R. Zurla, and G. Torelli, 'A charge pump with enhanced charge transfer for energy harvesting applications', in *2016 International Symposium on Power Electronics, Electrical Drives, Automation and Motion (SPEEDAM)*, Jun. 2016, pp. 1396–1400, doi: 10.1109/SPEEDAM.2016.7525955.

[53] T. Tanzawa and T. Tanaka, 'A dynamic analysis of the Dickson charge pump circuit', *IEEE J. Solid-State Circuits*, vol. 32, no. 8, pp. 1231–1240, Aug. 1997, doi: 10.1109/4.604079.

[54] G. Palumbo, N. Barniol, and M. Bethaoui, 'Improved behavioral and design model of an Nth-order charge pump', *IEEE Trans. Circuits Syst. Fundam. Theory Appl.*, vol. 47, no. 2, pp. 264–268, Feb. 2000, doi: 10.1109/81.828583.

[55] T. Tanzawa, 'A Switch-Resistance-Aware Dickson Charge Pump Model for Optimizing Clock Frequency', *IEEE Trans. Circuits Syst. II Express Briefs*, vol. 58, no. 6, pp. 336–340, Jun. 2011, doi: 10.1109/TCSII.2011.2158166.

[56] B. Shen, S. Bose, and M. L. Johnston, 'A 1.2 V–20 V Closed-Loop Charge Pump for High Dynamic Range Photodetector Array Biasing', *IEEE Trans. Circuits Syst. II Express Briefs*, vol. 66, no. 3, pp. 327–331, Mar. 2019, doi: 10.1109/TCSII.2018.2850341.

[57] A. Ballo, A. D. Grasso, and G. Palumbo, 'A Subthreshold Cross-Coupled Hybrid Charge Pump for 50-mV Cold-Start', *IEEE Access*, vol. 8, pp. 188959–188969, 2020, doi: 10.1109/ACCESS.2020.3032452.

[58] A. Ballo, A. D. Grasso, and G. Palumbo, 'A simple and effective design strategy to increase power conversion efficiency of linear charge pumps', *Int. J. Circuit Theory Appl.*, vol. 48, no. 2, pp. 157–161, 2020, doi: 10.1002/cta.2704.

[59] G. D. Cataldo and G. Palumbo, 'Double and triple charge pumps with mos diodes: Dynamic models to an optimized design', *Int. J. Circuit Theory Appl.*, vol. 22, no. 5, pp. 377–386, 1994, doi: 10.1002/cta.4490220506.

[60] S. Atsumi *et al.*, 'A 16-Mb flash EEPROM with a new self-data-refresh scheme for a sector erase operation', *IEEE J. Solid-State Circuits*, vol. 29, no. 4, pp. 461–469, Apr. 1994, doi: 10.1109/4.280696.

[61] A. Mahmoud, M. Alhawari, B. Mohammad, H. Saleh, and M. Ismail, 'A Charge Pump Based Power Management Unit With 66%-Efficiency in 65 nm CMOS', in *2018 IEEE International Symposium on Circuits and Systems (ISCAS)*, May 2018, pp. 1–4, doi: 10.1109/ISCAS.2018.8350898.

[62] M. Bloch, C. Lauterbauch, and W. Weber, 'High efficiency charge pump circuit for negative high voltage generation at 2 V supply voltage', in *Proceedings of the 24th European Solid-State Circuits Conference*, Sep. 1998, pp. 100–103, doi: 10.1109/ESSCIR.1998.186218.

[63] A. Ballo, A. D. Grasso, and G. Palumbo, 'Current-mode body-biased switch to increase performance of linear charge pumps', *Int. J. Circuit Theory Appl.*, vol. n/a, no. n/a, doi: 10.1002/cta.2851.

[64] R. Gariboldi and F. Pulvirenti, 'A monolithic quad line driver for industrial applications', *IEEE J. Solid-State Circuits*, vol. 29, no. 8, pp. 957–962, Aug. 1994, doi: 10.1109/4.297702.

[65] R. Gariboldi and F. Pulvirenti, 'A 70 m/spl Omega/ intelligent high side switch with full diagnostics', *IEEE J. Solid-State Circuits*, vol. 31, no. 7, pp. 915–923, Jul. 1996, doi: 10.1109/4.508203.

[66] Y. Nakagome *et al.*, 'An experimental 1.5-V 64-Mb DRAM', *IEEE J. Solid-State Circuits*, vol. 26, no. 4, pp. 465–472, Apr. 1991, doi: 10.1109/4.75040.

[67] C. Lauterbach, W. Weber, and D. Romer, 'Charge sharing concept and new clocking scheme for power efficiency and electromagnetic emission improvement of boosted charge pumps', *IEEE J. Solid-State Circuits*, vol. 35, no. 5, pp. 719–723, May 2000, doi: 10.1109/4.841499.

[68] C. Ulaganathan, B. J. Blalock, J. Holleman, and C. L. Britton, 'An ultra-low voltage self-startup charge pump for energy harvesting applications', in *2012 IEEE 55th International Midwest Symposium on Circuits and Systems (MWSCAS)*, Aug. 2012, pp. 206–209, doi: 10.1109/MWSCAS.2012.6291993.

[69] T. Tanzawa, T. Murakoshi, T. Kamijo, T. Tanaka, J. J. McNeil, and K. Duesman, 'Design challenge in 3D NAND technology: A 4.8X area- and 1.3X power-efficient 20V charge pump using tier capacitors', in *2016 IEEE Asian Solid-State Circuits Conference (A-SSCC)*, Nov. 2016, pp. 165–168, doi: 10.1109/ASSCC.2016.7844161.

[70] A. Ballo, A. D. Grasso, G. Palumbo, and T. Tanzawa, 'Linear distribution of capacitance in Dickson charge pumps to reduce rise time', *Int. J. Circuit Theory Appl.*, vol. 48, no. 4, pp. 555–566, 2020, doi: 10.1002/cta.2761.

[71] D. Rozgić and D. Marković, 'A Miniaturized 0.78-mW/cm2 Autonomous Thermoelectric Energy-Harvesting Platform for Biomedical Sensors', *IEEE Trans. Biomed. Circuits Syst.*, vol. 11, no. 4, pp. 773–783, Aug. 2017, doi: 10.1109/TBCAS.2017.2684818.

[72] M. Dezyani, H. Ghafoorifard, S. Sheikhaei, and W. A. Serdijn, 'A 60 mV Input Voltage, Process Tolerant Start-Up System for Thermoelectric Energy Harvesting', *IEEE Trans. Circuits Syst. Regul. Pap.*, vol. 65, no. 10, pp. 3568–3577, Oct. 2018, doi: 10.1109/TCSI.2018.2834312.

[73] I. Doms, P. Merken, C. Van Hoof, and R. P. Mertens, 'Capacitive Power Management Circuit for Micropower Thermoelectric Generators With a 1.4 μA Controller', *IEEE J. Solid-State Circuits*, vol. 44, no. 10, pp. 2824–2833, Oct. 2009, doi: 10.1109/JSSC.2009.2027546.

[74] Z. Luo, L.-C. Yu, and M.-D. Ker, 'An Efficient, Wide-Output, High-Voltage Charge Pump With a Stage Selection Circuit Realized in a Low-Voltage CMOS Process', *IEEE Trans. Circuits Syst. Regul. Pap.*, vol. 66, no. 9, pp. 3437–3444, Sep. 2019, doi: 10.1109/TCSI.2019.2924581.

[75] M. Cazzaniga and T.-Y. Liu, 'Charge pump system that dynamically selects number of active stages', WO2012087518A3, Jan. 10, 2013.

[76] G. Palumbo, D. Pappalardo, and M. Gaibotti, 'Charge pump with adaptive stages for non-volatile memories', *IEE Proc. - Circuits Devices Syst.*, vol. 153, no. 2, pp. 136–142, Apr. 2006, doi: 10.1049/ip-cds:20041235.

[77] W. Zhu *et al.*, 'A charge pump system with new regulation and clocking scheme', *IEICE Electron. Express*, vol. 16, no. 4, pp. 20190005–20190005, 2019, doi: 10.1587/elex.16.20190005.

[78] B. Rumberg, D. W. Graham, and M. M. Navidi, 'A Regulated Charge Pump for Tunneling Floating-Gate Transistors', *IEEE Trans. Circuits Syst. Regul. Pap.*, vol. 64, no. 3, pp. 516–527, Mar. 2017, doi: 10.1109/TCSI.2016.2613080.

[79] R. Suriyakul and N. Ayudhya, *Pulse width Modulation Control a Switched-Capacitor Dickson Charge Pumps for High Voltage High Power Applications*. .

[80] Y.-H. Chang, 'Design and analysis of pulse-width modulation-based two-stage current-mode multi-phase voltage doubler', *IET Circuits Devices Syst.*, vol. 4, no. 4, pp. 269–281, Jul. 2010, doi: 10.1049/iet-cds.2009.0111.

[81] S. Tokuda and T. Tanzawa, 'Toward a Minimum-Operating-Voltage Design of DC-DC Charge Pump Circuits for Energy Harvesting', in *2019 IEEE International Symposium on Circuits and Systems (ISCAS)*, May 2019, pp. 1–4, doi: 10.1109/ISCAS.2019.8702677.