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An Automatic Offset Calibration Method for Differential Charge-Based Capacitance Measurement

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Abstract: Charge-Based Capacitance Measurement (CBCM) technique is a simple but effective technique for measuring capacitance values down to the attofarad level. However, when adopted for fully on-chip implementation, this technique suffers output offset caused by mismatches and process variations. This paper introduces a novel method that compensates the offset of a fully integrated differential CBCM electronic front-end. After a detailed theoretical analysis of the differential CBCM topology, we present and discuss a modified architecture that compensates mismatches and increases robustness against mismatches and process variations. The proposed circuit has been simulated using a standard 130-nm technology and shows a sensitivity of 1.3 mV/aF and a 20× reduction of the standard deviation of the differential output voltage as compared to the traditional solution.

Keywords: capacitance measurement; capacitive sensors; charge based capacitance measurement; mismatch compensation

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1. Introduction

In the field of the integrated sensors, the capacitive sensing represents one of the most adopted transduction methods thanks to its relative simplicity of implementation, high sensitivity, high resolution, low temperature sensitivity and low noise performances [1]. Capacitive sensors are adopted in many fields, such as biological [2–6] (for example to detect the growth rate of a bacteria), gyroscopes [7,8], accelerometers, humidity sensors, and quality air for the detection of airborne particulate matter [9–12].

Among the different solutions that can be adopted to convert a capacitance variation into a voltage [1], a simple but effective solution is represented by Charge-Based Capacitance Measurement (CBCM), which was originally introduced in [13,14] to measure the cross-talk capacitance between metal interconnections in integrated circuits. The method has been subsequently extended and improved [15] and, thanks to its simple topology, also adopted in other applications, like lab-on-chip cells monitoring [5,16–20] or particle detectors [11,21].

CBCM offers several advantages like low silicon area, static power consumption close to zero and a resolution that can be reduced by properly choosing the integration capacitance [1]. In particular, low-area occupation enables the adoption of this topology when several capacitive electrodes must be processed at the same time [16,17,21]. However, the main limit of CBCM technique is represented by high sensitivity to mismatch and process variations that can cause an output offset voltage higher than that associated with the maximum capacitance variation to be detected. In the state of the art, some methods that allow to overcome this drawback for differential CBCM have been reported. In particular, in [17,20], adjustable current mirrors are exploited, while in [19], a floating-gate trimming circuit is adopted. These methods, however, require cumbersome off-line trimming by an additional calibration step, executed cyclically before each measurement, implemented

through additional digital circuitry and human intervention. This calibration step can be very long and tedious, especially for large arrays of capacitive electrodes, since it must be executed for each sensing capacitance.

To overcome these limitations, in this paper we present a novel topology of differential CBCM that allows to compensate offset automatically and continuously. The solution exploits, for the first time in the literature, scramblers and dynamical element matching (DEM) to allow working without human intervention.

2. Analysis of the Differential CBCM

2.1. Working Principle

The schematic of fully differential CBCM amenable for fully integrated implementation, which was first proposed in [18,19], is reported in Figure 1. A couple of pseudo-inverters (M1, M3 and M2, M4) charge/discharge the sensing capacitor, C_s, and the reference capacitor, C_r. The pseudo-inverters are driven by clock phases φ_1 and φ_2, which are set to avoid short-circuit currents from V_{DD} to ground, i.e., concurrent activation of transistors M1–M3 and M2–M4.

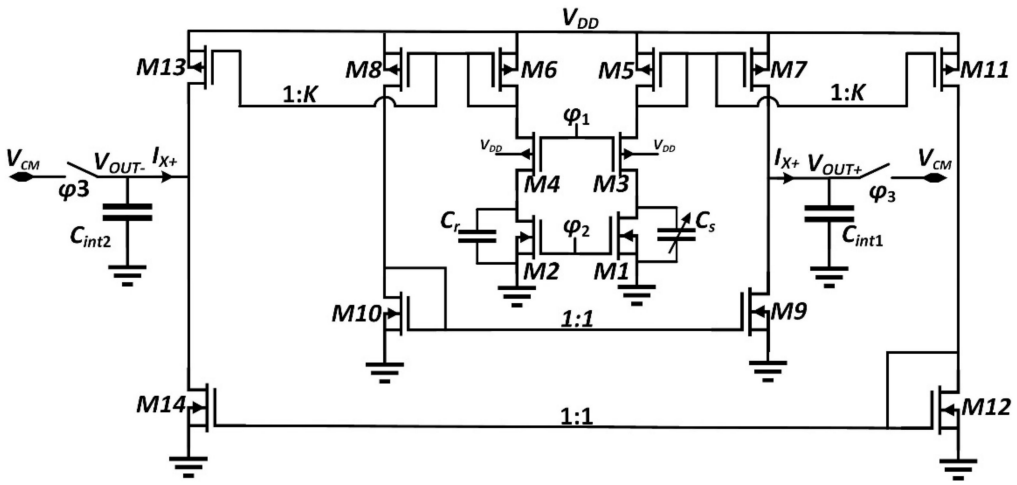


Figure 1. Schematic of the differential CBCM structure.

When clock phases φ_1 and φ_2 are low, C_s and C_r are charged through transistors M3 and M4. Current mirrors M5–M7, M6–M8 and M9–M10 enable subtraction of the instantaneous currents flowing in C_s, yielding

$$I_{X+}(t) = I_{M7}(t) - I_{M9}(t) = K\left(C_s\frac{dV_{Cs}}{dt} - C_r\frac{dV_{Cr}}{dt}\right) \quad (1)$$

where K is the gain of current mirrors M5–M7 and M6–M8.

The current I_{X+} is averaged by capacitor C_{int1}, yielding over one clock period, T_S

$$\overline{I_{X+}} = \frac{1}{T_s}\int_0^{Ts} I_{X+}(t)dt = \frac{K}{T_s}\int_0^{V_{DD}-|V_{TP}|}\left(C_s\frac{dV_{Cs}}{dt} - C_r\frac{dV_{Cr}}{dt}\right)dt \approx \frac{K\Delta C(V_{DD}-|V_{TP}|)}{Ts} \quad (2)$$

where V_{TP} is the threshold voltage of transistors M5 and M6 and $\Delta C = C_s - C_r$. The rightmost approximation in Equation (2) holds considering that C_S and C_r are charged to nearly $V_{DD} - |V_{TP}|$ in one clock period.

The common mode voltage at the output of the CBCM circuit in Figure 1 is set to V_{CM} by two auxiliary switches driven by the clock phase φ_3 whose period, T_3, should be sufficiently higher than *Ts*. Using Equation (2), the output voltage is expressed by

$$V_{out+} = \frac{K\Delta C(V_{DD} - |V_{TP}|)}{T_s} \cdot \frac{T_3}{C_{\text{int1}}} \quad (3)$$

From Equation (3), it is apparent that by increasing the switching frequency or the supply voltage, the output voltage can be increased.

Due to circuit symmetry in Figure 1, we get $I_{X+} = -I_{X-}$ and, consequently, $V_{out+} = -V_{out-}$ (i.e., the differential output voltage is twice the value predicted by Equation (3)). When φ_2 is high, the sensing and reference capacitors are discharged by M1 and M2. In this phase, PMOS of the pseudo-inverters are turned off, therefore the rest of the circuit is decoupled from the core and, neglecting leakage currents, the integration capacitors would maintain the charge gained during the previous clock cycle.

2.2. Simulation Results

The circuit in Figure 1 is designed and simulated using a standard 130-nm CMOS technology provided by STMicroelectronics. The supply voltage, switching period and common mode voltage is set equal to 3.3 V, 30 ns and 0.9 V, respectively. Although the nominal supply voltage of the adopted technology is 1.8 V, the high thickness field oxide devices are adopted for the circuit in order to increase the supply voltage to 3.3 V, which in turn allows increasing the output voltage level, as predicted by Equation (3). The common-mode voltage is fixed to 0.9 V, which is equal to half the supply voltage (equal to 1.8 V) of the comparator connected at the output of the circuit, which is not reported in this paper. The adopted main parameters for the circuit in Figure 1 are reported in Table 1. The absolute value of the reference and sensing capacitor plays a fundamental role in the circuit performance, but it cannot be freely set by the designer since it is related to the specific application. In our case, the circuit in Figure 1 is designed for a particulate matter detector where the value of C_s and C_r depends on the physical dimension of the capacitive electrode while the capacitance variation is in the order of tens of attofarads [21,22].

Table 1. Main parameters of the circuit in Figure 1.

Parameter	Value
M1, M2	1 µm/0.5 µm
M3, M4	3 µm/0.5 µm
M5, M6, M7, M8, M11, M13	2 µm/2 µm
M9, M10, M12, M14	5 µm/10 µm
K	2
$C_{int1,2}$	5 pF
$C_{s,r}$	1 fF

Figure 2 shows the differential output voltage, $V_{out+} - V_{out-}$, when a capacitance difference ΔC equal to 10 aF is applied at 150 µs. The figure confirms the behavior predicted by the analysis reported in Section 2.1.

Figure 3 compares the simulated transcharacteristic of the circuit in Figure 1 assuming T_3 equal to 300 µs, with the theoretical values predicted through Equation (3). The simulated sensitivity is equal to 22 mV/aF.

The error between the two curves in Figure 3 is lower than 10% for $\Delta C \leq 60$ aF and increases up to 20% for higher capacitance difference values due to the nonlinearity of the simulated transcharacteristic. The nonlinear behavior of the circuit can be justified considering that the actual mirror current gain, K, is not constant but, due to the channel length modulation effect, is also a function of the output voltage V_{out+} and V_{out-}. Note that this effect regards all the current mirrors connected to the output nodes (i.e., M5–M7,

M6–M13, M9–M10). The variation of the current mirror gain is therefore more pronounced for high values of ΔC, thus justifying the simulated behavior in Figure 3.

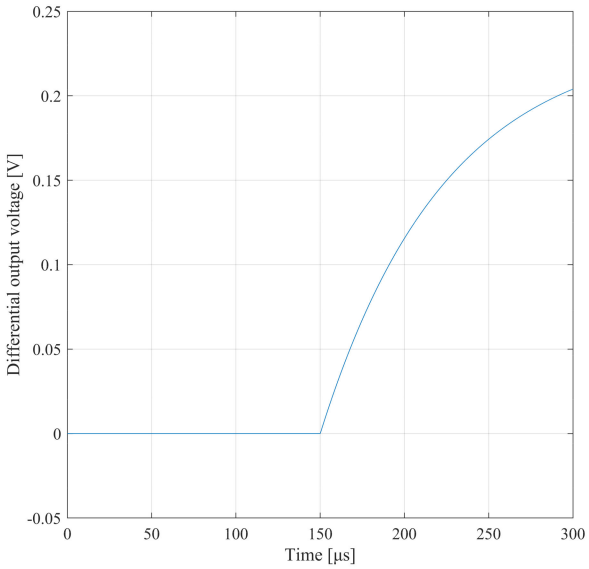


Figure 2. Simulated differential output voltage of the traditional CBCM in Figure 1 with ΔC = 10 aF at 150 µs.

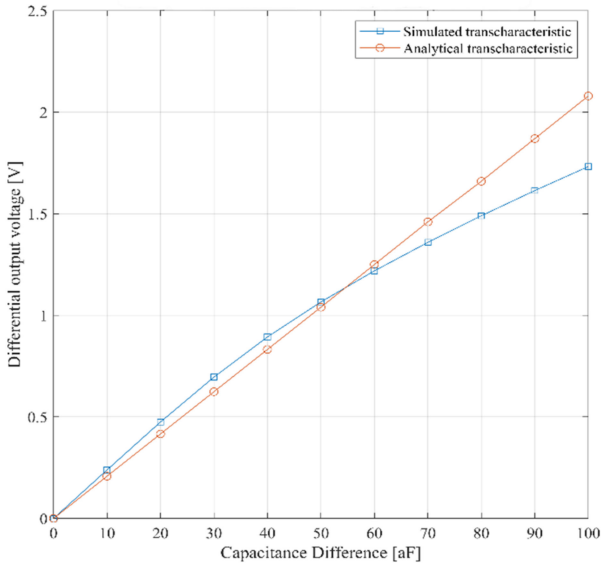


Figure 3. Transcharacteristic of the traditional CBCM in Figure 1.

Note, however, that the non-linearity of the transcharacteristic in Figure 3 does not represent an issue in applications requiring the "activation" of a capacitive electrodes, like, as an example, airborne particle counters [10–12,21,22]. Nonetheless, the linearity of the circuit can be increased by adopting cascode current mirrors.

The critical issue of the CBCM system is the output offset caused by mismatch and process variations. Random mismatch variations can be evaluated by using the mismatch model in [23]:

$$\sigma_{\frac{\Delta I_D}{I_D}} = \sigma_{\frac{\Delta k}{k}} + \frac{g_m}{I_D}\sigma_{\Delta V_{th}} \quad (4)$$

where $\sigma_{\frac{\Delta k}{k}}$ and $\sigma_{\Delta V_{th}}$ are inversely proportional to the active area, while the ratio of gm and drain current is related to the transistor working region.

Regarding the mirrors, due to the very low charging currents, they are expected to work in the weak inversion saturated region. While the standard deviation of the variation of threshold can be minimized increasing the transistor area, the ratio between transconductance and drain current is the maximum, that is, a fundamental condition of the transistor operating in weak inversion. This condition leads to the conclusion that a residual mismatch is still caused by the subthreshold operating point even if the area is very high.

To better understand the effect of mismatches, let us consider, as an example, a mismatch between transistors M3 and M4 in Figure 1. In nominal condition (i.e., $\Delta C = 0$), this mismatch will cause a charge difference, Q, during each switching cycle. If the charge flowing in M3 is bigger than that of M4, the integrating capacitor C_{int1} accumulates more charge than C_{int2}, thus generating a differential output voltage offset expressed by

$$V_{diff,offset} = 2N\frac{\Delta Q}{C_{\text{int1,2}}} \tag{5}$$

where N is the number of clock cycles. According to the value of ΔQ and N, mismatch can cause an output voltage as high as the power supply. Of course, the same reasoning can be extended to any other couple of matched transistors.

As a confirmation of the analysis reported above, Figure 4 reports the Monte Carlo simulations over 100 runs of the differential output voltage of the traditional CBCM in Figure 1 assuming $\Delta C = 0$ aF. It is apparent that the circuit shows standard deviation of the differential output voltage equal to about 1.35 V. Such a huge variation prevents the use of this simple topology unless a proper compensation strategy is adopted [17,19,20].

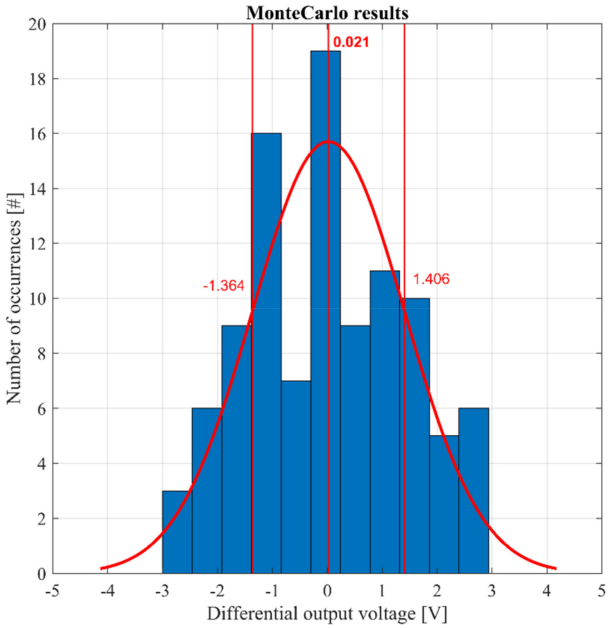


Figure 4. Monte Carlo simulation results for the circuit in Figure 1.

3. The Proposed Auto-Compensated CBCM Circuit

3.1. Working Principle

In order to decrease the standard deviation of the differential output voltage, an auto-compensated topology is proposed as shown in Figure 5. First of all, three ancillary blocks, called "scramblers", have been added to the central core, to the reference and sensing capacitors and to the 1:1 mirrors. The scramblers are driven by two non-overlapping clock phases and periodically swap the drains of transistors, or the sensing and reference capacitors. In this way, in one semi period, the connection is the direct one (looking at the

central core M1-C_s-M3), while in the second semi period, the connection is through M1-C_r-M3. Consequently, the mismatch current is averaged, thus reducing the equivalent offset.

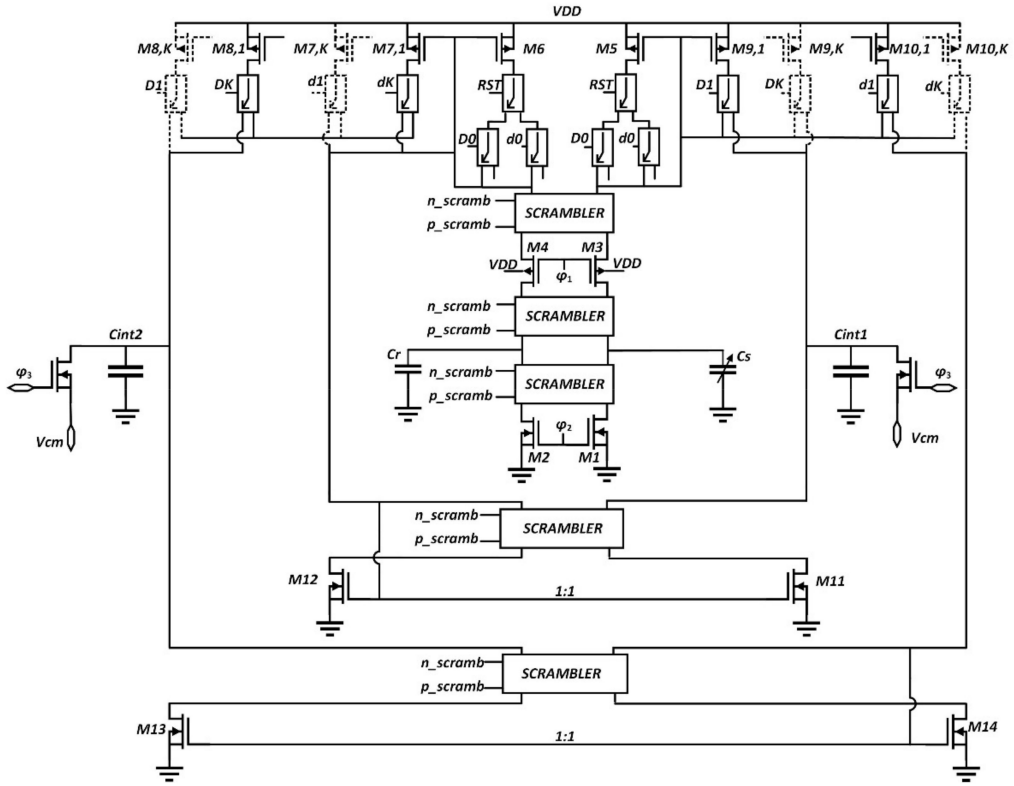


Figure 5. Schematic of the proposed auto-compensated CBCM circuit.

Let us consider again, as an example, a mismatch between transistors M3 and M4 in nominal condition (i.e., $\Delta C = 0$). By periodically swapping the drains of M3 and M4, the charge mismatch will be averaged over time. Assuming that the clock period of the scrambler, t_{scramb}, is lower than the clock period, T_s, of the main phases φ_1 and φ_2, a simplified diagram of the differential output voltage is shown in Figure 6. It is worth noting that the principle of operation is like that of the chopping technique [24].

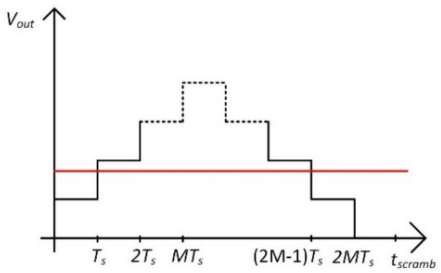


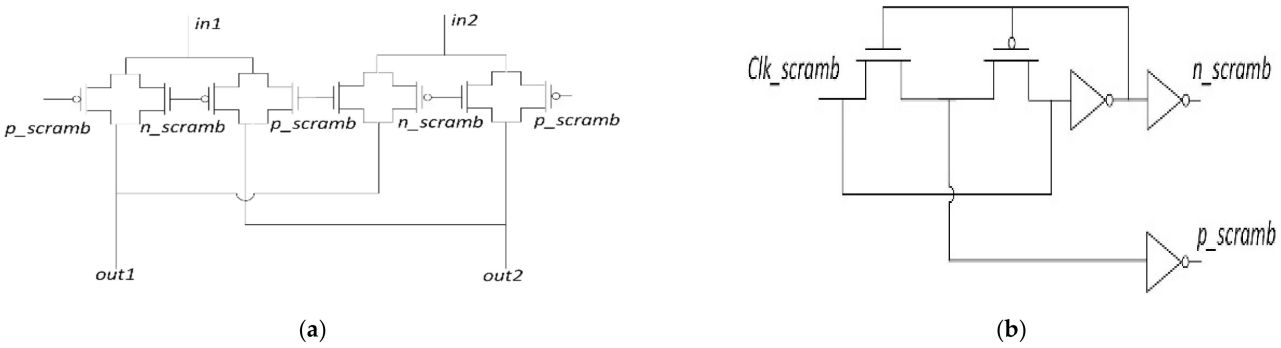
Figure 6. Output voltage over one period of the clock of the scrambler.

If the ratio t_{scramb}/T_s is an integer number, M, it is apparent that if M3 and M4 are exchanged at the Mth main clock cycle, at the $2M$th clock cycle, the differential voltage is averaged and the offset to due mismatch is eliminated. In general, the differential voltage function is a growing and decreasing series of steps with an average value that increases as M increases, as shown in the following equation:

$$\overline{V_{out}} = \frac{\sum_{a=1}^{M/2} \frac{2a\Delta Q}{C_{int1,2}} T_s - \sum_{b=1}^{M/2} \frac{(M-2b)\Delta Q}{C_{int1,2}} T_s}{t_{scramb}} = \frac{\sum_{a=1}^{M/2} 2a\Delta Q - \sum_{b=1}^{M/2} (M-2b)\Delta Q}{MC_{int1,2}} \quad (6)$$

Obviously, this reasoning can be applied to every pair of symmetrical transistors, thus reducing the total average error. Note, however, that the offset between the nominal values of C_s, C_r and C_{int1}, C_{int2} must be compensated by an additional trimming circuit, like that proposed in [25].

The schematic of the scrambler is represented in Figure 7a, where the aspect ratios are 1 µm/0.5 µm and 3 µm/0.5 µm for NMOS and PMOS transistors, respectively. The scrambling circuit is basically a passive mixer driven by two 180° phase-shifted waves generated by the circuit in Figure 7b. When phase *n_scramb* is high, the central pair of transmission gates is open while the rightmost and leftmost part are a low impedance path, thus the classic connection of the CBCM. When phase *p_scramb* is high, the condition is the opposite, therefore the connections are swapped. The aspect ratios is 0.8 µm/0.5 µm for all transistors in Figure 7b.



(**a**) (**b**)

Figure 7. (**a**) Schematic of the scrambler circuit; (**b**) schematic of the scrambler phase generator.

To reduce the offset due to the mismatch of the 1:*K* current mirrors, an approach similar to the dynamical element matching (DEM) technique is adopted [26]. Each diode-connected transistor is periodically swapped with the other transistors of the current mirror. The schematic of the switch connected to the drains of the transistors of the 1:*K* current mirrors is shown in Figure 8, where the aspect ratios are 2.4 µm/0.5 µm and 0.8 µm/0.5 µm for NMOS and PMOS transistors, respectively. The 10-bit binary word $D < 0{:}K >$ is made up by a series of zeroes with only a "1" that moves cyclically from the right to the left and is generated by a finite state machine (FSM). When the signal *D*1 is high, the rightmost transmission gate is a low impedance path therefore, taking in account the M5-M9 mirror, the M9,1 PMOS exchanges with the diode connected. In the third period, the diode connected MOS is exchanged with the second PMOS M9,2, etc. In the first state, when D0 is high, the situation is the classical one. In this way, the mismatch of a mirror is reduced, producing an average offset much smaller than the uncompensated version.

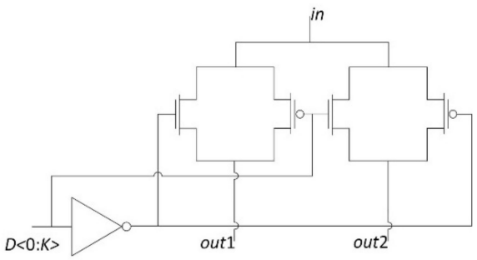


Figure 8. Schematic of the switch connected to the drains of the transistors of the 1:*K* current mirrors.

The diode connected PMOS overhangs a combination of three scramblers, because the diode connected PMOS in a first phase is exchanged with the PMOSs that overhang the output node, then with the PMOSs that overhang the diode connected NMOS (therefor, two different FSM that are set and reset by two signal in phase opposition). The parallel of

the two scramblers under the principal one are unable/enabled by the reset signal of the memory part of the FSM.

3.2. Simulation Results

The proposed circuit in Figure 5 has been simulated using the same parameters reported in Figure 1. The switching period of the scramblers is set equal to 600 ns (i.e., M = 20 in Equation (6)). The FSM clock period is set equal to 60 ns.

Figure 9 shows the differential output voltage, $V_{out+} - V_{out-}$, when a capacitance difference ΔC equal to 10 aF is applied at 50 µs. As compared to the traditional solution, the output voltage variation is reduced. This is due to the effect of the transistors implementing the switches of the scramblers and the DEM circuit that cause a reduction of the charging current into the integrating capacitors. The magnitude of the ripple in Figure 9 is due to the scramblers and, in particular, to the DEM applied to the current mirrors. This ripple can either be reduced by degenerating the mirror devices or trimming it before doing DEM. Alternatively, DEM ripple can also be suppressed by an additional low pass filter.

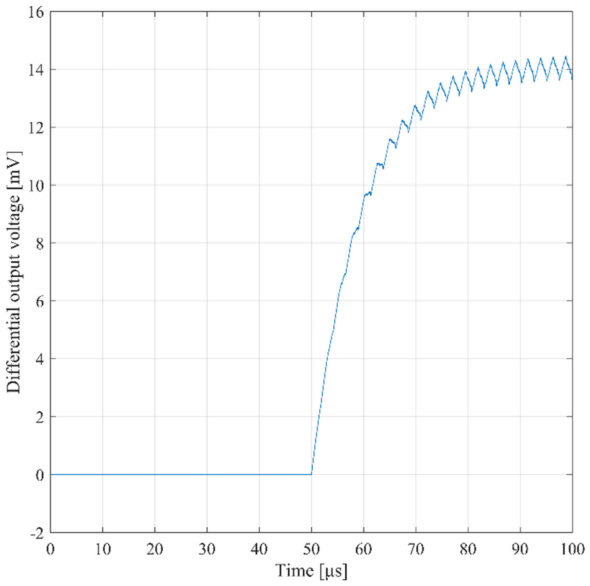


Figure 9. Simulated differential output voltage of the proposed circuit in Figure 5 with ΔC = 10 aF at 50 µs.

Figure 10 reports the transcharacteristic of the circuit in Figure 5 assuming T_3 is equal to 100 µs. The sensitivity is equal to 1.3 mV/aF, therefore it is 17 times lower than that of the traditional solution.

Finally, Figure 11 reports the Monte Carlo simulations over 100 runs of the differential output voltage of the proposed circuit assuming ΔC = 0 aF. It can be noted that now the standard deviation has been reduced to about 65 mV, which is about 20 times lower than that of the traditional solution.

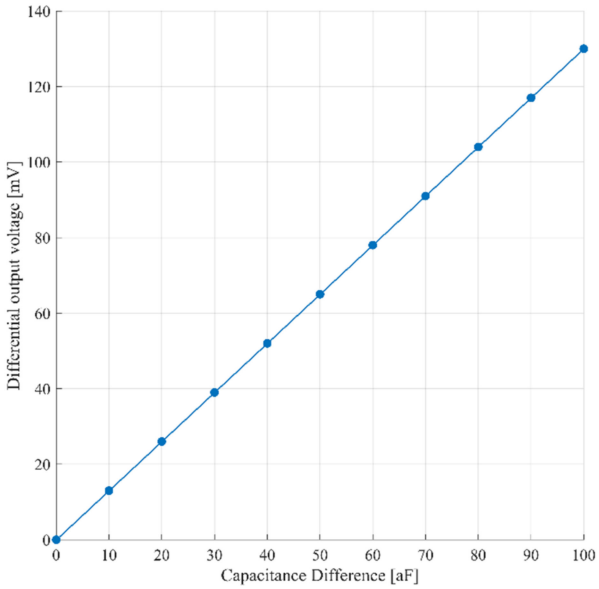


Figure 10. Transcharacteristic of the proposed CBCM in Figure 5.

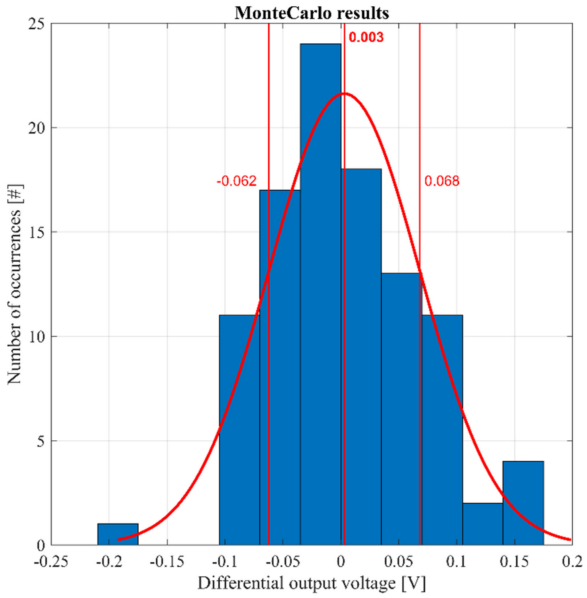


Figure 11. Monte Carlo simulation results for the circuit in Figure 5.

4. Conclusions

In this paper an automatic offset cancellation topology is proposed to improve the performance of the differential CBCM. The proposed circuit allows reducing the offset of the output voltage due to mismatches in an automatic way by exploiting scramblers and DEM technique. Simulation results shows the effectiveness of the proposed strategy, which allows a 20× reduction of the standard deviation, but with a 14× reduction of the sensitivity. The performance increase, moreover, is paid by additional area occupation and circuit complexity, but it is worth noting that the offset is automatically and continuously reduced without human intervention, thus enabling the adoption of the CBCM topology in those applications where hundreds of capacitive electrodes must be processed in parallel.

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