electronics

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A 28 nm Bulk CMOS Fully Digital BPSK Demodulator for US-Powered IMDs Downlink Communications

Andrea Ballo, Alfio Dario Grasso * and Marco Privitera

Department of Electrical, Electronic and Computer Engineering, University of Catania, Viale A. Doria, 6, 95125 Catania, Italy; andrea.ballo@unict.it (A.B.); marco.privitera@phd.unict.it (M.P.)
* Correspondence: alfiodario.grasso@unict.it

Abstract: Low-invasive and battery-less implantable medical devices (IMDs) have been increasingly emerging in recent years. The developed solutions in the literature often concentrate on the Bidirectional Data-Link for long-term monitoring devices. Indeed, their ability to collect data and communicate them to the external world, namely Data Up-Link, has revealed a promising solution for bioelectronic medicine. Furthermore, the capacity to control organs such as the brain, nerves, heart-beat and gastrointestinal activities, made up through the manipulation of electrical transducers, could optimise therapeutic protocols and help patients' pain relief. These kinds of stimulations come from the modulation of a powering signal generated from an externally placed unit coupled to the implanted receivers for power/data exchanging. The established communication is also defined as a Data Down-Link. In this framework, a new solution of the Binary Phase-Shift Keying (BPSK) demodulator is presented in this paper in order to design a robust, low-area, and low-power Down-Link for ultrasound (US)-powered IMDs. The implemented system is fully digital and PLL-free, thus reducing area occupation and making it fully synthesizable. Post-layout simulation results are reported using a 28 nm Bulk CMOS technology provided by TSMC. Using a 2 MHz carrier input signal and an implant depth of 1 cm, the data rate is up to 1.33 Mbit/s with a 50% duty cycle, while the minimum average power consumption is cut-down to 3.3 µW in the typical corner.

Keywords: BPSK modulation; energy harvesting; implanted medical devices; ultra-low-power; ultrasonic wireless link

Citation: Ballo, A.; Grasso, A.D.; Privitera, M. A 28 nm Bulk CMOS fully Digital BPSK Demodulator for US-Powered IMDs Downlink Communications. *Electronics* **2022**, *11*, 698. https://doi.org/10.3390/electronics11050698

Academic Editor: Kiat Seng Yeo

Received: 15 January 2022
Accepted: 22 February 2022
Published: 24 February 2022

1. Introduction

In recent years, a considerable portion of the electronics field has been focused on bioengineering applications. The modern internet of medical things (IoMTs) or the body area networks (BANs), as well as the less recent implantable neural prostheses, are proof that more and more attention is being paid to these kinds of applications. Looking to neurological and mental disorders, their impacts can often be alleviated by bioelectronics and neuroprosthetics medicine. Implantable neural prostheses, such as deep brain the Ref. [1], cortical [2] or nerve [3] stimulators and cochlear implants [4] are examples of clinically adopted neuro-technology to revert impaired or lost functions.

In general clinically adopted implantable neural prostheses, a micro-electrode array is kept in contact with the tissue and it is electrically linked, often by using cables, to a unit aimed at recording neuronal activities and/or for neural stimulation. The design principle has its roots back to the first fully implantable battery-powered pacemaker [5]. Since then, several variations of this design principle were used in many successful applications, despite having several critical limitations. For instance, the excessive intrusiveness and mechanical stresses that cables and connectors can have on human tissues are weak points of the system, often leading to failure. Moreover, due to its size, the implanted unit cannot be located close to the target tissue. Instead, it is placed in a remote location and wires are used to connect them to micro-electrode arrays for stimulation.

To get rid of this drawback, more recently adopted implantable neurostimulators have employed a wireless link for power and data transfer from/to the implanted IC. This constitutes a technological challenge in neurostimulation, whose state-of-the-art culminates with arrays of free-standing smart electrodes, not relying on powered units and wired connections [6]. Such smart electrodes should integrate all the required elements to receive power and operational commands (downlink communication), while the preserve size should be compatible with the intended application, ideally smaller than 1 mm^3. For this reason, the miniaturisation of the implantable device is crucial to achieve safe and noninvasive surgical implantation. Such a system is better-known with the acronym IMD, which stands for an "implanted medical device".

In this framework, as a part of wireless IMDs, we propose a new solution of a Binary Phase-Shift Keying (BPSK) demodulator in order to design a robust, low-area and low-power downlink for ultrasound (US)-powered implanted units. The implemented system is fully digital and PLL-free, thus reducing area occupation and making it fully synthesizable. Simulation results are reported using a 28 nm Bulk CMOS technology provided by TSMC.

The paper is organized as follows. Section 2 reports a system overview of US-powered implanted medical devices. Then, starting from the US-link characterization shown in Section 3, the proposed fully digital BPSK demodulator is introduced and described in each single block in Section 4. Section 5 shows post-layout simulation results of the proposed circuit as also compared with the state-of-the-art. Finally, the last section reports the conclusions of this work.

2. US-Powered IMDs: A System Overview

The system represented in Figure 1 is an illustrative description of the US-powered integrated circuit to be implanted in the human brain. It is worth noting that the same IC could be used for any specific biomedical application, such as heart-beat stimulations, gastrointestinal activities manipulation, and other kinds of controls and actuations applied to patients affected by chronic diseases [7–10]. The IMDs are powered-up, exploiting US-acoustic waves generated from external piezo-transducers (*TX-PIEZO*, in Figure 1) kept under the electrical resonance condition and placed in contact with the skin. Thus, once the acoustic waves reach the depth of a second power-receiving piezo-transducer (*RX-PIEZO*), they can be efficiently rectified and conditioned to power up a storage capacitor, namely C_{STOR}, in the Figure mentioned above. In fact, the described system is battery-less and plainly covers the concept of Energy Harvesting, exploiting the electro-acoustic coupling of two small, thick and low-invasive piezoelectric devices.

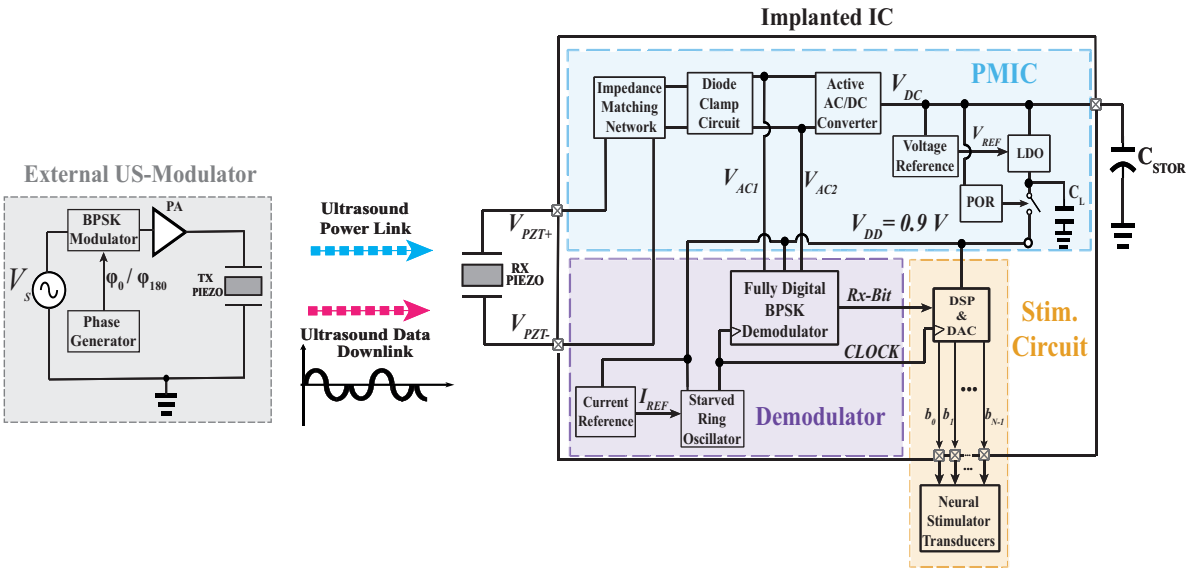

Figure 1. Simplified scheme of a US-powered IMD.

As depicted in most of the works presented in the literature on the Power Management Integrated Circuit (PMIC) for Energy Harvesting systems, as reviewed in the Ref. [11], the power conditioning circuit is often made up of an impedance matching network [12], an active AC/DC converter [13,14], a voltage reference [15] and a low-dropout voltage regulator (LDO) [16] that provides a regulated rectified voltage (i.e., $V_{DD} = 0.9\,\mathrm{V}$ in Figure 1). Moreover, starting from the experimental measurements conducted by the authors, a diode-clamping circuit could be necessary for those cases in which the maximum voltage amplitude raises the maximum allowable voltage for the adopted IC technology. Moreover, a Power-On Reset (POR) circuit, as the one shown in the Ref. [17], is often needed to enable/disable the load circuitry.

On the other hand, two further subsections are presented in Figure 1, namely, the demodulator and stimulation circuit, both powered by the PMIC. Indeed, the presence of a communication sub-system for an IMD is mandatory, since it allows to establish data communication between the IMDs and the external world for long-term monitoring and stimulation purposes. In particular, the feature of collecting data and communicating them to the external world, namely Data Up-Link, has revealed a promising solution for bioelectronic medicine that exploits these devices [7]. Furthermore, the ability to act on neurons, nerves, the heart-beat, and gastrointestinal activities, made up through the manipulation of electrical transducers, could optimise therapeutic protocols and help relieve patients' pain [10]. These kinds of stimulations come from the modulation of a powering signal generated from an externally placed unit coupled to the implanted receivers for power/data exchanging. The established communication is also defined as a Data Down-Link. Thus, an incoming-signal demodulator is needed to acquire an external signal to properly drive the above-mentioned electrical transducers. Then, the received information is elaborated into an implanted processing unit (i.e., a Digital Signal Processor, DSP, or a Field Programmable Gate array, FPGA) that works together with a Digital-to-Analog Converter (DAC), allowing for the electrical stimulation of the nerves/brain, as schematically represented in Figure 1.

This work mainly concerns the design of a US-Data Down-Link embedding the proposed fully digital BPSK demodulator. Indeed, the state-of-the-art presents several modulation schemes, such as the ASK [18,19], PWM-ASK [20], OOK [19,21,22], and OOK-PM [23,24], while the BPSK demodulation has often been used for RF-powered IMDs [25–31].

The choice of this modulation scheme arises from three main reasons. The first one regards the presence of a clamping circuit that often makes the amplitude demodulation on the incoming acoustic waves difficult; indeed, a variation of the voltage amplitude on the driving *TX-PIEZO* could not be proficiently detected once impinged on the implanted IC. The second motivation is the necessity of a continuous powering of the IMDs, making the efficient use of the On–Off Shift Keying (OOK) proposed in the Refs. [19,21,22] difficult. Finally, the last motivation arises from inspection of the graph reported in Figure 2. It shows the Bit-Error-Rate (BER) for different modulation schemes as a function of the Signal-to-Noise Ratio (SNR) defined as the ratio E_b/N_o, where E_b is the energy-per-bit and N_o is the noise power. Specifically, the compared schemes modulate the received signal amplitude (BASK), its frequency (BFSK), its phase (BPSK) or its phase with differential modulation (DPSK). It is possible to observe that the BPSK presents the lowest BER, for a given value of the SNR. Furthermore, if the BPSK demodulation system does not require any synchronization between the data transmitter and the data receiver, it is defined as a non-coherent BPSK modulation.

Assuming BPSK modulated the input signal, the external powering and modulating electronic system depicted in the left-most side of Figure 1 is essentially based on an FPGA that generates the sinusoidal signal at the piezo-transducers electrical resonance frequency, f_0, as well as a power amplifier (PA) which drives the *TX-PIEZO* with the suitable power level.

The FPGA acts as a modulator exploiting a proper digital signal, named *MOD*, that exchanges the two sinusoidal phases, φ_0 and φ_{180}, generating the following transmitted signal

$$V_{PZT}(t) = \begin{cases} \sin(2\pi f_0 t + \varphi_0) = \sin(2\pi f_0 t) & \text{if } MOD \text{ is low} \\ \sin(2\pi f_0 t + \varphi_{180}) = \sin(2\pi f_0 t + 180°) & \text{if } MOD \text{ is high} \end{cases} \quad (1)$$

As shown in Figure 1, the implanted demodulator of the integrated system requires a robust oscillator (i.e., current starved ring (CSRO) oscillator, as proposed in the Ref. [6]). However, it is worth noting that the internal oscillator of the implanted processing unit could be equivalently used, thus reducing both the area occupation and the power consumption of the entire data-receiving system.

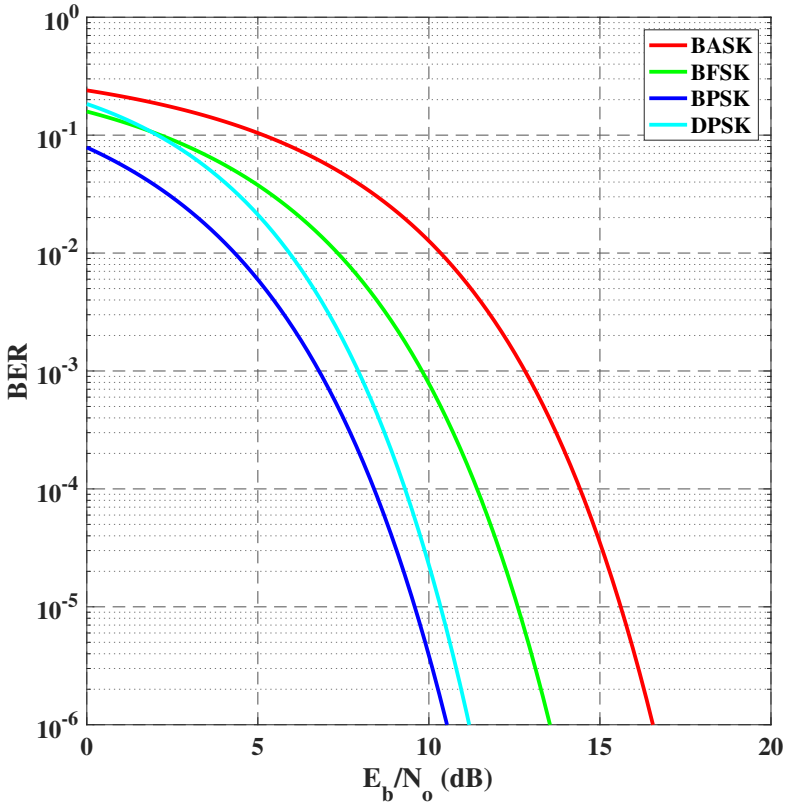

Figure 2. BER vs. SNR (E_b/N_o) for binary modulation schemes: comparison by applying theoretical equations shown in the Ref. [32]. The graph was obtained by using the MATLAB code reported in [33], supposing a AWGN channel and a unitary energy-per-bit, while the bit signal length is 10^5.

3. Characterization of the US Data Link

Since the features of links for power and data transfer determine part of the specifications for the all the implemented devices and, in particular, for PMIC and the demodulator, this section focuses on its characterization. It consists of two piezoelectric devices. The first one is the power transmitting piezo, TX PIEZO, which is placed outside the body and used to transfer power and transmit data to the implanted device (down-link); the other one is the RX PIEZO which, as indicated in Figure 1, is implanted together with the entire IC. It harvests the transferred power, receives data, and is also used to send data to the outside device (up-link). US-piezo receivers were selected among the ones present on the market, trying to carry out the best trade-off between dimensions, operating frequency, and the maximum transferable power. As per the results of previously conducted studies, the operating frequency under an electrical resonance condition was selected to be equal to $f_0 \sim 2$ MHz, for both piezoelectric devices, with a thickness, t, of about 0.4–0.5 mm for the receiving piezo. This choice was due to a trade-off between the miniaturization

requirement and the harvested power. In order to emulate the acoustic impedance of body tissues, ballistic gel was used. This solution was already adopted in various medical fields, such as the anthropomorphic cardiac phantom for ultrasound imaging, and thanks to its acoustic properties, and compatibility with conventional plastics molding techniques, it has been designated as among the best materials for tissue-mimicking [34]. Considering that both piezoelectric transducers should be separated by a physical sandwich composed by the skin, vessels, and cerebral cortex, the distance between them should be in the order of d = 0.5–1.5 cm; in this way, both the devices are encapsulated in ballistic gel, keeping such a distance fixed.

As for the materials selection, they are the same as that used in the Ref. [14]. The TX-PIEZO is the PRY+0111 provided by PI Ceramics. It is made up by a disk of PIC255 with a diameter equal to 10 mm, with a radial resonant frequency equal to 250 kHz and a transverse resonance frequency equal to 2 MHz. As for the RX-PIEZO, it is the 000065944 provided by the same manufacturer. It is a thin layer of PIC255, with a square form whose area is equal to 9 mm^2 and a thickness of t = 0.5 mm; its radial resonance frequency is placed at 500 kHz, while its transverse resonant frequency is about 2 MHz. Figures 3 and 4 show the US-data link for testing and the RX-PZT. In detail, Figure 3 shows the encapsulation in ballistic gel with a fixed distance, $d = 1.0$ cm between the RX-PZT and the TX-PZT to mimic the acoustic impedance of tissues, while Figure 4 presents the block diagram of the experimental measurement setup used for the characterization of the US-power link. A signal generator was used to drive the RX-PZT with a 20-V_{pp} sinusoidal signal, while an oscilloscope measured the received electrical signal over the TX-PZT.

Let us now consider the definition of wavelength; $\lambda = v/f$, when $f = f_0 = 2$ MHz and $v \sim 1540$ m/s, it follows that $\lambda = 0.77$ mm. It means that the distance $d = 1$–1.5 cm is quite large compared to the US-wavelength in tissues, so the waves propagate in a far-field region. This is further demonstrated by considering (2). In fact, it is worth remembering that the distance between the last sound pressure's maximum value and the sound source is called the near-field length, which is expressed by N, and the area within the N is called the near-field area. The region where the distance from the axis of the wave source is greater than the length of the near-field region is called thefar-field region. The ultrasonic near-field area can be calculated by the following equation [35]:

$$N \approx \frac{D^2}{4\lambda} = \frac{A}{\pi\lambda} \sim 3.7\,\text{mm} \tag{2}$$

where D is the diameter of the material, and A, its area, equals to about 9 mm^2, while λ is the US-wavelength in tissues. This proves that the system works in the far-field region.

The impedance characterization of the devices was carried out using a VNA (E5061B provided by Keysight Technologies), measuring out both the magnitude of the impedance, $|Z|$, and the phase ϕ as functions of the frequency. Both piezo devices were connected to the VNA, and the equivalent Butterworth–Van Dyke (BVD) electric circuits were carried out. Furthermore, resonance doublets were depicted by using two parallel RLC series circuits but, as claimed before, for the power transfer to the implanted device, just the electric resonance is important. The piezo devices, under the electrical resonance condition, presents finite impedances (in the order of magnitude of 0.1–1 kΩ), when acting as a passive component (e.g., the TX-PIEZO). On the other hand, the Thévenin equivalent model deals with the concept of active generation when resonance for the RLC series circuit occurs (see Figure 5c)). The received voltage amplitude falls in the following range $V_{PZT} \in [2.0\text{–}4.5]$ V, while the received power in $P_{RX} \in [1.0\text{–}3.0]$ mW and the equivalent series resistance is $R_{PZT} \in [0.5\text{–}1.5]$ kΩ. A peak-to-peak sine signal applied to the TX-PZT equals to 20 V_{pp}, and the electrical resonance frequency is the same as that of the RX-PZT, $f_0 = 2$ MHz.

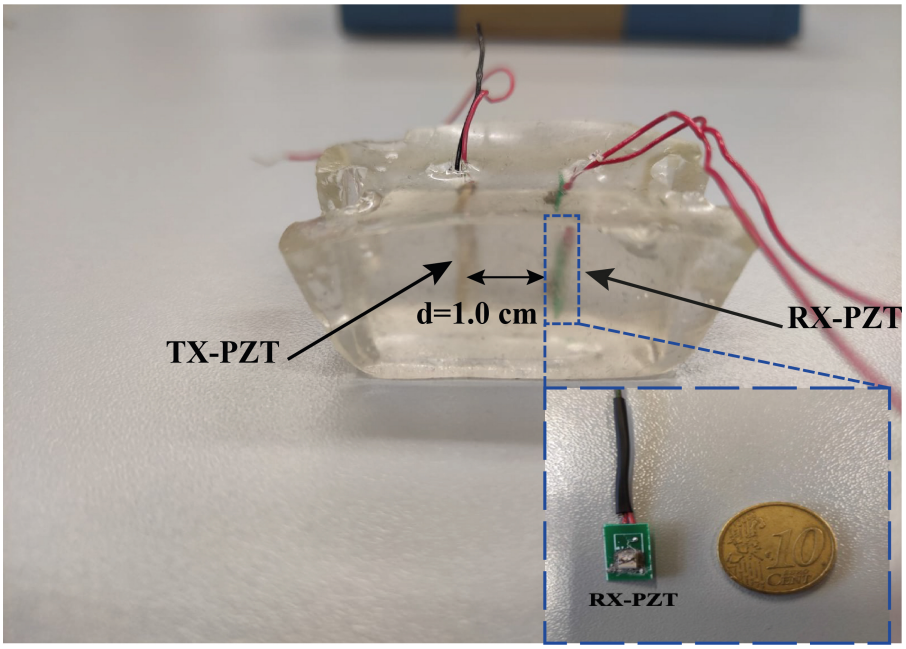

Figure 3. TX-PZT and RX-PZT encapsulated in ballistic gel at a distance of about 1.0 cm and the RX-PZT device compared to a 10 cent coin.

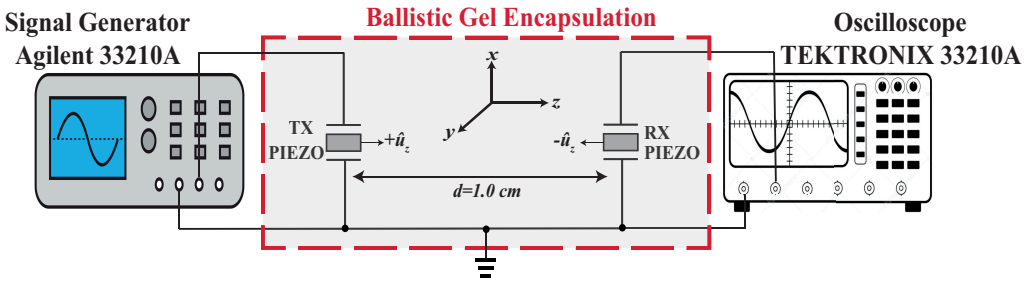

Figure 4. The experimental measurements setup used, including ballistic gel for the encapsulation of the two piezoelectric transducers.

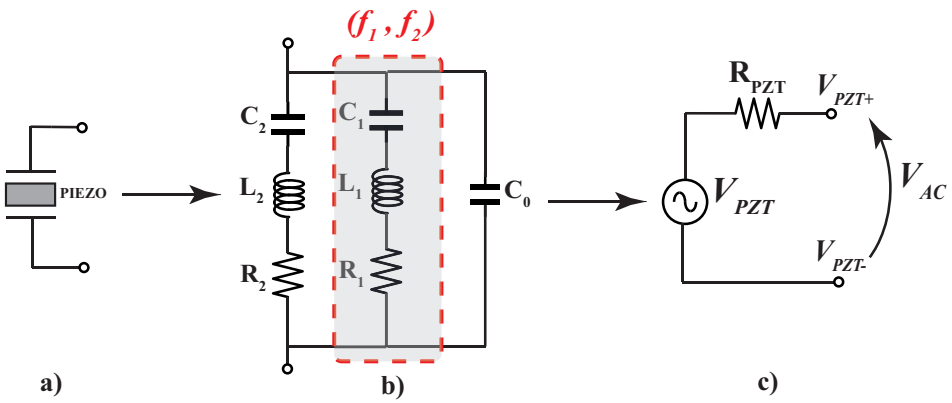

Figure 5. (**a**) The piezoelectric device, (**b**) BDV model with two resonance doublets, and (**c**) its equivalent Thévenin model assuming electric resonant conditions.

4. The Proposed Fully Digital BPSK Demodulator

The Binary Phase Shift Keying (BPSK) is the most famous PSK modulation, and the most widely adopted method to recover data from a BPSK signal is the Costas loop for coherent modulation schemes [36]. As explained in the Ref. [25], the above-cited loop consists of two parallel phase-locked loops (PLLs), where one is called the *in-phase loop*, *IPL*, and

the other is called the *quadrature-phase loop, QPL*. Their phase error outputs are multiplied to control the frequency of the oscillator. The square term of the data stream makes the control signal proportional to the phase difference as the conventional PLL and, in the locked state, the output at the in-phase branch becomes the demodulated signal. Generally, a four-quadrant analog multiplier is adopted to realize the I/Q arm phase detector and the multiplier in the voltage-controlled oscillator (VCO) branch. Such complexity in terms of the needed circuitry constitutes the main drawback of the conventional *Costas loops* for BPSK demodulators, limiting its use in practical applications.

On the other hand, recent works have exploited digital architectures for BPSK demodulation [26,28,30,31]. Many schemes have adopted a 1-bit Analog-to-Digital Converter (ADC) implemented with Schmitt's Triggers, a clock-recovery circuit and D-Flip-Flops (DFFs) whose role is as frequency dividers or as counters. However, it is important to underline that most of them present a *non-coherent* demodulation scheme, since phase synchronization is not required with the source of the modulated signal.

The system proposed in this paper falls within the last family. Figure 6 shows the simplified block diagram of the whole BPSK demodulator and its working principle is explained in the following, with the help of the timing diagram reported in Figure 7.

1. The two input sinusoidal waves that come out from the *RX-PIEZO* are firstly clamped out, and, consequently, they degenerate two semi-square waveform signals, namely $V_{AC1,2}$, in Figure 6. When the phase modulation occurs, one of the two phases will present a doubled time duration. In this paper, just the negative sine phase, V_{AC2}, is taken into account as the incoming modulation signal is high (i.e., *MOD* in Equation (1) is high).
2. A non-overlapping phase generator is strongly required, since it allows to better separate and distinguish, from a temporal point of view, the two clamped-sine incoming phases and to detect the bit-start/end signals. Moreover, its output, V_{P2}, is the resulting modulating phase.
3. A current-starved ring oscillator starts oscillating just when the enabling phase (V_{P2}) is high.
4. The core of the proposed demodulator is constituted by a 2-bit frequency divider and a CMOS XOR gate which allows to count the number of pulses generated by the ring oscillator, when enabled by V_{P2}. Briefly, the changes in the output bit state happen when a doubling on the number of pulses of the oscillator occurs (i.e., two clock pulses are generated when *MOD* goes high and, vice-versa, a single clock pulse when no modulation occurs). In such event, the two output states Q_0 and Q_1 will present different time durations, and this difference will be detected by the XOR gate.
5. The pulses generated by the XOR gate, XOR_{out}, which are slightly delayed as indicated Δt in Figure 7, allows the reconstruction of the bit '1' from the modulator. It must be noted that the time delay is symmetric and equal for both the rising and falling edges of the received bit and, therefore, the time delay does not affect the demodulated data.

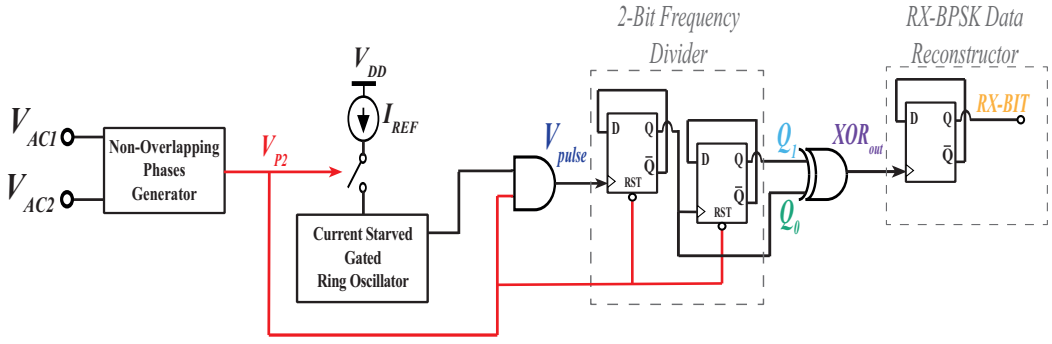

Figure 6. Block diagram of the proposed BPSK demodulator.

Concerning the data frequencies that could be achieved with such a demodulation system, they are identified starting from the timing diagram in Figure 7 and using the following equations,

$$T_{BPSK,ON}(n) = T_{RX,ON}(n) = \frac{3}{2}T_0 + nT_0, \quad n \in \mathbb{N}_0 \tag{3}$$

$$f_{RX}(n) = \frac{1}{T_{RX}(n)} = \frac{1}{T_0(3+2n)} = \frac{f_0}{(3+2n)}, \quad n \in \mathbb{N}_0, \tag{4}$$

where T_0 is the oscillation period and f_0 is the oscillation frequency of the US-wave source, $T_{BPSK,ON}$ is the BPSK-bit '1' duration, and $T_{RX} = 2T_{BPSK,ON}$ is the period of the received data. The maximum bit rate, B^{MAX}, is established when $n = 0$ and it is equal to

$$B^{MAX} = 2 \cdot f_{RX}(n=0) = 2 \cdot f_{RX}^{MAX} = \frac{2}{3T_0} = 2\frac{f_0}{3} \tag{5}$$

In the case under analysis, the natural index n was set as equal to zero, while $T_0 = 500\,\text{ns}$ and $f_0 = 2\,\text{MHz}$, giving as results of Equations (4) and (5), that the time of the received BPSK signal is $T_{ON,BPSK} = 750\,\text{ns}$, while the bit rate is 1.33 MHz. Moreover, the modulation/demodulation frequency, as well as the bit rate, could be changed and reduced. Indeed, for most of the neural stimulation applications, the required bit rate goes from a few kb/s up to hundreds of kb/s.

The adopted technology is a 28 nm bulk CMOS process provided by TSMC. The SVT thick-oxide transistors were used since they could work up to 1.8 V. The thickness of the oxide was $C_{OX} \simeq 10\,\text{fF}/\mu\text{m}^2$, while the threshold voltages of NMOS and PMOS transistors were respectively $V_{tn} \simeq 450\,\text{mV}$ and $|V_{tp}| \simeq 460\,\text{mV}$, for $L_{n,p} = 4L_{min} = 0.6\,\mu\text{m}$. The simulation environment used was CADENCE VIRTUOSO.

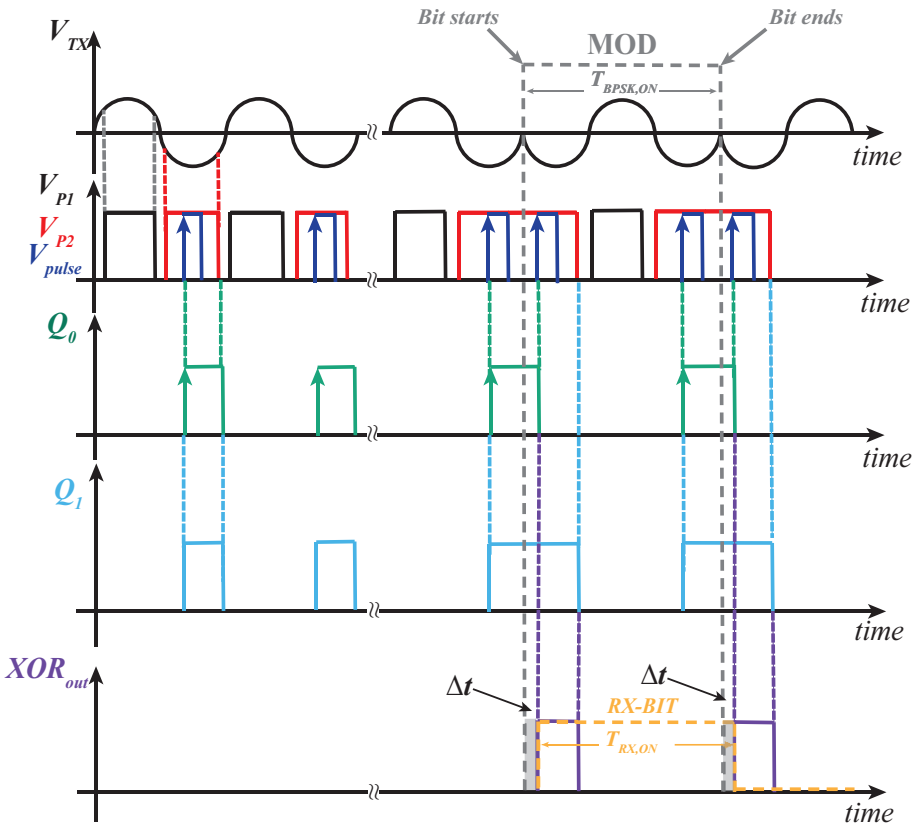

Figure 7. Timing diagram of the proposed demodulator circuit.

The following subsections report an in-depth description of each single block that compose the system in Figure 6.

4.1. Non-Overlapping Phases Generator

The non-overlapping phases generator is a well-known circuit in digital design literature [37,38]. The solution used for the demodulator, shown in Figure 8, generates the two counter-phase non-overlapped signals,V_{P1} and V_{P2}, starting the input signals, V_{AC1} and V_{AC2}. As can be seen in Figure 6, only the signal V_{P2} is used for the successive circuital blocks and, for this reason, it is the only one buffered.

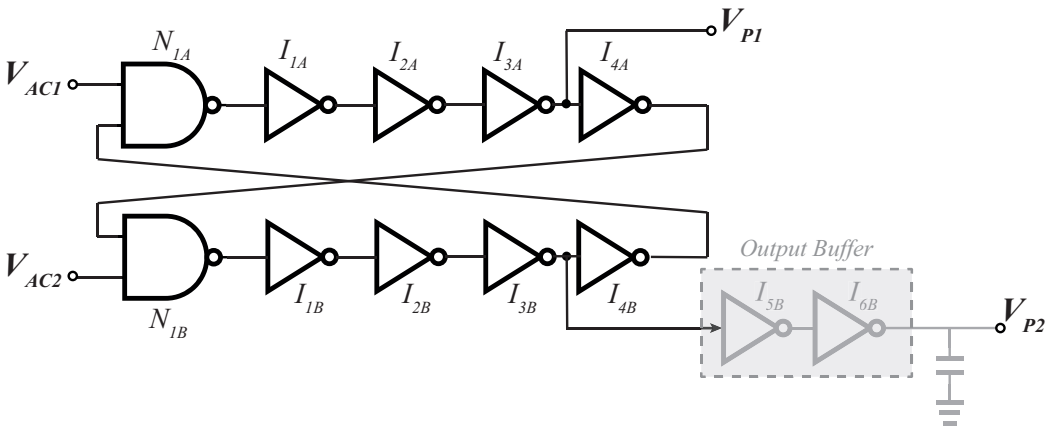

Figure 8. Non-overlapping phases generator circuit.

The amount of separation, $\Delta\varphi$, is set by the introduced delay cells in the like-latch connected NAND gates. The dimensions of the CMOS inverters are set as follows: the widths $W_n = 0.32\,\mu$m and, being $\alpha = \sqrt{\mu_n/\mu_p} \sim 3$, for symmetry reasons, $W_p = \alpha W_n = 0.96\,\mu$m. As for the NAND gates, $N_{1A,1B}$, their dimensions are found using the equivalent inverter rule. Indeed, the widths of the NMOS transistor were chosen as $W_{n,N_{1A,1B}} = 0.64\,\mu$m and for the PMOS transistor, $W_{p,N_{1A,1B}} = 1.92\,\mu$m. The lengths were chosen as $L_{n,p} = 6L_{min} = 0.9\,\mu$m in order to reduce the overall power consumption of the block. As claimed above, an output CMOS buffer was added to increase the driving capability for the modulation driving/enabling phase V_{P2}. A 25-fF capacitor, implemented by using the M1–M3 MOM option, was added to reduce output glitches. The measured phase separation was $\Delta\varphi \sim 4$ ns, whose value is made evident in the zoomed portion of Figure 9.

4.2. Current-Starved Gated Ring Oscillator (CSGRO)

The oscillator chosen for the proposed design, see Figure 6, is a current-starved ring oscillator that is turned ON/OFF by means of the signal V_{P2}. It is also known as the *Gated Ring-Oscillator*, since its structure is similar to the ones adopted for time-to-digital converters (TDCs) in Digital-PLL design [39,40]. The scheme shown in Figure 10 exploits a biasing current reference, $I_{REF} = 325$ nA, that is mirrored by the current mirror system made up of transistors M_1–M_9. Analyzing the working principle of this circuit, when the signal V_{P2} is low, the last inverter is practically disabled because no mirrored current flows through M_6 and the inverter chain of the ring oscillator results in being electrically open. Contrariwise, when the enabled signal becomes high, the M_6 transistor starts to mirror the reference current, and the oscillation begins.

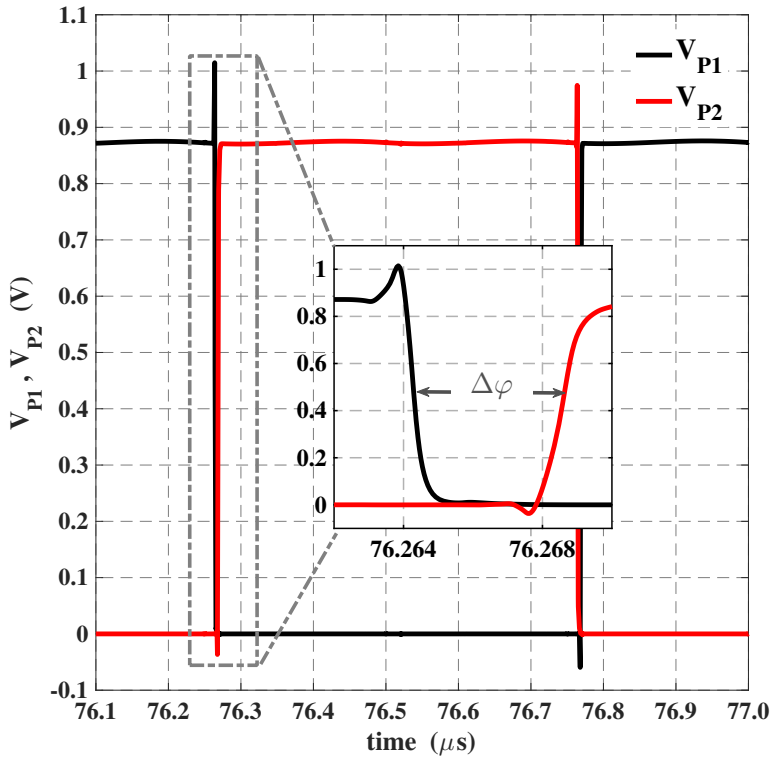

Figure 9. Transient simulation of the non-overlapping phase generator with zoom on the $\Delta\varphi \sim 4$ ns.

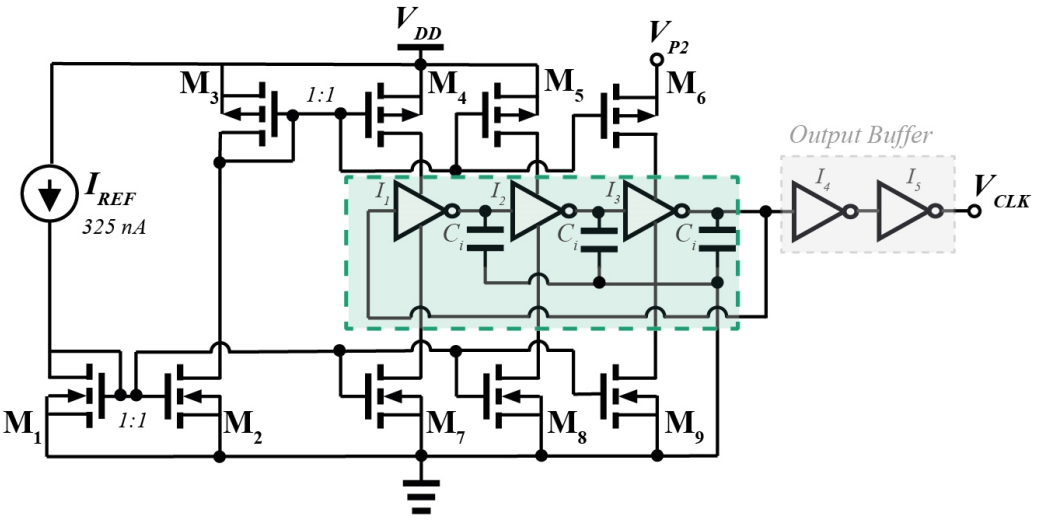

Figure 10. Schematic of the proposed current starved gated ring oscillator (CSGRO).

All the transistors involved worked in the sub-threshold region, and the oscillation frequency was fixed by exploiting the following equations [38]:

$$C_{TOT} = C_{par,int} + C_i + C_{wire} \approx C_{par,int} + C_i \simeq 30\,\text{fF} \tag{6}$$

$$f_{OSC} = \frac{I_{REF}}{NV_{DD}C_{TOT}} = \frac{325\,\text{nA}}{3 \times 0.9\,\text{V} \times 30\,\text{fF}} \simeq 4.0\,\text{MHz} \tag{7}$$

where N is the number of inverting stages, C_{TOT} is the overall capacitance associated to the output node of each inverter, $C_{par,int}$ is the parasitic intrinsic contribution due to transistors, and C_i is the load capacitance added to each output stage. The wiring parasitic contribution, C_{wire}, was neglected. Added capacitors C_i were implemented using NMOS-Cap and their dimensions are reported in Table 1. Their value was around 25 fF and chosen

to be higher than the parasitic capacitance of the inverter transistors, in order to make the latter negligible and better stabilize the oscillation frequency, $f_{OSC} = 4.0\,\text{MHz}$. In this way, the oscillator will produce just one pulse when no modulation occurs on the enabling phase, V_{P2}, with an on-time $T_{ON,osc} = 125\,\text{ns}$. Then, when the phase modulation occurs, it will generate two output pulses with the same duration described above and shown in Figure 11.

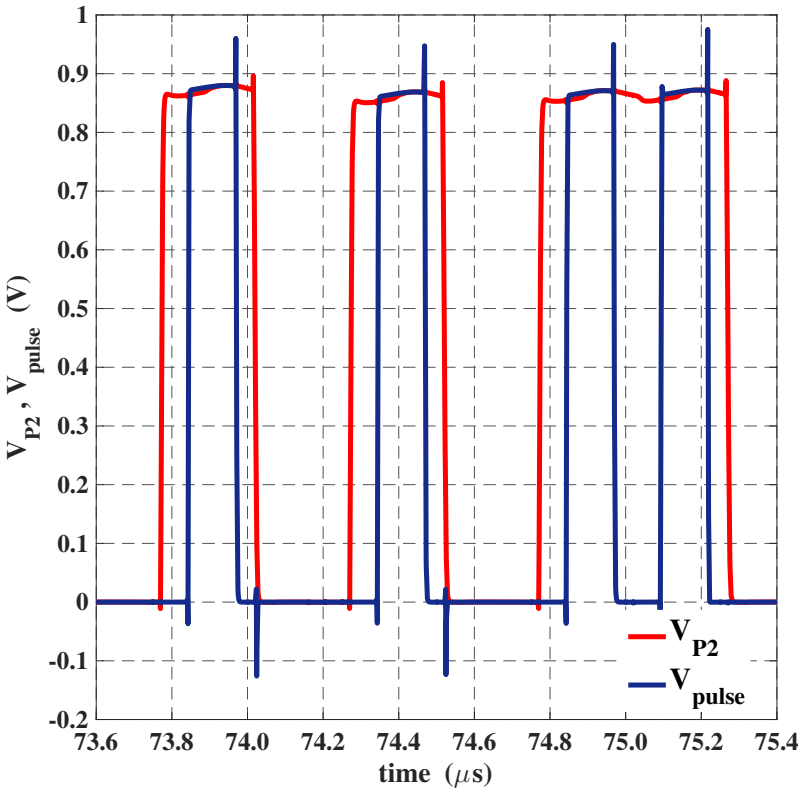

Figure 11. Transient simulation of signals V_{P2} and V_{pulse}. At time instant $t = 75\,\mu\text{s}$ the phase modulation starts.

Corner simulations were carried out at $T = 37\,^{\circ}\text{C}$, being the circuit to be implanted inside human bodies. Both the oscillation frequency, f_{OSC}, and the average power consumption, P_{DD}, of the CSGRO are reported in Table 2.

Table 1. Transistor aspect ratios of CSGRO.

Transistor	Aspect Ratio [μm/μm]
M_1–M_9	4.8/0.9
M_{N1}–M_{N3} *	0.32/0.6
M_{P1}–M_{P3} *	0.96/0.6
M_{N4} †	0.32/0.6
M_{P4} †	0.96/0.6
M_{N5} †	0.64/0.6
M_{P5} †	1.92/0.6
M_{C_i} ‡	9 × 1.0/0.4

* Dimensions of transistors inside the three-stage inverters of the core of the CSGRO in green in Figure 10; † dimensions of the output CMOS buffer in Figure 10; ‡ dimensions of the NMOS-Cap used as an output inverter stage external load indicated with C_i in Figure 10.

Table 2. Corner simulations of CSGRO at body temperature (37 °C).

Corners @ $V_{DD} = 0.9$ V, $I_{REF} = 325$ nA and $T = 37$ °C					
Parameter	**TT**	**FF**	**FS**	**SF**	**SS**
f_{OSC} (MHz)	4.07	3.72	4.16	3.95	3.93
P_{DD} (µW)	1.0	1.37	1.0	1.0	0.87

4.3. D-Flip-Flops (DFFs) and XOR Gate

The frequency dividers used in the block diagram in Figure 6 were designed using True Single-Phase Clocking (TSPC) D-flip-flops (D-FFs) [41]. The single TSPC D-FF operates with only one clock signal and offers advantages, such as small silicon area occupation for clock lines, reduced clock skew and high-speed operations. Figure 12a shows the schematic block diagram of the TSPC D-FF in the version rising-edge. It is based on three clocked inverting stages, a p-type MOSFET, M_{10} for the reset and the last CMOS inverter to provide the direct output starting from the negated one. The only disadvantage of this topology is related to the clock slope; indeed, if it is not sufficiently steep, both NMOS and PMOS transistors of the clocked inverter could simultaneously be turned on during the clock transition. As a result, the logic level of internal signals may become undefined, and a race condition may occur. However, as compared with the conventional master-slave flip-flop, TSPC D-FF has the advantages of reducing the load of the clock distribution network and the switching power dissipation. Moreover, by requiring only a single-phase clock signal, they are less affected by clock skews caused by process variations [42]. By inspection of Figure 6, the reset (RST) inverted signal is driven, for the 2-bit frequency divider, by the modulating phase signal V_{P2}, while for the RX-BPSK Data Reconstructor (consisting of a 1-bit frequency divider), the RST terminal is pulled up to the power supply.

Regarding the XOR gate, its scheme is depicted in Figure 12b). The inputs are both complementary signals outputted from the 2-bit frequency divider. For the XOR gate, the pull-up transistors (M_5–M_8) are configured based on the function $Q_O \oplus Q_1$, while the structure of the pull-down transistors is determined by the function $\overline{Q_O \oplus Q_1}$. The output is at the logic high level when only one of the inputs is set to the logic high level. When the logic level of both inputs is either high or low, that of the output is low. Aspect ratios of transistors in the TSPC D-FF and XOR gate are summarized in Table 3.

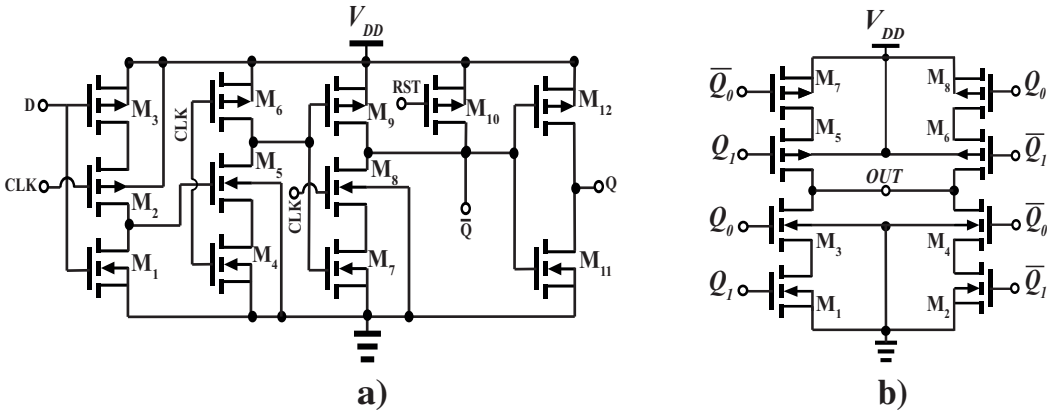

Figure 12. (**a**) Schematic of the TSPC D-FF and (**b**) schematic of the XOR Gate used for the proposed demodulator.

Table 3. Aspect ratios of TSPC D-FF and XOR transistors.

TSPC D-FF		XOR Gate	
Transistor	**Aspect Ratio [μm/μm]**	**Transistor**	**Aspect Ratio [μm/μm]**
M_1	0.32/0.9	M_1–M_4	0.64/0.6
M_4, M_5, M_7, M_8	0.64/0.9		
M_{11}	0.32/0.45		
M_2, M_3	1.92/0.9	M_5–M_8	1.92/0.6
M_6, M_9	0.96/0.9		
M_{10}, M_{12}	0.96/0.45		

5. Simulations of the Proposed Fully Digital BPSK Demodulator

Transient simulations were run using CADENCE VIRTUOSO, in order to carry out parameters and the timing diagram, as reported in Figure 13. Corner simulations were executed to demonstrate the robustness of the proposed design against process variations, concentrating them around body temperature, $T = 37$ °C. Furthermore, the human-body thermometer range (i.e., $T \in [30–50$ °C]) was chosen as the temperature investigation field in order to remark that system performances and functionalities are maintained against the temperature variations too. The performance parameters considered for the Corner simulations, as shown in Table 4, are: the oscillation frequency of the CSGRO, the time-delay between the rising edges (or falling-edges) of *MOD* and *RX-BIT* signals, the average overall power consumption, P_{DD}, and the energy-per-bit, E_b, defined as the ratio P_{DD}/Data Rate.

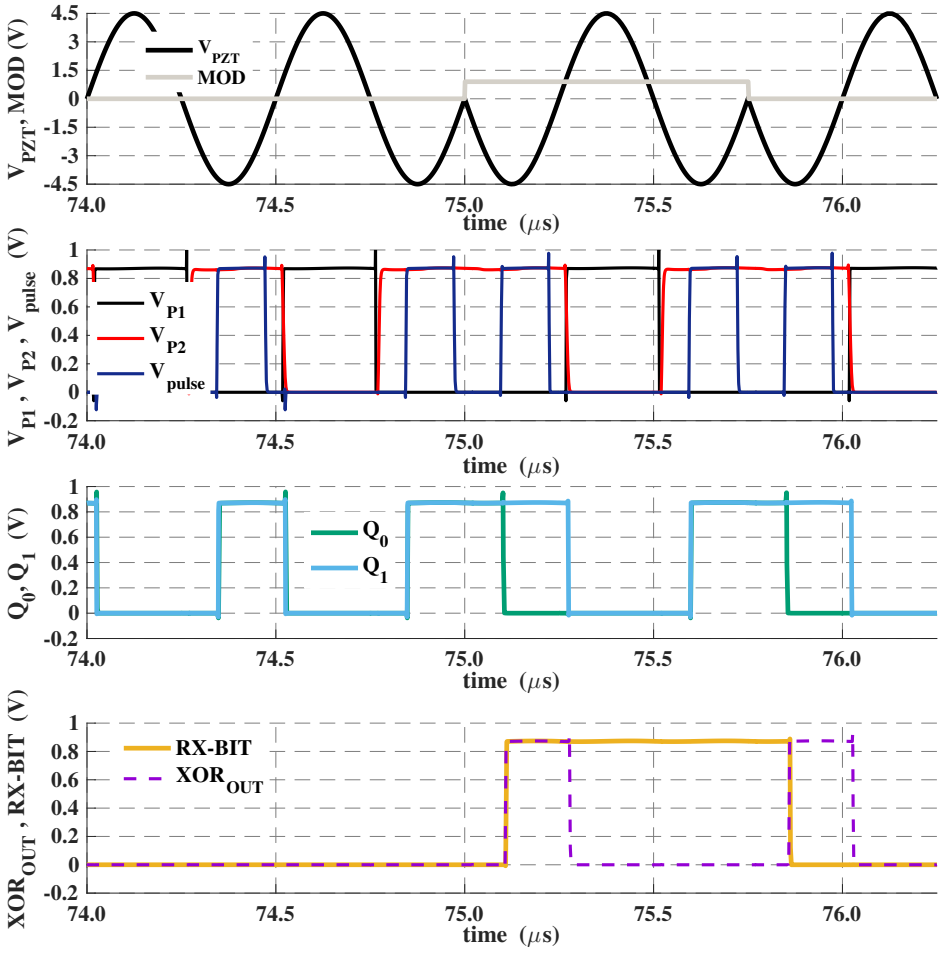

Figure 13. Timing-Diagram of the simulatedFully Digital BPSK modulator.

Table 4. Corner Simulations of the proposed BPSK demodulator @ $V_{PZT} = 4.5\,\text{V}$ and $R_{PZT} = 1.5\,\text{k}\Omega$.

Corners @ $V_{DD} = 0.9\,\text{V}$, $I_{REF} = 325\,\text{nA}$ and $T = 30\,^{\circ}\text{C}$					
Parameter	**TT**	**FF**	**FS**	**SF**	**SS**
f_{pulse} (MHz)	3.95	3.85	4.15	3.90	3.80
Δt (ns)	97	102	85	114	131
$P_{DD,TOT}$ (µW)	2.58	3.00	2.54	2.63	2.41
E_b (pJ/bit)	1.94	2.25	1.91	1.97	1.81
Corners @ $V_{DD} = 0.9\,\text{V}$, $I_{REF} = 325\,\text{nA}$ and $T = 37\,^{\circ}\text{C}$, body temperature					
Parameter	**TT**	**FF**	**FS**	**SF**	**SS**
f_{pulse} (MHz)	4.07	3.84	4.18	3.95	3.84
Δt (ns)	95	105	82	112	128
$P_{DD,TOT}$ (µW)	2.61	3.1	2.55	2.64	2.4
E_b (pJ/bit)	1.96	2.33	1.92	1.98	1.80
Corners @ $V_{DD} = 0.9\,\text{V}$, $I_{REF} = 325\,\text{nA}$ and $T = 50\,^{\circ}\text{C}$					
Parameter	**TT**	**FF**	**FS**	**SF**	**SS**
f_{pulse} (MHz)	4.1	3.72	4.2	3.95	4.1
Δt (ns)	92	108	81	109	92
$P_{DD,TOT}$ (µW)	2.64	3.3	2.64	2.67	2.43
E_b (pJ/bit)	1.98	2.48	1.98	2.01	1.83

5.1. Post-Layout Simulations and Performance Parameters

In order to investigate the effect of parasitic contributions given by a tape-out of the proposed solution, transient simulations of the post-layout view were also carried out. Several parameters, extracted form the time-domain results, were considered and are here reported as proof-of-robustness of the system. In particular, the modulating signal, V_{P2}, and the pulses generated by the CSGRO, V_{pulse}, were analyzed in pre-layout and post-layout transient simulations and are reported in Figures 14 and 15, respectively.

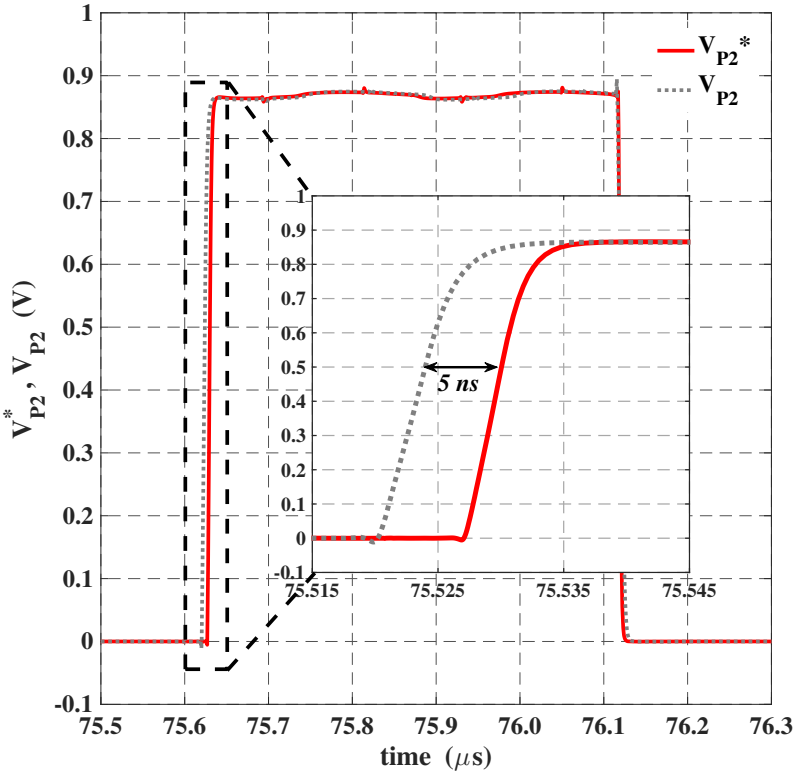

Figure 14. Pre-Layout (V_{P2}) vs. Post-Layout (V^*_{P2}) transient simulation results.

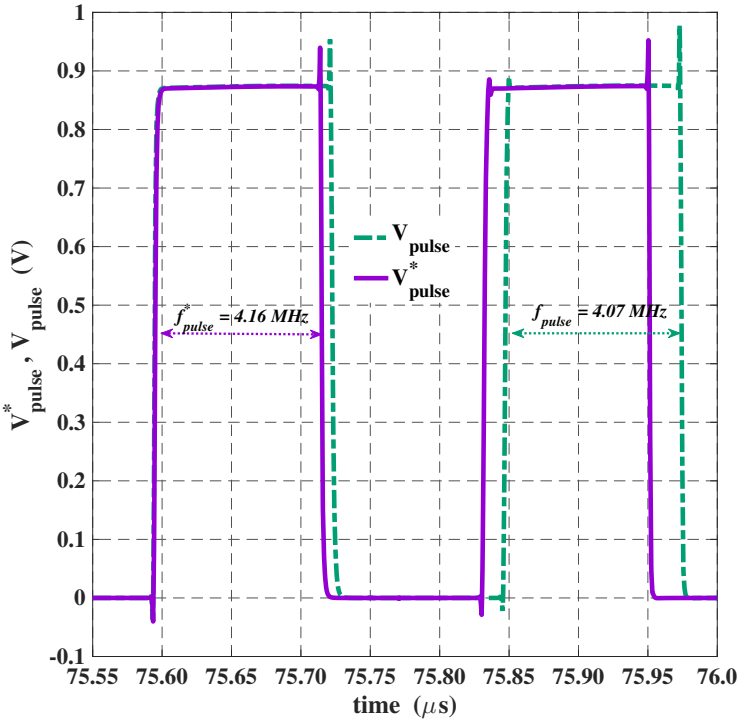

Figure 15. Pre-Layout (V_{pulse}) vs. Post-Layout (V^*_{pulse}) transient simulation results.

In Figure 14 it is possible to observe a time-delay of about 5 ns between the pre- and post-layout signals, named V_{P2} and V^*_{P2}, respectively. On the other hand, pulses presented in Figure 15 have different time durations, which suggests a spread of the oscillation frequency, f_{pulse}. Such a difference can be ascribed to an increment of the loading capacitance associated to the output nodes of the ring oscillator core. However, to compensate this spread, the current I_{REF} can be raised up to 425 nA, in order to maintain the oscillation frequency about equal to the pre-layout value, thus 4 MHz (7). After post-layout calibration, corner transient simulations were run and the achieved results are reported in Table 5. It is possible to observe good robustness against PT variations, although a slight increment was introduced both in the bias current, I_{REF}, and in the oscillation frequency, f_{OSC}, as compared to the results in Table 2.

Looking at the power consumption, it is mainly dominated by the CSGRO as understood by inspection of the power breakdown pie chart depicted in Figure 16. A remarkable total power consumption equal to $P_{DD} \approx 3.3$ µW was achieved.

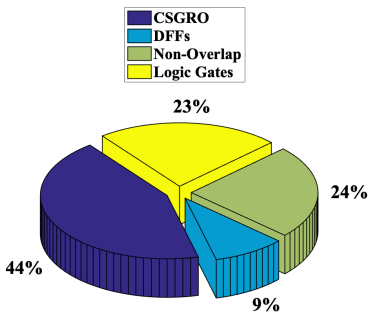

Figure 16. Power consumption breakdown associated to each sub-block.

Finally, the entire layout top-view of the proposed fully Digital BPSK demodulator is shown in Figure 17. The silicon occupied area is estimated to be 1848 µm^2. The Figure presents red dashed boxes to highlight the constitutive blocks of the circuit shown in Figure 6.

Table 5. Current Starved Gated Ring-Oscillator (CSGRO): post-layout corner simulations at body temperature.

Corners @ $V_{DD} = 0.9$ V, $I_{REF} = 425$ nA and $T = 37$ °C					
Parameter	**TT**	**FF**	**FS**	**SF**	**SS**
f_{OSC} (MHz)	4.2	4.00	4.31	4.13	3.92
P_{DD} (µW)	1.3	1.44	1.27	1.25	1.15

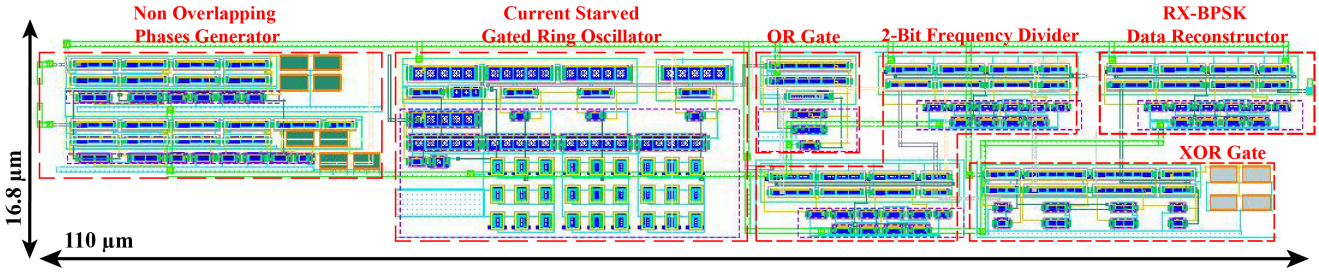

Figure 17. Top view of the proposed demodulator layout.

5.2. Comparison with the State-of-the-Art

In order to compare the proposed solution with others presented in the literature, we suggest two Figures of Merit (*FoMs*) for demodulators for Data-Link in IMDs as extracted from the review of Karimi et al. in the Ref. [32]. The most important parameters for these devices are power consumption, area occupation, maximum bit-rate and energy-per-bit, E_b, and all of them could be summarized with the following equations [32,43]:

$$FoM_1 = \frac{DR}{f_d \cdot P_{DD} \cdot A} \tag{8}$$

$$FoM_2 = \frac{DR}{f_d \cdot P_{DD} \cdot \frac{A}{(L_{min})^2}} \tag{9}$$

where DR is the data rate, f_d is the carrier frequency and A is the area occupation. The ratio DR/f_d is also defined as the *Data-to-Carrier Frequency Ratio* (*DCFR*) and is sometimes expressed in percentages. On the other side, the ratio DR/P_{DD} is the inverse of the parameter E_b. It could be noted that these *FoMs* increase if the data rate increases too and if the E_b decreases. Moreover, the demodulator power consumption P_{DD} is expressed in micro-watts, while the area in µm^2 and the L_{min} is reported in µm. As can be seen, the FoM_2 reported above includes both data, power and area parameters, also taking into account the technology used with the parameter L_{min}, while the first, FoM_1 does not include any technological parameter.

The comparison with the state-of-the-art is reported in Table 6, where we have taken other works into account that take advantages from the US-link in order to establish a data downlink. It could be observed that the proposed fully digital BPSK demodulator is the only one that exploits the BPSK demodulation scheme, and it also presents the lowest E_b parameter. This is mainly due to an overall power consumption, P_{DD}, that equals to about 3.3 µW, that makes the system very competitive with the state-of-the-art, with a data rate that is more than 25 times higher than other solutions reported in Table 6. Furthermore, as a result of the comparison with the other works that report the area occupation (or alternatively, it was possible to evaluate this parameter from the die photo of the IC), the solution presented in this work shows the lowest area occupation. Starting from these considerations, the proposed demodulator is more than 2400 times FoM_1 and about 60 times higher FoM_2 compared to the other solutions reported in Table 6.

Table 6. Comparison with the state-of-the-art.

Parameter	[23] ^{C}	[18] ^{C}	[19] ^{C}	[24] ^{C}	[20] ^{C}	[22] ^{C}	[9] ^{C}	[21] ^{C}	**This Work** ^{S}
Year	2013	2016	2016	2017	2018	2019	2020	2021	2022
Techology (nm)	350	500	180	65	180	65	65	65	**28**
Application	Deep-Tissue Stim.	Back-Telemetry	US-ID IMD	IMD Stim.	Elec./Opt. Nerve Stim.	Environment Expl.	Neural Stim.	Impl. Light Sensor	Neural Stim./Imaging
Distance Range (cm)	5.0	0.2	-	6.0–8.5	10.5	320	5.5	5.0	1.0
Modulation scheme	OOK-PM	ASK	OOK/ASK	OOK	PWM-ASK	OOK	OOK	OOK	**BPSK**
Carrier Amplitude	3.0–4.5	2.7–10	1.5	1.0	4.5 *	-	4.0	4.0–5.0	2.0–4.5 (1.8 *)
Carrier Data Frequency (MHz)	1.0	13.56	1.0	1.0	1.3	40	1.85	2.0	2.0
Data Rate (kbps)	25.0	-	50.0	25.0	11.0	1.0	-	-	**1333**
V_{DD} (V)	2.5–3.3	1.9–3.8	1.5	1.0	1.8	0.8	2.5	1.2	0.9
Demodulator Power Cons. (μW)	<400	3.3	184	-	13.75	**1.18**	-	<140	3.3
E_b (pJ/bit)	16×10^3	-	3680	-	1250	1.18×10^3	-	-	**2.5**
BER	-	-	-	$<10^{-4}$	$<10^{-5}$	$<10^{-3}$	-	$<10^{-5}$	$<10^{-5}$ ‡
Area (μm^2)	360×10^3 †	-	-	-	140×10^2 †	-	-	-	**1848**
$FoM_1 \cdot 10^6$	0.17	-	-	-	43.82	-	-	-	**109272**
$FoM_2 \cdot 10^6$	0.021	-	-	-	1.42	-	-	-	**85.67**

^{C} Measured; ^{S} Post-layout simulations; * Clamped AC input voltage; † Estimated area occupation from die photo; ‡ Estimated BER using theoretical results in Figure 2 and assuming an overall SNR equal to 10 dB; $FoM_1 = \frac{DR\,(\text{kbps})}{f_d\,(\text{MHz}) \cdot P_{DD}\,(\mu\text{W}) \cdot A\,(\mu\text{m}^2)}$; $FoM_2 = FoM_1 \cdot L_{min}^2(\mu\text{m}^2)$.

6. Conclusions

A new solution for a BPSK demodulator was presented in this paper in order to design a robust, low-area and low-power Downlink for ultrasound (US)-powered IMDs. The implemented system is fully digital and PLL-free, hence reducing area occupation and reducing power consumption. Using a 2 MHz carrier input signal and an implant depth of 1 cm, the data rate was up to 1.33 Mbit/s with a 50% duty cycle, while the minimum average power consumption was cut down to 3.3 µW in the typical corner. Post-layout simulation results were reported using a 28 nm Bulk CMOS technology provided by TSMC. A comparison with the state-of-the-art emphasizes the novelty of this work, this being the first time in which the BPSK demodulation scheme was introduced for the US-data downlink. Furthermore, it presented the lowest energy-per-bit, with the highest bit rate and the lowest area occupation compared to other works that established a data-link exploiting US-waves. The main limitations of the proposed solution were related to voltages and temperature variations; indeed, although the system was simulated with a fixed supply voltage, V_{DD} = 0.9 V, and in a fixed temperature range, it could be susceptible to both voltage and temperature variations, thus requiring successive calibrations for the current reference used in the CSGRO. In addition, the DCFR could be increased by up to the 100%, as for most of the RF solutions regarding the BPSK demodulator for IMDs.

From a medical point of view, the proposed design enables miniaturization of the implanted device through both reduced area occupation and power consumption. This latter characteristic, in particular, allows the reduction of the area of the piezoelectric device which constitutes the biggest portion of the overall area of the IMD. Moreover, a higher data rate allows for the transmission of higher data to the IMD for a given value of transmitting frequency. Therefore, for the low invasiveness, the ULP consumption and the quite high bit rate, the proposed system is largely suitable not only for the presented US-powered brain-implantable IC, but also for all the similar electronics systems that could be brought back to the concept of IoMTs.

Author Contributions: Conceptualization: A.D.G. and M.P.; data curation: M.P.; original draft preparation: M.P.; writing, review and editing: all authors; formal analysis: all authors; supervision: A.B. and A.D.G. All authors have read and agreed to the published version of the manuscript.

Funding: This research has been funded by the Brain28nm Project (Prot.20177MEZ7T)-Italian Minister of University and Research.

Institutional Review Board Statement: Not applicable.

Informed Consent Statement: Not applicable.

Conflicts of Interest: The authors declare no conflict of interest.

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