Two-Stage OTA with all Subthreshold MOSFETs and Optimum GBW to DC-Current Ratio

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***Abstract*—An approach for the design of two-stage class-AB OTAs with sub-1μA current consumption is proposed and demonstrated. The approach employs MOS transistors operating in subthreshold and allows maximum gain-bandwidth product (GBW) to be achieved for a given DC current budget, by setting optimum distribution of DC currents in the two amplifier stages. Following this strategy, a class AB OTA was designed in a standard 0.5-μm CMOS technology supplied from 1.6-V and experimentally tested. Measured GBW was 307 kHz with 980-nA DC current consumption while driving an output capacitance of 40 pF with an average slew rate of 96 V/ms.**

***Index Terms*—Low power design, subthreshold operation, two-stage amplifier, Miller compensation, CMOS.**

I. Introduction

The growing interest in wireless sensor networks, biomedical electronics and the Internet of Things [1]-[4], continuously demands for novel CMOS circuits and sub-systems with limited DC current consumption well below one microampere. Among the CMOS analog building blocks, the operational transconductance amplifier (OTA) is one of the most popular thanks to its high versatility so that it is frequently instantiated, even several times, within a single integrated circuit, for the implementation of high-accuracy closed-loop configurations. It is consequently of great importance to find suitable OTA architectures and associated design criteria enabling the optimized exploitation of the limited DC current budget, while preserving performance in terms of gain-bandwidth product (GBW) or, alternatively, settling time.

To this aim, subthreshold operation of MOS transistors has been exploited since 1977 [5] until very recently, where, for instance, inverter-based subthreshold amplifiers have been proposed [6], [7]. However, inverter-based solutions suffer from inaccurate control of the DC current that therefore depends on process and supply voltage variations. To reduce current and power consumption, alternative architectures and design techniques have also been conceived like body-driven OTAs [8]-[12], dynamic amplifiers [13] or ring amplifiers [14].

Nevertheless, OTAs based on gate-driven differential pairs remain quite indispensable thanks to their robustness and reliability, qualities that make these solutions the most acceptable by the industry standards [15]-[19]. Of course, reduction of the DC current consumption, especially under high capacitive loads while maintaining adequate slew rate values, mandates for a class AB output stage. An optimized design methodology for three-stage subthreshold OTAs was presented by the authors in [20]. In this paper, this approach is modified for a two-stage OTA, which can be employed in those cases where a lower DC gain is required and/or a reduced DC current consumption.

More specifically, a design approach using a class AB two-stage OTA with all transistors in subthreshold region exploiting Miller frequency compensation with pole-zero cancelation (MCPZC) that maximizes the gain-bandwidth product for a given total current budget is presented in this paper. The approach is discussed in Sec. II and is subsequently exploited in Sec. III to design an amplifier in a standard 0.5-μm CMOS technology. Measurement results confirm the proposed guidelines, revealing an outstanding performance in terms of small and large-signal characteristics as well as current efficiency.

II. Proposed Design Strategy

A. Preliminary Considerations

The schematic diagram of the class AB OTA utilized in this paper is depicted in Fig. 1. It is based on a folded-cascode input stage with *p*-channel source-coupled pair (M_0-M_{10}) and a common-source class-AB second stage (M_{11}-M_{12}), with M_{bat} and C_{bat} providing DC biasing and AC driving for transistor M_{12}, as a result of the so called quasi-floating gate (QFG) approach [21]-[23]. Transistors M_{b1}-M_{b6} implement a conventional bias network. For the low current application target, all transistors are biased in subthreshold regime.

Fig. 2 shows the simplified equivalent small-signal circuit of the OTA where g_{mi}, R_{oi}, and C_{oi} are the *i*-th stage transconductance, output resistance and output capacitance. Specifically, the input-stage transconductance is $g_{m1}=g_{m\mathrm{M1}}=g_{m\mathrm{M2}}$ and the output transconductance is $g_{m2}=g_{m\mathrm{M11}}+g_{m\mathrm{M12}}$. [i]

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[i] More precisely, the term g_{mM12} is attenuated by the capacitor divider generated by the QFG, as $g'_{mM12} = g_{mM12}C_{bat}/(C_{bat} + C_{GS12} + C_{GB12})$.

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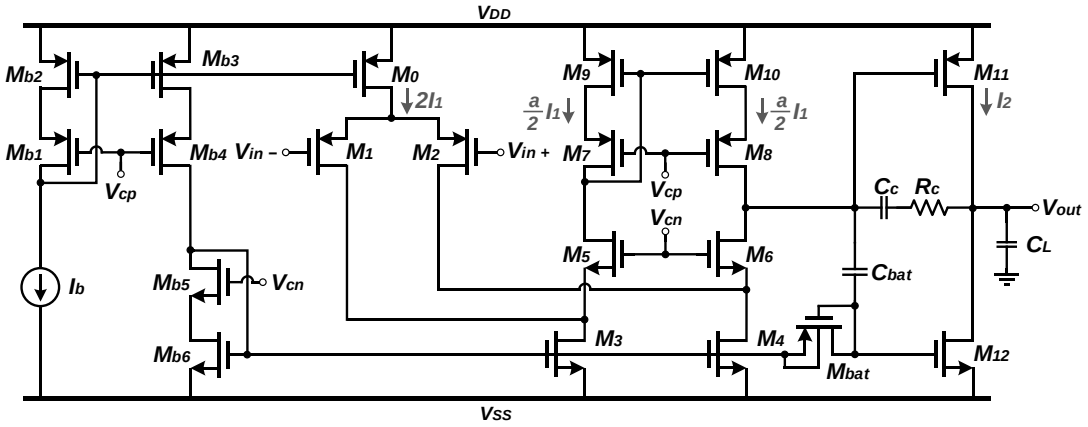

Fig. 1. Schematic of the two stage folded-cascode class-AB OTA.

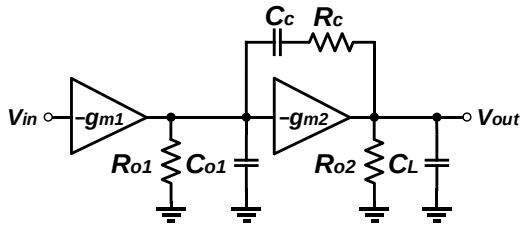

Fig. 2. Simplified small-signal equivalent circuit of the OTA.

C_L is the load capacitor that also accounts for C_{o2}. The frequency compensation branch is implemented by the Miller capacitor C_C in series with the nulling resistor R_C.

Evaluation of the transfer function V_{out}/V_{in} through conventional analysis gives the expression of the DC gain, which is

$$A_o = g_{m1}R_{o1}g_{m2}R_{o2} \tag{1}$$

Moreover, the transfer function includes three (real and negative) poles and one zero. Their expressions are summarized in (2)-(5), where ω_{p1} is the dominant pole frequency and ω_{p2} and ω_{p3} the first and second non-dominant pole frequency, respectively, being usually $C_L >> C_{o1}$.

$$\omega_{p1} \approx \frac{1}{R_{o1}g_{m2}R_{o2}C_C} \tag{2}$$

$$\omega_{p2} \approx \frac{g_{m2}}{C_L} \tag{3}$$

$$\omega_{p3} \approx \frac{1}{R_C C_{o1}} \tag{4}$$

$$\omega_z \approx \frac{1}{(R_C - 1/g_{m2})C_C} \tag{5}$$

The expression of the gain-bandwidth product is obtained by multiplying (1) and (2),

$$\omega_{GBW} = A_o\omega_{p1} \approx \frac{g_{m1}}{C_C} \tag{6}$$

which is a key parameter that approximates the unity-gain frequency under dominant pole behavior (i.e., $\omega_{p2} > \omega_{GBW}$).

The value of R_C, which modifies the zero frequency in (5), can be set by following two approaches. The first one nullifies the zero moving it towards ideally infinite frequency. This method is called Miller compensation with nulling resistor (MCNR) [24], [25]. The second one moves the zero to the left half plane in order to cancel out the non-dominant pole and is referred to as Miller compensation with pole-zero cancellation (MCPZC) [26]. This latter method is more efficient because it enhances the phase margin and settling time without additional power consumption and increase in circuit complexity. Its drawback is that it is based on an inherently inaccurate pole-zero cancellation. Note that the MCPZC leaves the third pole as the non-dominant one and can allow a lower compensation capacitance to be exploited, compared to the MCNR method.

As a result, following the conventional MCNR design strategy, the value of resistor R_C is set as given by (7a) in order to nullify the denominator of (5). Considering that the phase margin ϕ is implicitly given by $\tan\phi \approx \omega_{p2}/\omega_{GBW}$, we also find the expression of C_C reported in (7b). Similarly, equations (8a) and (8b) are found by following the MCPZC approach, as discussed in [27].

$$\text{MCNR} \quad \begin{cases} R_C = \dfrac{1}{g_{m2}} & \text{(7a)} \\ C_C = \dfrac{g_{m1}}{g_{m2}} C_L \tan\phi & \text{(7b)} \end{cases}$$

$$\text{MCPZC} \quad \begin{cases} R_C = \dfrac{C_L + C_C}{g_{m2}C_C} & \text{(8a)} \\ C_C = \dfrac{g_{m1}}{g_{m2}}\left(1 + \sqrt{1 + 4\dfrac{C_L}{C_{o1}}\dfrac{g_{m2}}{g_{m1}\tan\phi}}\right)C_{o1}\dfrac{\tan\phi}{2} & \text{(8b)} \end{cases}$$

In subthreshold the MOS transconductance is given by the ratio of the DC drain current to the thermal voltage, $g_m = I_D/nV_t$. Consequently, (7b) and (8b) can be rewritten as a function of current ratio $x = I_1/I_2$, where we remind that I_1 and I_2 are defined in Fig. 1. At this purpose, since $g_{m2} = g_{m\mathrm{M11}} + g_{m\mathrm{M12}}$ and hence $g_{m2} = 2I_2/nV_t$, we can rewrite (7b) and (8b), respectively for MCNR and MCPZC, as

$$C_{C\_MCNR} = \frac{I_1}{2I_2}C_L\tan\phi = \frac{1}{2}xC_L\tan\phi \tag{9a}$$

$$\begin{aligned} C_{C\_MCPZC} &= \frac{I_1}{2I_2}\left(1 + \sqrt{1 + 4\frac{C_L}{C_{o1}}\frac{2I_2}{I_1\tan\phi}}\right)C_{o1}\frac{\tan\phi}{2} \\ &= \frac{x}{4}\left(1 + \sqrt{1 + \frac{C_L}{C_{o1}}\frac{8}{x\tan\phi}}\right)C_{o1}\tan\phi \end{aligned} \tag{9b}$$

Regarding C_{o1}, an accurate model is required. In subthreshold, the three main transistor intrinsic parasitic capacitances (C_{GS}, C_{GD} and C_{GB}) are in the same order of magnitude. Moreover, $C_{GB} > (C_{GS} \approx C_{GD})$. This is different from strong inversion, in which the assumption $C_{GS} >> C_{GB} > C_{GD}$ is adopted.

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An approximated expression of C_{o1} is then given by (10), where the sub-caption number is related to the associated MOS transistor in Fig. 1.

$$C_{o1} \approx C_{GD6} + C_{DB6} + C_{DB8} + C_{GS11} + C_{GB11} + C_{bat}\frac{C_{GS12}+C_{GB12}}{C_{bat}+C_{GS12}+C_{GB12}} \quad (10)$$

From the above expression, it is worth noting that the floating battery loads the internal high-impedance node.

B. Optimized Design

Consider now the total DC current dissipation of the OTA, which can be also expressed in terms of I_2 and current ratio $x=I_1/I_2$

$$I_T=2I_1+aI_1+I_2=(2+a)I_1+I_2=[(2+a)x+1]I_2 \quad (11)$$

where a is the ratio of the bias current in M_7-M_{10} to I_1, as depicted in Fig. 1. Using (7b), (8b) and (11) we can evaluate the gain-bandwidth product for MCNR and MCPZC compensation approaches. For the MCNR technique we get

$$\omega_{GBW\_MCNR}=\frac{g_{m1}}{C_C}=\frac{g_{m1}}{\frac{g_{m1}}{g_{m2}}C_L\tan\phi}=\frac{2I_2}{nV_tC_L\tan\phi} =\frac{2I_T}{nV_tC_L\tan\phi}\frac{1}{(2+a)x+1} \quad (12)$$

which increases with I_2, or equivalently it tends to infinite for x=0, meaning that no optimization can be provided for a given set of I_T, C_L and ϕ. For the MCPZC technique we get

$$\omega_{GBW\_MCPZC}=\frac{g_{m2}}{\left(1+\sqrt{1+4\frac{C_L}{C_{o1}}\frac{g_{m2}}{g_{m1}\tan\phi}}\right)C_{o1}\frac{\tan\phi}{2}} =\frac{4I_T}{nV_tC_{o1}\tan\phi}\frac{1}{[(2+a)x+1]\left(1+\sqrt{1+8\frac{C_L}{C_{o1}\tan\phi}\frac{1}{x}}\right)} \quad (13)$$

It is shown in the Appendix that (13) has a maximum in x_M whose approximated expression is found in (A5), also rewritten below for convenience

$$x_M \approx \frac{1}{2+a} \quad (14)$$

Given I_T, C_L and ϕ, (14) states that the gain-bandwidth product is maximized for $I_2\approx(2+a)I_1$, yielding

$$\omega_{GBW\_MCPZC}=\frac{2I_T}{nV_tC_{o1}\tan\phi}\frac{1}{\left(1+\sqrt{1+8(2+a)\frac{C_L}{C_{o1}\tan\phi}}\right)} \quad (15)$$

In our design we will set for simplicity a=2, condition that equalizes the positive and negative internal slew rate, *SR*, (the currents charging and discharging C_C have the same magnitude equal to $2I_1$, so that $SR=2I_1/C_c$). Of course, $0<a<2$ can in principle be chosen to further reduce DC current consumption. As a result, being a=2 and considering (14), we get that $I_2=4I_1$ would be the optimal setting for a given total current budget and, we remark, for this specific OTA topology. Moreover, it is also worth noting that (6) in subthreshold becomes

$$\omega_{GBW}=\frac{I_1}{nV_tC_C}=\frac{1}{2}\cdot\frac{SR_+}{nV_t} \quad (16)$$

hence, optimization of ω_{GBW} leads also to an optimal internal *SR*, which in a class-AB OTA is the limiting parameter with respect to the external *SR* [24], [25].

Let us now analyze further the implication of this optimization method by considering that it leads from (11) to $I_1=I_T/(2a+4)$. In certain circumstances, this value of I_1 could be too small. For instance, I_1 could not meet additional specifications such as the equivalent input noise. In this case, to keep constant I_T, we should decrease I_2 from its optimum value and increase I_1, at the expense of a reduction of ω_{GBW}. Fortunately, as it can be inferred from Fig. A1 in the Appendix, selecting $I_2<4I_1$ up to $I_2=I_1$ (i.e., x=1) reduces ω_{GBW} by no more than 30%, compared to its theoretical maximum. This means that a good trade-off between the OTA gain-bandwidth product and the equivalent input noise voltage performance is achieved by setting $I_2=I_1$. Assuming a=2, from (11) this choice means that $I_1=I_T/5$ yielding to a 60% increase of I_1 from $I_T/8$, in the optimum ω_{GBW} condition. In conclusion, we will purposely set a=2 and $I_2=I_1$ in our design.

III. Experimental Results

A test chip prototype of the amplifier in Fig. 1 was fabricated using the AMI 0.5-μm n-well CMOS process, with nMOS (pMOS) threshold voltage of 0.67 V (-0.97 V). The subthreshold slope for both devices was approximately 1.5. As design constraints, the supply voltage was set to 1.6 V and the load capacitor C_L was set externally to 40 pF. The target phase margin was ϕ=60º. To achieve subthreshold operation, $2I_1$ was set to 300 nA and the same value was set as DC current of transistors M_3 and M_4 (i.e., as already stated we set a=2). The second stage DC current I_2 was set equal to I_2=150 nA. The total bias current from (11) is therefore equal to 750 nA.

The aspect ratios (in μm/μm) of transistors are 7.5/1(x8) for M_0; 15/0.6(x8) for $M_{1,2,b4}$; 7.5/1(x4) for $M_{3,4,b3}$; 2.55/1(x2) for $M_{5\text{-}8}$; 3.75/1(x4) for $M_{9,10}$; 7.5/1(x2) for $M_{11,12,b2,b6}$; 15/0.6(x4) for M_{b1}; 4.95/1(x2) for M_{b5}. Note how the aspect ratio of differential pair has been increased to improve the input signal swing as well as noise performance. For the QFG implementation, C_{bat} is 1 pF and M_{bat} is 1.5/1 according to [21]. Regarding frequency compensation, C_C and R_C are set equal to 1.4 pF and 4.1 MΩ, respectively, which can be obtained by substituting the DC conditions in equations 8a and 8b. Because of the high-valued resistor required by MCPZC, R_c was implemented by using a MOS transistor in ohmic region. Finally, C_{o1} is 50 fF. Evaluating the ratio C_L/C_{o1} we found that parameter b defined in the Appendix is greater than 3600. The maximum *GBW* is from (15) 458 kHz and a reduction of about 20 % is caused by selecting $I_2=I_1$. The die photograph of the OTA is shown in Fig. 3, whose occupied area is 0.0088 mm^2.

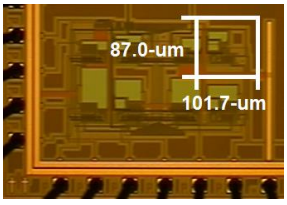

Fig. 3. Chip microphotograph.

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The simulated AC response of the OTA is reported in Fig. 4 while Fig. 5 shows the measured transient response. A reduction of the measured negative slew rate is observed as compared to the simulated value, which can be justified by introducing additional parasitic capacitors not considered in simulations. Indeed, transconductance of M_{12} is attenuated by a capacitor division of $\beta=C_{bat}/(C_{bat}+C_{QFG})$ where $C_{QFG}=C_{GS12}+C_{GB12}+C_{GD12}(1+g_{m12}r_{o12})+C_{bat,subs}+C_{Mbat}$ in which $C_{bat,subs}$ is the bottom-plate parasitic capacitance of C_{bat}, and C_{Mbat} is the parasitic capacitance of pseudo-resistor M_{bat} at the node that connects it to C_{bat}. In addition, parametric process variations could also reduce the transconductance of M_{12}, leading to a degradation in the negative slew rate.

Table I summarizes the main performance parameters. A comparison with other amplifiers operating in subthreshold is reported in Table II. Note that the total quiescent current is higher than 750 nA since it includes the current dissipated by the biasing circuit. Performance comparison is carried out considering two widely adopted figures of merit [9], [12], [18]-[20]

$$IFOM_S = \frac{\omega_{GBW}}{I_T} C_L \tag{17}$$

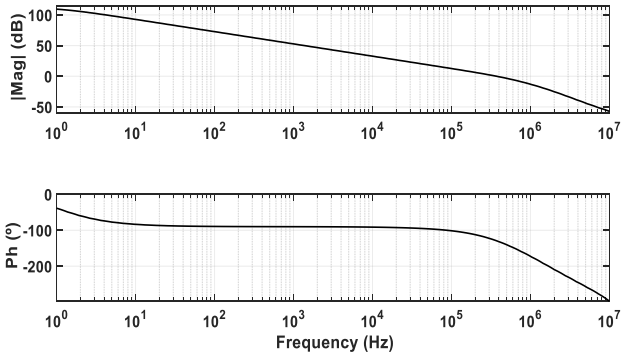

Fig. 4. Simulated AC response.

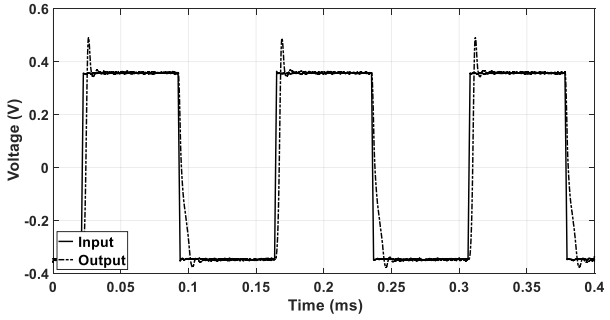

Fig. 5. Measured transient response.

TABLE I – MEASURED PERFORMANCE

Parameter	Value
Supply voltage (V)	1.6V
Total quiescent current (μA)	0.98
GBW (kHz) †	370.5
DC gain (dB) †	104.8
Phase margin (°) †	53.5
Pos./Neg. settling time 1% (μs)	10.7/12
Pos./Neg. Slew rate (V/ms)	148.8/-43.5
CMRR (dB) †	90.1
PSRR+/PSRR− (dB) †	72.3/75.0
Eq. Input Noise (nV/√Hz) †	175.8 @ 370.5 kHz
Area (mm^2)	0.0088

†Simulated

TABLE II –PERFORMANCE COMPARISON

Parameter	[11]	[12]	[16]	[17]	[18]	[19]	[20]	This work
Tech. (μm)	0.18	0.065	0.18	0.18	0.18	0.18	0.35	0.5
Area (mm^2)	0.0082	0.002	0.017	0.057	0.036	0.057	0.0044	0.0088
Sup. voltage(V)	0.3	0.25	0.5	0.8	0.5	0.5	1	1.6
C_L (pF)	20	15	20	8	40	30	200	40
DC Gain (dB)	63	70	62	51	77	70	129	105
Power (μW)	0.0168	0.026	75	1.2	0.07	0.075	0.195	1.568
GBW (kHz)	0.0028	0.0095	10000	57	4	8	20	307.5
PM (°)	61	88	60	60	56	55	52	54
SR† (V/μs)	0.0071	0.002	2	0.14	0.002	0.003	0.005	0.096
CMRR (dB)	72	63	65	65	55	--	70	90
PSRR (dB)	62	38	43	--	52	--	184	72
No. of stages	2	3	2	1	2	2	3	2
$IFOM_S$ (kHz·pF/μA)	1	1.37	1.33	0.30	1.14	3.60	20.51	12.55
$IFOM_L$ (V/μs·pF/μA)	2.54	0.29	0.27	0.75	0.57	0.60	5.13	3.92

†average value

$$IFOM_L = \frac{SR}{I_T} C_L \tag{18}$$

As compared to other OTAs, the proposed amplifier exhibits the second highest values of $IFOM_S$ and $IFOM_L$, being only the three-stage OTA in [20] the best in terms of both small and large-signal performance.

IV. CONCLUSIONS

A methodology to design subthreshold two-stage CMOS OTAs with optimized GBW to DC-current ratio is presented. The optimization process relates the first and second stage bias currents with the compensation capacitors as well as other design constraints such as load capacitance, output first stage capacitance and phase margin. Through this ratio, GBW is maximized for a given current budget, increasing both FOM_S and FOM_L. The proposal has been verified in class-AB OTA implemented with the QFG technique, improving the small and large-signal performance with no additional power increment. In order to verify the whole guidelines, a 0.5-μm test chip prototype has been simulated and fabricated, demonstrating the proposed methodology and exhibiting outstanding results.

APPENDIX

The maximum of (13) is found by minimizing the function $f(x)$ in (A1), in which we define for simplicity parameter $b=8C_L/(C_{o1}\tan\phi)$. Note that b is much greater than the unity, being $C_L>>C_{o1}$.

$$f(x) = \left[(2+a)x+1\right]\left(1+\sqrt{1+\frac{b}{x}}\right) \tag{A1}$$

The derivative of (A1) with respect to x is

$$f'(x) = \frac{2(2+a)x^2\sqrt{1+\frac{b}{x}}\left(1+\sqrt{1+\frac{b}{x}}\right) - b\left[1+(2+a)x\right]}{2x^2\sqrt{1+\frac{b}{x}}} \tag{A2}$$

Setting the derivative to zero and being $x>0$, we get

$$2(2+a)x^2\left(\sqrt{1+\frac{b}{x}}+1+\frac{b}{x}\right)-(2+a)bx-b=0 \qquad \text{(A3)}$$

where we can neglect the squared term in the round brackets, being its argument much greater than the unity. Moreover, considering that $b/x>>1$, we get

$$(2+a)bx-b\approx 0 \qquad \text{(A4)}$$

Therefore, the maximum of (13), i.e. the minimum of (A1), occurs for

$$x_M \approx \frac{1}{2+a} \qquad \text{(A5)}$$

As a further illustrative proof of this result, we plot $1/f(x)$ versus x in three selected example cases, namely, for a=2 with b equal to 2000 and 4000, and for a=1 with b=4000. In particular, we see that the three diagrams are relatively flat near their maximum, which occurs at x_M=1/4 for a=2 in curves a and b, and at x_M=1/3 for a=1 in curve c, as anticipated by (A5).

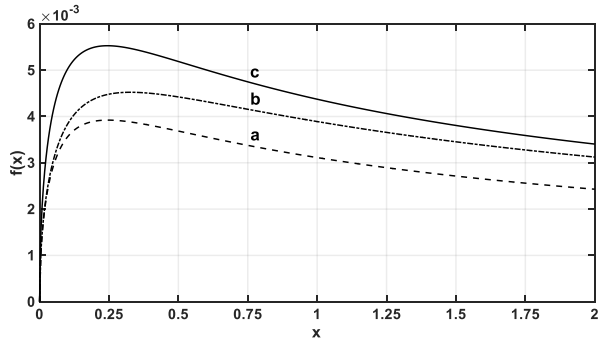

Fig. A1. Plot of $1/f(x)$ versus x for: a) a=1, b=4000, b) a=2, b=4000, and c) a=2, b=2000.

The almost flat behavior of the curves around the maximum indicates that $x>x_M$ can be chosen without strongly reducing the gain-bandwidth product. For example, selecting $I_2=I_1$ (i.e., x=1) causes a ω_{GBW} reduction of around 20% in the cases of curves a and b, and of around 30% in the case of curve c.

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