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Design of voltage-controlled oscillators for mm-wave application in 28-nm FD-SOI CMOS technology

Ph.D. Thesis

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Abstract

This thesis summarizes the main activities that I have been carried out during the three years of Ph.D. studies at the *Radio Frequency Advanced Design Center* (RF-ADC), a joint research center between University of Catania and STMicroelectronics, Catania.

Aimed at supporting driving and significantly improving the on-road safety, advanced driver assistance systems (ADASs) have quickly become a very popular feature in most modern vehicles. Nowadays, modern ADASs provide vehicles with a growing automation in the driving functions and represent the key underlying technology in emerging autonomous vehicle. To accomplish its operation, such systems rely on the information provided by many on-board sensors, which detect the state of the vehicle as well as the surrounding environment and other road actors. Since comprehensive and accurate information about the vehicle surrounding cannot be provided by any single sensor, several kinds of sensors must be equipped in vehicles to address the driving tasks. Among them, mm-wave radar sensors provide a key enabling technology for the deployment of effective and reliable driving systems, as they are able to detect and localize obstacles with a high range of coverage over every weather or lighting condition. To cover the several functionalities of a driver assistance system, long-range and short-range radar sensors, operating in 76-77 GHz and 77-81 GHz frequency bands, respectively, are properly distributed around the car to recognize a target ranging from few centimeters to about 250 m.

Modern automotive radar sensors rely on frequency-modulated continuous wave (FMCW) principle to reduce both complexity and power consumption, while benefit from the multimode radar approach to further constraining the whole system cost. Indeed, they can support both long- and short-range radar operation modes, thus avoiding the

need for different radar devices. However, this poses significative challenges on mm-wave transceivers (TRXs) especially for the frequency synthesizer, which must be able to guarantee both wide frequency tuning range and high spectral purity to enable high-resolution sensing for short-range operation and accurate detection of low reflected signals for long-range operation, respectively. In a voltage-controlled oscillator (VCO)-based frequency synthesizer, these requirements are largely determined by the VCO itself. The design of VCOs that are capable of simultaneously achieving low phase noise and wide tuning range is a very challenging task, especially at mm-wave frequencies. Moreover, the transition toward CMOS technologies, to pursue for cost reduction and system-on-chip (SoC) solutions, poses additional challenges in the VCO, which asks for an advanced circuit design.

This thesis deals with the design of mm-wave VCOs for *W*-band automotive FMCW radar applications, which is able of providing a proper frequency tuning range without impairing the phase noise. To this end, basic concepts about automotive radar sensors based on the FMCW operating principle, along with the related design challenges for the mm-wave TRX, are introduced in chapter 1 with special emphasis on frequency synthesizers. In addition, an overview on the adopted 28-nm FD-SOI CMOS technology by STMicroelectronics is also provided at the end of the chapter.

Following the introduction, Chapter 2 deals with the design of integrated inductors and transformers for mm-wave applications. Indeed, passive components with good quality factor are a key design requirements for many performance parameters in both RX and TX as well as for the oscillator performance. To this end, fundamental features of both integrated inductors and transformers in CMOS technology have been discussed and a comparative analysis on different structures of integrated transformers for mm-wave frequencies have been carried out. This preliminary activity has been exploited to meet the stringent requirements of *W*-band automotive radar applications. Finally, since the parameters of the transformer are closely related to that of the adopted technology, a comparative analysis of two 28-nm CMOS technology based on standard and mm-wave-optimized (i.e., thick metals and intermetal oxides) back-end-of-line (BEOL) is also provided.

Chapter 3 gives the fundamental concepts concerning the design of mm-wave VCOs. The most meaningful phase noise models are introduced to provide the theoretical

background of the most common LC-oscillator topologies. Starting from the limitations of the very popular class-B topology, an overview of the most interesting approaches that try to overcome them is provided, highlighting benefits and drawbacks of each solution. Moreover, main approaches for the phase noise optimization are also discussed along with sub-harmonic PLL solutions for performing the final operating frequency. Based on the consideration carried out in this chapter, a first implementation of a 38-GHz VCO has been carried out with the main aim of consolidating the design flow for mm-wave transformer-based oscillators in 28-nm FD-SOI CMOS technology.

Presently, mm-wave frequency synthesizers are highly demanded in a wide range of applications, including automotive radar sensors. Whatever the addressed application, mm-wave frequency synthesizer must provide proper tuning range (TR) to cover the desired operating band. Moreover, fast settling time must be achieved to meet high speed requirements of modern communication systems. In a VCO-based frequency synthesizer, the required tuning capability is achieved by the VCO itself, which must be able to provide a frequency tuning range larger than the desired operating frequency band to compensate for process, voltage and temperature (PVT) variations. By referring to the main limitations of the state-of-the-art solutions, two novel approaches are introduced in chapter 4, which are aimed at improving the oscillator tuning range without impairing the phase noise performance. A first approach relies on a varactor-based technique to implement a dual-band VCO, which allows both long range (i.e., from 76 GHz to 77 GHz) and short range (from 77 GHz to 81 GHz) radar operation to be achieved, thus avoiding the need for different radar devices. A second approach is based on a flash frequency tuning technique for SC-based VCOs, which overcomes the tuning delay limitations of state-of-the-art solutions, thus achieving high speed frequency locking, useful in a wide range of modern frequency synthesizers. Both techniques reduce the varactor size allowing the desired tuning range in two or more sub bands to be achieved. Unfortunately, the tuning curves in the sub bands move up or down due to PVT variations, which limit the varactor size. To address this issue, a novel calibration strategy has been proposed, which compensates for PVT variations during the PLL start-up, thus resulting in a more relaxed VCO tuning range requirement.

The proposed VCOs have been embedded in a sub-harmonic PLL where a novel push-push frequency doubler has been implemented to address the high sensitivity of this

circuit to the impedance supply paths, which is a critical issue at mm-wave frequencies. Unfortunately, only simulations are provided on the dual-band VCO that uses the varactor-based technique, being the related chip under manufacturing. Conversely, experimental results and comparison with recent state-of-the-art of mm-wave CMOS VCOs is provided for the proposed SC-based VCO based on a flash frequency tuning technique. Finally, all the proposed architectures have been patented, thus showing the industrial interest towards this Ph.D. research activity.

Besides the main topic, during my Ph.D. studies I was involved in the design of a passive-mixer and a power amplifier (PA) for *W*-band automotive radar applications, which were designed exploiting the same 28-nm CMOS technology used for VCOs. Specifically, I have accurately analyzed mm-wave passive structures, such as inductors, transformers, and interconnections, for the matching networks of both the mixer and PA, and properly accounted for layout parasitic effects through extensive electromagnetic simulations.

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List of Abbreviations

ADAS	Advanced Driver Assistance Systems
ACC	Adaptive cruise control
A-MOS	Accumulation-MOS
AC	Alternating current
ADCs	Analog-to-digital converters
AM	Amplitude modulation
AM-to-PM	Amplitude modulation to phase modulation
B	Magnetic field
BEOL	Back-end-of-line
BER	Bit error rate
BiCMOS	Bipolar complementary metal-oxide semiconductor
BOX	Buried Oxide
CM	Common mode
CMOS	Complementary metal-oxide semiconductor
CP	Charge pump
DACs	Digital-to-analog converters
DC	Direct current
DDFS	Direct digital frequency synthesizer
DK	Design Kit
DM	Differential-mode
DSP	Digital signal processor
E	Electric field
ECUs	Electric control units
EIRP	Equivalent isotropic radiated power
EM	Electromagnetic
ESD	Electrostatic discharge
ETSI	European Telecommunications Standard Institute
F	Noise excess factor
FAR	False alarm ration

FCC	Federal Communications Commission
FD-SOI	Fully depleted silicon on insulator
FFT	Fast Fourier transform
FM	Frequency modulation
FMCW	Frequency modulated continuous wave
FoM	Figure of merit
FPGA	Field programmable gate array
GaAs	Gallium-arsenide
GSG	Ground-signal-graund
HBT	hetero-junction bipolar transistor
ICs	Integrated circuits
IF	Intermediate frequency
IL	Insertion Loss
ILFM	Injection-locked frequency multiplier
InP	Indium-phosphide
ISF	Impulse sensitive function
km	Magnetic coupling
LIDAR	Light detection and ranging
LO	Local Oscillator
LPF	Low pass filter
LRR	Long-range radar
LTI	Linear time-invariant
LTV	Linear time-variant
MMICs	Mm-wave integrated circuits
MOM	Metal-oxide-metal
NF	Noise figure
NLTV	Nonlinear time-variant
PA	Power Amplifier
PAPR	Peak-to-average power ratio
PCB	Printed circuit board
PFD	Phase frequency detector
PGS	Pattern ground shield
PLL	Phase-Locked-Loop
PN	Phase noise
PSD	Pulse stream detector
PVT	Process, voltage and temperature
Q	Quality factor
RADAR	Radio detection and ranging
RCS	Radar-cross section
RF	Radio frequency
RL	Return loss

rms	Root-mean-square
ROM	Read-only memory
RX	Receiver
SC	Switched capacitor
SFDR	Spurious-free dynamic range
SiGe	Silicon-germanium
SNR	Signal-to-noise ratio
SoC	System-on-chip
SR	Shift Register
SRF	Self-resonant frequency
SRR	Short-range radar
SSCR	Single-sideband-to-carrier ratio
TC	Timing Counter
TCR	Transformer characteristic resistance
TDCs	Time-to-digital converters
ToF	Time-of-flight
TR	Tuning range
TRXs	Transceivers
TVCs	Time to voltage converters
TX	Transmitter
UTBB	Ultra-Thin Body and Buried Oxide
UWB	Ultra-wide band
VCO	Voltage-controlled oscillator
WLAN	Wireless local area network

Chapter 1

Automotive radar sensors in CMOS technology

1.1. Introduction

The automotive world market has experienced a deep evolution over the last decades, which has tuned the vehicle concept itself from a simple mode of transport into a sophisticated computing and sensing hub aimed at accomplishing a more safety, security, and comfortable drive experience. In truth, safety and security for drivers, passengers, and any other road users have always been a matter of primary importance since from the early days of on-road vehicles. To this purpose, the automotive industry has been continuously looking for new technologies, devices, and systems capable of reducing road accidents and the associated casualties by alerting drivers from potentially hazardous conditions and/or taking corrective actions on the vehicle control. Over the years, this resulted in a widespread adoption of many passive and active devices into the vehicles, thus implementing systems aimed at supporting drivers in different driving phases. Such systems, commonly referred to as Advanced Driver Assistance Systems (ADASs), have quickly become a very popular feature in most vehicles, providing automotive manufacturers with a way to differentiate their offerings while promoting consumer safety. The ongoing automation of driving functions in cars has led the evolution of ADASs into systems capable of highly automated driving, which, in turn, are targeted to accomplish fully autonomous driving systems [1]. Therefore, modern-day ADASs are the key underlying technology in emerging autonomous vehicle. Currently, autonomous driving is one of the megatrends in the automotive industry, and most car manufacturers are already introducing various levels of autonomy into commercially

available vehicles [2]. Since the autonomous driving aims at replacing human driver in both sensing and decision making, a large number of electric control units (ECUs) and sensors, which provide reliable and dense information on the vehicular surroundings, are required. Specifically, it is necessary to acquire information about drivable areas on the road and to report all objects above the road level as obstacles to be avoided [2]. Therefore, the on-vehicle sensors need to detect, localize, and classify a large variety of objects, such as vehicles, pedestrians, poles, guardrails, etc., in many different driving scenarios. Since comprehensive and accurate information about the vehicle surrounding cannot be provided by any single practical sensor, several kinds of sensors must be equipped in vehicles to address the autonomous driving tasks. Automotive millimeter-wave (mm-wave) radar, along with other sensors such as light detection and ranging (LIDAR), camera and ultrasound, properly distributed around the car in a sensor network, represents the backbone of ADASs as well as emerging autonomous driving. Exploiting such sensor network, information about vehicle surrounding scenario can be constantly collected and combined each other, thus enabling a microcontroller to monitor and hence control the vehicle motion by means of several functionalities such as: automatic emergency braking systems, adaptive cruise control, blind spot detection, intelligent park assist, forward collision warning, etc [3]. Some of these ADAS functionalities are shown in Figure 1.1 along with the adopted sensors.

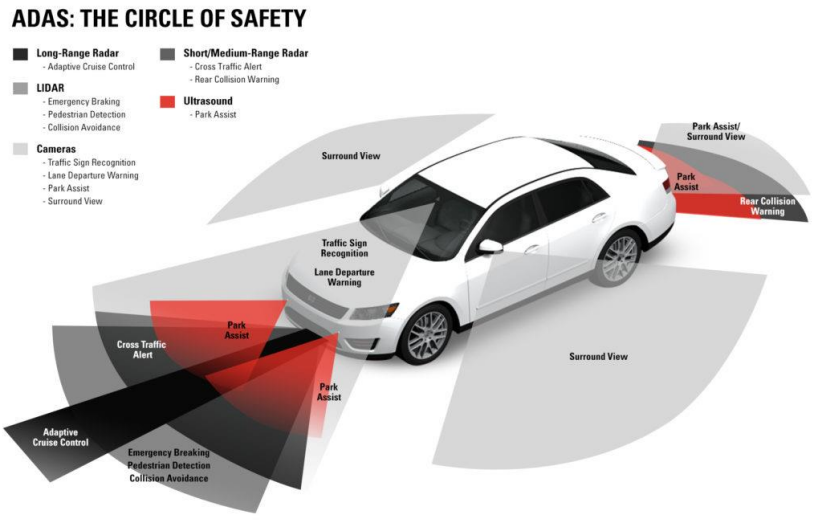


Figure 1.1. Typical ADASs functionalities and related sensor technologies.

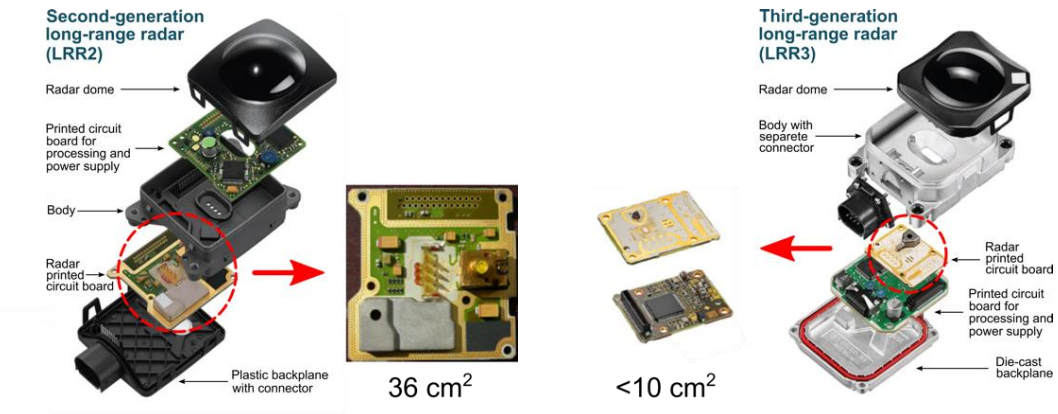
The deployment of effective and reliable driving systems calls for sensors with long detection range able to detect and classify obstacles over every weather or lighting

condition. To this end, radar represents one of the key sensing technologies, since it is capable of providing environmental perception over any weather conditions. Indeed, compared to other sensor technologies, the mm-wave radar sensor guarantees high robustness over environment interference (i.e., poor light, extreme temperature, bad weather conditions, etc.) and hence it properly operates wherein the other sensors could fail. In addition, the radar sensor can perform accurate and direct measurements of range, relative velocity and, with a suitable antenna system, also the angle of multiple targets with a high range of coverage. To accomplish the several functionalities of a driver assistance system, multiple radar sensors are commonly used to recognize an obstacle from few centimeters to about 250 m. This leads to various sensor requirements, which are met from different radar sensors usually classified as long-rang radar (LRR) and short-range radar (SRR). The operating frequencies and standard of such sensors are regulated in Europe by the European Telecommunications Standard Institute (ETSI), which allocated two frequency bands for LRR (i.e., from 76 to 77 GHz) and SRR (i.e., from 77 to 81 GHz). However, while the 76-77 GHz band was established worldwide for automotive radar applications since many years, the 77-81 GHz band is much newer. Indeed, the 24-GHz UWB band (from 21.625 to 26.625 GHz) was temporarily authorized in Europe to enable fast market introduction of early SRR applications. Compared with the 24-GHz band, the 79-GHz band allows the development of more compact SRR sensors, due to a shorter wavelength and the benefit of a wide frequency band up to 4 GHz.

The history of automotive radar sensors starts with the first investigations came up in the early 1970s by Bendix, Info Systems Inc., RCA, and General Motors, which was partly supported by the U.S. Department of transportation [4]-[6], followed by the Japanese companies Mitsubishi and Nissan [7], [8]. At the same time, in Germany, the companies SEL, VDO, and AEG Telefunken started a related work supported by the German Ministry of Science and Technology [9], [10]. Although, the resulting prototypes allowed distance measurement and collision warning, the available technology was not yet mature enough to bring these products to market.

In the following years, advances in semiconductor technologies as well as signal processing circuits have provided a decisive impulse to development of automotive radar sensors. The development of first MMICs in III-V based technologies, such as

gallium-arsenide (GaAs) and indium-phosphide (InP), led to the introduction of the first generation of automotive radar sensors. In particular, the first commercialized product were provided by VORAD in 1995 for 24-GHz band [11] and by Mercedes Benz in 1999 for the 76-GHz band with the introduction of the so-called *Distronic* system [12]. In the coming years, several other products were developed by an increasing number of established companies like Aptiv, Bosh, Denso, Delphi, Mando or Veoneer in partnership with other car manufacturers such as Jaguar, Nissan, Audi, and BMW [13]. As early as 2003, radar systems were offered by most major car manufacturers as optional equipment in their vehicles. However, first radar-based driver assistance systems were equipped only in high-end car models due to the high cost motivated by the low integration level of the adopted III-V based technologies [14]. The availability of silicon-based technologies with f_T / f_{max} values close to or even higher than 200 GHz, has made possible to replace the traditional and expansive solutions with implementations in silicon-germanium (SiGe) hetero-junction bipolar transistor (HBT) technologies. The development of SiGe MMICs with several radar channels in a single chip was a very important step in the automotive radar evolution leading to the first commercial product in silicon technology by Bosh in 2009 [15]. Figure 1.2 shows two products, one in SiGe and the other in GaAs technology.



(a) (b)

Figure 1.2. Examples of commercial radar sensors in (a) GaAs and (b) SiGe technologies by Bosch.

Besides the reduction in power consumption, size, and cost, the higher integration density has allowed to add more features to the radar sensors. Few years later, the first radar circuits in SiGe HBT BiCMOS technologies were implemented by ST Microelectronics for 24-GHz [16] and 77-GHz sensors [17] and by Freescale for

77-GHz LRRs [18]. The high performance of SiGe HBT devices combined with CMOS transistors, suitable for low-frequency circuits, has permitted a further increasing in the integration level. For the first time, a complete radar sensor including mm-wave radio front-end, analog baseband including analog-to-digital converters (ADCs), and digital interface was implemented in a single chip, thus projecting mm-wave radar sensors toward the large-scale production. Consequently, radar-based driver assistance systems have become available even for middle-class cars. The rapid development of new radar sensor generations has enabled a greater penetration of ADASs in the automotive market with an always growing number of features.

However, to make such systems a standard equipment even in low-end vehicles a further manufacturing cost reduction is required, thus making inevitable the transition toward very scaled CMOS technologies. On the other hand, nanometer CMOS technologies are now able to provide a f_T comparable to modern SiGe-BiCMOS technologies, exceeding 300 GHz in 40-nm and 28-nm nodes. They are now fast enough to support mm-wave applications with the advantage of a higher transistor density for analog/digital section and a lower cost for mass-market production. By taking advantage of the higher integration level, microcontroller cores, memory, or machine learning engines can potentially also be integrated, enabling standalone operation with minimal additional out-side components. These features make advanced CMOS the best candidate for the system-on-chip (SoC) implementation of high-performance low-cost radar sensors for next-generation automotive applications [19]-[21].

The feasibility of mm-wave radar sensors in sub-μm CMOS technologies has been demonstrated in a variety of papers over the last years, as discussed in [20]-[23] and an already available commercial example of SoC implementation in 45-nm CMOS technology is also described in [24]. Most of these solutions benefit from the frequency-modulated continuous wave (FMCW) architecture to reduce both complexity and power consumption, while exploiting a multimode radar approach to further constrain the whole system cost. Indeed, they can support both long- and short-range radar operation modes, thus avoiding the need for different radar devices. However, multimode radars pose significative challenges on mm-wave transceivers (TRXs) especially in frequency synthesizers. Since they provide the signal for frequency up/down-conversion, wide frequency tuning range along with high spectral purity must

be guaranteed at the same time to enable high-resolution sensing for short-range operation and accurate detection of low-level reflected signals for long-range operation, respectively.

Actually, developing a CMOS multimode radar solution requires very advanced circuit design and numerous shortcomings have to be solved mostly in the mm-wave radar transceivers (TRXs). Along with the scaling of CMOS technology nodes, the supply voltage is reduced accordingly (around 1 V or even less beyond the 28-nm node) leading to a lower dynamic range in analog circuits. As a consequence, severe limitations arise for both the transmitter (TX) and receiver (RX) chain in terms of transmitted output power and 1-dB compression point, respectively. Frequency synthesizers are also affected from CMOS technology nodes scaling. In a voltage-controlled oscillator (VCO)-based frequency synthesizer, frequency tuning range and spectral purity requirements are largely set by the VCO itself. Here, a reduced supply voltage leads to a lower VCO control voltage as well as a limited oscillator signal swing, thus constraining the oscillator performance especially in terms of both frequency tuning range and phase noise. The ability to provide a low phase noise in a proper frequency tuning range is mandatory to preserve the TRX performance. Indeed, the oscillator phase noise could cause reciprocal mixing in the receive path thus degrading the receiver sensitivity, while the oscillator phase noise in the transmit path, can desensitize a nearby receiver.

In addition, flicker noise is worsened with the scaling of CMOS technology. High-*k* materials, commonly used to reduce the leakage current in nanometer CMOS process, increases the trap density [25]. Halo doping that is used to mitigate the short-channel effects, leads to a nonuniform threshold across the channel [26]. These effects become prominent in advanced CMOS technologies and degrade the flicker noise performance.

The availability of good quality integrated passive components, such as inductors, transformers, and capacitors, is another crucial point in radar TRX design. The use of passive components with a low-quality factor in the mm-wave front-end leads to increased losses in both TX and RX paths as well as in VCOs. As the frequency goes up, skin and proximity effects became always even more significant, thus causing an increase in ohmic losses. The substrate losses also become important at mm-wave frequencies, especially in nanometer CMOS due to a very dense back-end-of-line (BEOL). The lower quality factor for on-chip passive components combined with the higher flicker noise

transistor make the CMOS oscillator PN poor, thus degrading the signal to noise ratio (SNR) of the demodulated signal.

In this chapter the fundamental concepts of automotive FMCW radar in CMOS technology are discussed, with special emphasis in frequency synthesizers. The automotive radar frequency regulation and the FMCW radar operating principle are widely reviewed in Section 1.2 and Section 1.3, respectively, followed by an analysis of the main FMCW radar requirements, reported in Section 1.4. Then, frequency synthesizers for automotive radar applications are briefly investigated in Section 1.5, along with the main related design challenges. Finally, in Section 1.6, an overview on the adopted 28-nm FD-SOI CMOS technology platform is provided.

1.2. Frequency regulation

Several radar sensors with different requirements are involved in a typical ADAS applications, which are commonly classified in two groups, according to the required operating distance, as mentioned before. The 77-GHz band (from 76 to77 GHz) has been available for vehicular long-range radar applications for many years. This band has the benefit of high allowed equivalent isotropic radiated power (EIRP) that enables functions like adaptive cruise control (ACC) where high precision is not mandatory. On the other hand, short-range radar applications, such as blind spot detection or parking aid, require a high range resolution which call for a wide bandwidth requirement. A consortium of automotive manufacturers and suppliers, known as *Short-Range Automotive Radar Frequency Allocation* consortium, worked on the worldwide frequency allocation for SRR UWB automotive radar. In the USA, the approval of a band ranging from 22 to 29 GHz was already granted in 2002 by Federal Communications Commission (FCC). The European Union, in contrast, has been more prominent on the regulation of mm-wave radar. Since a relevant part of the spectrum around 24 GHz was already reserved for radio astronomy applications, the 77-81 GHz band was allocated for wideband automotive radar. Nevertheless, as the development of SRR sensors for those frequencies was not yet sufficiently advanced, the 24-GHz UWB frequency band was temporarily authorized, working toward an early introduction of equipment operating in the 79-GHz band (from

77 to 81 GHz) by means research and development program. In Figure 1.3, the adopted frequency band for both SRR and LRR are schematically illustrated.

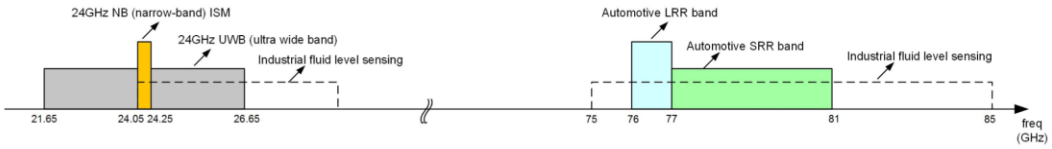


Figure 1.3. SRR and LRR frequency bands.

Currently, automotive radar sensors operate mainly in the 79-GHz band and will continue to do so in the future to completely replace the 24-GHz band. The availability of wide bandwidth significantly improves range resolution and accuracy in 79-GHz band. The higher range resolution results in a better separation of targets, thus improving environmental object classification. Besides to smaller form factor for the radar sensor, a higher operating frequency also allows better velocity resolution to be achieved. These advantages are essential to enable many important features especially for emerging fully autonomous vehicles.

1.3. FMCW radar operating principle

The history of radio detection and ranging, more commonly known as *radar*, starts with the experiments carried out by Hertz and Hülsmeyer on the reflections of electromagnetic (EM) waves and ideas advocated by Tesla and Marconi in the late 19th and early 20th centuries [27]. Although earlier developments in radar technology were limited to military purpose, many civilian applications gradually emerged over the last four decades, including automotive one. Today, radars are used in many applications with the aim of detecting the presence of one or more targets of interest and estimating their range, angle, and relative motions. Whatever the application, a radar system operates by radiating electromagnetic waves and detecting the reflected signal from the target, commonly referred to as *echo*. Specifically, a signal with a particular frequency shape is radiated by a transmitter. Any obstacle or target invested by the radiated signal reflects a portion of the incident power, producing an *echo*, which will be detected by the receiver, after down-conversion, amplification and processing. Target proprieties are estimated

from the resulting down-converted signal exploiting the propagation delay τ between the transmitted and received signals due to the wave roundtrip time-of-flight (ToF) and the Doppler frequency shift.

Although a lot of architectures can be exploited for the radar system implementation, only few of them are relevant in the automotive context, which are mainly the *pulsed radar* and the *frequency-modulated continuous-wave (FMCW) radar*. The pulsed radar operating principle is based on the transmission of signals compressed into relative short rectangular pulses characterized by a high peak-to-average power ratio (PAPR) [28]. However, this is critical to accomplish with CMOS technologies because, differently from SiGe BiCMOS ones, a low supply voltage is available, thus limiting the achievable output power. On the other hand, FMCW radar continuously transmit a modulated signal to extract information from the target, thusresulting in a lower PAPR than the pulsed counterpart. This adavntage combined along with a simpler modulation scheme makes the FMCW radar the best choice for CMOS mm-wave integrated radar sensors [28], [29].

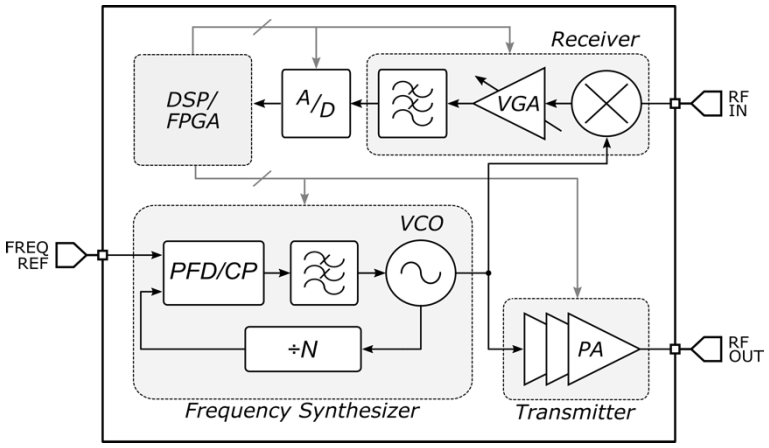


Figure 1.4. A typical FMCW direct conversion transceiver for automotive radar system.

A typical FMCW direct-conversion transceiver for automotive radar application is shown in Figure 1.4. An FMCW waveform, also referred to as a *chirp*, is generated by a frequency synthesizer as a complex sinusoid, whose frequency increases linearly with time. A transmitter (TX) amplifies the FMCW signal with a power amplifier (PA) and radiates it by the antenna. Then, the radiated signal reaches the target, and a portion of its power is back-scattered toward the radar TRX. The resulting *echo* at the radar receiver contains a delayed and attenuated copy of the transmitted chirp. A receiver (RX) collects this back-scattered signal with its antenna, which is then amplified and mixed with the

same FMCW signal used for the TX, thus performing the down-conversion. The resulting base-band signal, referred to as *beat signal*, is then a complex sinusoid, whose frequency, f_b, is the instantaneous difference between the transmitted, f_{TX}, and received, f_{RX}, signal frequencies ($f_b = |f_{\mathrm{TX}} - f_{\mathrm{RX}}|$). If the frequency of the generated FMCW signal is linearly swept with time, then f_b is directly related to the round-trip time-of-flight (ToF) of the signal as well as the Doppler frequency shift. Therefore, after sampling the beat signal, a frequency detection, such as a Fast Fourier Transform (FFT), is performed by the DSP to determine the beat frequency, thus estimating distance and relative velocity of the target in the digital domain.

The transmitted signal frequency is usually swept from a minimum, f_0, to a maximum frequency, $f_0 + B$, with a triangular or sawtooth profile. Since, the transmitted frequency increases linearly with time in a period T_{m}, the frequency slope of the chirp is then determined.

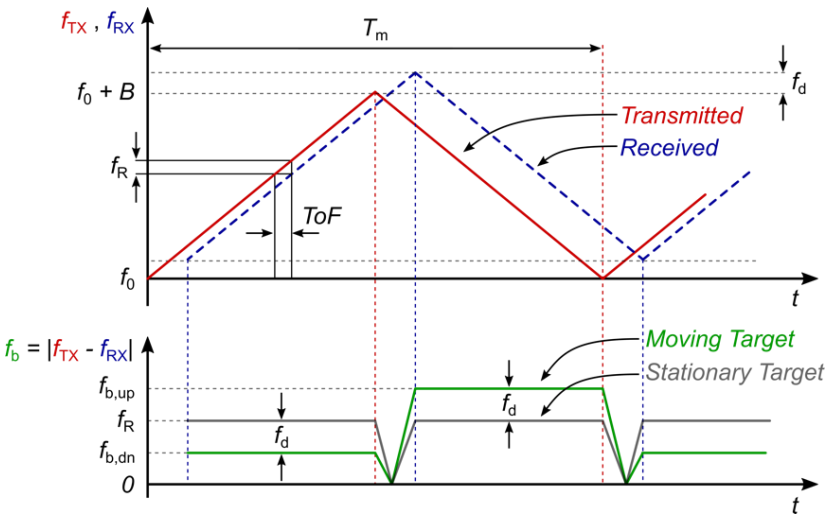


Figure 1.5. FMCW operating principle with triangular chirp profile.

The FMCW operating principle using a triangular chirp profile is shown in Figure 1.5. In such a condition, if a stationary target is located at a distance R from the radar TRX, the echo signal will be received with a delay equals to $\tau = 2R/c$, where c is the speed of light in the free space. The frequency difference between the transmitted and the received signals during the rising and falling slope of the frequency ramp are known as up-chirp beat frequency, $f_{b,up}$, and down-chirp beat frequency, $f_{b,dn}$, respectively. In this case,

the beat frequency is the same for both rising and falling slope of the frequency ramp, and it is only related to *R* as:

$$f_{b,up} = f_{b,dn} = f_R = |f_{TX} - f_{RX}| = \text{SL} \cdot \tau = \frac{4\,R\,B}{c\,T_m} \tag{1.1}$$

where SL is the frequency slope of the chirp. On the other hand, if the target is in relative motion with the radar sensor, a doppler frequency shift, equal to $f_d = \pm(2f_0/c_0)v_r$, will be superimposed on the received frequency, thus obtaining two distinct beat frequencies given by:

$$f_{b,up} = f_R - f_d \tag{1.2}$$

$$f_{b,dn} = f_R + f_d \tag{1.3}$$

Since $f_{b,up}$ and $f_{b,dn}$ are not available simultaneously, the system requires digital processing with a memory that allows measurements of an entire period T_m, after which it will be possible to determine the distance *R* and relative velocity, v_r, of the target as [30]:

$$R = \frac{c\,T_m\,f_R}{4\,B} = \frac{c\,\left(f_{b,up} + f_{b,dn}\right)\,T_m}{8\,B} \tag{1.4}$$

$$v_r = \frac{c\,f_d}{2\,f_0} = \frac{c\,\left(f_{b,up} - f_{b,dn}\right)}{4\,f_0} \tag{1.5}$$

Since distance and relative velocity measurements are related to the frequency of the base-band signal, the measurement resolution is linked to the minimum frequency that the system is capable to appreciate. The beat frequency has a rectangular profile with a period of $T_m/2$, as illustrated in Figure 1.5. Therefore, its corresponding spectrum is a sinc function centered in f_b with first zero crossing at $2/T_m$. Consequently, the smallest frequency that the system can appreciate will be:

$$\Delta f = \frac{2}{T_m} \tag{1.6}$$

Substituting (1.6) in (1.4) and (1.5), the range resolution and the minimal resolvable velocity can be derived as:

$$\Delta R = \frac{c\,T_m}{4\,B} \cdot \Delta f = \frac{c}{2\,B} \tag{1.7}$$

$$\Delta v_r = \frac{c}{2\,f_0} \cdot \Delta f = \frac{c}{T_m\,f_0} \tag{1.8}$$

Consequently, a larger modulation bandwidth is beneficial for a finer range resolution, whereas a longer chirp period offers a better velocity resolution.

However, in a real complex traffic scenario with N moving targets, $2N$ beat frequencies are generated, and the system cannot correctly match the frequency pair of each target, thus causing the so-called *ghost target* problem. As the ghost target issue is related to the rising and falling slope of the triangular chirp, a possible solution lies in the use of multiple chirps with different slope. Nevertheless, this approach requires a more complex algorithms to distinguish real from ghost targets. In principle, sawtooth chirps can be used to avoid the generation of ghost targets. The FMCW operating principle using a sawtooth chirp profile is shown in Figure 1.6.

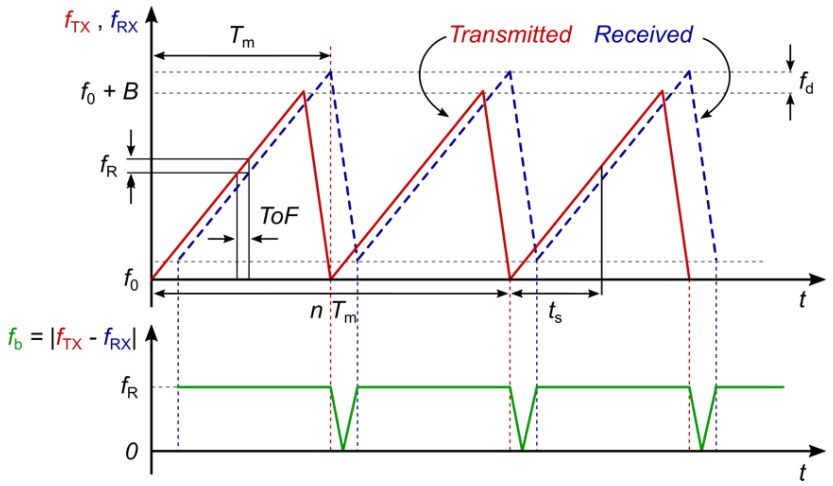


Figure 1.6. FMCW operating principle with sawtooth chirp profile.

In this case, the frequency slope of the chirp is $SL = B/T_m$, thus the transmitted signal can be written as:

$$s_{TX}(t) = A_{TX} \cos\left[2\pi\left(f_0 + \frac{B}{2\,T_m}t_s\right)t_s + \varphi_0\right] \tag{1.9}$$

where t_s is the time from the start of the $(n+1)^{th}$ chirp, defined as $t = t_s + nT_m$ with $0 \le t_s \le T_m$, whereas A_{TX} and f_0 are the amplitude and starting frequency of the TX

signal, respectively. Hence, the echo signal received after the delay τ can be expressed as:

$$s_{RX}(t) = \alpha \cdot A_{TX} \cos\left\{2\pi\left[f_0 + \frac{B}{2\,T_m}(t_s - \tau)\right](t_s - \tau) + \varphi_0\right\} \tag{1.10}$$

where α is a damping factor due to path and reflection losses and τ is the transmission delay of the EM wave. In a relative motion scenario, the frequency of the received signal slightly change over the time, according to time-variant nature of the road-trip delay defined as below. Consequently, the simplified base-band signal can be derived after the down-conversion mixing as:

$$\tau = \frac{2(R + v_r t)}{c} = \frac{2(R + v_r t_s + v_r n T_m)}{c} \tag{1.11}$$

$$s_{IF}(t) = A_{IF} \cos\left[2\pi\left(\frac{B}{T_m}\left(\frac{2R}{c}\right)t_s + \frac{2\,f_0\,v_r}{c}nT_m + \frac{2\,f_0\,R}{c}\right)\right] \tag{1.12}$$

Before the digital processing, the signal is sampled by an ADC whose sample rate is f_s. Hence, the sample index m can be defined as $m = t_s \cdot f_s$ leads to the following expression for the baseband signal.

$$s_{IF}(t) = A_{IF} \cos\left[2\pi\left(\frac{B}{T_m}\left(\frac{2R}{c}\right)\frac{m}{f_s} + \frac{2\,f_0\,v_r}{c}nT_m + \frac{2\,f_0\,R}{c}\right)\right] \tag{1.13}$$

Therefore, distance and relative velocity of the target can be estimated from the beat frequency if the sawtooth chirp is fast enough to make the doppler frequency shift negligible within the period [31]. In this case, the detection of targets and respective distance can be accomplished with a single chirp by means of FFT, while to determine the relative velocity, Doppler frequency shift can be determined by tracking the phase difference between several consecutive ramps, and hence a second FFT is carried out as explained in [32]. For sake of compliance, expression of distance and relative velocity along with range resolution and minimal resolvable velocity for the sawt chirp are derived and reported below.

$$R = \frac{c\,T_m}{2\,B} f_R \tag{1.14}$$

$$v_r = \frac{c}{2\,f_0} f_d \tag{1.15}$$

$$\Delta R = \frac{c}{2\,B} \tag{1.16}$$

$$\Delta v_r = \frac{c}{2\,f_0\,nT_m} \tag{1.17}$$

Finally, it is worth noting that, equations (1.16) and (1.17) describe the ideally achievable resolutions, while their actual values are further limited by several factors including the overlap of the transmitted and received chirps due to the signal propagation delay, time gating to discard highly nonlinearity chirp segments near the chirp turnaround points, and, mostly important, chirp non-linearity [33].

1.4. FMCW radar requirements

To gain insight about design challenge and requirements of automotive radar sensors, is useful starting with the well-known radar equation. Supposing that a power P_T is radiated by a transmitter through an antenna with gain G_T, the power density S_T reaching a target placed at a distance R from the radar sensor is given by:

$$S_t = \frac{P_T G_T}{4\pi R^2} \tag{1.18}$$

The amount of power scattered in the direction of the RX antenna will be a function of the target size, material, orientation, and profile which are taken into account through a parameter known as radar-cross section (RCS) σ. Therefore, the backscattered power, P_r, at the target location is equal to:

$$P_r = S_t\sigma = \frac{P_T G_T \sigma}{4\pi R^2} \tag{1.19}$$

Since power decays at a rate of $1/R^2$ away from the target, the power density at the RX antenna location due to backscattered power, P_r, will be:

$$S_R = \frac{P_r}{4\pi R^2} = \frac{P_T G_T \sigma}{(4\pi R^2)^2} \tag{1.20}$$

Assuming a receiving antenna with an effective area, A_R, the receiving power, P_R, is given by:

$$P_R = S_R A_R = \frac{P_T G_T \sigma A_R}{(4\pi R^2)^2} \tag{1.21}$$

A_R is also used in direct relationship to the gain G_R:

$$G_R = \frac{4\pi A_R}{\lambda^2} \tag{1.22}$$

This yield

$$P_R = \frac{P_T G_T G_R \lambda^2 \sigma}{(4\pi)^3 R^4} = \frac{P_T A_T A_R \sigma}{4\pi \lambda^2 R^4} \tag{1.23}$$

where A_T is the effective area of the TX antenna. To take into account losses due to atmosphere or any mismatch in power and polarization, a term L_{ATM} is usually introduced and hence the previous equation becomes:

$$P_R = \frac{G_T G_R \lambda^2 \sigma}{(4\pi)^3 R^4 L_{ATM}} P_T \tag{1.24}$$

Moreover, the lowest detectable power level of RX, $P_{R,min}$, can be expressed as:

$$P_{\mathrm{R,min}} = NF \cdot kT \cdot \mathrm{BW_{FFT}} \cdot SNR_{\mathrm{min}} \tag{1.25}$$

where kT have the usual meaning, NF and $\mathrm{SNR_{min}}$ are the noise factor and the minimum signal-to-noise ratio of the overall RX, while BW_{FFT} denotes the FFT resolution bandwidth used for the beat frequency processing. By combining (1.25) and (1.24), the maximum range of coverage, R_{max}, (i.e., the distance beyond which the signal level at the receiver input is too small to be detected), can be evaluated as:

$$R_{max} = \sqrt[4]{\frac{G_T G_R \lambda^2 \sigma}{(4\pi)^3 kT \cdot L_{ATM} \cdot BW_{FFT} \cdot SNR_{min}} \left(\frac{P_T}{NF}\right)} \tag{1.26}$$

In a typical application scenario, a multimode radar sensor must be able to guarantee an operating distance R ranging from a few meters to about 250 m, with a resolution better than 5 cm in the short-range operation mode. Assuming an operating frequency of

79 GHz, the signal wavelength, λ, is 3.8 mm, whereas the atmosphere propagation losses, L_{ATM}, can be approximated around 0.3−0.5 dB/km, according to [34]. The transmitting and receiving antenna gains, i.e., G_T and G_R, can be assumed around 20 dBi, while 1 kHz is the typical FFT resolution bandwidth. To guarantee 99% detection probability along with 10^{-8} false alarm ratio (FAR), SNR_{min} higher than 16 dB should be achieved as suggested in [35]. Based on these assumptions and considering that the radar-cross section for a mid-size car is about equal to 30 m^2 [30], the relationship between transmitted power, NF, and maximum detectable distance, are shown in Figure 1.7.

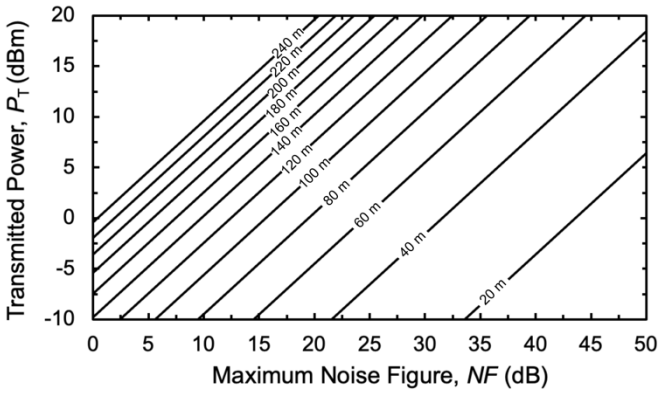


Figure 1.7. Relationship between PT and NF for different maximum detectable distance.

An average output power of 13 dBm is a reasonable value for a 28-nm CMOS PA [36]. Therefore, to achieve a maximum detectable distance of 250 m, the RX should be designed to provide a noise figure below 16 dB, according to Figure 1.7. This means that, for an operating distance ranging from 250 m to 2 m, the echo signal power spans from −110 dBm to −30dBm. Hence, the receiver input signal is characterized by a wide range of variation (i.e., 80 dB) along with a very low minimum level. In addition, FMCW architectures highly suffer from the crosstalk between TX and RX. Indeed, a portion of the TX output power leaks to the RX input, thus leading to a high blocking signal for the receiver at the same frequency of the transmitted one, thus producing a big offset after down-conversion. Assuming a typical 20 dB of attenuation, the power level of this spurious signal at the receiver input is around −10 dBm, which is much higher than the received echo signal. Consequently, sensing the low-level signal reflected by the target, superimposed to an extremely high blocking signal, poses severe constraints to the radar receiver mainly in terms of gain and linearity performance. To overcome this drawback,

the TX leakage has to be suppressed as proposed in [37] for a 28-nm CMOS radar receiver.

The frequency synthesizer performance is also critical for FMCW radar system. As discussed in the previous section, the FMCW chirp bandwidth, B, and period, T_m, must be carefully designed to meet radar system requirements. For instance, to achieve 5 cm of range resolution, ΔR, a chirp bandwidth wider than 3 GHz is required. While for a Δv_r as low as 0.5 m/s, the data length per frame, i.e. nT_m, needs to be larger than 3.9 ms. Furthermore, the frequency synthesizer phase noise as well as the non-linearity in the chirp generation significantly affect the FMCW radar performance. Specifically, the phase noise that is converted into the baseband noise after the down-conversion affects the receiver SNR. By following the analysis carried out in [38] and [39], if a PLL is used to implement the frequency synthesizer, the phase noise contribution to the SNR can be evaluated as:

$$SNR_{PN} = \frac{1}{2\,\sigma^2_{\varphi,out}} \tag{1.27}$$

where $\sigma^2_{\varphi,out}$ is the phase variance of the baseband signal given by:

$$\sigma^2_{\varphi,out} = \int_0^\infty S_{\varphi,out}(f)df = \frac{D_\varphi}{\pi f_{PLL}}\left[1 - exp\left(-\frac{4\pi f_{PLL} R}{c}\right)\right] \tag{1.28}$$

where f_{PLL} is the PLL bandwidth and D_φ is the phase diffusivity expressed as:

$$D_\varphi = 2\pi^2 S_{\varphi,VCO}(\Delta f)(\Delta f)^2 \tag{1.29}$$

where $S_{\varphi,VCO}(\Delta f)$ is the PLL phase noise given at the offset frequency, Δf, located in the region of the phase noise spectrum with −20 dBm per decade. According to (1.27), (1.28) and (1.29), setting the PLL bandwidth and the target distance to 300 kHz and 250 m, respectively, 99% detection probability with 10^{-8} FAR can be achieved if the PLL provides a mm-wave signal with a phase noise less than –92 dBc/Hz at 1 MHz frequency offset. Fortunately, transmitted and received signal phase noise components are partially correlated. Since the baseband signal is obtained by mixing the received signal with the transmitted one (i.e., the LO signal), part of the phase noise is cancelled out thanks to the correlation, thus improving the radar sensitivity and relaxing the phase noise requirement.

The effectiveness of this cancellation, which is not considered in (1.29), is closely related to the target distance as investigated in [40].

As far as the nonlinearity of the FMCW chirp is concerned, it affects the radar distance resolution. Following [1] and [41], the FMCW chirp nonlinearity is defined as:

$$Lin = \frac{\delta f}{B} \tag{1.30}$$

where B is the bandwidth of the FMCW chirp and δf is the frequency error. By considering the chirp nonlinearity, the distance resolution expressed by (1.16) becomes:

$$\Delta R = \sqrt{\left(\frac{c}{2\,B}\right)^2 + (Lin \cdot R)^2} \tag{1.30}$$

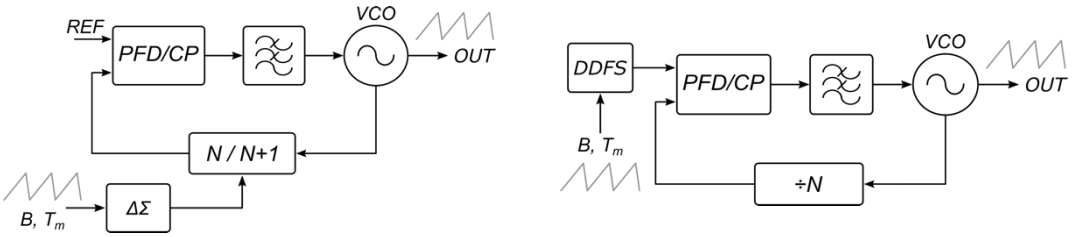
Therefore, for a FMCW chirp bandwidth of 4 GHz and a 250-m detection distance, to achieve a distance resolution of 0.05 m requires a nonlinearity ratio, *Lin* defined as (1.30), less than 0.02%.

1.5. Frequency synthesizer for FMCW radar application

As highlighted from the analysis carried out in the previous sections, frequency synthesizers are key components for the FMCW radar sensor, since both distance and velocity resolution are determined by chirp bandwidth and period, respectively. A highly linear FMCW chirp is also required to minimize the frequency error which deteriorates both distance and velocity accuracy [42]. An adequate phase noise performance is also crucial to preserver the overall SNR in the receiver. Moreover, in a real multi-target scenario, since the power of received signals can vary significantly, the synthesizer phase noise up-converted around the most powerful tone can degrade other weaker signals.

Phase-Locked Loop (PLL) has been shown to be more effective in linear FMCW chirp generation compared to the open loop techniques [43]. Presently, fully-integrated synthesizer PLLs can be implemented in analog or digital fashion. All-digital PLLs offer a great programmability and area efficiency but they suffer from a lower output

frequency, which requires many frequency-multiplication stages to achieve the mm-wave spectrum [43]. In addition, the use of conventional time-to-digital converters (TDCs) results in a poor time resolution, which severely affects the PLL phase noise [44]. Consequently, the analog implementations still dominate as the most feasible for mm-wave frequency synthesizers. In such implementation, FMCW chirp signals can be generated either with a fractional-N PLL whose output is modulated by an integrated delta-sigma (ΔΣ) modulator [30], or with a direct digital frequency synthesizer (DDFS) whose frequency modulated output drives the reference input of an integer-N PLL [45].



(a) (b)

Figure 1.8. FMCW synthesizer with (a) fractional-N PLL and (b) DDFS based approaches.

In a fractional-N PLL approach, the frequency modulation is performed by changing the division ratio, as is shown in the simplified block diagram in Figure 1.8 (a). Fractional division is accomplished by the ΔΣ-modulator, which switches the programmable divider between different integer values, thus achieving the desired average fractional value. Modulation of the feedback divider approximates the desired FMCW signal as sequence of discrete levels with a certain stepping rate. The advantages of this solution are both lower power consumption and silicon area. It is an increasingly popular approach especially when digital PLL or two-point modulation techniques are employed [46], [47]. However, a slow settling time, which is limited by the PLL loop bandwidth, is typically ehibited by this solution. In contrast, the DDFS-based solution, whose simplified block diagram is reported in Figure 1.8 (b), has the merit of more flexible chirp period configuration and better phase noise, mainly due to the absence of the ΔΣ-modulator. Here, the frequency modulation is simply accomplished by changing the input reference provided by the DDFS. However, this approach suffers from a higher power and area penalties, primarily due to the DDFS, which could require high-resolution digital-to-analog converters (DACs) and large read-only memory (ROM) to achieve fine frequency tuning. Also in this case, the desire FMCW waveform is provided as series of

discrete levels in a stair-step shape. Requirements of the DDFS, such as clock frequency and phase resolution, can be determined by the range accuracy and corresponding ToF.

However, the stair-step approximation of the chirp signal leads to trade-offs in the choice of the PLL bandwidth. Indeed, the PLL should exhibits a settling behavior fast enough for the PLL output frequency to accurately follow the chirp trajectory, thus resulting in a PLL loop bandwidth much larger than chirp modulation frequency. On the other hand, the PLL bandwidth must be small enough to smooth the stair-like PLL output signal, which would cause degradation in chirp linearity. Consequently, a proper choice of the FMCW chirp slope has a significant impact on this trade-off as well as on the overall radar performance.

The adoption of slow and moderate chirps, i.e. with low and moderate slopes, allows relaxing the PLL bandwidth requirements. Unfortunately, the beat frequency generated in this case typically falls into the higher phase noise region of the synthesizer and could be covered by the phase noise itself. Conversely, fast chirp modulation results in a higher beat frequency, which falls into a region with a lower phase noise, thus improving the baseband SNR. By reducing the period of the chirp, a faster target identification as well as distance and velocity sensing is achieved. In a multi-target scenario, if a faster chirp is used, the resulting beat frequencies will be more separated from each other, further relaxing the phase noise requirements. However, a faster frequency modulation requires a faster PLL settling time, which results in a wider PLL bandwidth. Furthermore, the generation of fast chirps could increase the close-in phase noise of the analog charge-pump. This is because fast chirps result in a large static phase error at the phase detector and thus a large charge pump duty cycle [44]. This effect is qualitative described in [48], where the adoption of a programmable loop filter capacitance is suggested to enable phase noise optimization for a given charge pump current and chirp slope.

In principle, faster chirps can be achieved either by reducing modulation period or increasing bandwidth. Increasing the modulation chirp bandwidth could be beneficial for the range resolution, but the PLL output frequency range is typically limited by the VCO tuning range. Consequently, faster chirps are commonly generated by shorter the modulation period. However, this leads to a reduction in the velocity resolution in the case the triangular profile is used. Therefore, the trade-off between chirp slope and velocity resolution must be considered for a targeted application. Alternatively,

implementation of different methods for extracting velocity information from the target, such as speed calculation based on consecutive range measurement results, could be considered.

1.6. The adopted technology platform: a 28-nm FD-SOI technology overview

Compared with the more traditional III-V semiconductor technologies, the CMOS technology is inferior in some of the most important performance parameters for active devices, such as maximum oscillation frequency, transition frequency, breakdown voltage, etc. However, higher integration level, lower power consumption and lower manufacturing costs have imposed the use of CMOS technologies for an ever-increasing number of applications.

Nowadays, the CMOS technology is already the standard and most cost-effective process for building digital circuits. Modern CMOS technologies allow both RF/mm-wave front-end and analog/digital base-band of the radar transceiver to be integrated in a single chip, thus providing a system-on-chip (SoC) implementation. Furthermore, the operation at mm-wave frequencies reduces the antenna size, thus enabling new packaging options including integration of the antenna on an advanced package solution.

With reference to the evolution of CMOS technology, integration scaling has led to light some important limitations for an efficient integration in a planar process, starting from the 40 nm technology node [49]. Consequently, fully depleted technologies have become predominant in semiconductor industry with the advent of the 28-nm CMOS technology node. Two main processes for fully depleted active devices have been identified by the semiconductor industry, referred to as FinFET CMOS and Fully Depleted Silicon on Insulator (FD-SOI) CMOS devices.

The VCO designs described in this work will benefit of the high-performance provided by the 28-nm FD-SOI CMOS technology platform by STMicroelectronics.

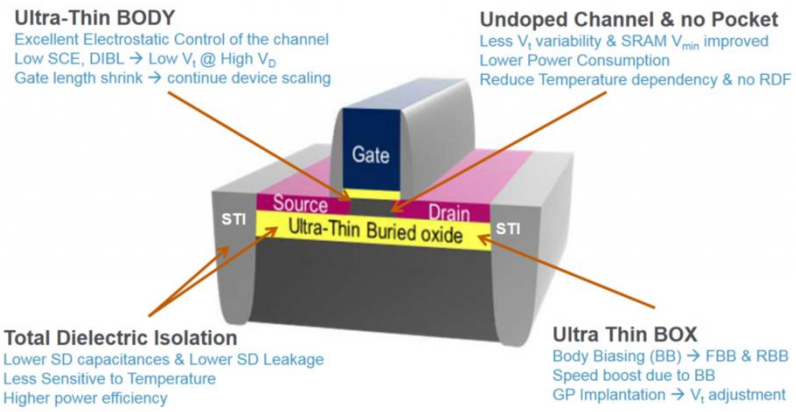


Figure 1.9. Cross section of FDSOI transistor along with its main technological advantage.

A generic cross-section of an FD-SOI transistor is shown in Figure 1.9 along with its main technological transistor advantages over a more traditional device. These advantages latter rely on two important innovations, which are a complete oxide isolation (BOX)and a very thin silicon film for the transistor channel. Due to these features, this technology is called Ultra-Thin Body and Buried Oxide (UTBB) FD-SOI CMOS. In the 28-nm node, the active devices are characterized by an ultra-thin conduction film of 7 nm and an oxide BOX of 25-nm insulation layer.

Therefore, the total dielectric isolation reduces parasitic components, thus reducing crosstalk between circuits and increasing frequency stability. Due to the thin silicon film, no channel doping is needed, thus making the transistor channel fully depleted. As a results, several process steps, such as channel implants, halo implants, and masking levels, are removed compared with a traditional bulk process. In addition, no pocket implants are needed for source and drain terminals, thus resulting in an enhanced high-frequency transistor behavior. Another interesting implication of the isolation BOX is the control of transistor threshold voltage from the body underneath the BOX (i.e., body biasing). Indeed, the threshold voltage can be varied by applying a voltage on the body. Therefore, transistors can be seen as planar dual-gate devices with the usual front-side gate terminal like in bulk technology and a second gate terminal provided by the body, where the buried oxide acts as back-side gate. Of course, the lower thickness of the front gate oxide with respect to the back gate one, provides ta larger transconductance than the body transconductance.

Compared with transistors implemented in traditional 28-nm CMOS bulk process, FD-SOI transistors provide a higher transconductance for a given current. This, combined with the lower parasitic capacitances due to oxide isolation, allows higher operating bandwidths, high gain, and lower power consumption to be achieved.

Parameter variability is also improved with respect to an equivalent bulk node, due to simpler manufacturing process steps. Thanks to the deep submicron lithography, this technology provides very fast transistors with f_T / f_{MAX} higher than 300-GHz and hence is able to cope with mm-wave operation. The body biasing feature can be profitably used to reduce PVT variations, which are critical in automotive radar applications. All these features make the 28-nm FD-SOI CMOS technology a very promising candidate for SoC implementation of automotive SRR and LRR sensors.

As far as the back-end-of-line (BEOL) is concerned, it is usually not inherently optimized for high-quality integrated passive components, as in most of nanometer CMOS technologies, despite they are key components in mm-wave circuit design. Although this might be seen as a limiting point, the eight metal layers of this technology allow quite good values for integrated passive components as demonstrated in this work. Specifically, inductors and transformers can take advantage of the last two copper metal layer in addition to the aluminum one at the top of the stack to reduce series losses and achieve acceptable quality factors.

Finally, high performance mm-wave integrated circuits can well benefit from advanced FD-SOI CMOS technologies despite the low-cost general-purpose BEOL is not best choice for mm-wave applications.

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Chapter 2

Integrated inductors and transformers: basic concepts on silicon technology for mm-wave applications

2.1. Introduction

Since Nguyen and Meyer demonstrated the feasibility of integrated inductors on silicon substrates, huge research efforts have been dedicated to their analysis, design, modelling, and optimization. The hundreds of papers dealing with integrated inductors published in specialized journals during the last two decades corroborate this fact. As a result of these efforts, the integrated inductor performance has been noticeably improved.

On the other hand, increasing demand for higher integration levels and lower fabrication costs has pushed the use of monolithic passive components in silicon RF/mm-wave ICs, thus promoting both layout and technology advances. Monolithic inductors and transformers [1], [2] are key components in the design of mm-wave integrated circuits such as voltage-controlled oscillators (VCOs) for frequency synthesizer [3], [4], integrated power amplifier [5], [6], low-noise amplifiers [7], [8] mixers [9], [10], etc. In particular, integrated transformers are very important passive components, especially at mm-wave frequencies, since they allow the implementation of several crucial functions such as single-ended-to-differential and differential-to-single-ended conversion, ac-coupling with easy bias point, electrostatic discharge (ESD) protection with galvanic isolation at input/output antenna interfaces [11], [12], resonant loads in RF/mm-wave amplification stages [13], [14] LC tank in oscillator [15], [16], signal or power combining [17], [18], etc. In addition, transformer

provide passive voltage or current gain, and hence, they inherently feature impedance transformation, resulting very suitable in filters and matching networks [19], [20]. However, as the frequency goes up, the losses in the passive components rise accordingly, thus affecting the circuit performance, especially with nanometer CMOS technologies. Furthermore, parasitic inductances coming from the interconnections have a not negligible weight compared with the low inductance values typically used in mm-wave circuits. Consequently, designing high performance on-chip inductors and transformers is a crucial task to set the overall performance of the entire mm-wave transceiver.

In this chapter integrated transformers are analyzed with the aim of highlighting key aspects of their properties. This knowledge will prove very useful to guide the circuit designer towards an efficient/optimum design of these components and help him to fully exploit their potential. Since an integrated transformer is nothing else than two coupled inductors, a solid knowledge of the characteristics and limitations of the integrated inductors represents an excellent starting point for the analysis of integrated transformers. Therefore, this chapter starts with Section 2.2 where a brief review of integrated inductors is provided, pointing out their fundamental characteristics and the main loss mechanisms that occur in silicon technology. Next, these concepts will be applied to the design of integrated transformers for mm-wave applications. In particular, Section 2.3 deals with the design and comparative analysis of three integrated transformers exploiting the most suitable configuration for a CMOS *W*-band automotive radar application. Finally, since the parameters of the transformer are closely related to those of the adopted technology, a comparative analysis of two 28-nm CMOS technologies based on standard and mm-wave-optimized (i.e., thick metals and intermetal oxides) back-end-of-line (BEOL) is provided in Section 2.4. The proposed comparison is carried out at both component and circuit level by means of a quantitative analysis, which provides the rate of performance improvement due to the adoption of a mm-wave-optimized BEOL. To this end, stand-alone transformer performance is first evaluated and then a 77-GHz down-converter for radar applications has been investigated as testbench.

2.2. Fundamental parameters of integrated inductors and main loss mechanisms

Inductors are planar windings made up of one or more metal layers that are available in the BEOL provided by the adopted technology. The top metal layers are typically made thicker than the other interconnection metals to reduce ohmic losses in supply distribution networks, and hence they are the most suitable layers for integrated inductor implementations. The geometric shape of the spiral winding affects performance and chip. Although a circular shape usually represents the best choice for the winding implementation, it is not always allowed by CMOS foundries in their design kits (DK) and hence, octagonal or square shape are the most common alternative. For a given shape, an integrated inductor is completely defined by a set of geometrical parameters such as the width of the metal layer (w), the numbers of the turns (n), the spacing (s) between adjacent layers, the outer (d_{out}) and inner diameter (d_{in}), as illustrated in Figure 2.1.

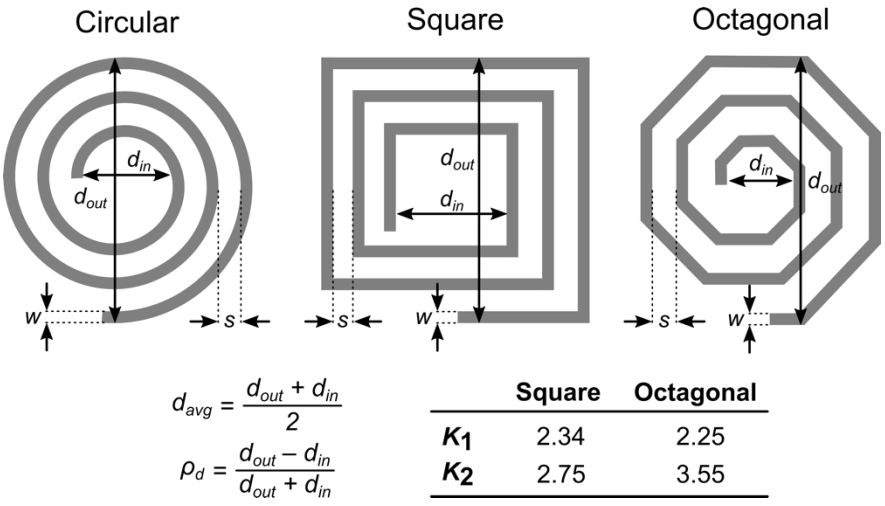


Figure 2.1. Examples of integrated inductors along with their main geometrical parameters.

Starting from these geometrical parameters, some compact approximated expressions are reported in literature to predict the inductance winding, such as [21]:

$$L = K_1 \mu_0 \frac{n^2 d_{avg}}{1 + K_2 \rho_d} \tag{2.1}$$

where the average inductor diameter, d_{avg}, and fill factor, ρ_d, are defined as in Figure 2.1 along with the inductor shape parameters, K_1 and K_2. However, inductance

value is only roughly estimated by (2.1) and hence electromagnetic simulations should be employed to verify and optimize the inductor size.

Two fundamental performance parameters that characterize the performance of any integrated inductor are the self-resonance frequency (f_{SR}) and the quality factor (Q). The self-resonance frequency is caused by the parasitic capacitance and gives an estimation of the maximum operating frequency at which the inductor can work. For frequencies higher than f_{SR}, the inductor shows a negative reactance, i.e. it operates like a capacitor. Because the parasitic capacitance is approximately proportional to inductance value, f_{SR} decreases as the inductance increases. In any practical application, inductors are designed to operate at a frequency equal to a fraction of f_{SR}, and this means that there is a maximum value of inductance that can be used for a given operating frequency. Therefore, large inductances that are important for higher gain cannot be used at high frequencies.

As far as the quality factor (Q) is concerned, it can be seen as a measure of the energy lost in the metal layers of the windings, in the non-ideal dielectrics, as well as in the conductive layers of the substrate. For any frequency of interest, ω_0, the Q-factor is defined as the ratio between electromagnetic energy stored by the inductor, (E_S), and the energy dissipation, E_D, in a cycle, $T = 2\pi/\omega_0$, according to:

$$Q = 2\pi \frac{E_S}{E_D} \tag{2.2}$$

Therefore, the higher the quality factor, the smaller the energy dissipated in the component. Applying equation (2.2) to the ideal case of an isolated coil, where the only considered loss is the series resistance, R_S, provides the well-known equation (2.3).

$$Q = 2\pi \frac{P_S \cdot T}{P_D \cdot T} = \omega_0 \frac{LI^2/2}{R_S I^2/2} = \omega_0 \frac{L}{R_S} \tag{2.3}$$

where P_S and P_D are the stored and dissipated power in the inductor layer, respectively, while I is the root-mean-square (rms) current flowing through the coil and L is the coil inductance. However, the inductor Q-factor is not limited only by the series resistance, but several other loss mechanisms are involved making accurate prediction of the quality factor a very complex task. Indeed, loss phenomena taking place not only in the coil but also in the substrate must be taken into proper account. Consequently, understanding

losses mechanisms and arrange the geometric parameters of the structure to minimize loss effects is a crucial step in the high-performance integrated circuit design.

2.2.1. Main loss mechanisms

The main energy dissipation mechanisms that affect the performance of an integrated inductor are sketched in Figure 2.2.

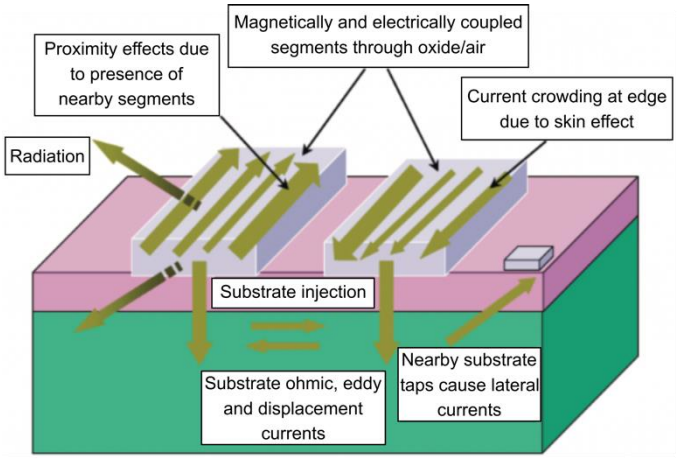


Figure 2.2. Energy dissipation mechanisms in an integrated inductor.

At the frequencies of interest, the most important losses occur in the metal layers used for the winding as well as in the conductive layers on the silicon substrate below the inductor. These loss phenomena can be coarsely divided in the so-called metal or series losses, caused by the ohmic energy dissipated in the coil metal, and substrate or parallel losses, related to electromagnetic coupling between the winding and the lossy substrate on which the inductor is fabricated.

At low frequency, series losses are mainly caused by the finite conductivity of the employed metal layers (i.e., Cu or Al). Specifically, the current flow is uniformly distributed inside the entire conductor cross-sectional area, which results in a constant coil series resistance determined by the thickness and width of the metal trace. However, as frequency rises, the ohmic losses rise as well. The current is no longer uniformly distributed in the metal trace but tends to flow in a thin region in the outer metal surface due to the skin and proximity effect. This leads to a reduction of the effective conductor cross-section area available for current conduction, which results in a coil equivalent series resistance that increases with frequency. Skin effect occurs when an alternating

current flow through an insulated conductor with finite conductivity. The density current flow, *J*, within the conductor generates a magnetic field, *B*, lying in the plane orthogonal to that of the current flow as describe from the Ampere's law, reported below for a sake of completeness.

$$\nabla \times \vec{B} = +\mu\vec{J} + \varepsilon\mu\frac{\partial\vec{E}}{\partial t} \tag{2.4}$$

On the other hand, the generated time-varying *B*-field induces an electric field, *E*, lying in the same plane as the original current flow that opposes to the *B*-field itself and, in turn, to the original current, according to Faraday's law reported below.

$$\nabla \times \vec{E} = -\frac{\partial\vec{B}}{\partial t} \tag{2.5}$$

Since the magnitude of the self-induced *E*-field is higher at the center of the conductor, the current crowds toward the outer surface. This phenomenon is graphically explained in Figure 2.3 for an isolated conductor, where darker gray represents higher current density.

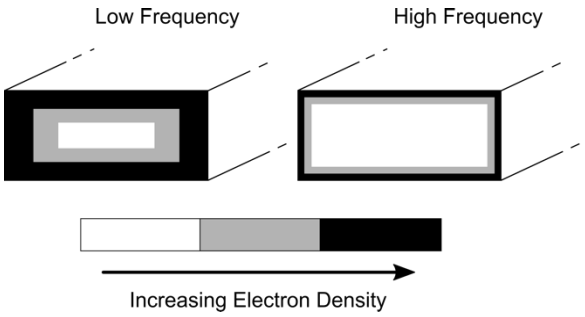


Figure 2.3. Skin effect in an isolated conductor with rectangular cross section.

As the frequency increases, the magnitude of the self-induced electric field also increases, forcing the current to flow in a thin layer (skin) at the edge of the conductor cross-sectional area, which gives the name to this phenomenon. The resulting current density follows an exponential decay from the outer surface to center of the conductor given as:

$$J = J_0 \cdot e^{-\frac{x}{\delta}} \tag{2.6}$$

where x is the radial distance from the edge to the center of the conductor and δ is the penetration depth defined as:

$$\delta = \sqrt{\frac{2\,\rho}{\omega\,\mu}} \tag{2.7}$$

where ρ is the conductor resistivity, ω is the angular frequency, and μ is the magnetic permeability.

As far as the proximity effect is concerned, it takes place when two or more metal spirals, carrying an alternating current flow, are placed close to each other as illustrated in Figure 2.4.

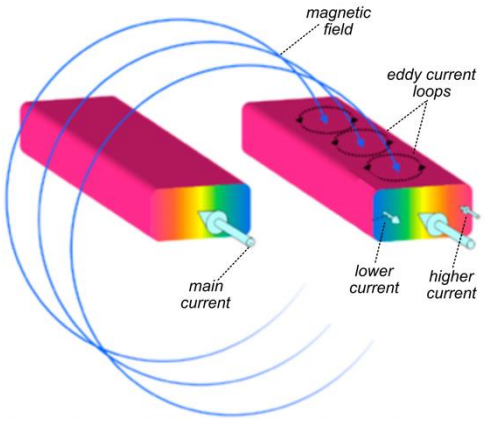


Figure 2.4. Proximity effect for two neighboring conductors.

The current flowing in a coil generates time varying *B*-field, which induces loops of current in the other coils, known as eddy current loops, according to the Faraday's law. This eddy currents are added to the coil current on the outside edge of the trace and subtracted from it on the inside edge, thus causing a crowding effect at the conductor outside edge. Consequently, the current flow in a winding becomes nonuniform and strongly dependent on the spatial distribution of the neighboring conductors.

Besides series losses also substrate losses contribute to worsen the *Q*-factor of integrated reactive structures in silicon technology. Basically, the cause of substrate losses manly lies in the capacitive and magnetic coupling between the metal layers of the windings and the underlying lossy substrate, which is again governed by Maxwell equations. These losses come into play at higher frequencies than series losses. Indeed,

the generated time-varying *E*-field and *B*-field in the substrate have smaller magnitude at lower frequency, since the substrate conductivity is lower than metal one. Due to the finite conductivity of the substrate, the generated *E* and *B*-fields produces current flows in the layers below the windings.

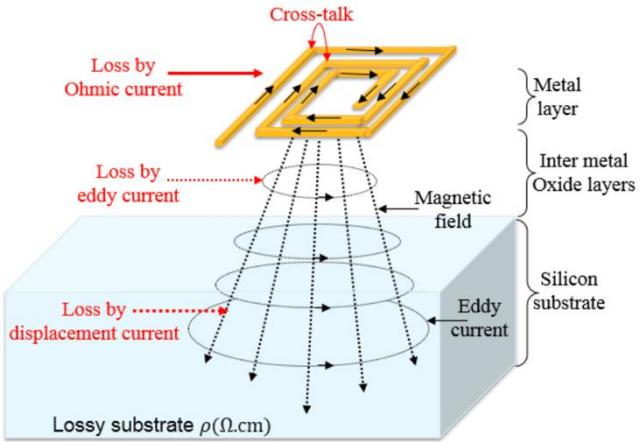
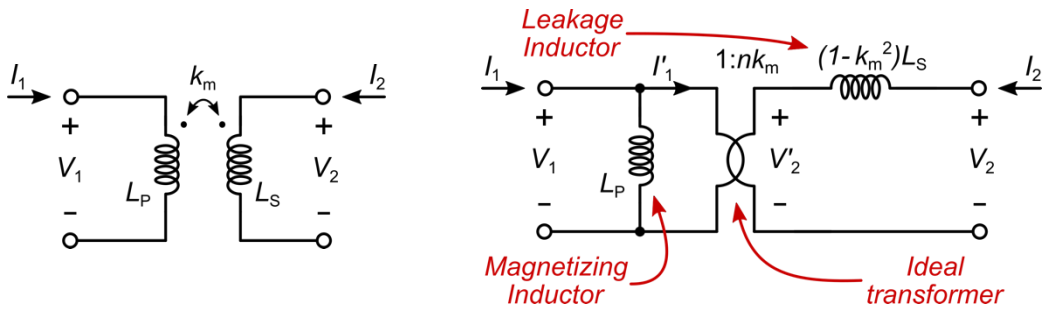


Figure 2.5. Substrate losses in an integrated inductor.

Figure 2.5 depicts the two phenomena that are responsible for the substrate losses. The capacitive coupling between windings and substrate results in vertical displacement currents through the dielectric layers (e.g., silicon oxide) that isolate the coils from the substrate. On the other hand, due magnetic coupling, eddy currents are induced in the substrate that flow in antiparallel to the currents impressed in the coils. Besides increasing the energy dissipation in the structure, eddy currents in the substrate induce a magnetic field that opposes that generated by the current in the winding, thus reducing the effective coil inductance by a small amount.

2.3. Integrated transformers: basic concept and design for mm-wave applications

As mentioned above, integrated transformers are fabricated by exploiting the mutual inductance between two or more inductors, which couple a signal from the *primary coil* to the *secondary coil*, without significant power losses. The symbol of the transformer is shown in Figure 2.6 (a). To describe integrated transformers, equivalent lumped circuits are often used. Among various possible equivalent circuits reported in literature, that one displayed in Figure 2.6 (b) results particularly simple and insightful [1], [22]. Only three components are used to implement this equivalent model. The first is an inductor shunting the primary coil of an ideal transformer, called *magnetizing inductor*, which accounts for the magnetic flux in the component to operate. A second inductor, called *leakage inductor*, models the limited coupling between the coils, which results in a flux leakage. Finally, the third component is an *ideal transformer* which is a lossless two-port network whose behavior is described by the ratio of the voltage at its ports equal to $V_S'/V_P = n \cdot k_m$. Here parameter n, defined as $n = \sqrt{L_S/L_P}$, is called turn ratio and parameter k_m is the transformer coupling factor. Due to the lack of losses, the ideal transformer exhibits an intrinsic impedance transformation feature described by $V_S'/I_S = (-V_P/I_P')n^2k_m^2$. This means that if the primary (secondary) port is terminated with an impedance, Z, at the secondary (primary) port the impedance Z is scaled up (down) by the square of the ideal transformer voltage gain [22].



(a) (b)

Figure 2.6. Schematic symbol of (a) coupled inductors and (b) its equivalent circuit.

In addition, the equivalent model illustrated in Figure 2.6 (b) can be enriched with further parameters, which account for losses and finite resonant frequency, thus

describing a real integrated transformer. However, along with the main performance parameters used for integrated inductor, such as, primary and secondary coil inductance, referred to as L_P and L_S, primary and secondary coil Q-factor, referred to as Q_P and Q_S, and f_{SR}, other parameters including transformer coupling factor (k_m), insertion loss (*IL*) and transformer characteristic resistance (*TCR*) [23] are used to fully describe the performance of an integrated transformer. Specifically, the *IL* provides a significant performance characterization when transformers are exploited in signal conversion/power combining under the assumption of *50*-Ω termination for both primary and secondary windings. Typically, this happens when the transformer is used at the input interface, for example between the antenna and the receiver (RX) front-end. In this scenario, *IL* directly affects both gain and noise figure (*NF*) of the RX. On the other hand, the *TCR* can be seen as the generalization of the well-know ωQL product for the transformer-loaded circuits. It represents the equivalent impedance offered by the transformer in the resonance condition and is the reference performance parameter when the gain of a transformer-loaded stage must be maximized. For the sake of completeness, expression for *IL* and *TCR* are reported below.

$$IL = -20 \cdot \log S_{21} \tag{2.8}$$

$$TCR = \omega Q_{EQ} L_{EQ} \tag{2.9}$$

with

$$Q_{EQ} = Q_P \frac{k_m^2 Q_P Q_S}{1 + k_m^2 Q_P Q_S} \cong Q_P \tag{2.10}$$

$$L_{EQ} = L_P \left(1 + \frac{1}{Q_p^2} + k_m^2 \frac{Q_S}{Q_P}\right) \cong L_P \left(1 + k_m^2 \frac{Q_S}{Q_P}\right) \tag{2.11}$$

According to the circuit design specifications, integrated transformers are usually implemented using conventional interleaved or stacked windings. Stacked transformers [2] are made up of two identical coils implemented using different metal layers placed one on top of the other, as shown in Figure 2.7 (a). This arrangement allows a relatively large magnetic coupling factor, k_m, to be achieved at the cost of larger parasitic capacitance between the transformer windings. In addition, since one coil is implemented in a lower metal layer, which usually is much thinner, both quality factor and parasitic

capacitance toward the substrate worsen. To avoid these drawbacks, the interleaved structure can be used, implementing both primary and secondary windings with the same metal layer, as displayed in Figure 2.7 (b). However, interleaved structures provide a smaller magnetic coupling along with an asymmetry in electrical/geometrical parameters between primary and secondary windings.

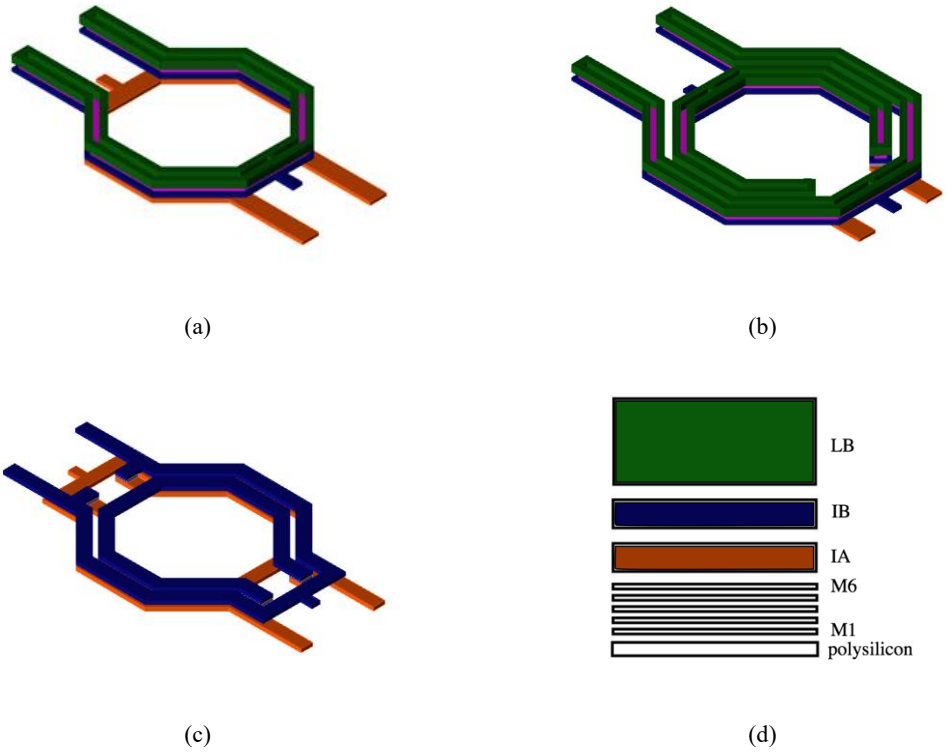


Figure 2.7. 3D-view of (a) stacked, (b) interleaved and (c) interstacked transformers (d) 28-nm FD SOI CMOS BEOL.

Some interesting variations to conventional transformer configurations were introduced over the years, with the aim of reducing series/substrate losses as well as to maximize the magnetic coupling factor. Among them, interstacked structures represent a valid solution for mm-wave integrated transformers [24], [25]. Interstacked transformers adopt a mixed interleaved/stacked coil configuration, which allows a high magnetic coupling to be achieved as well as a high electrical/geometrical symmetry between primary and secondary coil. Specifically, outer (inner) spiral of primary winding is stacked to the outer (inner) spiral of the secondary winding and interleaved with the inner (outer) spiral of the secondary winding at the same time, as illustrated in Figure 2.7 (c). For a sake of completeness, the adopted BEOL is also reported in Figure 2.7 (d).

2.3.1. Design and comparison of three integrated transformers for mm-wave applications

A comparative analysis of monolithic transformers was carried out to identify the most suitable structure for typical mm-wave radar circuits as well as to gain insight on transformer design itself [26], [27]. To this aim, three octagonal single-turn transformers were designed in 28-nm FD-SOI CMOS technology by adopting stacked, interleaved, and interstacked configurations, respectively, through extensive use of 2D electromagnetic (EM) simulations in Advanced Design System (ADS) Momentum by Keysight Technologies. Each of the designed strictures was sized to achieve a f_{SR} at least about twice the operating frequency (i.e., 77 GHz). As depicted in Figure 2.7 (d), the adopted 28-nm FD-SOI CMOS technology [28], by STMicroelectronics, provides a general-purpose low-cost back-end-of-line (BEOL) consisting of eight copper metal layers, whose thicker ones are the last two (referred to as IB and IA) and an aluminum metal layer (LB) at the top of the stack.

Based on loss mechanisms analysis previously carried out, to reduce both series and substrate losses, the two thick-copper metals, namely IA and IB, in addition to the aluminum one, namely LB, can be profitably used to implement integrated transformer coils. The choice of the metal width as well as the number of turns should be oriented to maximize the *Q*-factor at the operating frequency of both primary and secondary windings. However, the skin/proximity effects along with the increase in the parasitic capacitances towards the substrate that occur at mm-wave frequencies, suggest to reduce the spiral width close to the minimum value allowed by the technology. In addition, the maximum inductance of the transformer windings is regulated by the desired f_{SR}, thus limiting the number of turns. Furthermore, to maximize the magnetic coupling between adjacent metal spirals and, at the same time, to minimize the occupied area, the coil spacing is usually fixed to the closest value allowed be technology.

In a typical design, pattern-ground-shield (PGS) is exploited for both integrated inductors and transformers to reduce substrate losses due to displacement and eddy currents [29]. However, the shield is effective for the *Q*-factor improvement at low frequencies up to *K*-band [30], but it has a negative effect on the *Q* for small inductors working at the *W*-band. This is mainly due to induced losses in the PGS itself, which are so high to frustrate the substrate loss reduction [5]. Furthermore, avoiding the PGS

prevents detrimental resonating phenomena of the shield structure, mainly due to undesired inductive path toward the ground in circuit applications [31]. Finally, to avoid additional losses, conductive dummy fillers are not present below the transformers, but only at a safe distance, within a transition region around the windings, which is sufficiently high to guarantee homogeneity and planarity between metal levels.

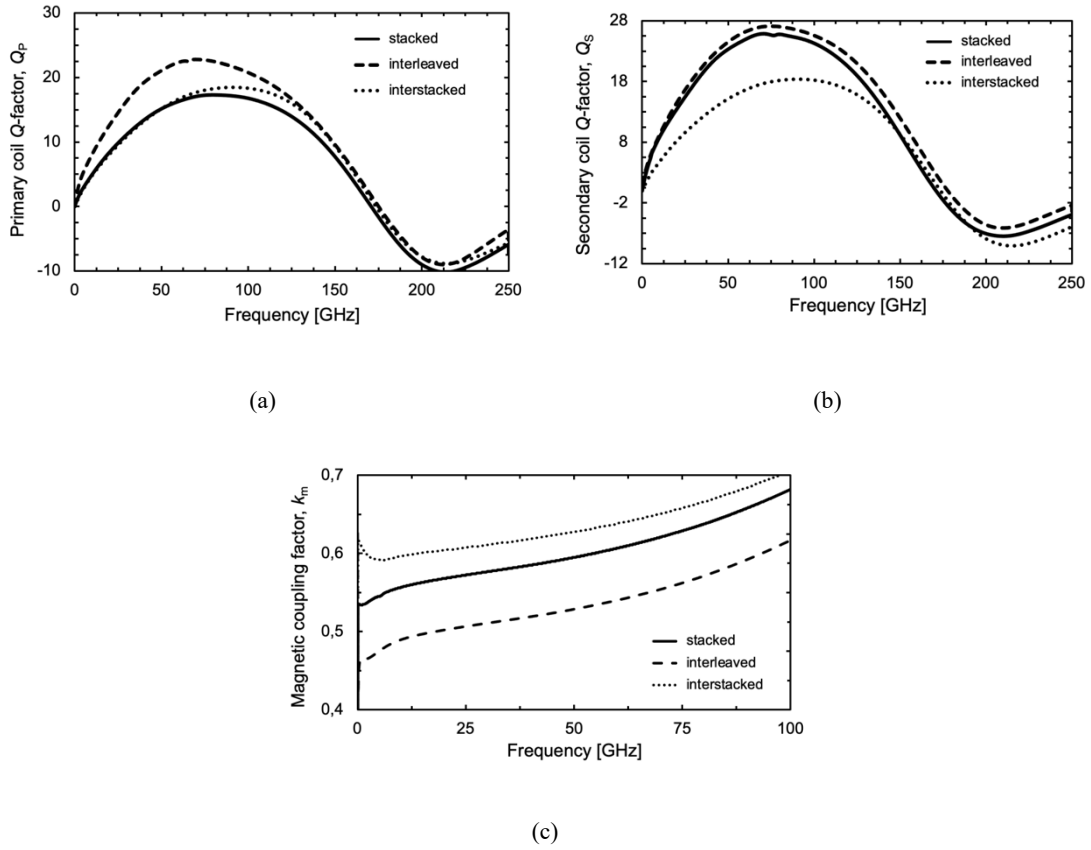
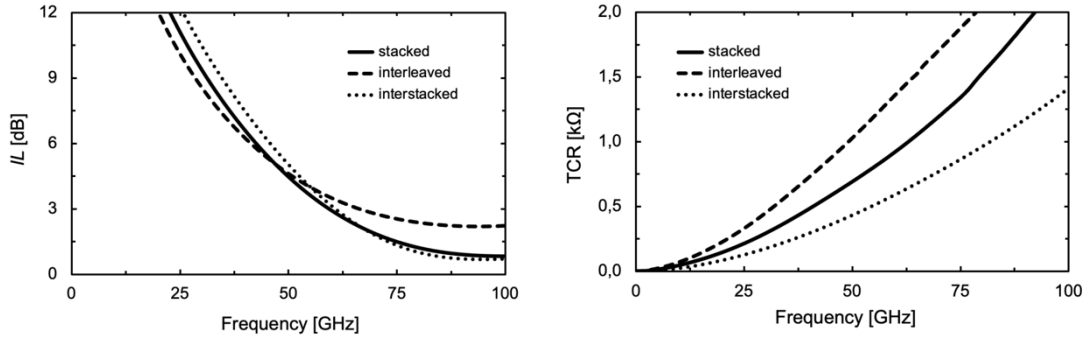


Figure 2.8. Q-factors, of (a) primary and (b) secondary coils, along with (c) k_m for stacked, interleaved, and interstacked transformers.

In Figure 2.8 (a), (b) and (c), the simulated Q-factor, of both primary and secondary windings and parameter k_m, for each of the designed transformers are shown. As apparent, all the designed structures exhibit an f_{SR} of about 170 GHz. The interleaved transformer guarantees the highest Q-factor at both primary and secondary coil, whereas the interstacked configuration allows maximizing the magnetic coupling with a k_m of about 0.68 at 77 GHz.



(a) (b)

Figure 2.9. Simulated performance of different transformer structures: (a) *IL* and (b) TCR.

Figure 2.9 (a) and (b), the *IL* and *TCR* are displayed for each transformer. The lowest *IL* at 77 GHz, around 1.2 dB, is achieved with the interstacked topology thus it is the best choice to implement function such as the single-ended-to-differential signal conversion. On the other hand, the interleaved transformer guarantees the maximum TCR (about 1.9 kΩ), thus resulting the best solution for resonant load of RF/mm-wave amplification stages.

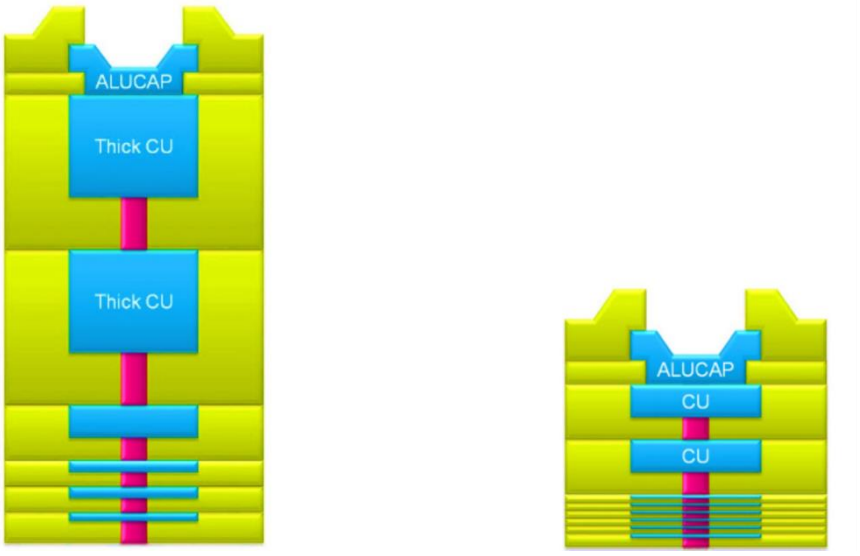
TABLE 2.1.
GEOMETRICAL AND ELECTRICAL PARAMETERS FOR DIFFERENT 77-GHZ TRANSFORMER CONFIGURATIONS.

	STACKED	INTERSTACKED	INTERLEAVED	UNITS
Metal width (*w*)	5.5	6.5	5.5	[μm]
Primary/secondary inner diameters	44	30	55/70	[μm]
Primary coil inductance	84	72	130	[pH]
Secondary coil inductance	96	72	110	[pH]
Primary coil *Q*-factor	17	18	23	-
Secondary coil *Q*-factor	26	18	27	-
Self-resonant frequency, f_{SR}	170	174	175	[GHz]
Magnetic coupling factor, k_m	0.63	0.68	0.56	-
Insertion loss, *IL* (in resonance mode)	1.4	1.2	2.5	[dB]
Transformer characteristic resistance, TCR	1.4	0.9	1.9	[kΩ]

Table 2.1 summarizes the geometrical and electrical parameters evaluated at 77 GHz of the designed transformers. As appears, the interstacked configuration is suitable when low *IL* and high k_m are required. The stacked transformer achieves performance very similar to the interstacked transformer with the advantage of a higher inductance at the same resonant frequency. Finally, an interleaved configuration can be used where a higher *TCR* is required.

2.4. A comparative analysis between standard and mm-wave-optimized BEOL in a nanoscale CMOS technology

In recent years, CMOS technologies have reached active device performance comparable to that provided by bipolar processes. Improvements in the transition frequency, f_T, and maximum oscillation frequency, f_{MAX}, for both MOS and bipolar transistors have been so remarkable that high-frequency IC performance is now mainly limited by the passive component losses. In this scenario, a key role is played by the back-end-of-line (BEOL) of the integration process. Traditionally, bipolar and BiCMOS technologies benefit from optimized BEOL for RF/mm-wave applications [32]-[35] with at least two thick copper top metals, along with thick intermetal oxide layers to reduce distributed ohmic losses and parasitic capacitance towards the substrate, respectively. Unfortunately, an optimized BEOL is not usually available in standard CMOS technologies, leading to lower quality passive components. Despite this limitation, modern scaled CMOS technologies have demonstrated promising results in comparison with traditional BiCMOS technologies [36]. In A comparison between BEOLs of mm-wave-optimized BiCMOS and standard 28-nm CMOS technologies is shown Figure 2.10.



(a) (b)

Figure 2.10. BEOL comparison between (a) mm-wave-optimized BiCMOS technology and (b) standard 28-nm CMOS technology BEOL.

The dilemma is still about the impact of the BEOL on the performance of mm-wave ICs and whether a technological investment can be justified by an effective performance improvement in actual applications. To this aim, an extensive comparison between two 28-nm CMOS technologies, i.e. one with a standard BEOL [28] and the other with a BEOL similar to a SiGe HBT BiCMOS technology [32], was carried out at two different levels. Initially, the performance of stand-alone integrated transformers designed with different BEOLs are compared, then the analysis is completed by designing a 77-GHz down-converter for FMCW radar applications [26], [27], as a macro-circuit testbench to emphasize the impact of passive component losses on the performance. Indeed, the 77-GHz down-converter is one of the most critical blocks of a mm-wave radar sensor, since it determines the receiver noise/linearity performance, while significantly contributing its gain. Furthermore, the adopted testbench allows a fair comparison between BEOL since both stacked and interleaved transformer configurations are used, thus providing an overall combined effect at the macroblock level.

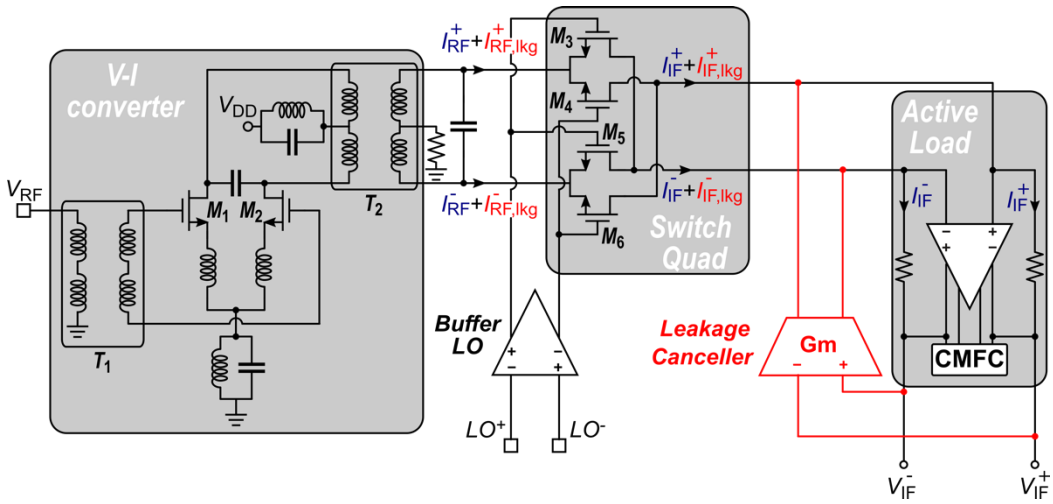


Figure 2.11. Simplified schematic of the 77 GHz down converted used for the BEOL comparison [37].

A simplified schematic of the 77-GHz down-converted used for the BEOL comparison is shown in Figure 2.11. It exploits a fully differential mixer-first architecture consisting of an input transformer, T_1, a voltage-to-current (*V-I*) converter, a passive mixer quad and a transresistance feedback amplifier. Transformer T_1 performs a single-ended-to-differential signal conversion, ESD protection and 50 Ω input matching. The *V-I* converter uses transformer T_2 as resonant load to perform a current buffer and achieve a better transconductance gain. It drives a double-balanced passive quad (i.e., the

switch quad), whose output signal current is delivered to the transresistance amplifier (i.e., the active load). More details and analysis about this 77-GHz down-converter can be founded in [37].

The down-converter design requires a careful optimization of both T_1 and T_2. Specifically, transformer T_1 mainly affects the down-converter *NF* and hence its *IL* must be minimized. On the other hand, transformer T_2 can impact the conversion gain if the parallel equivalent load resistance at the operating frequency is not high enough with respect to the mixer input resistance. Indeed, the higher is *TCR* the more efficiently the RF current is delivered to the passive mixer, thus preserving the conversion gain. Therefore, transformer T_1 and T_2 are designed with the aim of minimizing *IL* and maximize the *TCR*, respectively. To this end, extensive 2D EM simulations in ADS Momentum by Keysight Technology were carried out, which represent a consolidated design flow for RF and mm-wave ICs, as reported by several published works in the *K*- and *W*-bands [5]-[11], [31]-[37]. To obtain highly reliable results at mm-wave frequencies, the EM simulations required an accurate set-up. The latter was defined and experimentally validated by taking advantage of on-wafer S-parameter measurements for a reference stacked transformer, T_R, fabricated in the 28-nm FD-SOI CMOS technology. Figure 2.12 displays the micrograph of the ground-signal-ground (GSG) structure adopted for on-wafer measurements of T_R. It consists of two identical series-connected transformers T_R, which are put in resonance at 77 GHz by means of an integrated capacitance, C_R, which shunts the two parallel-connected spirals of the transformers This arrangement was exploited to properly draw a meaningful *IL* measurement of T_R, since in actual applications it is operated in a resonance condition.

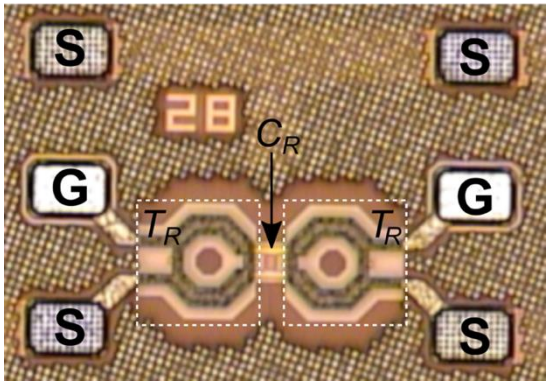


Figure 2.12. GSG structure for on wafer measurements of a stacked transformer in 28-nm FD-SOI CMOS.

The *IL* of the single transformer T_R can be easily extracted from the test structure. Indeed, if the return loss (i.e., $RL = -20\log S_{11}$) of the measured structure is sufficiently high, the *IL* of the single transformer can be obtained by halving the measured *IL* of the test structure, after de-embedding the GSG pad loss. The comparison between the estimated and measured *IL* of T_R is shown in Figure 2.13. An excellent agreement can be observed with an error of only 0.3 dB at 77 GHz, which is a very accurate result for such a small component. For the sake of completeness, the measured *RL* at 77 GHz is about 24 dB, which makes negligible the loss due to the impedance mismatch.

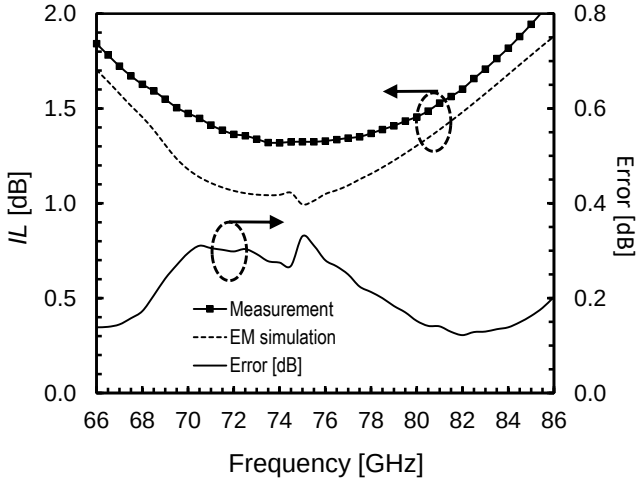


Figure 2.13. Simulated and measured *IL* of reference transformer T_R and corresponding error in dB.

The EM simulation set-up, properly thanks to the above detailed experimental validation, has been adopted to simulate the down-converter transformers, T_1 and T_2, for the BEOL comparison.

2.4.1. Transformers comparative analysis in standard and mm-wave-optimized BEOL

For comparison purpose, transformer T_1 and T_2 are implemented using standard configurations, i.e., stacked and interleaved, and they are geometrical sizing with the aim of optimizing the transformer performance, while guaranteeing the same f_{SR}. Indeed, the simple use of the same transformer geometry in different BEOLs could be not suitable for a fair comparative performance evaluation since the transformers would have different f_{SR} and hence different levels of optimization.

Table 2.2 reports the geometrical parameters of stacked transformer T_1, in standard and mm-wave-optimized CMOS BEOL, along with the main performance parameters compared at the operating frequency of the down converter (i.e., 77 GHz). For the sake of completeness, the BEOL comparison in terms of Q-factors, k_m and TCR was also carried out throughout the useful frequency range as illustrated in Figure 2.14.

TABLE 2.2.
GEOMETRICAL AND ELECTRICAL PARAMETERS FOR THE STACKED TRANSFORMER T_1 AT 77 GHZ.

	STANDARD CMOS BEOL	MM-WAVE-OPTIMIZED CMOS BEOL	UNITS
Primary/secondary coil width, *w*	5.5/5.5	5.5/5.5	[μm]
Primary/secondary inner diameter, d_{in}	44/44	60/60	[μm]
Primary/secondary coil inductance	84/96	119/130	[pH]
Primary/secondary coil *Q*-factor	25/17	27/21	-
Self-resonant frequency, f_{SR}	170	170	[GHz]
Magnetic coupling factor, k_m	0.63	0.62	-
Insertion loss, *IL* (in resonance mode)	1.3	1.2	[dB]
Transformer characteristic resistance, TCR	2.3	3.6	[kΩ]

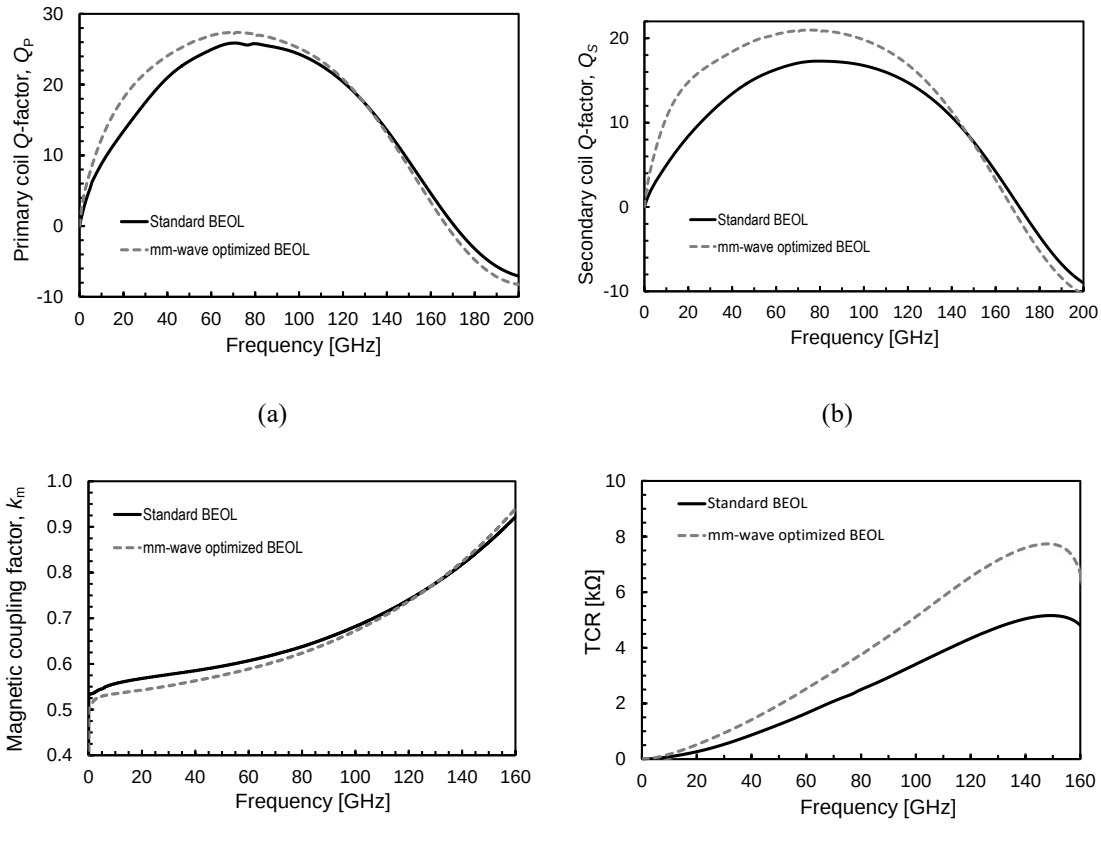


Figure 2.14. Comparison between parameters of stacked transformer T_1 in Table 2.2 for different BEOL. (a) Primary coil Q-factor, Q_P, (b) secondary coil Q-factor, Q_S (c) magnetic coupling factor, k_m, (d) transformer characteristic resistance, TCR.

The thicker oxide layers and consequent lower parasitic capacitances toward the substrate in the mm-wave optimized BEOL allows stacked geometry to benefit of a larger inner diameter and hence higher values of primary and secondary coil inductances. Moreover, thanks to thicker top Cu metal layers (2.5 μm instead of 1 μm) the *Q*-factor of both primary and secondary coils is improved at the cost of a small reduction of k_m, due to the thicker intermetal oxide between windings. In particular, the secondary coil highly benefits from the thick IA Cu layer since its *Q*-factor is improved in a wide frequency band, as shown in Figure 2.14 (b). The improvements of the *IL* and the *TCR* at 77 GHz are of 0.2 dB and 56%, respectively, as a direct consequence of higher inductance and *Q*-factor values and an almost constant magnetic coupling, as shown in Figure 2.14 (c).

The geometrical and performance parameters of interleaved transformer T_2 are summarized for both standard and mm-wave-optimized CMOS BEOL in Table 2.3, whereas Figure 2.15 shows the BEOL comparison in terms of *Q*-factor, k_m and *TCR* as a function of frequency. Looking at Table 2.3, it can be noted that, despite the mm-wave-optimized BEOL having thicker oxide layers between the transformer windings (i.e., AL and IB) and the substrate, identical geometrical dimensions (i.e., *w* and d_{IN}) lead to the same f_{SR} (i.e., 175 GHz). On the other hand, the winding inductance values are slightly lower, due to a higher value of the metal ratio thickness to width (t/w) according to the well-known effect analyzed in [38]. Moreover, there is a negligible increment in both primary and secondary winding *Q*-factors, as is also visible in Figure 2.15 (a) and (b). Consequently, the resulting *TCR* is about the same, as shown in Figure 2.15 (d), while the magnetic coupling coefficient, k_m, is slightly improved in the mm-wave-optimized BEOL transformer.

TABLE 2.3.
GEOMETRICAL AND ELECTRICAL PARAMETERS FOR THE INTERLEAVED TRANSFORMER T_2 AT 77 GHZ.

	STANDARD CMOS BEOL	MM-WAVE-OPTIMIZED CMOS BEOL	UNITS
Primary/secondary coil width, *w*	5.5/5.5	5.5/5.5	[μm]
Primary/secondary inner diameter, d_{in}	70/55	70/55	[μm]
Primary/secondary coil inductance	130/110	120/100	[pH]
Primary/secondary coil *Q*-factor	26/22.5	26.5/23	-
Self-resonant frequency, f_{SR}	175	175	[GHz]
Magnetic coupling factor, k_m	0.56	0.58	-
Insertion loss, *IL* (in resonance mode)	1.4	1.2	[dB]
Transformer characteristic resistance, TCR	3.4	3.3	[kΩ]

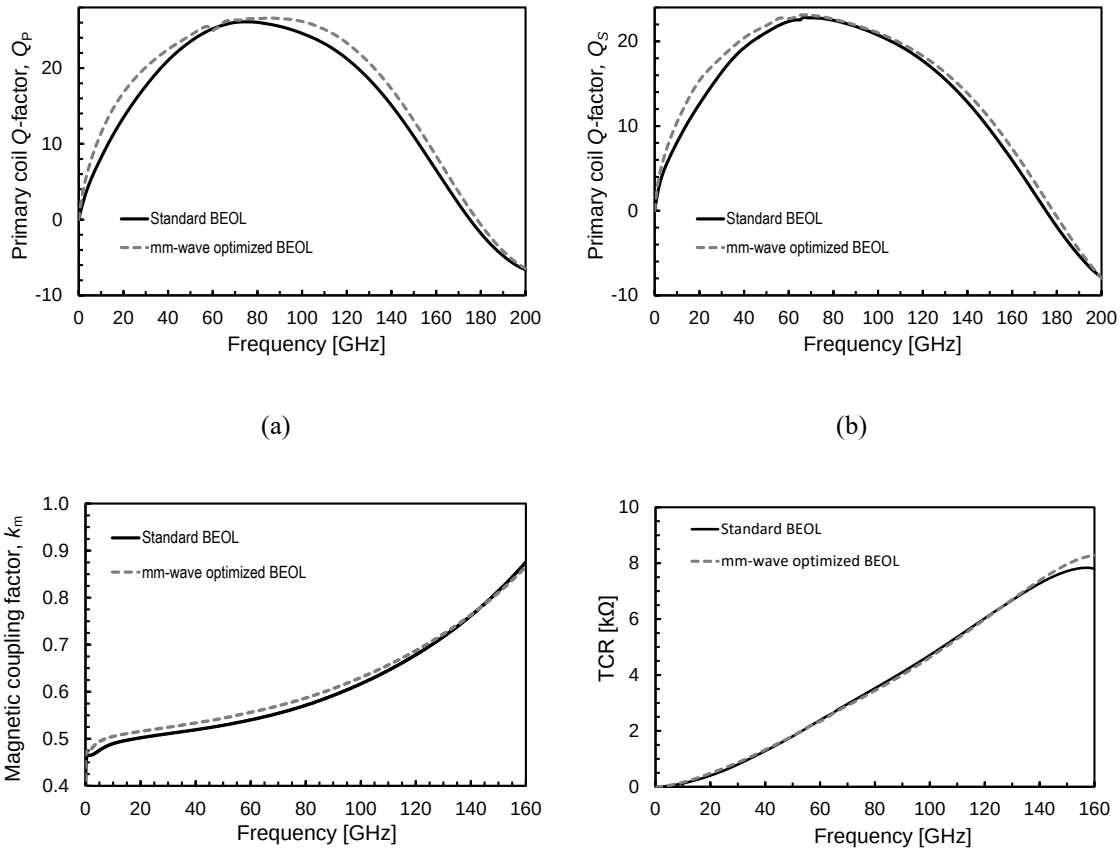


Figure 2.15. Comparison between parameters of interleaved transformer T_2 in Table 2.3 for different BEOLs. (a) Primary coil Q-factor, Q_P, (b) secondary coil Q-factor, Q_S (c) magnetic coupling factor, k_m, (d) transformer characteristic resistance, TCR.

The obtained results seem highly counterintuitive since significant improvements in terms of Q-factor and TCR would be expected in the best BEOL thanks to thicker metals and oxides. However, the issue should be seen under the correct perspective by starting from the above mentioned f_{SR} invariancy in the interleaved configuration.

To evaluate the parasitic capacitance in integrated components, the well-known equation for a parallel plate capacitance is usually considered:

$$C = \varepsilon \frac{W \cdot L}{D} = \frac{\varepsilon}{b} L \tag{2.12}$$

where ε, W, L and D are the dielectric permittivity, the width, the length, and the distance from the silicon substrate, respectively, with $b = D/W$ defined as capacitor aspect ratio. According to (2.12), an increased distance of the top metal from the substrate (as in the mm-wave optimized BEOL) should have produced a reduction in the

transformer capacitance with a consequent higher f_{SR}. On the contrary, an f_{SR} invariancy is found with the EM analysis, as shown in Table 2.3. This can be mainly ascribed to the very small size of the mm-wave transformers and hence to the non-negligible effect of the fringing electric field. Indeed, the capacitance of a parallel plate capacitor in (2.12) was formulated assuming that the separation between the electrode plates is very narrow and then the electric charge density on the plates is uniform, which allows the fringing fields of the edges to be neglected. Actually, a crucial role is played by the aspect ratio, b. Equation (2.12) works quite well only for $b < 0.03$ with an underestimation of about 10%, while for $b \approx 0.5$ it produces errors of about 100%[39], [40]. By introducing proper corrections to (2.12), transformer parasitic capacitances can be better evaluated for the interleaved structure previously analyzed, finding out that the thicker oxide in a mm-wave-optimized BEOL produces a reduction of the capacitance toward the substrate, while an increment of the fringing capacitance, which explains the observed f_{SR} invariancy. Therefore, this phenomenon tends to frustrate the benefits provided by the optimized BEOL for interleaved transformers, while better explaining the results on the stacked transformers, which highly benefit from the improved BEOL due to the lack of significant fringing capacitive effects (i.e., single-turn configuration is used).

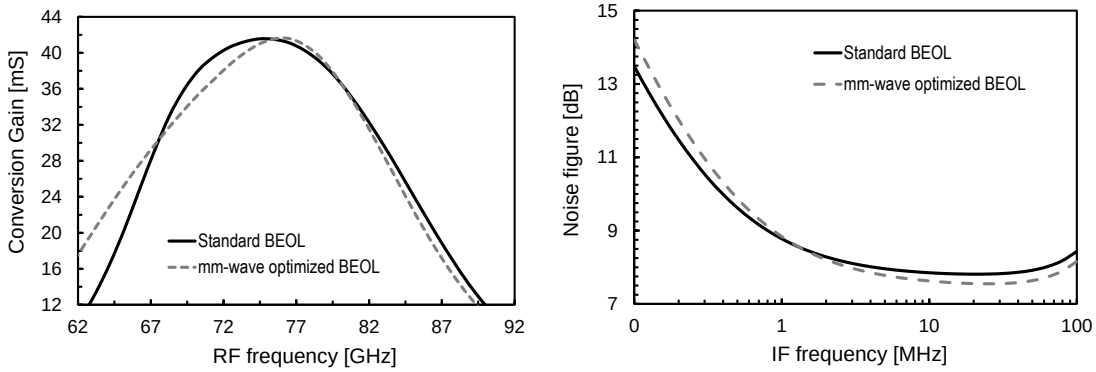
It is worth mentioning that all the above considerations are limited to the analyzed transformer values useful for mm-wave frequencies. On the other hand, an improved BEOL could have a very important impact for inductive components operated at lower frequencies, where higher inductances and hence larger coils are used, since the percentage effect of the fringing capacitances is greatly reduced.

2.4.2. 77-GHz down-converter: a test-case for standard and mm-wave-optimized BEOL comparison

Based on the transformer performance comparison, a macro-circuit analysis was carried out by exploiting the 77-GHz down-converter architecture for radar application shown in Figure 2.11 [26], [27], [31], [37], as a testbench. Specifically, the BEOL benefits were evaluated in terms of the main performance parameters, *NF,* and conversion gain. As mentioned before, transformers T_1 and T_2 exploit stacked and interleaved configurations, respectively, with the aim of minimizing the *IL* and maximizing the *TCR*, which directly affect the *NF* and conversion gain, respectively. The stacked transformer represents the best solution for the input balun implementation in both technologies, since

IL is the important parameter. On the other hand, standard and mm-wave-optimized BEOL provide the highest *TCR* with interleaved and stacked configurations, respectively. Nevertheless, to make a meaningful comparison in terms of down-converter performance, the interleaved structure was selected for the implementation of the inter-stage transformer, T_2. This choice is also supported by the very close *TCR* value (about 3 kΩ) achieved by standard BEOL interleaved and mm-wave-optimized BEOL stacked transformers (see Table 2.2 and 2.3).

The short-circuit transconductance conversion gain and the *NF* of the 77-GHz down-converter are reported in Figure 2.16 (a) and (b), respectively, for both technologies. As expected, the two BEOLs provide similar *NF* values (around 9 dB at 1 MHz), whereas the mm-wave-optimized process allows a slightly higher conversion gain at 77 GHz (40.9 mS against 40.3 mS) to be achieved. Table 2.4 compares the main performance of the down-converter in the two BEOLs. From these results, it appears that the advantages offered by the adoption of an optimized BEOL in terms of down-converter performance are almost irrelevant at mm-wave frequencies, as already anticipated by the stand-alone transformer comparison.



(a) (b)

Figure 2.16. Down converter performance: (a) short circuit transconductance conversion gain as function of the RF frequency; (b) NF as function of the IF frequency.

TABLE 2.4.
PERFORMANCE OF THE 28-NM CMOS DOWN CONVERTER IN THE TWO BEOLS.

	STANDARD CMOS BEOL	MM-WAVE-OPTIMIZED CMOS BEOL	UNITS
Voltage supply	1	1	[V]
Current consumption	15	15	[mA]
Conversion gain @ 77 GHz	40.3	40.9	[mS]
***NF* (evaluated for 1 MHz of IF Frequency)**	9	9	[dB]

In conclusion, despite thicker metals and intermetal oxide provide some advantages, especially with the stacked configuration, the potential improvements for the mm-wave transformers are highly reduced by EM fringing effects. Indeed, they are not negligible when the transformer size is comparable with the chip vertical dimensions, as happens at mm-wave frequencies. The evaluation on the adopted circuit testcase (i.e., 77 GHz down-converter) further confirms that very limited improvement can be achieved from an optimized BEOL technology. These results question the pros and cons of more expensive and complex BEOLs for nanometer CMOS platforms, providing a different perspective on technology developments for mm-wave applications.

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Chapter 3

Fundamentals of integrated VCOs

3.1. Introduction

In mm-wave transceivers, voltage-controlled oscillators (VCOs) are essential building blocks for frequency synthesis in both transmit and receive paths. They are embedded in a PLL to provide a stable reference signal used by the mixer to perform up- and down-conversion. However, modern applications pose severe requirements on the spectral purity of generated frequency. A very high spectral purity is required in mm-wave radar sensors to achieve a best target discrimination. In many instances, the VCO noise performance is the main limiting factor for the sensitivity of integrated receivers. In truth, random noise fluctuations in the output frequency, expressed in terms of jitter and phase noise (PN), have a direct impact on the overall transceiver (TRX) performance. The PN present in the oscillator output signal results in reciprocal mixing in the receive when a large interferer (also known as a blocker) is received together with the desired signal. Indeed, the oscillator PN is mixed with the blocker in the down-conversion mixer and then appears superimposed to the desired signal, thus degrading the receiver signal-to-noise ratio and hence sensitivity [1]. In the transmit path, the oscillator PN is amplified and desensitizes a nearby receiver while increasing the noise floor.

Driven by the demand for even higher spectral purity, several efforts have been carried out to understand and model the PN for an optimize oscillator design. The phenomenon of PN generation in VCOs has been the main focus of important research efforts. Through

the years, the resulting knowledge about the conversion mechanisms of circuit noise voltage and current sources into phase noise has allowed effective VCO design techniques and circuit solutions to be developed. The ability to achieve optimum PN performance is usually paramount in most VCO designs and the improvement of PN is also mandatory for the efficient use of the frequency spectrum.

To this purpose, this chapter deals with the fundamental concepts about the mm-wave VCO design, starting from a review of most meaningful theories on phase noise model, which are reported in Section 3.2. The derived theoretical procedure has directly impacted the oscillator design leading to several topologies as well as in frequency synthesizer architectures and phase noise optimization techniques, which are discussed in the overviews provided in Section 3.3, Section 3.4, and Section 3.5, respectively. Finally, many considerations carried out in this chapter are used to provide a VCO design example for *W*-band automotive radar application, which will be discussed in Section 3.6.

3.2. Review of oscillator phase noise models

Since the primary function of an oscillator is to generate a periodic signal, ideally its output should be a perfect sinusoidal signal of the form $v(t) = A_0 \cos(\omega_0 t + \phi_0)$, where A_0, ω_0 and ϕ_0 are the oscillator amplitude, angular frequency and initial phase, respectively. These parameters are constant over the time. In the frequency domain, this means that the oscillator output power is concentrated in a single tone that can be represented as a Dirac Delta function at ω_0. However, in any practical oscillator, the unavoidable presence of noise sources in the circuit induces random fluctuations, which modulate amplitude and phase, thus making them time-dependent. For a sake of simplicity, it is possible to divide the modulation between amplitude and frequency/phase.

If only a single-tone amplitude modulation is considered, the oscillator output voltage can be written:

$$v(t) = A_0 \left[1 + m \cdot \cos(\omega_m t)\right] \cos(\omega_0 t + \phi_0) \tag{3.1}$$

where $m \ll 1$ and $\omega_m \ll \omega_0$. The resulting output spectrum now consist of a Delta Dirac function at ω_0 along with a couple of side-tones at angular frequencies $\omega_0 \pm \omega_m$. Therefore, the output voltage can be rewritten as:

$$v(t) = A_0 \sin(\omega_0 t) + \frac{mA_0}{2}\cos[(\omega_0 - \omega_m)t] - \frac{mA_0}{2}\cos[(\omega_0 + \omega_m)t] \quad (3.2)$$

where $\frac{mA_0}{2}\cos[(\omega_0 - \omega_m)t]$ and $\frac{mA_0}{2}\cos[(\omega_0 + \omega_m)t]$ are the lower- and the upper-side band.

On the other hands, when only a single-tone frequency modulation is considered, the modulated frequency can be expressed as $\omega(t) = \omega_0 + \omega_m(t)$, and hence, since the phase is the integral of the frequency, the resulting output signal become:

$$v(t) = A_0 \cos\left[\omega_0 t + \phi_0 + \frac{\Delta\omega_0}{\omega_m}\sin(\omega_m t)\right] \quad (3.3)$$

A corresponding phase modulation also arises in this case, with $m = (\Delta\omega_0/\omega_m)$ as modulation index, and the resulting phase is equal to $\phi(t) = \Delta\phi \cdot \sin(\omega_m t)$, where $\Delta\phi = \Delta\omega_0/\omega_m$. If a small-angle modulation is considered, i.e., $\Delta\phi \ll 1$ (the so-called *narrow band frequency modulation*), the expression of the output signal can be approximated as:

$$\begin{aligned} v(t) &\cong A_0 \cos(\omega_0 t + \phi_0) - A_0 \sin(\omega_0 t + \phi_0) \cdot \frac{\Delta\omega_0}{\omega_m}\sin(\omega_m t) \\ &= A_0 \cos(\omega_0 t + \phi_0) - \frac{A_0}{2} \cdot \frac{\Delta\omega_0}{\omega_m}\cos[(\omega_0 - \omega_m)t] \\ &+ \frac{A_0}{2} \cdot \frac{\Delta\omega_0}{\omega_m}\cos[(\omega_0 + \omega_m)t] \end{aligned} \quad (3.4)$$

The spectrum of the modulated output signal is depicted in Figure 3.1 (a). The ratio between the power of each side-tone and the power of carrier is known as *Spurious-Free Dynamic Range* (SFDR). It is interesting to note that the SFDR, which is usually expressed in dBc, i.e., dB with respect to the carrier, is equal to half the phase noise power spectral density, S_ϕ, which is shown in Figure 3.1 (b). Since S_ϕ is inversely proportional to the square of the frequency offset, ω_m, a $1/\omega_m^2$ or $1/\omega_m^3$ dependence arises in presence of white or flicker noise, respectively.

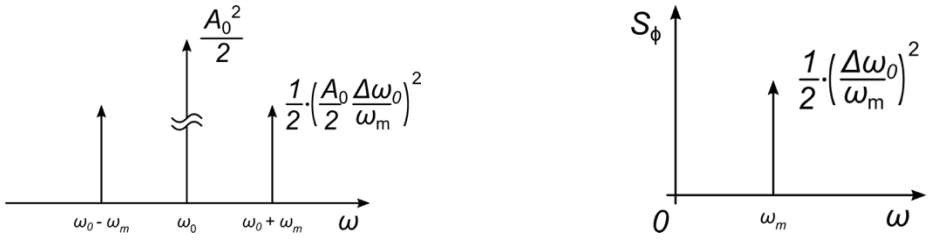


Figure 3.1. Spectrum of the (a) modulated output voltage $v(t)$ and (b) of the modulated phase $\Delta\phi$.

The power spectral density of the output voltage at $\omega_0 \pm \omega_m$ is given by $S_V(\omega_0 \pm \omega_m) \cong \frac{S_\phi(\omega_m)}{2} \cdot \frac{A_0^2}{2}$. The noise level is now expressed by the ratio between the noise power in a 1-Hz bandwidth at offset ω_m and the power of the carrier. This figure quantifying the amount of phase noise is defined single-sideband-to-carrier ratio (SSCR) and it is usually denoted with $\mathcal{L}(\omega_m)$:

$$\mathcal{L}(\omega_m) = \frac{S_V(\omega_0 \pm \omega_m)}{A_0^2/2} \cong \frac{S_\phi(\omega_m)}{2} \tag{3.5}$$

It worth highlighting that, while the power spectrum of the phase, S_ϕ, diverges to ∞ at zero offset frequency, the power spectrum of the output voltage, S_V, does not. This a consequence of the small-angle approximation, which is no longer valid as ω_m approaches zero. As a results, if only the white noise is considered, the voltage spectrum tapers off with a Lorentzian shape and has not singularities when the offset frequency approach *0*, while preserving the same asymptotic behavior.

3.2.1. Leeson's model

The most popular phase noise model is described by Leeson's equation, introduced in the 1966 [2]. It is important to note that this model was developed uses a linear time-invariant (LTI) approach, and it assumes the tuned circuit filters out all the harmonics. Assuming the PN as a small perturbation, Leeson linearizes the oscillator around the steady-state point to obtain a closed-form equation for PN. For a tuned tank oscillator, the PN at an offset frequency $\Delta\omega$ from a carrier at ω_0 is given by:

$$\mathcal{L}(\Delta\omega) = 10 \cdot \log\left\{\frac{2FkT}{P_s} \cdot \left[1 + \left(\frac{\omega_0}{2Q_T\Delta\omega}\right)^2\right] \cdot \left(1 + \frac{\Delta\omega_{1/f^3}}{\Delta\omega}\right)\right\} \tag{3.6}$$

where F is an empirical parameter called noise excess factor of the active device, k is the Boltzmann's constant, T is the absolute temperature, P_S is the average power dissipated in the resistive part of the tank, which is roughly related to the oscillation amplitude as $P_S \sim V_{osc}^2$, Q_T is the effective quality factor of the tank, and $\Delta\omega_{1/f^3}$ is the flicker noise corner frequency.

As illustrated in Figure 3.2, which graphically shown the Leeson's equation as a function of the offset frequency $\Delta\omega$, the PN profile pass through different slope regions.

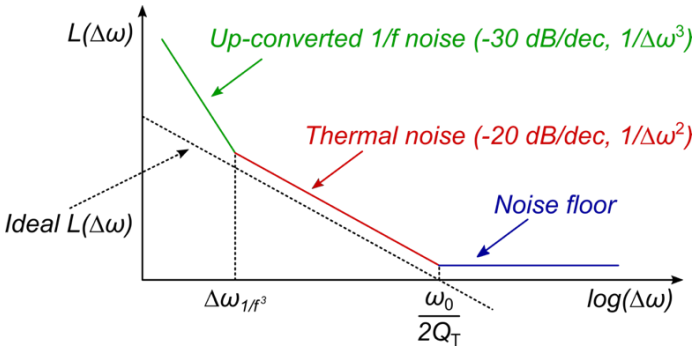


Figure 3.2. Graphical representation of the PN spectrum in the Leeson model.

The region near the carrier is called close-in phase noise or flicker $(1/f)$ phase noise region and exhibits a slope of $1/\Delta\omega^3$, i.e. −30 dB per decade. This region of frequency offset is dominated by the flicker noise up-conversion. Above that, the slope become −20 dB per decade, i.e. $1/\Delta\omega^2$. This region is generally referred to as white or thermal phase noise region because it is caused by thermal noise upconverted in the period of oscillation. Finally, at higher offset frequency from the carrier, the spectrum become flat, limited by the noise floor of the active devices, which is given by kTF/P_s.

Despite its simplicity, Leeson's equation provides useful indications about the impact of design parameters, such as Q_T and P_S, on phase noise. However, the predictive power of the Leeson model is limited by the use of two fitting parameters, F and $\Delta\omega_{1/f^3}$, which give the dependence of phase noise on the active devices and usually derived by a posteriori fitting of experimental data. Therefore, Leeson's formulation cannot provide quantitative prediction of phase noise and can be considered just as behavioral model.

3.2.2. Lee and Hajimiri's model

To overcome the limitations of the Leeson's formula, Lee and Hajimiri proposed a linear time variant model (LTV) to predict the noise proprieties of an oscillator [3], [4]. The PN analysis given in the Lee and Hajimiri's noise model characterizes the oscillator by means of two impulse responses, namely $h_{A_0}(t,\tau)$ and $h_{\phi}(t,\tau)$, which link each noise source with the resulting amplitude and phase perturbations, as a function of the injecting time instant. Indeed, if a current impulse is injected at the peak of the oscillator waveform, as illustrated in Figure 3.4 (a), the oscillation amplitude will be disturbed but no phase perturbation occurs and hence $h_{\phi}(t,\tau) = 0$. Conversely, if the injection happens at the zero crossing, the maximum phase perturbation occurs, while the oscillation amplitude remains unchanged, as depicted in Figure 3.4 (b). Therefore, if a current impulse is injected between the zero crossing and the peak of the oscillation waveform, both amplitude and phase perturbation arise. However, the impulse response associated to amplitude perturbations, $h_{A_0}(t,\tau)$, is usually of little interest since it is progressively attenuated by the transconductor nonlinearity. On the contrary, the phase perturbation is permanent, thus making the associated impulse response of greater interest.

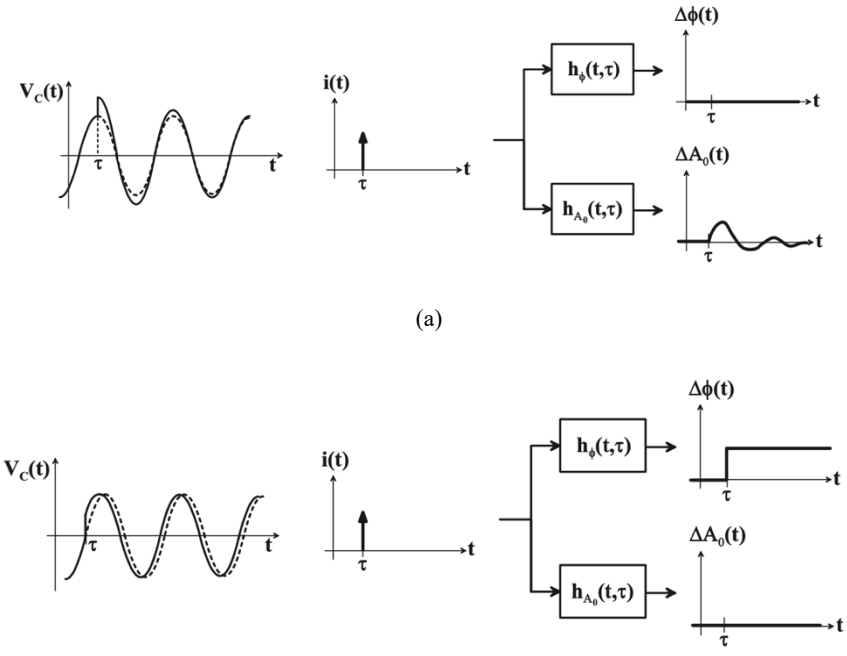


Figure 3.3. Impulse response of phase, $h_{\phi}(t,\tau)$, and amplitude, $h_{A_0}(t,\tau)$, for an impulse current injected (a) at the peak of the oscillator waveform and (b) at the zero crossing.

Since an impulsive input current produces a step change in phase, the impulse response can be expressed as:

$$h_{\phi}(t,\tau) = \frac{\Gamma(\omega_0\tau)}{q_{max}} u(t-\tau) \tag{3.7}$$

where $\Gamma(\omega_0\tau)$ is a dimensionless and periodic function, called impulse sensitivity function (ISF), which takes into account the periodic dependence of the induced phase shift on the charge injection time τ, and $u(t-\tau)$ is the unit step function. Since, the ISF is a periodic function, it can be expressed in Fourier series as:

$$\Gamma(\omega_0\tau) = \frac{c_0}{2} + \sum_{n=1}^{\infty} c_n \cos(n\omega_0 t + \theta_n) \tag{3.8}$$

where c_n are the Fourier series coefficients and θ_n is the phase of the n^{th} harmonic. The resulting phase shift, $\Delta\phi_n(t)$, due to a generic current noise source, $i_n(\tau)$, is than evaluated by the superposition integral as:

$$\Delta\phi_n(t) = \frac{1}{q_{max}}\left[\frac{c_0}{2}\int_{-\infty}^{t} i_n(\tau)d\tau + \sum_{n=1}^{\infty} c_n \int_{-\infty}^{t} i_n(\tau)\cos(n\omega_0 t + \theta_n)\, d\tau\right] \tag{3.9}$$

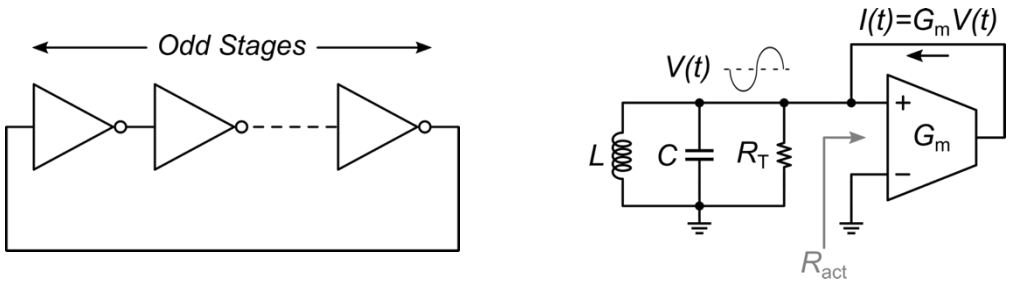
Eq. (3.9) inherently implies the up/down-conversion of out of band noise, since noise components at $n\omega_0 \pm \Delta\omega$ will be folded at $\Delta\omega$ by multiplication with the ISF coefficients at $n\omega_0$, thus providing some insights that Leeson's model lacks. In addition, the low-frequency flicker noise components are up-converted into close-in PN by multiplication with coefficient c_0, which can be minimized by symmetrizing the rising and falling edges of the oscillator waveform.The same results can be achieved in the frequency domain by using the alternative phasor-based analysis proposed in [5] and then further developed in a more general way in [6].

One of the limitations of the ISF theory is that it is not able to predict the Lorentzian shape of the oscillator voltage spectrum, which establishes the power at the oscillation frequency to be finite. Consequently, the Hajimiri-Lee's model fails when a sinusoidal perturbation is injected whose frequency is close enough to the oscillation frequency and hence, it is unable to capture phenomena like injection-locking [7]. To address the LTV model limitations, Demir and Kartner proposed a nonlinear time variant (NLTV) approach to predict the oscillator PN by means of a complex mathematical description,

featuring Floquet theory and stochastic differential equations [8], [9]. Although this model correctly predicts the Lorentzian shape of the output spectrum, it provides a pure statistical characterization of the oscillator which does not deliver the circuit designer a physical insight into the phase noise generation mechanism, and hence its results are not straightforward to use in a practical design.

3.3. Different oscillation topologies

To generate a periodic output signal, a self-sustained mechanism, ascribed to a positive feedback system, is typically exploits in oscillating circuits. To sustain a stable oscillation, the positive feedback system is designed to fulfill the well-known Barkhausen's criteria for oscillation. This means that the phase shift around the feedback loop must be 0° or an even multiple of 360° at some frequency and that the magnitude of the loop gain at that frequency be unity. Since the self-sustain oscillation is usually generated by switching circuits with self-limited gain mechanisms, a simple oscillator can be composed by a series connection of inverters, (odd device number is required) as depicted in Figure 3.4 (a).



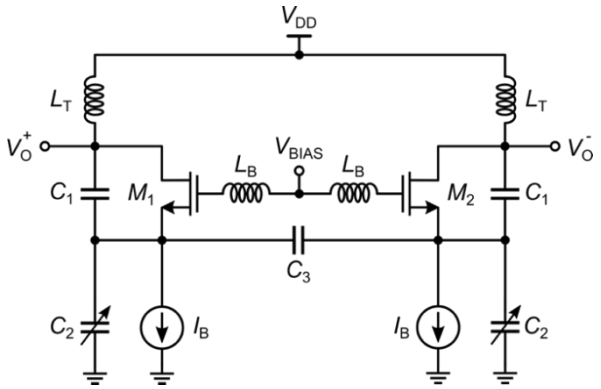
(a) (b)

Figure 3.4. Schematic representation of (a) a ring oscillator and (b) LC oscillator.

This circuit, commonly known as *ring oscillator*, provides an oscillation frequency inversely proportional to the total delay generated by the inverters. The lack of integrated inductors allows a very compact chip area and wide tunable frequency range to be achieved, which are the main advantages of this oscillator [10]. However, ring oscillators suffer from a very poor phase noise (PN) performance compared with the LC oscillator counterpart and hence they are not suitable in frequency synthesizers for modern mm-wave applications.

A typical LC-oscillator, schematically representant in Figure 3.4 (b), consists in the parallel connection of an LC resonator, also known as LC-tank, which sets the oscillation frequency and an active stage, i.e. a transconductor, which provides the non-linear negative conductance to balance the tank losses and provides the oscillation stability.

Especially at mm-wave frequencies, integrated oscillators are often implemented in a differentially topology, due to their higher immunity to common-mode (CM) spurious signals compared to the single-ended counterparts. In CMOS technology, differential cross-coupling and Colpitts oscillator are the most popular topologies. The Colpitts oscillator represents one of the most traditional solutions for LC-oscillator, which is one of the main implementations of the so-called three-point topologies, along with Clapp and Hartley oscillator [11]. A CMOS implementation of a differential Colpitts oscillator is reported in Figure 3.5. In such a circuit, the negative feedback provided by capacitors C_1 and C_2 leads to a negative resistance that varies with frequency and is equal to $-g_m/[(2\pi f_0)^2 C_1 C_2]$. Therefore, the oscillation arises when the negative resistance equals the inductor series loss resistance, $R_S \approx \omega_0 L/Q_L$. Consequently, the expression of both oscillation frequency and start-up condition can be derived as reported in Figure 3.5.



$$f_0 = 1\Big/2\pi\sqrt{L_T\frac{C_1C_2}{C_1+C_2}}$$

$$g_m Q_L^2 R_S \geq \frac{(C_1+C_2)^2}{C_1C_2}$$

Figure 3.5. Simplified schematic of a Colpitts oscillator along with the expression for both oscillation frequency and start up condition.

It is interesting to note that, by changing capacities C_1 and C_2, several optimization levels for both PN and power consumption can be achieved. However, the Colpitts topology requires a higher current consumption, or alternative a higher tank Q-factor, to achieve a robust start-up condition as that provided by the cross-coupled oscillators. The more robust start-up condition is one of the reasons that cross-coupled oscillators are actually preferred over the more tradition three-point ones. In addition, differential

Colpitts and cross-coupled oscillator are able to provide an excellent PN performance, but the cross-coupled topology allows a better oscillator Figure-of-Merit (FoM) [12], defined as:

$$\text{FoM} = \mathcal{L}(\Delta\omega) + 10\log(P_{DC}/1mW) - 20\log(\omega_0/\Delta\omega) \tag{3.10}$$

where $\mathcal{L}(\Delta\omega)$ is the PN at the offset frequency, $\Delta\omega$, and P_{DC} is the DC power consumption. Based on (3.10), a better oscillator FoM can be achieved by reducing the PN without impairing the power consumption or, in alternative prospective, by lowering the power consumption keeping the PN constant. To this purpose, a key role it is played by the VCO power efficiency, η_P, which relates P_{DC} with the power dissipated into the tank, P_{RF}. According to [13] and [14], this relationship can be expressed in terms of voltage and current efficiencies, η_V and η_I, as:

$$P_{RF} = \eta_P \cdot P_{DC} = \left(\frac{I_{\omega_0}}{I_{DC}} \cdot \frac{V_{osc}}{V_{DC}}\right) \cdot P_{DC} = (\eta_V \cdot \eta_I) \cdot P_{DC} \tag{3.11}$$

where I_{ω_0} and V_{osc} are the oscillation current and voltage components in the tank, whereas I_{DC} and V_{DC} are the supply current and voltage, respectively. The oscillator power consumption can be reduced by improving both η_V and η_I. This concept, along with the theoretical advances derived from the ISF theory, have had a direct impact on the oscillator design, especially for the cross-coupled oscillators. As a results, many alternative topologies aimed at improving PN as well as the oscillator FoM are currently available in literature, thus making the cross-coupled oscillators the dominant solution for most mm-wave applications. In the following, main topologies based on the cross-coupled oscillator will be briefly introduced by highlighting the advantages and drawbacks.

3.3.1. Class-B oscillator

The traditional class-B cross-coupled oscillator is depicted in Figure 3.6 (a). Since the current is alternative steered into the two transistors for half of the oscillation period, the idealized drain current exhibits an almost square waveform, as illustrated in Figure 3.6 (b), with a fundamental harmonic component, I_{ω_0}, equal to $(2/\pi)I_B$. The class-B oscillator show the best achievable performance by increasing the bias current I_{B}

until an oscillation amplitude equal to V_{DD} is achieved, resulting in η_V=1 with $\eta_I = 2/\pi$. This usually happen when I_B is chosen at the border between the so-called *voltage-* and *current-limited* operation regions, whereas a further increase in the bias current beyond this point would result only in higher power dissipation without any significant benefit [15].

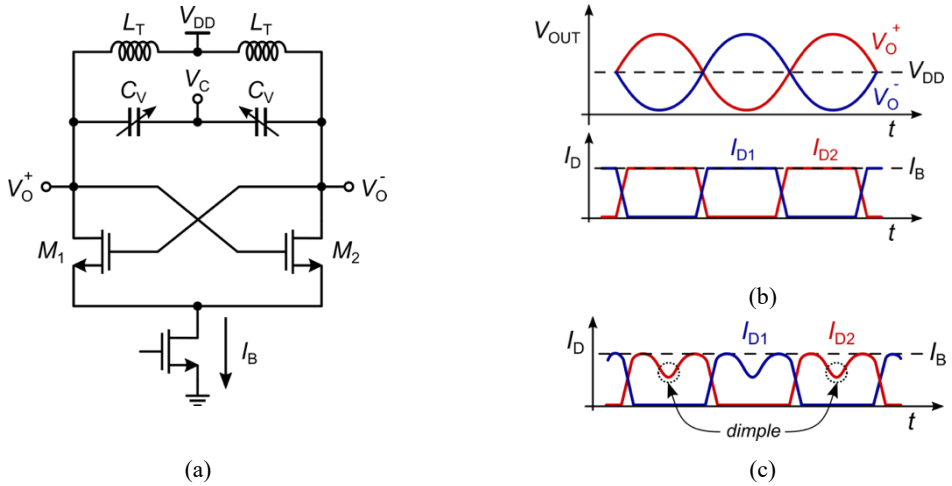
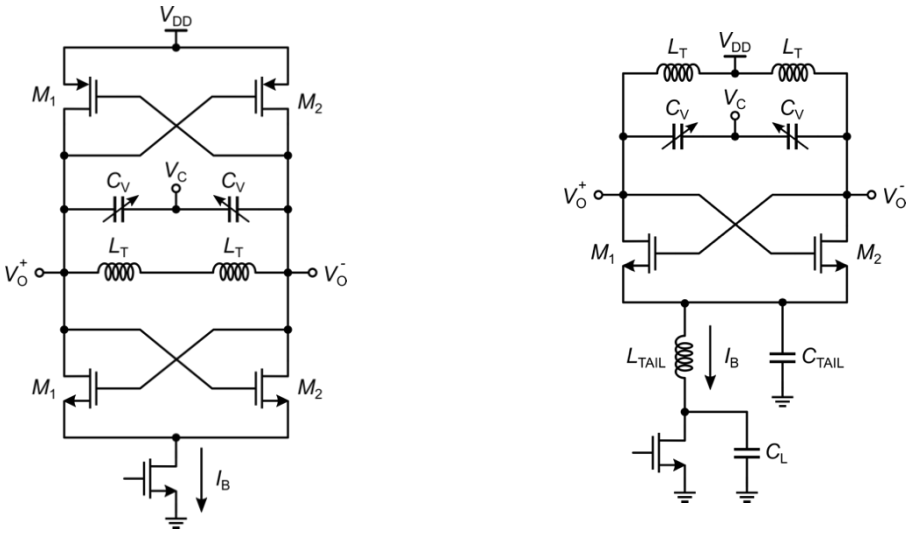


Figure 3.6. (a) Simplified schematic of a typical class-B oscillator along with (b) the ideal voltage and current waveforms and (c) the ideal drain current waveform.

The performance of the class-B oscillator is limited by both the noise and the additional voltage drop coming from the bias current source. By increasing the size of the current source, η_V can be improved, but at the cost of a higher noise contribution. Moreover, η_I also drops when the switching transistor M_1 and M_2 are in the triode region, due to the parasitic capacitance at the common source node. Since this parasitic capacitance tends to maintain a constant common source voltage, the drain current experiences a dimple that reduces the current efficiency, as sketched in Figure 3.6 (c). In addition, a low impedance path between the output tank and ground is provided by these capacitances when M_1 and M_2 are in triode region, which degrades the tank Q-factor and hence PN. Several solutions have been proposed in literature to improve the class-B oscillator PN or to relax the inherent trade-off between PN and power consumption. A complementary class-B oscillator, whose schematic is shown in Figure 3.7 (a), can be exploited to improve the current efficiency (i.e., reducing current consumption) while preserving the oscillator start-up, thanks to the larger small-signal loop gain with respect to the conventional NMOS-only implementation [15], [16]. Moreover, assuming operation in the *current-limited* region, all the current I_B flows differentially in the tank,

with some benefit for the oscillation amplitude despite a lower bias current. Unfortunately, the maximum achievable voltage swing is reduced (i.e., lower voltage efficiency) and the noise contribution of transistors increased, thus leading to a lower PN performance with respect to the NMOS implementation. Therefore, the complementary class-B oscillator is useful when a low consumption is the main target and PN requirement is relaxed.



(a) (b)

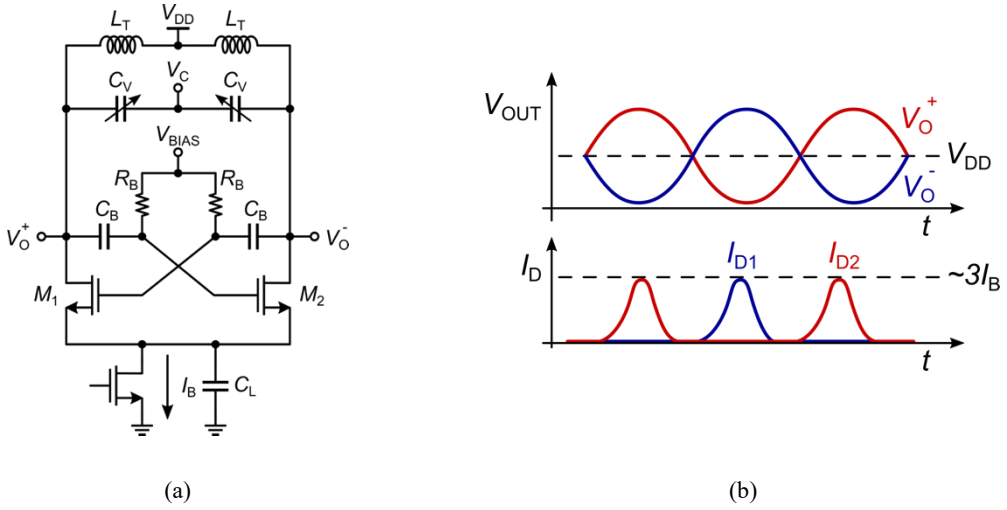
Figure 3.7. Schematics of (a) complementary class-B oscillator and (b) class-B oscillator with tail filter.

The performance of the NMOS class-B oscillator can be considerably improved using the LC-tail filter [17], as illustrated in Figure 3.7 (b). In this implementation, an inductance L_{TAIL} is introduced to resonate with the tail capacitance C_{TAIL}, thus performing a high impedance tuned at twice of the oscillation frequency to prevent the active devices to load the tank. Furthermore, a large capacitance C_L, placed in parallel with the tail current source, shorts to ground the tail transistor noise around the second harmonic of the oscillation frequency. Since the parasitic drain capacitance is absorbed in the capacitance, C_L, the current source transistor area can be increased to reduce its flicker noise contribution. Additionally, the capacitance C_L ac-grounds the tail inductance L_{TAIL}, allowing the maximum oscillation amplitude to be increased above $2V_{DD}$ thus overcoming the limitation of the traditional class-B oscillator and improving the voltage efficiency [13]. This is a very popular technique for low phase noise design and can be arranged in various ways [18]. However, a practical limit of the class-B oscillator with tail filter is related to the large voltage swing that the transistor pair experiences, which

can lead to reliability issues. Moreover, the tail filter technique, requires an additional resonator, which results in an increased design complexity, area and hence cost. In addition, the CM impedance of the tank at the second harmonic of the oscillation frequency can reduce the effectiveness of the tail filter since it changes its resonant frequency. Seeking to mitigate these issues, the CM resonance of the tank can be tuned at the 2nd harmonic of the oscillation frequency, while the fundamental is provided by the differential-mode (DM) resonance exploiting a transformer-based tank as reported in [19] and [20].

3.3.2. Class-C oscillator

An alternative and, from a certain point of view, dual approach to the tail-filter technique, consists of improving η_I by forcing a class-C operation through the configuration shown in Figure 3.8 (a), known as class-C oscillator [21], [22].



(a) (b)

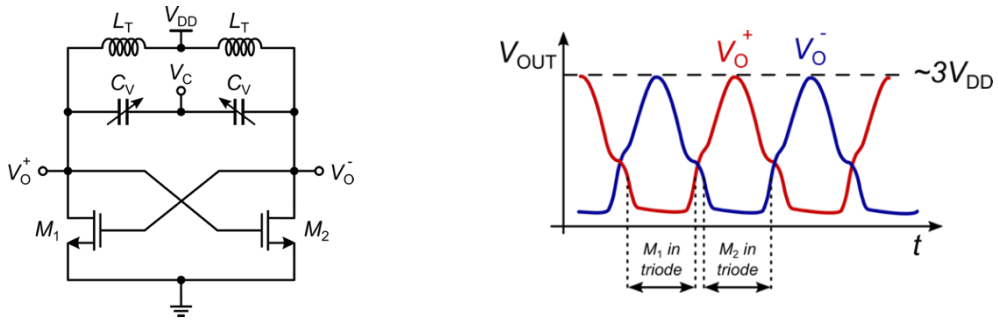
Figure 3.8. (a) Schematic of a typical class-C oscillator along with (b) the ideal voltage and current waveforms.

Thanks to the ac-coupled at the gate of the cross-coupled pair, transistors can be biased to work in the saturation region providing a high impedance during the entire oscillation period, thus preserving the tank Q-factor. For a class-C operation, the bias voltage, V_{BIAS}, is set quite low, typically around $V_{DD}/3$, and transistors are both off when the outputs are balanced. In such a condition, a large tail capacitance, C_T, shunting the current source, causes the drain current waveforms are no longer square waves, but rather tall and narrow pulses delivered at the peak of the voltage swing, as shown in Figure 3.8 (b). In this way a drastically reduction of the conduction angle arises along with an increased current

efficiency. However, if the oscillation amplitude is large enough to push transistors M_1 and M_2 into the triode region, the tank Q-factor greatly drops, due to the low-impedance path provided by C_T. Consequently, the drain current will no longer feature tall and narrow pulses and current efficiency decrease accordingly. This constrain limits the maximum oscillation amplitude around $V_{DD}/2$, when a V_{BIAS} as low as a transistor threshold voltage is adopted. Although the PN and the power efficiency are improved for low oscillation amplitudes, compared to a class-B oscillator at the same oscillation amplitude, the voltage swing constrains limits the PN performance in the class-C oscillator. In addition, this oscillator also suffers from a serious trade-off between start-up requirement and oscillation amplitude, which could further reduce the potential advantages with respect to a class-B [14]. Indeed, a high V_{BIAS} is required for the oscillation start-up, which conflicts with the class-C operation. To improve this trade-off, some solutions have been proposed in literature such as the hybrid class-B/class-C architecture reported in [23] and [24] as well as the dynamically biased class-C oscillator discussed in [14].

3.3.3. Class-D oscillator

A higher oscillation amplitude can be achieved by exploiting the class-D oscillator [25] depicted in Figure 3.9 (a).



(a) (b)

Figure 3.9. (a) Simplified schematic of a class-D oscillator along with (b) its voltage waveform.

Starting from the traditional class-B oscillator, class-D operation can be achieved by removing the tail current source and sizing a transistor aspect ratio large enough to become almost ideal switch. This allows maximizing the oscillation voltage amplitude, which can reach about three times V_{DD}, thus improving power efficiency beyond 90%. Consequently, switching transistors M_1 and M_2 are pushed deep into the triode region

(even more than in the class-B oscillator) and hence they generate considerable amount of noise. Nevertheless, the oscillation voltages at the drain nodes are forced to ground for almost half the oscillation period, when M_1 and M_2 are in the triode region, as sketched in Figure 3.9 (b). Thanks to that, most of the transistor noise is prevented to be up-converted in PN.

The high oscillation amplitude, the reduced supply voltage and the excellent switches provided by nanoscale CMOS technologies, well explain the interest about this oscillator topology [26]. However, class-D oscillator must be used with a very low supply voltage to preserve transistors from breakdown and reliability issue, given the need for thin-oxide devices to guarantee nearly ideal switching. The oscillation amplitude is manly set by the supply voltage, while the current consumption is imposed by the tank losses. In addition, the absence of a bias current source gives high sensitivity to the supply voltage variations. The use of an on-chip LDO attempts to mitigate this issue [27], but it leads higher power consumption.

3.3.4. Class-F oscillator

Another interesting approach to improve the oscillator performance is by acting on the resonator with the aim of increasing the slope of the oscillation voltage making it an almost square waveform. In such a condition, the active devices dissipate power for a small percentage of the oscillation period and, at the same time, the low-frequency noise up-conversion into PN is reduced. Class-F oscillators perform such oscillation waveforms by increasing the third or the second harmonic of the oscillation voltage through an additional resonance. A possible class-F oscillator implementation is proposed in [28] and depicted in Figure 3.10 (a). Besides the main resonator at the fundamental frequency, an additional parallel resonator at the 3rd harmonic is placed in series with the pair. Consequently, the overall impedance, $Z_{IN,}$ has the shape shown in Figure 3.10 (b). In this condition, the transistor noise contribution to the overall PN is considerably reduced by the almost square voltage waveform, sketched in Figure 3.10 (c), despite the presence of a discharge path to ground for the tank. Indeed, transistors M_1 and M_2 are pushed in the triode region even longer than in the case of class-B oscillator, thus injecting a significant amount of noise into the tank.

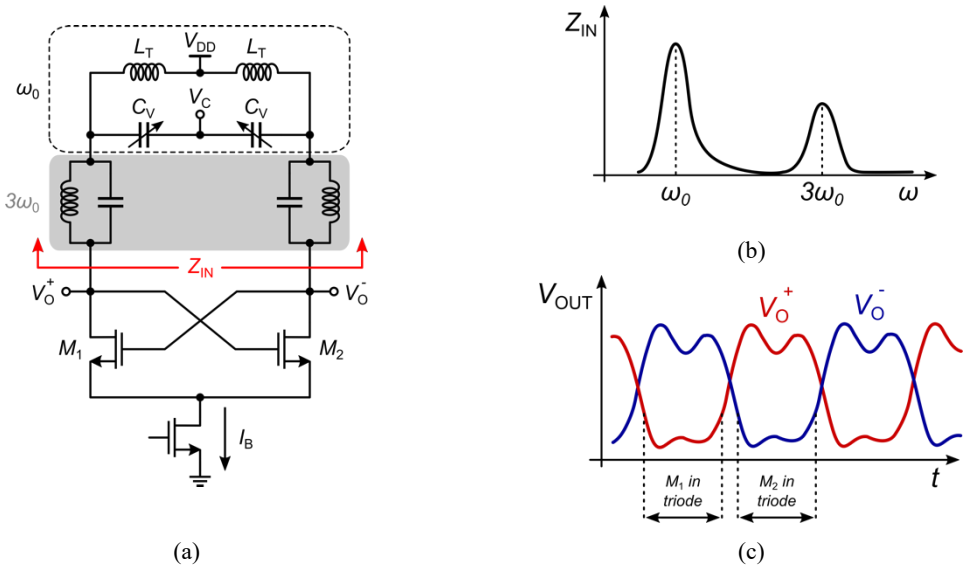


Figure 3.10. (a) A possible implementation for the class-F oscillator along with (b) the input impedance exhibits by the tank and (c) the output voltage waveform.

The area penalty related to the use of an extra tank can be avoided by including the auxiliary resonance at the 3rd harmonic into a transformer-based tank along with the fundamental one [29]. It was theoretically demonstrated in [13] that to significantly improve PN with respect to the tradition class-B oscillator, the *Q*-factor of the auxiliary resonance at the 3rd harmonic should be higher or at least comparable to that at the fundamental frequency.

Presently, many arrangements of the class-F oscillator are available in literature aimed at improving both PN and the pseudo-squaring of voltage waveform but at the cost of increasing the tank complexity [30]-[33].

3.3.5. Transformer-based oscillator

A transformer is often used in the LC-tank instead of a simple inductor to implement a harmonic oscillator. To this purpose, transformer-based tank can be tuned into an oscillator by connecting the transistor pair at one of its ports, thus performing the so-called one-port oscillator illustrated in Figure 3.11 (a). Alternatively, the feedback loop can be made around the transformer itself by connecting the primary and secondary windings at the gate and drain terminal, respectively, thus resulting in the two-port oscillator shown in Figure 3.11 (b). Topologies that combine both approaches are also allowed as reported in [34]-[37].

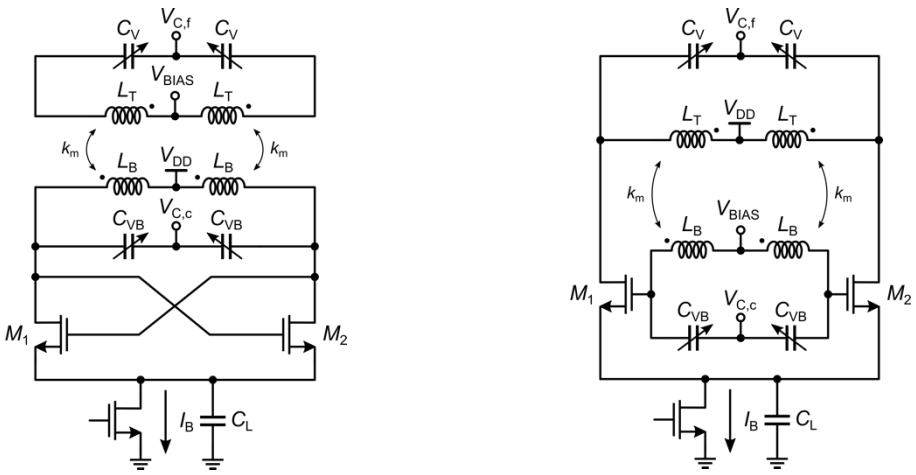


Figure 3.11. Schematic of transformer-based oscillator with (a) one-port and (b) two-port resonator.

The magnetic coupling as well as the two parallel resonance frequencies provided by the transformer, are the key features of this oscillator topology, which can be exploited for several design purpose. In [35]-[38], the two oscillation modes are used to improve the frequency tuning range by performing two frequency bands driven by two active stages. In [39], a transformer is used to implement feedback between drain and gate terminals of a cross-coupled pair to increase the oscillation amplitude. Another ingenious use of transformers in the design of integrated oscillators is to implement an ac-coupling varactor in the tank [32], [40], [41]. On the other hand, a transformer tank can be also exploited to improve the oscillator noise performance. The second resonance can be tuned at the 2nd harmonic of the oscillation frequency, to perform a CM resonance in a class-B oscillator [20], or around the 3rd harmonic to achieve the class-F operation [29]. When the transformer is configured as a two-port resonator, the voltage gain of the tank can be used to reduce the active device noise contributions. This was accomplished in [21] using a step-up transformer for a class-C oscillator achieving a very impressive FoM. However, the step-up transformer-coupled oscillator suffers from several drawbacks. The *Q*-factor of the secondary winding is usually lower than the primary one, making its noise no more negligible. Furthermore, there is a serious issue of reliability due to the large voltage swing at the transistor gates. To mitigate this problem, a complementary topology and/or a supply voltage reduction can be used.

It is worth noting that, with the increase of the resonator order, frequency stability becomes an issue, and more design parameters have to be optimized simultaneously

including inductance ratio, capacitance ratio and coupling factor. Although, many tools are available to design and automatically optimize inductors, transformers are mostly custom designed and hence they call for an extensive use of EM simulations. As a result, transformer-based oscillators are significantly more complex to optimize than a simple LC-tank oscillator. In addition, the transformer is a fourth-order network and hence the resonator quality factor is not uniquely defined for a given transformer and oscillation frequency. Indeed, primary and secondary capacitances affect the resonator quality factor and, in many cases, their contribution could result higher than that of primary and secondary inductors when considered as stand-alone elements. Nevertheless, the increase of tank complexity to achieve a better PN or PN/TR trade-off has attracted considerable interest and is one of the most important trends in the integrated oscillator design in CMOS technology.

3.4. Challenges in mm-wave VCO design

To provide a stable and tunable carrier frequency, VCO is embedded in a phase locked loop (PLL), which usually performs the frequency synthesizer in mm-wave transceivers. The transceiver architecture directly affects the frequency synthesizer requirements with a huge impact especially on VCO and pre-scaler design. The two most common transceiver architectures are super-heterodyne and direct-conversion [11]. Both architectures work as frequency conversion systems, and they differ for the number of conversions made to translate signal frequency from mm-wave to baseband and vice versa. However, super-heterodyne architecture needs more than one frequency synthesizer to convert the frequency along with a bulky off-chip image rejection and channel filters. On the contrary, direct conversion uses LO at the same frequency of the RF signal and is usually preferred in a fully integrated design mainly because it avoids the need for off-chip filters and requires only a single frequency synthesizer. Unfortunately, it suffers from many drawbacks such as LO leakage, offset, and frequency pulling in VCO due to the power amplifier (PA) working at the same frequency. Indeed, due to finite substrate and power supply isolation or undesired parasitic return paths, the PA output signal leaks into the VCO, corrupting the output spectrum. This leakage is a very critical issue in mm-wave radar transceiver and poses severe limitation to the RX sensitivity. At mm-wave frequencies, direct LO synthesis techniques face additional

design challenges to meet the desired PN and TR requirements. Unfortunately, as the VCO oscillation frequency increases the varactor quality factor drops rapidly, thus degrading the overall tank quality factor. This leads to PN degradation in the thermal noise region and demands for a trade-off between TR and low PN. The reduction in the tank quality factor at mm-wave frequency results also in a higher power consumption, usually required to guarantee a good PN performance. The need for larger transistors to support the oscillation and the consequent larger interconnection area gives rise to heavy parasitic capacitances, which in turn greatly impact TR especially when a low supply voltage is used [42]. Moreover, the flicker noise corner frequency tends to worsen in VCOs operating at mm-wave frequencies [30] and this is further exacerbated by the use of nanoscale CMOS technologies. Finally, current return paths become even more important at mm-wave frequencies, since they might shift the CM resonance frequency causing an oscillator PN degradation and even unwanted oscillations [20], [30].

To partially overcome all these drawbacks, a common solution consists of lowering the VCO oscillation frequency and then achieving the operating mm-wave frequency by means a frequency multiplier. Thank to that, passive components with higher quality factor can be designed, thus guaranteeing a better PN/TR trade-off. Moreover, a VCO with a lower oscillation frequency simplifies the PLL implementation since it relaxes the pre-scaler design and prevents the system from being affected by PA pulling effects. To this aim, several frequency multiplication techniques are typically employed, such as subharmonic injection-locking [43], self-mixing [44], *N*-push VCO [45], extraction of harmonics (e.g., second [46], [47] or third harmonic [30], [48]), or any combination of these techniques. However, all these approaches need to face out some relevant trade-offs.

The injection-locked frequency multiplier (ILFM) technique exploits an auxiliar oscillator operating at a lower frequency to lock the frequency of the mm-wave VCO, as is shown in Figure 3.12 (a). The injected signal is generated as an harmonic of the low-frequency VCO, which should be strong enough to lock the output at the desired frequency. As a result, amplification stages could be needed [49]. In addition, fundamental oscillator with a wide locking range is required to guarantee injection locking despite the PVT variations. LO self-mixing technique allows easily doubling [50] or tripling [44] the oscillation frequency by combining the VCO output signal with itself,

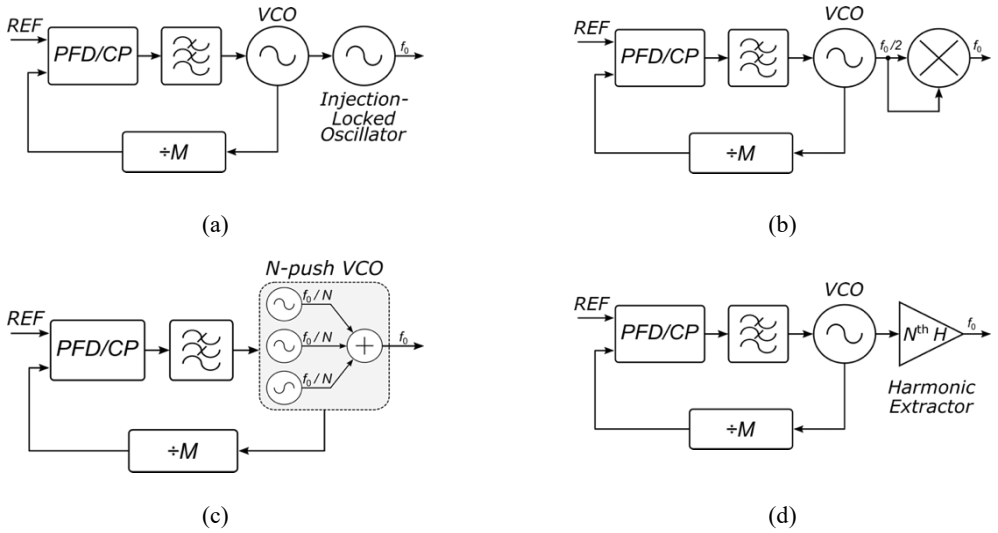


Figure 3.12. Frequency multiplier based on (a) sub harmonic injection locking, (b) self-mixing, (c) N push VCO and (d) harmonic extraction.

or its 2nd harmonic, through a double-balanced gilbert-cell, as displayed in Figure 3.12 (b). This approach has the great advantage of producing a differential output, but it results in high complexity, high current consumption, and large silicon area occupation. A triple-push-VCO architecture [45] is shown in Figure 3.12 (c), where fundamental and 3rd harmonic of the oscillation frequency generated by three VCOs are added destructively and constructively, respectively. Although this technique allows a large frequency tuning range, it is affected by phase mismatches between oscillators. Furthermore, the use of multiple oscillators greatly increases power consumption and area occupation. Device non-linearity is exploited to perform the mm-wave signal with the generation of the signal through the harmonic extraction technique depicted in Figure 3.12 (d). Another interesting approach is the push-push frequency doubler that provides the 2nd harmonic signal by exploiting a common-mode node of the oscillator and the transistor non-linear behavior [51], [52]. This approach exhibits low complexity and reduced power consumption but suffers from low output power.

3.5. Phase noise in VCO: an overview of optimization approaches

As previously discussed, to achieve high frequency accuracy VCOs are embedded in a PLL and hence they can benefit from the frequency behavior of the loop to filter out the oscillator noise close the carrier. Hence, the minimization of the PN in the thermal region is a quite crucial task in every oscillator design strategy. However, the PLL loop bandwidth is commonly chosen to minimize the noise contribution of the CPs. Consequently, if the PLL bandwidth is less than flicker noise corner frequency a portion of the oscillator low-frequency noise remains unfiltered degrading the frequency synthesizer performance. Furthermore, as the CMOS technology advanced, the flicker (1/*f*) noise in MOS transistor has worsened making the 1/*f* noise up-conversion in oscillator a very critical issue especially in FinFETs [53] and FD-SOI [54] process. Indeed, compared with SiGe bipolar transistors, CMOS transistors are affected by a higher 1/*f* noise due to interface states and, thus, exhibits higher corner frequencies of several MHz [55]. On the other hands, most of the modern wireless communication systems are rely on frequency synthesizers capable to providing a very low PN frequency sources. Consequently, understanding of the 1/*f* noise up-conversion and ensuring the reduction of these mechanisms is highly recommended.

3.5.1. Phase noise optimization in the thermal noise region

Despite its simplicity, *Leeson*'s formula provides useful indication to minimize the oscillator PN, especially in the thermal noise region. Neglecting the flicker noise contribution and considering $P_s = V_{osc}^2/(2R_T)$, where V_{osc} is the oscillation amplitude and R_T is the tank equivalent parallel loss resistance, *Leeson*'s formula can be rewritten in the following simplified form.

$$\mathcal{L}(\Delta\omega) = 10 \cdot \log\left[\frac{FkT}{V_{osc}^2} \cdot R_T \cdot \left(\frac{\omega_0}{Q_T \Delta\omega}\right)^2\right] \tag{3.12}$$

A proper topology selection, along with an optimal biasing condition, is essential to maximize the oscillation amplitude while maintaining low the noise excess factor. However, the maximum oscillation amplitude is related to the supply voltage V_{DD}, which

scales with technology node (about 1 V for a 28-nm CMOS technology) and is limited by the oscillator topology and reliability issues.

As highlighting in (3.12), PN can be reduced by minimizing the expression R_T/Q_T^2, while keeping the oscillation swing constant. Both R_T and Q_T are technology related parameters and dependent only on the tank components. Scaling down the tank inductance has always been one of the most common solutions to reduce PN in LC-oscillators. As a matter of fact, the procedure of reducing the inductor size to lower the PN is intuitive as it progressively reduces the noise contribution of the equivalent tank parallel resistance ($R_T = \omega_0 L_T Q_T = Q_T\sqrt{L_T/C}$), which directly injects noise in the output nodes. In the thermal noise region, PN is linearly proportional to R_T and hence if the impedance is reduced by a factor of N, PN reduces by N. Furthermore, all other noise sources (represented by F in Eq. 3.12) scale down as well by the same amount since their contributions to noise are referred to the one produced by the tank [6], [56]. On the other hands, scaling down the equivalent tank parallel resistance calls for a higher bias current to restore the desired oscillation amplitude. As a result, PN minimization through tank inductance reduction is achieved at the cost of a larger power consumption, which does not lead to any improvement on the FoM. In addition, a lower inductance requires an increase in the tank capacitance to achieve the desired oscillation frequency, which in turn increases the tank losses. It is interesting to note that reducing inductance by the inductor shrinking is a valid strategy just until its quality factor does not significantly drop. Alternatively, the inductance can be reduced through the parallelization of multiple identical tanks or oscillators, thus realizing a multi-core VCO [40], [57]-[59]. Although the multi-core strategy allows a low PN without impairing the tank quality factor, it comes at the cost of complicated design flow and layout along with a substantial increase in the silicon area occupation.

A most powerful approach consists of maximizing Q_T, as it allows a simultaneous improvement of both oscillator PN and power consumption. Following the consideration carried out in the previous sections, a lower oscillation frequency is beneficial to implement passive components with a higher Q-factor. Therefore, the choice of the oscillation frequency is a crucial point also for the PN optimization. Obviously, many trade-off with the other system block requirements are involved in this choice, but from the oscillator PN standpoint some useful considerations can be carried out. While a small

inductance improves PN by reducing R_T, the inductor Q-factor tends to increase for large inductor values. Nevertheless, a larger inductor limits the achievable TR [60]. In addition, a physical limitation to the improvement of the Q-factor in a large inductor size is occurs for the substrate losses. Consequently, an optimal value can be found for the oscillation frequency, which reduces parameter R_T/Q_T^2 leading to a lower PN. In addition, a transformer-based tank can be profitably used at mm-wave frequencies since it allows a better PN, thanks to an enhanced resonator Q-factor.

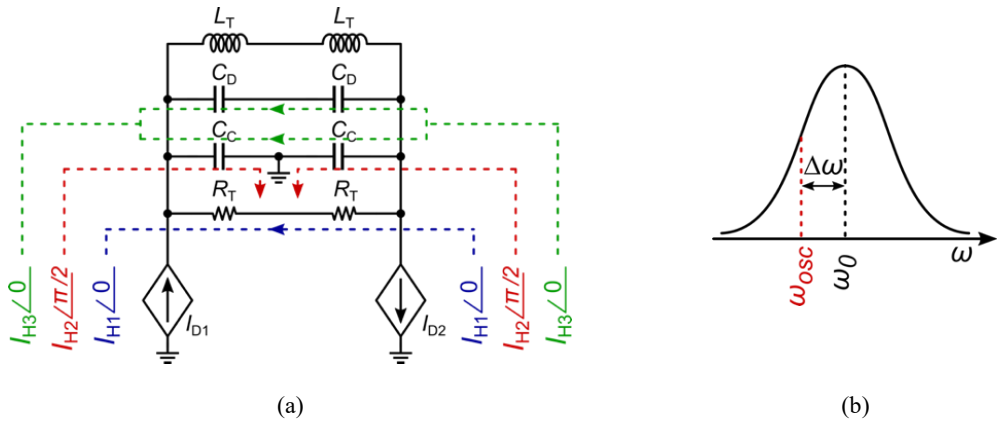
Finally, the thermal noise of the tail current source around the 2nd harmonic of the oscillation frequency is direct down-converted into PN around the fundamental tone. To reduce this PN contribution a large tail capacitor as well as a LC-tail filter tuned at the 2nd harmonic of the oscillation frequency can be used [17].

3.5.2. Phase noise optimization in the flicker noise region

Differently from the PN in the thermal noise region, whose main actors have been well recognized as early as 1966 in the Leeson's PN model, the theory on the $1/f$ noise up-conversion was not effectively developed until the ISF function was introduced in 1998 by Hajimiri and Lee. A few years later, the early studies on the $1/f$ noise up-conversion in LC-oscillators, mainly focused on current-biased VCO, allowed Rael and Abidi [61] to provide an initial description about flicker noise up-conversion mechanisms related to the tail-current source.

For LC oscillators based on the differential-pair, two main mechanisms, describing how the flicker noise of the tail current source transistor is up-converted in PN, have been recognized by Rael and Abidi. In a first mechanism, the switching action of the differential pair translates the flicker noise of the tail current source likewise to a single-balanced mixer. Therefore, the translated flicker noise appears at the resonator as amplitude modulation (AM) and then is converted to frequency modulation (FM) mainly through nonlinear parasitic capacitances of the transistors and varactors. Actually, the AM-to-FM conversion performed by varactors translates any noise voltage modulating the oscillation amplitude in a phase noise [62], [63]. To minimize this effect, without impairing the overall VCO tuning range, a viable solution is the use of a small varactors for the finer frequency tuning along with an array of switched capacitors for the coarse tuning [64].

Regarding the second mechanism, it is related to the higher-order harmonics of the current injected into the LC tank. Indeed, differential pair transistors generate a current with a rich harmonic content. The fundamental component of this current, I_{H1}, flows into the equivalent parallel loss resistance of the tank, while higher harmonics are filtered out by the resonator capacitance as shown in Figure 3.13 (a), thus upsetting the power balance. Consequently, a down shift of the oscillation frequency from its expected value occurs, as illustrated in Figure 3.13 (b), to increase the inductive reactive energy, and restore the energy equilibrium of the tank. This effect is commonly referred to as the Groszkowski effect [65].



(a) (b)

Figure 3.13. (a) Current harmonic paths leading to the Groszkowski effect and (b) the resulting shift in the oscillation frequency.

In addition, any fluctuation in the current injected into the tank can lead to a modulation of that shift, thus resulting in an indirect flicker noise up-conversion. A very thorough analysis of this effect, referred to as incremental Groszkowski effect, is provided in [66], where more saturated transistors are suggested to reduce this mechanism but at the cost of an increased power consumption and/or higher parasitic capacitances. Especially at mm-wave frequencies, another Groszkowski effect arises due to the nonlinear parasitic capacitances of the transconductor, which are no longer negligible [67]. Since the flicker noise is modulated onto the 2nd harmonic current flowing through these capacitances, a tail filter is commonly used to suppress the 2nd harmonic of the current [17]. Alternatively, the amplitude of the 2nd harmonic could be kept constant by adding a differential source capacitance [68].

Following the demand for a reduced supply voltage due to advanced CMOS technologies, the tail-current source is often completely removed or replaced with a

switched tail-resistor, thus making a voltage-biased oscillator. This is an increasingly popular approach, since it cuts the tail transistor noise contribution and is suitable for low-supply voltage operation [14], [39], [69]. [69]. In this case, the *1/f* noise up-conversion is mainly ascribable to the modulation of the harmonics of the output voltage waveform. As suggested from the ISF theory, this *1/f* up-conversion can be suppressed by symmetrizing both rising and falling edges in the oscillating waveform. Actually, both 2nd [20] and 3rd [70]-[72] harmonics are recognized as the cause of this asymmetry, as explained in [73]. Seeking to mitigate their effects, several techniques have been proposed in literature. An approach [74] is accomplished by narrowing the conduction angle by operating in class-C, as in [21], [49], [75]-[77]. Alternatively, two controlled switches implemented by two PMOS transistors and placed under the cross-coupled pair through the coupling of an RC-filter [78] or transformer [79] can be used. In [80] and [81], the linearization of the active stage transconductance was proposed by reducing the transistor width or by adopting resistors in series to sources with the aim of reducing the level of current harmonics at the expense of oscillator start-up robustness and increased PN in the thermal region. These limitations can be circumvented by adding resistors in series to drains as in [71]. On the other hand, waveform shaping of the drain-source voltage waveform by acting on the 2nd harmonic has proved to be an effective method to reduce the flicker noise up-conversion in NMOS-only in class-B [57], class-D [20] and class-F oscillators [30], [33]. Otherwise, the 2nd harmonic voltage is inherently minimized in a complementary oscillator, due to the complementary operation itself as reported in [83]. For such oscillator, the waveform asymmetries are mainly ascribable to the 3rd harmonic, whose PN effects can be reduced by a proper waveform shaping as in the class-F operation. However, the implementation of an auxiliary resonance in a harmonically tuned tank is critical, especially for mm-wave frequencies since any parasitic contribution could shift the auxiliary frequency resonance. Consequently, those techniques have tight constraints in practical designs and their use at mm-wave frequencies is not so straightforward and does not always lead to reliable solutions.

3.6. Transformer-based VCO for *W*-band automotive radar applications: a design example

Previously, several of the main LC-oscillator topologies have been introduced highlighting their benefits and drawbacks. The limits of the traditional class-B oscillator have been overviewed and solutions to overcome them have been suggested. Among them, the transformer-based topology can be profitably used at mm-wave frequencies since it provides great design flexibility that can be exploited for the PN optimization or, better, for the best trade-off between PN and TR, in both one- and two-port oscillator configurations. Therefore, this topology has been chosen for the VCO implementations discussed in this dissertation.

Based on the considerations made so far, in the next paragraph a design example of a VCO for *W*-band automotive application is proposed, which provides design guidelines for transform-based oscillator at mm-wave frequencies. Although several performance enhancing techniques have been proposed in literature to improve PN in the transformer-based VCO topology, their use at mm-wave frequencies is not so straightforward and does not always lead to reliable solutions. Consequently, the PN performance is addressed in this design by exploiting the enhanced resonator *Q*-factor provided by the transformer-based tank, as is shown below.

3.6.1. Analysis of the proposed transformer-based VCO

Figure 3.14 (a) shows the schematic of the proposed VCO. It consists of a transformer-based topology with an oscillating core at 38 GHz. The resonator is built around the integrated transformer, T_1, which enhances the *Q*-factor and provides a positive feedback path from the drains to the gates of the cross-coupled differential pair, $M_{1,2}$.

To compensate for the PVT tuning reduction, the VCO was designed to cover about 4 GHz of frequency tuning range (37 – 41 GHz), which is higher than the nominal tuning range of 2.5 GHz required by the radar application. To provide the required tuning capability Accumulation-MOS (A-MOS) varactors, C_V, with a single ended control voltage, V_C, were adopted.

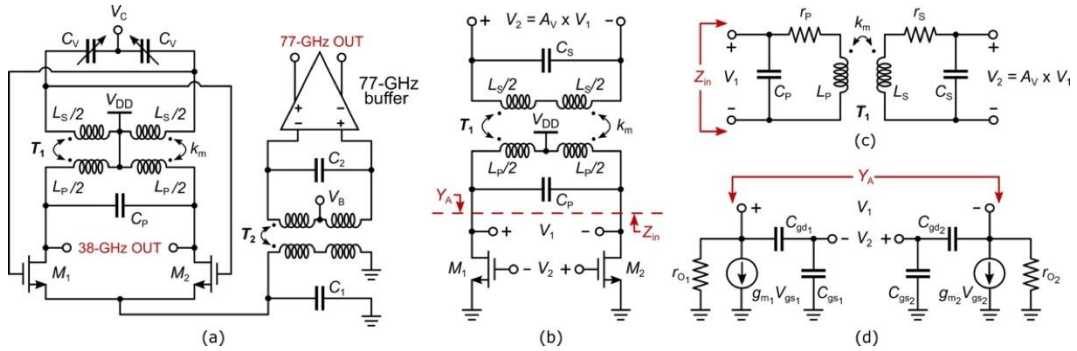


Figure 3.14. (a) Simplified schematic of the proposed VCO. (b) Transformer based VCO equivalent circuit. (c) Transformer based tank. (d) Small signal active core equivalent circuit.

As shown in Figure 3.14 (a), the 77-GHz signal is picked up at the common source node of $M_{1,2}$ using transformer T_2, whose primary and secondary winding resonances are tuned at the 2nd harmonic of the VCO oscillation frequency. This signal is applied to a buffer that delivers it at the output with the desired power level. Note that the resonance at the first coil of T_2 provides a high impedance path between the differential pair and ground at the 2nd harmonic of the oscillation signal. This resonance prevents the differential pair from loading the tank when M_1 or M_2 are pushed into the triode region, thus avoiding PN degradation. Finally, the 38 GHz VCO output that drives the PLL pre-scaler is drawn from the primary winding of transformer T_1.

To analyze the start-up condition, the VCO can be replaced with the equivalent circuit in Figure 3.14 (b). Here, voltage V_2 at the secondary side of T_1 is equal to voltage V_1 at the primary side multiplied by the voltage gain, A_V, provided by the transformer. Voltage V_2 is also the voltage across the gates of transistors $M_{1,2}$. Therefore, the equivalent circuit in Figure 3.14 (b) can be divided into the transformer-based tank and the active core as shown in Figure 3.14 (c) and Figure 3.14 (d), respectively. Resistances r_P and r_S in Figure 3.14 (c) account for the losses in the primary and secondary windings of T_1, whereas capacitors C_P and C_S include the resonant capacitor and the varactor at the primary and secondary winding, respectively, besides parasitic capacitance contributions at the gate and drain of the input pair. The MOS parameters in Figure 3.14 (d) have the usual meaning.

The input impedance, Z_{in}, the transimpedance, Z_t, and the voltage gain, A_V, of this network are calculated in (3.13), (3.14) and (3.15), respectively. They are fourth-order

transfer functions with two pairs of complex conjugate poles, which account for the resonances at the primary and secondary windings. Assuming that the coupled inductors L_P and L_S have a sufficiently high Q-factor at the operating frequency, i.e., $Q_P = \omega L_P/r_P \gg 1$ and $Q_S = \omega L_S/r_S \gg 1$, the two resonant frequencies can be written as in (3.16).

$$Z_{in}(s) = \frac{s^3[L_P L_S C_S(1-k_m^2)] + s^2[C_S(L_S r_P + L_P r_S)] + s(L_P + r_S r_P C_S) + r_P}{s^4[L_P L_S C_P C_S(1-k_m^2)] + s^3[C_P C_S(L_S r_P + L_P r_S)] + s^2(L_P C_P + L_S C_S + r_S r_P C_P C_S) + s(r_P C_P + r_S C_S) + 1} \quad (3.13)$$

$$Z_t(s) = \frac{s k_m \sqrt{L_P L_S}}{s^4[L_P L_S C_P C_S(1-k_m^2)] + s^3[C_P C_S(L_S r_P + L_P r_S)] + s^2(L_P C_P + L_S C_S + r_S r_P C_P C_S) + s(r_P C_P + r_S C_S) + 1} \quad (3.14)$$

$$A_V(s) = \frac{V_2}{V_1} = \frac{Z_t(s)}{Z_{in}(s)} = \frac{s k_m \sqrt{L_P L_S}}{s^3[L_P L_S C_S(1-k_m^2)] + s^2[C_S(L_S r_P + L_P r_S)] + s(L_P + r_S r_P C_S) + r_P} \quad (3.15)$$

$$\omega_{L,H}^2 = \frac{1 + \xi \pm \sqrt{(1+\xi)^2 - 4\xi(1-k_m^2)}}{2(1-k_m^2)} \omega_S^2 \quad (3.16)$$

where k_m is the magnetic coupling coefficient and ξ is defined as:

$$\xi = \left(\frac{\omega_P}{\omega_S}\right)^2 = \frac{L_S C_S}{L_P C_P} \quad (3.17)$$

The transconductance that satisfies the start-up condition can be found by evaluating the small signal admittance, Y_A, across the drain nodes of transistors $M_{1,2}$ as shown in Figure 3.14 (d). Considering the feedback provided by T_1 that is expressed by gain A_V, Y_A is given by:

$$Y_A(j\omega) = -\frac{g_m}{2} A_V + \frac{1}{2r_O} + j\omega \frac{C_{gd}}{2}(1 + A_V) \quad (3.18)$$

Eq. (3.18) reveals that the equivalent transconductance of the differential pair is boosted by the transformer voltage gain. By evaluating (3.13) and (3.15) for $s = j\omega$ and combining them with (3.18), the constrain on the couple pair transconductance, g_m, imposed by the start-up condition can be derived as follows:

$$g_m > \frac{\omega}{\omega_P} \cdot \frac{\left[\left(\frac{\omega}{\omega_S}\right)^2 - 1\right] + \xi\left[\left(\frac{\omega}{\omega_P}\right)^2 - 1\right]\frac{Q_P}{Q_S}}{\omega_P n k_m Q_P L_P} \quad (3.19)$$

where $n = \sqrt{L_S/L_P}$ is the transformer turn ratio. As expected, the primary coil inductance and quality factor play a key role in the start-up condition. In addition, it is

interesting to note that the transconductance in (3.19) is negative only for $\omega = \omega_L$. Hence, the oscillation never occurs at the higher frequency ω_H.

It is well-known that the tank Q-factor plays a key role in the start-up condition as well as in the oscillator PN performance, as previously highlighted in the Leeson's formula (see Eq. (3.12)). As consequence, it is very important to understand how the design parameters should be set to optimize the tank Q-factor. The transformer-tank Q-factor, Q_T, can be evaluated from Figure 3.14 (c) using Z_t from (3.14) along with the following definition [1]:

$$Q_T = \frac{\omega}{2}\left|\frac{d}{d\omega}\angle Z_t(j\omega)\right|_{\omega=\omega_0} \tag{3.20}$$

Considering that for $\omega = \omega_0$, the imaginary part of the frequency response in (3.14) is negligible and assuming $Q_P Q_S \gg 1$, Q_T can be written as:

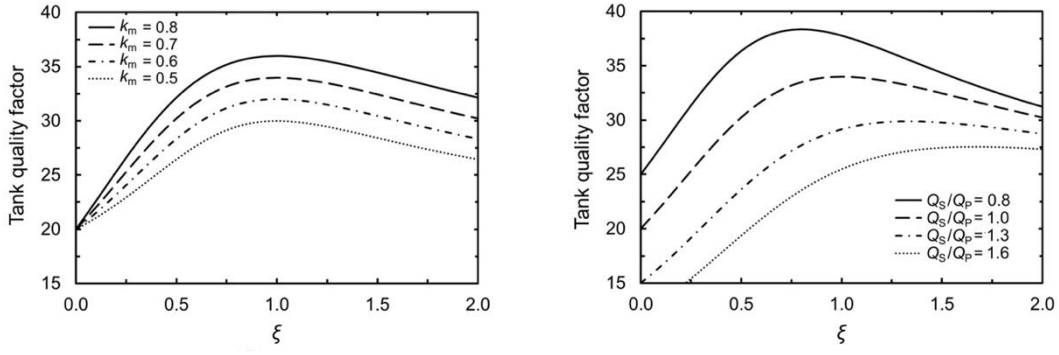
$$Q_T \approx Q_P \frac{2(1-k_m^2)\left(\frac{\omega_0}{\omega_S}\right)^2 - 1 - \xi}{\left[\left(\frac{\omega_0}{\omega_S}\right)^2 - 1\right] + \xi\left[\left(\frac{\omega_0}{\omega_P}\right)^2 - 1\right]\frac{Q_P}{Q_S}} \tag{3.21}$$

Eq. (3.21) gives the resonator Q-factor as a function of the primary and secondary coil quality factors, Q_P and Q_S, coupling coefficient k_m, and parameter ξ. Figure 3.15 shows Q_T, evaluated at ω_0, as function of ξ and for different values of k_m and Q_S/Q_P.

As apparent in Figure 3.15 (a), the resonator Q-factor increases with k_m. In a typical design, the transformer coils are assumed to have the same Q (i.e., $Q_P = Q_S = Q_O$) [84], hence the maximum tank Q-factor, $Q_{T,max}$, is achieved for $\xi = 1$ and is given by:

$$Q_{T,max} = Q_O(1 + k_m) \tag{3.22}$$

According to (3.22) the tank Q-factor is increased by a factor $1 + k_m$ with respect to the single inductor Q-factor. Moreover, Q_T is equal to Q_P when $\xi = 0$. Although $Q_P = Q_S$ is a usual design condition, the value of ξ that maximizes Q_T depends in general on the ratio Q_S/Q_P, as is apparent in Figure 3.15 (b). Indeed, by keeping Q_S constant and increasing Q_P, Q_T increases and reaches the maximum value for $\xi = \xi_{opt} = Q_S/Q_P$ according to (3.21). Considering the optimal value of ξ, a useful design strategy for tank



(a) (b)

Figure 3.15. Tank Q-factor evaluated at ω_0 as a function of ξ for different values of (a) k_m ($Q_S = Q_P = 20$) and (b) the ratio ($Q_S = Q_P = 20$) ($k_m = 0.7$).

optimization can be drawn from (3.17). For a given transformer T_1, the maximum Q_T is achieved by properly setting the primary and secondary coil capacitances C_P and C_S. Specifically, rewriting (3.17) as a function of ξ_{opt}, C_P and C_S can be expressed as:

$$C_P = \frac{1 + \xi_{opt} - \sqrt{1 + \xi_{opt}^2 - 2\xi_{opt}(1 - 2k_m^2)}}{2(1 - k_m^2)(2\pi f_0)^2 \xi_{opt} L_P} \tag{3.23}$$

$$C_S = \frac{1 + \xi_{opt} - \sqrt{1 + \xi_{opt}^2 - 2\xi_{opt}(1 - 2k_m^2)}}{2(1 - k_m^2)(2\pi f_0)^2 n^2 L_P} \tag{3.24}$$

Finally, the minimum transconductance value, g_{min}, is given by:

$$g_{min} = -\omega_O \cdot \frac{nC_S\sqrt{1 + \xi^2 - 2\xi(1 - 2k_m^2)}}{\xi k_m Q_T} \tag{3.25}$$

Eq. (3.25) is obtained by substituting (3.21) in (3.19). As expected, it shows the relationship of the inverse proportionality that binds g_{min} to Q_T.

3.6.2. Design of the proposed transformer-based VCO

The proposed VCO was designed in a 28-nm FD-SOI CMOS technology, which uses a general-purpose low-cost back end of line (BEOL) consisting of eight copper metal layers, whose thicker ones are the last two (referred as IB and IA) and an aluminum metal layer (LB) at the top of the stack. The previous analysis was adopted, which is summarized in the design flow in Figure 3.16.

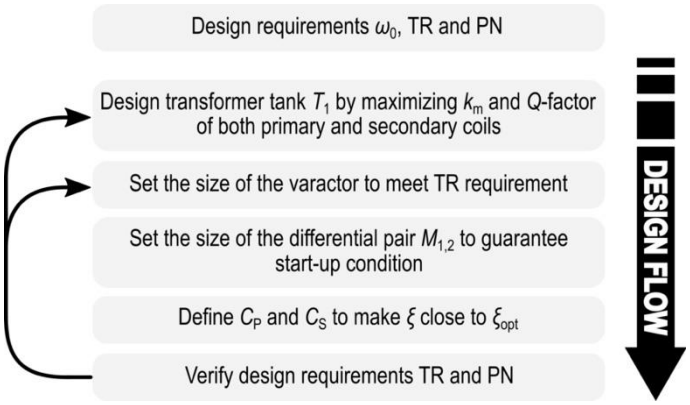


Figure 3.16. Proposed design flow.

Maximization of the resonator Q-factor is a key design point for low PN and a robust start-up condition, as highlighted in the previous Section. For a given operating frequency, Q_T depends on the parameters k_m and ξ, as shown in (3.21), and achieves its maximum, $Q_{T,max}$, if the condition $\xi = \xi_{opt}$ is satisfied.

Q_T increases with k_m and the Q-factor of both the primary and secondary windings of T_1. Moreover, a higher k_m also reduces the minimum transconductance for the start-up condition, as is apparent in (3.25). This, in turn, leads to a smaller size of the input pair and hence to smaller parasitic capacitances. To achieve a high k_m, the stacked configuration for the tank transformer was adopted.

As is well known, low inductance and large capacitance should be used in the tank to minimize PN [41], [85]. However, this approach leads to a low equivalent parallel loss resistance in the tank, which reduces the oscillator loop gain and hence entails the use of larger transistors to guarantee the start-up. This results in an increase in the parasitic capacitances, which limit the oscillator tuning range. Therefore, the sizes of the primary and secondary coil inductances of the transformer tank must be sized considered as part of a trade-off among between PN performance, tuning range, and power consumption.

Figure 3.17 shows a 3-D view of the VCO tank transformer, along with the adopted metal stack and its main parameters. The transformer was implemented by adopting a single turn octagonal winding with a stacked configuration, whose inner diameter and metal width were 65 μm and 25 μm, respectively. To minimize both resistive losses and parasitic capacitances toward from the substrate, the aluminum layer, LB, and the upper

copper metal layer, IB, were used for the primary and secondary windings, respectively, while the metal layer IA was used for the underpass. Moreover, neither polysilicon nor a metal patterned ground shield (PGS) was used in the transformer design, since it has a negligible impact on substrate losses at mm-wave frequencies [86], [87], but significantly reduces the self-resonant frequency. The whole transformer structure was designed using the 2.5-D electromagnetic (EM) simulator "Momentum," by including interconnections and supply/ground paths, with the aim of maximizing the Q-factor of both primary and secondary coils.

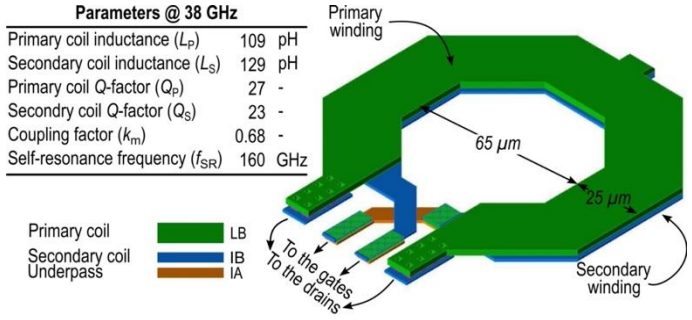


Figure 3.17. 3-D view of transformer T_1 with the adopted metal stack.

A-MOS varactors were profitably used to meet the TR requirement. Unfortunately, varactors exhibit a poor Q-factor at mm-wave frequencies, which is the main hindrance regarding the resonator quality factor. Therefore, varactors must be designed to be as small as possible, even though this is in contrast with the TR performance. Thanks to the transformer tank implementation that was adopted, the transformer turn ratio, n, was slightly higher than 1, and hence the varactors could be advantageously placed between the transistor gates. Indeed, the capacitance variation at the secondary winding was equivalently increased by a factor n. This allowed for a smaller varactor to be used to cover the tuning range, with the benefit of a reduced amplitude-to-phase noise conversion due to the varactor nonlinearity [47]. According to the previous consideration, a small A-MOS varactor connected to the secondary winding of transformer T_1 was used, which provided a capacitance ranging from 40 fF to 80 fF and a Q-factor around 14 at 38 GHz. Due to the underpass that performed the cross-connection of the transformer with the gates, the secondary winding of T_1 exhibited higher losses, although the overall tank Q-factor was dominated by the varactors. Using (3.21) and assuming that ξ was close to its optimal value, an equivalent tank Q-factor around 33 was achieved, which was higher than that of the transformer inductors.

As far as the differential pair is concerned, the size was set by considering that a larger transistor width provides a robust start-up condition but increases the thermal noise and parasitic capacitances, which affect PN and TR, respectively. The layout at mm-wave frequencies greatly impacts the performance of a VCO in terms of PN and TR. Therefore, accurate layout design becomes mandatory to minimize parasitic effects, especially gate resistance and gate-to-drain capacitances [88]. For this purpose, extensive EM and post-layout simulations were carried out to select the size of the transistor pair, whose aspect ratio was set to 28 μm/100 nm. Moreover, a multifinger transistor with double gate contacts was used in this design. Indeed, each transistor finger is a distributed RC network, and a double contact reduces the resistance of each finger by a factor of four, thus reducing the equivalent thermal noise.

To set ξ close to its optimal value, C_P and C_S must be set according to (3.23) and (3.24), respectively. For this design, C_P and C_S had overall values of 102 fF and 64 fF, respectively, which accounted for the parasitic, additional, and varactor capacitances, as mentioned before.

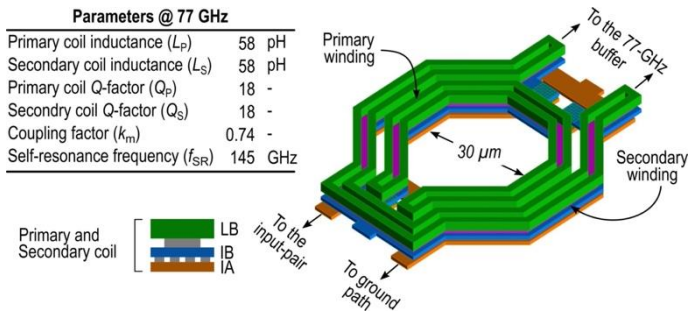


Figure 3.18. 3-D view of transformer T_2 with the adopted metal stack.

Transformer T_2 at the source node of the differential pair was designed using similar layout considerations to those of T_1 but with the aim of minimizing the insertion loss (IL) at 77 GHz. For this purpose, an interstacked configuration was preferred [86], whose 3-D view is shown in Figure 3.18, along with the transformer's main parameters. Both the primary and secondary windings were implemented with upper metal layers IA, IB, and LB by adopting a spiral width of 5.5 μm, which allowed for a good trade-off between the winding parasitic capacitances and series resistance to be achieved. The winding metal spacing was set to the minimum value (i.e., 2 μm) to improve the magnetic coupling

coefficient that was involved in the signal transfer and the inner diameter was set to 30 μm.

3.6.3. Experimental Results

The 38-GHz VCO was implemented in the 28-nm FD-SOI CMOS technology by STMicroelectronics, which provided as fast active device with f_T and f_{max} up to300 GHz [89] and a general-purpose BEOL. The chip was assembled with the chip on-board approach in an FR4 PCB. The measurement setup is shown in Figure 3.19. Frequency dividers and a buffer were also included in the test chip (see the dashed area in Figure 3.19), which was mounted in the PCB, together with a commercial PFD/CP and a discrete loop filter (LP) to enable closed-loop measurements at 4.8 GHz.

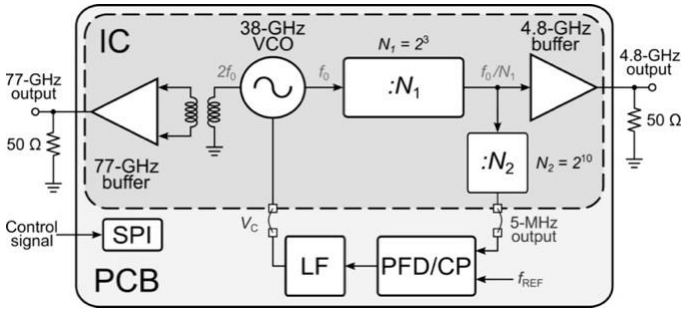


Figure 3.19. Simplified block diagram of the measurement setup.

Figure 3.20 shows the die microphotograph. The total die area was 1660 μm × 1280 μm, including the electrostatic discharge (ESD) protection ring and the radio frequency (RF) ground-signal-ground (GSG) pads, whereas the VCO core area was only 300 μm × 135 μm.

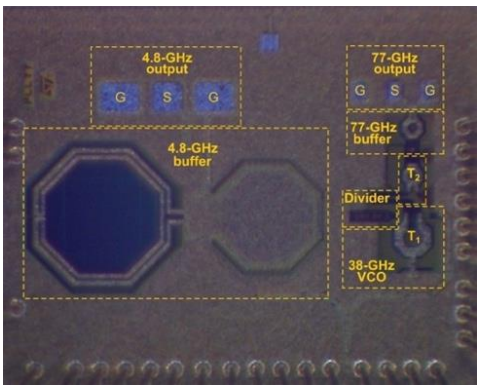


Figure 3.20. Die microphotograph.

The current consumptions of the VCO, divider, and testing buffer were 26, 30, and 4.5 mA, respectively, from a 1-V power supply. The measured tuning range was 4 GHz (i.e., from 35 to 39 GHz), when the varactor control voltage V_C swept from 0 to 1 V, as shown in Figure 3.21 (a). The comparison with the simulated curve highlighted a frequency shift of around 2 GHz, which could mainly be ascribed to the first-tentative varactor model available at the time of the VCO design.

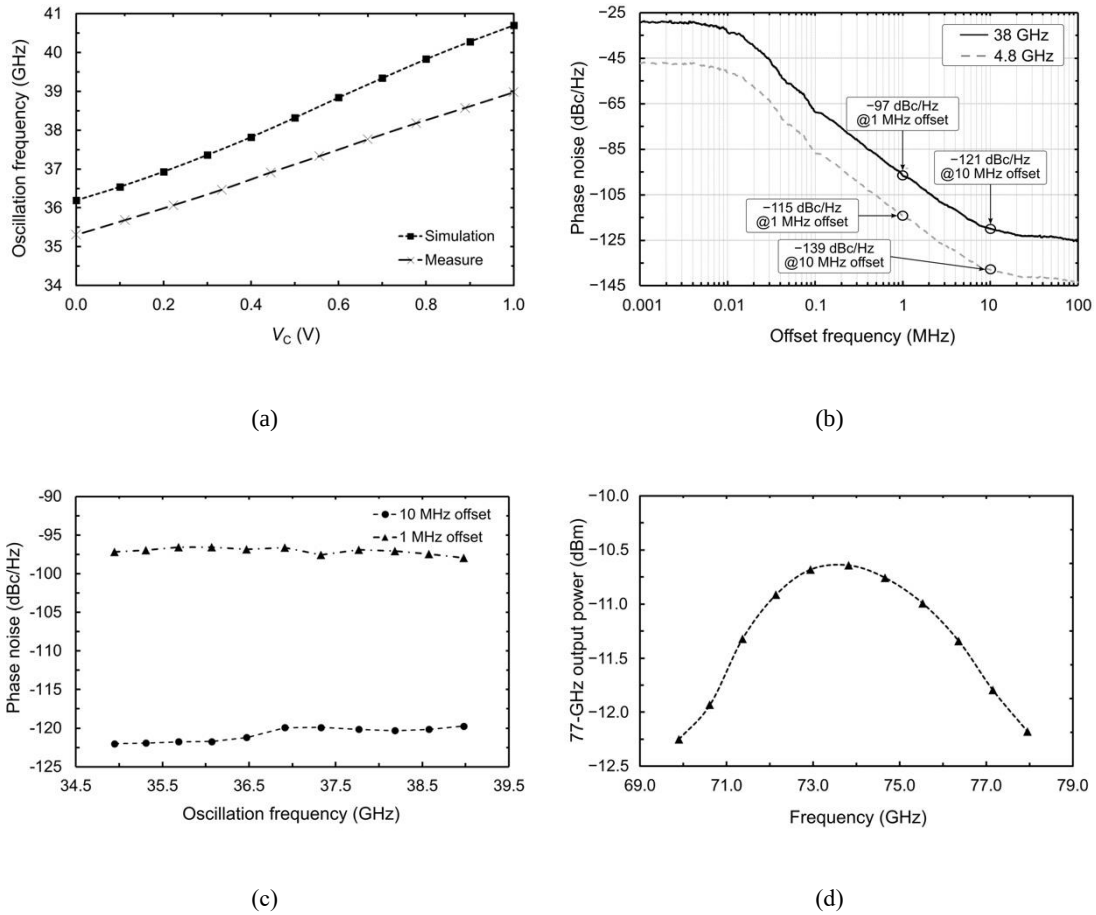


Figure 3.21. Measured (a) frequency tuning range, (b) phase noise, (c) phase noises at the 1-MHz and 10-MHz offset frequencies versus the VCO oscillation frequency, and (d) 77-GHz output power.

The measured VCO phase noise is illustrated in Figure 3.21 (b). The PNs at the 4.8 GHz were −115 dBc/Hz and −139 dBc/Hz at the 1 MHz and 10 MHz offset frequencies, respectively. The extrapolated curve at 38 GHz is also shown in Figure 3.21 (b), which was calculated from the assumption of a PN degradation factor of N^2 using a frequency division ratio of N. At a 38 GHz oscillation frequency, the equivalent PNs were about −97 dBc/Hz and −121 dBc/Hz at the 1 MHz and 10 MHz offset frequencies, respectively. The measured VCO phase noise at 1 MHz and 10 MHz

over the whole frequency tuning range is shown in Figure 3.21 (c). In these curves, the best, average, and worst PNs at a 1 MHz offset frequency were −96.6 dBc/Hz, −97 dBc/Hz, and −98 dBc/Hz, respectively, whereas the best, aver- age, and worst PNs at a 10 MHz offset frequency were −122 dBc/Hz, −121 dBc/Hz, and −120 dBc/Hz, respectively.

Figure 3.21 (d) shows the measured second harmonic output power as a function of the tuning voltage. The output power at 77 GHz varied between −12.2 dBm and −10.6 dBm in the entire frequency range.

Table 3.1 provides a summary of the measured results and a comparison with state-of-the-art mm-wave CMOS VCOs. To consider the oscillator's main performance parameters, a comparison was also carried out by considering the well-known figure of merits, FoM and FoM_T.

TABLE 3.1.
PERFORMANCE SUMMARY AND COMPARISON WITH THE STATE OF THE ART.

		MA JSSC'20 [90]	KASHANI TMTT'19 [91]	HU JSSC'18 [30]	CHEN TMTT'17 [92]	MAMMEI ISSCC'13 [93]	**THIS WORK**
CMOS technology		65 nm	65 nm	28 nm	90 nm	32 nm	28 nm FD-SOI
Bias approach		Current	Voltage	Voltage	Current	Current	Voltage
Power supply	**(V)**	1	1	1	1	1	1
Power consumption	**(mW)**	11.7	6.2	22.5[a]	8.1	9.8	26
Center frequency	**(GHz)**	39.6	55	29.5[b]	20.85	40	37
Tuning range	**(GHz)**	37.2 to 42	50.1 to 59.8	27.3 to 31.2	19.2 to 22.5	33.6 to 46.2	35 to 39.1
PN[c] @ 1 MHz	**(dBc/Hz)**	-94	-93.3	-103	-95.7	-97.3	-97
PN[c] @ 10 MHz	**(dBc/Hz)**	-120.3	-115.4	-123.5	-120	-117.3	-121
FoM[c] [d] @ 1 MHz	**(dBc/Hz)**	-175	-176.9	-180.5[a]	-177.8	-178.7	-175
FoM[c] [d] @ 10 MHz	**(dBc/Hz)**	-181	-178.9	-181[a]	-182.3	-178.7	-181
FoM_T[c] [e] @ 10 MHz	**(dBc/Hz)**	-176	-181.9	-183.5[a]	-181.8	-188.7	-176
FoM_T[c] [e] @ 10 MHz	**(dBc/Hz)**	-183	-184	-184[a]	-186.3	-188.7	-182

[a] Including the power consumption of the multiplier and buffer; [b] third harmonic extraction from a 10-GHz oscillating core; [c] normalized around 37 GHz; [d] $\mathrm{FoM} = \mathcal{L}(\Delta f) - 20\log(f_0/\Delta f) + 10\log(P_{diss}/1mW)$;
[e] $\mathrm{FoM}_T = \mathrm{FoM} - 20\log(\mathrm{TR}(\%)/10)$

By normalizing the PN according to its typical dependence on the oscillation frequency expressed by the Leeson's formula, the proposed VCO exhibited the best performance regarding the PN, except for [30], whose output frequency was achieved by exploiting the third harmonic of a 10 GHz oscillator. Specifically, the PN performance at a 10 MHz offset frequency, which is the most critical PN requirement for an automotive radar sensor, achieved an excellent value of −121 dBc/Hz. Regarding the FoMs, the proposed VCO showed similar values to the state-of-the-art oscillators.

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Chapter 4

Design and results of proposed mm-wave VCOS

4.1. Introduction

Mm-wave frequency synthesizers are highly demanded in a wide range of applications, such as medical imaging [1]-[3], wireless communications (e.g., WLAN [4], [6], 5G generation cellular networks [7], [8], etc.) and automotive radar sensors [9]-[13]. Whatever the addressed application, the mm-wave frequency synthesizer must provide proper tuning range (TR) to cover the desired operating band. Moreover, fast settling time must be achieved to meet high speed requirements of modern communication systems (e.g., 5G) that claim data transfer with low latency along with bit rates up to Gbps [14]. High speed operation is further required in pulsed radar for effective frequency coding [10].

In a VCO-based frequency synthesizer, the required tuning capability is achieved by the VCO itself, which must be able to provide a frequency tuning range larger than the desired operating frequency band in order to compensate for process, voltage and temperature (PVT) variations. Unfortunately, the technology scaling leads to a substantial reduction of the supply voltage, which limits the VCO control voltage swing and hence affects tuning range.

Designing mm-wave VCOs able to simultaneously archive low phase-noise and wide tuning range with low power supply is not a trivial task. Indeed, the lower is the power supply the larger should be the varactor size to preserve tuning range. However, a large

varactor leads to heavy losses, which no longer can be neglected with respect to the inductor ones. Moreover, varactor parasitic capacitances greatly increase their contribution on the overall tank capacitor especially in mm-wave VCOs, thus still reducing tuning range.

To improve the tuning range without impairing the phase noise performance, two different approaches are proposed in this Chapter. A first approach is a varactor-based technique that implements a dual-band VCO, which allows both long-range (i.e., from 76 GHz to 77 GHz) and short-range (from 77 GHz to 81 GHz) radar operation to be achieved, thus avoiding the need for different radar devices. A second approach is based on a flash frequency tuning technique for SC-based VCOs, which overcomes the tuning delay limitations of state-of-the-art solutions, thus achieving high speed frequency locking useful in a wide range of modern frequency synthesizers. Both techniques reduce the varactor size allowing the desired tuning range in two or more sub-bands. Unfortunately, the tuning curves in the sub-bands move up or down due to PVT variations, which limit the varactor size. To address this issue, a novel calibration strategy has been proposed, which compensates for PVT variations during the PLL start-up, thus resulting in a more relaxed VCO tuning range requirement.

Finally, the proposed VCOs have been embedded in a sub-harmonic PLL where a novel push-push frequency doubler has been implemented to address the high sensitivity of this circuit to the impedance supply paths, which is a critical issue at mm-wave frequencies.

In this Chapter, the proposed VCOs, frequency doubler and calibration strategy are presented, and the achieved results are discussed and compared with the state of the art. The adopted frequency synthesizer architecture is reported in Section 4.2, followed by the frequency doubler and calibration strategy, which are discussed in detail in Section 4.3 and Section 4.4, respectively. In Section 4.5, the design and the simulation results of the dual-band mm-wave VCO are provided, and finally Section 4.6 deals the design and experimental results of the proposed flash-frequency tuning technique for SC-based VCOs.

4.2. Proposed frequency synthesizer architecture

As discussed in the previous chapter, a very popular and useful approach to synthesize a frequency in the mm-wave spectrum consists of cascading a lower frequency PLL with a frequency multiplier. Assuming a noiseless frequency multiplication, this architecture results in a no theorical PN degradation compared with fundamental frequency ones. On the other hand, higher *Q*-factor for the passive components achievable by lowering the oscillation frequency is beneficial for a better oscillator performance and this advantage is directly translated to the desired mm-wave output frequency by the frequency multiplier.

In this work, a 38-GHz VCO has been designed to synthesize the operating frequency, which is embedded in a PLL with the architecture depicted in in Figure 4.1 and followed by a frequency doubler.

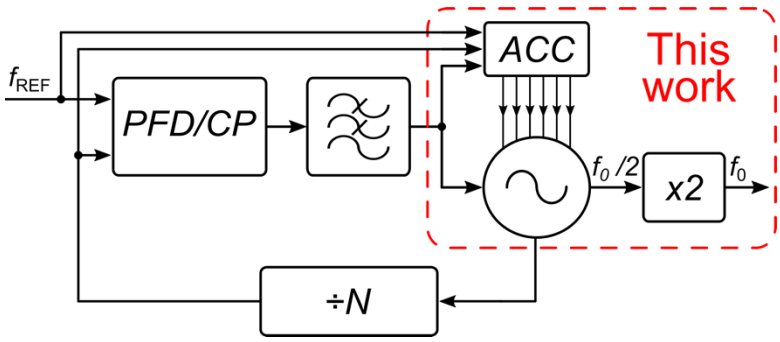
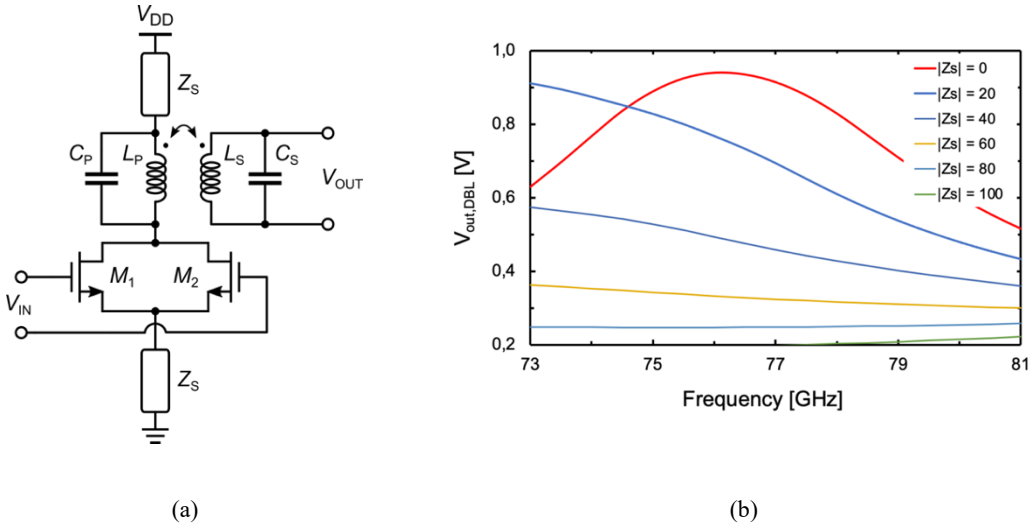


Figure 4.1. Adopted frequency synthesizer architecture.

In particular, the research activity presented in this dissertation has led to the design of two different 38-GHz VCOs based on patented techniques [15] aimed at providing a proper tuning range without impairing the phase noise performance. An automatic calibration circuit (ACC), based on a novel calibration strategy [18]-[20], is also introduced to compensate for the PVT variations during the PLL start-up, thus relaxing the VCO TR requirements. Furthermore, a novel push-push frequency doubler [21] has been proposed, which reduces the impedance supply paths sensitivity, which is one of the most critical issue in mm-wave frequency multipliers.

4.3. Proposed push-push frequency doubler

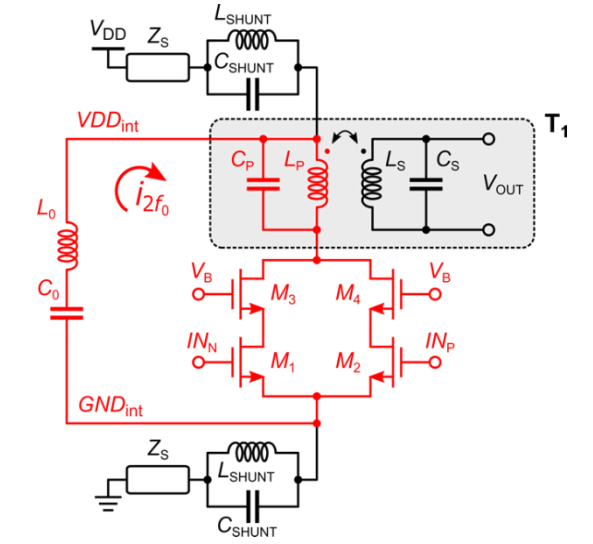
Among the different frequency multiplier architectures reported in literature [22], [23], push-push frequency doublers are commonly used due to their low complexity and reduced current consumption. However, these circuits are relied on the nonlinearity of the active devices and hence they typically suffer from low output power. Furthermore, push-push frequency multipliers are inherently single-ended and thus are affected by a high sensitivity to the impedance of supply paths (V_{DD}/GND), which is a critical issue especially for mm-wave applications. Consequently, special care must be taken in designing of the supply paths. Indeed, push-push frequency doublers call for low-impedance supply paths to properly operate. To corroborate this, a push-push frequency doubler, whose simplified schematic is shown in Figure 4.2 (a), was simulated sweeping the supply impedance, Z_S, as reported in Figure 4.2 (b).



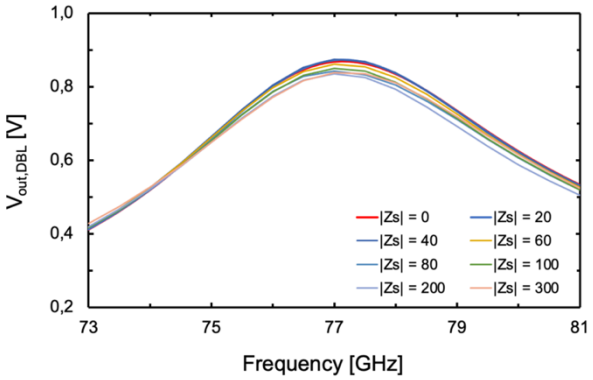
(a) (b)

Figure 4.2. (a) Simplified schematic of a typical push-push frequency doubler. (b) Simulated output voltage for different values of supply path impedance Z_S.

As can be seen, simulation results highlight that push-push frequency doubler performance are heavy affected by the supply path impedance, which significantly modifies the output voltage on the resonant load. Unfortunately, in a typical device for mm-wave applications, the control of the supply impedance is a non-trivial task due to the die complexity achieved using multiple TX and RX channels. To this aim a push-push frequency doubler insensitive to impedance of the supply path (V_{DD}/GND) is proposed, whose simplified schematic is shown in Figure 4.3 (a).



(a)



(b)

Figure 4.3. (a) Simplified schematic of the proposed push-push frequency doubler. (b) Simulated output voltage for different values of supply path impedance Z_S.

By suppling the circuit with 2nd harmonic shunt resonators (L_{SHUNT}, C_{SHUNT}), the desired current signal, i.e., i_{2f_0}, is prevented from being drawn by the DC supplies (V_{DD}/GND), making the proposed solution almost insensitive to the impedance of the supply paths, as displayed in Figure 4.3 (b). A 2nd harmonic tuned bypass (L_0, C_0) connecting the inherent supplies (i.e., VDD_{int} and GND_{int}) provides a return path for the desired current signal, thus guaranteeing proper circuit operation. In addition, a differential output is provided by using the load transformer T_1, which performs the single-ended-to-differential conversion.

Besides guaranteeing insensitivity to the supply path impedances, the proposed solution exhibits low complexity, which results in reduced current consumption and low silicon area occupation. Furthermore, by exploiting the cascode push-push pair ($M_1 - M_4$)

a high conversion gain can be achieved, thus reducing the VCO input signal for a given output signal.

To overcome the output swing limitation under low-voltage operation due to the cascode structure, a folded cascode variant of the push-push frequency doublers has been also proposed, as is shown in Figure 4.4.

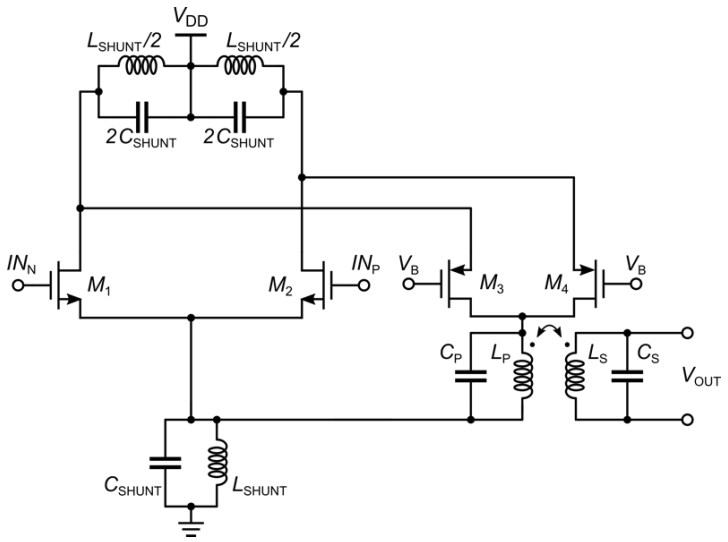


Figure 4.4. Simplified schematic of the folded push-push frequency doubler.

The folded-cascode solution guarantees the same insensitivity to the supply path impedances of the previous one, while exploiting a reduced number of inductive components. The required supply voltage can be effectively reduced with this implementation, but at the cost of a higher power consumption and a slightly lower gain, thus making cascode implementation preferable when a sufficient high supply voltage is available.

4.4. Proposed automatic calibration strategy

Process tolerances move the oscillation frequency outside the nominal tuning range that is defined by the maximum excursion of control voltage V_C imposed by the charge pump (CP). Calibration techniques are often used in PLLs to adjust tuning curves inside to the target frequency bandwidth by compensating the frequency variation induced by PVT variations. During the calibration process, comparison between the VCO (or its derivative signal) frequency and the reference frequency is involved, whose can be carried out when the PLL loop is either closed or opened. Thus, VCO calibration techniques can be categorized into two types according to the PLL status during calibration [24].

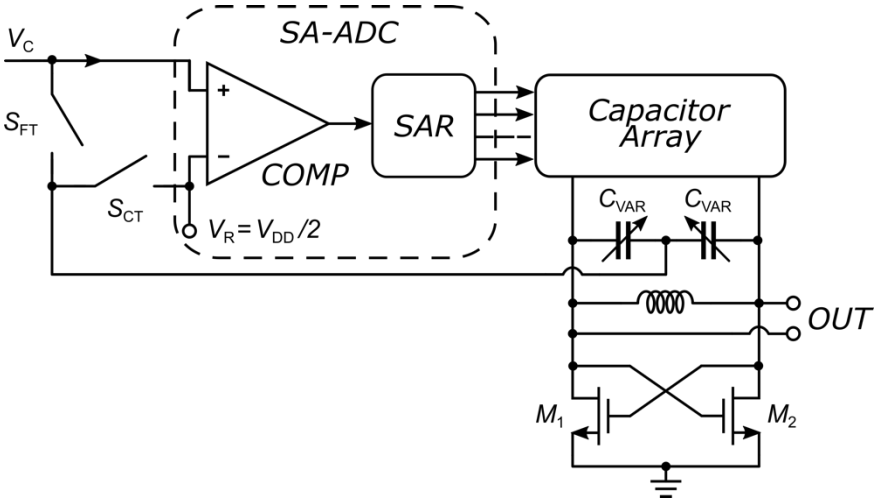


Figure 4.5. A typical state of the art calibration solution.

In Figure 4.5, a typical open-loop state-of-the-art calibration approach is shown. A successive approximation ADC is used to drive a capacitor array with 2^N capacitor units and relative switches, where N is the number of bits. Specifically, calibration and tuning are performed in two different steps to avoid instability issue. In the calibration step, the PLL loop is opened (switch S_{FT} off and switch S_{CT} on) and the VCO control voltage is connected to a reference DC voltage, V_R. As a result, the varactor provides a constant capacitance and the comparison between the reference voltage, V_R, and the control voltage, V_C, provided by the CP, is performed. Consequently, by enabling or disabling the unit capacitors in the SC-array, the adjustment of the tuning curve is performed. Without calibration, a very large varactor would have been required leading to high noise

and high-power consumption. In the tuning step, the PLL loop is closed (switch S_{FT} on and switch S_{CT} off) and the varactor is connected to control voltage V_C thus providing the tuning capability within the calibrated curve.

Although a lot of solutions are available in literature, which can be adapted for a start-up calibration, a simple approach is here discussed that guarantees both low area occupation and low power consumption. A block diagram of the proposed calibration circuit is shown in Figure. 4.6 along with the PLL forward building blocks.

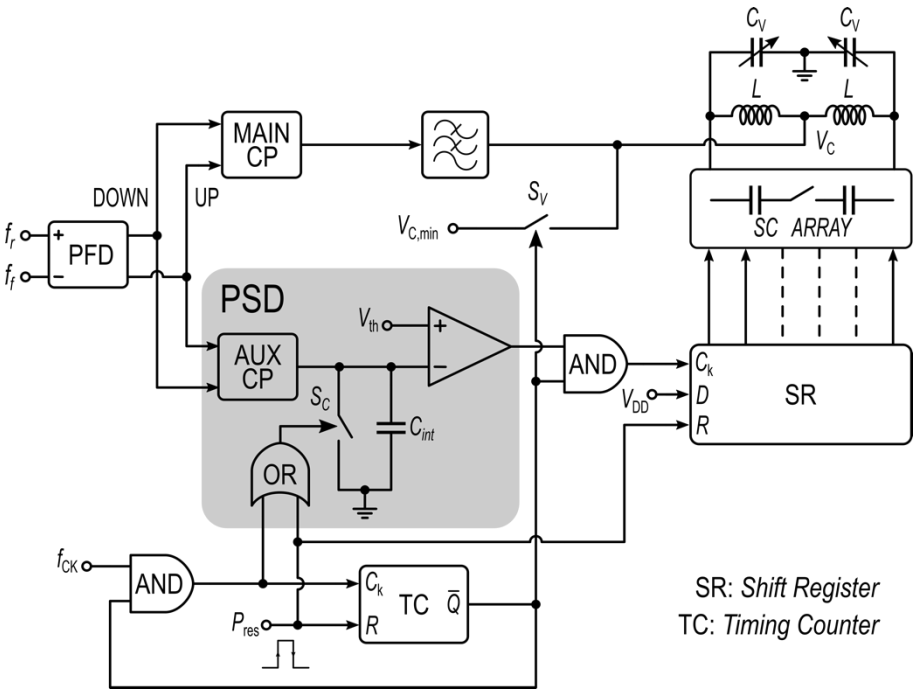


Figure 4.6. Proposed calibration strategy.

The main operation of the circuit is carried out by the pulse stream detector (PSD), which is performed through an integration approach to guarantee robustness. The PSD is mainly composed of an auxiliar charge pump (AUX CP), an integration capacitor, C_{int}, a reset switch, S_C, and a threshold comparator. The calibration circuit uses SC-array whose capacitors are selected by the parallel output of a shift register (SR).

At the beginning of the calibration imposed by the reset pulse, P_{res}, all the switches of SC-array are open and the contribution to tank capacitor is only due to the varactor that is biased to give the minimum capacitance. To provide this biasing, control voltage V_C is connected to a fixed voltage, $V_{C,min}$, of a resistor string through switch S_V. Moreover, the loop division factor, N, during calibration is set for the maximum output frequency, $f_{O,max}$

(i.e. $f_O=f_{O,max}=Nf_r$). In such a condition, the PLL loop is open and the oscillation frequency is higher than $f_{O,max}$, regardless process tolerances being the tank capacitance very small. Therefore, the PFD output is a sequence of UP pulses since the PLL attempts to increase V_C and hence the tank capacitor to reduce the output frequency.

The calibration is hence performed by adding a proper number of unit capacitors in parallel to the varactor until the oscillation frequency will become slightly lower than $f_{O,max}$, thus changing the pulse stream at the PFD output from UP to DOWN pulses.

Reset pulse P_{res} that starts the calibration cycle is generated at the PLL start-up. This pulse performs a first discharge of C_{int} and also resets both SR driving the capacitor array and the timing counter (TC) that sets the maximum calibration time. TC enables the SR clock input during the calibration time.

The integration of the current pulses of the auxiliar CP into capacitor C_{int} is controlled by a master clock, f_{ck}. Specifically, when f_{ck} is low C_{int} is charged by the auxiliar CP. As soon as the voltage across C_{int} reaches the threshold voltage, V_{th}, the comparator output goes high and charges SR with a bit 1. This bit appears in the SR parallel output driving a cell of the capacitor array and inserting a unit capacitor in parallel to the varactor. When clock f_{ck} goes high, it discharges C_{int}, and a new integration cycle is enabled. The integration is repeated until the f_O becomes slightly lower than $f_{O,max}$ and PFD output switches from UP to DOWN pulses. In such a condition, capacitor C_{int} is no longer charged, the comparator remains low, and the bits in the shift register are frozen. As soon as the timing counter reaches the maximum time allocated for the calibration, the counter and the SR clock signal are disabled, switch S_V opens thus closing the PLL loop, the auxiliar and main CPs are turned OFF and ON, respectively, and the PLL is ready to operate.

Differently from the main CP whose pulse widths depend on the phase difference at the PFD input, the auxiliar CP has been designed to perform output pulses with minimum width of around 2 ns. This is mandatory for the prediction of the maximum calibration time.

Considering that the PLL reference frequency has been set to 100 MHz and that the values of the current pulse amplitude of the auxiliar CP, the integration capacitor, and

comparator threshold voltage are 5 µA, 0.8 pF, and 300 mV, respectively, the maximum duration of a single integration step is about 250 ns. To guarantee correct operation of the PSD, the comparator switching instant must fall before the clock rising edge, which means an integration time lower than half clock period. Since the integration time changes with PVT variations, the clock period has been safely set four time higher (i.e., 1 µs). Therefore, the maximum calibration time to enable the 16 elements of the SC array is hence around 16 µs.

Alternatively, the proposed calibration strategy can be realized in a fully digital implementation, replacing the PSD with a digital integrator as illustrated in Figure 4.7.

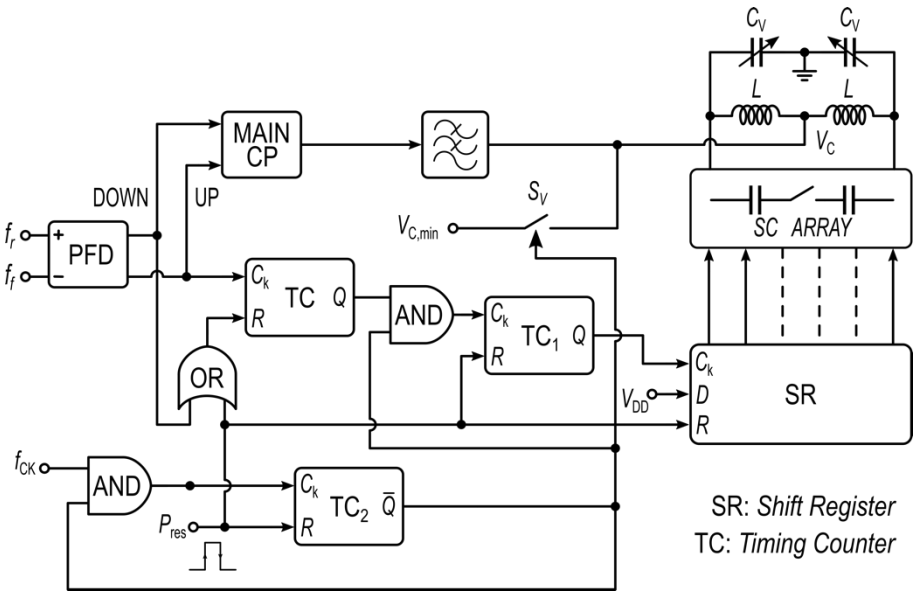


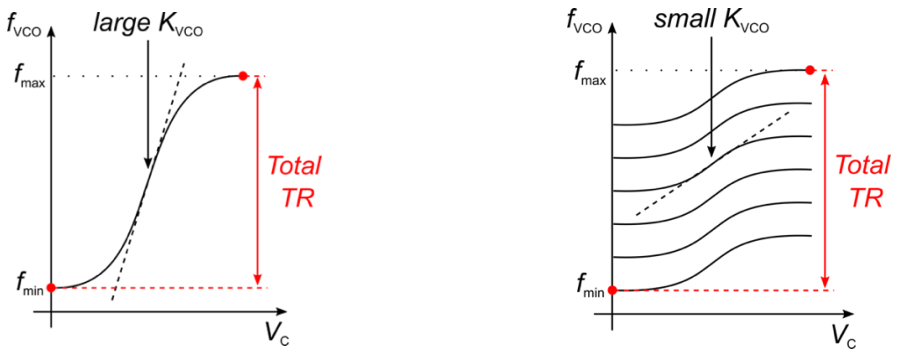
Figure 4.7. Digital implementation of the proposed calibration strategy.

The operating principle is almost identical to that seen in the previous implementation. The calibration starts with the reset pulse, P_{res}, provided at the PLL start-up, which close switch S_V, biasing the varactor to the minimum capacitance and resetting both SR and TC_2. In such a condition, the PLL loop is open, and the oscillation frequency is higher than $f_{O,\,max}$. Unlike the previous implementation, here the sequence of UP pulses provided by PFD is exploited to advance the time counter TC_1, which drives the SR to add unit capacitors in parallel to the varactor.

4.5. A Dual-Band mm-wave VCO for automotive radar applications

In a typically *LC*-tuned VCO design, frequency tuning range requirements are accomplished using varactors. In particular, accumulation-MOS (A-MOS) varactors are widely used in CMOS mm-wave systems, due to their superior performance at higher frequencies [25]. However, as the power supply decreases the varactor size grows up to preserve the desired tuning range, thus increasing losses and parasitic capacitances in the tank. As a result, PN/TR trade-off limits the use of varactors only in the *LC*-tank. In addition, a smaller tuning voltage combined with a wide tuning requirement considerably increases the VCO gain (K_{VCO}), which severely degrades the PLL phase noise and spurious performance. Indeed, a large K_{VCO} causes increased translation of noise voltage from the tuning control terminal to phase noise at the PLL output. Moreover, the VCO gain significantly varies over the wide tuning range, this, in turn, further degrades the PLL performance.

To achieve a wide tuning range with a small K_{VCO}, the targeted tuning range is usually divided into multiple sub-bands by employing both discrete and continuous tuning mechanisms as illustrated in Figure. 4.8.



(a) (b)

Figure 4.8. Method of achieving a wide tuning range with a small K_{VCO}

Accumulation-MOS (AMOS) varactors can be profitably used in CMOS technology to provide the required tuning capability inside each sub-band while the overall frequency tuning range is braked in multiple overlapped tuning curves. Such approach shows the advantage of avoiding large area varactors to cover the overall tuning range with the double benefit of increasing the tank *Q*-factor and reducing parasitic capacitances.

Several techniques have been proposed in literature to accomplish this sub-band division. The simplest solution is to employ different VCOs whose tanks are optimized to cover each of different bands [26]-[28]. As is shown in Figure 4.9, this solution employs switches to alternatively turn on and off the VCO active cores, which however can potentially affect phase noise performance besides adding parasitic capacitances.

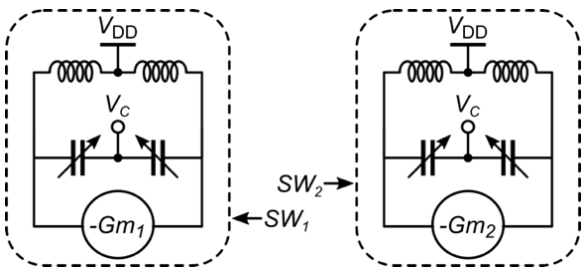
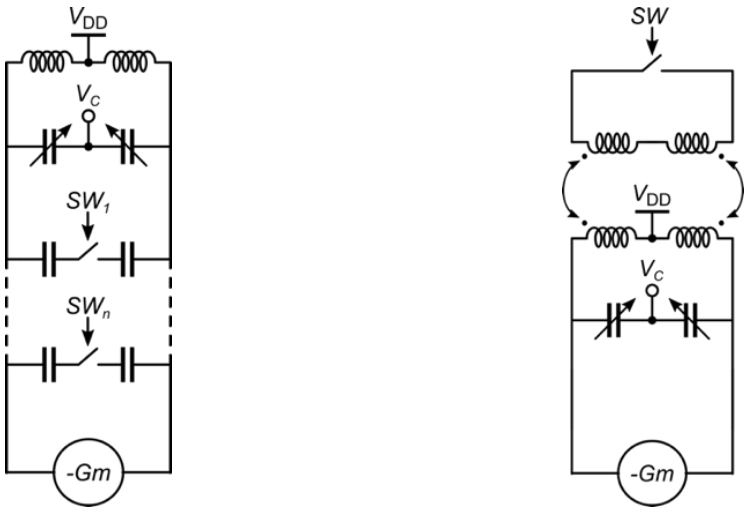


Figure 4. 9. Switched core based VCO.

The main drawback is that each sub-band requires a dedicated *LC*-tank, thus leading to a very high silicon area occupation. Furthermore, using multiple VCOs, that are connected to the same PLL circuitry, results in a high layout complexity, which can make interconnections a very critical issue.

SC-arrays enable a large number of sub-bands with a single tank inductor. They are employed for a coarse frequency calibration [24], [28]-[31], leaving the fine tuning to a small varactor as sketched in Figure 4.10 (a).



(a) (b)

Figure 4.10. (a) SC-based VCO. (b) Switched-inductor based VCO.

However, since the same varactor is used for each sub-band, it must be designed to cover the wider tuning range. For instance, the sub-bands for the automotive radar application are unbalanced in width and hence the varactor should be sized to cover the wider bandwidth of 4 GHz required by the SRR operation mode. This results in an oversized varactor for the LRR operation mode, where only 1 GHz bandwidth is required, leading to additional losses that limit the PN performance. To address this issue, a smaller varactor can be used at the cost of an increased design and layout complexity due to additional control circuits [24], [29].

Alternatively, magnetic-tuning technique can be profitably used to enable multi band operation. In this solution, a transformer is used for the tank, whose primary and secondary coils are connected to the active core and a parallel switch, respectively, as illustrated in Figure 4.10 (b). By opening and closing this switch, the equivalent inductance at the transformer primary coil can be varied, thus implementing the two sub-bands required by the automotive radar sensor [32].

However, a large switch is needed to preserve the tank Q-factor and the consequent increase in the parasitic capacitances limits the operative frequency, especially at mm-wave frequencies. Moreover, also in this case the use of the same varactor to cover each sub-band limits the PN performance resulting in a non-optimized solution.

To adopt an optimized varactor size for the two sub-bands using a single tank inductor, the solution illustrated in Figure 4.11 has been proposed.

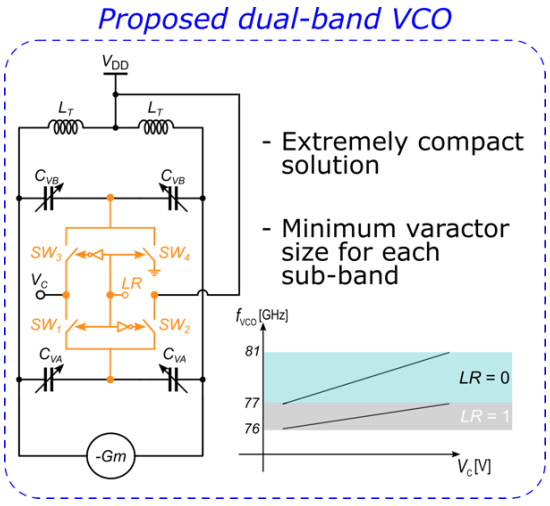


Figure 4.11. Proposed dual-band VCO.

The solution is suitable for the dual-band VCO for automotive radar sensors, since it enables a dual-band operation (i.e., both SRR and LRR band) thanks to four switches ($SW_{1\text{-}4}$) and two A-MOS varactors (C_{VA} and C_{VB}). The varactors can be sized using the minimum value required by each sub-band, thus avoiding additional losses of typical state-of-the-art solutions based on unbalance sub-bands. Figure 4.12 (a) and (b) show the two configurations determined by the switches for the LRR and SRR operation modes, respectively. By properly setting the control bit, LR, the common-mode terminal of one of the two varactors is biased to V_{DD} and gives a negligible contribution, whereas the other varactor is connected to control voltage V_C and determines the operating sub-band. Since, in the adopted configuration, switches are connected at the common-mode node of the varactors, their losses do not impact the tank Q-factor and hence PN degradation is avoided. For the same reason, switch parasitic capacitances are not involved in the LC-tank and hence they do not limit the oscillation frequency allowing a more relaxed switch design.

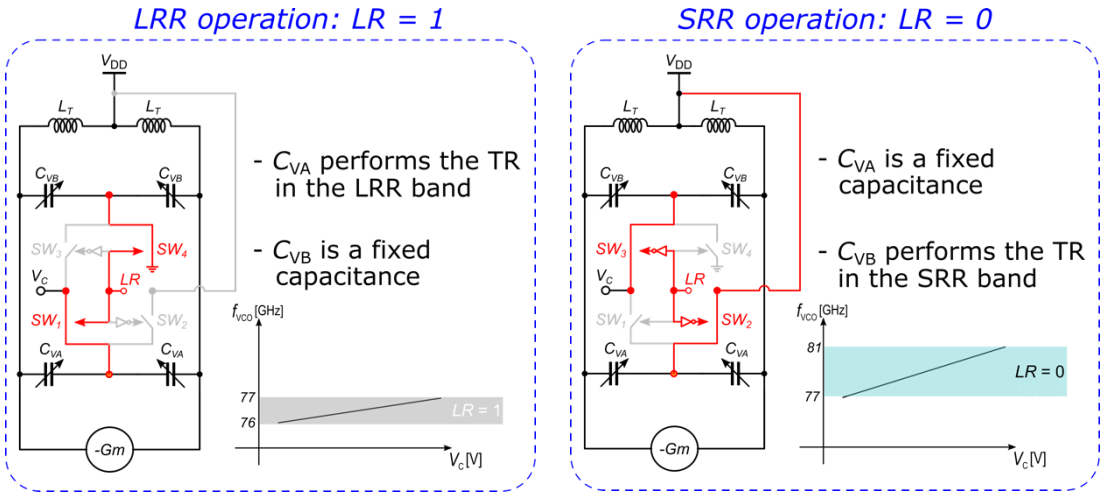
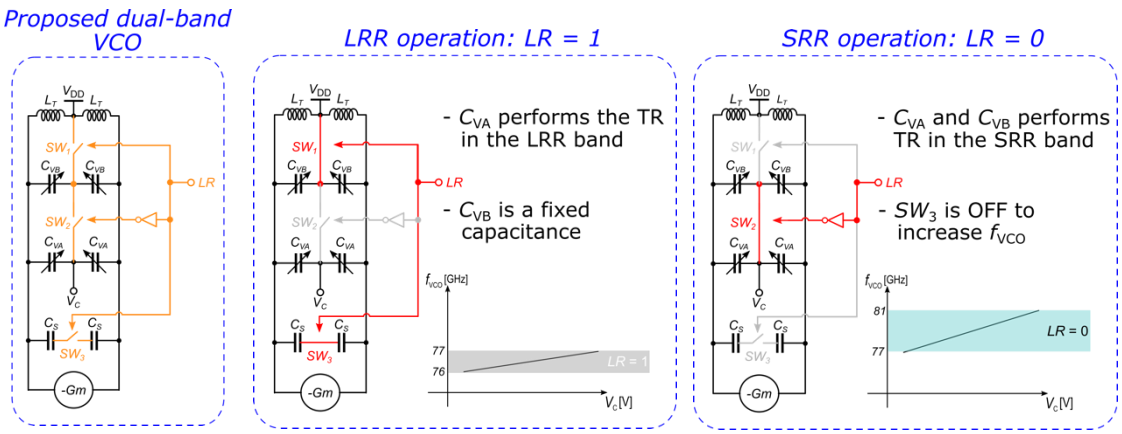


Figure 4.12. Proposed dual-band VCO in (a) LRR operation mode and (b) SRR operation mode.

To further decrease C_{VB} size, an alternative implementation of the proposed solution can be achieved by introducing a small switched capacitance, as illustrated in Figure 4.13 (a).



(a) (b) (c)

Figure 4.13 (a) Alternative implementation of the proposed dual-band VCO in (b) LRR operation mode and (c) SRR operation mode.

Unlike the previous implementation, here C_{VA} is always connected to V_C, hence it is involved in the tuning capability of both sub-bands, while C_{VB} is enabled or disenabled by two switches (SW_1 and SW_2), which modify its common-mode node DC voltage. Indeed, when the LRR operation mode is selected (i.e., LR = 1), C_{VB} is biased to provide the minimum capacitance by closing SW_1, which connects the common-mode node of the varactor to V_{DD}. The required TR in the LRR operation mode is provided only by C_{VA} and hance it can be sized to optimize the PN performance. However, the capacitance provided by C_{VB} does not allow the lower sub-band to be achieved, which calls for a higher capacitance. To this aim, a small capacitance driven by switch SW_3 is introduced as sketched in Figure 4.13 (b).

As soon as LR goes high, SW_3 is closed providing the capacitive contribution required to reach the LRR operation mode band. Conversely, in the SRR operation mode (i.e., with LR = 1), the contribution of the switched capacitance is disabled by opening SW_3 while varactor C_{VB} is placed in parallel with C_{VA} by closing SW_2. as is shown in Figure 4.13 (c). Consequently, the tuning range required in the higher sub-band is provided by both C_{VA} and C_{VB} resulting in a lower size for C_{VB} compared to the previous implementation.

4.5.1. Circuit Description

Figure 4.14 shows the schematic of the proposed dual-band VCO along with the adopted calibration circuit.

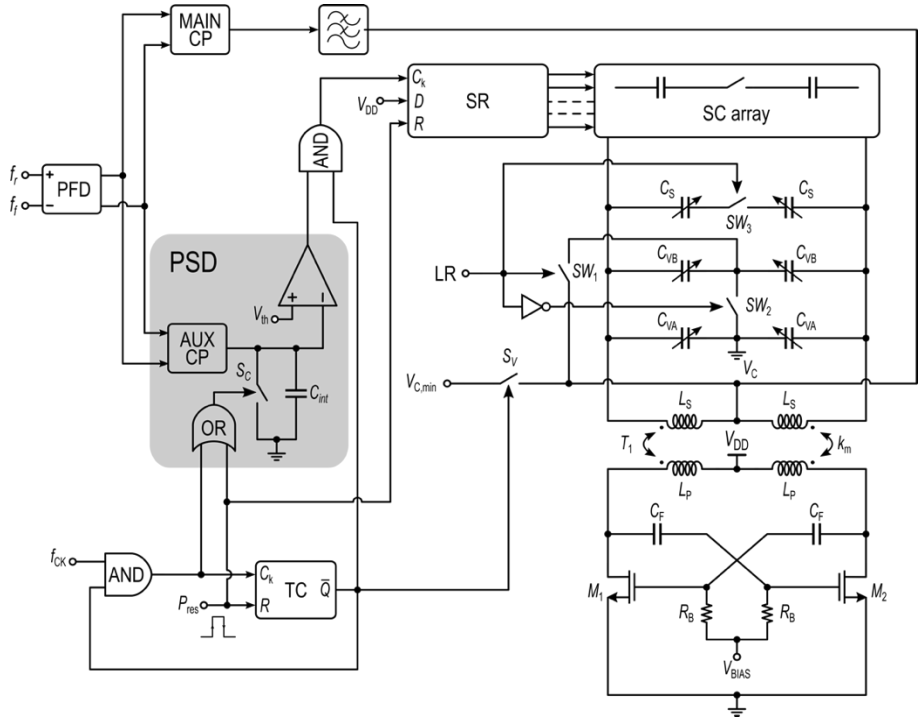


Figure 4.14. Schematic of the proposed dual band VCO.

It consists of a transformer-coupled resonator tank, T_1, with a fundamental oscillation frequency of 38 GHz. The desired tuning range is accomplished in the LRR and SRR band by the A-MOS varactor C_{VA} and C_{VB}, respectively, enabling the dual-band operation through two switches (SW_1 and SW_2) along with a switched capacitor, C_S, driven by switch SW_3. Exploiting transformer T_1, varactors are directly connected between ground and the control terminal, and ac-coupled to the input transistor pair. This arrangement preserves maximum TR and avoids that the supply noise from being reflected on the VCO PN through the AM-to-PM conversion and the varactor non-linearity. In addition, a switched-capacitors (SC) array is introduced in parallel with the varactors to perform a calibration, which compensates for the effect of the PVT variations on the oscillation frequency, thus further relaxing the varactor size.

As far as the SC-array is concerned, 9 switchable MOM unit capacitances are used, which are designed to provide a capacitance step (ΔC) of about 2.5 fF and cover a

frequency shift until 2 GHz. According to the frequency step size provided by the calibration unit capacitor, A-MOS varactors, C_{VA} and $C_{VB,}$ have been designed to cover a frequency range slightly larger of the corresponding sub-bands, thus providing enough frequency variation to cover their respective bands continuously. The varactor control voltage, V_C, is applied to the center tap of the transformer secondary coil to correctly drive the varactors while their common-mode nodes are connected to ground. In this way, the larger parasitic capacitance of the varactors does not affect the oscillation frequency [33]. In addition, the varactor Q-factor is maximized by choosing minimum length and width for the MOS varactors. MOM capacitances in the SC-array are implemented without the lower copper metal layer to reduce the parasitic capacitance toward the substrate. Furthermore, a dedicated calibration strategy based on an analog integrator has been used to drive the NMOS switches of the SC-array, as described in the previous section. The analog implementation has been preferred over the digital one due to its simplicity, which results in lower power consumption.

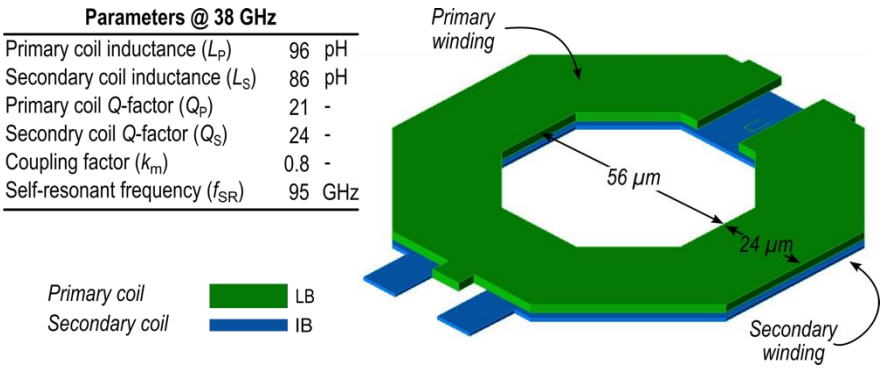


Figure 4.15. 3-D view of the transformer coupled tank, T_1.

In Figure 4.15, a 3-D view of the transformer-coupled tank, T_1, is shown along with the adopted metal stack and its main electrical parameters. The transformer has been chosen to have a 1:1 turn ratio and it is laid out using a single-turn octagonal winding stacked configuration with a 24 µm metal width and an inner diameter of 56 µm. Since the overall tank capacitance is placed in parallel with the primary winding is very small, the oscillation frequency is mainly determinate by the secondary side of the transformer, thus the secondary coil inductance has been chosen accordingly (i.e., if $C_1 \ll C_2$, then $\xi \gg 1$ and $\omega_L \approx \omega_2$). To ensure a high Q-factor at the oscillation frequency, the transformer secondary winding has been implemented on the top aluminum metal layer, LB, while the primary winding, which Q-factor is less critical, has been implemented on

the upper metal layer, IB. The advantage of this choice is twofold, as it allows a high magnetic coupling factor and a reduced parasitic capacitance toward the substrate at the same time. Moreover, neither polysilicon nor metal patterned ground shield (PGS) has been used in the transformers design, since it has a negligible impact on substrate losses at mm-wave frequencies while significantly reduces the self-resonant frequency [34], [35].

Regarding the oscillator active stage, it has been implemented by exploiting a NMOS cross-coupled pair, $M_{1,2}$, where the gate nodes are ac-coupled to the drains by relative large capacitors (around 350 fF) and a dc biasing is supplied through 3 kΩ resistors. A careful design of the transistor layout is essential to minimize parasitic effects, such as the gate resistance and gate-to-drain parasitic capacitances, thus performance degradation while guaranteeing a robust start-up condition. For this purpose, both EM analysis and post-layout simulations have been carried out to properly select the transistor size, whose aspect ratio has been set to 28 µm / 45 nm. Furthermore, a multi-finger transistor has been used to reduce the resistance of each transistor finger, and hence the equivalent thermal noise.

The proposed VCO has been also included in a fully integrated *W*-band transmitter along with a two-stage 77-GHz PA that it is able to deliver around 17-dBm output power when it is driven with a 0-dBm input power [36]. The required PA input signal is provided by a push-push frequency doubler exploiting the cascode topology previously described. To minimize power losses involved in the signal transfer, a stacked configuration has been preferred for the load transformer of the doubler to maximize the transformer coupling-factor. In Figure 4.16, the 3-D view of the transformer is depicted along with its main electrical parameters.

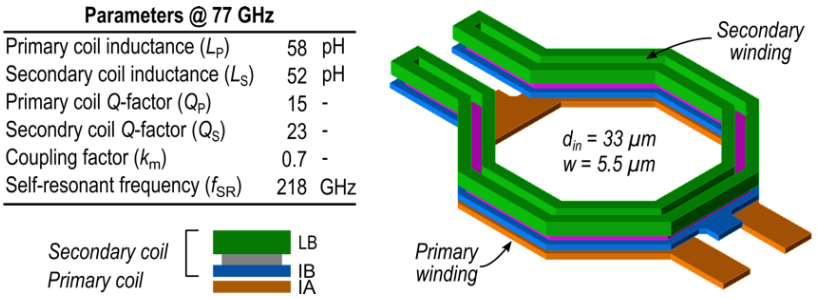


Figure 4.16. 3-D view of the frequency doubler transformer load.

A 38-GHz buffer loaded by a three-way transformer, T_{BUFF}, is used to drive the frequency doubler and the PLL prescaler with the VCO output signal, at the same time. Specifically, the primary winding of T_{BUFF} provides the buffer with the proper resonant load, whereas its secondary windings split the VCO output signal to the doubler and prescaler inputs, while providing a voltage gain, according to the adopted turn ratio.

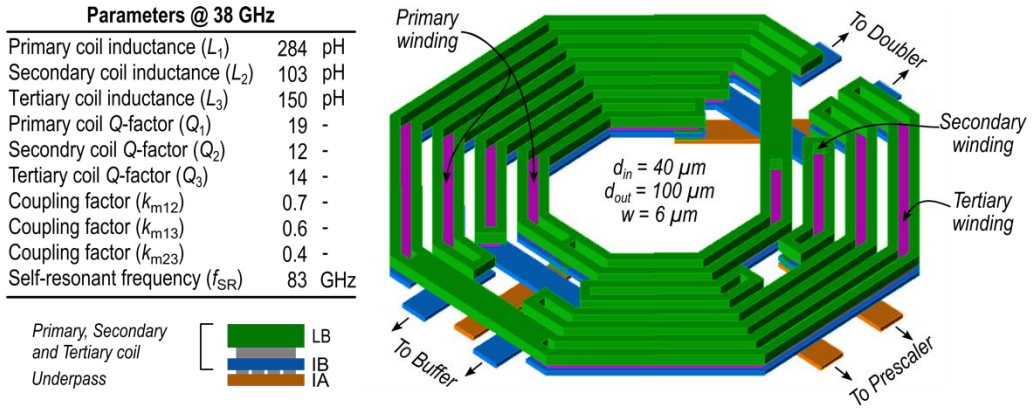


Figure 4.17. 3-D view of the buffer three-way transformer load.

In Figure 4.17, a 3-D view of the three-way transformer, T_{BUFF}, is shown along with the adopted metal stack and its main electrical parameters. The transformer has been implemented by adopting an interleaved configuration and exploiting the upper copper metal layer, IB, and the aluminum layer, LB, for the windings, while the copper metal layer, IA, has been used for the underpass. Furthermore, the primary winding has been designed with a two-turn coil to optimize both TCR and transformer coupling-factor.

Minimum channel length and optimum current density have been used for transistors of both frequency doubler and 38-GHz buffer to achieve the maximum f_T. In addition, neutralization capacitors have been adopted in the design of the 38-GHz buffer to compensate for transistor gate-to-drain capacitances. This results in a higher input/output isolation, thus improving frequency stability and gain performance. Furthermore, the neutralization technique prevents the buffer equivalent input capacitance from being increased by the Miller effect, thus leading to a lower capacitive load for the VCO.

4.5.2. Simulation results

The proposed dual-band VCO has been embedded within a PLL designed for testing purposes, which uses an off-chip second-order loop filter (LPF). Integrated switches SW_1, SW_2 and SW_3 are externally driven to select the operation mode. The integrated PLL uses a frequency divider by 384, which leads to a reference frequency of around 100 MHz. The current consumptions of the VCO and 38-GHz buffer are 24 and 3.2 mA, respectively, from a 1-V supply voltage, while the frequency doubler draws a 4.1 mA from a 2-V supply voltage (i.e., the same power supply of the PA). The calibration circuit draws only about 100 µA during the calibration process and can be powered down once the VCO calibration is completed.

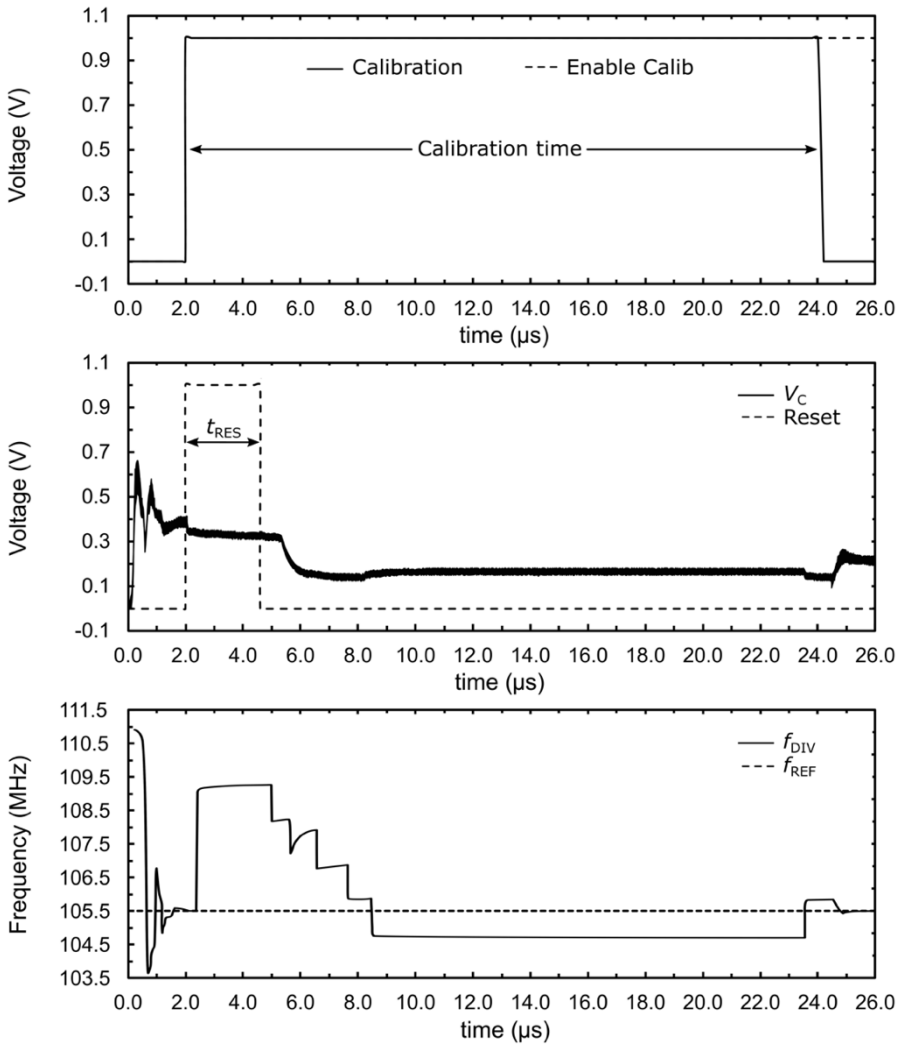


Figure 4.18. Operation of VCO calibration process.

After start-up, the PLL enters in the calibration phase when the reset pulse, P_{res}, is provided as shown in Figure 4.18. During the calibration process, the PLL is opened and the oscillation frequency becomes greater than $f_{O,max}$, since the control voltage V_C is set to $V_{C,min}$ (i.e., minimum varactor capacitance) and all the switches of the SC-array are open. Before the calibration is performed, a small reset time pre-charges the loop filter capacitance. Once the pre-charge time of the filter capacitor is over, the calibration is performed by adding a proper number of unit capacitors until the oscillation frequency becomes slightly lower than $f_{O,\,max}$. As soon as this condition happens, a unit capacitor is reinserted in the SC-array to guarantee an oscillation frequency slightly higher than $f_{O,max}$. Since the varactor capacitance is set to the minimum value during calibration ($V_C = V_{C,min}$), this condition is mandatory to allow the varactor covering all the tuning range.

In the LRR operation mode, i.e., when LR = 1, the tuning capability is achieved only with varactor $C_{VA,}$ which provides a tuning range of 0.8 GHz (i.e., from 37.9 to 38.7 GHz) when the varactor control voltage V_C varies from 0.1 to 0.9 mV. The tuning range performance is shown in Figure 4.19 along with the calculated K_{VCO}. As can be seen, K_{VCO} is almost constant within the V_C range of 0.1 to 0.9 mV, with an average value of 1 GHz/V, which reduces the PN contribution due to AM-to-PM conversion due to the varactor non-linearity.

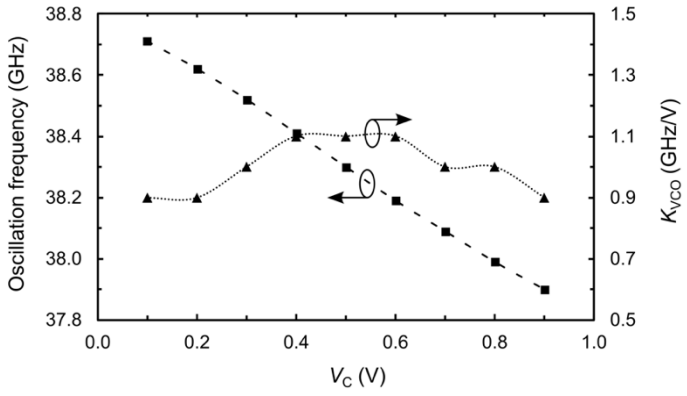


Figure 4.19. Simulated tuning range and K_{VCO} for the LRR operation mode.

On the other hands, when the SRR operation mode is chosen, i.e., LR=0, the tuning range is improved by connecting varactor C_{VB} in parallel with C_{VA} while the K_{VCO} is degraded due the larger equivalent varactor area. As shown in Figure 4.20, the resulting tuning range in the SRR operation is around 2.4 GHz (i.e., from 38.1 to 40.5 GHz) when

the varactor control voltage V_C swept from 0.1 to 0.9 mV. Unlike the LRR operation mode, here a higher and variable K_{VCO} makes the SRR operation more sensitive to the PN contribution of both CP and AM-to-PM conversion. However, it is important to highlight that each frequency tuning curve covers the frequency range of at least the chirp bandwidth since no tuning curve variation is allowed during the chirp period.

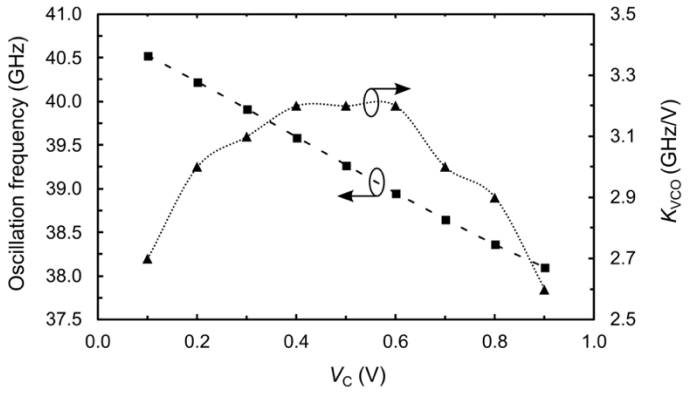


Figure 4.20. Simulated tuning range and K_{VCO} in the SRR operation mode.

To evaluate the inherent PN performance of the proposed VCO, the PLL bandwidth has been set around 20 kHz. The simulated VCO phase noise, for the LRR and SRR operation mode, at 1-MHz and 10-MHz over the overall frequency tuning range is reported in Figure 4.21 and Figure 4.22, respectively.

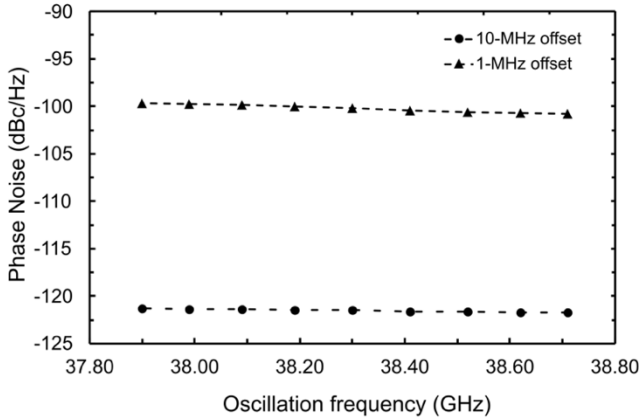


Figure 4.21. Simulated phase noise in the LRR operation mode.

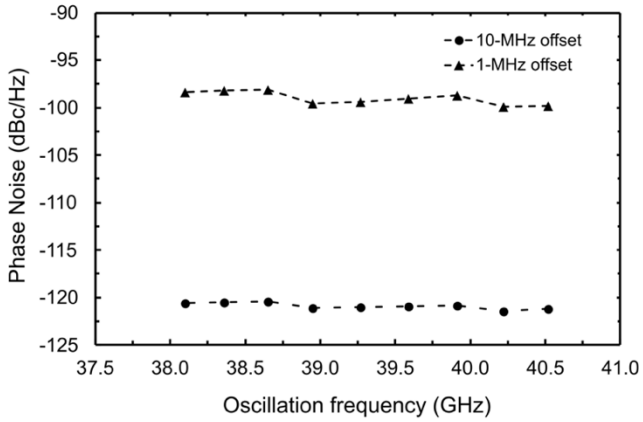


Figure 4.22. Simulated phase noise in the SRR operation mode.

As apparent, the PN in the LRR operation is quite constant across the whole tuning range, achieving the average value of −100.5 dBc/Hz and −121.8 dBc/Hz at 1-MHz and 10-MHz offset frequency, respectively. As expected, the larger varactor used in the SRR operation mode leads to a slightly worse PN performance, achieving the average value of −99.4 dBc/Hz and −120.6 dBc/Hz at 1-MHz and 10-MHz offset frequency, respectively. However, continuous coverage of the required bandwidth is a highly demanded requirement for many applications, including long- and short-range automotive radars. Conversely, PN requirements are typically less stringent for the short-range radar compared to the long-range counterpart. As a consequence, the proposed dual-band VCO is well suitable for the multi-mode radar application.

In Table 4.1, a summary of the simulated performance is provided along with the evaluated figure of merit, FoM.

TABLE 4.1.
PERFORMANCE SUMMARY OF THE PROPOSED VCO.

		THIS WORK
CMOS technology		28 nm FD-SOI
Power supply	**(V)**	1
Power consumption	**(mW)**	22 /24
Tuning approach		SC + Varactor
Center frequency	**(GHz)**	39.2
Tuning range	**(GHz)**	37.9 to 40.5
PN @ 1 MHz	**(dBc/Hz)**	-99.4 / -100.5
PN @ 10 MHz	**(dBc/Hz)**	-120.6 / -121.8
FoM[(a)] @ 1 MHz	**(dBc/Hz)**	-178 / -179
FoM[(a)] @ 10 MHz	**(dBc/Hz)**	-179 / -180

[(a)] $\text{FoM} = \mathcal{L}(\Delta f) - 20\log(f_0/\Delta f) + 10\log(P_{diss}/1mW)$.

As is shown, the proposed VCO provides a proper TR for the automotive radar application while exhibiting a very good PN performance at both 1-MHz and 10-MHz frequency offset. Specifically, the PN at 10-MHz offset frequency, which is the most critical PN for an automotive radar sensor, achieves the excellent value of –121.8 dBc/Hz for the LRR operation mode.

4.6. A Flash Frequency Tuning Technique for SC-based mm-Wave VCOs

Arrays of switched-capacitors (SCs) along with fully digital or analog/digital control circuits allow a large number of sub-bands for a coarse tuning calibration to be performed, while leaving the fine tuning to a very small varactor. The resulting tuning range consists of multiple frequency bands, as shown in Figure 4.23 (a). This approach has the double advantage of increasing the overall tank *Q*-factor and reducing parasitic capacitances, since it avoids the use of large area varactors. Indeed, the capacitors that are usually adopted in an SC-array exhibit lower losses and parasitic capacitances than the varactor counterpart.

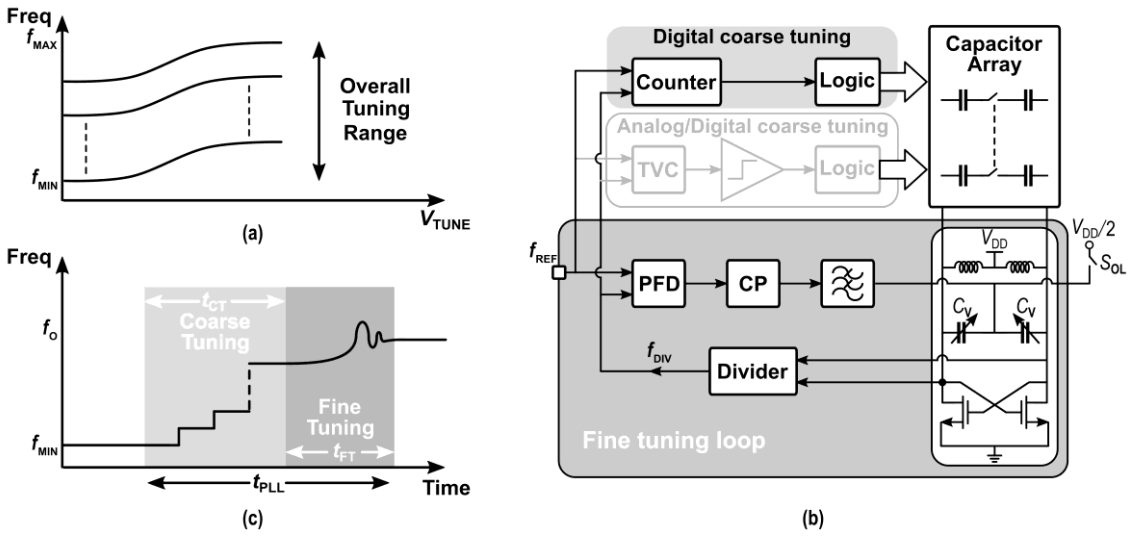


Figure 4.23. Switched capacitor based VCO. (a) Frequency tuning range. (b) Simplified block diagram of the coarse and fine tuning implementation. (c) Frequency locking transient response.

Several approaches have been proposed in literature for implementing a coarse tuning exploiting SC-array [24], [26], [29]-[31]. They can be built in a digital or in a mixed

analog/digital implementation and can operate with the PLL in closed or open loop condition. However, the closed loop approaches are affected by large delay since the PLL needs to be settled before proceeding with each calibration step, thus resulting inadequate to achieve fast lock time.

Figure. 4.23 (b) shows a simplified block diagram of an SC-based VCO with an insight of state-of-the-art open-loop frequency calibrations [24], [30], [31]. These techniques require a two-step operation to perform frequency locking. Firstly, the PLL loop is opened by means of a switch, S_{OL}, that sets the VCO control voltage to V_{DD} /2 during its on state. In this condition, reference and feedback signals are compared by means of digital counters or time to voltage converters (TVCs), which provide a relative frequency/period detection to allow the digital logic to properly operate on the capacitor array. As soon as the input frequencies, f_{REF} and f_{DIV}, are close enough, the PLL loop is closed by turning off S_{OL} and the varactors provides the fine tuning. As a consequence, the PLL settling time, t_{PLL}, is given by the time for coarse, t_{CT}, and fine tuning, t_{FT}, phases, as shown in Figure. 4.23 (c). Of course, these coarse and fine-tuning operations are separated to guarantee stability. This however is a serious drawback, especially when fast tuning is required. To combine coarse and fine-tuning operations in a single time slot, the SC-array is driven by a ΔΣ converter in [26]. However, 1 MHz RC filters are needed to prevent problems during VCO control signal transitions, thus inherently leading to low speed operation.

The large delay time of the state-of-the-art coarse-tuning techniques makes these approaches not suitable for modern applications, such as fifth generation (5G) communication networks [14] or automotive radar sensors [39], where a short settling time is an essential requirement.

To address this issue, a novel tuning strategy for SC-based VCO is presented, which overcomes the tuning delay limitations of state-of-the-art solutions, thus achieving high speed frequency locking. The proposed technique uses a flash A/D based control circuit [16], which allows coarse and fine-tuning operations to be simultaneously performed. Moreover, an automatic frequency calibration circuit [18] is designed, which operates at the start-up to compensate process tolerances on the oscillation frequency, thus maximizing the SC-array benefits. To demonstrate the effectiveness of the proposed

tuning strategy, an SC-based mm-wave VCO has been designed, which provides wide tuning range while operating at a power supply as low as 0.7 V.

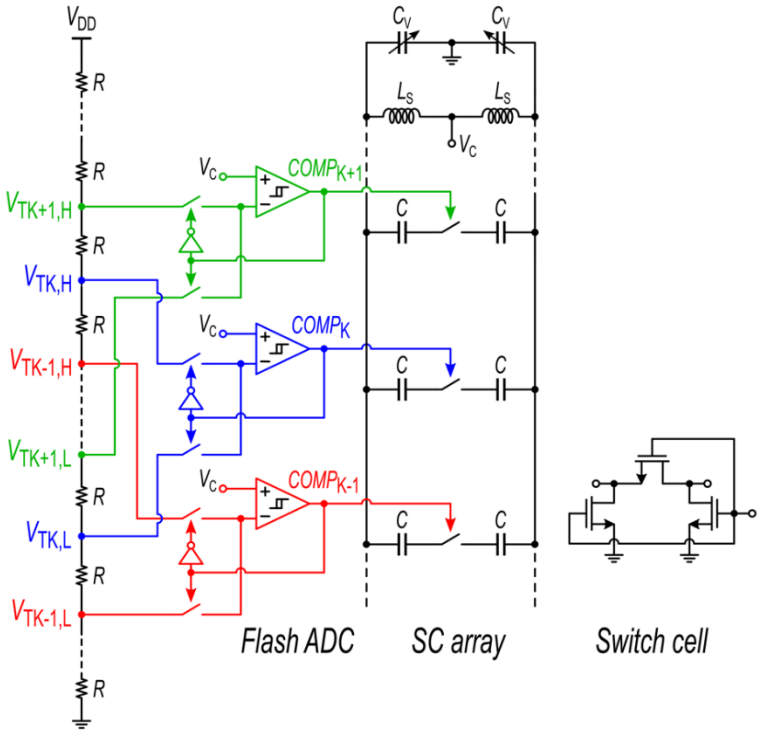


Figure 4.24. Simplified schematic of the proposed tuning strategy.

The proposed tuning circuit is shown in Figure 4.24. It is based on a flash A/D converter and a capacitor array performing a coarse frequency tuning and on a small-area varactor, C_V, for the fine tuning. The converter is implemented uses k comparators with hysteresis and a resistor string. The latter sets the comparator threshold voltages that in turn define the segments of the coarse conversion, which are properly overlapped to trade-off varactor size and supply voltage. The use of comparators with hysteresis is a fundamental feature of the proposed solution, since it guarantees a stable behavior while avoiding the need for a two-step tuning operation. This makes the coarse tuning not only fast but also suitable for those applications where a continuous tuning operation is required.

As far as the capacitor array is concerned, it is made up of high-Q MOM capacitors, C, connected to MOS switches. Each of these switches introduces parasitic capacitances, which limit frequency variation, and this leads to the use of small size switches. On the

other hand, when the switches are on, a small size gives rise to a high on-resistance, which degrades the tank quality factor and hence the phase noise.

A differential switch is used to drive the capacitances in the SC-array. It consists of a combination of three switches as shown Figure 4.24 [40]. Compared with a traditional single-ended switch with the same size, this configuration reduces the resistance in the on state by a factor of 3/2. Therefore, a reduced switch size can be used in the switch differential topology to achieve the same on-resistance but with a lower parasitic capacitance, thus reducing the effects on the tuning range.

Each element of the array is driven by a comparator and provides an equivalent unit capacitor, C_U, equal to *C/2*. Assuming that the high and low threshold voltages of the *k-th* comparator are $V_{Tk,H}$ and $V_{Tk,L}$, respectively, the varactor is sized to guarantee the following condition

$$C\left(V_{T,kH}\right) - C\left(V_{T,kH}\right) > C_U \tag{4.1}$$

that is required to achieve fine tuning within the coarse tuning segments.

The tuning circuit works as follows. As soon as control voltage V_C reaches the value of threshold voltage $V_{Tk,\,H}$, the *k-th* comparator switches high and a unit capacitor, C_U, is placed in parallel to the varactor, thus increasing the overall tank capacitor. After comparator switching, control voltage V_C will continue increasing toward $V_{Tk+1,\,H}$ or will decrease toward $V_{Tk,\,L}$, depending on the PLL output frequency, f_O. Specifically, if f_O after switching is, for instance, higher than the value imposed by the PLL reference and divider, V_C will go higher than $V_{Tk,\,H}$ and if it reaches $V_{Tk+1,\,H}$ a further unit capacitor is added in parallel to the varactor. If instead f_O is close to its steady-state value, this means that $V_{Tk,\,H}$ is the coarse conversion of V_C, which will settle around $V_{Tk,\,H}$ according to the condition:

$$V_{Tk,L} < V_C < V_{Tk+1,H} \tag{4.2}$$

thanks to the varactor that performs the fine frequency tuning. It is worth mentioning that the comparator hysteresis along with the condition in (4.1) are key concepts for the stability in this tuning strategy. Specifically, without hysteresis, control voltage V_C and

hence the PLL output frequency would oscillate around the steady-state value defined by the coarse conversion. Actually, hysteresis enables flash A/D converter and allows fast discrete coarse tuning and continuous fine tuning to be simultaneously achieved without additional delay. Compared with standard tuning approaches using only varactors, the proposed technique needs a much smaller varactor. On the other hands, the varactor size is instead slightly larger than conventional SC-based tuning approaches. However, the varactor K_{VCO} is quite low and almost constant, which is important to avoid amplification of the charge pump noise and to preserve noise performance over frequency variation, respectively.

4.6.1. Circuit Description

Figure 4.25 shows the schematic of the proposed VCO. It consists of an ac cross-coupled pseudo-differential transistor pair whose load is the primary winding of the transformer, T_1. The secondary winding of T_1 implements the tank inductance. The fundamental oscillation frequency has been set to 38 GHz and to meet the desired tuning range, a combination of a small accumulation-MOS (A-MOS) varactor, C_V, used for fine tuning and an SC-array, for coarse tuning and calibration, has been used in this design. Due the ac-coupling provided by transformer T_1, the common-mode node of the varactors has been set to ground to preserve varactors from the supply noise as previously discussed [41].

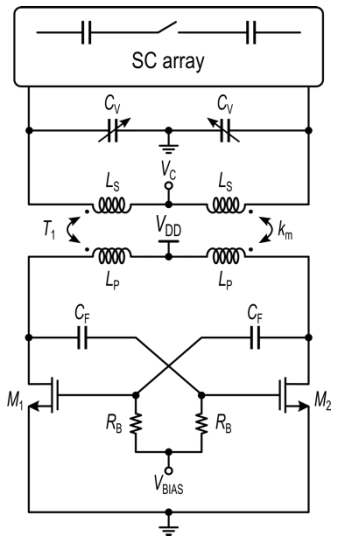


Figure 4.25. Simplified schematic of the proposed mm-wave VCO.

As far as the SC-array is concerned, 9 switchable MOM capacitances are used for coarse tuning purpose, which are designed to provide a capacitance step (ΔC) of 2 fF to cover about 3.5 GHz of the frequency tuning range (corresponding about to the 9.2% of TR). A-MOS varactors are sized to provide enough frequency variation, thus avoiding gaps in the tuning range between the digital capacitor bank states. To compensate the effect of the PVT variations on the frequency oscillation, further 16 switchable MOM capacitances are added to the SC-array. Unlike the previous ones, here the unit capacitance has been sized to guarantee a ΔC of 2.5 fF, which compensates for frequency shift until 2 GHz. Both tuning and calibration capacities are switched by a NMOS switches through dedicated strategies, which have been explained in detail in the previous subsections. According to previous considerations, the switches are sized to preserve tank quality factor while avoiding an excessive contribution of parasitic capacitances.

The VCO was designed in a 28-nm FD-SOI CMOS technology, which uses a general-purpose low-cost back-end-of-line (BEOL) consisting in eight copper metal layers, whose thicker ones are the last two (referred as IB and IA) and an aluminum metal layer (LB) at the top of the stack.

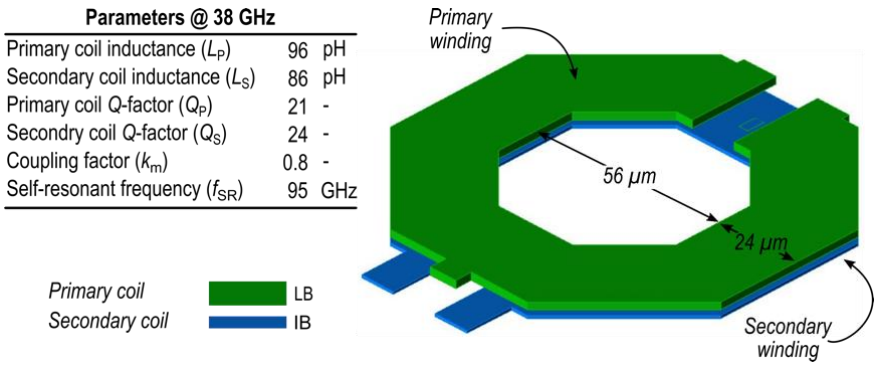


Figure 4.26. 3-D view of the transformer coupled tank, T_1.

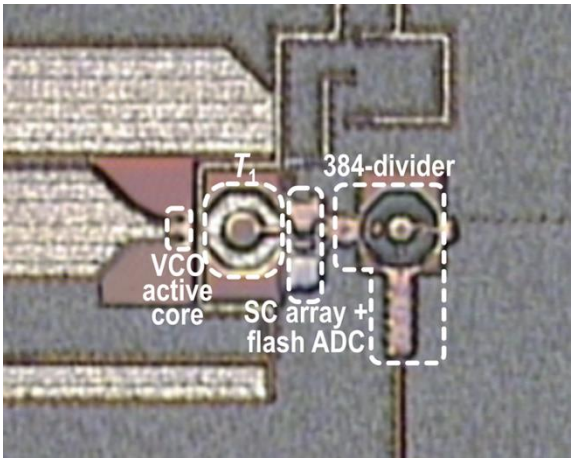
Figure 4.26 shows a 3-D layout view of the transformer-coupled tank, T_1, along with the adopted metal stack and its main parameters. The transformer has been designed with a single-turn octagonal winding stacked configuration with a 24 µm metal width and an inner diameter of 56 µm. The turn ratio has been set to 1. To guarantee a high Q-factor at the oscillation frequency, the transformer secondary winding has been implemented on the top aluminum metal layer, LB, while the primary winding uses the upper metal layer, IB. Moreover, neither polysilicon nor metal patterned ground shield (PGS) have

been used, since it has a negligible impact on substrate losses at mm-wave frequencies but significantly reduces the self-resonant frequency [34] [35].

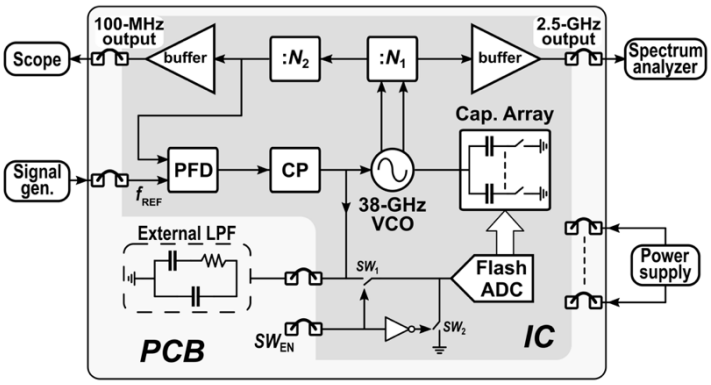
Transformer secondary coil is connected to the SC-array by exploiting the upper metal layers, LB and IB, to minimize both resistive and reactive parasite introduced by the interconnections. The MOM capacitances that make up the SC-array do not use the lower copper metal layer to reduce parasitic capacitances toward the substrate.

4.6.2. Experimental Results

The die microphotograph of the proposed VCO is shown in Figure 4.27 (a). The VCO has been fabricated in 28-nm CMOS FD-SOI process and occupies a core area of 210 µm x 150 µm.



(a)



(b)

Figure 4.27. (a) Die microphotograph. (b) Simplified block diagram of the measurement setup.

Figure 4.27 (b) shows the adopted measurement setup. The VCO was embedded within an on chip PLL designed for testing purposes, which uses an off-chip second-order loop filter (LPF). Integrated switches SW_1 and SW_2 are externally driven to enable/disable the SC-array. The integrated PLL exploits a frequency divider by 384, which leads to a reference frequency of around 100 MHz. The measurement setup includes a spectrum analyzer and a digital oscilloscope for spectrum and transient measurements, respectively. A signal generator was also used to generate the PLL input reference signal.

Measurements were performed at 0.7 V power supply. The current consumptions of the VCO, PFD/CP and dividers are 12, 0.6, and 28 mA, respectively, while the two testing buffers draw 3.2 mA.

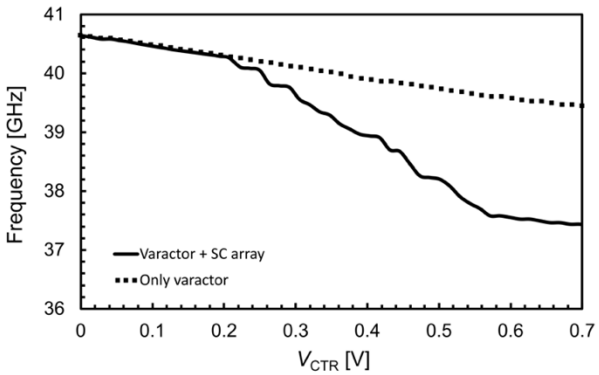


Figure 4.28. Measured tuning range.

Figure 4.28 depicts the measured VCO tuning range. The oscillation frequency ranges from 37.4 to 40.7 GHz, when varactor control voltage sweeps from 0 to 0.7 V. For the sake of completeness, the tuning range provided only by the varactor (i.e., tuning array disabled) is also reported. As apparent, the varactor performs a small fraction of the overall tuning range, which instead is mainly achieved thanks to the SC array.

Figure 4.29 shows the VCO frequency transient response. The PLL bandwidth was set to 5 MHz and a frequency step from 97.6 MHz to 105.6 MHz was applied to the PLL reference. Under these conditions, the VCO frequency settles in about 0.2 µs, which is the overall PLL locking time including both array and varactor operation. Consequently, the PLL time response is not affected by delay limitation and/or stability problems caused by the proposed tuning strategy, even with a large PLL bandwidth.

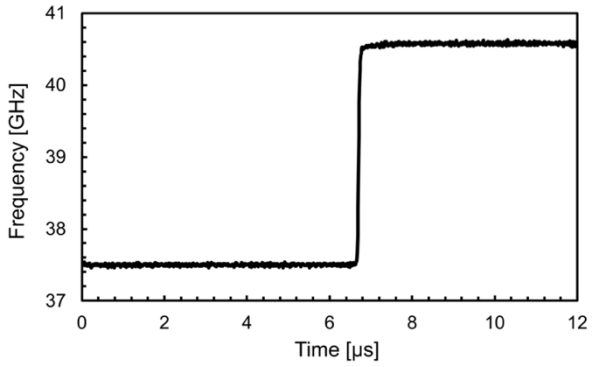


Figure 4.29. Transient response of the VCO oscillation frequency.

Figure 4.30 depicts the measured VCO frequency waveform for a frequency modulated reference signal with a triangular shape. which is typically adopted in automotive radar sensor applications. Specifically, a period of 40 μs with a 3 GHz bandwidth was set. As apparent, continuous-time operation with variable PLL frequency is possible. Such a dynamic response is enabled by the proposed tuning strategy based on a flash A/D converter.

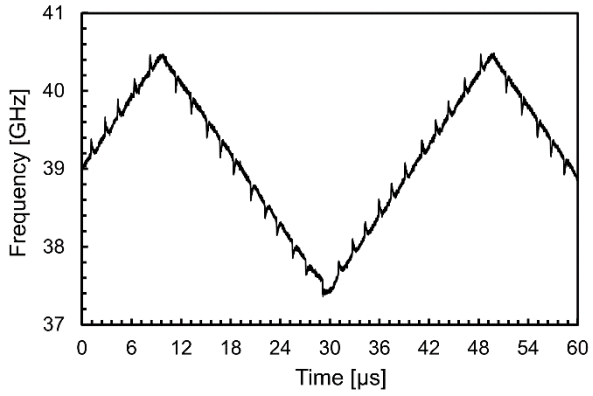


Figure 4.30. Measured dynamic frequency locking with a triangular reference frequency.

For the sake of completeness, the phase noise of the stand-alone VCO was also measured at 2.5 GHz carrier frequency and extrapolated at 39 GHz. The measurement was carried out by setting the PLL bandwidth to around 20 kHz. The measured PN is about –94 dBc/Hz at 1 MHz offset frequency.

TABLE 4.2.
PERFORMANCE SUMMARY AND COMPARISON WITH THE STATE OF THE ART.

		EK JSSC'18 [8]	MA JSSC'20 [13]	DENG JSSC'20 [42]	**THIS WORK**
CMOS technology		28 nm FD-SOI	65 nm	65 nm	28 nm FD-SOI
Power supply	**(V)**	1.2	1	1	0.7
Power consumption	**(mW)**	3.3	-	11.6[(c)]	8.4
Tuning approach		SC + varactor	SC + varactor	SC + Varactor	SC + varactor
Center frequency	**(GHz)**	18	39.6	20	39
Tuning range	**(GHz)**	16.3 to 19.7	37.2 to 42	17.4 to 22.4	37.4 to 40.7
PN[(a)] @ 1 MHz	**(dBc/Hz)**	-92.3[(b)]	-93.4[(c)]	-96.9[(c)]	-94
Calibration extra time		YES	YES	YES	NO

[(a)] Normalized around 39 GHz. [(b)] Simulated. [(c)] Overall PLL.

The overall measured performance is summarized and compared with recent state of the art mm-wave CMOS VCOs in Table 4.2. The proposed solution does not suffer from the additional delay of conventional coarse tuning techniques based on SC-arrays. Moreover, the VCO exhibits a phase noise and tuning range that are similar to state-of-the-art SC-based VCOs, despite a lower power supply.

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Appendix A

Publications

A. Patents

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D. Courses

1. “Topic on Microelectronics (ToM) 2021/1 — XV year,” Italy, from May 25th to May 27th, 2021.
2. “Topic on Microelectronics (ToM) 2019/2 — XIII year,” in Milan, Italy, from September 10th to September12th, 2019.
3. “BCD DAYS 3.0,” in Catania, Italy, from May 07th to May 09th, 2019.

Conclusion

In this work, two novel approaches aimed at improving the oscillator tuning range without impairing the phase noise performance have been proposed, which are suitable for mm-wave VCOs in a very scaled CMOS technology. Both approaches reduce the varactor size allowing the desired tuning range in two or more sub-bands to be achieved, while also addressing the sub-band PVT frequency variations through a novel calibration strategy performed during the PLL start-up. In addition, the proposed VCOs have been embedded in a sub-harmonic PLL where a novel push-push frequency doubler has been implemented to address the high sensitivity of this circuit to the impedance supply paths.

In Chapter 1, fundamental concepts about automotive radar sensors based on the FMCW operating principle are introduced, along with the related challenges of a fully integrated mm-wave transceiver design, with special focus on frequency synthesizers. Indeed, additional challenges are posed by nanometer CMOS technologies especially in the VCO design, where the simultaneous achievement of low phase noise and wide tuning range is a non-trivial task. On the other hand, CMOS technologies are mandatory to achieve manufacturing cost reduction and system-on-chip (SoC) solutions for new-generation automotive radar sensors. This chapter also provides an overview on the adopted 28-nm FD-SOI CMOS technology by STMicroelectronics.

In Chapter 2, the design of integrated inductors and transformers for mm-wave applications are discussed. Here, a comparative analysis of three 77-GHz integrated transformers has been performed with the aim of finding out the most suitable configuration for *W*-band automotive radar CMOS applications. The comparison has shown that an interstacked configuration is suitable when low insertion loss and high *k*-factor are required. A stacked transformer achieves performance very similar to the

interstacked one with the advantage of higher primary and secondary coil inductance values for a given resonant frequency. On the other hand, interleaved configurations are most suitable configurations when a higher *TCR* is required. Since the transformer parameters are closely related to those of the adopted technology, a comparative analysis of two 28-nm CMOS technology based on standard and mm-wave-optimized BEOL is provided. To this end, a stand-alone transformer performance is first analyzed and then a testbench made up of 77-GHz down-converter for FMCW radar applications is described. Although thicker metals and intermetal oxide providing some advantage, especially for stacked configurations, mm-wave transformer performance in the optimized BEOL is affected by parasitic EM effects, which are no more negligible when the transformer size is comparable with the chip vertical dimensions. The evaluation of the 77-GHz down-converter further confirms that very limited performance enhancements can be obtained with an optimized-BEOL technology. These results question the pros and cons of more expensive and complex BEOLs for nanometer CMOS platforms, providing a different perspective on technology developments for mm-wave applications.

In Chapter 3, fundamental concepts concerning the design of mm-wave VCOs are discussed. The most meaningful phase noise models are introduced to provide the theoretical background underlying the evolution of both the most adopted *LC*-oscillator topologies and phase noise optimization approaches. The main challenges in mm-wave VCO are also discussed by pointing out the advantages of sub-harmonic PLL approaches to synthesize the desired output frequency. Based on these considerations, a first implementation of a 38-GHz VCO has been done with the aim of consolidating the proposed design flow for mm-wave transformer-based oscillators in a scaled 28-nm FD-SOI CMOS technology. This circuit exploits a transformer two-port configuration, with the aim of improving the tank quality factor. The proposed VCO exhibits an average PN as low as – 97 dBc/Hz and – 121 dBc/Hz at 1 MHz and 10 MHz offset frequencies, respectively, while providing a frequency variation of around 4 GHz. The silicon area occupation of the VCO core was 300 μm × 135 μm.

In Chapter 4, novel approaches to address the VCO design with the objective of improving the oscillator tuning range without impairing the phase noise performance have been introduced. A first approach relies on varactor-based technique to implement a dual-band VCO, which allows both long range (i.e., from 76 GHz to 77 GHz) and short

range (from 77 GHz to 81 GHz) radar operation to be achieved. It consists of a transformer-coupled resonator tank with a fundamental oscillation frequency of 38 GHz. Here, the desired tuning range is accomplished in both LRR and SRR band by means of A-MOS varactors, enabling the dual-band operation with two switches and a switched capacitor. In LRR operation, the proposed solution achieves an average PN as low as −100.5 dBc/Hz and −121.8 dBc/Hz at 1 MHz and 10 MHz offset frequencies, respectively. An average PN of around −99.4 dBc/Hz and −120.6 dBc/Hz at 1 MHz and 10 MHz offset frequencies, respectively, is obtained in SRR operation. As far as the tuning range is concerned, a continuous coverage of the required bandwidth is accomplished in both LRR and SRR operation, providing a frequency variation of around 0.8 GHz and 2.4 GHz, respectively. Unfortunately, only simulations results can be provided for this prototype since the related chip is under manufacturing.

A second approach based on a flash frequency tuning technique for SC-based VCOs has been proposed to overcome the tuning delay limitations of state-of-the-art solutions, thus achieving high speed frequency locking, which is useful in a wide range of modern frequency synthesizers. To demonstrate the effectiveness of the proposed tuning strategy, an SC-based mm-wave VCO has been designed using a transformer-coupled configuration, which provides wide tuning range while operating at a power supply as low as 0.7 V. The proposed tuning strategy is based on a flash A/D converter and a capacitor array performing a coarse frequency tuning and on a small-area varactor for the fine tuning. Here, the use of hysteresis comparators is a fundamental feature of the proposed solution since it guarantees a stable behavior while avoiding the need for a two-step tuning operation. This makes the coarse tuning not only fast but also suitable for those applications where a continuous tuning operation is required.

The fabricated VCO occupies a silicon area of 210 μm × 150 μm while providing an oscillation frequency ranges from 37.4 to 40.7 GHz, when varactor control voltage sweeps from 0 to 0.7 V. As shown by experimental results, no delay limitation and/or stability problems for the PLL come from the proposed tuning strategy, even with a large PLL bandwidth. To corroborate this behavior, a measurement test has been carried out by setting the PLL bandwidth around 5 MHz and using a frequency step from 97.6 MHz to 105.6 MHz at the PLL reference. Under these conditions, the VCO frequency settles in about 0.2 μs, which is the overall PLL locking time including both array and varactor

operations. The phase noise of the stand-alone VCO was also measured and is about – 94 dBc/Hz at 1 MHz offset frequency.

Additional improvements can be done to make the proposed VCOs more appealing, especially on the phase noise performance, which calls for dedicated strategies. The bottleneck is the effectiveness of the state-of-the-art PN optimization techniques, which requires some special care to be exploited at mm-wave frequencies. For instance, the 2^{nd} harmonic resonance technique has proven to be an effective way to reduce the flicker noise up-conversion in mm-wave VCOs but its behavior is very sensitive to the CM tank impedance, thus requiring an additional CM tuning capacitor back, which in turn limits the maximum oscillation frequency. Alternatively, the implementation of a proper feedback in the active stage aimed at minimizing the 2^{nd} harmonic level of the oscillation signal, could be a viable solution to improve the PN without impairing both tuning range and maximum oscillation frequency. However, this idea is currently only supported by simulations results, while the layout is still in progress. Further developments could include the design of improved circuit solutions for both the charge pump and frequency divider aimed at reducing the noise contribution to the phase noise and lower power consumption of the overall PLL, respectively, and finally, the integration of the proposed solutions in a complete mm-wave transceiver.