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Lumped Parameter Modelling of Internal Temperature Dynamics in Multichip Power Modules

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Abstract. This study assesses a lumped parameter modelling strategy for the fast response, layer-resolved prediction of the thermal field within the die of a selected power module device. A benchmark 1D lumped parameter model was initially defined, providing a simple description of the thermal field through the identification of a low number of lumped parameters but retaining information only on the junction temperature. A refined analytical model was therefore developed by adding the internal temperature nodes at the interfaces between the device layers. Thus, with a moderate increase of the lumped parameters, the model was able to predict the thermal behaviour of the inner layers of the die, which is the fundamental information required by reliability analysis. The set of model parameters were determined from the step-response thermal impedances of the power module, simulated by means of a numerical model purposely assessed under a boundary condition of forced liquid cooling. The lumped parameter identification consisted in a curve fitting procedure calculating the couples of thermal resistance and conductance. Both models were implemented in Matlab-Simulink, and simulated in order to predict the thermal response of the device to conditions of both step-wise and alternating current power inputs.

1. Introduction

The increasing demand of efficient and compact power electronic systems is boosting the transition from conventional silicon devices, such as silicon MOSFET and IGBT, to wide bandgap (WBG) solution in silicon carbide (SiC), such as, in particular, SiC MOSFET [1]. The latter, in fact, provides both a relevant reduction of the power losses and the high thermal conductivity and high temperature resistance of SiC, which sensibly facilitate the thermal management and the possibility to increase the maximum accepted power density [2]. Yet, high temperature reliability is still a main limitation to a wider spreading of SiC power modules in high power applications. In fact, the thermal profile expected in operation, i.e. in response to a specified duty cycle or mission profile, affects the performance and the reliability of the device in two different ways:

- the deterioration of the materials constituting the layers of the device as a consequence of either transient overloading or repeated long-term exposures to high temperature profiles, typically occurring as delamination or dielectric erosion phenomena or as gate oxide breakdown [3];

- the breakage caused by the wear-out of fragile elements, such as the bond-wire or the solder layers, subjected to the thermal fatigue [4].

Thermal fatigue is caused by cyclical mechanical stresses arising as a consequence of the different thermal expansion coefficients of the materials; thus, it is associated mainly to transient operations, such as in particular the device start-up and shut-down, but also to the thermal cycling shown by the device in response to the frequency of the feeding current during regime operations.

It emerges that the design for reliability [5] of SiC MOSFET devices requires prediction tools that must be computationally effective while properly accounting for the intrinsic time dependence of regime operations as well as of typical duty cycles [6].

Not all modelling approaches for the prediction of the temperature field are appropriate for dynamic simulations. FEM models provide accurate predictions but require high computational efforts and, above all, are excessively time-consuming for practical application in the prediction of the temperature dynamics with time-varying power inputs [7]. Models based on the direct use of experimental measurements, on the other hand, require the physical instrumentation of a reference power module, providing direct access to the required monitoring points; moreover, accurate dynamic predictions are possible only with fast response optical temperature probes, available for surface temperature detection but not for internal nodes; therefore, the use of experimental methods is practically limited just to the prediction of the junction temperature but not for that of the thermal distribution in the device layers [4]; parenthetically, a general concern is that relevant uncertainty may affect the generalization to other devices of the results achieved from the instrumented reference module.

The most effective approach for reliable and time-effective dynamical predictions is represented by lumped-parameter models. These are based on a network of thermal impedances, made up of resistance-capacitance coupled elements, able to simulate the heat flow path within the device and to predict the dynamics of the temperature at the nodes of interest, i.e. those at the layers' interfaces which are related to reliability issues.

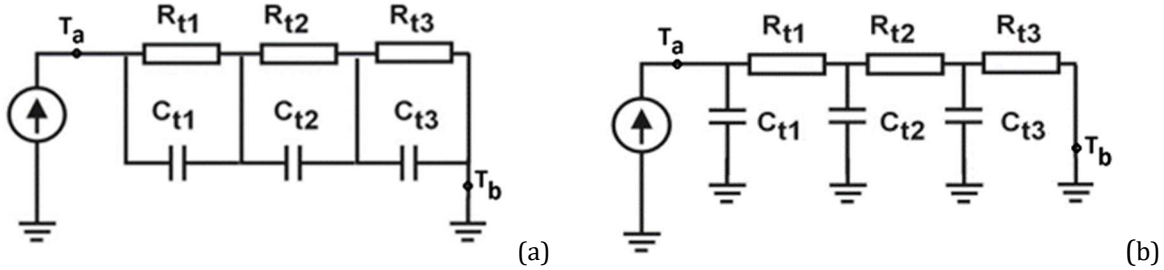


Figure 1. Lumped-parameter equivalent electric schemes of the thermal network between to temperature nodes T_a and T_b: (a) Foster network (b) Cauer network [9].

Two main approaches are used for the construction of a thermal network between two given temperature nodes, namely the Foster-type and the Cauer-type network schematized in figure 1 (a) and, respectively, (b) [8].

The thermal impedance between two temperature nodes T_a and T_b is defined as:

$$Z_{th}(t) = \frac{T_a(t) - T_b(t)}{P_d(t)} \tag{1}$$

with $P_d(t)$ instantaneous heat power crossing the branch of the network. Depending on the network order N_p, i.e. the number of poles of the impedance transfer function, Z_{th} analytically expresses the superposition of N_p thermal modes, each characterized by a time constant τ_n, produced in response to a step-wise variation of the applied P_d:

$$Z_{th}(t) = \sum_{n=1}^{N_p} R_{th,n} \cdot \left(1 - e^{-\frac{t}{\tau_n}}\right) \quad \text{with} \quad \tau_n = R_{th,n} \cdot C_{th,n} \tag{2}$$

Referring to the Foster network in figure 1 (a), the model order n and the parameters $R_{th,n}$ and $C_{th,n}$ are optimized in order to ensure a satisfactory curve fitting with the reference step-response of the device between the two nodes. While the intermediate nodes do not retain any physical meaning of intermediate temperatures, a main advantage of the approach is that the lumped parameters of the model can be easily extracted by either experimental measurements or by accurate numerical simulations of the step-response, provided that available data are satisfactorily resolved both in space and time. This explains why, being the junction and the case detectable boundary nodes, this approach is used for the junction-to-case Foster network experimentally derived by manufacturers and reported in the datasheets of commercial devices. Conversely, Foster networks between internal nodes are not easily obtained from experimental measurements but might be extracted from numerical simulations.

Referring to the Cauer network in figure 1 (b), each intermediate $R_{th,n} - C_{th,n}$ couple represents the thermal resistance and capacitance of each of the intermediate layers, calculated under the assumption of 1-D heat flow across the layer provided that the geometry and the thermophysical properties of the layers are properly assessed. Therefore, the internal nodes of the Cauer network retain the physical meaning of temperatures at the interface between layers [9]. Nonetheless, in practical applications, due to peripheral heat flows orthogonal to the main heat flow from junction to case, the validity of the assumption of 1-D heat flow is compromised; thus, the effective values of the $R_{th,n} - C_{th,n}$ couple of the Cauer network do not actually correspond to those theoretically calculated and the error introduced in the model predictions might be unacceptable. A viable solution to this problem is represented by the evaluation of the effective values of $R_{th,n} - C_{th,n}$ couples from the so-called Structure Function, SF [10]. As the SF is built up from the time constant spectrum of the junction-to-case Foster model of the reference thermal step-response, the SF-based Cauer model can be set to be more reliable.

The present study proposes the first step of assessment of a lumped-parameter thermal model of a SiC MOSFET multichip device, ACEPACK DRIVE, produced by STMicroelectronics for electric and hybrid vehicles. This is a three-phase inverter consisting of three modular legs, each made up of two switches formed by 8 dies topologically divided in two contiguous interacting quartets.

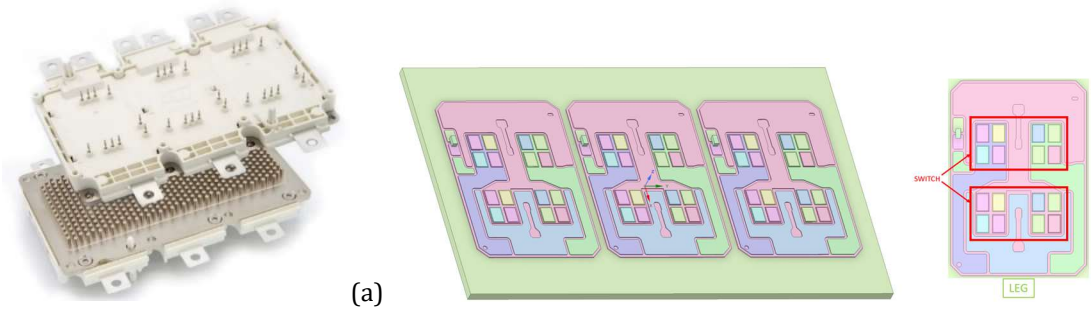
For the same power module device herein considered, a 1D thermal model was proposed in [11] providing the description of a quartet of die through a junction-to-case Foster network that accounts for the thermal coupling between dies but does not model the layers nodes beneath the dies.

The proposed lumped-parameter scheme is specifically designed for the 1-D thermal modelling of a single die with the aim of overcoming the limits of the basic junction-to-case 1-D Foster model, which is nonetheless assessed and used as a reference benchmark. With a marginal increase of the computational cost, the structure of the basic model is modified through the addition of the internal temperature nodes at the interfaces of the device layers. For both reported

models, the lumped parameters were extracted by the numerical simulations of the step-response thermal impedances of the device by means of a curve fitting algorithm. A model with such a structure represents a tool for the dynamical prediction of the temperature profile within the device layers beneath the die and is, therefore, fundamental for properly addressing the issues involved in thermal fatigue analysis. Thus, scaling the thermal network to a quartet of dies and, thereafter, to the whole set of dies, represents the future development of the model herein discussed and aims at properly modelling the time-dependent temperature distribution within the device layers.

The approach proposed in the present study is similar to that reported in [3], [4], [10], [12], where lumped-parameter models were built for multidie devices based on either Foster or Cauer subnetworks connecting *n* temperature nodes of interest within the layers of the power module.

Reported results of the proposed model, in good agreement with the numerical simulations, outline its capability of predicting the dynamics of internal interface temperatures in response to an alternative current input.



(a) (b)

Figure 2. Schematic of ACEPACK DRIVE Power Module: (a) distribution of the three-phase legs; (b) detail of a leg, formed by a couple of switches with 8 diodes each.

2. ACEPACK DRIVE SiC MOSFET device

Silicon technology is indeed the most widely used power electronic devices but it is characterized by relative low switching velocity, affecting the power losses, and by reliability issues severely increasing with the growth of power density requirement for current applications in traction inverters. In fact, the automotive sector is leading the transition towards technologies based on novel semiconductor materials, such as silicon carbide (SiC) and gallium nitride (GaN). SiC MOSFET devices possess advantageous physical properties, such as admitted maximum junction temperatures up to 600°C, as compared to 150°C of silicon devices, and high thermal conductivity, which strongly enhances the heat dissipation efficiency, both substantially reducing the limitations on the maximum power density.

Further increases of the power density are achieved with power modules with a built-in heat sink, such as the SiC MOSFET ACEPACK DRIVE produced by STMicroelectronics, reported in figure 2 (a) and object of the modelling discussed in the present study. It is a traction inverter for electric and hybrid vehicles, in sizes ranging from 100 to over 300 kWe. Such high-power densities can be obtained by the direct connection of the heat sink and the baseplate through a Sn-Ag alloy solder, much more efficient than typical thermal interface material used for power modules. As shown in figure 2 (b), the three-phase device consists of 48 dies, divided into 3 legs (one for each of the

phases) arranged on the baseplate; each leg consists of a pair of switches made up of 8 diodes. Figure 3 shows the vertical cross-section of a leg and the detail of the die connection to the common Cu layer shared by the diodes on the three legs.

3. Numerical model of ACEPACK DRIVE power module

The numerical modelling was developed in Ansys, through a virtual CAD model implemented in SpaceClaim and imported in Mechanical of Ansys. The constituting materials and the thermophysical properties of each of the layer schematized in figure 3 were assigned through the software library. These were considered isotropic and, with the exception of the sinter and solder layers, their temperature dependence was accounted during the simulation as they sensibly vary in the device operating range.

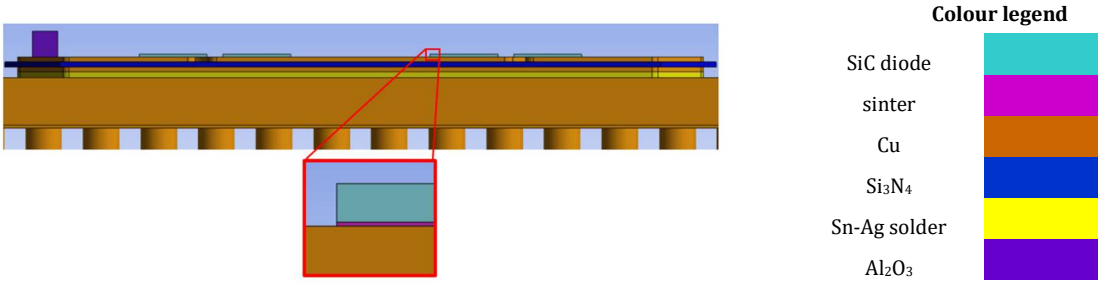
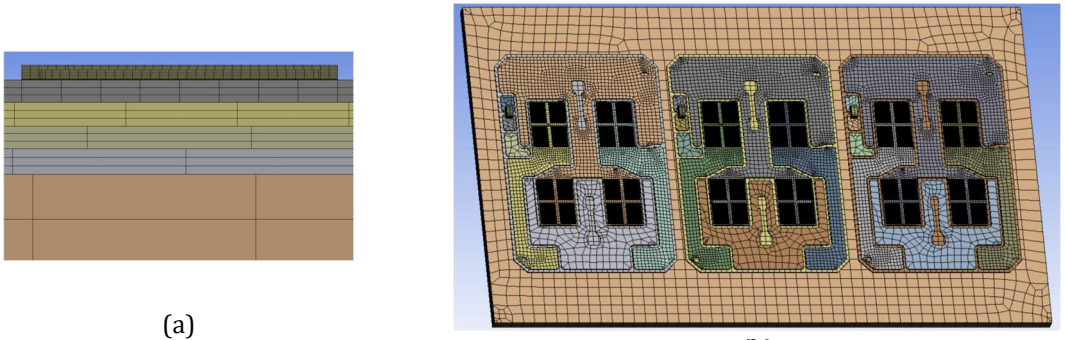


Figure 3. Cross-section of a leg of ACEPACK DRIVE with details of material layering.

In a previous numerical model, a uniform distribution was used for the elements of each layer. To achieve an accurate resolution of the local temperature profile along the device layers, the constraint on uniformity led to a mesh of 6,910,641 nodes and 1,517,380 elements, which was computationally very demanding. Therefore, without loss of accuracy, in the numerical model herein proposed a substantial reduction of the number of nodes and elements was achieved by adopting the edge sizing rule, so as to refine the mesh of the various layer with the desired accuracy. As shown in figure 4 (a), the edge refinement was performed optimizing the element size with respect to both the layer thickness and the local heat flow density, depending as a function of the distance from the dies, i.e. the active heat sources.



(a) (b)

Figure 4. Mesh details: (a) element distribution along the layer cross-section; (b) mesh refinement on the Cu layer under the switch of a leg (die region)

Moreover, to refine the distribution of the element, the MultiZone meshing tool was adopted for all layers, with the exception of the ceramic, solder and copper layers between them, where element distribution was already satisfactory. The MultiZone tool generates a pure hexahedral mesh, resulting in regions with structured mesh, but automatically switch on an unstructured mesh generation in those regions that are more difficult to capture.

Finally, a face-sizing rule was applied at the Cu layer under the footprint of the regions occupied by the dies, thickening the mesh to a value of 6·10-4 m, while the mesh of the remaining part of the copper layer was generated according to the general rule. This led to a smooth control of the variation of the mesh size from one layer to another. Figure 4 (b) reports a plan view of the final mesh, from which the main differences between the mesh of the layers beneath the heat sources are observable. In summary, the adopted meshing criteria led to a mesh consisting of 5,300,657 nodes and 1,073,916 elements, i.e. lower of about 25% with respect to the previous.

The setting of the boundary conditions was based on the specific requirement of achieving the maximum junction temperature at the die surfaces, $T_{j,max} = 175°C$, with a tolerance of 0.2°C. This is, in fact, the design limit of the device within which the manufacturer guarantees the performance and reliability of the power module. Thus, a set of preliminary numerical tests were performed in order to set the value of the power loss at the dies, P_{die}, leading the regime junction temperature at $T_{j,max}$. This was obtained for $P_{die} = 111\ W$, assuming uniformly distributed on each of the surfaces of the active dies.

For the scope of the present study, in order to avoid unnecessary CFD simulation of the coolant flow within the water-jacket, the boundary condition at the heat sink surface was simplified by assuming a constant heat transfer coefficient (HTC) dependent on the properties of the coolant and on the flow rate crossing the heatsink. For the simulation discussed in the present study it was always considered HTC=104 W/m2 °C with a constant coolant reference temperature equal to 65°C. Parenthetically, this HTC value had been previously evaluated by means of CFD simulations, performed considering a flow rate of 6 10-3 m3/min of a coolant solution of water and glycol at an inlet temperature of 65 °C. For all other surfaces, where no HTC value was assigned, adiabatic boundary conditions are automatically assigned by the numerical model's resolution algorithm, which is a simplified condition that is indeed acceptable in consideration of the robust thermal insulation determined by the protective gel that covers all the device surfaces. The numerical simulations were performed with the aim of determining the step response of the thermal field along the device layers caused by the activation of the dies, i.e. imposing a step change of the feeding power from $P_{die} = 0\ W$ to $P_{die} = 111\ W$. In consideration of the exponential time decay of the thermal step-response, the numbers and amplitudes of the simulation time steps were modulated, so as to achieve the proper resolution in a limited computational time.

3.1 Simulated thermal field

This section reports the description of the regime thermal field obtained at the extinction of the step response transitory under two conditions of interest:

i. step-wise simultaneous activation of all of the dies of the device with the maximum heat power $P_{die} = 111\ W$;
ii. ii. step-wise activation of a single die, selected on the central leg of the device, with the maximum heat power $P_{die} = 111\ W$.

Though numerical thermal maps for this case are not reported for the sake of conciseness, this simulation allowed to quantify: i. the time required for the extinction of the step response

transitory, i.e. 13.5 s after the activation of the dies, ii. the maximum steady-state temperatures of about 175°C hottest die on each leg of the device, i.e. the cyan-colored dies of the bottom-right quartet of each leg in figure 2 (b), and iii. the substantial equivalence of the thermal field on the three legs.

The second simulated condition concerns the step response produced by the activation of a single die; among the possible dies, this was chosen by selecting the die of the central leg at which the maximum steady-state temperature was reached at the end of the numerical simulation discussed insofar, i.e. for the case of simultaneous stepwise activation of all dies with the maximum heat power $P_{die} = 111\ W$.

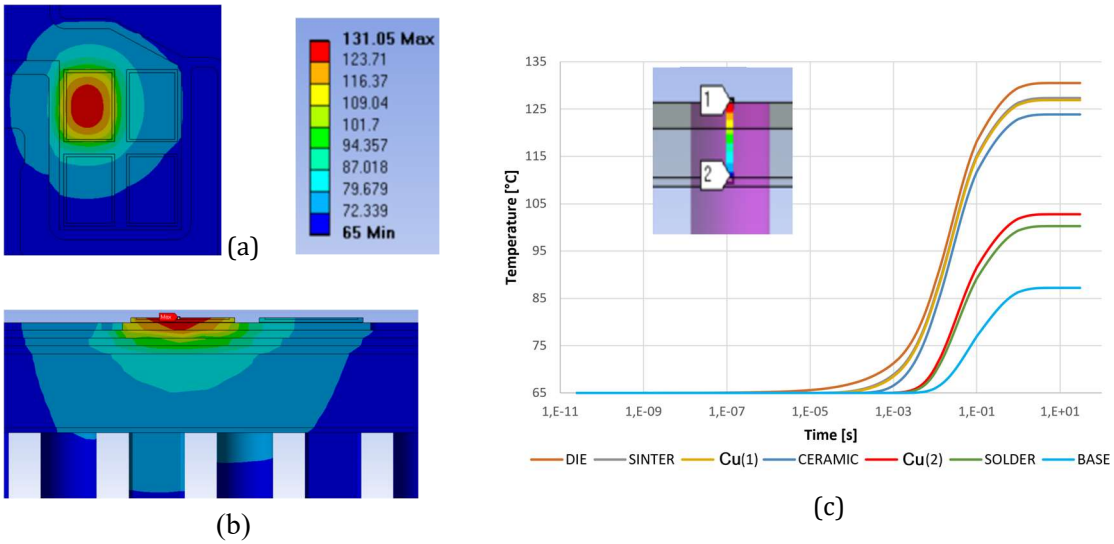


Figure 5. Step-response simulation with the activation of a single die in the central leg: (a)-(b) maps of the steady state thermal field reached at the end of the step response transitory, (c) step-response transitory of the internal temperatures at the interfaces between the layers.

Activating only this die with the same heat power, $P_{die} = 111\ W$, the highest temperature reached at steady state on the die surface, i.e. the maximum achived junction temperature, is 131.05 °C. Moreover, this value is attained at the simulation step 256, thus after 10.5 s since the die activation. Therefore, as expected, the maximum junction temperature is reached more rapidly and is lower of about 44°C than that obtained after the activation of all the dies, due to the peripheral heat flow along the layers. This clearly emerge from the thermal map reported in figure 5 (a), where an asymmetrical propagation is observed in the surrounding of the active die, as a consequence of the geometrical layout of the Cu layer that poses a limitation to the possibility to propagate heat towards the region on top and on the left of the die.

The temperature values at the interfaces between the layers are fundamental for the assessment of the lumped parameter thermal model discussed in the following paragraph. Therefore, the thermal distribution across the layers of the device, mapped in figure 5 (b), was extracted by the numerical model along a vertical path, originating in the point of the die where the maximum temperature is reached, and ending at the interface between the solder and the baseplate layers. In this way the transient step response of the temperatures at the layer interfaces reported in figure 5 (c) were evaluated and were subsequently used to derive the parameters of the model discussed in the next section.

4. 1-D lumped-parameter thermal models of a single die

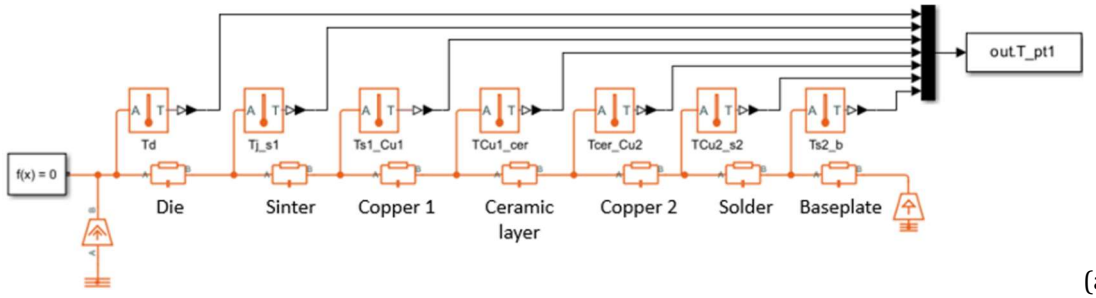
The first proposed model recalls the canonical junction-to-case 1-D model and serves just as a reference benchmark. Worth mentioning that for the purpose of the present study, concerning a power module with a built-in heat sink, the reference 1-D case temperature is, in fact, substituted by the reference temperature of the coolant, T_{fl}, circulating in the water jacket of the device, which was assumed to be constant at the current state of the modelling activity. In this basic model, the junction temperature, $T_j(t)$, is the only prediction that can be withdrawn in order to characterize the thermal response of the device at the time varying power input to the die, $P_{die}(t)$. With this premises, a unique Foster network is required between the temperature nodes T_j and T_{fl}, which is identical to the one reported in figure 1 (a) for the generical nodes T_a and T_b. The numerical simulations discussed in the previous section for the step-wise activation die with a power input $P_{die} = 111\ W$ and a coolant temperature $T_{fl} = 65°C$ were used to calculate through equation (1) the overall numerical thermal impedance between the model nodes T_j and T_{fl}. Afterwards, the order $N_p$of the Foster model and the corresponding values of the N_p couples of lumped parameters $R_{th,n}$ and $C_{th,n}$ were assessed through a specific MATLAB® function that calculates the parameters of the Foster impedance curve providing the best fitting with the numerical impedance, for a given model order. Starting from the first order, the model order was increased until $N_p = 3$, for which the fitting was found to be satisfactory. For brevity, it is only mentioned that the third order parameters for the junction-to-case model and the corresponding Foster thermal impedance calculated by the fitting procedure were found to be comparable with the manufacturer expectations; moreover, the numerical and analytical predictions of the step response transitory of the junction temperature and of the junction-to-case thermal impedance were both found to be in good agreement.

The second 1-D model of the die was constructed in order to be able to provide the prediction of the internal temperatures at the interface of the layers of the die. It is important to highlight that knowing the temperatures of the intermediate layers is crucial to predicting which of them will be most critical and therefore will affected by failures more quickly and easily because of thermal fatigue. This goal was achieved by means of a novel thermal network, built as a sequence of Foster sub-models, one for each layer, connected at the interface nodes. The representation of this model in the Simulink-MATLAB® interface is reported in figure 6 (a), in which each a Foster block represents a sub-model corresponding to a layer of the die.

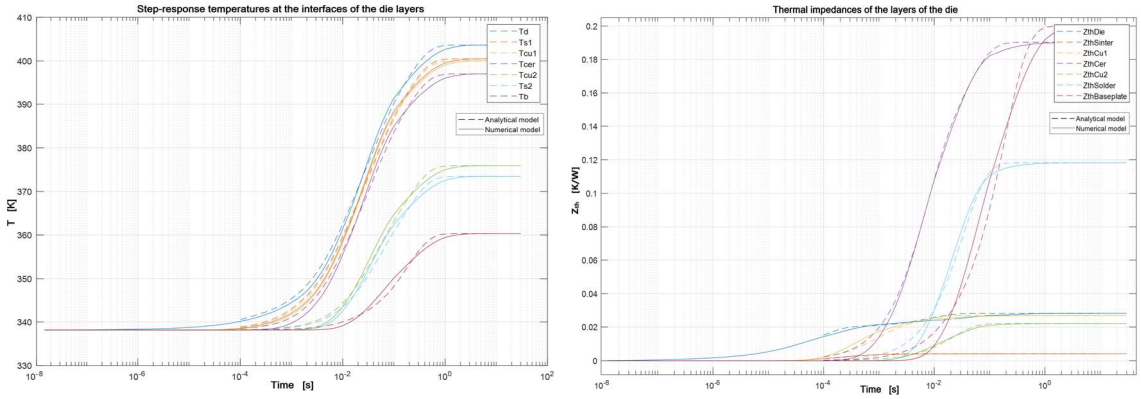
For the specified purpose, in the FEM simulation, monitoring points are selected at the center position of each die and on the surface of each layer at the same vertical position below each chip, and time series of temperature values are extracted. The thermal impedance curves for each layer are then calculated numerically, considering these temperature values at the top and at the bottom of each layer. Therefore, the impedances were calculated for each single layer, and then, the same procedure discussed for the first model was used for identifying the order of each sub-model and of the related set of $R_{th,n}$ and $C_{th,n}$ parameters.

Noticeably, in this case the thermal impedance of each Foster sub-model was calculated by applying the curve fitting procedure to the numerical thermal impedance calculated by the numerical time series on the interface surfaces, extracted as described in section 2. Again, for all the sub-models, the third order model was found to be the one that give a satisfactory fitting without an excessive increase of the number of parameters. Once the model parameters were identified, the model was simulated in order to compare its prediction with the available

numerical results for the die step-response. Figure 6 (b) and (c) compare the numerical and analytical simulations of the step-response of the temperatures at the interfaces of the layers and of the thermal impedances of each layer, respectively.



(a)



(b) (c)

Figure 6. Mesh details: (a) element distribution along the layer cross-section; (b) mesh refinement on the Cu layer under the switch of a leg (die region); (c) planimetric view of the generated mesh.

As these preliminary results show satisfactory agreement, the analytical model was simulated under the condition of a pulsating power input, i.e. the time-varying input condition that corresponds to the alternative current that feeds the dies of the ACEPACK DRIVE module in actual operations. For comparison with previous results, figure 7 shows the predictions of the temperatures at the interfaces between the layers simulated under the condition of an alternative power input $P_{die}(t)$ of amplitude 111W and frequency 100 Hz. The straightforward advantage of the proposed lumped-parameter 1-D model is represented by its ability to produce, in a negligible simulation time, not only the dynamics of the junction temperature but also the thermal cycling of the interface temperatures, i.e. one of the main causes of thermal fatigue leading power electronics devices to failure.

Reported results show that, the proposed lumped-parameter model of a single die, though preliminary to the construction of the model of the whole multidie power module, demonstrates to reliably predict internal temperature dynamics with very limited computational effort; a main advantage is the very small number of parameters and the repeatable procedure that can be reproduced for other power modules in order to assess a device-specific tool for the prediction of the temperature dynamics and, thus, for thermal fatigue and reliability analysis for any type of mission profile.

5. Conclusion.

The study reports the definition of a refined 1-D lumped parameter models for the preliminary identification of the internal thermal impedances of the layer of a single die of ACEPACK DRIVE SiC MOSFET power module, produced by STMicroelectronics. The lumped parameters were extracted from the step response transient time series of the layer interface temperatures, simulated by means of an accurate numerical model purposely assessed. The model was shown to be able to produce a fast and computationally efficient prediction of the dynamics of the internal temperature distribution within the die, both for a step-wise variation of the power input and for an alternative power input, i.e. dynamical phenomena causing thermal cycling leading to failure.

The current development of the present study is oriented to the assessment of a 3-D lumped parameter model that encompasses, for each of the dies of the device, not only the 1-D model herein discussed but also the thermal mutual impedances that govern the peripheral heat transfer between confining dies.

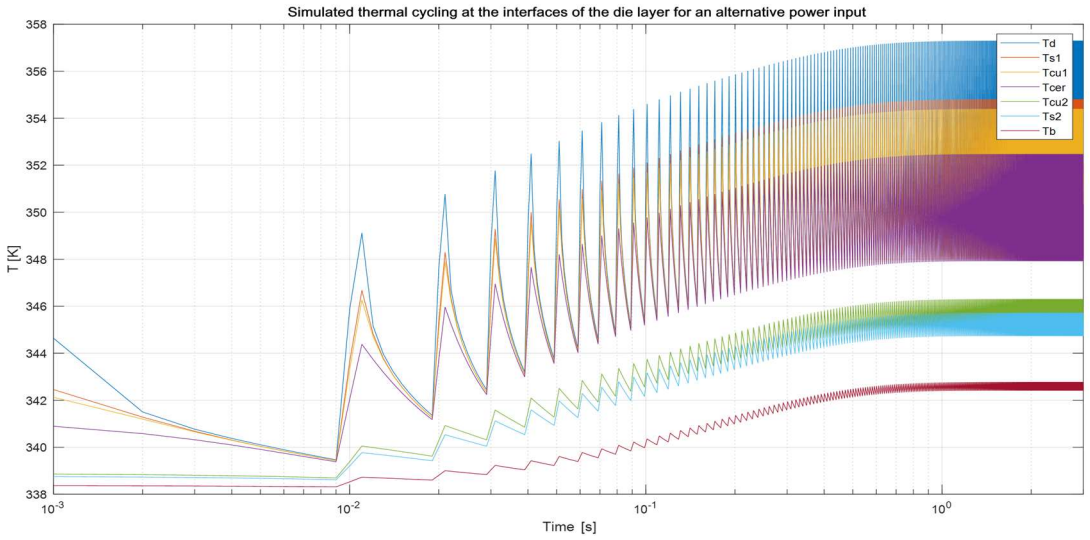


Figure 7. Predicted thermal cycling dynamics of the internal temperatures at the interfaces of the die layers, simulated for an alternative power input $P_{die}(t)$ of amplitude 111W and frequency 100 Hz.

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