UNIVERSITY OF CATANIA

DEPARTMENT OF ELECTRICAL, ELECTRONIC

AND COMPUTER ENGINEERING

Ph.D. Course of
SYSTEMS, ENERGY, COMPUTER AND
TELECOMMUNICATION ENGINEERING
Cycle XXXVI

Ph.D. Thesis

Package-scale galvanically isolated systems for data transfer

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ACADEMIC YEAR 2022-2023

SUMMARY

This thesis dissertation summarizes the research studies which I have been carried out during the three years of Ph.D. course at the University of Catania. Some of these activities have been performed in collaboration with STMicroelectronics within the EU Project GaN4P.

Nowadays, the adoption of galvanic isolation techniques is required in several environments to guarantee safety and reliability. Application fields such as the industrial, the automotive and the medical one, require increasingly isolation rating (i.e., V_{SURGE} up to 20 kV). On the other hand, the higher switching frequencies allowed by wideband power devices, such as GaN and SiC transistors, require increasingly high immunity to transient disturbances (i.e., CMTI beyond 200 kV/μs). Unfortunately, chip-scale isolators based on capacitive and inductive coupling cannot easily address these new challenges due to inherent technological limitations. Therefore, to deal with these more and more demanding requirements a promising solution

is to move from a chip-scale approach to a package-scale one. This means to implement a galvanically isolated system by exploiting packaging/assembling techniques and RF planar coupling between micro-antennas. The most relevant activity which I was involved in concerns the design of a package-scale isolated channel for gate-driver applications in GaN technology. However, other technology platforms (i.e., CMOS and BCD) have been exploited achieving some meaningful research results in the matter of galvanic isolation based on RF planar coupling.

The thesis is organized as follows. The basics of galvanic isolation, along with the principal application fields and a brief overview of the state-of-the-art, are given in Chapter 1. Chapter 2 discusses package-scale isolation pointing to the key aspects of this approach as well as main advantages over traditional isolators. An optimized design flow for the micro-antennas is proposed and validated by means of 3D electromagnetic (EM) simulations carried out in a 0.32-μm BCD technology. Moreover, a novel low-consumption RF oscillator topology conceived for package-isolation is discussed. The advantages of the proposed solution are highlighted in comparison with a traditional one (i.e., complementary cross-coupled oscillator) within an isolated data link designed in a 0.18-μm CMOS technology. A whole package-scale isolated control channel in GaN technology for gate-drive applications is presented in Chapter 3. I mainly worked on the design and layout of the micro-antennas and the TX front-end, which adopts nearly the same oscillator topology discussed in the previous chapter. The isolated link has been fabricated and characterized by showing low power consumption while maintaining state-of-the-art performance.

Finally, a side activity in which I have been especially involved in the last year of my Ph.D. studies concerns the modeling and characterization of passive devices fabricated in a GaN RF technology developed by STMicroelectronics. Main results achieved in this context are reported in Appendix A.

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Nomenclature

ABBREVIATION/ ACRONYM	DESCRIPTION
ac	Alternating current
BCD	Bipolar-CMOS-DMOS
BEOL	Back end of line
CMOS	Complementary MOS
CMTI	Common mode transient immunity
DC	Duty cycle
dc	Direct current
DTI	Distance through isolation
EM	Electromagnetic
GaN	Gallum nitride
HEMT	High electron mobility transistor
HV MOS	High voltage MOS
IEC	International Electrotechnical Commission
IL	Insertion loss
LDMOS	Laterally diffused MOS
MOS	Metal-oxide-semiconductor
PVT	Process, voltage and temperature

ABBREVIATION/ ACRONYM	DESCRIPTION
PWM	Pulse width modulation
RF	Radio frequency
RX	Receiver
SiO_2	Silicon dioxide
SiP	System in Package
TX	Transmitter
UL	Underwriters Laboratories
PVT	Process, voltage and temperature

Chapter 1.

Galvanically isolated systems

1.1. Introduction

The aim of a galvanic isolation system is to electrically separate two domains, meanwhile allowing power and/or data transfer between them. A general block diagram is shown in Fig. 1.1. Domain A is usually called user interface whereas domain B is defined as isolated interface. The two domains must be galvanically isolated since interface B, which typically operates in harsh, noisy or high-power environment, is subject to lighting strikes, hazardous voltages and/or requires a different ground reference. Energy is transferred across the galvanic barrier only from domain A to B, thus

providing a power supply for the isolated interface. On the other hand, the exchange of information can occur in both directions giving place to bidirectional data communication. As far as low-power applications are concerned, isolated power levels in the order of hundreds of mW with data rate up to 100 Mbit/s are required [1].

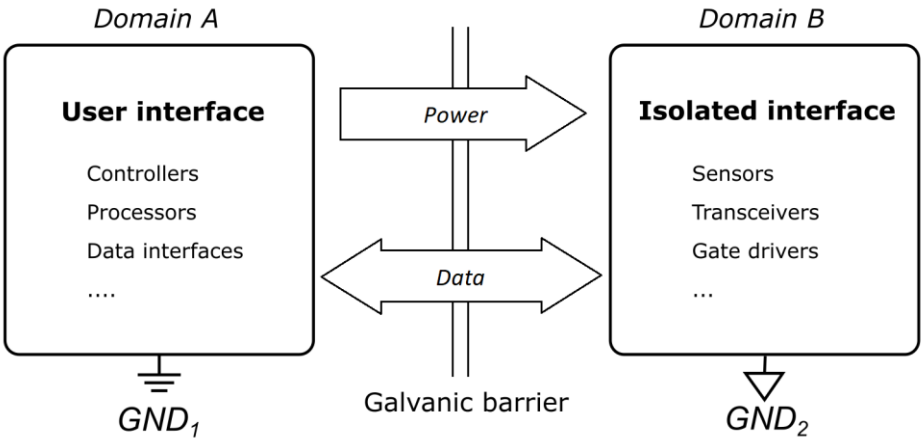


Fig. 1.1 Simplified block-diagram of a galvanically isolated system.

In recent years, several application fields (such as industrial, medical, automotive and power conversion ones) have been taking advantage of galvanic isolation techniques in order to improve safety and reliability, especially in harsh environments. The adoption of galvanic isolation is mandatory when high power equipment is operated by human beings, however it is also required when relatively low power levels are involved (e.g., industrial sensors interfaces, low-power medical equipment, gate driver for power converter and motor control, etc.). In this regard, in the last decades the research interests have been addressed to the development of low-cost

highly integrated galvanically isolated systems based on inductive, capacitive and more recently, RF coupling, replacing traditional expansive and bulky solutions (i.e., optocouplers and discrete transformers).

This chapter is arranged as follows. Recent regulation in the matter of semiconductor galvanic insulators, including the isolation rating classification, safety testing procedures and requirements is discussed in the next section. Low-power applications, especially gate drivers, are briefly presented in Section 1.3. Finally, the state-of-the-art isolation technologies are summarized in Section 1.4.

1.2. Safety isolation standards

The main reason for adopting galvanic isolation is to guarantee people safety against electrical shocks. Indeed, if proper isolation is not provided a human being touching an electronic device can be electrocuted, namely experience a current flow into his body. Unfortunately, thousands of electrocution accidents, some of them fatal, occur every year. Depending on the current magnitude, contact duration and other conditions, several pathophysiological effects can arise such as injuries, tetanization (i.e., strong involuntary muscle contraction), burns, respiratory attest, ventricular fibrillation and, ultimately, death [2]. In this regard, Fig. 1.2 summarizes the effects of alternating currents at utility frequency (i.e., 15-100 Hz) flowing through the human body [3], [4].

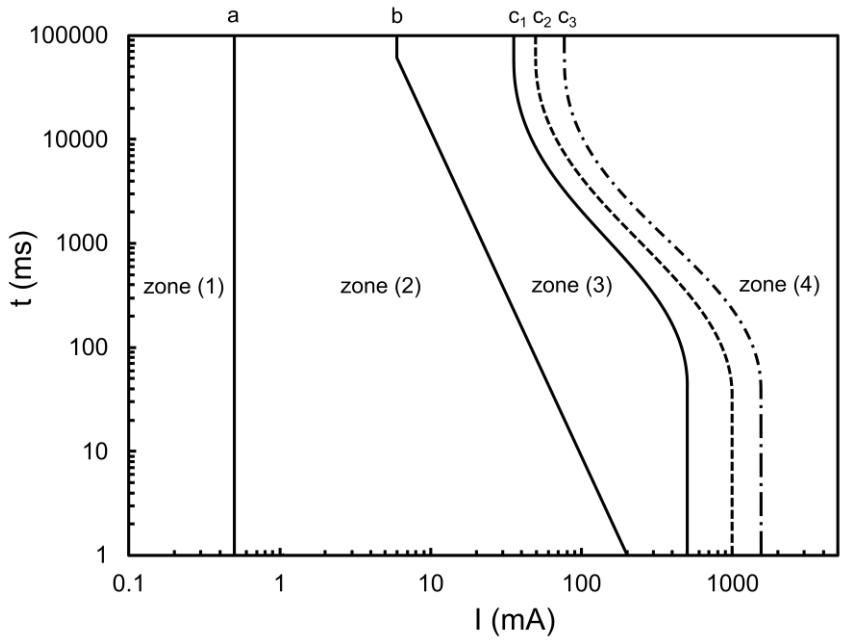


Fig. 1.2 Safety I-t curves.

The following safety curves are defined as a function of the current intensity, I, (expressed as rms value) and duration, t:

- curve a: perception threshold,
- curve b: tetanization threshold,
- curve c_1: ventricular fibrillation threshold,
- curve c_2: curve associated with a probability of triggering ventricular fibrillation equal to 5%,
- curve c_3: curve associated with a probability of triggering ventricular fibrillation equal to 95%.

The safety threshold curves delimit four regions associated with different effects on human beings:

- zone (1): absence of reactions,
- zone (2): perception of the electrocution without the occurrence of pathophysiological effects,
- zone (3): manifestation of pathophysiological effects, whose gravity grows with current intensity and duration, such as tetanization, difficulty breathing and heart troubles without triggering of ventricular fibrillation,
- zone (4): possibility of triggering ventricular fibrillation, with increasing probability as the current magnitude and duration increase.

The values illustrated by the I-t safety curves should be intended as a general reference based on statistical data. Indeed, the effects due to the same current flowing for the same amount of time may differ from one person to another depending on physical characteristics like age, body structure and state of health. Moreover, variables involving the resistance of the human body such as the current path (e.g., left hand – right foot or right hand – both feet), the clothes worn, any humidity of the body part that gets in touch with the non-isolated device etc. results in different risks and damages. It is worth mentioning that safety curves are defined also in dc showing slightly lower thresholds. High frequency currents are instead less dangerous for human beings compared to utility frequency ones.

The physical damage caused by electrical shocks which has been just discussed, has led over the time to the definition of safety standards including design procedures, certification processes and general rules for isolators

testing. National and international bodies have developed regulations in the matter of galvanic isolation, both at component and system level. Among these organizations the Verband der Elektrotechnik, Elektronik und Informationstechnik (VDE), the Underwriters Laboratories (UL), the Canadian Standards Association (CSA), the International Electrotechnical Commission (IEC) and the European Norms (EN) must be quoted. The main system-level standards are summarized in Table 1.1. However, even if the same safety standards are referred [5], certification requirements can vary across the different areas of the globe, thus the above-mentioned national and international institutions are working on the simplification and unification of the certification procedures.

Table 1.1 Main safety system-level standards in the matter of galvanic isolation [5].

	Household	**Industrial**	**Information technology**	**Measurement and control**	**Medical**
International	IEC 60065	IEC 60204	IEC 60950	IEC 61010-1	IEC 60601
Germany	VDE 860		EN 60950	VDE 410/ 0411	VDE 0750
USA	UL 60065	UL 508, UL 60947	UL 60950	UL61010	UL 60601
Canada		CSA. 14-10	CSA 60950	CSA 61010	CSA 601

One of the fundamental outcomes of the safety standardization is the definition of the isolation degree of electrical systems through the classification in four categories: functional, basic, double and reinforced isolation [6]-[8], as illustrated in Fig. 1.3. Functional isolation does not

prevent humans from being electrocuted but only guarantees the proper system functionality providing simple separation of ground references. Basic isolation is achieved by implementing a galvanic barrier withstanding voltage drops of several kilovolts. In many cases basic isolation is considered enough to ensure appropriate protection against electrical shocks. However, when a higher level of safety is required, double isolation can be exploited by connecting two galvanic barriers in series. Although an additional barrier improves the isolation level providing also redundancy in case of isolation failure, implementing double isolation is typically more complex and expensive. For these reasons reinforced isolation, which is the highest isolation degree available on the market, has been standardized. It is obtained with a single isolation barrier that provides the same electrical strength, reliability and shock protection as a double basic barrier, while saving cost and space [8].

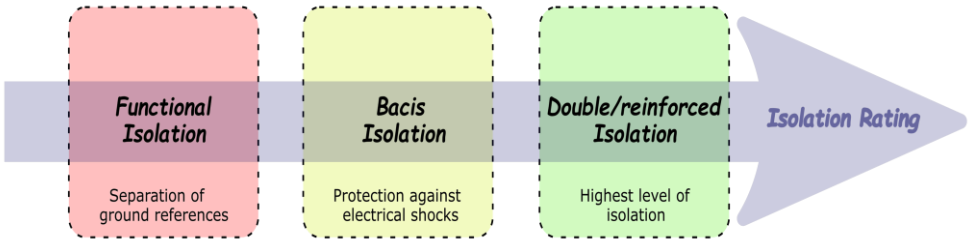


Fig. 1.3 Classification of galvanically isolated systems.

Component-level standards provide the definition of several parameters and testing procedures used to qualify the isolation performance of a single component whatever the isolation degree of the whole system. In this regard the most widely adopted standards are:

• UL 1577: Standard for Optical Isolators

• IEC 60747-5: Semiconductor Devices - Optoelectronic devices

• VDE 0884-11: Semiconductor Devices - Magnetic and Capacitive Coupler for Basic and Reinforced Isolation

Specifically, the overall UL 1577 and the 5th part of the IEC 60747 standards concern the isolation characteristic of optocoupler devices, whereas the requirements and test methodology for highly integrated isolators based on transformers and capacitors are detailed in VDE 0884-11 standard. According to this standardization, semiconductor galvanic insulators must withstand high voltages both for short periods of time and throughout the device lifetime. This leads to two different specifications: the maximum transient voltage (V_{IOTM}) and the maximum repetitive voltage (V_{IORM}). The first one is referred to as the peak transient voltage that the isolator can withstand without breaking down for a given short amount of time. On the other hand, V_{IORM} is defined as the maximum repetitive peak voltage that the isolator can handle over a specific long period.

The voltage values V_{IOTM} and V_{IORM} are measured together by means of two testing procedures [9], named Method A and Method B1 respectively, as described in the VDE 0884-11 standard. The first method is a destructive test applied throughout the certification process while the second one, which instead does not deteriorate the isolation capability of component, is used in the production manufacturing phase. Every device must pass the second test in order to be released to the market. The simplified test profiles of Method A and Method B1 are displayed in Fig. 1.4 and 1.5, respectively. It can be noted that the two profiles show quite similar shape, however the processes

substantially differ for duration and thus resulting stress of the component. Indeed, in the destructive test the isolator must withstand a voltage $V_{ini}=V_{IOTM}$ for a minute, then it subjects a partial discharge at a voltage $V_m = 1.6*V_{IORM}$ for a times t_m of 10 seconds. In Method B1 instead the insulator is stressed at V_{IOTM} just for one second, while the discharge occurs at 1.875 times V_{IORM} with t_m=1s.

The most stringent requirement defined by the regulation (i.e., IEC 60747-5 and VDE 0884-11) is the maximum surge isolation voltage (V_{SURGE}) that quantifies the capability of the isolator to withstand very high voltage impulses of a certain transient profile. Fig. 1.6 shows the surge test profile, which is used to evaluate the isolation degree at component level. Specifically, the reinforced isolation is achieved only if the component passes the surge test with a V_{SURGE} greater than 10 kV.

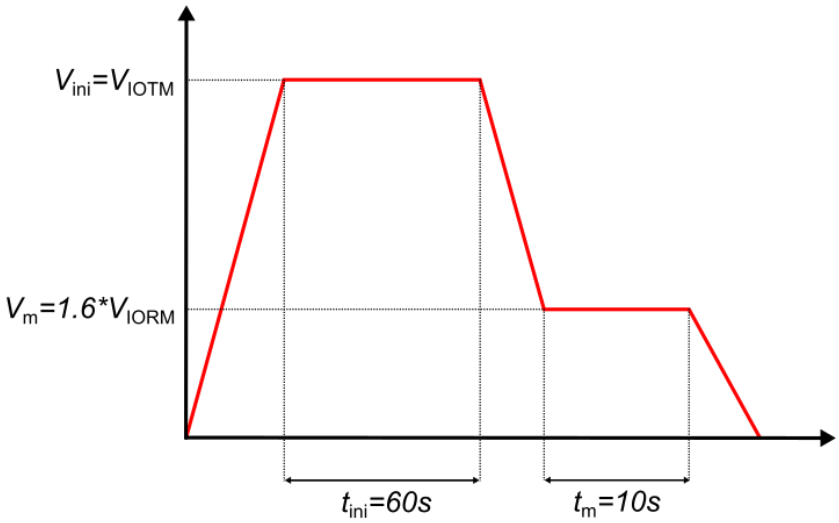


Fig. 1.4 Simplified Method A test profile.

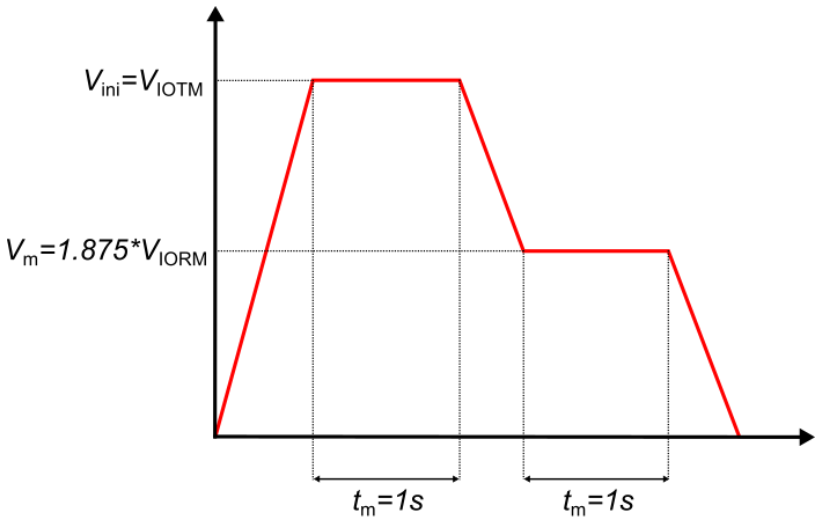


Fig. 1.5 Simplified Method B1 test profile.

Nevertheless, the galvanic barrier can be also subject to common-mode currents arising from fast voltage shift between the grounds of the two interfaces (i.e., high dV/dt). This results in the definition of another key performance parameter called common mode transient immunity (CMTI), which quantifies the capability of the isolator to withstand rapid shift of grounds and whose typical values range from 50 to 200 kV/μs.

Finally, it is worth mentioning that often component and system-level standards include specific requirements on the clearance and creepage (i.e., distance through air and along the surface, respectively) of the isolation package. Nevertheless, more commonly it is referred to the distance through isolation (DTI), which is defined as the smallest distance between the user and the isolated interfaces, internal to the device's package.

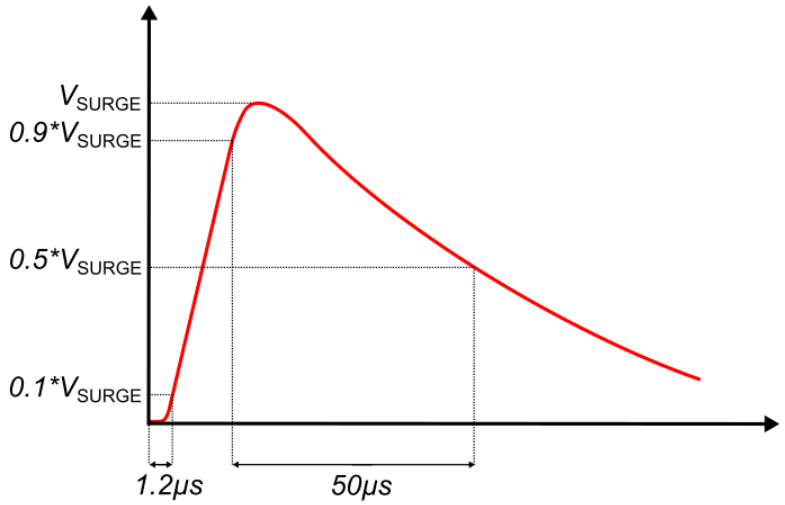


Fig. 1.6 Simplified surge test profile.

1.3. Gate driver applications

Currently galvanic isolation is considered crucial, in some cases even mandatory, in several application fields. In addition, to guarantee user safety, isolation techniques can be profitably adopted for other purposes such as ensuring system protection and signal integrity. For instance, wireline networks take advantage of isolators to break any ground loop between two nodes avoiding data corruption and signal distortion [10]. Another typical application is current monitoring systems in which power and data transfer through user (i.e., low-voltage side) and measuring (i.e., high-voltage side) interfaces are enabled by means of isolated dc-dc converter and digital isolator, respectively [11]. Regarding low-power environments, home appliances, sensors, inductive cookers, defibrillators, patient monitoring

devices and other medical equipment take advantage of galvanic isolation for safety and reliability purposes. Among application fields of galvanically isolated systems, due to its relevance within the main focus of this thesis dissertation, gate drivers deserve to be discussed more closely in the following.

As a few times recalled, the primary aim of an isolation barrier is the protection of low-voltage circuitry, that can get in touch with human beings, from any electric lighting and surge coming from a high-power side. This circumstance occurs in large power conversion systems (i.e., power levels from hundreds to several thousands of kW) which can be found for instance in renewable energy plants, particularly solar and wind ones [12]. Nowadays these systems commonly exploit switched-mode power electronics achieving high efficiency in power conditioning as well as control. An example of power conversion circuit which still represents a remarkable research field [13]-[15], suited for automotive applications, photovoltaic inverters and UPS equipment [16], [17], is gate driver.

A simplified schematic of a motor drive system employing gate drivers is displayed in Fig. 1.7. This architecture is based on a half-bridge inverter which exploits N-type power switching devices (i.e., power MOSFET, IGBT or GaN HEMT) to convert the input PWM signal into a frequency-variable output voltage that drives a motor [18]. Gate drivers are exploited to improve the converter performance minimizing the conduction losses and the switching time of transistors M_1 and M_2, while avoiding detrimental conditions that occur when the two power switches conduct at the same time.

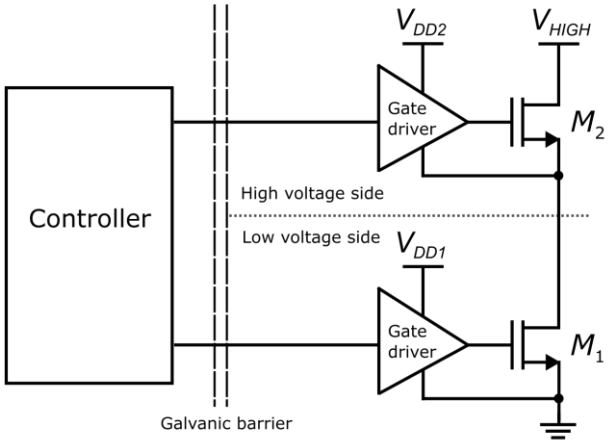


Fig. 1.7 Simplified half-bridge architecture for motor drive.

In order to ensure a correct operation of power switch M_2, the high-side supply voltage, V_{DD2}, must be very close to the inverter supply value, V_{HIGH}. This working condition is commonly accomplished by means of boost capacitors. However, this technique suffers from some limitations in terms of start-up and maximum off time of the high-side switch. Moreover, due to inductive and free-wheeling diode spikes, latch up on the low-side gate driver can take place. These drawbacks can be overcome by connecting the source of each power switch to the respective gate driver's ground, while an auxiliary galvanically isolated supply voltage is provided to both high and low-side.

As far as gate drive applications are concerned, GaN technologies appear quite attractive since they allow efficient high-frequency switched-mode power conversion. Moreover, typically low-voltage and power transistors are available in the same technological platform, enabling fully integrated GaN approach including analog/digital control circuitry along with the power section [19], [20]. However, just one example of galvanically isolated

interface in GaN technology has been recently proposed in literature [21]. Therefore, the implementation of a high-performing GaN-integrated isolated system, suited for applications such as gate drivers, represents a challenging research topic.

1.4. State-of-the-art of galvanic isolation

In order to guarantee galvanic isolation, several approaches can be adopted. The current available isolation technologies, both for power and data transfer, along with their main advantages and drawbacks are summarized in Fig. 1.8. Regarding data transfer, devices based on optical transmission in the near-infrared region have been traditionally adopted. Opto-isolators provide high isolation levels but are affected by some disadvantages, such as fast degradation and poor reliability. As far as power transfer is concerned, the traditional approach instead exploits discrete magnetic-core isolation transformers. In the last years, optocouplers have been widely replaced by highly integrated solutions based on capacitive, inductive, and near-field RF coupling [22]. Isolation capacitors and transformers are referred to as chip-scale isolators to distinguish them from package-scale ones. Specifically, this paragraph deals with package-scale isolators based on a stacked-chip (called also face-to-face) configuration, whereas the planar approach will be discussed in Chapter 2.

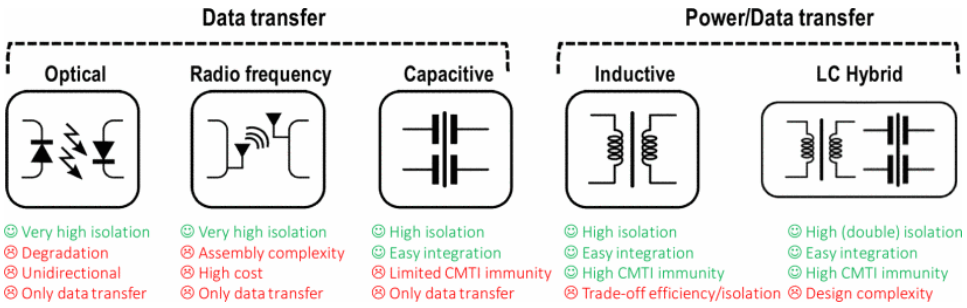


Fig. 1.8 Galvanic isolation technology overview [22] © 2019 IEEE.

Fig. 1.9 displays the simplified architecture of an isolated power link. A dc-ac and an ac-dc converters are exploited to enable energy transfer across the galvanic barrier providing dc isolated power supply at the output. For high power transfer, the isolation device must be a magnetic-core transformer and the dc-ac conversion is carried out by means of inverter with low switching frequency (i.e., frequencies lower than 1 MHz). On the other hand, for low power transfer an integrated transformer can be used, while the dc-ac conversion is performed by a power oscillator (i.e., oscillation frequency over 100 MHz). The total power efficiency of an integrated power link, except for customized semiconductor technologies adopting magnetic layers [23], is typically below 30% [24]-[26]. Since most of the input power is wasted due to low efficiency, the overheating of system components limits the isolated power below 1 W. Fig. 1.10 displays the simplified architecture of an isolated data link. Data transmission is implemented by means of voltage pulses or by using modulated RF signals. The first method achieves very high data rates (i.e., up to several hundreds of Mbit/s) at the cost of a lower CMTI whereas the second one, although more robust, enables lower data rates (i.e., up to a few hundreds of Mbit/s).

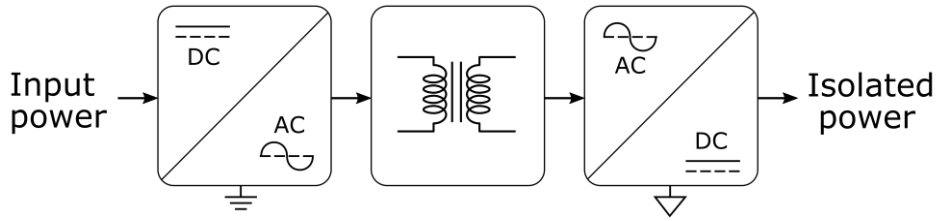


Fig. 1.9 Block diagram of an isolated power link.

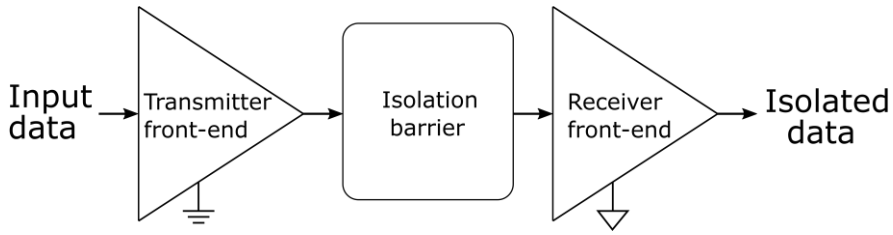


Fig. 1.10 Block diagram of an isolated data link.

Galvanic isolators based on capacitive, inductive and face-to-face RF coupling are represented in Fig. 1.11. As regards capacitive coupling, the most common isolation approach is to build high-voltage capacitors exploiting several layers of inter-metal silicon dioxide (SiO_2), keeping costs down thus enabling large-scale production. However high-performance capacitive isolation exploiting customized advanced technologies have been proposed [27], [28]. Another key advantage of capacitive insulators, along with high isolation rating and cost-effectiveness, is the low consumption (i.e., currents usually in the order of few milliamps) [28]-[30]. A serious drawback is represented instead by the quite low CMTI achievable values (i.e., 50-150kV/μs), which are proportional to the adopted capacitor size. Moreover, these devices are suited only for data transfer since efficiency

degradation caused by signal partition between the isolation capacitance itself and the bottom plate parasitic one, hinders the generation of a usable output power level [31].

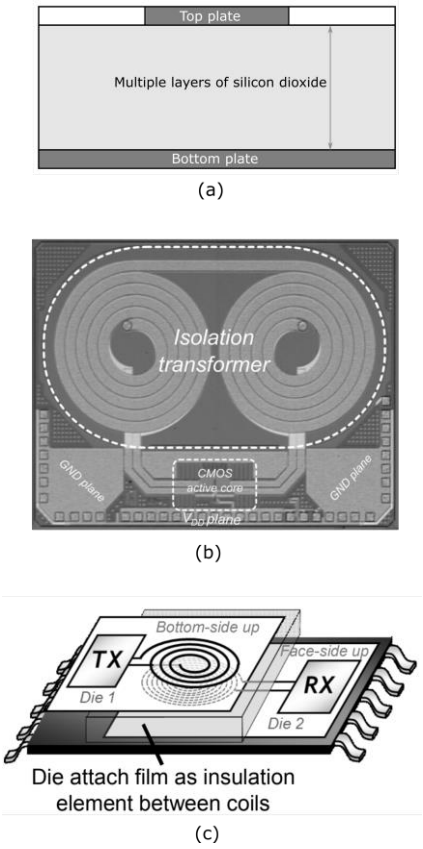


Fig. 1.11 Galvanic insulators based on EM coupling: (a) simplified cross-sectional view of an isolation capacitor, (b) Microphotograph of an isolation transformer [24] © 2015 IEEE, (c) 3D view of an RF face-to-face isolator [32] © 2014 IEEE.

The inductive approach is usually preferred in designing and fabricating integrated galvanically isolated systems. Indeed, transformers enable both data and power transfer achieving at once higher isolation rating and CMTI

performance (up to 20 kV and 200 kV/μm, respectively) compared to capacitors [33]-[37]. Isolation devices based on magnetic coupling are commonly made up as a two-chip or three-chip system in a package (SiP), as shown in Fig. 1.12. In the first case a thick oxide (i.e., a few micrometers) is used as galvanic barrier between primary and secondary transformer coil, whereas a stand-alone post-processed chip exploiting polyimide layer is adopted in the second solution [38], [39].

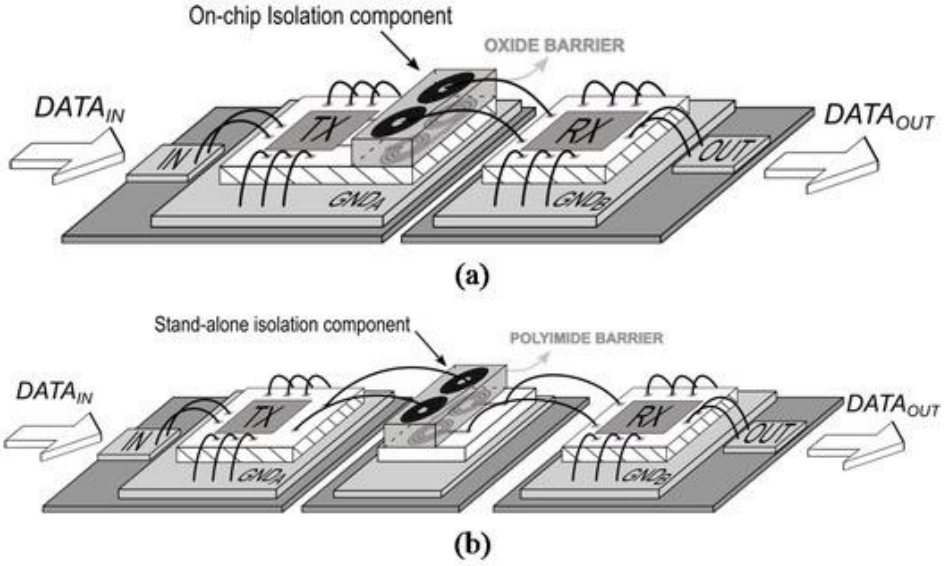


Fig. 1.12 (a) Si-integrated isolation device (two-chip SiP), (b) Post-processed isolation device (three-chip SiP) [40].

The basic idea under RF face-to-face isolation is to implement a transformer taking advantage of near field coupling between metal spirals by opposing two wafers [32], [41]-[43]. A dielectric layer (typically polyimide or glass), which ensures the desired isolation rating, is placed between the two chips while trough silicon vias (TSVs) are used for external connections. The

overall chip stacking structure is typically assembled into a package by using bonding wires and solder balls for top and bottom wafer connections, respectively. Although it would be possible as matter of principle, power transfer systems exploiting face-to-face RF isolator have not yet been proposed. However, it is worth mentioning that chip assembling complexity and package cost have hampered the diffusion of this isolation technology even for data communication [22].

Silicon dioxide and polyimide barriers employed in chip-scale isolators have different maximum surge voltages, fabrication costs and integration levels. Specifically, thanks to the high breakdown voltage (BV) of SiO_2 (i.e., about 1 kV/m) [26], [27] a few microns thick layer is sufficient to guarantee isolation ratings of 5-6 kV [24]-[26], [44]-[46]. Indeed, due to both wafer mechanical stress and second-order BV effects it is not possible to increase the oxide thickness beyond a certain limit (i.e., about 10 μm). Therefore, usually for digital isolators, two series-connected barriers can be exploited to improve the isolation rating [8], [47], [48]. In most cases double isolation is achieved by means of hybrid systems in which the total isolation voltage is sustained in part by a magnetic barrier while in part by a capacitive one [46]. Two capacitive barriers can be easily series-connected without significantly affecting data transfer performance [8] whereas only a few examples of pure inductive approach to double isolation have been proposed in literature [49]. A polyimide barrier provides a BV of just 250 V/m, thus about three times thicker layer is required to withstand the same isolation voltage as a dioxide one. Although SiO_2 barriers enable higher integration level compared to stand-alone post-processed polyamide one, the total manufacturing costs, including both chips and package, are commonly greater.

Finally, it is worth noting that due to their relatively DTI, both solutions suffer of intrinsic limitations not only in terms of maximum isolation rating but also regarding the CMTI. Indeed, such a low DTI (i.e., at most 30 μm) implies high parasitic capacitance (in the order of tens of femtofarads), hence high common-mode currents are produced by ground shifts limiting the CMTI performance. In order to overcome those constraints thus dealing with the new challenges in the matter of galvanic isolation, a promising solution is moving to a package-scale approach based on RF planar coupling, as discussed in the following chapter.

Chapter 2.

Package-scale isolation based on RF planar coupling

2.1. Introduction

As stated at the end of the previous chapter, the maximum thickness of a silicon dioxide or a polyimide isolation barrier, is given by both wafer mechanical stress and second-order BV effects. The resulting relatively low distance trough isolation (DTI), which is in the order of tens of microns, not only limits the isolation rating but also the CMTI performance. Package-scale approach based on RF planar coupling drastically changes the traditional paradigm in the matter of semiconductor isolation, enabling to overcome

these inherent limitations. Indeed, the key aspect of this isolation technique is to use standard molding compound as galvanic barrier between two side-by-side co-packaged chips, thus exploiting a wider DTI (typically hundreds of microns between the chip lead frames). Consequentially, both isolation rating and CMTI are significantly improved compared to chip-scale isolators [40], [41], [50], [51].

Package-scale isolation takes advantage of the near-field coupling between micro-antennas integrated on two side-by-side co-packaged chips, as shown in Fig. 2.1, to realize a physical data channel. The distance between lead frames must be chosen to guarantee the required isolation rating, ensuring at the same time a reasonable electromagnetic (EM) coupling level between the transmitter (TX) and receiver (RX) micro-antennas. Moreover, it should be noted that the minimum value of the DTI can be limited by packaging/assembling issues. Standard molding compound exhibit dielectric strength (EM) of about 50–100 kV/mm [52], [53], thus reinforced isolation (i.e., V_{SURGE} over 10 kV) is enabled with a DTI of just 200 μm, which produces very low capacitive parasitics thus allowing CMTI better than 200 kV/μs [51].

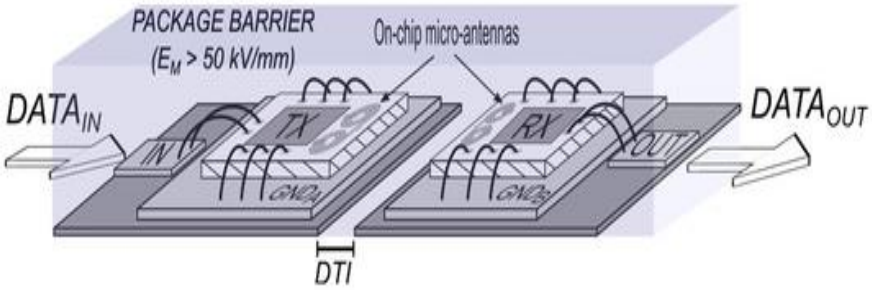


Fig. 2.1 Galvanic isolator based on RF planar coupling [40].

Galvanic isolator based on RF planar coupling has other advantages compared to traditional chip-scale approaches. Firstly, a customized technology/component is not required, whereas standard packaging is sufficient to guarantee outstanding isolation and CMTI performance. Moreover, this approach is highly flexible and can be tailored to the application specifications without time-consuming and expensive technology development. On the other hand, such benefits are counterbalanced by a larger silicon area consumption due to on-chip antennas on both dies. Finally, it should be noted that, since the EM coupling between antennas is extremely weak (i.e., magnetic coupling coefficient less than 10^{-2}), package-scale isolation cannot be exploited for power transfer applications. Indeed, due to high isolation channel loss, carrier-based modulation is mandatory to enable CMTI performance better than 200 kV/s. Package-scale isolation is concisely compared with the state-of-the-art chip-scale approaches in Table 2.1.

Table 2.1 State-of-the-art galvanic isolation approach comparison [40].

Isolation Approach	**Inductive**	**Capacitive**	**RF planar coupling**
Isolation Layer	SiO_2/Polyimide	SiO_2/Polyimide	Molding compound
No. Chips	2/3	2/3	2
Custom Technology	Required	Required	Not required
Design Flexibility	Low	Low	High
DTI	10-30 µm	10-30 µm	300-700 µm
Isolation Rating	5-20 kV	5-10 kV	10-25 kV
CMTI	75-200 kV/µs	50-150 kV/µs	200-250 kV/µs
Si Area	Medium	Low	Medium/high
Power transfer	Yes	No	No
Modulation	Impulsive/ Carrier-based OOK	Impulsive	Carrier-based OOK

This second chapter is organized as follows. The system architecture of a typical package-scale isolated data link, along with main circuit blocks, is discussed in the next section. Section 2.3 is focused on the micro-antennas design. Particularly, general guidelines are given in Subsection 2.3.1 whereas an optimized design flow which has been validated by means of 3D EM simulations is proposed in Subsection 2.3.2. Finally, a novel RF oscillator topology properly conceived for package-scale isolation is presented in Section 2.4. Specifically, theoretical topology description and its validation, including a comparison with a traditional oscillator, are discussed in Subsection 2.4.1 and 2.4.2, respectively.

2.2. System architecture and circuit description

The simplified block-diagram of a data link adopting package-scale isolation based on RF planar coupling is shown in Fig. 2.2. Since the EM coupling between the TX and RX micro-antennas is extremely weak, the system needs to be operated in resonance condition. Moreover, carrier-based narrowband communication is mandatory to ensure good performance in terms of data rate and CMTI [41], [50], [51]. In this regard, on-off keying (OOK) pulse width modulation (PWM) of an RF carrier is typically adopted since this technique guarantees higher robustness compared to the traditional amplitude-shift keying (ASK) modulation. Chip A integrates the TX front-end mainly including an RF oscillator connected to the TX micro-antenna, L_{TX}, which is exploited as an inductive tank. Input data are fed to a PWM modulator which drives a turn on/turn off circuitry to properly switch on/off

the oscillator. Thanks to the near-field coupling between the two antennas, an RF modulated voltage is induced across the RX coil, L_{RX}, on Chip B. After rectifying and filtering, the RX envelope voltage, further amplified by the gain stage G, drives a hysteresis comparator to reconstruct the transmitted PWM signal. Finally, a baseband PWM demodulator is used to draw the original bit stream.

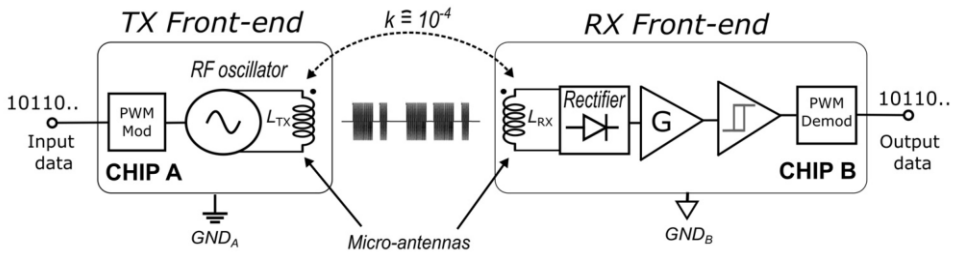


Fig. 2.2 Block diagram of an isolated data channel based on RF planar coupling [40].

The RF oscillator represents a bottleneck for the whole data link. Indeed, the design of this circuit block is very challenging due to stringent specifications in terms of current consumption and start-up time. In this regard, the commonly used LC oscillator topologies are displayed in Fig. 2.3. D-class oscillator, shown in Fig. 2.3(a), is highly preferred when transistors with very high breakdown voltage, such as LDMOS, HV MOS [26], [44], [54], [55] and GaN HEMTs [21], are available. Indeed, the D-class topology can provide quite high oscillation voltage, i.e., more than twice the supply one, V_{DD}, [56]. Given that the maximum allowable drain-source voltage, V_{DS_MAX}, is typically higher than the corresponding gate-source value, V_{GS_MAX}, coupling capacitors, C_B, are exploited to perform a voltage partition with the gate capacitance of M_{12} thus preventing gate-oxide breakdown.

Instead, if the adopted technology provides only standard MOS devices, the traditional inductor-loaded complementary cross-coupled oscillator (shown in Fig. 2.3(b)) can be used [51]. This topology maximizes the oscillation amplitude within the supply voltage, while giving the advantage of nearly doubled transconductance at the same current level compared with a simple cross-coupled oscillator, also minimizing the startup time. It is worth noting that in both topologies a parallel capacitor C_p, which is added to the transistor and TX antenna parasitcs, is exploited to set the oscillation frequency, f_{RF}. Indeed, an accurate modeling of core parasitic capacitances is very hard due to their high nonlinearity. Thus, a dominant capacitor C_P (i.e., at least ten times higher than the parasitic capacitance) should be adopted to avoid unpredictable simulation errors.

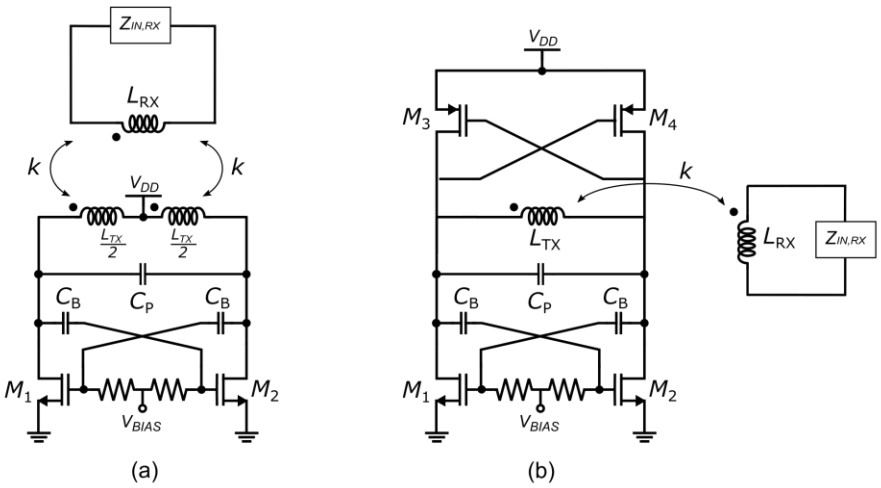


Fig. 2.3 RF oscillator topologies adopted in package-scale isolation: (a) D-class oscillator, (b) complementary cross-coupled oscillator.

As regards the RX front-end, the rectifier stage represents a crucial block which must achieve high performance in terms of sensitivity, input impedance, CMTI and power consumption. The mixer-based topology adopted in [51] presents drawbacks such as the high-power consumption and the need for an additional pre-amplification stage. Therefore, rectifier circuits based on common-source (CS) configurations that inherently ensure good voltage gain along with high input impedance and low power consumption [57], have been exploited [21]. Moreover, the quiescent voltage at the input of the hysteresis comparator must be accurately set to ensure correct operation of the RX front-end. Indeed, this bias point is highly sensitive to the offset voltage caused by process-volta-temperature (PVT) variations at the amplifier input. Therefore, to guarantee robustness allowing a correct reconstruction of the PWM signal the adoption of an offset compensation technique is mandatory [21], [58].

Multi-channel capability is often required in galvanic isolated digital interfaces. When sufficiently high data rate is available, it can be implemented by multiplexing different data channels on the same physical link [39], [59]. For half-duplex data transfer, a single physical isolated link can be exploited, whereas full-duplex communication requires an additional physical link [51]. In this regard, TX-to-RX cross-talk between channels has to be taken into account in designing bidirectional full-duplex galvanic isolator based on RF planar coupling. A simple solution to reduce detrimental effects of crosstalk is to increase the spacing between channels as done in [51]. However, channel spacing must be quite large (i.e., more than twice the DTI) to achieve a reasonable TX-to-RX rejection (i.e., better than 15 dB), thus implying high area consumption. Therefore, in order to save area, it is

mandatory to exploit different RF carrier frequencies for each channel (i.e., frequency separation) [50].

The strong channel attenuation (i.e., about 30-45 dB) of a package-scale isolator can affect the output signal demodulation, thus compromising the whole link functionality. Indeed, the induced voltage across the RX antenna must be sufficiently high to ensure proper operation of the data link. In this regard micro-antenna layout optimization, with the aim of increasing the EM coupling, is required. Furthermore, circuit TX front-end design improvements to maximize the transmitted voltage, while ensuring low current consumption, must be pursued. These two open research issues, which have represented crucial topics of my Ph.D. studies, are extensively discussed in the following sections.

2.3. Micro-Antenna Design

2.3.1. Design Guidelines

The design of on-chip micro-antennas has several similarities with the design of RF spiral inductors. However, in galvanic isolators based on RF planar coupling the main goal is the reduction of the channel loss, which calls for the antenna EM coupling maximization. Therefore, to properly address the micro-antenna design, some crucial differences with traditional inductors must be highlighted. Although the insertion loss, *IL*, is typically used to account for the losses of a passive component, a more significant parameter

reflecting the isolated channel attenuation, is the TX-to-RX coupling loss [40], [51] *TRX*. It is defined as:

$$TRX = -20\log_{10}\left|\frac{V_{RX}}{V_{TX}}\right| \tag{2.1}$$

where V_{TX} and V_{RX} are the voltage across the TX and RX antenna, respectively.

Indeed, the insertion loss is calculated with 50-Ω terminations, whereas the RX input impedance, $Z_{IN,RX}$, is usually quite high (i.e., in the order of a few kΩ). The fact that the system operates in resonant condition represents an additional reason for the unsuitability of *IL* as performance parameter.

The fabrication process, as in the traditional inductive devices, plays a fundamental role in determining the loss mechanisms taking place within both coil metal trace (i.e., series losses) and substrate (i.e., parallel losses). As regards parallel losses, main performance parameters of micro-antennas are generally more and more degraded as the substrate conductivity, σ_S, increases. Specifically, the degradation of antenna quality factors (Q_{TX} and Q_{RX}), magnetic coupling coefficient (k), and TX-to-RX coupling loss (*TRX*), turns to be quite strong for σ_S higher than 10^3 S/m, as shown in Fig. 2.4. The reported curves represent the results of parametric 3D-EM simulations carried out, at an operative frequency of 1 GHz, on a typical TX/RX micro-antennas configuration at a distance of 600 μm. Particularly, an optimum range of the substrate conductivity (i.e., between 10 S/m and 100 S/m) which is typical of standard RF CMOS and BiCMOS platforms, can be noticed. From these simulation results, quite good performance is expected also from package-

scale isolators integrated in technologies adopting high-resistivity substrate, such as CMOS-SOI or GaN on Si.

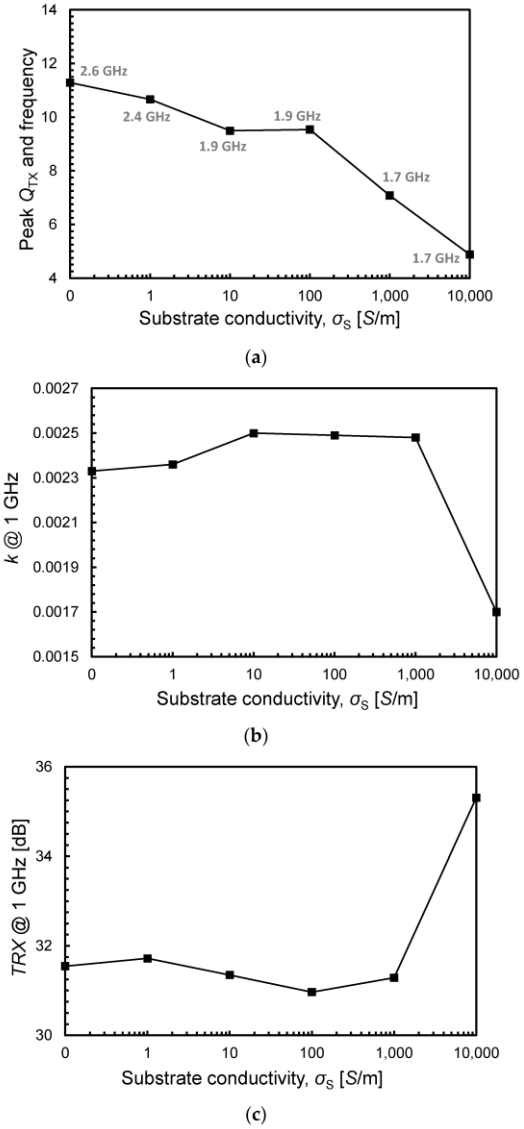


Fig. 2.4 Main micro-antenna performance parameters as a function of substrate conductivity: (a) peak TX quality factor and corresponding frequency, (b) magnetic coupling coefficient at the operative frequency, (c) TX-to-RX coupling loss in open circuit in resonance condition [40].

Unfortunately, galvanic isolated interfaces are also required in standard BCD platforms, largely used in power applications (e.g., gate drivers). Since such semiconductor technologies exploit very highly doped substrate ($\sigma_S > 10^4$ S/m), additional challenges are posed as far as micro-antenna design is concerned. In particular, the TX-to-RX coupling loss in resonance condition is worsening by more than 4 dB for a substrate conductivity of 10^4 S/m, as shown in Fig. 2.4(c).

The main design goal is to minimize the TX-to-RX coupling loss i.e., maximizing the induced voltage at the RX antenna for a given voltage at the TX one. Therefore, it is useful to figure out more precisely the dependency of the voltage amplitude across the RX coil from main channel electrical parameters. For this purpose, the simple circuital model of the isolated link at the operative frequency displayed in Fig. 2.5 can be adopted.

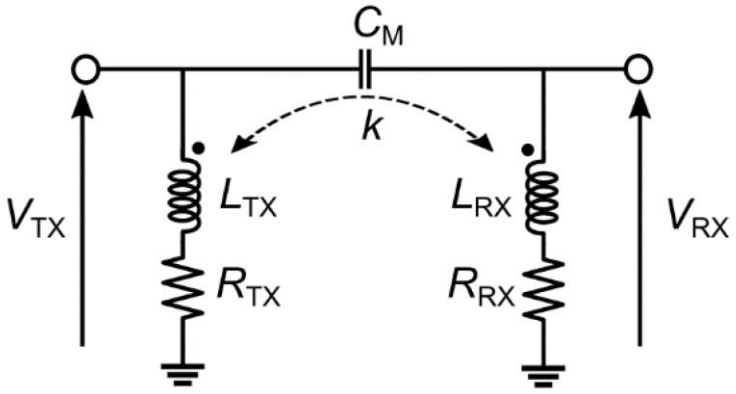


Fig. 2.5 Simplified model of the isolated channel [40].

It takes into account the overall micro-antenna losses (i.e., both series losses and parallel losses) by means of two equivalent resistances, R_{TX} and R_{RX}, series connected to the equivalent antenna inductances, L_{TX} and L_{RX}.

Magnetic and electric couplings between TX and RX antennas are modeled by the magnetic coupling factor, *k*, (or equivalently the mutual inductance, *M*) and the parasitic capacitance, C_M, respectively. Due to the high value of the RX input impedance, open circuit condition can be assumed, thus the following equation is drawn:

$$V_{RX,OC} = \frac{j\omega M + j\omega C_M(Z_{TX}Z_{RX} + \omega^2 M)}{Z_{TX} + j\omega C_M(Z_{TX}Z_{RX} - \omega^2 M)} V_{TX} \tag{2.2}$$

where Z_{TX} and Z_{RX} stand for the equivalent ohmic-inductive series impedance of the TX and RX antenna, respectively.

Since in actual implementations the parasitic capacitance value is very low (i.e., below 5 fF), its coupling effect can be neglected. Therefore, equation (2.2) is simplified as follow:

$$\left|\frac{V_{RX}}{V_{TX}}\right|_{OC} = \frac{kN}{\sqrt{1 + \frac{1}{Q_{TX}^2}}} \tag{2.3}$$

where *N* is the turn ratio defined as:

$$N = \sqrt{\frac{L_{RX}}{L_{TX}}} \tag{2.4}$$

From equation (2.3), which can be used as a simple but effective design expression, it is evident that minimizing *TRX* calls for the maximization of the magnetic coupling coefficient, turn ratio, and TX antenna quality factor. It is worth noting that the dependency of equation (2.3) on the *Q*-factor is typically negligible. For instance, by considering Q_{TX} equal to 4, the ratio between the induced voltage and the transmitted one, in open circuit

condition, can be approximated to the *kN* product with an error of only 3% compared to the value given by (2.3).

As far as the antenna shape is concerned, although polygonal and circular spirals enable higher quality factors, the use of square or rectangular coils is recommended to maximize the EM coupling. The aspect ratio of a rectangular antenna, *AR*, (i.e., ratio of its longer-facing side to its shorter side) must be optimized by accounting for contrasting performance, such as the *Q*-factor and the EM coupling. Indeed, the higher the aspect ratio the lower the quality factor due to increased current crowding into the inner windings. Regarding instead the coupling, there is an optimal value of *AR* that maximizes the magnetic coupling coefficient, as demonstrated by the EM simulation results reported in Fig. 2.6. Furthermore, if bidirectional channels are present, the TX-to-RX cross-talk plays a key role in defining the antenna aspect ratio. In fact, a high *AR* value turns to be useful to reduce the parasitic EM coupling between different adjacent channels.

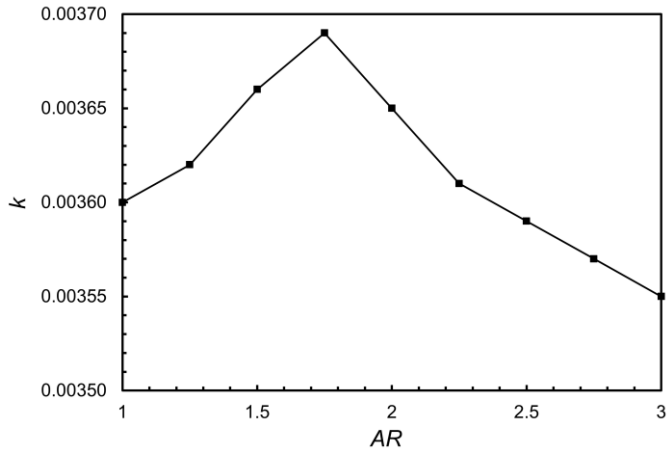


Fig. 2.6 Simulated magnetic coupling factor, *k*, as a function of antenna aspect ratio for a typical TX/RX micro-antennas configuration.

The layout of the TX antenna must comply with the adopted oscillator topology. Indeed, a standard not symmetric spiral such that one shown in Fig. 2.7(a), can be exploited in a complementary cross-coupled oscillator, whereas a symmetric configuration is mandatory to ensure the central tap connection for the supply voltage when a D-class oscillator is used. As far as symmetric antennas are concerned, two different solutions are feasible. The first layout (see Fig. 2.7(b)) consists of two identical series-connected coils in a U-shape fashion. This configuration, rather the S-shape one [48], is adopted to increase the EM planar coupling, since the current flowing in the antenna has the same direction (i.e., clockwise or counterclockwise) in both single windings. Alternatively, to achieve a better inductance-to-area ratio a fully symmetric coil geometry can be adopted as shown in Fig. 2.7(c). However, this second solution should be preferred only when a technology providing sufficiently thick metal layers along with low substrate conductivity is used. Otherwise, unacceptable *Q*-factor degradation due to the higher number of required underpasses will occur.

The starting point in the micro-antennas design is the definition of their layout parameters (i.e., the number of turns, n, the inner diameter, d_{IN}, the metal width, w, and the metal spacing, s) to set the low-frequency inductance values. In this regard, several closed-form equations are available in literature [60], [61], also exploiting the dependency from the metal thickness, t, to improve the accuracy for high t/w ratio. In order to increase the step-up ratio, the RX coil inductance, L_{RX}, must be maximized. However, the inductance value is upper bounded by the input parasitic capacitance of the RX front-end which should be kept as low as possible. A general design guideline for the

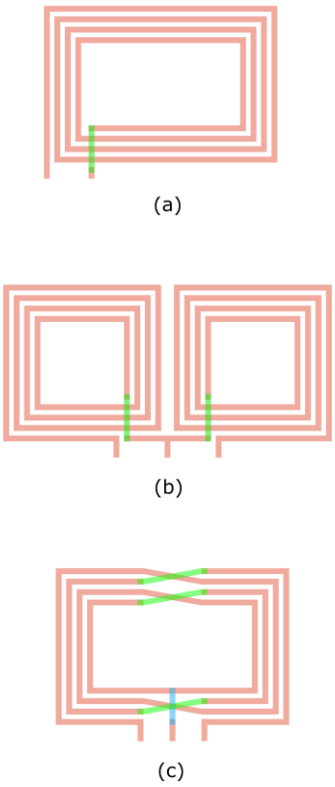


Fig. 2.7 Micro-antenna layout: (a) standard not symmetric single coil, (b) symmetric two series-connected coils, (c) fully symmetric coil.

RX antenna is using a small (i.e., even the minimum allowed by the fabrication technology) metal width, *w*, along with a high number of turns to achieve the highest value of the inductance-to-area ratio thus the highest self-resonance frequency (*SRF)*. Moreover, it is worth noting that since the input impedance of the RX front-end is typically high, the degradation of Q_{RX} due to a small width does not significantly affect the RX induced voltage amplitude. As far as the TX antenna is concerned, lowest inductance value, L_{TX}, compatible with proper operating conditions of the RF oscillator, must

be set. Indeed, on the one hand L_{TX} should be minimized to achieve higher N, on the other hand a proper $\omega_{RF}Q_{TX}L_{TX}$ product is necessary to ensure both low startup time and power consumption of the oscillator. Therefore, in designing the TX antenna, large metal width (i.e., high Q-factor) along with low number of turns (i.e., low inductance value) are preferred.

2.3.2. Micro-antenna optimization

This subsection proposes an optimized design flow following the abovementioned guidelines, which has been validated on a package-scale isolator integrated in a 0.32-μm BCD technology by STMicroelectronics. This technology platform had been chosen since it is widely adopted in high-voltage applications both in automotive and industrial fields. Furthermore, laterally diffused metal-oxide-semiconductor (LDMOS) transistors, well suited to implement a D-class oscillator, are available. The process provides a back-end-of-line (BEOL) with three thin Al layers along with a top thick Cu metal and a very conductive silicon substrate (i.e., σ_S is about 10^4 S/m). The adoption of such technology is particularly useful to highlight some design issues. Indeed, the high value of σ_S turns to be critical in terms of EM coupling, as show in Fig. 2.4, thus a careful optimization of the micro-antennas is required.

The design of the package-scale isolator has been carried out by means of EM simulations of micro-antennas. Although time-consuming, a 3D full-wave simulator (i.e., Ansoft HFSS) was preferred to a more traditional 2D (i.e., Keysight ADS Momentum) one due to its higher accuracy in terms of EM coupling when the substrate conductivity is quite high. Indeed,

probably due to its inability to distinguish each antenna dice, a significantly lower TX-to-RX coupling loss is expected by 2D simulator [40]. A 3D-view of the isolator simulated in HFSS environment is given in Fig. 2.8. As far as the simulation set-up is concerned, a box of molding compound surrounding the two dies was encased within a box of air. A first-order absorbing boundary condition (ABC) was assigned on the whole air-box surface except for the two regions under the chip frames where perfect-E boundary conditions were held. Three lumped ports for each micro-antenna, connected to the coil terminals and central tap respectively, are used to excite the system. A finite tetrahedral first-order elements mesh, adaptively refined through ten steps, was adopted. To achieve higher accuracy, an additional mesh refinement was exploited in the metal traces and in the molding compound area between the chips. Finally, the solution frequency was equal to the working frequency, f_{RF}, while a wider frequency sweep from 0.1 GHz up to 8 GHz was set.

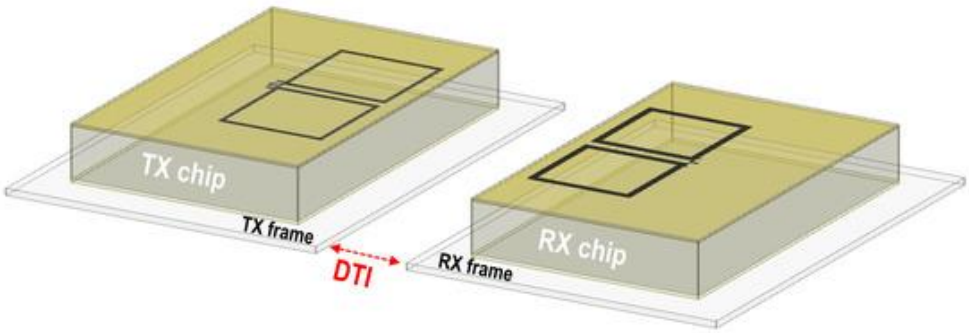


Fig. 2.8 3D EM simulation view of TX and RX micro-antennas for a package-scale galvanic isolator [40].

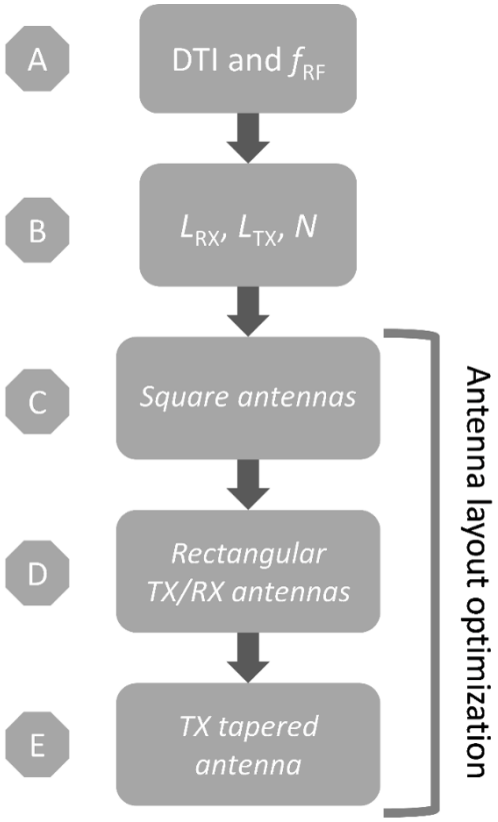


Fig. 2.9 Simplified block diagram of the proposed design flow [40].

The adopted design flow is schematically illustrated in the block diagram of Fig. 2.9. In the first step A, the DTI between chips and RF carrier frequency are set. The distance through isolation must comply with both the desired isolation rating and packaging/assembling issues. On the other hand, the RF carrier frequency is upper limited by the oscillator operation in terms of current consumption and can be subjected to other constraints depending on the specific application. In this design example, f_{RF} has been set equal to 1.5 GHz whereas a DTI of 500 μm has been chosen to achieve an isolation rating of 20 kV whit standard molding compound ($\varepsilon r = 5.5$). In In step B, both

TX and RX antenna inductances are properly chosen. The starting point is the RX antenna inductance, L_{RX}, which must be set to the highest value compatible with the input capacitance of the RX front-end. Then the turn ratio, N, is maximized by using the lowest value of the TX antenna inductance, L_{TX}, ensuring the RF oscillator to be properly operated within a given current budget. In this case the inductances were set around 7 nH and 78 nH for the TX and RX coils, respectively, achieving N higher than 3.

The last part of the proposed flow diagram (i.e., steps C, D, and E) concerns the antenna geometry optimization to the aim of maximizing the EM coupling. Throughout the whole process both the inductance values at the operative frequency and the step-up ratio are kept broadly constant. In the initial antenna optimization step (namely step C of Fig. 2.9), TX and RX coils have been designed according to the general guidelines discussed in Subsection 2.3.1. Due to high substrate conductivity and given that only one thick metal is available, square antennas with two windings in a U-shape fashion (see Fig. 2.7(b)) have been designed, thus avoiding further Q-factor degradation due to underpasses. The minimum allowed metal trace (i.e., 1.6 µm) has been chosen for the RX antenna, whereas the TX spiral width has been set to ensure a proper antenna ωQL. For instance, adopting a D-class oscillator assuming a current budget of 15 mA, a minimum value of the TX Q-factor of about 4 must be guaranteed. Moving to the next optimization step (D in Fig. 2.9), the rectangular shape is adopted for both antennas with the aim of improving the EM coupling thanks to longer facing sides. The aspect ratio of the RX antenna has been increased up to 1.3, while only a slight variation of AR is exploited for the TX antenna avoiding Q-factor deterioration. In the last step E, further optimization is carried out by using a

tapered coil configuration (i.e., using a variable width in the same coil). Specifically, an improvement of the coupling factor due to a reduction of the metal width on the facing side has been demonstrated [40], thus this layout was adopted for the TX antenna. As regards the RX coil, since its width has already been minimized, additional improvements cannot be achieved by means of a tapered layout.

Table 2.2 Main geometrical parameters of the designed antennas [40].

Antenna Layout	**TX antenna**					**RX antenna**				
	AR	*w* [μm]	*s* [μm]	*n*	$d_{out,max}$ [μm]	*AR*	*w* [μm]	*s* [μm]	*n*	$d_{out,max}$ [μm]
C	1	4	1.5	2	306	1	1.6	1.7	6	306
D	1.03	7	1.5	2	345	1.3	1.6	1.7	6	345
E	1.03	1.6/9.8	1.5	2	345	1.3	1.6	1.7	6	345

Geometrical parameters of TX and RX antennas for each optimization step are summarized in Table 2.2. It is worth mentioning that the TX coil perimeter increases going from step C to step D, thus allowing an effective increase of the metal width (from 4 to 7 μm) to keep the L_{TX} value almost constant. Antenna inductance and *Q*-factor curves are displayed in Fig. 2.10 for each layout configuration. No significant performance variations occur in the RX antenna from design step C (see Fig. 2.10(b)) to D, while the coil layout remains the same from D to E. As shown in Fig. 2.10(a) the increase of the TX antenna parasitic capacitance produces a slight reduction of its *SRF*, while the *Q*-factor value at the working frequency is always sufficient to ensure a proper operation of the RF oscillator. Thanks to the antenna optimization procedure, the magnetic coupling factor, *k*, is improved by about

19% from steps C to E, which, in turn, produces a reduction of the TX-to-RX coupling loss in open circuit and resonance condition of about 1.7 dB.

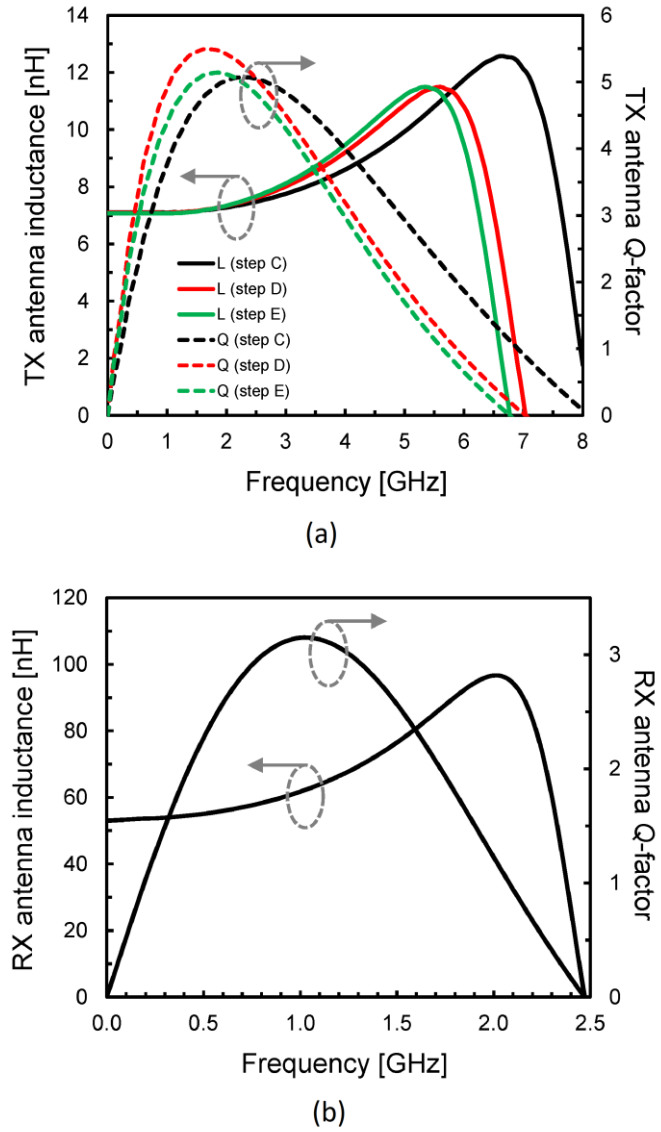


Fig. 2.10 Inductance and *Q*-factor for each optimization step: (a) TX antenna, (b) RX antenna [40].

2.4. Capacitive-Coupled Class-D Oscillators

2.4.1. Oscillator topology description

As claimed in Section 2.2, the well-known class-D oscillator represents a remarkable solution for package-scale galvanic isolators providing high oscillation voltage. However, it suffers from two significant drawbacks. On the one hand, to ensure safe operation this topology requires special devices able to withstand very high voltages, such as LDMOS or GaN HEMT. On the other hand, high oscillation amplitude results in significant current consumption. In this section, a novel recently patented oscillator topology [62], [63] is presented. It has been conceived for isolated data link based on RF planar coupling with the aim of overcoming the main disadvantages of a traditional class-D oscillator. Specifically, the proposed topology takes advantage of current-reuse and voltage-combining techniques, along with capacitive coupling to produce high voltage across the RX antenna, meanwhile keeping low TX front-end consumptions. Moreover, this oscillator enables safe operation of standard MOS transistors (i.e., with a low breakdown voltage) with high supply voltages.

The simplified schematic of the proposed topology is shown in Fig. 2.11. It includes two identical synchronized class-D oscillators (i.e., *OSC 1* and *OSC 2*) each one loaded with a TX micro-antenna, $L_{TX1,2}$. The two oscillators are stacked between the supply voltage, V_{DD}, and ground sharing the same current (i.e., current-reuse configuration). TX antennas must exploit symmetric configuration providing a center tap for the supply voltage and oscillator interconnection, respectively. Robust frequency/phase

synchronization is ensured by pure capacitive coupling between the oscillators achieved by means of two sufficiently high capacitors, C_S [64], [65]. By setting the central tap voltage, V_O, to $V_{DD}/2$, each oscillator produces half oscillation amplitude (i.e., V_{TX1} and V_{TX2}) of a traditional class-D with half current consumption. Finally, due to voltage combining at the RX antenna, L_{RX}, almost the same voltage of a traditional class-D oscillator is produced.

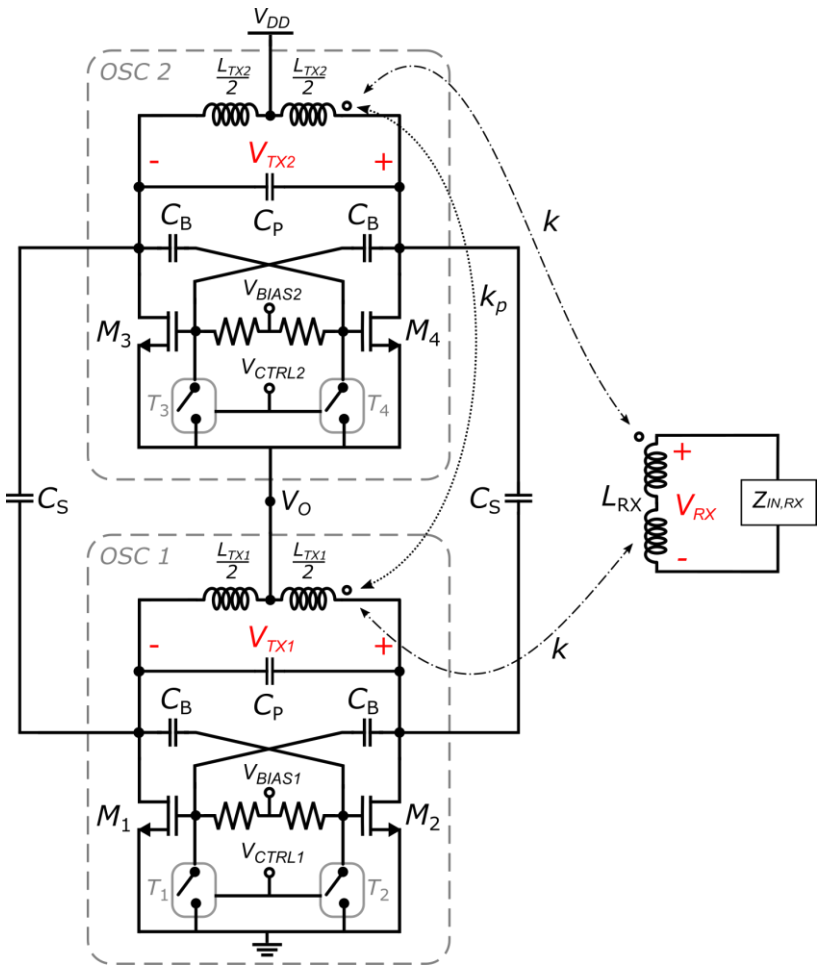


Fig. 2.11 Simplified schematic of capacitive-coupled stacked class-D oscillators.

Using class-D oscillator equations reported in [56] and neglecting losses, the peak of oscillation voltages, $V_{TX1,2}$, can be calculated by the following expression:

$$V_{TX,peak} = V_{DD}\left(\frac{1}{2} + \sqrt{\frac{\alpha^2\pi^2}{16} + \frac{1}{4}}\right) \approx 1.64V_{DD} \tag{2.5}$$

where α is given by:

$$\alpha = \frac{1}{2} + \sqrt{\frac{1}{4} + \frac{4}{\pi^2}} \approx 1.3 \tag{2.6}$$

Moreover, ignoring all the capacitive contributions, a simple equation for the average current flowing into the oscillators can be drawn:

$$I_{avg} \approx \frac{5V_{DD}}{4\pi f_{osc} Q_{TX} L_{TX}} \tag{2.7}$$

where f_{osc} is the oscillation frequency given by:

$$f_{osc} = \frac{\sqrt{2}}{2\pi\alpha}\sqrt{\frac{1}{L_{TX}}} \tag{2.8}$$

The resulting voltage at the RX antenna due to the combining of the TX oscillation voltages, $V_{TX1,2}$, can be easily evaluated in open circuit condition (it is reminded that the RX input impedance, $Z_{IN,RX}$, is typically high). By considering the 3 micro-antennas as a system of lossless coupled inductors the following relations can be written:

$$\begin{cases} V_{TX1} = j\omega L_{TX1} I_{TX1} + j\omega M_p I_{TX2} \\ V_{TX2} = j\omega M_p I_{TX1} + j\omega L_{TX2} I_{TX2} \\ V_{RX} = j\omega M I_{TX1} + j\omega M I_{TX2} \end{cases} \tag{2.9}$$

where M is the mutual inductance between L_{TX1} (or L_{TX2}) and L_{RX}, while M_p stands for the parasitic mutual inductance between the two TX coils.

The first two equations of (2.9) can be seen as a linear system whose unknowns are the current flowing in the TX antennas I_{TX1} and I_{TX2}. By solving the system, we obtain:

$$\begin{cases} I_{TX1} = \dfrac{V_{TX1} - k_p \sqrt{\dfrac{L_{TX1}}{L_{TX2}}} V_{TX2}}{j\omega L_{TX1}(1 - k_p^2)} \\ I_{TX2} = \dfrac{V_{TX2} - k_p \sqrt{\dfrac{L_{TX2}}{L_{TX1}}} V_{TX1}}{j\omega L_{TX2}(1 - k_p^2)} \end{cases} \tag{2.10}$$

where k_p is the parasitic coupling factor which corresponds to M_p. Since the TX coils have the same inductance, L_{TX}, across which the same voltage, V_{TX}, is generated, the two currents are equal. Hence, the following expression is achieved:

$$I_{TX} = \frac{V_{TX}}{j\omega L_{TX}(1 + k_p)} \tag{2.11}$$

By substituting (2.11) in the last equation of system (2.9) a simple expression for the voltage induced across the RX antenna in open circuit is finally obtained:

$$V_{RX,OC} = \frac{2kN}{1 + k_p} V_{TX} \tag{2.12}$$

where N is the turn ratio as defined in (2.4).

Looking at equation (2.12), it is clear that the parasitic magnetic coupling factor, k_p, must be kept as small as possible to maximize the RX induced voltage. It is worth noting that no synchronization issues arise due to the low value of k_p. Indeed, unlike similar topologies based on magnetic or hybrid coupled oscillators [24], [25] in this case synchronization is guaranteed by means of pure capacitively coupling. Assuming $k_p \approx 0$, the presented topology provides the same oscillation voltage of a standard class-D oscillator with a 50% lower current consumption. Since the voltage amplitude reduction across the RX antenna with respect to the ideal case turns to be relevant (i.e., beyond 15%) as k_p approaches 0.2, it is recommended limiting the parasitic coupling to this value. Finally, it is pointed out that transistors $M_{1,4}$ must withstand about half the drain-source voltage of a traditional class-D oscillator. For this reason, the novel topology lends itself to be used even with low breakdown voltage devices, such standard CMOS ones.

As mentioned in Section 2.2, a turn on/off circuitry for the oscillator is required to modulate the RF transmitted signal. In this regard, four switches (T_1, T_2, T_3 and T_4), properly driven by two control signals, V_{CTRL1} and V_{CTRL2}, can be used, as shown in Fig. 2.11. Specifically, to ensure the correct switch on/switch off operation the two control signals must be shifted by the central tap voltage, V_O, at any given time. In this regard, a simple example of a circuit generating the shifted signal V_{CTRL2} exploiting operational amplifiers is reported in Fig. 2.12. It is worth noting that, thanks to capacitive coupling and current reuse configuration, forcing the start-up/shutdown of *OSC 1* by means of T_1 and T_2 should consequentially imply start-up/shutdown of *OSC 2*.

However, using four switches is highly recommended for better robustness against PVT variations.

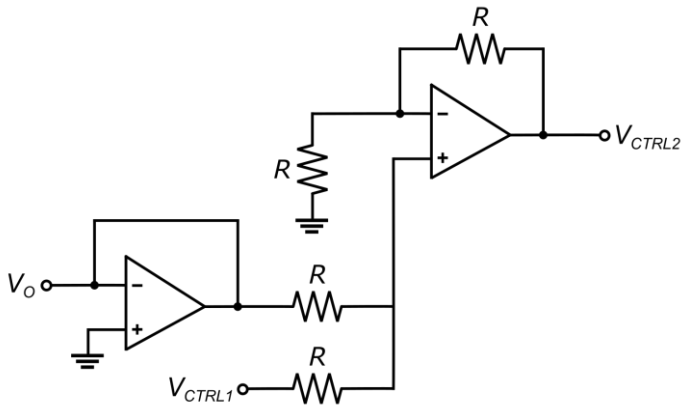


Fig. 2.12 Simple circuit for shifted control signals generation.

The topology can be generalized to the case of *n*-coupled stacked class-D oscillators, as displayed in Fig. 2.13. Frequency/phase synchronization is achieved by means of capacitive nearest-neighbor bilateral coupling [66], i.e., capacitors $C_{Si,i+1}$ are exploited to couple the adjacent stages *OSC i* and *OSC i+1*. Thanks to the voltage combining, almost the same amplitude of a traditional class-D oscillator is induced at the RX antenna, whereas the power consumption is ideally reduced by a factor of 1/*n* thanks to the current-reuse configuration. Specifically, the signal across the RX antenna, in open circuit and lossless conditions, turns to be a linear combination of the *n* transmitted voltages compactly expressed by:

$$V_{RX,OC} = \boldsymbol{M}_{TRX}^{T} \boldsymbol{L}_{TX}^{-1} \boldsymbol{V}_{TX} \tag{2.13}$$

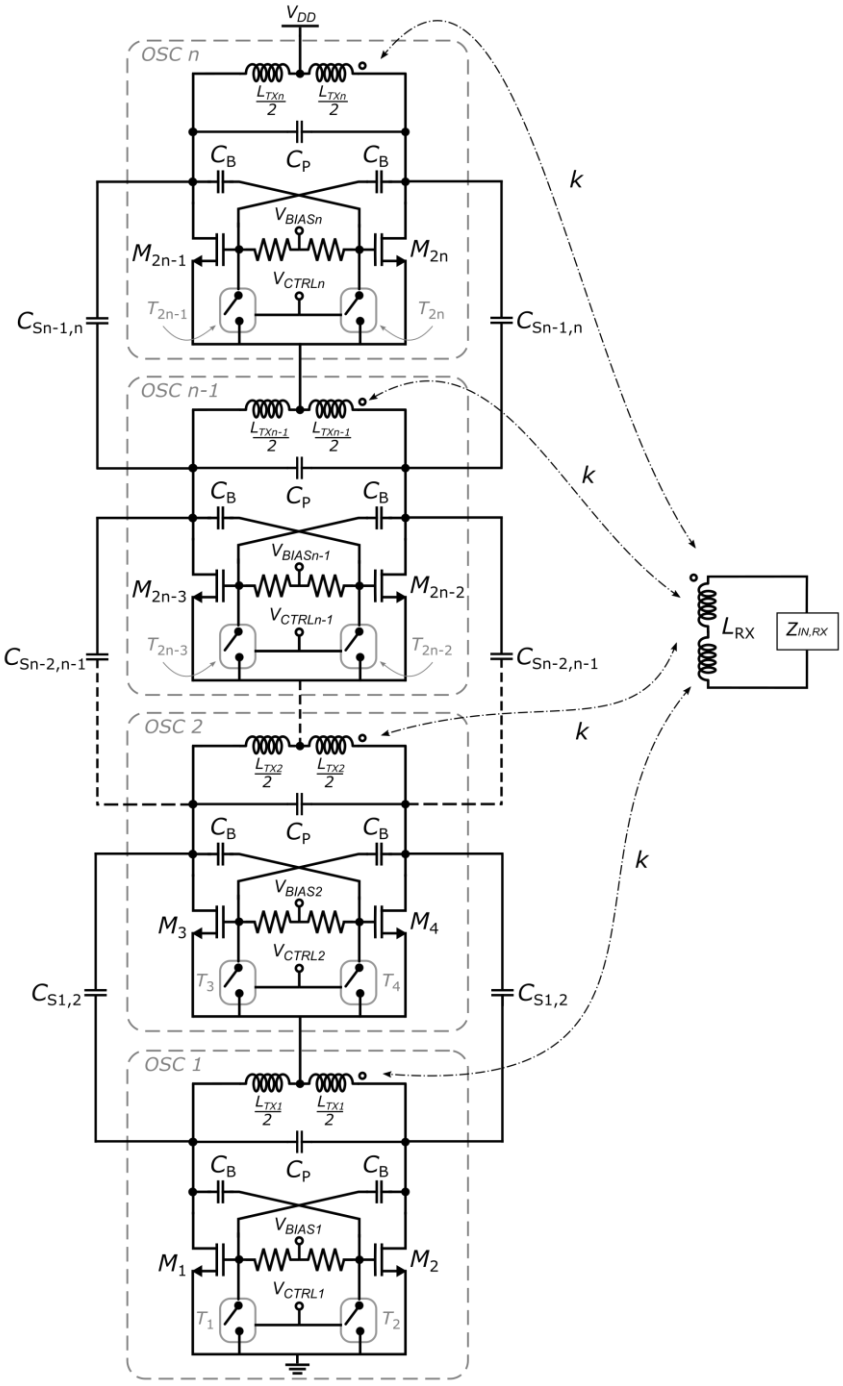


Fig. 2.13 Generalized schematic of the proposed oscillator topology for n-coupled stages.

$\boldsymbol{M}_{\mathrm{TRX}}$ stands for a vector whose components are the mutual inductances between each TX antenna and the RX antenna, $\boldsymbol{L}_{\mathrm{TX}}$ is the inductance matrix of the TX antennas and $\boldsymbol{V}_{\mathrm{TX}}$ is the vector of the oscillation voltages. It can be simply proved that the last equation turns into (2.12) when n=2. The general expression (2.13) is quite complicated, thus cannot be used as an effective design formula. Hower in actual implementation large area occupation of antennas along with layout issues hinder the exploitation of more than three stacked coupled oscillators. In that case, under some simplifying assumptions, the following expression can be drawn:

$$V_{RX,OC} = \frac{3 - 4k_p}{1 - 2k_p^2} kNV_{TX} \tag{2.14}$$

Finally, for the sake of completeness, the generalization of equations (2.5) and (2.7) to the case of n coupled cells is reported below:

$$V_{TX,peak} = \frac{V_{DD}}{n}\left(1 + \sqrt{\frac{\alpha^2\pi^2}{4} + 1}\right) \approx \frac{3.27}{n} V_{DD} \tag{2.15}$$

$$I_{avg} \approx \frac{5V_{DD}}{2\pi n f_{osc} Q_{TX} L_{TX}} \tag{2.16}$$

2.4.2. Oscillator design and validation

The proposed oscillator topology requires at least two TX micro-antennas, thus the issue arises of how to effectively place the coils with respect to each other. Although traditional configurations adopted for integrated transformers (i.e., stacked, interleaved and tapped one) enable low

area consumption, these arrangements cannot be used due to high magnetic coupling between coils. Indeed, the higher the magnetic coupling factor between TX antennas, k_p, the lower the RX induced signal according to (2.12), as discussed in the previous subsection. Two TX antenna configurations which can be exploited within capacitive-coupled class-D oscillators are displayed in Fig. 2.14. The simplest arrangement consists of two identical TX coils placed at a distance d_{TX}, as shown in Fig. 2.14(a). A less than linear decay of k_p has been observed by means of EM simulations whereas k is almost constant, as reported in Table 2.3. Therefore, it is suggested to set d_{TX} to minimize the silicon area at the required level of induced RX voltage amplitude.

Table 2.3 Magnetic coupling coefficient as a function of dTX (DTI= 500 μm) [63].

d_{TX}	50 μm	100 μm	150 μm	200 μm	250μm
k	3.11 E-03	3.06 E-03	3.01 E-03	2.95 E-03	2.90 E-03
k_p	3.92 E-02	2.54 E-02	1.81 E-02	1.36 E-02	1.06 E-02

An alternative configuration (see Fig. 2.14(b)) consists of a partial overlapping of the TX antennas, obtained by diagonally shifting the coils from each other to reduce both k_p and the port-to-port capacitance. This solution allows saving area at the cost of a slight degradation of other performance parameters. Indeed, due to higher parasitic coupling the voltage across the RX antenna turns to be 10-15% lower than the first configuration. Moreover, the overlapped structure causes a reduction of the TX antenna self-resonance frequencies along with Q-factors deterioration due to heavier proximity effects. For these reasons the superimposition between TX spirals

should not be pushed beyond approximately 50%. The coupling coefficients between RX antenna and each of the TX antennas are not equal, then in equation (2.12) we refer to *k* as the average value. Finally, it is worth noting that the TX micro-antenna arrangements displayed in Fig. 2.14 can be easily generalized to the case of *n*-coupled oscillators.

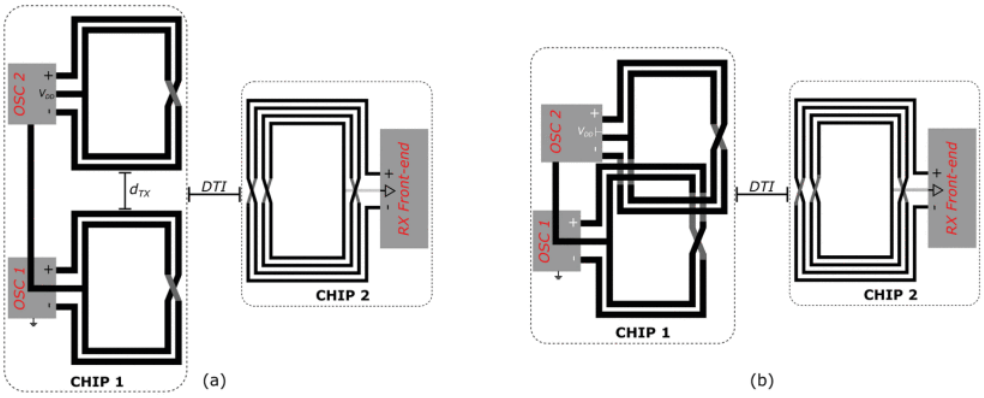


Fig. 2.14 Micro-antenna arrangements for the proposed oscillator topology (n=2): (a) separated layout, (b) overlapped layout [63].

The proposed topology is compared with the complementary cross-coupled oscillator, typically exploited in package-scale isolation when only standard MOS transistors are available, as stated in Section 2.2. Specifically, a 0.18-µm 1.8-V CMOS process, whose BEOL provides a top 3.7-um Cu metal layer along with two 0.5-µm Al ones, has been used. A three-coupled stacked class-D oscillator and a complementary cross-coupled one have been designed in this technology for an isolated data link operating at 2 GHz. A DTI of 500 µm has been set enabling high isolation rating of around 20 kV with standard molding compound. To perform a fair comparison, the same receiver antenna has been adopted in both implementations, also exploiting a

similar step-up ratio value, N. The supply voltage, V_{DD}, has been properly set to guarantee safe operation limiting the oscillation drain-source voltage within the nominal value of 1.8 V. Consequently, the novel topology and the traditional one enables V_{DD} as high as 2.3 V and 1.6 V, respectively.

Micro-antennas have been designed according to the guidelines discussed in Section 2.3. Specifically, the RX antenna exploits a full symmetric layout (see Fig. 2.7(c)) as well as the three TX coils of the class-D stacked oscillator. A separated layout arrangement as shown in Fig. 2.14(a) has been preferred for the designed TX antennas with the aim of maximizing the RX induced voltage. On the other hand, not symmetric coil, as that one shown in Fig. 2.7(a), has been chosen for the complementary cross-coupled topology. Tables 2.4 and 2.5 summarize the geometrical parameters and EM-simulated performance of the designed antennas, respectively. It should be pointed out that symmetric and not symmetric TX antenna layouts provide similar inductance and quality factor at the operative frequency, f_{RF}.

Parametric simulations have been carried out in order to determine the value of C_s which ensures robust synchronization, as shown in Fig. 2.15. It has been observed that the coupled oscillators are definitively in phase for synchronization capacitances higher than about 1 pF, thus C_S has been set equal to 1.5 pF. The single-ended drain-source voltages are reported in Fig. 2.16 for both topologies, confirming oscillation operation within MOS device safe region. The peak value of the induced voltage at the RX antenna in open circuit and resonant condition turns to be 250 mV for the capacitive-coupled stacked class-D topology. On the other hand, the traditional complementary cross-coupled topology achieves a lower peak value (i.e., only 120 mV), which is below the minimum signal of 140 mV for

proper demodulation [51]. This comparison highlights that at high DTI values (i.e., very high isolation rating), the package-scale approach is enabled only by the proposed capacitive-coupled stacked class-D topology.

Table 2.4 Geometrical parameters of the designed micro-antennas [63].

Parameters	**TX antennas**		**RX antenna**	**Units**
	Capacitive-coupled stacked class-D	**Complementary cross-coupled**		
Configuration	Symmetric	Standard	Symmetric	-
No of turns, n	3	2	4	-
Metal width, w	12	9	5	µm
Metal width, s	3	3	5	µm
d_{out_MAX}	400	540	540	µm
d_{out_MIN}	350	510	320	µm
d_{TX}	10	-	-	µm

Table 2.5 EM-simulated performance parameters of the designed micro-antennas [63].

Parameters	**TX antennas**		**RX antenna**	**Units**
	Capacitive-coupled stacked class-D	**Complementary cross-coupled**		
Low-frequency inductance	6.2	6	14.5	nH
Inductance @f_{RF}	6.6	6.5	19.4	nH
Peak Q-factor	17	17.5	11.3	-
Q-factor @f_{RF}	17	17.2	10.9	-
SRF	6.40	6.45	3.9	GHz
k @f_{RF}	2.3 E-03	3.2 E-03	-	-
k_p @f_{RF}	5.9 E-01	-	-	-
N @f_{RF}	1.71	1.73	-	-

Finally, Fig. 2.17 shows the PWM operation of the proposed oscillator with a data rate of 10 Mbit/s. The turn-on/off delays are equal to 24 ns and 6 ns, respectively, with a propagation delay of 3 ns between TX and RX signals and average current consumption of 3.65 mA (26% more than ideal value).

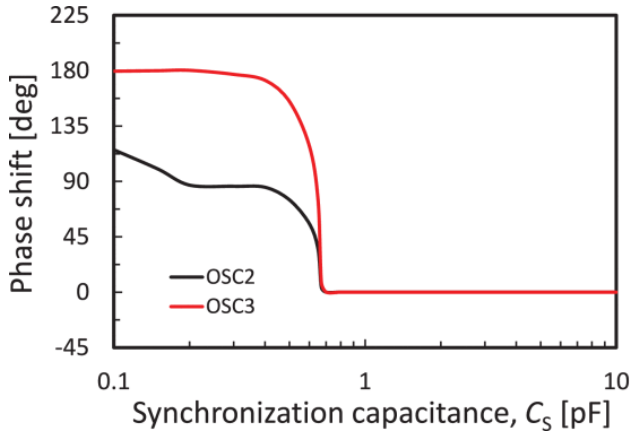


Fig. 2.15 Phase shift between *OSC 1* and *OSC 2* / *OSC 3* as a function of C_S [63].

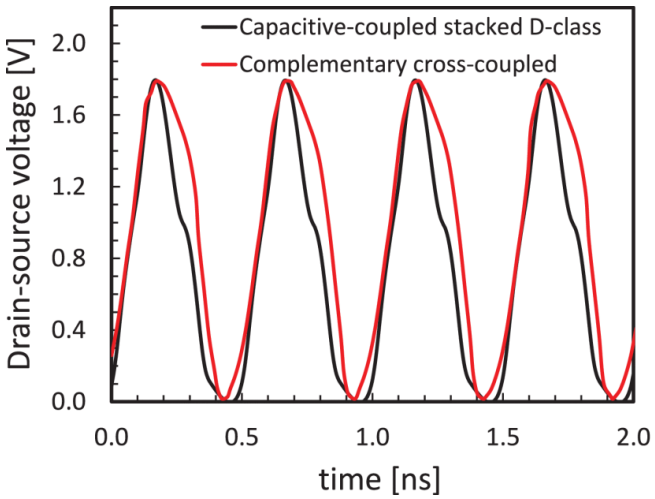


Fig. 2.16 Drain-source voltage for capacitive-coupled stacked class-D and complementary cross-coupled oscillators [63].

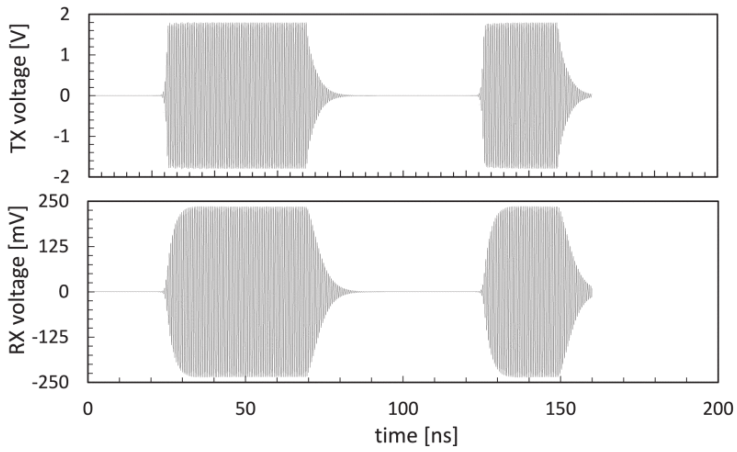


Fig. 2.17 Modulated voltage at TX/RX antennas for the proposed topology [63].

Chapter 3.

A GaN-integrated isolated data link for gate-driver applications

3.1. Introduction

This last chapter summarizes the most relevant activity that I carried out during my Ph.D. studies. It concerns the design and the characterization of an isolated data channel for gate-drive applications based on package-scale approach. In particular, I was involved in the design of the TX front-end, as well as micro-antennas. A 0.5-µm GaN on Si technology has been chosen to build up the isolated link in the perspective of a possible integration along with driver/power circuitry [67]. It is worth mentioning that, although GaN process seems really promising in the matter of fully integrated power

switching electronics, currently ICs design is very critical due to technological limitations. Indeed, the lack of p-channel devices, as well as large spreads of process parameters and high mismatches between GaN transistors [68], [69] have posed several design challenges for the isolation channel, as will be discussed below. A chip-on-board assembly has been realized to test the package-scale isolation link leading to a successful characterization. This activity has been performed in collaboration with STMicroelectronics within the EU Project GaN4AP [70]. It is worth mentioning that the choice to exploit a silicon substrate rather than a most common and performing silicon carbide (SiC) one has been carried out for cost and technology availability reasons.

The chapter is organized as follows. The system architecture with a focus on the design of main circuit blocks (i.e., TX font-end, micro-antennas and RX font-end) is presented in Section 3.2. Finally, experimental results are reported in Section 3.3.

3.2. System description

A simple block-diagram of the designed isolated data link is shown in Fig. 3.1. Chip A integrates the TX front-end including two coupled RF oscillators, *OSC 1* and *OSC 2*, employing current-reuse technique and two transmitter micro-antennas, L_{TX1} and L_{TX2}. The input PWM signal drives a switch on/switch off circuitry to properly turn on/off the oscillators simultaneously. Due to the near-field coupling between micro-antennas, the two on-off keying (OOK) modulated RF signals provided by the oscillators

are combined at the RX coil, L_{RX}, on Chip B. The RX front-end includes a rectifier stage that demodulates the signal across the RX antenna, followed by an amplifier to properly increase the voltage level. Finally, a buffer is exploited to perform a differential to single ended signal conversion to drive the power section. Since the EM coupling is extremely weak, the system has to be operated in resonance condition with all the micro-antennas tuned at the carrier frequency, f_{RF}, which is set to 2 GHz. The design of TX front-end, micro-antennas and RX front-end, along with some relevant information about the adopted technology platform and assembling, is detailed in the following subsections.

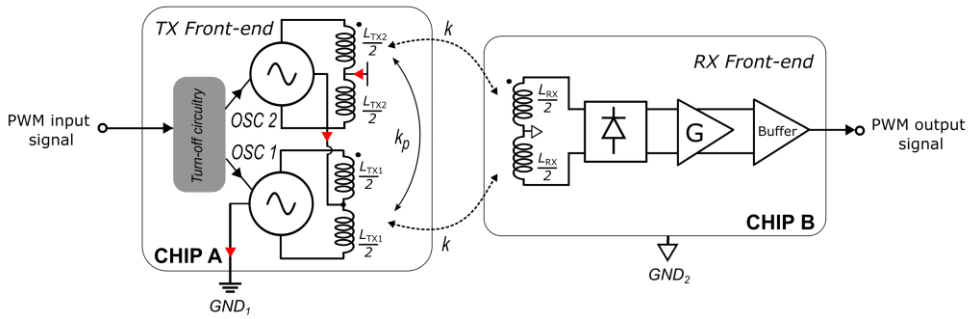


Fig. 3.1 Simplified block-diagram of the designed isolated data link.

3.2.1. Fabrication technology and assembling

Both chips of the isolation data link were designed and fabricated in a 0.5-µm GaN on Si process. The chosen technology features enhancement (E) and depletion (D) n-channel transistors, capacitors, and resistances. A 650-V power transistor is also available, which enables the integration of the isolated gate-driver control channel with the power section. The transition frequency,

f_T, and the maximum switching frequency, f_{max}, of the enhancement device are 9 GHz and 14 GHz respectively. The back-end-of-line (BEOL) consists of two thick AlCu metal layers (3 μm) and a thinner one (around 1 μm), which allow, along with the high resistivity substrate, to design inductive components with very good RF performance. Unfortunately, GaN technology parameters are affected by large spreads. For instance, the threshold voltage variation is more than 40% for both enhancement and depletion transistors. Moreover, transistor mismatches are very high compared to CMOS ones. Consequently, the bias point and the power consumption can be hardly set with accuracy. In this implementation the two chips were assembled side-by-side in the package lead frames at a DTI of 250 μm. A standard molding compound with a dielectric strength of 50 kV/mm has been used guaranteeing an isolation rating of about 12.5 kV along with a CMTI value higher than 200 kV/μs.

The use of GaN technology in implementing a package-scale isolated link for gate driver applications is promising since it allows the integration of the power section along with the data channel itself. Indeed, as already mentioned in Section 1.3, the perspective of a fully integrated approach including analog/digital control and power switching circuitries is quite attractive. Therefore, the main benefit of GaN process with respect to other technology platforms (i.e., CMOS and BCD) concerns the application field rather than the galvanic isolation itself. However, adopted GaN technology provides some inherent advantages which are reflected in the isolated channel performance. Specifically, the process adopts a high resistivity silicon substrate with respect to standard BCD technology enabling both quite high magnetic coupling coefficient and micro-antenna quality factor, as

extensively discussed in Section 2.3. In addition, the available metal back-end further contributes to the ohmic loss reduction in the antenna coils. Finally, thanks to the higher breakdown voltage of GaN transistors compared to CMOS one, large TX oscillation amplitude is achieved, and thus higher RX induced voltage is obtained.

3.2.2. TX front-end design

The RF oscillator represents the very bottleneck of the TX front-end, thus of the entire isolated data link, as already underlined in the previous chapter. Complementary cross-coupled topology cannot be adopted since the GaN process provides only n-channel transistors. On the other hand, although class-D oscillator can be exploited in this technology enabling large amplitude of the TX signal, it requires high current consumption. For these reasons an oscillator topology very similar to the one presented in Section 2.4, which takes advantage of current reuse and voltage combining techniques, has been used. The simplified schematic of the designed oscillator is displayed in Fig. 3.2.

The circuit consists of two stacked class-D oscillators (i.e., *OSC 1* and *OSC 2*) synchronized by means of two coupling capacitors, C_S. TX micro-antennas, L_{TX1} and L_{TX2}, are exploited as resonant inductors providing center tap for the supply voltage, V_{DD}, and oscillator interconnection, respectively. A current mirror (which is not shown in the schematic of Fig. 3.2 for the sake of simplicity) is used to set the gate voltage, V_{BIAS}, of transistors Q_{E1} and Q_{E2}. On the other hand, the top oscillator, *OSC 2*, is biased though the supply voltage itself in order to reduce the turn on/off time while avoiding

layout complexities. Setting the central tap voltage, *O*, around $V_{DD}/2$ each oscillator provides half oscillation amplitude of a standard class-D with a 50% lower current.

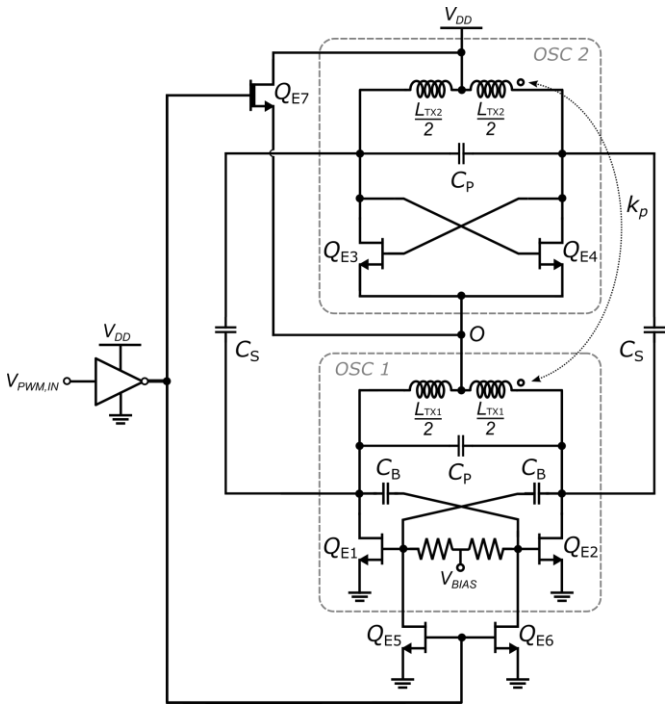


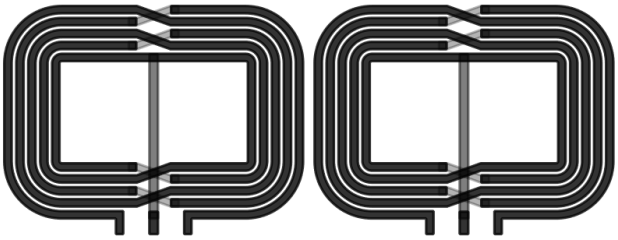
Fig. 3.2 Schematic of current-reuse capacitively coupled oscillators.

However, the induced signal at the RX coil turns to be slightly lower than the ideal case due to parasitic magnetic coupling between TX antennas, as expressed by equation (2.12). It is worth noting that, thanks to the reduced supply voltage of each oscillator (i.e., $V_{DD}/2$) the maximum gate-source voltage allowed by the technology, $V_{GS\text{-}MAX}$, turns to be higher than the oscillation voltage. Consequently, the two capacitances C_B can be set to a low value since no reduction of the gate-source voltages of Q_{E1} and Q_{E2} is required

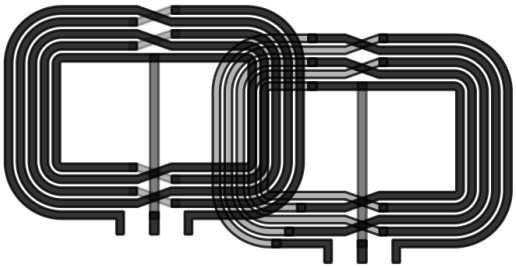
as usually occurs in class-D oscillators. As far as the turn on/off circuitry is concerned, the same PWM signal, $V_{PWM,IN}$, is employed to switch enhancement n channel transistors $Q_{E5,6}$ and depletion transistor Q_{E7}.

3.2.3. Micro-antennas design

As explained in the previous chapter, isolated data links based on package-scale isolation require an accurate design of the micro-antennas with a view to maximize the near field coupling, thus achieving a sufficiently high voltage across the RX coil. Since a voltage-combining technique with two TX spirals is exploited, antenna design is even more challenging (see Subsection 2.4.2). Specifically, two different antenna layouts have been designed. In the first design (i.e., layout A) two identical TX micro-antennas were placed at a distance, d_{TX}, of 20 μm. This value has been chosen as a trade-off between the antenna area occupation and the voltage amplitude at the RX spiral. In the second configuration (i.e., layout B), an overlapping of around 30% has been exploited by a shifting of 50 μm and 160 μm along the x (namely the channel direction) and y axis, respectively. The same RX antenna is adopted in both layout configurations. Since the BEOL provides high-quality metal layers along with low conductive substrate, fully symmetrical layout has been employed for the three antennas. Specifically, the spirals are made up by means of the top thick AlCu layer, whereas the two lower metals are used for underpasses and central tap. As far as the antenna shape is concerned, a rectangular form with rounded corners adopting an optimized aspect ratio has been used. The designed micro-antennas are shown in Fig. 3.3 while their main geometrical parameters are summarized in Table 3.1.



(a)



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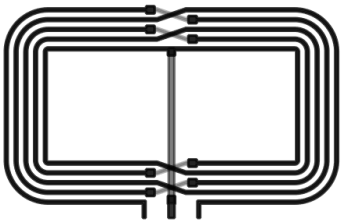

(c)

Fig. 3.3 Layout of the designed micro-antennas: (a) layout A with separated TX antennas, (b) layout B with overlapped TX antennas, (c) layout of the RX antenna.

Table 3.1 Geometrical parameters of the designed micro-antennas.

Parameters	TX antennas	RX antenna	Units
Number of turns, *n*	5	5	-
Metal width, *w*	12.8	5	µm
Metal spacing, *s*	8	12	µm
Max outer diameter, $d_{OUT-MAX}$	520	580	µm
Min outer diameter, $d_{OUT-MIN}$	370	340	µm
Aspect ratio, *AR*	1.4	1.7	µm

Table 3.2 Electrical parameters of the designed micro-antennas.

Parameters @ f_{RF}	Separated TX antennas (Layout A)	Overlapped TX antennas (Layout B)	RX antenna	Units
L	16.7	16.9/16.8	22.2	nH
Q-factor	13.1	11.6/10.4	7.8	-
k_P	0.2 E-02	5.1 E-02	-	-
k	4.3 E-03	4.6 E-03 / 4.0 E-03	-	-
N	1.15	1.15/1.15	-	-
SRF	4	4/3.9	4	GHz

The micro-antennas have been analyzed by means of 2D EM simulator Keysight ADS Momentum. The resulting electrical parameters are summarized in Table 3.2. Moreover, the inductance and *Q*-factor curves as a function of frequency are depicted in Fig. 3.4 and 3.5, for the TX and RX antennas, respectively. It is noted that overlapped TX spirals show lower quality factors, while maintaining the *SRF* almost unchanged. On the other hand, the magnetic coupling *k* is not degraded in layout B, whereas the parasitic coupling k_p is considerably higher (i.e., about 25 times). It should be

underlined that, despite having the same layout parameters (see Table 3.1), overlapped antennas exhibit different electrical performance since one antenna must use a lower (and less conductive) metal layer to avoid short circuits in the overlapped regions. Separated TX antenna configuration requires larger area compared to the overlapped one (about 8%) but it guarantees a higher induced voltage at the RX antenna (around 10%). Layout A has been finally chosen for actual integration since the area increment is negligible. It is worth mentioning that, although the general guidelines presented in Section 2.3.1 have been profitably followed, in this design the maximization of the TX antennas ωQL product (i.e., over 2 kΩ) rather than the step-up ratio, N, have been pursued. Indeed, a sufficient voltage amplitude across the RX antenna can be achieved even with quite low N due to high oscillation amplitudes provided by the GaN transistors.

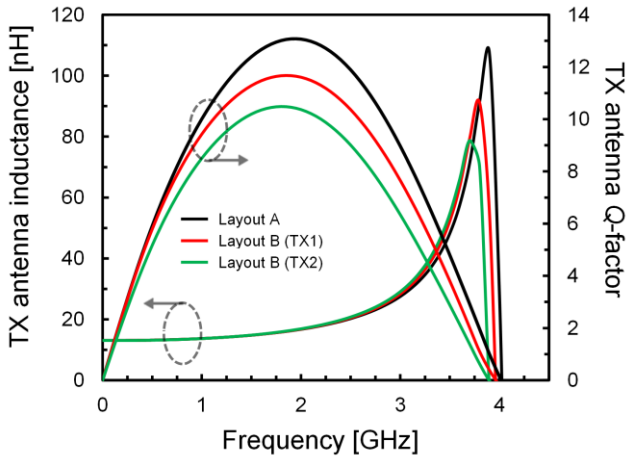

Fig. 3.4 Simulated inductance and Q-factor of the TX antennas.

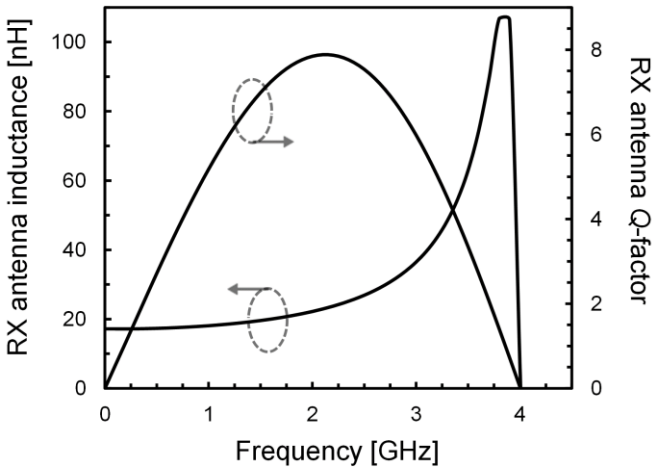

Fig. 3.5 Simulated inductance and *Q*-factor of the RX antenna.

Fig. 3.6 displays the performance of the isolated link in terms of micro-antenna insertion loss (*IL*) compared to the results in [21]. For the chosen DTI (i.e., 250 μm), the designed antennas exhibit an *IL* of 55 dB, which is around 2.5 dB lower than the value reported in [21]. Furthermore, it should be noted that voltage combining technique reduces the actual insertion loss of about 3 dB. However, as stated in Chapter 2 a most significant parameter which quantifies the channel attenuation in actual operative condition is the TX-to-RX coupling loss. This concept, which has been defined through equation (2.1), can be easily extended to the case of voltage combining with two TX micro-antennas as follows:

$$TRX = -20\log_{10}\left|\frac{V_{RX}}{V_{TX1}+V_{TX2}}\right| \qquad (2.1)$$

Fig. 3.7 reports the *TRX* value obtained with the RX antenna loaded with the RX input impedance, as a function of the DTI with and without (w/o)

resonance tuning at 2 GHz. It can be noted that resonance condition provides a reduction of the channel losses of about 15 dB. Specifically, a *TRX* around 30 dB is achieved with the selected DTI of 250 μm.

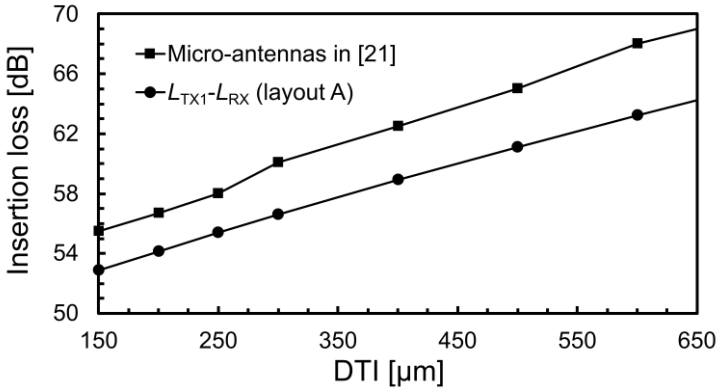

Fig. 3.6 Insertion loss of the micro-antennas with layout A and in [21].

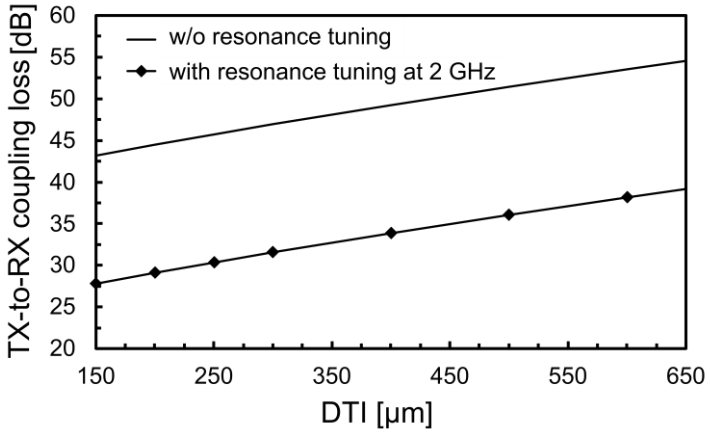

Fig. 3.7 Micro-antennas TX-to-RX coupling loss, *TRX*, with layout A.

3.2.4. RX front-end design

The RX front-end consists of the receiver antenna, L_{RX}, tuned at the operative frequency by means of the parallel capacitor, C_{RX}, a rectifier stage, a differential amplifier, and a buffer, as already shown in Fig. 3.1. The main block of the RX front-end is the rectifier since it extracts the envelope signal from the OOK modulated RF signal at the antenna, V_{RX}, while guaranteeing a significant conversion gain compensating for the high channel losses.

The simplified schematic of the rectifier stage is shown in Fig. 3.8. Specifically, a common source configuration with resistive load, R_L, is adopted ensuring good voltage gain along with low consumption [57], [71]. The rectifier bias current is set by means of a cascode mirror consisting of transistors Q_{E8-10} and $Q_{E11,12}$. Furthermore, the common-gate transistor, Q_{E11}, is included to the aim of reducing the capacitive effect on the rectifier input due to the gate-drain capacitances of the input pair, $Q_{E8,9}$. The RX micro-antenna is connected to the rectifier input by means of coupling capacitors, C_C, and its central tap is grounded to improve the CMTI. The envelope signal at the rectifier output, V_{RECT}, is fed to the amplifier and then to the buffer, thus recovering the PWM signal. However, the large PVT variations of the GaN technology produce a very high offset voltage at the amplifier input that hinders a correct reconstruction of the original signal. Therefore, the mixed analog/digital dynamic offset compensation technique in [21] was adopted. This technique also provides hysteresis to increase the receiver reliability against disturbances. It is worth mentioning that, differently from the RX front-end in [21], traditional current mirrors for current generators rather than the solution based on depletion transistors with degeneration resistance have been adopted [73].

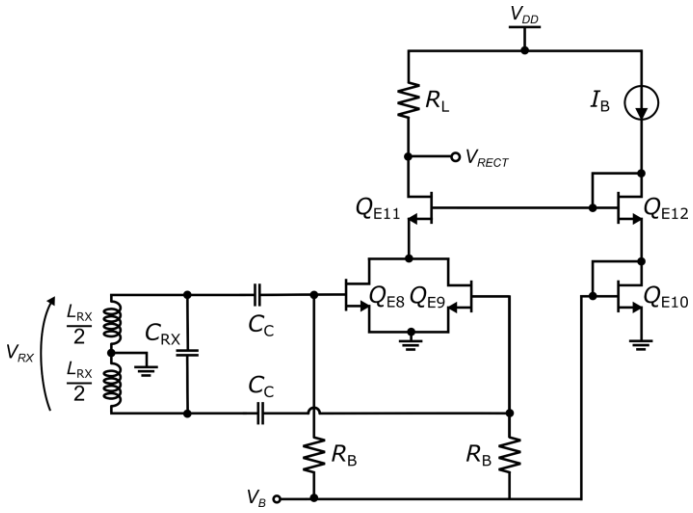

Fig. 3.8 Simplified schematic of the adopted rectifier stage.

3.3. Experimental results

The experimental validation of the designed galvanically isolated data link was carried out by means of a chip-on-board assembly with a DTI of 250 μm, as shown in Fig. 3.9. The TX and RX front-ends are placed at the left- and right-hand sides, respectively with the two TX antennas, $L_{TX1,2}$ and the receiver one, L_{RX}, labelled for the sake of readability. The isolation link occupies an overall GaN area of about 2.9 mm^2 including pads.

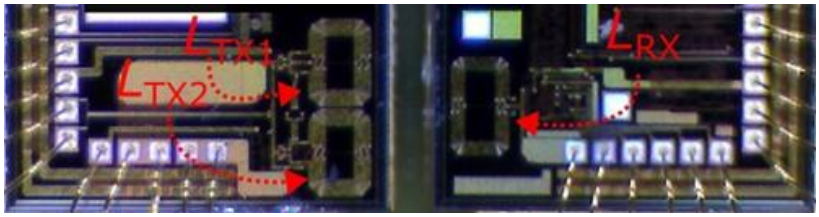

Fig. 3.9 Photograph of the chip-on-board assembly of the galvanically isolated channel.

The measurement set-up is schematically illustrated in Fig. 3.10. Five power supplies have been used to set the TX and RX supply voltages as well as the biasing of each circuit block. It is worth mentioning that the gain and output buffer are biased by the same power supply through a shared pad. The input PWM signal has been provided by a pulse function generator which can produce signals with maximum voltage and frequency of 5 V and 330 MHz, respectively. A spectrum analyzer with an absolute amplitude accuracy of 0.19 dB has been exploited to detect the RF carrier frequency at the output of an integrated buffer connected to the top oscillator (i.e., *OSC 2*). A 1-GHz bandwidth oscilloscope with 4 channels has been used to display and acquire the desired RF signals. Finally, the current consumptions of the oscillator, TX test buffer and RX front-end have been measured by means of three multimeters (not shown in Fig. 3.10 for the sake of simplicity).

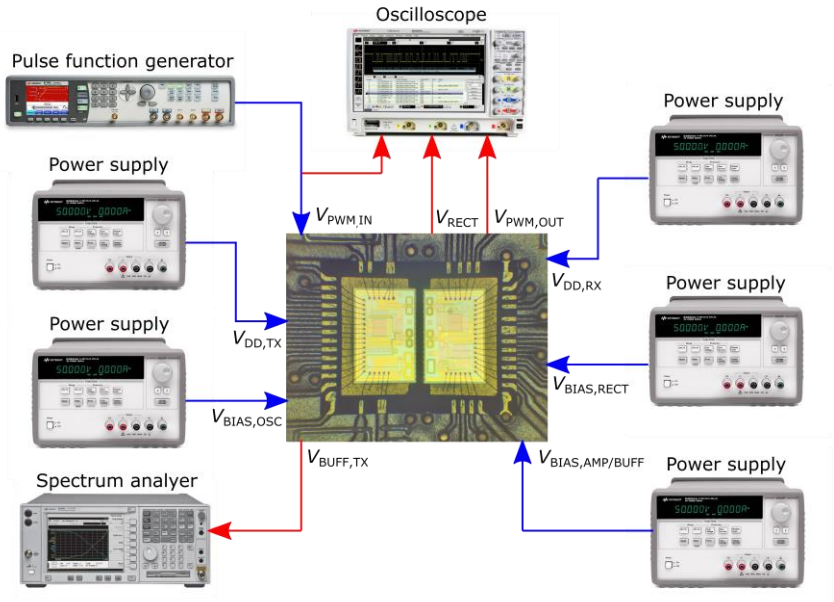

Fig. 3.10 Simplified diagram of the experimental set-up.

All measurements were performed at the nominal supply voltages. Specifically, a V_{DD} of 6 V, which is a typical value adopted in power switch drivers, has been set for the RX front-end. On the other hand, a lower supply (i.e., 5 V) has been selected for the TX front-end with a view to further reducing power consumptions. The measured signal spectrum at the TX buffer is displayed in Fig. 3.11. The peak frequency turns to be around 2.1 GHz, which is only 5% higher than the nominal oscillation frequency, f_{RF}. This difference is quite low considering the large spread of GaN process, and it is probably due to an incorrect evaluation of capacitive parasitcs. However, this discrepancy does not significantly affect the performance of the isolation channel. Since the buffer loss is about 14 dB, the oscillation amplitude of the top oscillator drains is estimated to be as high as 4.9 V.

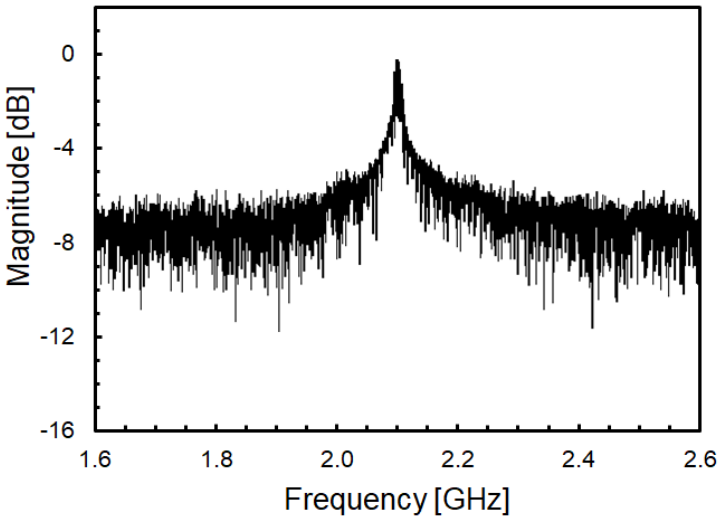

Fig. 3.11 TX oscillation signal spectrum of the top oscillator.

The isolated link was extensively tested up to a PWM frequency of 500 kHz with different values of the duty cycle (DC). The signal V_{RECT} captured at the rectifier output by means of a dedicated testing buffer, is displayed in Fig. 3.12. For a 500-kHz PWM input signal with DC= 50%, the rectified signal amplitude turns to be around 600 mV, while the propagation delay is about 25 ns. It is noted that this last value represents almost the overall estimated propagation delay of the whole isolation channel. Indeed, the effects on propagation delay due to subsequent stages of the RX front-end (i.e., amplifier and output buffer) can be considered negligible.

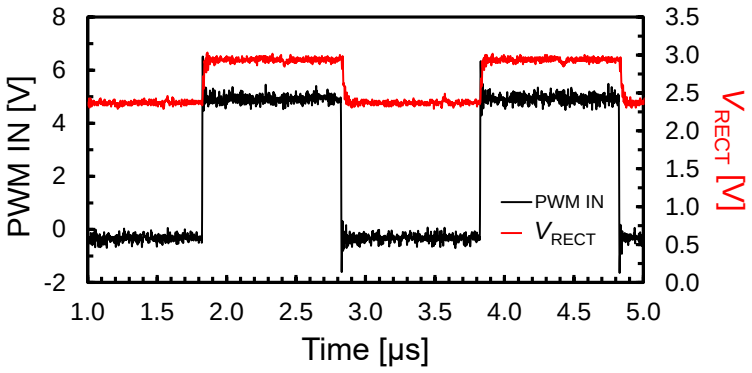

Fig. 3.12 Rectified signal, V_{RECT} (500-MHz PWM, DC=50%).

Fig. 3.13 depicts the operation of the isolation channel for 500 kHz PWM input signals at three DC values. Although the functionality of the designed data link is demonstrated, an abnormal deterioration of the propagation delay caused by the blocks after the rectifier is observed. This unexpected degradation was not present in the RX front-end in [21] that shares almost the same circuit blocks except for the current mirrors. This issue, which is currently under investigation, could be attributed to a bias

point drift in the amplifier and/or in the output buffer. This discrepancy between nominal operative conditions and effective ones is in turn probably due to the strong mismatches of GaN transistor along with the adoption of traditional current mirrors. The oscillator current consumption turns to be 2.7 mA for a DC of 50% while the test buffer and the RX front-end draw about 1 mA each.

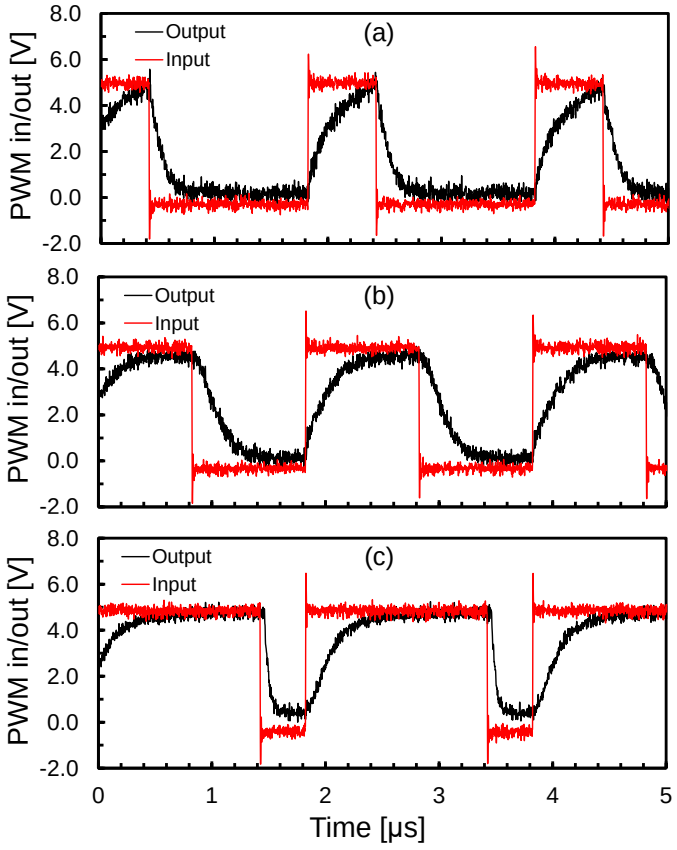

Fig. 3.13 500-kHz PWM signals: (a) DC=30%, (b) DC=50%, (c) DC=80%.

Table 3.1 Summarized performance and comparison with state of the art.

	CHIP-SCALE ISOLATION			**PACKAGE-SCALE ISOLATION**			
	Polyimide transformers	**On-chip SiO_2 capacitors**	**On-chip SiO_2 lateral**	**Stacked antennas**	**Planar antennas**	**Planar antennas**	**Planar antennas**
Reference	[73]	[74]	[75]	[32]	[50]	[21]	This work
No of channels	2	2	2	4	2	2	1
Data/PWM rate	1 MHz	1 MHz	80 Mbit/s	1 Mbit/s	500 Mbit/s	4 MHz	500 kHz
Propagation delay [ns]	44	28	15.5	42	n.a.	30	25(1)
Supply voltage [V]	5	3 / 5.5	5	3.3	1.8	6	5 / 6 (3)
Isolation	5.7 V_{RMS}	8 kV_{PK}	5 kV_{PK}	7 V_{RMS}	24 kV_{PK}	12 kV_{PK}(2)	12 kV_{PK}(2)
Current per channel [mA]	n.a.	n.a.	1.9 (4)	1.65	n.a.	5.3 (5)	3.7 (5)
Technology	n.a.	n.a.	0.25-µm CMOS	0.25-µm BiCMOS SOI	0.18-µm CMOS	0.5-µm GaN	0.5-µm GaN
CMTI [kV/µs]	150	100	650	n.a.	50	>250 (2)	>250 (2)
No. of dice	2	3	2	2	2	2	2
Area [mm^2]	n.a.	n.a.	0.95	n.a.	12.8(6)	5.8	2.9

(1) Measured at the rectifier output.
(2) Estimated.
(3) TX (Chip 1) / RX (Chip 2).
(4) At 1Mbit/s.
(5) w/o the output buffer (DC=50%).
(6) Estimated from die photos in [50].

In conclusion, the performance of the isolated data link is summarized in Table 3.3 compared with the state of the art of galvanic isolation techniques, considering both chip-scale and package-scale approaches,

respectively. In particular, voltage-combining and current-reuse techniques adopted in this isolation channel based on RF planar coupling demonstrated competitive performance with a reduction of about 37% and 30% of the TX front-end and overall link power consumption, respectively, compared to [21]. Finally, it is worth underling that the maximum PWM rate, estimated to be as high as 2 MHz in simulation, was limited to only 500 kHz in measurement due to the anomalous behavior of the blocks after the rectifier, as previously discussed.

APPENDIX A

Modeling of inductors in GaN technology

A. Introduction

This appendix presents the major results obtained in the framework of the development of RF GaN on Si technology by STMicroelectronics. The final goal of this activity will be the realization of the passive components required for the implementation of an integrated power amplifier for 5G applications in the sub-6GHz band. Currently, in fact, the technology has only the discrete transistor and therefore it is necessary to create micromodules to implement a complete power amplifier. The availability of passive components will

allow replacing the micromodule with an entirely on-chip system, substantially reducing both costs and space occupation. Particular attention has been given to the design, integration and consequent modeling of reactive components (i.e., inductors and capacitors). Indeed, it is well known that the main performance of an RF power amplifier (i.e., output power, efficiency and gain) are strongly dependent by the characteristics of the matching networks, which in turn are mostly determined by the inductive devices. In this context, I worked on the development of a lumped scalable circuital model for inductors which will be included in the process design kit (PDK) of the technology. This activity, which took advantage of extensive use of 2D EM simulator Advanced Design System (ADS) Momentum by Keysight, is discussed in detail in the next Section.

B. Lumped scalable model for inductors

A simple standard π-topology has been chosen as shown in Fig. A.1. The ideal inductor, L, is used to model the spiral and underpass inductances, as well as the magnetic coupling within the substrate. Two capacitors, C_{P1} and C_{P2}, (whose values are different due to asymmetric inductor layout) are adopted considering the capacitive effects towards the substrate. Moreover, a further capacitor, C_S, is exploited to take into account other capacitive effects. Specifically, parasitic capacitances thorough the inductor turns along with overlap between the spiral and the underpass are considered. Finally, ohmic and substrate losses are modeled by means of frequency-variable resistances, R_S and R_P, respectively.

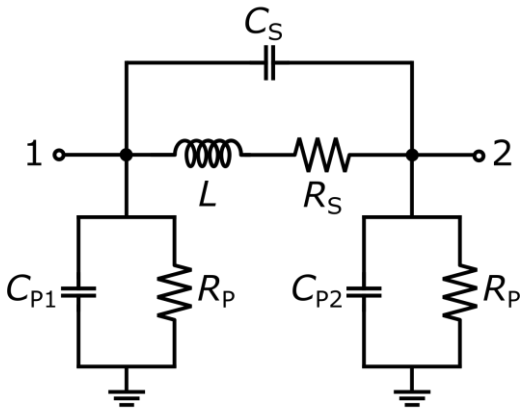

Fig. A.1 Proposed inductor lumped model.

Table A. 1 Layout parameters of the modeled inductors.

Inductor	w **[**μm**]**	n **[**μm**]**	d_{in} **[**μm**]**
IND 1	10	3.5	60
IND 2	10	6.5	60
IND 3	20	1.5	220
IND 4	20	3.5	150
IND 5	40	1.5	120
IND 6	40	2.5	200
IND 7	60	1.5	290
IND 8	60	2.5	240
IND 9	100	1.5	100
IND 10	100	1.5	300

All the electrical parameters have been extracted from EM simulations carried out on a set of ten circular spiral inductors with different metal trace width, w, inner diameter, d_{in}, and number of turns, n. The metal spacing, s, has been set to the minimum value allowed by the technology. The BEOL

provides two thick metal layers, the top one has been used to made up the coil while the lower one has been exploited for the underpass. The geometrical layout parameters of all the modeled inductors are summarized in Table A.1. Moreover, Fig. A.2 displays the layout of inductor IND 6 as an example.

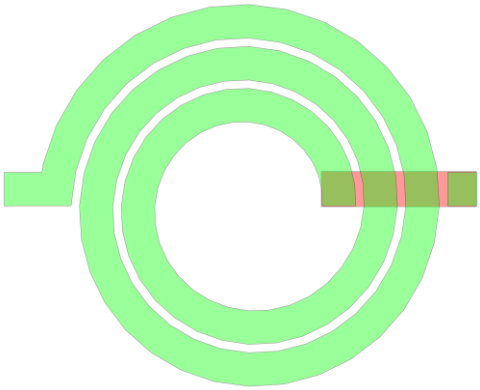

Fig. A. 2 Layout of inductor IND 6.

The starting point of the proposed model has been the low-frequency inductance extraction by means of:

$$L = \frac{Im\left\{\frac{1}{Y_{11}}\right\}}{2\pi f} \tag{A.1}$$

The resulting value has been considered as the sum of three contributions:

$$L = L_{coil} + L_{und} + L_{sub} \tag{A.2}$$

being L_{coil} and L_{under} the inductances of the coil and the underpass, respectively, while L_{sub} accounts for the magnetic field induced in the substrate. The first two terms of equation (A.2) can be calculated by using

well-known closed form expressions available in literature [60], [61], whereas the last one has been evaluated by using the following monomial formula:

$$L_{sub} = -4\pi\alpha n^2 d_{avg}^2 w \tag{A.3}$$

where d_{avg} is the average inductor diameter and α is a fitting coefficient of around 0.92. It should be noted that L_{sub} is a negative value since a reduction of the total inductance is expected due to the induced magnetic field within the substrate.

For each inductor the capacitance C_S has been drawn from EM simulation data as:

$$C_S = \frac{1}{L(2\pi SRF_{21})^2} \tag{A.4}$$

being SRF_{21} the self-resonance frequency related to the transverse admittance of the π-model (i.e., the frequency for which the imaginary part of $1/Y_{21}$ is zero).

The following scalable equation has been obtained from the extracted values:

$$C_S = \frac{1}{N_{over}} \frac{\varepsilon_M w^2}{t_M} p(n) \tag{A.5}$$

where N_{over} is the number of overlaps between the spiral and the underpass, ($N_{over} = n + 1.5$), ε_M and t_M represent the electric permittivity and thickness of the intermetal dielectric layer, respectively, while *p(n)* is a fitting second order polynomial expression:

$$p(n) = 0.9(n^2 - 3n + 4\alpha) \tag{A.6}$$

The minimum of *p(n)* is obtained for $n = 1.5$, which is the lowest value of the number of turns as a part of the inductor set. It is worth noting that the second factor appearing at the right-hand side of (A.5) ideally represents the capacitive contribution due to a single overlap between spiral and underpass. Capacitances C_{P1} and C_{P2} have been drawn similarly to C_S, as:

$$C_{P1} = \frac{1}{L(2\pi SRF_{11})^2} - C_s \tag{A.7}$$

$$C_{P2} = \frac{1}{L(2\pi SRF_{22})^2} - C_s \tag{A.8}$$

where SRF_{11} and SRF_{22} are the frequency values that nullify the imaginary part of $1/Y_{11}$ and $1/Y_{22}$, respectively.

The extracted values of C_{P1} have been fitted by the following equation:

$$C_{P1} = \frac{C_{sp}A_{coil}}{2}\left[1 + (1+\alpha)e^{-\beta w}\right] \tag{A.9}$$

where A_{coil} stands for the effective area given by the product of coil width and length, l_{coil}:

$$l_{coil} = \pi n[d_{in} + w + (n - 0.5)(w + s)] \tag{A.10}$$

C_{sp} represents the substrate capacitance per unit area, whereas β is an experimental coefficient estimated to be $3.53 \cdot 10^4$. Capacitance C_{P2} can be also evaluated through (A.9) by adopting a modified expression for the spiral length accounting for the inductor asymmetrical structure:

$$l_{coil,mod} \approx \pi n \left[d_{in} + w + \left(\frac{7}{12} n - 0.5 \right) (w + s) \right] \qquad \text{(A.11)}$$

It is observed that the capacitance given by equation (A.9) is reduced to the ideal value as the metal width increases. This behavior is consistent with the fringing effects of the electric field. Indeed, these phenomena turn to be relevant in inductors exploiting small width, thus small effective area A_{coil}, giving place to a considerable growth of the parasitic capacitance throughout the substrate.

The series resistance, R_S, has been derived from EM simulations by means of:

$$R_S = -Re\left\{ \frac{1}{Y_{21} + j\omega C_S} \right\} \qquad \text{(A.12)}$$

The resulting resistance showed a roughly parabolic behavior as a function of the frequency for all the considered inductors:

$$R_s = R_{DC} \left[1 + \left(\frac{f}{f_{R0}} - \frac{f^2}{2 f_{R0} f_{RM}} \right) \left(\frac{f_{R0}}{2 f_{RM}} - 1 \right)^{-1} \right] \qquad \text{(A.13)}$$

where R_{DC} is the DC resistance of the whole metal trace (i.e., spiral and underpass) whereas f_{RM} and f_{R0} are the frequencies for which R_S assumes its maximum and zero, respectively. These two frequency values are quite

difficult to predict starting from the inductor layout parameters. However, the following empirical formulas can be used to get a good approximation:

$$f_{R0} \approx \left(1 - 2200\sqrt{wd_{in}}\right) SRF_{11} \tag{A.14}$$

$$f_{RM} \approx \frac{0.04 SRF_{11}}{w^{0.1} n^{0.23} d_{in}^{0.12}} \tag{A.15}$$

Regarding substrate losses, R_P has been extracted as:

$$R_P = Re\left\{\frac{1}{Y_{11} + Y_{21}}\right\} \tag{A.16}$$

As a first approximation, the parallel resistance turns to be inversely proportional to the frequency and can be evaluated as:

$$R_P = \frac{\rho_{Si} t_{Si}}{A_{out}} \frac{f_0}{6f} \tag{A.17}$$

being ρ_{Si} and t_{Si} the resistivity and the thickness of the silicon substrate, A_{out} the area of the circle defined by the inductor outer diameter and f_0 the operative frequency of 3.5 GHz.

Fig. A.3 reports a comparison between model and EM simulation results of three devices in terms of inductance and quality factor curves. A quite good fitting it is observed in the considered frequency range. The average inductance, peak quality factor and self-resonance frequency errors on the whole inductor set are about 5%, 10% and 8%, respectively.

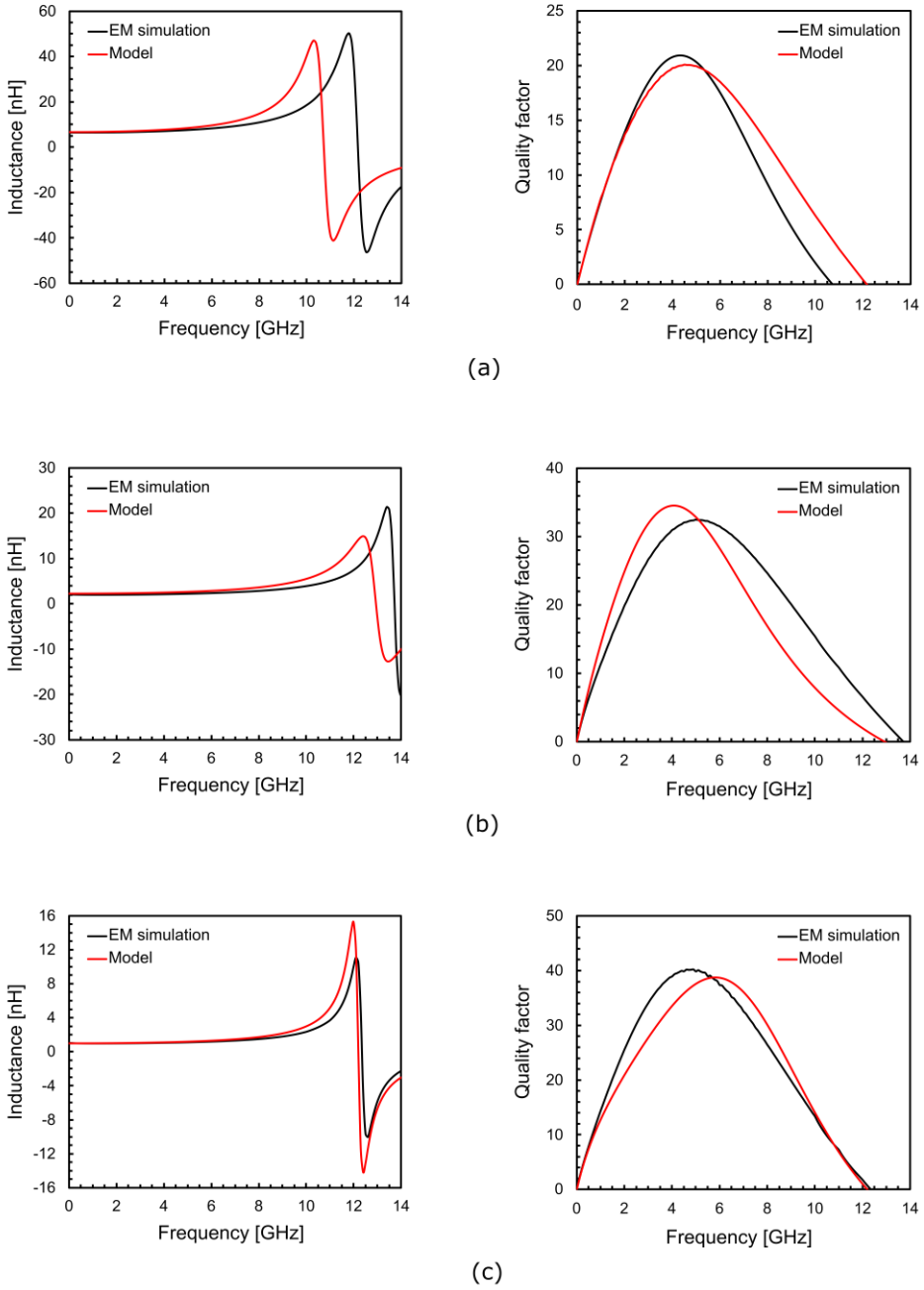

Fig. A. 3 Comparison between model and EM simulation: (a) IND 1, (b) IND 6, (c) IND 10.

It is interesting to highlight some remarkable differences between this work and a recently published study [76] on the same topic (i.e., modelling of GaN on Si inductors). Indeed, although a larger number of inductors with various shapes have been analyzed in [76], the model proposed in this thesis dissertation considers a much wider range of the metal trace width. This circumstance is reflected in the explicit dependency of the model equations, specifically in (A.3) and (A.9), from the layout parameter *w*. A considerable general difference between the two works concerns the modelling methodology itself. Indeed, in [76] a pure analytical approach has been followed, using a lot of circuit elements to account for the several physical phenomena occurring in metal and substrate layers. On the other hand, the scalable model presented in this appendix adopts a much easier equivalent circuit, consisting of only seven lumped components, and starting for some theoretical considerations exploits experimental coefficients to fit the EM simulation data. Finally, it is worth noting that the proposed model turns out to be broadly comparable to [76] in terms of percentage errors on main performance parameters.

APPENDIX B

Publications

A. Patents

1. S. Spataro, S. Coffa and E. Ragonese, “Capacitive-coupled stacked class-D oscillators for galvanic isolation,” U.S. Patent Appl. 17732026, filed 28 Apr 2022, granted 04 Apr 2023.

B. Conferences

1. S. Spataro and E. Ragonese, “Design and optimization of silicon-integrated inductive components for automotive radar applications in K-

and W-bands," *2020 AEIT International Conference of Electrical and Electronic Technologies for Automotive (AEIT AUTOMOTIVE)*, Torino, Italy, 2020, pp. 1-6.

C. Peer-reviewed journals

1. S. Spataro, N. Salerno, G. Papotto, E. Ragonese, "The effect of a metal PGS on the Q-factor of spiral inductors for RF and mm-wave applications in a 28-nm CMOS technology," *International Journal of RF Microwave Computer-Aided Engineering*, 2020, 30, 1-12.
2. E. Ragonese, C. Nocera, A. Cavarra, G. Papotto, S. Spataro, G. Palmisano, "A comparative analysis between standard and mm-Wave optimized BEOL in a nanoscale CMOS technology," *Electronics*, 2020, 9, 2124.
3. S. Spataro, N. Spina, E. Ragonese, "Package-scale galvanic isolators based on radio frequency coupling: micro–antenna design," MDPI Electronics, vol. 11, article no. 291, Jan. 2022.
4. S. Spataro and E. Ragonese, "Capacitive-coupled stacked class-D oscillators for galvanic isolators," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 70, no. 4, pp. 1356-1360, April 2023.
5. S. Spataro, E. Ragonese, N. Spina, G. Palmisano, "A GaN-integrated galvanically isolated data link based on RF planar coupling with voltage combining for gate-driver applications," *IEEE Access* (manuscript submitted on 14 October 2023).

Conclusion

In the near future, galvanically isolated interfaces for industrial, automotive and medical applications will require very high isolation ratings (i.e., over 20 kV). Moreover, the higher switching frequencies enabled by wideband power devices, such as GaN and SiC transistors, call for CMTI values beyond 200 kV/μs. Those challenges cannot be easily addressed by means of traditional isolators, thus it is necessary to think about new approaches in the matter of galvanic isolation. An overview of galvanic isolation systems was given in Chapter 1 presenting basics concepts along with main requirements, safety standards and applications. Then, state-of-the-art isolation techniques has been discussed underlying the intrinsic limitations of traditional chip-scale devices exploiting capacitive and magnetic couplings.

Package-scale isolation has been addressed in Chapter 2. This approach takes advantage of packaging/assembling techniques and RF planar coupling

between micro-antennas to enable isolated data transfer. Key concepts and crucial advantages of this technique over traditional isolation capacitors and transformers have been discussed. A brief description of a typical data link adopting package-scale isolation, including main circuit blocks of the TX and RX front-ends, has been presented. Due to high channel losses (i.e., about 30-45 dB), the voltage amplitude across the receiving antenna may not be sufficiently high to ensure proper operation of the data channel. This circumstance results in two open research issues which constitute core topics of this thesis work. Indeed, an optimized micro-antenna design, aimed at EM coupling maximization, must be adopted. On the other hand, it is crucial to implement topology optimization of the TX front-end to maximize the transmitted voltage while keeping down power consumption.

The first topic has been covered in Section 2.3. Specifically, the dependency of electric performance (i.e., antenna inductances, quality factors, magnetic coupling coefficient and TX-to-RX coupling loss) from process and layout parameters has been investigated leading to general design guidelines. Then a step-by-step design flow has been presented and validated by means of 3D EM simulations carried out in a 0.32-μm BCD technology. A reduction of channel loss of about 1.7 dB has been demonstrated passing by a rough antenna layout to an optimized one. Section 2.4 has regarded instead the TX front-end block design. Specifically, a novel RF oscillator topology based on class-D one, suitable for package-scale isolation, has been proposed. Thanks to current-reuse and voltage-combining techniques along with almost pure capacitive coupling, the presented solution ideally produces the same oscillation voltage of a standard class-D one with half current consumption. The advantages of the novel topology have been highlighted in

comparison with a traditional complementary cross-coupled oscillator within an isolated data channel integrated in a 0.18-μm CMOS technology. Simulation results have shown that, unlike the traditional solution, the proposed oscillator is able to provide sufficiently high signal for correct demodulation at low supply voltage and with a high DTI value.

Finally, the design and characterization of a complete package-scale isolated data channel in GaN technology for gate-drive applications has been presented in Chapter 3. This activity, which represents the most significant outcome of this thesis dissertation, has been performed in collaboration with STMicroelectronics within the EU Project GaN4AP. I mainly worked on the design and layout of the TX front-end (which basically exploits the same oscillator topology discussed in Chapter 2), as well as the TX/RX micro-antennas. A chip-on-board assembly has been realized to test the package-scale isolation link leading to a successful characterization. Indeed, measurement data have proved the effectiveness of the proposed approach to achieve low power consumption, while maintaining state-of-the-art performance.

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