IEEE Access
Multidisciplinary | Rapid Review | Open Access Journal

Date of publication xxxx 00, 0000, date of current version xxxx 00, 0000.

Digital Object Identifier 10.1109/ACCESS.2017.Doi Number

Hybrid Cascode Compensation with Hybrid *Q*-Factor Control for Three-Stage Unconditionally Stable Amplifiers

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ABSTRACT This paper presents Hybrid Cascode Compensation with Hybrid *Q*–Factor Control (HCCHQ), for three-stage feedback operational transconductance amplifiers (OTA) capable of handling any load capacitor (C_L). The design incorporates an enhanced Miller compensation strategy, exploiting cascode-Miller compensation with hybrid pathways to effectively separate the dominant pole from non-dominant poles for bandwidth expansion. It also combines a hybrid quality factor (*Q*–factor) control with a local impedance attenuation (LIA) module, adjusting the *Q*–factor of non-dominant poles by mitigating the ringing in the time response and the frequency peaking for lighter C_Ls. The new design can accommodate capacitive loads ranging from zero to infinity, owing to the Miller– and load–compensated solutions for the light and heavy C_Ls, respectively. Fabricated in a 180-nm standard CMOS process, a prototype of the proposed amplifier demonstrates a quiescent current of 25 µA under a 1.8 V single supply. It boasts a compact 0.0055 mm^2 area and exhibits unconditional stability when configured as a voltage buffer driving any C_L. With a mean DC gain of 115 dB, the average unit-gain frequency (UGF) is 2.30 MHz and 0.11 MHz for 0.1 and 47 nF external capacitive loads, respectively. The mean 1% settling time is measured as 2.41 µs and 40 µs for the same capacitive loads, respectively, when a 0.4 V pulse signal is applied to the input.

INDEX TERMS Feedback; frequency compensation; frequency response; load capacitor; Miller compensation; operational amplifier; settling time and stability.

I. INTRODUCTION

A key application of feedback operational transconductance amplifiers (OTAs) is to drive/buffer input signals over a wide range of capacitive loads. This feature is crucial for the design of various integrated blocks, spanning analog-to-digital (A/D) and digital-to-analog (D/A) converters, audio drivers, linear regulators, liquid-crystal-diode (LCD), line drivers, active filters, and capacitive sensors [1-8]. However, due to fundamental constraints on operating voltage and the diminishing intrinsic gain to ten and below in advanced low-power (LP) CMOS technologies, basic single-stage amplifiers can no longer sustain the minimum 100-dB gain factor level essential for the routine applications across the different process corners. Prior to combination with a secondary design solution, single-stage amplifier topologies are consequently deemed unsuitable for driving a broad range of capacitive loads [9-12]. Cascading multiple gain stages is thus necessary to ensure sufficient DC gain under low-voltage operation [13-34]. Addressing stability issues, however, poses some practical challenges, especially when a feedback amplifier, comprising at least three stages, needs to handle a very wide range of C_L. A three-stage amplifier with more than three poles in the transfer function is prone to instability without frequency compensation. The classical solution to regain the stability is nested-Miller compensation (NMC) [35-38], which involves splitting the dominant and non-dominant poles using typically a large C_L-dependent Miller capacitor. NMC amplifiers not only suffer from high quiescent current in the output stage for enlarging the magnitude of load-dependent poles and a right-half plane (RHP), but also require an additional compensation capacitor (C_C) to adjust the non-dominant

poles quality factor. Higher performance metrics are expected using reversed NMC (RNMC) for the OTAs driving large C_Ls, as the loading of the output terminal is not influenced by the additional C_C [39]. Nonetheless, an undesired RHP zero tends to limit the bandwidth. In contrast, solutions relying on a single Miller capacitor among the first and the third stages tend to enhance both large- and small-signal performances for comparable area and power [40]. However, stability complications arise from the second stage since the only C_C is meant to separate the output pole of the first stage from that of the third stage. Despite bandwidth can be extended by incorporating feedforward stages and nulling resistors [40, 41], special considerations are therefore needed to reduce the *Q*–factor of the induced pole pair via the gain factor of the second stage [40]. A RHP zero in the single-Miller compensation (SMC) transfer function worsens the phase margin (*PM*) at heavy C_Ls also, and the zero can be moved to higher frequencies via a current buffer/amplifier cascaded with C_C in the form of a so-called cascode-Miller compensation [42-44]. As for cross-feedforward cascode compensation (CFCC) [43] in this category, e.g., the gain-bandwidth product frequency (*GBW*) can be positioned well beyond that of SMC. What's more, the gain factor can be boosted by adding a gain enhancement (GE) circuitry into the first stage topology [42]. Despite these advantages, the lower C_L value still remain in nF-range, as proper *Q*-factor values cannot be guaranteed for sufficient gain margin (*GM*) at small C_Ls. A series Resistor−Capacitor (*RC*) branch can be added, serving as a LIA network to reduce the value of capacitive load, as demonstrated in some configurations [45, 46].

Hybrid cascode-Miller compensation is an advanced solution aimed at enhancing the operation of three- and four-stage OTAs from the perspectives of power, area and bandwidth [47-50]. It involves adding another Miller loop in addition to the main Miller loop, by dividing into equal sections the original Miller capacitor. Not only this increases the non-dominant poles frequency, but also reduces the *Q*–factor without relying on excessive power or area. This strategy can be combined with a LIA network [47] or with internally-compensated mid-stages [49] to address the stability issues of the multi-stage OTAs driving a very wide C_L range. The operation is, however, constrained, either at very large or at very small loads, due to the inappropriate positioning of the poles that yields unacceptable *GM* / *PM*. While adequate frequency compensation methods are suggested for three-stage amplifiers aiming to widen the range of load capacitor to infinity, the issue of lower C_L either persists in several pF-range or the operation is impaired at very small C_Ls. The output-compensated OTA with no C_C reported in [51] can handle as low as 90 pF capacitive loads. The inclusion of feedback stages, rather than a Miller capacitor, however, increases the design complexity other than reducing the power efficiency. Furthermore, the amplifier needs reconfiguration for maintaining necessary *PM* at high load capacitors. An amplifier capable of driving any C_L is introduced by the authors in [52]. The performance is, however, compromised at very light C_Ls, resulting in some ringing particularly in the absence of output capacitor.

To overcome the limitations of the previously-described solutions, this paper presents HCCHQ for three-stage OTAs driving any C_L. Using this method, the C_L drivability range can be expanded from zero to infinity via the combination of a LIA network and a *Q*–factor control module realized by capacitors and passive resistors. Such arrangement effectively modifies the *Q*–factor, mitigating frequency peaking and minimizing time response ringing within critical zero to some pF C_L range. The final design is Miller-compensated for light capacitive loads, seamlessly transitioning to C_L compensation at cross-over zone [52] and completes for ultra-large load capacitors. The remainder of this paper is organized as follows. Section II aims to provide an analysis of the principles of operation of HCCHQ amplifier, accompanied by a discussion of the main design targets. Section III focuses the simulated and experimental data obtained from a prototype manufactured in a 180-nm CMOS technology. Section IV gives the concluding remarks.

II. HYBRID CASCODE COMPENSATION WITH *Q*–FACTOR CONTROL AND LIA NETWORK

A. BLOCK DIAGRAM AND CIRCUIT SCHEMATIC

The schematic of the HCCHQ amplifier is depicted in Fig. 1(a), with v_O representing the output voltage and v_i as the input voltage ($v_i = v_i^+ - v_i^-$). The input stage consists of transistors M_0, M_{1a}–M_{1b} to M_{5a}–M_{5b}, implementing a folded-cascode configuration suited for low-voltage operation with M_{1a}–M_{1b} as input devices. The first-stage equivalent transconductance, g_{m1}, is determined by the latter, while g_{mC} is assumed to be the identical transconductance of the cascode devices M_{3a}–M_{3b} and M_{4a}–M_{4b}. Although achieving perfect matching is challenging, especially between an *n*MOS and a *p*MOS, it is important to note that small mismatches in the transconductance of these devices can subtly alter the positions of the poles and zeros and creates insignificant doublets without affecting the general analysis described here [47]. The current mirror M_{5a}–M_{5b} facilitates the signal conversion from differential to single-ended. The non-inverting second-stage gain is formed by M_6, M_{7a}–M_{7b} and M_8, establishing the second-stage transconductance g_{m2} as the product of the transconductance of M_6 and the gain of the current mirror M_{7a}–M_{7b}.

The output stage is implemented using M_9 and M_{10}, where g_{m3} and g_{mf} represent their transconductances, respectively. The push-pull strategy inherent in this stage enhances both large- and small-signal load driving capabilities. Fig. 1(b) displays the amplifier diagram, where the output impedance

of various stages is represented by equivalent resistors R_{1-3} and capacitors C_{1-3}. The output terminal drives C_L, typically having a much higher value than the parasitic C_{1-3}.

The frequency compensation includes the series components R_D and C_D, alongside C_{C1} and C_{C2}, divided into identical fractions. The dual Miller capacitors, denoted as $C_{C1}/2$, link the source of common-gate devices M_{3a} and M_{4a} to the output, adding two g_{mC} stages with input resistance $1/g_{mC}$ to the compensation loop, preceding v_{O1} in Fig. 1(b). In contrast to the alternative SMC solution, which involves coupling v_{O1} and v_O through a monolithic C_{C1} [40], or potentially the CFCC approach which links v_O to the source of M_{3a} via C_{C1}, the proposed arrangement allows for about 40% increase in the magnitude of non-dominant poles [47, 48]. The proposed compensation strategy additionally includes dual $C_{C2}/2$ to fine-tune non-dominant poles quality factor, especially at very small C_Ls. Linking the source terminal of M_{3b} and M_{4b} to the second stage v_{O2} in Fig. 1(a), these capacitors form additional feedback loops to sense the gain factor and, accordingly, adjust the Q–factor, as will be analyzed later. M_{3b} and M_{4b} share identical gate ratios and biasing currents with M_{3a} and M_{4a}, allowing their transconductance to be modeled by g_{mC} as used for the case of Miller capacitors. The LIA branch made of R_D and C_D influences the high-frequency impedance at node v_{O1}, providing adaptive control over the location of the non-dominant poles generated by compensation loop.

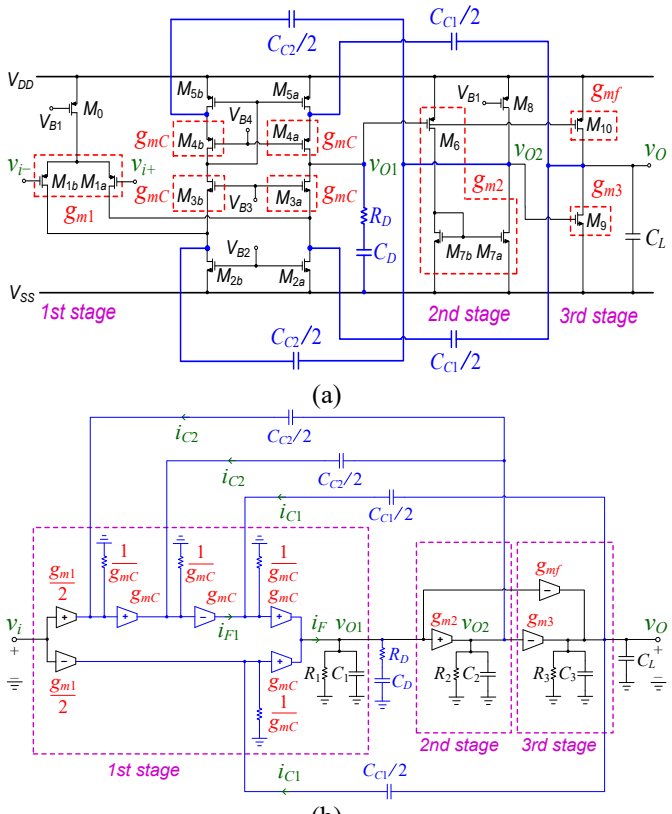


FIGURE 1. Three-stage HCCHQ amplifier: (a) Schematic; (b) Small-signal equivalent circuit.

B. SMALL-SIGNAL ANALYSIS

Analysis of the original HCCHQ amplifier appears to be difficult, primarily due to the complications added by the nested feedback loops involving $C_{C1}/2$ and $C_{C2}/2$. These difficulties hinder the direct derivation of a simplified transfer function. For this reason, it is imperative to combine the hybrid feedback loops, simplifying the original configuration illustrated in Fig. 1(b). The feedforward currents directed towards v_{O2} through the dual $C_{C2}/2$ can be disregarded for $C_{C2}s << g_{mC}$, enabling to write i_{F1} as:

$$i_{F1} = \left[\frac{1}{g_{mC}} \cdot g_{mC} \cdot \left(\frac{g_{m1}}{2} v_i + i_{C2}\right) + i_{C2}\right] \cdot \frac{1}{g_{mC}} \cdot \left(-g_{mC}\right) = -\left(2i_{C2} + \frac{g_{m1}}{2} v_i\right) \quad (1)$$

where

$$i_{C2} = \frac{v_{o2}}{\frac{1}{g_{mC}} + \frac{2}{C_{C2}s}} \quad (2)$$

is the current feedback originating from v_{O2} to the first stage through the either $C_{C2}/2$. Fig. 2(a) illustrates an equivalent model of Fig. 1(b) by ignoring the negligible feedforward currents, which results in a same i_{F1} expression:

$$i_{F1} = 2i_{C2} \cdot \frac{1}{g_{mC}} \cdot \left(-g_{mC}\right) \cdot \frac{-g_{m1}}{2} v_i = -\left(2i_{C2} + \frac{g_{m1}}{2} v_i\right) \quad (3)$$

In this modified version, the feedback pathways involving the dual $C_{C2}/2$ are distinctly separated from the input signal pathway, still all contributing to the same i_{F1}. The current i_F at the first stage output is given as:

$$i_F = \left(i_{F1} + 2i_{C1} - \frac{g_{m1}}{2} v_i\right) \cdot \frac{1}{g_{mC}} \cdot g_{mC} \quad (4)$$

where

$$i_{C1} = \frac{v_{o2}}{\frac{1}{g_{mC}} + \frac{2}{C_{C1}s}} \quad (5)$$

represents the current component fed back from the output by Miller capacitors. Substituting i_{F1} and i_{C1} from (3) and (5) in (4) yields:

$$i_F = -\left(2\frac{v_{o2}}{\frac{1}{g_{mC}} + \frac{2}{C_{C2}s}} + \frac{g_{m1}}{2} v_i\right) + 2\frac{v_o}{\frac{1}{g_{mC}} + \frac{2}{C_{C1}s}} - \frac{g_{m1}}{2} v_i = -g_{m1} v_i + \frac{v_o}{\frac{1}{2g_{mC}} + \frac{1}{C_{C1}s}} - \frac{v_{o2}}{\frac{1}{2g_{mC}} + \frac{1}{C_{C2}s}} \quad (6)$$

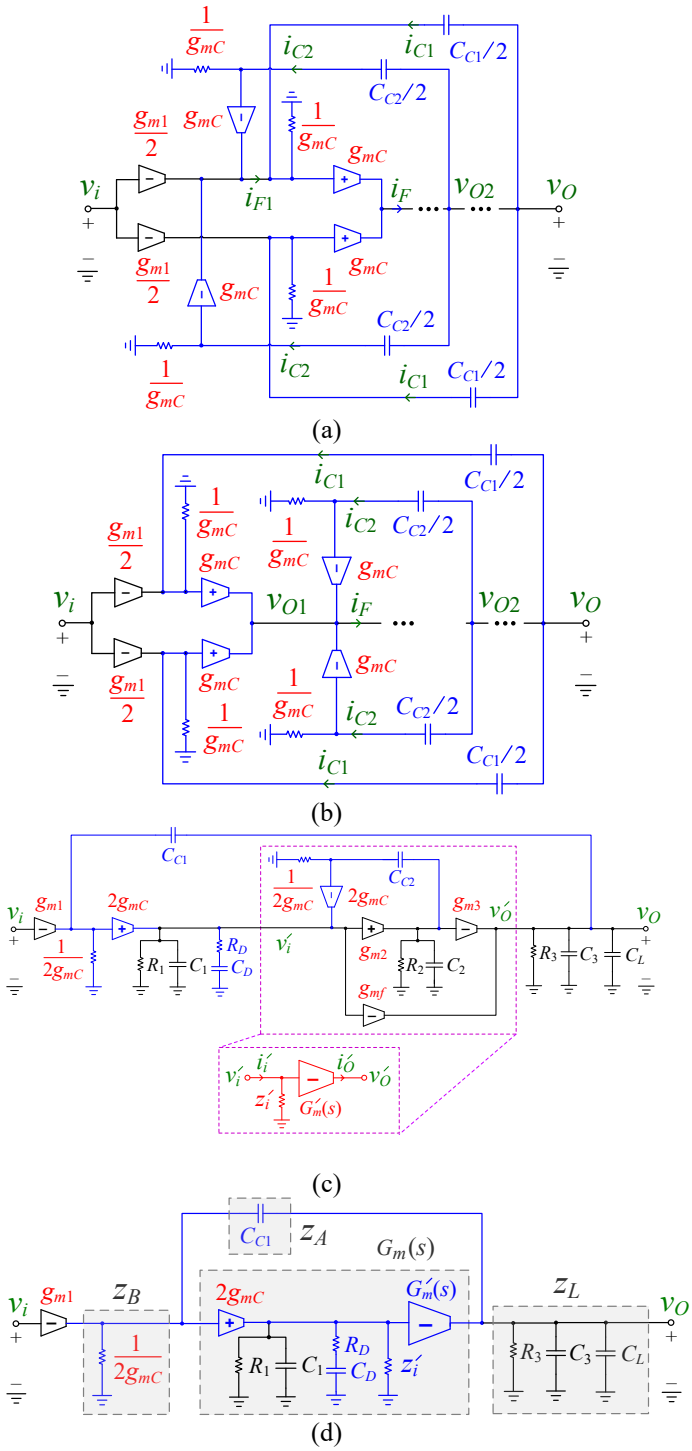


FIGURE 2. Simplifying the HCCHQ amplifier diagram; (a) Isolating the input path from the dual $C_{C2}/2$ feedback paths; (b) The $C_{C2}/2$ paths when referred to the first stage output; (c) Simplified HCCHQ diagram; (d) Fitting the amplifier diagram to a standard model type I.

Fig. 2(b) depicts an equivalent model derived from Fig. 2(a), taking into account the specific terms outlined in (6) while excluding the negligible feedforward currents. The revised model allows for merging the parallel feedback pathways due to symmetry, ultimately to construct the practical diagram in Fig. 2(c). Notably, it contains the overall parameters C_{C1}, C_{C2} and $2g_{mC}$ in a simplified manner, contrasting with several feedback loops made from multiple $C_{C1}/2$, $C_{C2}/2$ and g_{mC} components in parallel. Analysis of the modified circuit in Fig. 2(c) is more straightforward, involving two loops rather than four in Fig. 1(b). The feedback path through C_{C2} inside the rectangular dash line can be viewed as a pure $G'_m(s)$ with an input impedance of z'_i and (v'_i, i'_i) and (v'_o, i'_o) as input and output voltages and currents, respectively. Under $C_{C2} >> C_2$, and after some algebra, $G'_m(s)$ and z'_i are given by:

$$G'_m(s)=\frac{i'_O}{v'_i}=\frac{g_{m2}g_{m3}}{C_{C2}s}\left(1+\frac{C_{C2}s}{2g_{mC}}\right)\left(1+R_2C_2s\right)+g_{mf}\approx \frac{g_{m2}g_{m3}}{C_{C2}s}\left(1+\frac{C_{C2}s}{2g_{mC}}\right) \tag{7}$$

$$z'_i(s)=\frac{v'_i}{i'_i}=\frac{1}{g_{m2}}\left(1+\frac{C_2}{C_{C2}}\right)\frac{1+R_2\dfrac{C_{C2}C_2}{C_{C2}+C_2}s}{1+R_2C_2s}\approx\frac{1}{g_{m2}} \tag{8}$$

The feedforward stage g_{mf} has little influence on the small-signal operation and thus is neglected in $G'_m(s)$, but is intended for improving large-signal operation. The equivalent circuit in Fig. 2(d) aligns with the model type I addressed in [33], comprising the following $G_m(s)$, $z_B(s)$, $z_A(s)$ and $z_L(s)$:

$$G_m(s)=2g_{mC}\cdot\left[R_1\,//\,\frac{1}{C_1s}\,//\left(R_D+\frac{1}{C_Ds}\right)//z'_i\right]\cdot G'_m(s)\approx 2\frac{g_{mC}g_{m3}}{C_{C2}s}\left(1+\frac{C_{C2}s}{2g_{mC}}\right) \tag{9}$$

$$z_A(s)=\frac{1}{C_{C1}s} \tag{10}$$

$$z_B(s)=\frac{1}{2g_{mC}} \tag{11}$$

$$z_L=\frac{1}{C_Ls}\,//\,R_3\,//\,\frac{1}{C_3s}\approx\frac{1}{C_Ls} \tag{12}$$

The purpose of the series R_D-C_D is to suppress the inherent R_1–C_1 of the first stage output, correspondingly moving their parasitic pole to higher frequencies [46]. These components along with z'_i all contribute to the loading of $2g_{mC}$ in Fig. 2(d), while $z'_i \approx 1/g_{m2}$ prevails others for $R_1 >> R_D$, C_{C2}, $C_D >> C_1$, C_2 and $g_{m2}R_D >> 1$. The latter thus shapes the G_m expression according to the approximation made in (9), as $2g_{mC}$ is primarily loaded by the lighter $z'_i \approx 1/g_{m2}$ rather than R_1, C_1, R_D and C_D at medium to high frequencies. Using the results elaborated in [33] for model type I, and upon $R_{1\text{–}3} >> R_D >> 1$, $g_{m1\text{–}3}R_{1\text{–}3}$,

$g_{m1-3}\,R_D$, $g_{mC}\,R_{1-3} >> 1$, and $C_L >> C_D$, $C_{C1-2} >> C_{1-3}$, the voltage-gain transfer function can be symbolically derived as:

$$A_v(s)=\frac{v_O}{v_i}\approx\frac{A_0}{1+\dfrac{s}{p_{-3dB}}}\cdot\frac{1+\dfrac{C_{C2}}{2g_{mC}}s-\dfrac{C_{C1}C_{C2}}{2g_{mC}g_{m3}}s^2}{1+\left[\dfrac{1}{2g_{mC}}+\dfrac{1}{g_{m3}}\left(1+\dfrac{C_L}{C_{C1}}\right)\right]C_{C2}s+\dfrac{C_{C2}C_L}{2g_{mC}g_{m3}}s^2}\approx \tag{13}$$

$$\frac{A_0\left(1+\dfrac{s}{z_1}\right)\left(1+\dfrac{s}{z_2}\right)}{\left(1+\dfrac{s}{p_{-3dB}}\right)\left(1+\dfrac{s}{Q\omega_0}+\dfrac{s^2}{\omega_0^2}\right)}$$

where

$$p_{-3dB}=\frac{1}{R_3C_L+g_{m2}g_{m3}R_1R_2R_3C_{C1}} \tag{14}$$

is the dominant pole whereas $A_0\approx g_{m1}g_{m2}g_{m3}R_1R_2R_3$ is the DC gain. The *GBW* frequency is measured by:

$$GBW=A_0\cdot p_{-3dB}=\frac{g_{m1}}{\dfrac{C_L}{g_{m2}g_{m3}R_1R_2}+C_{C1}} \tag{15}$$

The latter simplifies to the standard g_{m1}/C_{C1} for small to medium C_L ($C_L << g_{m2}g_{m3}R_1R_2C_{C1}$), smoothly transitioning to $g_{m1}g_{m2}g_{m3}R_1R_2/C_L$ at high C_L values. The *GBW* is proportionally reduced as load capacitor becomes significant ($C_L >> g_{m2}g_{m3}R_1R_2C_{C1}$), indicating that the proposed amplifier relies on compensation by C_L rather than C_{C1} for heavy capacitive loads. The impact of the first and second non-dominant poles is substantial on amplifier's stability, determined by their frequency ω_0 and Q−factor:

$$\omega_0=\sqrt{\frac{2g_{mC}g_{m3}}{C_{C2}C_L}} \tag{16}$$

$$Q=\frac{1}{g_{m3}+2g_{mC}\left(1+\dfrac{C_L}{C_{C1}}\right)}\sqrt{\frac{2g_{mC}g_{m3}C_L}{C_{C2}}} \tag{17}$$

There are also two zeros approximated by:

$$z_{1,2}\approx-\frac{g_{m3}}{2C_{C1}}\left(1\pm\sqrt{1+8\frac{g_{mC}C_{C1}}{g_{m3}C_{C2}}}\right) \tag{18}$$

One zero is positioned in the left-half plane (LHP) and can be used to partially eliminate the phase lag induced by non-dominant poles, while the other lies in the right-half plane (RHP) and should be strategically positioned well beyond the *GBW* product. The pole-zero map and its variation against C_L is illustrated in Fig. 3. The poles p_2 and p_3 convert from complex and conjugate to real form as C_L rises (Eq. (17)), while p_{-3dB} transfers to the origin consistent with (14). In summary, five key insights can be concluded from the derived expressions:

a) The simplified transfer function A_V contains two zeros and three poles, remaining unaffected by the process-dependent parasitic resistors and capacitors and rely on transconductors, C_L and frequency compensation components, providing flexibility to ensure stability across the various process corners and loading conditions.
b) While zeros remain unchanged, increasing C_L yields a decline in the Q−factor of p_2 and p_3, transforming it from conjugate and complex form to real form.
c) The factor "2" in (16) and (17) enhances the amplifier's stability. Arising from dual loops made by hybrid $C_{C1}/2$ and $C_{C2}/2$, this coefficient not only enlarges the magnitude of non-dominant poles but also diminishes their Q−factor in comparison to a single loop.
d) R_D and C_D exert minimal effect on ω_0, Q and the frequency of the main zeros. In fact, the primary role of the LIA network is to ensure that the impact of R_1 and C_1 is minimized despite the mismatches between complementary $C_{C1}/2$ and $C_{C2}/2$ loops, rendering the high-frequency loading of $2g_{mC}$ close to $1/g_{m2}$ rather than the process-dependant parasitic components.
e) The value of C_{C2} should be optimized. Enlarging C_{C2} diminishes the Q−factor of p_2 and p_3 and concurrently reduces their natural frequency.

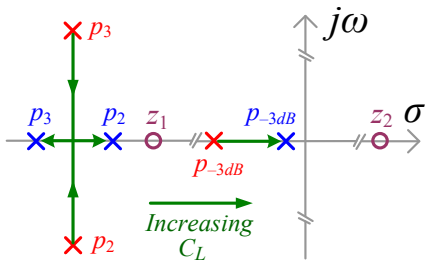


FIGURE 3. **Variations of the poles and zeros as C_L increases.**

C. STABILITY ANALYSIS

Ensuring stability across a broad range of C_L is the specific goal of the described HCCHQ scheme. In this section, we delve into the analysis of stability conditions spanning from the zero- to full-load. The insights gained from extreme cases establish crucial design rules for implementing the proposed OTA. Beginning with the *GM* definition for a feedback factor of unity, the transfer function allows derivation as:

$$GM=-20\log\left(\frac{\sqrt{\left[1+\left(\dfrac{PX}{z_1}\right)^2\right]\left[1+\left(\dfrac{PX}{z_2}\right)^2\right]}}{\dfrac{PX}{GBW}\sqrt{\left(1-\dfrac{PX^2}{\omega_0^2}\right)^2+\left(\dfrac{PX}{Q\omega_0}\right)^2}}\right) \tag{19}$$

The phase crossover frequency (*PX*) is approximately ω_0 when disregarding the influence of zeros [49]. Referring to

the transfer function in (13), the *GM* becomes:

$$GM = 20\log\left[\left(\frac{C_{C1}}{C_L}+\frac{1}{g_{m2}g_{m3}R_1R_2}\right)\cdot\frac{g_{m3}+2g_{mC}\left(1+C_L/C_{C1}\right)}{g_{m1}}\right] - 10\log\left[1+8\frac{g_{mC}}{g_{m3}C_{C2}C_L}\left(\frac{C_{C1}}{1+\sqrt{1+8\frac{g_{mC}C_{C1}}{g_{m3}C_{C2}}}}\right)^2\right] - 10\log\left[1+8\frac{g_{mC}}{g_{m3}C_{C2}C_L}\left(\frac{C_{C1}}{1-\sqrt{1+8\frac{g_{mC}C_{C1}}{g_{m3}C_{C2}}}}\right)^2\right]. \quad (20)$$

The −3 dB pole frequency p_{-3dB} becomes dependent on the capacitive load when $C_L >> g_{m2}g_{m3}R_1R_2C_{C1}$ as per (14). This implies that the compensation of OTA is accomplished by C_L instead of C_{C1} in heavy capacitive loads. The stability remains uncompromised by *GM* at large C_L as inferred from (20), indeed *GM* rises as C_L approaches infinity:

$$\lim_{C_L\to+\infty} GM \approx 20\log\left(\frac{2g_{mC}C_L}{g_{m1}g_{m2}g_{m3}R_1R_2C_{C1}}\right) \quad (21)$$

In the scenario of small to medium capacitive loads ($C_L << g_{m2}g_{m3}R_1R_2C_{C1}$), the −3 dB pole frequency would be inversely proportional to C_{C1} only, yielding a *GM* value that can be made sufficiently large when C_L approaches zero:

$$\lim_{C_L\to 0} GM \approx 20\log\left(\frac{\left(g_{m3}+2g_{mC}\right)C_{C1}}{g_{m1}C_3}\right) - 20\log\left(\frac{\sqrt{1+8\frac{g_{mC}C_{C1}}{g_{m3}C_{C2}}}-1}{\sqrt{1+8\frac{g_{mC}C_{C1}}{g_{m3}C_{C2}}}+1}\right) \quad (22)$$

Enlarging the g_{m3}/g_{m1} and C_{C1}/C_3 ratios is thus suggested to increase the *GM* value in the light loading conditions. Referring to the definition of *PM* for the feedback factor of unity, it can be expressed through the derived transfer function as:

$$PM \approx 90° - \tan^{-1}\left[\frac{GBW}{\left(1-GBW^2/\omega_0^2\right)\omega_0 Q}\right] - \tan^{-1}\left(\frac{GBW}{|z_2|}\right) + \tan^{-1}\left(\frac{GBW}{|z_1|}\right) \quad (23)$$

Upon substituting (15) to (18) into (23) and performing some algebraic steps, the initial relation is further expanded as:

$$PM \approx 90° - \tan^{-1}\left\{\frac{\frac{g_{m1}g_{m2}\left[g_{m3}+2g_{mC}\left(1+\frac{C_L}{C_{C1}}\right)\right]R_1R_2}{2g_{mC}\left[1-g_{m3}C_{C2}C_L\left(\frac{g_{m1}g_{m2}R_1R_2}{g_{m2}g_{m3}R_1R_2C_{C1}+C_L}\right)^2\right]}\cdot\frac{C_{C2}}{g_{m2}g_{m3}R_1R_2C_{C1}+C_L}\right\} + \tan^{-1}\left\{\frac{2g_{m1}g_{m2}R_1R_2}{\sqrt{1+8\frac{g_{mC}C_{C1}}{g_{m3}C_{C2}}}-1}\cdot\frac{C_{C1}}{g_{m2}g_{m3}R_1R_2C_{C1}+C_L}\right\} + \tan^{-1}\left\{\frac{2g_{m1}g_{m2}R_1R_2}{\sqrt{1+8\frac{g_{mC}C_{C1}}{g_{m3}C_{C2}}}+1}\cdot\frac{C_{C1}}{g_{m2}g_{m3}R_1R_2C_{C1}+C_L}\right\} \quad (24)$$

Regrettably, determining the minimum phase margin from the above equation is not feasible, as solving $\partial PM/\partial C_L = 0$ results in a symbolic equation that cannot be represented using classical mathematical functions. Nevertheless, the assessment of *PM* for infinite C_L yields:

$$\lim_{C_L\to+\infty} PM \approx 90° - \tan^{-1}\left(\frac{g_{m1}g_{m2}R_1R_2C_{C2}}{C_{C1}}\right) \quad (25)$$

The dominant pole is relevant to C_L when the load approaches infinity, ensuring stability for large capacitive loads but with a trade-off of reduced bandwidth. Referring to (25), it becomes apparent that optimizing g_{m1}, g_{m2}, C_{C1} and C_{C2} results in a sufficiently elevated *PM* for heavy capacitive loads. Zeros remain largely unaffected by the load, but increasing C_L decreases both non-dominant poles and the *GBW* product and minimizes the stability variations. The poles ultimately transform into real form, with one maintains nearly unchanged and the other declines with the capacitive load at the same *GBW* rate. Enhancing this approach is possible by positioning the load-dependent pole of heavy capacitive loads at frequencies beyond the *GBW*. Opting for $\alpha = 5$ for a pole frequency of $\alpha\times GBW$ ensures that the load-dependent pole will not influence the phase response. For this to happen, we need to set:

$$\frac{g_{m3}C_{C1}}{C_{C2}C_L} > \alpha\frac{g_{m1}g_{m2}g_{m3}R_1R_2}{C_L} \Rightarrow \frac{C_{C1}}{C_{C2}} > \alpha g_{m1}g_{m2}R_1R_2 \quad (26)$$

Equation (26) indicates that favorable stability conditions can be maintained with an enlarged C_{C1}/C_{C2} ratio. The minimum value of C_L will not be constrained by the *PM* when utilizing a precisely tailored compensation network. As mentioned earlier, the dominant pole is solely influenced by C_{C1} when the condition $C_L << g_{m2}g_{m3}R_1R_2C_{C1}$ is met, thus reducing C_L to zero leads to:

$$\lim_{C_L \to 0} PM \approx 90° - \tan^{-1}\left(\frac{g_{m1}\left(g_{m2}+2g_{mC}\right)C_{C2}}{2g_{mC}g_{m3}C_{C1}}\right) + \tan^{-1}\left[\frac{2g_{m1}}{g_{m3}\sqrt{1+8\frac{g_{mC}C_{C1}}{g_{m3}C_{C2}}}-1}\right] + \tan^{-1}\left[\frac{2g_{m1}}{g_{m3}\sqrt{1+8\frac{g_{mC}C_{C1}}{g_{m3}C_{C2}}}+1}\right] \quad (27)$$

Reducing C_L results in an increase in ω_0 as is evident from (16), leading to a larger phase margin in the case its contribution surpasses the *GBW* rising in (15). In practice, stability conditions are predominantly governed by the *GM* rather than *PM* for lower capacitive loads, as lowering C_L typically induces a peak in the frequency spectrum by compromising the stability of the Miller loops. Enlarging the *PM* limit in (27) is possible by fine-tuning the compensation network similar to the situation explained for very large C_Ls. The designer should position the sole non-dominant pole of $C_L = 0$ in (13) at $\alpha \times GBW$ after the *GBW* product, in order to minimize the phase lag attributed to the corresponding pole. Mathematically:

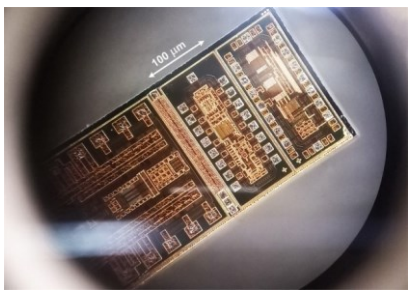
$$\frac{1}{\left(\frac{1}{2g_{mC}}+\frac{1}{g_{m3}}\right)C_{C2}} > \alpha\frac{g_{m1}}{C_{C1}} \Rightarrow \frac{C_{C1}}{C_{C2}} > \alpha g_{m1}\left(\frac{1}{2g_{mC}}+\frac{1}{g_{m3}}\right) \quad (28)$$

The outcome obtained from (28) align with those deduced from (26), indicating that increasing the C_{C1}/C_{C2} ratio lead to improved stability conditions spanning from no-load to full-load conditions. However, increasing C_{C1}/C_{C2} ratio may contradict our preliminary $C_{C2} \gg C_2$ assumption before deriving a simplified transfer function. Consequently, while (26) and (28) provide valuable insight, simulations are required to fine-tune the frequency compensation elements across the entire load range and in the presence of non-ideal effects under various process, voltage and temperature (PVT) scenarios.

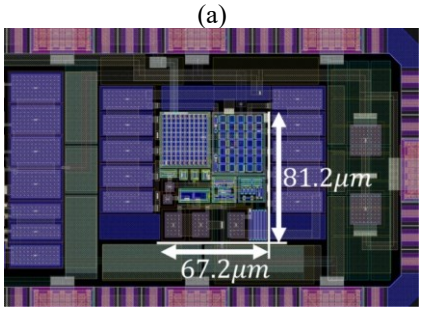
III. CASE STUDY

The HCCHQ amplifier was integrated in a standard 180-nm CMOS technology and tested using a single 1.8-V voltage supply. Fig. 4(a) presents the chip micrograph, including the physical layout of a sample with the details illustrated in Fig. 4(b), which occupies an area of approximately 0.0055 mm^2. The circuit core consumes a quiescent current I_{DD} of about 25 µA. The printed circuit board (PCB), designed for the experimental setup, is depicted Fig. 4(c).

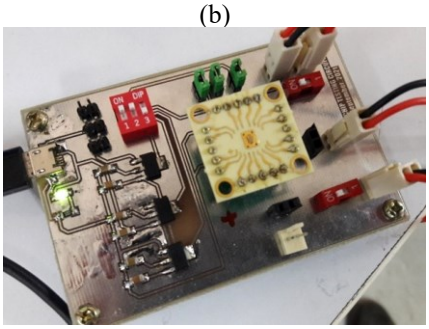
Table I summarizes the key components and the small-signal parameters of the amplifier, addressing the device sizes, transconductance of different stages, and the resistor and capacitors of the compensation network. The compensation capacitors collectively amount to 1 pF, and the compensation resistance, 35 kΩ. Unfortunately, directly measuring the amplifier's performance with zero C_L is impossible since inherent capacitances from the PCB, the packaging, the pads, and the probes cannot be avoided. These sources contribute a minimum capacitance of about 30 pF even without an external loading. Fig. 5(a) illustrates the simulated open-loop frequency response for the capacitive load from 100 nF down to 0. The DC gain is roughly about 115 dB for the entire C_L range. The average unity-gain frequency is 4.4 MHz, 2.3 MHz, and 79 kHz for no-load, 0.1 nF, and 100 nF load, respectively. Notably, the *GBW* product and C_L are inversely correlated across the specified C_L range. Fig. 5(b) presents the frequency response for C_L = 500 pF across various process corners, considering the variations in supply voltage and temperature. The OTA maintains stability throughout these corners, exhibiting minimum *GM* and *PM* of 10 dB and 45°, respectively.



(a)



(b)



(c)

FIGURE 4. A prototype fabricated in a 180-nm CMOS process; (a) Chip micrograph; (b) Layout; (c) The PCB designed for experiments.

TABLE I
TRANSISTORS DIMENSIONS AND SMALL-SIGNAL PARAMETERS

Stage	Device	W/L	Parameter	Value
#1	M_0	4.8 µ/0.9 µ	g_{m1}	16 µA/V
	$M_{1a}-M_{1b}$	6.9 µ/3.9 µ	g_{mC}	48 µA/V
	$M_{2a}-M_{2b}$	1.1 µ/1.0 µ		
	$M_{3a}-M_{3b}$	1.0 µ/5.5 µ		
	$M_{4a}-M_{4b}$	2.7 µ/0.2 µ		
	$M_{5a}-M_{5b}$	6.7 µ/0.2 µ		
#2	M_6	2.5 µ/0.2 µ	g_{m2}	90 µA/V
	M_{7a}	1.1 µ/2.6 µ		
	M_{7b}	3.3 µ/2.6 µ		
	M_8	3.2 µ/0.4 µ		
#3	M_9	24.0 µ/0.2 µ	g_{m3}	146 µA/V
	M_{10}	9.4 µ/0.2 µ	g_{mf}	117 µA/V
Comp. Network	C_D			300 fF
	R_D			35 kΩ
	C_{C1}			600 fF
	C_{C2}			100 fF

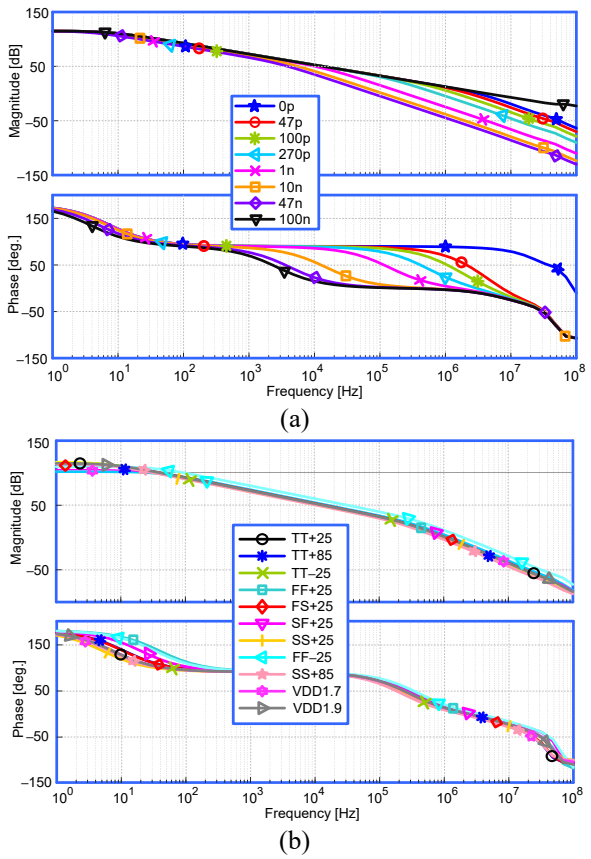


FIGURE 5. Simulated open-loop frequency response (a) against CL, (b) across different PVT corners.

Fig. 6 depicts the measured output settling behavior for external loads ranging from 100 nF down to 0. The amplifier was configured as a buffer with an input step voltage of 400 mV. The "<30 pF>" symbol represents the approximated inherent capacitance from the measuring system, excluding the output loading. The amplifier remains stable with any C_L tested. The 1% settling times averaged 2.41 µs for 100 pF and 40 µs for 47 nF external capacitive loads, respectively.

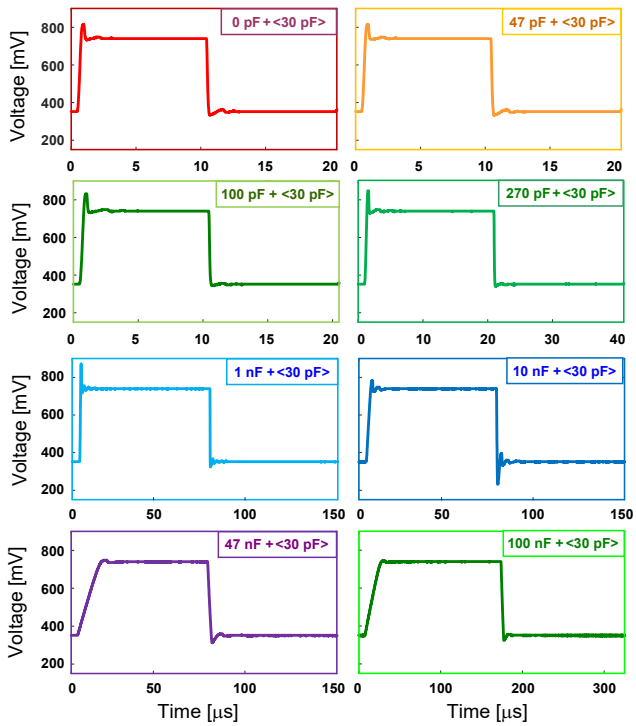


FIGURE 6. Measured large-signal settling response from zero to 100-nF load capacitor.

Table II presents a summary of the performance metrics and provides a comparison with the results from some of the recently published three-stage amplifiers. The average 1% small-signal settling time of the proposed OTA were measured as 0.018, 0.017 and 0.19 µs for 0, 470 pF and 100 nF capacitive load, respectively, when the size of input step is set to 0.4 V. The FOM metrics defined under Table 2 evaluate the large- and small-signal performance of different combinations depending on the interactions between area, quiescent current (I_{DD}), slew-rate (SR), bandwidth, and maximum to minimum C_L ratio ($C_{L,max}$ /$C_{L,min}$) [22, 44, 51]. The FOMs have been determined for maximum C_L of other configurations, and for the suggested OTA under 0, 470 pF and 100 nF external loading. In the case of $LR\text{-}IFOM_{LA}$ and $LR\text{-}IFOM_{SA}$, the proposed amplifier outperforms competing topologies by producing infinite values, a result of achieving unlimited $C_{L,max}$ /$C_{L,min}$. However, this comes at the cost of increased silicon area and more power consumption required for Q−factor control through implementation of the LIA and feedback networks, yielding inferior $IFOM_S$, $IFOM_L$, $IFOM_{SA}$, $IFOM_{LA}$ when compared to the solutions with limited C_L range. The total compensation capacitance appears to be twice that of the three-stage amplifier discussed in [44]. However, reducing the minimum drivable C_L from 5 nF to 0 nF comes at the cost of almost 4× consuming current.

TABLE II.
COMPARISON OF THE PROPOSED AMPLIFIER WITH PRIOR ART

	2016 [22]	2018 [44]	2020 [51]	2022 [52]			This work		
Process [nm]	350	350	130	65			180		
Area [mm^2]	0.003	0.0025	0.006	0.0028			0.0055		
I_{DD} [µA]	25	6.4	185	13.1			25*		
A_0 [dB]	>100	113	72	100			~115*		
Total C_C [pF]	1	0.5	0	1			1		
C_L [nF]	5–15	5–100	4.45–50	0.0	0.5	100	0.0	0.47	100
$C_{L,max}$ / $C_{L,min}$	3.0	20.0	11.3	∞			∞		
1% t_S [µs]	0.63–0.93	2.0–7.7	0.28–4.62	0.62**	6.3**	16.8**	1.8	1.7	19
GBW [MHz]	2.85–2.38	2.88–0.43	5.41–0.46	18.69	0.705	0.022	4.40*	1.12*	0.079*
SR [V/µs]	0.76–0.30	0.360–0.045	0.49–0.04	3.52	0.60	0.0044	1.60	1.60	0.021
$IFOM_S$ (1)	1'433.7	6'761	124.3	0	26.97	168	0	21.06	316
$IFOM_L$ (2)	180.7	707.6	10.81	0	22.95	33.66	0	30.08	84.00
$IFOM_{SA}$ (3)	482.7	2'704'403	20'721	0	9'632	60'104	0	3'828	57'455
$IFOM_{LA}$ (4)	60.8	283'019	1'801	0	8'196	12'021	0	5'469	15'273
$LR\text{-}IFOM_{SA}$ (5)	1'448.1	54'088'060	232'904	∞			∞		
$LR\text{-}IFOM_{LA}$ (6)	182.4	5'660'380	20'243	∞			∞		

* Simulated results ; ** Small-signal settling time with an input step amplitude of 0.1 V.

$$^{(1)}\ IFOM_S = \frac{GBW \cdot C_{L,\max}}{I_{DD}}\left[\frac{MHz \cdot pF}{\mu A}\right] \quad ^{(2)}\ IFOM_L = \frac{SR \cdot C_{L,\max}}{I_{DD}}\left[\frac{V/\mu s \cdot pF}{\mu A}\right] \quad ^{(3)}\ IFOM_{SA} = \frac{GBW \cdot C_{L,\max}}{I_{DD} \cdot Area}\left[\frac{MHz \cdot pF}{\mu A \cdot mm^2}\right]$$

$$^{(4)}\ IFOM_{LA} = \frac{SR \cdot C_{L,\max}}{I_{DD} \cdot Area}\left[\frac{V/\mu s \cdot pF}{\mu A \cdot mm^2}\right] \quad ^{(5)}\ LR-IFOM_{SA} = \frac{GBW}{I_{DD} \cdot Area} \cdot \frac{C_{L,\max}}{C_{L,\min}}\left[\frac{MHz}{\mu A \cdot mm^2}\right] \quad ^{(6)}\ LR-IFOM_{LA} = \frac{SR}{I_{DD} \cdot Area} \cdot \frac{C_{L,\max}}{C_{L,\min}}\left[\frac{V/\mu s}{\mu A \cdot mm}\right]$$

The OTA outlined in [51] is unique in that it eliminates the need for a Miller capacitor. Nonetheless, its consuming current is significantly higher than this study (185 µA vs. 25 µA) and any other topology listed in Table II. Additionally, both $C_{L,\max}$ /$C_{L,\min}$ and the DC gain fall short when compared to the configuration proposed in this work.

V. CONCLUSION

Multistage amplifiers face significant stability challenges when dealing with a wide range of capacitive loads. This complexity arises from varying position of the poles and zeros, which are directly influenced by C_L. A modified frequency compensation scheme has been introduced, aiming at stabilizing a three-stage amplifier without imposing a C_L limit. The approach incorporates a hybrid compensation loop, featuring dual Miller capacitors in series with embedded current buffers. A hybrid feedback network is also introduced from the second stage to the first stage, strategically adjusting the Q−factor of non-dominant poles for enhanced stability across a broad C_L range. It was analytically proved that the proposed OTA design offers significantly large load drivability, particularly with the new hybrid feedback scheme and the LIA network included. Fabrication of the proposed amplifier is accomplished in a standard 180-nm CMOS technology, and its operation was tested and compared to classical approaches. The results demonstrated improved small- and large-signal figure-of-merits, considering limitless capacitive load drivability range.

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